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**On the Conception and Analysis of a 12 GHz Push-Push Phase
Locked Dielectric Resonator Oscillator for Broadband Wireless
Applications**

A dissertation submitted in partial satisfaction of the
requirements for the degree

Master of Engineering (M.Eng.)

in

Electrical Engineering

by

Jean-François Gravel, B.Eng.

July 2003

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Abstract

On the Conception and Analysis of a 12 GHz Push-Push Phase Locked
Dielectric Resonator Oscillator for Broadband Wireless Applications

by

Jean-François Gravel, B.Eng.

PHASE Locked Dielectric Resonator Oscillators *PLDROs* have been in use in the wireless industry since early 1970s. They provide stable low phase noise local oscillators for microwave and millimeter wave radios. Reliability and cost are the two main inconveniences of standard PLDROs. Actually, PLDROs are an expensive solution due principally to the difficulty of producing them in high volume. The standard PLDRO is a high performance solution that needs to be modified in order to increase reliability and enter mass production processes. The modified PLDRO approach presented in this work has several advantages that are intended to increase reliability of the standard PLDRO. The modified PLDRO targets a higher phase detection sensitivity by the use of an intermediate frequency and a "Push-Push" DRO design that reduces oscillator sensitivity to components and manufacturing variations. Research results indicate that the modified PLDRO has excellent phase detector sensitivity, saturated output power, phase noise performance and frequency stability. The modified PLDRO has the same acquisition bandwidth as its DRO tuning bandwidth and the push-push DRO fundamental is rejected by 47 dBc.

To Geneviève, Isaac and Olivier.

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On the Conception and Analysis of a 12 GHz Push-Push Phase Locked
Dielectric Resonator Oscillator for Broadband Wireless Applications

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Chapter 1

Introduction

THE wireless industry is poised to be the next wave in the telecom industry following the optical boom. Indeed, broadband optical networks have been installed during the late 90s across the globe incurring an incommensurable spending spree. While some of those investments were profitable, most of them did not cope with expectation of high double digit profits. A major issue limiting profit of optical network providers was their incapacity to fill their available bandwidth. Consequently, it was difficult to get enough recurring monthly dues to pay for their initial investments and make expected profits.

Optical network providers could afford to connect businesses, educational sector, commercial centers and government agencies because of the considerable user density for a given connection. Then, it was worthwhile to excavate for laying fiber. But, the really huge market was the residential connectivity. Residential fiber connection, at low cost, would have been their "salut" to become profitable. Obviously, trenching a fiber to each residence was too costly and users would probably not have

paid an exorbitant monthly fee for the broadband home fiber connectivity.

A probable and effective solution to resolve the residential access lacuna, is to provide a wireless instead of an optical access. The bandwidth available is not of the magnitude of an optical connection but, probably, more than enough for immediate and future residential needs. A major and well known issue of external microwave wireless connections is their proven unreliability in the industry. Indeed, wireless links have a tendency to fail because their microwave carrier has become unstable due to different climatic conditions over time. A typical wireless link could also fail for other electrical reasons or link budget issues, such as, a lossier transmitting channel due to rain for example.

1.1 Goal of Research

The goal of this research work is to design and to present the performances of a microwave fixed frequency local oscillator (*LO*) that minimize wireless link failures due to an unstable LO, while providing excellent phase noise to use higher order modulation schemes. Usually, microwave oscillators, that exhibit excellent phase noise, are sensitive to electrical and physical parameter changes and make them likely to fail over a period of time. Many topology approaches can be undertaken to minimize the risk of LO link failures.

The author has chosen a modified phase locked dielectric resonator oscillator (*PLDRO*) to be designed and ruggedized for use as a reliable fixed frequency microwave LO. Figure 1.1 presents the modified PLDRO complete block diagram and Table 1.1, the notable differences that should improve the modified PLDRO reliability compared to a standard PLDRO.

Figure 1.1. Complete push-push PLDRO block diagram

1.2 Thesis Outline

Chapter 2 discusses basic phase locked loop (*PLL*) theory and is intended for readers who have limited knowledge of PLL systems, or people that once were familiar with PLL and just need a review of the theory. Since the intention here is not to reinvent PLL theory, the bulk of Chapter 2 theory follows from "Alain Blanchard, Phase-Locked Loops", a well written text book on PLLs.

Chapter 3 discusses the push-push dielectric resonator oscillator (*DRO*) design, implemented in the modified PLDRO. An analysis of the $TE_{01\delta}$ dielectric

	Standard PLDRO	Modified PLDRO
Resonator	F_o Dielectric Disk	$0.5 \cdot F_o$ Dielectric Disk
VCO Design	Feedback/Series Coupled	Push-Push Series Coupled
Phase Detection	Sampling Phase Detector	IF Frequency Mixer
Phase Detector Gain	Minimal	Excellent
Stability	Reference Dependent	Reference Dependent
Acquisition Bandwidth	Low	High
Phase Noise Performances	Excellent	Excellent
Likelihood to Unlock	High	Low

Table 1.1. Standard PLDRO versus modified PLDRO

resonator (DR) electromagnetic fields is presented as well as the push-push oscillator design, along with its expected and measured frequency spectrum and phase noise.

Chapter 4 discusses the reference multiplier design used to lock the DRO. A step recovery diode (SRD) multiplier analysis is presented. The crystal oscillator (XO) reference phase noise and stability are discussed along with its multiplied phase noise. The frequency multiplier, predicted and actual phase noise performances and output spectrum are also shown and discussed.

Chapter 5 discusses the loop filter topology chosen with its calculated and implemented parameters. The phase detector (PD) sensitivity K_1 and the dielectric resonator oscillator modulation sensitivity K_3 are measured to compute the closed loop parameters. The sub-circuits designed to render the push-push PLDRO "radio functional" are presented with simulated and measured data.

Chapter 6 discusses the push-push PLDRO closed loop performance with an accent on various frequency spectrums, phase noise plot comparisons, and integrated phase noise. The PLDRO tracking, acquisition bandwidth and mechanical tuning

bandwidth are also discussed and measured.

Chapter 7 concludes the thesis work and discusses final observations.

1.3 Contribution

A major challenge in the design of a PLDRO is not to simply lock the DRO to a reference to prove the PLL concept. This has been done often. Where the design challenge still stands is, to make it in such a way that it is volume manufacturable, inexpensive and reliable in the field.

This thesis is intended to go a few steps further than the standard PLDRO, and to design a new PLDRO that will come much closer to the desired low cost manufacturable PLDRO. This objective is attained by the use of a modified PLDRO. The modified PLDRO uses a push-push approach that cuts the oscillator frequency by half and hence reduces its mechanical and electrical sensitivity. Also, the modified PLDRO topology is designed with a lower comparison frequency for phase detection instead of at the carrier frequency, as in commercial PLDROs. This provides better detector sensitivity and prevents D.C. offset imbalances from perturbing the loop over temperature. The push-push approach combined with a divide-by-4 circuit and a 3 GHz IF reference frequency improves the standard PLDRO reliability and achieves mass producible units.

Chapter 2

Phase Locked Loop Fundamentals

2.1 Introduction

The phase locked loop (*PLL*) is a feedback system in which the phase of the output signal has to track the phase of the input signal. Consequently, in a normal application mode, the PLL output frequency is locked to the input frequency. There are many applications of a PLL such as tracking filters, phase and frequency demodulation, frequency synthesis, and carrier and clock recovery. The first known application of the PLL was in 1932, for the synchronous detection of radio signals [1].

The PLL equations can become complex in presence of noise, non-linearities and transients. The main objective is to give the fundamentals of PLL theory without getting lost in the depths of mathematics. The present chapter will therefore give enough analog PLL information to follow through the next chapters, and thus limits

complex PLL equation derivations.

2.2 Phase Locked Loop Building Blocks

A standard analog PLL has three fundamental building blocks. A phase detector (*PD*), a voltage controlled oscillator (*VCO*) and a loop filter ($F(s)$). These elements are required to lock the PLL output to an input frequency. More advanced topologies may include a prescaler, divide-by-*N* and gain blocks. Figure 2.1 presents the classic PLL topology.

Figure 2.1. PLL building blocks

From Figure 2.1, the basic PLL behavior can be explained without further investigations. The objective is to lock the output signal $y_o(t)$ to an input signal $y_i(t)$. Initially, both signals are out of synchronism.

$$y_i(t) = A \cos(\omega_i t + \theta_i) \quad (2.1)$$

$$y_o(t) = B \cos(\omega_o t + \phi_o) \quad (2.2)$$

Assuming a sinusoidal phase detector, the error signal out of the PD is expressed as,

$$u_1(t) = K_1 \cos[(\omega_i - \omega_o)t + \theta_i - \phi_o] \quad (2.3)$$

The error signal u_1 presents a sinusoidal waveform of amplitude K_1 , also known as the "Beat Note", when both signals have different angular frequencies. In order to have a null output from the PD, frequency synchronism has to be achieved, while θ_i and ϕ_o need to be in quadrature. The phase detector sensitivity K_1 is expressed in Volts per rad (V/rad). At $t=0$, the command voltage u_2 is applied to the VCO. After a short period of time, when all the transients have vanished, the PLL has synchronized the output signal $y_o(t)$ to the reference input signal $y_i(t)$. Now, $y_o(t)$ can be expressed as,

$$y_o(t) = B \cos(\omega_i t + \psi_o) \quad (2.4)$$

and the initial VCO phase ϕ_o has become a linear function of time [2].

$$\phi_o = (\omega_i - \omega_o)t + \psi_o \quad (2.5)$$

The loop filter allows the PD output signal u_1 , which is now a D.C. signal, to command the VCO. Indeed, when both frequencies are in synchronism, the time varying function cancels out and only a D.C. component remains. The loop filter transfer function $f(t)$ evaluated at D.C. is unity and frequency independent.

$$u_2 = u_1 * f(t) = K_1 \cos(\theta_i - \psi_o) \quad (2.6)$$

Considering the VCO instantaneous angular frequency ω_{inst} to be a perfect linear function of the command signal u_2 around the central angular frequency ω_o ,

$$\omega_{inst} = \frac{d}{dt}(\omega_o t + \phi_o) = \omega_o + K_3 u_2 \quad (2.7)$$

thus,

$$\frac{d}{dt}(\phi_o) = K_3 u_2 \quad (2.8)$$

where K_3 is the VCO proportionality constant expressed in radian per second per volt ($rad/s/V$). By combining Equations 2.5 and 2.6 into 2.8, we get,

$$\omega_i - \omega_o = K_1 K_3 \cos(\theta_i - \psi_o) \quad (2.9)$$

and the locked output phase ψ_o is then,

$$\psi_o = \theta_i - \arccos\left[\frac{\omega_i - \omega_o}{K_1 K_3}\right] \quad (2.10)$$

From Equation 2.9, if the $K_1 K_3$ product is much lower than the initial frequency offset $\omega_i - \omega_o$, the phase difference between the input $y_i(t)$ and the output $y_o(t)$ converges toward $\pi/2$. By combining Equations 2.6, 2.9 and 2.10, the error signal u_1 can be conveniently expressed as,

$$u_1 = \frac{\omega_i - \omega_o}{K_3} \quad (2.11)$$

2.2.1 Phase Detector

In a PLL system, the phase detector (PD) is used to detect phase error between the input signal $y_i(t)$ and the output signal $y_o(t)$. While there are various PD types on the market, they fall mainly into three categories, related to the maximum linear phase detection without sign reversal.

- Sinusoidal $\implies$ Phase detection of $1/2$ rad;
- Triangular $\implies$ Phase detection of π rad;
- Sawtooth $\implies$ Phase detection of 2π rad.

A double-balanced bridge or "ring modulator" is a typical diode arrangement for phase detection purposes. This PD detects phase difference between the LO drive and the RF signal linearly for a period approximately of $1/2$ rad, whether on the positive or negative slope of the phase detection. For our phase detection analysis, the double-balanced bridge operation is detailed. Figure 2.2 shows a typical diode arrangement with a symmetry line that separate the phase detector right and left hand side (*RHS* and *LHS* respectively).

Figure 2.2. Double-balanced bridge or "ring modulator"

Generators E_s and $-E_s$ are presumed to have zero internal impedance, generators E_r and $-E_r$ have an internal impedance of value R and ideal diodes are assumed. Consequently, when a diode is forward biased, the voltage drop across the element is null and the potential seen at O is E_s or $-E_s$, depending on which diode conducts. If both diodes are forward biased, the voltage at point O is null and for the specific case where both diodes are reverse biased, the potential at point O is $-E_r$. Potentials at points A and A' are independent of diode conduction conditions. Therefore, potentials at point O and O' are independent as well. The circuit

Case	D_1'	D_2'	Limit Conditions	V_o'
1	Off	Off	$E_s > E_r$ and $-E_s < E_r$	E_r
2	On	Off	$E_s \leq E_r$ and $-E_s < 0$	E_s
3	Off	On	$E_s > 0$ and $-E_s \geq E_r$	$-E_s$
4	On	On	$E_s \leq 0$ and $-E_s \geq 0$	0

Table 2.1. RHS conduction limits D_1' and D_2'

Case	D_1	D_2	Limit Conditions	V_o
1	Off	Off	$E_s < E_r$ and $-E_s > E_r$	$-E_r$
2	On	Off	$E_s \geq E_r$ and $-E_s > 0$	$-E_s$
3	Off	On	$E_s < 0$ and $-E_s \leq E_r$	E_s
4	On	On	$E_s \geq 0$ and $-E_s \leq 0$	0

Table 2.2. LHS conduction limits D_1 and D_2

RHS and LHS can then be analyzed independently to provide phase detection from $0 \leq \omega t \leq T/2$ and $T/2 \leq \omega t \leq T$ respectively.

Tables 2.1 and 2.2 present diode conduction conditions for the double-balanced bridge RHS and LHS. The phase detector output voltage at potential O and O' can be plotted using the tabulated conditions. The bridge RHS and LHS develop a waveform for half a cycle each. The two waveforms are added together to form a "Beat Note" signal $v(t)$ of amplitude K_1 , having a fundamental frequency twice the comparison frequency. Figures 2.3 and 2.4 shows the bridge conduction cycles and the full detection waveform respectively.

The PD used for the push-push PLDRO has a sinusoidal output waveform generated by a double-balanced bridge or "ring modulator". While it has inconveniences when used with broadband tunable VCOs, this passive PD is likely to outperform others in a low noise fixed frequency environment. The $1/2$ rad linear phase detection limit is not a major issue, considering that the push-push PLDRO

Figure 2.3. RHS and LHS phase detector output waveform

Figure 2.4. Complete phase detector output waveform

is a fixed frequency source with limited tuning bandwidth.

2.2.2 Loop Filter

Another important block in a PLL is the loop filter $F(j\omega)$, it is located between the PD output and the VCO input. The loop filter can be either active or completely passive depending on the application or performances to be met. The loop filter transfer function $F(j\omega)$ is the ratio of the VCO command signal U_2 to the

PD error signal U_1 ,

$$F(j\omega) = \frac{U_2(j\omega)}{U_1(j\omega)} \quad (2.12)$$

The simplest loop filter is an "all-pass" filter. This filter is basically a transmission line that connect the PD to the VCO and known as a first order loop PLL. Figure 2.5 shows the "all-pass" filter and Equation 2.13, its associated transfer function.

Figure 2.5. All-pass filter

$$F(j\omega) = 1 \quad (2.13)$$

A basic LPF can also be used as a loop filter. The LPF filter adds a second pole to the loop transfer function. While being an advantage, this filter does not provide the degree of freedom required to fully control a second order transfer function. The LPF filter adds a pole to the loop but provides a single adjustment parameter τ_1 . Hence, this reduces considerably the fundamental parameter adjustment for a second order loop, the damping factor ζ and the natural angular frequency ω_n . Figure 2.6 shows a basic LPF and Equation 2.14, its associated transfer function.

$$F(j\omega) = \frac{1}{1 + j\omega\tau_1} \quad (2.14)$$

Figure 2.6. Passive LPF

A passive LPF with phase lead correction is often used, this filter has a series resistor with the capacitor to provide two degrees of freedom τ_1 and τ_2 to fully control a second order loop. Figure 2.7 shows the LPF with phase lead correction network and Equation 2.16, its associated transfer function.

Figure 2.7. LPF with phase lead correction network

$$F(j\omega) = \frac{1 + j\omega R_2 C}{1 + j\omega(R_1 + R_2)C} \quad (2.15)$$

$$= \frac{1 + j\omega\tau_2}{1 + j\omega\tau_1}, \quad (2.16)$$

where, $\tau_1 = (R_1 + R_2)C$ and $\tau_2 = R_2C$.

An active LPF with phase lead correction is also commonly used, this filter behaves somewhat like the LPF with phase lead correction but it adds gain G to the loop. This characteristic is welcome when the PD sensitivity is low. If an operational amplifier is used as an active device, the open loop D.C. gain is in the neighborhood of $G \approx 100 \text{ dB}$. Figure 2.8 shows the active LPF with phase lead correction network and Equation 2.19, its associated transfer function.

Figure 2.8. Active LPF with phase lead correction network

$$F(j\omega) = -\frac{1}{R_1} \left\{ \frac{1}{R_2 + 1/j\omega C} + \frac{1}{G} \left(\frac{1}{R_1} + \frac{1}{R_2 + 1/j\omega C} \right) \right\}^{-1} \quad (2.17)$$

$$= -G \frac{1 + j\omega R_2 C}{1 + j\omega(R_1 + GR_1 + R_2)C} \quad (2.18)$$

$$= -G \frac{1 + j\omega\tau_2}{1 + j\omega\tau_1}, \quad (2.19)$$

where, $\tau_1 = (R_1 + GR_1 + R_2)C$ and $\tau_2 = R_2C$.

If the amplifier gain G is large and if the output phase relationship with the reference signal is not an important factor (i.e. the output can lead or lag the input by $\pi/2$), the negative sign can be disregarded. The PD will detect the phase on the positive or negative sign slope. Then, Equation 2.20 can be used as a simplified version of Equation 2.19,

$$F(j\omega) \simeq \frac{1 + j\omega\tau_2}{j\omega\tau_1}, \quad (2.20)$$

where, $\tau_1 = R_1C$ and $\tau_2 = R_2C$.

2.2.3 Voltage Controlled Oscillator

An ideal voltage controlled oscillator (*VCO*) is a device where the output frequency would represent a constant amplitude delta Dirac function $\delta(\omega)$ along with an infinite frequency tuning bandwidth controlled by a voltage signal. Obviously, such devices do not exist and probably never will. A real VCO has tuning frequency limitations as well as phase noise around the carrier. Generally speaking, an oscillator with a high loaded quality factor Q_L has reduced phase noise, and is harder to tune its output frequency. Of course, there are circuits like the yttrium iron garnet (*YIG*) oscillator that presents octave tuning bandwidth while having phase noise equivalent to a DRO. However, the YIGs have others physical issues like sensitivity to microphonics and higher power consumption than a standard VCO or a DRO for instance. The main properties required for a VCO to operate in a PLL environment are as follows:

- An adequate center frequency stability ω_o ;
- Tuning bandwidth as wide as the synchronization bandwidth $\pm K$;
- Tuning linearity preferably within $\pm 5\%$;
- Minimal phase jitter around the carrier.

Characterizing a VCO in a PLL environment is trivial. The VCO has an frequency output ω_{inst} proportional to the D.C. input u_2 . Equation 2.21 is the instantaneous angular frequency ω_{inst} at the VCO output,

$$\omega_{inst} = \omega_o + K_3 \cdot u_2, \quad (2.21)$$

where ω_o is the center frequency, K_3 the modulation sensitivity constant in $(rad/s/V)$ and u_2 the command voltage.

While being trivial in PLL analysis, the VCO design is still an intense research area. Often, VCO research is directed to produce a wide tuning bandwidth with the lowest phase noise possible. The topology chosen here for the PLDRO prototype is a push-push DRO. This oscillator has a limited tuning bandwidth with good phase noise performances. The push-push PLDRO is intended to be used as a fixed frequency LO. Thus, tuning bandwidth is required only for tracking purposes. Consequently, there is no need for tuning over several hundreds of MHz.

2.3 Phase Locked Loop Linear Operation

This section derives the main PLL equations from the general non-linear case to the more frequently used linear equations. Then, the loop stability is investigated for an active LPF with phase lead correction network. To complete the section, the PLL behavior to disturbances is analyzed for two different input stimulus. The fixed frequency operation of the PLDRO requires basic understanding of the PLL behavior for a phase step θ and a frequency step disturbance $\Delta\omega$. The input stimulus analysis is done for the active loop filter with phase correction network as in the loop stability subsection.

The sinusoidal phase detector generates a time domain error signal $u_1(t)$ as follows,

$$u_1(t) = K_1 \sin(\phi_i(t) - \phi_o(t)) \quad (2.22)$$

the loop filter time domain impulse response is the Fourier transform of its frequency domain transfer function,

$$f(t) = \int_{-\infty}^{+\infty} F(j\omega) \cdot e^{j\omega t} d\omega \quad (2.23)$$

the VCO command voltage $u_2(t)$ is found by convoluting the filter impulse response with the command voltage $u_1(t)$,

$$u_2(t) = K_2 u_1(t) * f(t) = K_2 \int_{-\infty}^{+\infty} u_1(\tau) \cdot f(t - \tau) d\tau. \quad (2.24)$$

The VCO output phase ϕ_o time derivative is from Equation 2.8,

$$\frac{d\phi_o}{dt} = K_3 u_2(t). \quad (2.25)$$

To get the general time domain equation that governs a PLL using a sinusoidal phase detector, we combine equations 2.22, 2.24 and 2.25,

$$\frac{d\phi_o}{dt} = K [\sin\{\phi_i(t) - \phi_o(t)\}] * f(t), \quad (2.26)$$

where $K = K_1 K_2 K_3$ and is known as the PLL synchronization bandwidth.

Equation 2.26, although fully characterizing a PLL with a sinusoidal phase detector, is not easy to handle, particularly with the convolution operator. If we assume the instantaneous phase error $\phi(t)$ quantity to be small (i.e. the phase deviation is within 1/2 rad.), the sine function can be linearized,

$$\sin\{\phi_i(t) - \phi_o(t)\} \approx \phi_i(t) - \phi_o(t) \quad (2.27)$$

In engineering, when possible, we prefer working in frequency domain instead of time domain because the expressions are easier to manipulate. So, we can

apply the Fourier transform to each member of Equation 2.26 to replace the convolution operator by a simple product,

$$j\omega\Phi_o(j\omega) = K[\Phi_i(j\omega) - \Phi_o(j\omega)] \cdot F(j\omega) \quad (2.28)$$

and rearrange Equation 2.28 into a transfer function form,

$$H(j\omega) = \frac{\Phi_o(j\omega)}{\Phi_i(j\omega)} = \frac{KF(j\omega)}{j\omega + KF(j\omega)}. \quad (2.29)$$

The error transfer function, can be found by inserting $\Phi_o(j\omega) = \Phi_i(j\omega) - \Phi(j\omega)$ into Equation 2.28 and rearranging to get,

$$1 - H(j\omega) = \frac{\Phi(j\omega)}{\Phi_i(j\omega)} = \frac{j\omega}{j\omega + KF(j\omega)}. \quad (2.30)$$

One may be inclined to substitute the steady state variable ($j\omega$) by a more general variable (s) that includes the transient performance ($s = \sigma + j\omega$). Then, the transfer and error functions become,

$$H(s) = \frac{\Phi_o(s)}{\Phi_i(s)} = \frac{KF(s)}{s + KF(s)} \quad (2.31)$$

and

$$1 - H(s) = \frac{\Phi(s)}{\Phi_i(s)} = \frac{s}{s + KF(s)}. \quad (2.32)$$

The previous two equations are the general linearized transfer and error functions that fully characterize a linear PLL with a general loop filter $F(s)$. The filter can be designed as needed to achieve the desired performance. One just has to compute the filter transfer function $F(s)$ and set the loop gain K . A case of interest for the PLDRO application is an active loop filter with a phase lead correction network. If we assume that G is in the neighborhood of 100 dB the approximation

operator " $\approx$ " from Equation 2.20 can be replaced by the equation operator " $=$ " and the filter transfer function becomes

$$F(s) = \frac{U_2(s)}{U_1(s)} = \frac{1 + s\tau_2}{s\tau_1} \quad (2.33)$$

where, $\tau_1 = R_1C$ and $\tau_2 = R_2C$.

The frequency domain transfer and error functions are found by inserting $F(s)$ from (2.33) into equations 2.31 and 2.32,

$$H(s) = \frac{\Phi_o(s)}{\Phi_i(s)} = \frac{KF(s)}{s + KF(s)} = \frac{K\tau_2s + K}{\tau_1s^2 + K\tau_2s + K} \quad (2.34)$$

$$1 - H(s) = \frac{\Phi(s)}{\Phi_i(s)} = \frac{s}{s + KF(s)} = \frac{\tau_1s^2}{\tau_1s^2 + K\tau_2s + K} \quad (2.35)$$

and its time domain equivalent can be found by using the inverse Fourier transform,

$$\tau_1 \frac{d^2\phi_o}{dt^2} + K\tau_2 \frac{d\phi_o}{dt} + K\phi_o(t) = K\tau_2 \frac{d\phi_i}{dt} + K\phi_i(t) \quad (2.36)$$

$$\tau_1 \frac{d^2\phi}{dt^2} + K\tau_2 \frac{d\phi}{dt} + K\phi(t) = \tau_1 \frac{d^2\phi_i}{dt^2}. \quad (2.37)$$

It should be remembered that these equations are only valid when the phase error $\phi(t)$ is small. When the phase error becomes larger and the sine approximation become less accurate, one should use the general transfer and error function shown below:

$$\tau_1 \frac{d^2\phi_o}{dt^2} = K \sin[\phi_i(t) - \phi_o(t)] + K\tau_2 \cos[\phi_i(t) - \phi_o(t)] \left\{ \frac{d\phi_i}{dt} - \frac{d\phi_o}{dt} \right\} \quad (2.38)$$

and

$$\tau_1 \frac{d^2\phi}{dt^2} + K\tau_2 \cos(\phi(t)) \frac{d\phi}{dt} + K \sin(\phi(t)) = \tau_1 \frac{d^2\phi_i}{dt^2}. \quad (2.39)$$

From equations 2.38 and 2.39, we find the linearized (i.e considered linear if the phase error is or smaller than $1/2$ rad.) time domain equations if $\{\sin[\phi_i(t) - \phi_o(t)]\}$ and $\{\cos[\phi_i(t) - \phi_o(t)]\}$ are approximated by $\{\phi_i(t) - \phi_o(t)\}$ and $\{1\}$ respectively.

The linearized frequency domain transfer and error function can be rewritten in a typical second order servo-loop form by dividing numerator and denominator by τ_1 ,

$$H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (2.40)$$

and

$$1 - H(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (2.41)$$

where, $\omega_n^2 = K/\tau_1$ and $2\zeta\omega_n = K\tau_2/\tau_1$.

2.3.1 Loop Stability

When a PLL operates in its linear region, general servo-loop stability criteria are most of the time sufficient to predict whether the PLL is in a stable operation mode. The PLL open loop transfer function H_o is found by multiplying the synchronization bandwidth K by $F(j\omega)/j\omega$. The integration by " $j\omega$ " is from the VCO frequency to phase conversion to keep the system phase consistent,

$$H_o(j\omega) = \frac{KF(j\omega)}{j\omega} \quad (2.42)$$

To get the open loop transfer function H_o for the active loop filter with phase lead correction network, we insert $F(j\omega)$ from Equation 2.20 into Equation 2.42,

$$H_o(j\omega) = \frac{K(1 + j\omega\tau_2)}{\tau_1(j\omega)^2} \quad (2.43)$$

The magnitude of $|H_o(j\omega)|$ crosses the 0 dB axis at $K\tau_2/\tau_1$ or equivalently at $2\zeta\omega_n$ when $\omega\tau_2 \gg 1$. The loop natural angular frequency ω_n is determined by $(K/\tau_1)^{1/2}$ and it corresponds to the point where $|H_o(j\omega)|$ would cross the 0 dB axis if the phase

lead correction network were omitted. The phase margin θ_m can be computed using $H_o(j\omega)$ evaluated at $2\zeta\omega_n$:

$$\theta_m = \angle\{H_o(j\omega)|_{\omega=2\zeta\omega_n}\} = \arctan\left(\frac{2\zeta\omega_n}{1}\right) + \arctan\left(\frac{2\zeta\omega_n}{1}\right) - \arctan\left(\frac{2\zeta\omega_n\tau_2}{1}\right) \quad (2.44)$$

In order to be stable, the phase shift introduced by $H_o(j\omega)$ has to be smaller than 180 degrees when the open loop transfer function module is evaluated at $2\zeta\omega_n$ or 0 dB point. For the active loop filter with phase lead correction, this condition is fulfilled with a good phase margin if, $\omega_n > 1/\tau_2$. Spurious induced phase shifts from the VCO and/or the PD are generally not impeding the loop stability because their time constants are usually much smaller than τ_2 . Consequently, they are omitted in Equation 2.44. For more advanced techniques on PLL stability one may refer to [1]. Figure 2.9 shows the modulus and phase plot of $H_o(j\omega)$ for the discussed loop filter.

Figure 2.9. Open loop transfer function with active filter and phase lead network

2.3.2 PLL Response to Disturbances

In this subsection, the PLL behavior is analyzed for a phase step θ and a frequency step $\Delta\omega$. These perturbations are often encountered in a fixed frequency application like a PLDRO. Indeed, when the PLDRO is synchronized, the odds that a phase "glitch" or "pop" from the reference or a frequency jump from the DRO will occur cannot be underestimated and are likely to happen over time, especially under temperature variations. Thus, it is worthwhile to go through the analysis of these two disturbances in order to understand how the PLL behaves under such circumstances. The analysis is realized for the active loop filter with phase lead correction network. For a phase or frequency perturbation, the PLL has to maintain its linear behavior for the following equations to remain valid. The PLL is initially assumed to be locked and the following two equations describe the steady state operation,

$$y_i(t) = A \sin(\omega t) \quad (2.45)$$

$$y_o(t) = B \cos(\omega t). \quad (2.46)$$

Initially, at $t < 0$, the PLL is locked with the output signal $y_o(t)$ in quadrature with the input signal $y_i(t)$. At time $t > 0$, a perturbation $\phi_i(t)$ occurs on the input signal. Equations 2.45 and 2.46 become

$$y_i(t) = A \sin(\omega t + \phi_i(t)) \quad (2.47)$$

$$y_o(t) = B \cos(\omega t + \phi_o(t)). \quad (2.48)$$

Phase Step Response

Under a phase step perturbation the input disturbance $\phi_i(t)$ is described as $\theta\Upsilon(t)$, where θ is the phase step amplitude and $\Upsilon(t)$ is the unit step function and

can be rewritten in the frequency domain as

$$\Phi_s = \frac{\theta}{s}. \quad (2.49)$$

The error induced can be defined using the error function as

$$\frac{\Phi(s)}{\Phi_i(s)} = 1 - H(s) \quad (2.50)$$

then, the phase error can be found in terms of servo-loop parameters,

$$\Phi(s) = \{1 - H(s)\} \cdot \frac{\theta}{s} \quad (2.51)$$

$$= \frac{\tau_1 s \theta}{\tau_1 s^2 + K \tau_2 s + K} \quad (2.52)$$

$$= \frac{s \theta}{s^2 + 2\zeta \omega_n s + \omega_n^2}. \quad (2.53)$$

Using the inverse Laplace transform on Equation 2.53, leads to the time domain expression,

$$\phi(t) = \theta \frac{\omega_n \alpha e^{-\omega_n \alpha t} - \omega_n \beta e^{-\omega_n \beta t}}{\omega_n \alpha - \omega_n \beta} \quad (2.54)$$

where, $\alpha = \zeta - \sqrt{\zeta^2 - 1}$ and $\beta = \zeta + \sqrt{\zeta^2 - 1}$.

From Equation 2.54, three cases can be distinguished depending of the damping constant ζ value,

$$\zeta > 1, \quad \frac{\phi(t)}{\theta} = e^{-\zeta \omega_n t} [\cosh \omega_n (\sqrt{\zeta^2 - 1}) t - \frac{\zeta}{\sqrt{\zeta^2 - 1}} \sinh \omega_n (\sqrt{\zeta^2 - 1}) t] \quad (2.55)$$

$$\zeta = 1, \quad \frac{\phi(t)}{\theta} = e^{-\zeta \omega_n t} (1 - \omega_n t) \quad (2.56)$$

$$\zeta < 1, \quad \frac{\phi(t)}{\theta} = e^{-\zeta \omega_n t} [\cos \omega_n (\sqrt{1 - \zeta^2}) t - \frac{\zeta}{\sqrt{1 - \zeta^2}} \sin \omega_n (\sqrt{1 - \zeta^2}) t]. \quad (2.57)$$

Figure 2.10 shows the PLL behavior for different damping constant values for an active loop filter with phase lead correction network. The maximum allowable phase step θ is about 1/2 radian for a sinusoidal phase detector and is represented as $\phi/\theta = 1$ on the ordinate axis.

Figure 2.10. Phase step response for an active filter with phase lead network, from Blanchard [2].

Frequency Step Response

Under a frequency step perturbation the input disturbance $\phi_i(t)$ is described as $\Delta\omega \cdot t \cdot \Upsilon(t)$, where $\Delta\omega$ is the frequency step amplitude and $\Upsilon(t)$ is the unit step function and can be rewritten in the frequency domain as

$$\Phi_s = \frac{\Delta\omega}{s^2}. \quad (2.58)$$

The error induced can be defined using the error function as

$$\frac{\Phi(s)}{\Phi_i(s)} = 1 - H(s) \quad (2.59)$$

then, the frequency error can be found in terms of servo-loop parameters,

$$\Phi(s) = \{1 - H(s)\} \cdot \frac{\Delta\omega}{s^2} \quad (2.60)$$

$$= \frac{\tau_1 \Delta\omega}{\tau_1 s^2 + K\tau_2 s + K} \quad (2.61)$$

$$= \frac{\Delta\omega}{s^2 + 2\zeta\omega_n s + \omega_n^2}. \quad (2.62)$$

Using the inverse Laplace transform on Equation 2.62 leads to the time domain expressions for different damping constant values. Again, three cases can be distinguished depending of the damping constant ζ value,

$$\zeta > 1, \quad \frac{\phi(t) \cdot \omega_n}{\Delta\omega} = e^{-\zeta\omega_n t} \cdot \frac{\sinh \omega_n(\sqrt{\zeta^2 - 1})t}{\sqrt{\zeta^2 - 1}} \quad (2.63)$$

$$\zeta = 1, \quad \frac{\phi(t) \cdot \omega_n}{\Delta\omega} = e^{-\omega_n t} \cdot \omega_n t \quad (2.64)$$

$$\zeta < 1, \quad \frac{\phi(t) \cdot \omega_n}{\Delta\omega} = e^{-\zeta\omega_n t} \cdot \frac{\sinh \omega_n(\sqrt{1 - \zeta^2})t}{\sqrt{1 - \zeta^2}}. \quad (2.65)$$

Figure 2.11 shows the PLL behavior for different damping constant values for an active loop filter with phase lead correction network. The maximum allowed frequency step $\Delta\omega$ is about 1/2 rad/s for a sinusoidal phase detector and is represented as $\omega_n \phi / \Delta\omega = 1$ on the ordinate axis.

This loop topology has no steady state frequency or phase error for any damping constant value providing the transient overshoot does not cross the maximum phase error $\phi(t)$ linearity limit. If this happens, the system enters a non-linear zone and the previous equations are unapplicable. In such a case, the PLL may overcome the non-linearity and settle on the same PD slope, or it may lock onto the adjacent slope, depending on the phase or frequency deviation amplitude. If the phase or frequency deviation is too large, the PLL may break lock, and will then need to reacquire lock to the reference signal $y_i(t)$ as next discussed in section 2.4.

Figure 2.11. Frequency step response for an active filter with phase lead network, from Blanchard [2].

2.4 Natural Acquisition for a Second Order Loop

Most of the time, a PLL has to initially acquire a signal outside the linearity region of the sinusoidal phase detector. This implies that the linear equations of section 2.3.2 cannot be used to initially characterize the PLDRO behavior. In order to predict acquisition for a second order loop, one must use the fundamental PLL second order non-linear differential equations (Ref: Eq.2.38, Eq.2.39). These equations are difficult to manipulate and are analytically insoluble. However, analytical approximations and phase plane method exist to overcome such difficulties. In this section, the acquisition pattern is analyzed for two loop filters:

- Perfect integrator with phase lead correction network;
- LPF with phase lead correction network.

It is generally accepted [2] that the perfect integrator with phase lead correction network is very well approximated by the active filter with correction network. However, the approximation might not always be applicable for acquisition purposes. The following analysis demonstrates that the perfect integrator filter always acquires independently of the initial frequency offset Ω_o . In practice, where the integrator ideality is only an approximation, the PLL might not acquire the reference signal $y_i(t)$. Under such circumstances, the perfect integrator acquisition equations are not helpful to understand acquisition behavior. For this reason, even if the PLDRO uses an active loop filter, the acquisition equations for a passive LPF with phase lead correction are analyzed to provide tools to better understand the acquisition phenomenon.

The difference in angular frequency Ω between the PLL input and output can be related as,

$$\Omega = \omega_i - \omega_o - K_3 u_{20} \quad (2.66)$$

where u_{20} is the slowly varying or DC component of the command voltage.

As long as $\Omega > 2\zeta\omega_n$, the error signal u_{10} can be expressed as,

$$u_{10} = K_1 \frac{K\tau_2}{2\tau_1} \frac{1}{\Omega}. \quad (2.67)$$

The differential equations relating u_{10} and u_{20} for a perfect integrator and a passive LPF, both with phase lead correction, are respectively,

$$\tau_1 \frac{du_{20}}{dt} = K_2 \left[\tau_2 \frac{du_{10}}{dt} + u_{10} \right] \quad (2.68)$$

$$\tau_1 \frac{du_{20}}{dt} + u_{20} = K_2 \left[\tau_2 \frac{du_{10}}{dt} + u_{10} \right]. \quad (2.69)$$

Combining Equations 2.66, 2.67 and 2.68, we find the general differential equation governing Ω versus time,

$$dt = \left(\frac{\tau_2}{\Omega} - \frac{\tau_1 \Omega}{\alpha^2} \right) d\Omega \quad (2.70)$$

$$t - t_0 = \tau_2 \ln \Omega - \frac{\tau_1}{\alpha^2} \frac{\Omega^2}{2}. \quad (2.71)$$

At $t=0$, $\Omega = \Omega_o$ then,

$$t = \tau_2 \frac{(\Omega_o^2 - \Omega^2)}{(2\zeta\omega_n)^2} - \ln \frac{\Omega_o}{\Omega} \quad (2.72)$$

where Ω_o is the peak deviation from the reference. Then, the required acquisition time T_{acq} for the perfect integrator with phase lead correction network is,

$$T_{acq} = \tau_2 \left\{ \left(\frac{\Omega_o}{2\zeta\omega_n} \right)^2 - 1 - \ln \left(\frac{\Omega_o}{2\zeta\omega_n} \right) \right\} \quad (2.73)$$

when Ω_o becomes large, the last two terms of equation 2.73 can be neglected,

$$T_{acq} \approx \tau_2 \left(\frac{\Omega_o}{2\zeta\omega_n} \right)^2 = \frac{\Omega_o^2}{2\zeta\omega_n^3} \quad (2.74)$$

where, $\tau_2 = 2\zeta/\omega_n$.

Equation 2.74 shows that for a PLL with a perfect integrator with phase lead correction network, the system will always acquire the input signal $y_i(t)$ unless its peak frequency deviation is beyond the VCO tuning range. Figure 2.12 presents associated curves for Equation 2.72. Other means, like the phase plane method, can be used to find if acquisition takes place under small frequency offset circumstances. Equation 2.72 considers a perfect integrator. An ideal integrator is not implementable in practice and thus, the previous equation might not be of great interest if the PLL does not acquire the reference signal. Although, the PLDRO uses an active filter with phase lead correction and can often be approximated by the perfect integrator, the acquisition behavior might fall short of the approximation

Figure 2.12. Acquisition for perfect integrator, acquisition always takes place, from Blanchard [2].

solution and acquire more like a passive LPF with phase lead correction network. The following analysis provides tools to understand the acquisition concept if the "perfect integrator approximation" does not have an infinite acquisition bandwidth.

Combining Equations 2.66, 2.67 and 2.69, we find the general differential equation governing Ω versus time,

$$dt = \frac{\alpha^2 \tau_2 - \Omega^2 \tau_1}{\Omega^3 - \Omega_o \Omega^2 + \alpha^2 \Omega} d\Omega \quad (2.75)$$

$$t - t_o = \alpha^2 \tau_2 \int \frac{d\Omega}{\Omega(\Omega^2 - \Omega_o \Omega + \alpha^2)} - \tau_1 \int \frac{\Omega d\Omega}{\Omega^2 - \Omega_o \Omega + \alpha^2} \quad (2.76)$$

with $\alpha^2 = K^2 \tau_2 / 2\tau_1$ and Ω_o the initial ($t = 0$) angular frequency difference. There are two possible solutions depending on whether the denominator roots, $\Omega^2 - \Omega_o \Omega + \alpha^2$

are real or complex conjugate.

a) For real roots; $\Omega_o^2 > K^2(2\tau_2/\tau_1)$, Equation 2.76 can be reformulated as,

$$t = \tau_2 \ln \frac{\Omega}{\Omega_o} + \frac{\tau_1 + \tau_2}{2} \ln \frac{\alpha^2}{(\Omega - \Omega_1)(\Omega - \Omega_2)} + \frac{\Omega_o(\tau_2 - \tau_1)}{2\sqrt{\Omega_o^2 - 4\alpha^2}} \left[\ln \frac{\Omega - \Omega_1}{\Omega - \Omega_2} - \ln \frac{\Omega_2}{\Omega_1} \right] \quad (2.77)$$

Figure 2.13 shows plots of Ω versus time for the real roots denominator. If $|\Omega_o| > K\sqrt{2\tau_2/\tau_1}$, the PLL pulls the free-running frequency from Ω_o to Ω_1 . Equation 2.77 shows that as $t \rightarrow \infty$, frequency Ω is asymptotic to pole Ω_1 which, is close to $\Omega_o/2$ and the acquisition does not take place.

$$\Omega \rightarrow \Omega_1 = \frac{\Omega_o + \sqrt{\Omega_o^2 - 4\alpha^2}}{2} \quad (2.78)$$

Figure 2.13. Acquisition for real roots, acquisition does not take place, from Blanchard [2].

b) For complex conjugate roots; $\Omega_o^2 < K^2(2\tau_2/\tau_1)$, Equation 2.76 can be reformulated as,

$$t = \tau_2 \ln \frac{\Omega}{\Omega_o} + \frac{\tau_1 + \tau_2}{2} \ln \frac{\alpha^2}{\beta} + \frac{\Omega_o(\tau_2 - \tau_1)}{\gamma} \left[\arctan \frac{2\Omega - \Omega_o}{\gamma} - \arctan \frac{\Omega_o}{\gamma} \right] \quad (2.79)$$

where, $\beta = \Omega^2 - \Omega_o\Omega + \Omega + \alpha^2$ and $\gamma = \sqrt{4\alpha^2 - \Omega_o^2}$. If Ω_o is much larger than $K(\tau_2/\tau_1)$, acquisition time T_{acq} is considered complete when $\Omega = K(\tau_2/\tau_1)$ and approximated by,

$$T_{acq} \approx \frac{2(\tau_1 - \tau_2)\Omega_o}{\sqrt{4\alpha^2 - \Omega_o^2}} \arctan\left\{\frac{\Omega_o}{\sqrt{4\alpha^2 - \Omega_o^2}}\right\} + \frac{\tau_1}{2} \ln \frac{K}{K - 2\Omega_o} \quad (2.80)$$

and the limit condition for a possible or impossible acquisition of the reference signal is,

$$\Omega_o^2 < 4\alpha^2 = 2K^2 \frac{\tau_2}{\tau_1} = (2K)(K \frac{\tau_2}{\tau_1}) = 2K(2\zeta\omega_n - \frac{1}{\tau_1}) \quad (2.81)$$

and we can rewrite the peak frequency deviation Ω_o limit as,

$$|\Omega_o| < 2\sqrt{K(\zeta\omega_n + \frac{1}{2\tau_1})}. \quad (2.82)$$

Figure 2.14 shows plots of Ω versus time for the complex conjugate roots denominator. The acquisition for complex conjugate roots takes place.

For weather dependent wireless radios, PLDROs have to withstand temperature variations from -40°C to $+75^\circ\text{C}$ and must track the reference signal without any failure (i.e. no loss of lock). In some cases, where the temperature disturbs the XO reference signal or the DRO, and produces a phase or frequency glitch at the phase detector, the PLL may "unlock". The PLL has then to re-synchronize. The acquisition process can be difficult to accomplish when the PLDRO is under temperature stresses. A low PD sensitivity is a major factor in PLDRO acquisition failures. If a microwave PLDRO uses a sampling phase detector (*SPD*) to evaluate the phase error, it is probable that the PD provides a weak sensitivity to the loop mainly due to a weak reference signal $y_i(t)$ at the mixer RF port. The mixer diodes are not perfectly balanced and a D.C. offset is generated at the PD output. This

Figure 2.14. Acquisition for complex conjugate roots, acquisition takes place, from Blanchard [2].

can be compensated at a given temperature, but is difficult to track over a temperature range. The combined effect of weak detector gain with temperature dependent D.C. offsets, put the loop under additional stresses for acquisition. To minimize such issues, one must ensure having a strong PD sensitivity to minimize D.C. offset imbalance effects on the loop. In a production environment, acquisition at microwave frequencies can be a difficult task without acquisition aid circuitry.

Chapter 3

Push-Push Dielectric Resonator Oscillator

3.1 Introduction

The VCO designed for the PLDRO prototype is based on a dielectric resonator (*DR*) resonant structure and a push-push series feedback oscillator topology. A push-push oscillator is basically two symmetrical oscillators that share the same resonant structure. The two oscillators are added together in anti-phase to provide an output frequency twice the resonator fundamental. Although more complex than a fundamental DRO, this topology has the advantage of reducing phase noise according to the coupled oscillator theory [3] and permits a higher final output oscillation frequency for a given active device. In this Chapter, the dielectric resonator $TE_{01\delta}$ electromagnetic fields are derived. A single fundamental oscillator is designed. Then, the push-push oscillator concept is analyzed when coupled to a dielectric resonator.

The oscillator simulation and design are also detailed. To complete the chapter, the oscillator output power combiner is designed and the push-push VCO parameters are characterized for a PLL circuit integration.

3.2 Dielectric Resonator $TE_{01\delta}$ Field Equations and Resonant Frequency

The dielectric resonator (DR) is an unmetallized piece of dielectric which functions as a resonant cavity by means of reflections at the dielectric/air interfaces. Usually, the DR is manufactured in a circular shape like a disk or a cylinder. The relative dielectric constant ϵ_r is much larger than one so the electromagnetic energy stored remains mostly inside the DR, while the outside fields decay rapidly. The dielectric resonator exact resonant frequency F_0 is somewhat difficult to predict. Many authors [4],[5],[6] have developed models and techniques to compute the resonant frequency. Frequently encountered models are the magnetic wall waveguide, the dielectric waveguide or a mixture of both. All of these models approximate the exact resonant frequency with an accuracy ranging from 3% to 10%. The following DR analysis uses the magnetic wall waveguide model.

The magnetic wall approximation is considered because the resonator has a very high dielectric constant. The reflection coefficient Γ of a wave propagating in the dielectric medium incident on an air interface is,

$$\Gamma = \frac{\eta_0 - \eta}{\eta_0 + \eta} = \frac{\sqrt{\epsilon_r} - 1}{\sqrt{\epsilon_r} + 1} \quad (3.1)$$

If the DR relative dielectric constant ϵ_r is large, the reflection coefficient approaches unity. Consequently, the wave energy is mostly reflected back into the resonator.

An electromagnetic wave is totally reflected back if it impinges on an electric wall ($\hat{n}X\vec{E} = 0$) or a magnetic wall ($\hat{n}X\vec{H} = 0$). In the DR case, most of the wave energy is reflected back without shorting the electric field (i.e. no high conductivity material at the interface). Thus, the magnetic field component has to be shorted for the propagating wave to bounce back at the interface [7] (i.e. magnetic wall hypothesis).

We must now find the TE_{01} circular dielectric waveguide mode with the magnetic wall boundary condition at $\rho = a$. For the transverse electric (TE) modes, the E_z component is null and H_z must satisfy the Helmholtz equation,

$$(\nabla^2 + k^2)H_z = 0, \quad (3.2)$$

where, $k = \sqrt{\epsilon_r}k_0$ for $|z| < L/2$ and $k = k_0$ for $|z| > L/2$. Since H_z is constant over a full circular variation, the partial derivative $\partial/\partial\phi$ derived from the Helmholtz equation is null. Then, the resonator transverse fields are reduced to,

$$E_\phi = \frac{j\omega\mu_0}{k_c^2} \frac{\partial H_z}{\partial \rho} \quad (3.3)$$

$$H_\rho = \frac{-j\beta}{k_c^2} \frac{\partial H_z}{\partial \rho}, \quad (3.4)$$

with $k_c^2 = k^2 - \beta^2$.

The magnetic field component H_z has to be finite at $\rho = 0$ and null at $\rho = a$. The solution to Equation 3.2 can be recognized as a Bessel function,

$$H_z = H_0 J_0(k_c \rho) e^{\pm j\beta z}. \quad (3.5)$$

Applying this solution for H_z to Equations 3.3 and 3.4, the transverse fields become

$$E_\phi = \frac{j\omega\mu_0 H_0}{k_c} J_0'(k_c \rho) e^{\pm j\beta z} \quad (3.6)$$

$$H_\rho = \frac{\mp j\beta H_0}{k_c} J_0'(k_c \rho) e^{\pm j\beta z} \quad (3.7)$$

where J_0 and J'_0 are Bessel's function of the first kind and its derivative respectively.

The cut-off wavenumber for the TE_{01} mode is $k_c = p_{01}/a$. The constant p_{01} refers to the Bessel function root $J(p_{01}) = 0$ for this propagating mode, and is 2.4048. The propagation constant in the dielectric resonator β , is real, implying propagating fields. The propagation constant outside the resonator α , is imaginary, implying decaying fields,

$$\beta = \sqrt{\epsilon r k_0^2 - k_c^2} = \sqrt{\epsilon r k_0^2 - (\frac{p_{01}}{a})^2} \quad (3.8)$$

$$\alpha = \sqrt{k_c^2 - k_0^2} = \sqrt{(\frac{p_{01}}{a})^2 - k_0^2}. \quad (3.9)$$

The wave impedances can be defined as

$$Z_d = \frac{\omega \mu_0}{\beta} \quad (3.10)$$

$$Z_a = \frac{j\omega \mu_0}{\alpha}. \quad (3.11)$$

The transverse field distributions for the $TE_{01\delta}$ mode are symmetrical with respect to the center of the dielectric resonator (i.e. $z=0$). Rewriting, the propagating transverse fields in the dielectric region are

$$E_\phi = A J'_0(k_c \rho) \cos(\beta z) \quad (3.12)$$

$$H_\rho = \frac{-jA}{Z_d} J'_0(k_c \rho) \sin(\beta z) \quad (3.13)$$

and the evanescent transverse fields outside the resonator are

$$E_\phi = B J'_0(k_c \rho) e^{-\alpha|z|} \quad (3.14)$$

$$H_\rho = \frac{\pm B}{Z_a} J'_0(k_c \rho) e^{-\alpha|z|}. \quad (3.15)$$

Matching the tangential fields at the resonator interface at $|z|=L/2$ leads to,

$$A \cos\left(\frac{\beta L}{2}\right) = B e^{-\alpha \frac{L}{2}} \quad (3.16)$$

$$\frac{-jA}{Z_d} \sin\left(\frac{\beta L}{2}\right) = \frac{B}{Z_a} e^{-\alpha \frac{L}{2}}. \quad (3.17)$$

Equations 3.16 and 3.17 can be reduced to a single transcendental equation,

$$-jZ_a \sin\left(\frac{\beta L}{2}\right) = Z_d \cos\left(\frac{\beta L}{2}\right). \quad (3.18)$$

We can rewrite this equation in a simpler form using Equations 3.10 and 3.11,

$$\tan\left(\frac{\beta L}{2}\right) = \frac{\alpha}{\beta}. \quad (3.19)$$

Equation 3.19 is required to compute the resonant frequency F_0 of a dielectric resonator. This solution gives a resonant frequency within about 10% of the actual measured frequency [8]. While the frequency error is large, the theoretical model is exact considering the assumption of a perfect magnetic wall. The intent of this analysis is to demonstrate that it is possible to compute the resonant frequency of a dielectric resonator to a certain level of accuracy depending on the validity of the hypothesis. New models were developed [9], that showed closer correlation with actual measured frequency. Figure 3.1 presents the dielectric resonator H_z field distribution.

The actual dielectric resonator implemented in the push-push VCO is manufactured as a 6 GHz resonator. It is of interest to measure its physical dimensions. Table 3.1 shows DR data from the manufacturer along with measured and computed data. The dielectric resonator resonant frequency is also computed from Equation 3.19 with the actual measured dimensions. The resonant frequency given by the transcendental Equation 3.19 is verified in Appendix A. The computed F_0 is 5.387

Figure 3.1. Dielectric resonator $TE_{01\delta}$ mode and H_z field distribution

	Manufacturer Data	Measured Data	Computed Data
Radius(mm)	4.4	4.3307	4.3307
Length(mm)	2.93	3.0226	3.0226
ϵ_r	46.2	N/D	46.2
$Q_{unloaded}$	6806	N/D	N/A
$\tau_f(\text{ppm}/^\circ\text{C})$	7.6	N/D	N/A
Composition	ZrS_nT_i Oxide	N/D	N/A
Freq.(GHz)	6.0182	5.94	5.387

Table 3.1. Dielectric resonator physical parameters

GHz or 10.21% lower than the manufacturer resonant frequency. This is in agreement with the magnetic wall approximation [10].

3.3 Push-Push Oscillator Theory and Design

The push-push oscillator combined with the DR electromagnetic fields produce an anti-phase combination at the fundamental and an in-phase combination at

the second harmonic. The oscillator produces a strong second harmonic signal at the output, with a cancelled out fundamental in the range of -30dBc to -90dBc [11]. The push-push concept [12],[13] is based on two symmetrical oscillators oscillating at half the output frequency. The oscillator output signals are,

$$S_1(t) = \alpha_1 \cdot e^{j\omega_o t} + \alpha_2 \cdot e^{j2\omega_o t} + \alpha_3 \cdot e^{j3\omega_o t} + \dots \quad (3.20)$$

and,

$$S_2(t) = \alpha_1 \cdot e^{j\omega_o(t-\Delta t)} + \alpha_2 \cdot e^{j2\omega_o(t-\Delta t)} + \alpha_3 \cdot e^{j3\omega_o(t-\Delta t)} + \dots \quad (3.21)$$

both signals are identical in frequency and amplitude but a phase difference $\omega_o \cdot \Delta t$ is present on signal $S_2(t)$. If the phase difference between $S_1(t)$ and $S_2(t)$ is π , and both signals are added together,

$$S_{out}(t) = \alpha_1 \cdot e^{j\omega_o t} (1 + e^{-j\pi}) + \alpha_2 \cdot e^{j2\omega_o t} (1 + e^{-j2\pi}) + \alpha_3 \cdot e^{j3\omega_o t} (1 + e^{-j3\pi}) + \dots \quad (3.22)$$

simplifying with Euler identity,

$$S_{out}(t) = 2\alpha_2 \cdot e^{j2\omega_o t} + 2\alpha_4 \cdot e^{j4\omega_o t} + 2\alpha_6 \cdot e^{j6\omega_o t} + \dots \quad (3.23)$$

If both oscillator circuits are perfectly symmetrical, the output shows no odd harmonics and even harmonics are increased by 6 dB compared to the single fundamental oscillator. Figure 3.2 presents the two fundamental single oscillators and the push-push oscillator waveforms. The push-push oscillator does present similar phase noise performance when compared with its uncoupled peer oscillator. According to coupled oscillators theory [3], the close-to-carrier phase noise is reduced by a factor of $1/N$ compared to a single oscillator. The push-push oscillator is based on two oscillators that share the same resonant structure (i.e. coupled oscillators). Therefore, the close-in phase noise L_{ssb} of the coupled oscillator is reduced by 6 dB compared to an

Figure 3.2. Fundamental and push-push oscillator waveforms, from Sinnesbichler [12].

uncoupled oscillator. Because of this 6 dB fundamental noise reduction and the 6 dB noise increase from the frequency doubling process, the push-push oscillator shows L_{ssb} noise similar to its single uncoupled oscillator at twice the frequency. Figure 3.3 shows a typical push-push FET oscillator and Figure 3.4, a $TE_{01\delta}$ typical push-push microstrip coupling for dielectric resonator.

Figure 3.3. Typical push-push FET DRO, from Pavio & Smith [18].

Figure 3.4. Dielectric resonator microstrip coupling and electromagnetic fields

In Figure 3.4, the microstrip transmission line has no ground plane under the substrate thickness. The ground plane is intentionally omitted to show the $\vec{H}$ field. If the ground plane was present, the $\vec{H}$ field would curve inside the dielectric substrate back into the resonator and the magnetic field would be tangent to the electric wall (i.e. ground plane).

3.3.1 Active Device

The active device plays a fundamental role in the oscillator concept. It provides the negative resistance port required to produce a sustained oscillation frequency. The device gain, at the desired frequency of oscillation, must overcome the loss and the phasing must be constructive at the desired frequency to produce an oscillation condition. The devices chosen for the push-push DRO are GaAs MESFET "AFM04P3" from Alpha Industries. The device gate width W_G and gate length L_G are respectively $400 \mu\text{m}$ and $0.25 \mu\text{m}$.

These devices are preferred in X to K_a band oscillator design for their low flicker noise N_{Flick} around the carrier and good gain [14]. Some authors use different device technology like the HBT on SiGe , InP or GaAs depending on the frequency

of operation and required gain [11],[15],[16]. Actual use favors SiGe HBT or GaAs MESFET up to Q band. InP HBT oscillator variants have been demonstrated to 108 GHz [17] and InGaAs-InP HEMT technology presented in push-push oscillators up to 130 GHz.

The author has investigated different active devices while using the same oscillator layout and the same dielectric resonator. The objective was to discover which device technology had the lowest flicker noise N_{Flick} . The oscillator used was a 12 GHz drain-to-gate feedback DRO. For each device, the bias was adjusted for optimum L_{ssb} . The experiment was simple but showed some trends that could be further analyzed. The results demonstrated that GaAs MESFET transistors present lower N_{Flick} and much less sensitivity to pushing than the other tested devices. For those reasons, the author has selected a MESFET active device for the push-push oscillator design. Table 3.2 presents the 12 GHz DRO experiment results.

3.3.2 Fundamental Oscillator Design

The initial step to design the fundamental oscillator is to characterize the MESFET device over the frequency of interest. The scattering parameters file, provided in Appendix C, Table C.1, is then implemented into the simulation software. The dielectric resonator exact lumped characteristics and coupling factor are somewhat difficult to define [18] and are estimated as a LC tank equivalent with an ideal transformer.

The single oscillator is configured as a series gate feedback with the DR located half a wavelength away from the gate terminal. The output matching network is a single stub tuner set to provide enough negative resistance for a sustained

	MESFET NE721	MESFET AFM04P3	PHEMT LPD200	PHEMT TC2181	HJ FET NE3210S	HJ FET NE32584C
L_G	0.80 μm	0.25 μm	0.25 μm	0.25 μm	0.20 μm	0.20 μm
W_G	330 μm	400 μm	200 μm	160 μm	160 μm	200 μm
$NF_{12\text{GHz}}$	N/A	1.3 dB	1.0 dB	0.5 dB	0.35 dB	0.45 dB
$G_{A12\text{GHz}}$	7.0 dB	9.4 dB	12 dB	12 dB	13.5 dB	12.5 dB
$I_{DS_{NF}}$	30 mA	25 mA	20 mA	10 mA	10 mA	10 mA
$V_{DS_{NF}}$	3 V	2 V	3.3 V	2 V	2 V	2 V
$I_{DS_{(Opt. L_{ssb})}}$	71 mA	144 mA	20 mA	15 mA	15 mA	15 mA
$V_{DS_{(Opt. L_{ssb})}}$	4.25 V	2.25 V	3.3 V	4 V	3 V	3 V
P_{1dB}	15 dBm	20 dBm	20 dBm	18 dBm	N/A	11 dBm
$P_{OUT_{(Opt. L_{ssb})}}$	3.29 dBm	2.56 dBm	8.54 dBm	9.69 dBm	0.1 dBm	6 dBm
L_{ssb} (dBc/Hz)						
10 kHz	-90	-100	-74	-73	-80	-72
100 kHz	-114	-114	-92	-91	-95	-95
1 MHz	-134	-136	-124	-119	-121	-123
$Push.$ (MHz/V)	0.328	0.510	3.23	1.74	2.08	1.87

Table 3.2. 12 GHz DRO performances for various active devices

oscillation. The impedance seen by the microstrip line when the DR is resonating is real and consequently, the microstrip impedance at this point is slightly higher than the transmission line impedance. A positive feedback network is added to the source to provide greater instability from the device at 6 GHz. Figure 3.5 shows the single oscillator transmission line topology.

Figure 3.5. Fundamental 6 GHz oscillator design

The oscillator is optimized with the simulation package *ADS*® for a targeted oscillation at 5.9 GHz. The author has preferred to design for a slightly lower resonant frequency to minimize the risk of an oscillating frequency above 6 GHz. A lower frequency can be increased by reducing the resonator length while reducing the frequency can be tedious. The oscillation condition is verified with *ADS*® using a "Oscstest" block between the resonator and the negative resistance port. On a polar chart, the $1+j0$ position has to be circled clockwise at least once to provide an oscillation condition. The expected frequency of oscillation is located at the vector maximum real component. The maximum real component intersected by the frequency sweep must be greater than one to insure a sustained oscillation. To add

weight to the predicted oscillation from the "Osctest" block, a one port scattering parameter test is also simulated. The measurement of the oscillator output match $S_{(1,1)}$ does provide extra information about the frequency of oscillation. If the reflected wave measured at the oscillator output port has gain at the desired frequency, it's highly probable that the circuit under test is unstable at this frequency and will oscillate. Figure 3.6 presents the single oscillator output match $S_{(1,1)}$ when the resonator is located at half a wavelength away from the gate terminal.

Figure 3.6. Fixed DR position at $\theta_{DR} = \lambda/2$

The output match shows a gain of 50 dB for the simple reason that the simulated resonator is considered lossless. By adding any loss in the lumped network, the gain drops to the neighborhood of 15 dB, depending on the inserted loss. The ideal transformer has a coupling factor set for a power loss of 3 dB.

To confirm that the oscillation condition is determined by the DR, two complementary tests were simulated.

- Variation of DR lumped component (L,C) values;
- Variation of DR position (θ_{DR}).

The frequency of oscillation is closely related to the lumped component values, and the resonant frequency corresponds to the usual equation

$$F_0 = \frac{1}{2\pi\sqrt{LC}}. \quad (3.24)$$

The DR position variation from the gate terminal θ_{DR} shows a strong oscillation dependence on the position. Moving the resonator away from its optimum location ($\lambda/2$) produce a shift in oscillation frequency and a reduction in amplitude. Figure 3.7 shows the $S_{(1,1)}$ behavior when the resonator is moved along the gate transmission line. On the LHS of marker one (m1) the DR is further away from $\lambda/2$ and on the RHS the DR is closer to the gate terminal. The previous simulation tests do provide insurance that the single oscillator oscillates at the desired frequency and that the frequency is dictated by the dielectric resonator and not by other device parasitics.

The methodology presented is a first order oscillation design using the basic scattering parameters file from the manufacturer. For a more accurate simulation, a second order transistor model has to be implemented with all the parasitics included. The DR has also to be fully characterized with transformer coupling coefficients to match the transistor model level of accuracy, in order to improve the oscillation frequency, amplitude and noise predictability. However, even with an excellent second

Figure 3.7. Swept DR position with center at $\theta_{DR} = \lambda/2$

order model, the transistor behavior in oscillation is tedious to accurately predict and often unnecessary because of the dielectric resonator frequency tolerance, which is in the order of 0.5%. Although not much help for the frequency predictability, the second order model gives better insight about expected output power and helps to optimize the second harmonic push-push matching network.

The single oscillator has now to be converted into a push-push oscillator. The single oscillator gate and source network design are considered to be optimal for the push-push operation while the drain network is un-optimized for the second harmonic [18]. When the two oscillators are placed in such a way that the two are perfectly symmetrical and diametrically opposed to the DR, the oscillators are out of phase by 180 degrees due to the $TE_{01\delta}$ field configuration. The summation of the two oscillator signals causes the first and odd harmonics to disappear and the second and even harmonics to increase by a factor of 2. Figure 3.8 presents the push-push DRO transmission line model. It consist of two identical single oscillators previously

designed and a Wilkinson power combiner, which will be discussed in subsection 3.3.3.

Figure 3.8. Push-push DRO design

To modify the drain network, in order to maximize the second harmonic power, one must optimize with a second order transistor model and adjust the bias to get maximum power at the desired frequency of operation. The author has kept the drain network fixed and optimized the bias on the actual prototype to give maximum drive level at the second harmonic.

Now the push-push DRO design has to be converted into a tunable source to be incorporated into the PLL system. In other words, it has to become a VCO. There are two common ways of adding a voltage control to an oscillator. Varactor diodes and direct transistor bias control are techniques often implemented. For this work on the push-push DRO, the tuning is realized with two SMV1253-079 varactor diodes from Alpha Industries. The concept of operation is to vary the diode capacitance C_{JX} by applying a reverse voltage (V_r) to tune the frequency of oscillation. The transmission line (TL) where the varactor is located varies in impedance from Z_0

to a lower impedance according to the reverse voltage applied. If the V_r is null, the varactor has maximum capacitance and the TL equivalent impedance is reduced. A lower impedance TL increases the loading on the gate TL and consequently reduces the oscillation frequency. On the other hand, a higher voltage on the varactor reduces its capacitance and the TL impedance increases until it reaches Z_0 . Then, the loading on the gate TL is minimum and the oscillation frequency is maximum. Figure 3.9 shows the DRO tuning topology design. The gap between the varactor TL and the

Figure 3.9. Push-push DRO voltage control topology

gate TL has a strong effect on the VCO tuning bandwidth. A very small gap induces larger tuning bandwidth but also decreases the loaded Q of the overall oscillator due to the varactor limited Q , and leads to a possible deterioration in phase noise. The coupling gap is set to 10 mil by the author from previous DRO tuning experiments. If the DRO tuning bandwidth is too limited for an adequate behavior in the PLL environment, the gap has to be reduced to increase the oscillation tunability. The varactor used has a zero-voltage capacitance C_{J0} of 70 pF and the ratio $C_{J0.3}/C_{J4.7}$ is in the neighborhood 12. The value of the Q factor is 350 and is specified at 50 MHz

with a 3 Volts reverse bias voltage. The 70 pF varactor C_{J0} value was empirically found.

3.3.3 Wilkinson Combiner

The push-push VCO needs a power combiner to add the two fundamental oscillator outputs. The desired power combiner has to induce no relative insertion phase shift between the two symmetrical oscillators. A Wilkinson power combiner is implemented at the push-push VCO output. At 12 GHz, the Wilkinson is printed directly on the substrate and requires only a $100\ \Omega$ resistor as a lumped component. The zero relative insertion phase shift from the Wilkinson and the 20-25 dB isolation between the two summing ports make this element a suitable choice for this application. Figures 3.10 and 3.11 show the equal split transmission line Wilkinson design and the simulated design on the actual substrate respectively.

Figure 3.10. Wilkinson combiner topology

The Wilkinson combiner adds the fundamental oscillator signals $S_1(t)$ and $S_2(t)$. Since this element has no relative phase shift from the input to the output, the desired 180 degrees phase shift between $S_1(t)$ and $S_2(t)$ is not altered. Thus, first harmonic cancellation is maximum and second harmonic signals, which are in

Figure 3.11. Wilkinson simulated scattering parameters

phase, are added together to provide the push-push output signal. If a combiner with a relative phase shift between the ports were used, like a 3 dB-hybrid, the fundamental cancellation and second harmonic power would be reduced.

3.4 Push-Push VCO Measured Parameters

In this section, the push-push VCO parameters are measured and discussed. The VCO modulation sensitivity constant K_3 is computed directly from the actual prototype and the mechanical tuning bandwidth is measured. The push-push DRO sensitivity to pushing is also discussed. The phase noise L_{ssb} is measured and the de-embedded output spectrum is presented.

To compute the loop filter and close the phase locked loop, the modulation sensitivity constant K_3 from the VCO has to be characterized. The actual prototyped VCO is connected to a spectrum analyzer and a D.C. power supply to measure its sensitivity. Table 3.3 shows the VCO frequency shift for a tuning voltage V_{tune}

	V_{tune} (V)	Frequency(GHz)	Delta(kHz)
Sample 1	3	11.999000	N/A
Sample 2	4	11.999188	188
Sample 3	5	11.999418	230
Sample 4	6	11.999693	275
Sample 5	7	11.999943	250
Sample 6	8	12.000081	138
Sample 7	8	12.000081	138
Sample 8	9	12.000206	125

Table 3.3. Measured VCO frequency versus applied voltage

variation from 3 V to 9 V. Although the VCO tunes over 2.5 MHz, from 0 V to 16 V, the particular interest is within a smaller V_{tune} range where the tuning remains mostly linear. The modulation sensitivity is found by extrapolating linearly from Sample 2 to Sample 5. This gives

$$K_3 = \frac{11.999188 - 11.999943}{4 - 7} = 252 \frac{kHz}{V} = 503\pi 10^3 \frac{rad/s}{V} \quad (3.25)$$

The total VCO tuning bandwidth is in the neighborhood of 2.5 MHz. While this is sufficient for the proof of concept, it may not be enough for an actual manufactured VCO. The tuning bandwidth should be around 10 MHz to 20 MHz to compensate for temperature and device variations. An increase of tuning bandwidth, for the same D.C. tuning range, increases the VCO sensitivity. A mechanical tuner that sits on top of the VCO tunes the frequency of oscillation from 11.9575 GHz to 12.0425 GHz a bandwidth of 85 MHz. This tuner is intended to set the free-running resonant frequency to

$$F_0 = F_{Lock} - \frac{ElecBW}{2}, \quad (3.26)$$

where F_0 is the free-running resonant frequency, $Elec_{BW}$ is the electrical tuning control bandwidth and F_{Lock} , the desired locked frequency.

The push-push DRO sensitivity to pushing is also measured. The pushing or the pushing figure is a characteristic of a given oscillator to be influenced, frequency wise, by the drain or the collector voltage variations. Usually expressed in Hz/V and measured with slight variation around the typical operation voltage. The prototyped push-push DRO drain voltage change, from 4.9 V to 5 V and 5 V to 5.1 V, produced a frequency drift of 111 kHz and 127 kHz respectively. Thus, the pushing figure is established to 1.19 MHz/V. The push-push oscillator free-running phase noise L_{ssb} is presented on Figure 3.12. The phase noise is measured from a 10 kHz minimum offset frequency to a maximum of 10 MHz offset frequency. This frequency span is usually sufficient to evaluate the L_{ssb} for this type of oscillator. The phase noise

Figure 3.12. Free-running push-push DRO L_{ssb} phase noise

density of -93 dBc/Hz at 100 kHz offset from the carrier is representative of a 12 GHz DR voltage controlled oscillator. From Table 3.2, the fundamental drain-to-

gate feedback oscillator at 12 GHz using the same active device and puck material showed a L_{ssb} noise of -114 dBc/Hz at 100 kHz offset. The significant difference can be explained by the different topology used for the two oscillators. The oscillator topology has considerable effect on the performance and one should not rely only on the active device and the dielectric resonator for a good DR oscillator design. In this case, phase noise and pushing is degraded by the push-push topology. To improve the push-push DRO phase noise, a different active device with lower N_{Flick} would probably have a greater and more significant effect than swapping to a different DR.

The push-push DRO output spectrum plots are combined with an output buffer. The buffer is implemented on the prototype to reduce the VCO load pulling. While direct measurement of the VCO would show a clearer picture of the main tone and harmonics, the VCO tones can be reasonably well de-embedded from the buffer if the transfer function is known. As will be discussed in Chapter 5, the buffer produces a 12 dBm P_{1dB} output power and a decreasing gain, from 25 dB to 15 dB, from 6 GHz to 18 GHz. The gain at 12 GHz is 20 dB. The push-push DRO broadband output spectrum is depicted on Figure 3.13 and its divided-down 3 GHz signal $y_o(t)$ broadband spectrum showed on Figure 3.14. From the buffer transfer function, the actual VCO tones are deduced as follows,

- 6 GHz fundamental $\rightarrow$ -27.84 dBm , -47.67 dBc from desired;
- 12 GHz second harmonic $\rightarrow$ 14.83 dBm;
- 18 GHz third harmonic $\rightarrow$ -17.84 dBm , -42.67 dBc from desired.

The harmonics at 9 GHz and 15 GHz are due to the divide-by-4 circuit that was powered with the same supply lines as the push-push DRO. If the divider is turned off,

Figure 3.13. Push-push DRO broadband output spectrum

Figure 3.14. 3 GHz divided-down DRO signal $y_o(t)$: broadband output spectrum

the tones disappear from the spectrum. The push-push oscillator close-in spectrum is generally of interest because it gives information about phase noise and short term stability. Although, the output is at 12 GHz, the designed oscillator can be studied under a 500 kHz span. A signal of this frequency that can be "spanned-in" without being too jittery, may preclude a temperature stable oscillator and reduced sensitivity to microphonics. Figure 3.15 shows the free-running oscillator in a 500 kHz span while, Figure 3.16, the phase locked oscillator in a 200 kHz span view.

Figure 3.15. Push-push DRO 500 kHz spectrum view

Figure 3.16. Push-push PLDRO 200 kHz spectrum view

Chapter 4

Reference Multiplier

4.1 Introduction

The PLDRO uses a reference signal to phase lock the divided free-running DRO signal. The PLDRO output frequency F_0 desired is 12 GHz and a divide-by-4 prescaler divides the frequency to the comfortable 3 GHz zone. Thus, most of the PLL circuitry uses 3 GHz frequency instead of the 12 GHz output frequency. The phase detection, amplifiers and the loop circuitry uses 3 GHz components, which are lower cost than the 12 GHz Ku band ones. Consequently, the design becomes much less sensitive to components, layout and manufacturing variations. One could have investigated other frequencies such as 1.5 GHz or 6 GHz and analyze the loop performance under such reference frequency. But, to limit the scope of this work, the PLDRO uses only a fixed divide-by-4 combined with a 3 GHz reference signal.

The reference multiplier concept is to use a low frequency stable source like a 100 MHz Crystal Oscillator (XO) and to hit a highly non-linear element to generate impulses. In the frequency domain, a comb of 100 MHz spaced frequencies is generated. These impulses are converted into a continuous wave (CW) via a resonator and filter combination. In our specific application, the XO 30th harmonic is filtered and amplified to provide a stable low phase noise 3 GHz reference signal $y_i(t)$ to phase lock the divided-down 3 GHz DRO signal $y_o(t)$. In this chapter, the step recovery diode multiplier theory is analyzed. Secondly, the crystal reference spectrum, stability and phase noise is discussed. Then, the multiplier filter is designed and measured. To conclude the chapter, the measured performance of the prototyped frequency multiplier is discussed. Figure 4.1 presents a typical frequency multiplier concept.

Figure 4.1. Multiplier concept

4.2 Step Recovery Diode Multiplier Theory

The key element in a step recovery diode (*SRD*) multiplier is the impulse generator circuit. The impulse circuit uses the SRD as a strong non-linear element having highly desired characteristics such as a short transition time t_t and long minority lifetime carrier τ . The SRD is a type of p-i-n diode that stores minority charge carriers in its i-region when forward biased, conduction continues until all of the stored charge has been removed. At that point, the conduction current "snaps" from a large reverse conduction value to zero in a very short time [19]. The SRD has a high impedance when storing charge and a low impedance during interval when stored charge flows. Thus, the SRD impedance is a function of time during a normal drive cycle. Since the reverse capacitance C_r is almost constant in reverse bias and the forward capacitance C_f can store almost any amount of charge in forward bias, the SRD can be modelled as two independent linear circuits [20]. This first order model assumes the diode changes state instantaneously. Refined models have been developed in recent work [21] and could be used to design more efficient impulse generator circuits. Usually, manufacturers specify t_t , τ and C_r . The D.C. series resistance R_s is easily found and the nonlinear resistor R_f can be related to C_f and τ as given by Kotzebue [22],

$$\tau = R_f C_f \quad (4.1)$$

Figure 4.2 shows the actual and ideal model for a SRD. The SRD is assumed to be driven hard into forward and reverse operation for the impulse generator to be efficient. It has been shown [20],[23] that when the harmonic generator resistive load is replaced by a resonant structure, the total impulse energy is transferred around the N^{th} harmonic where the resonant circuit is tuned. About 60% to 70% of the impulse

Figure 4.2. Idealized and conventional SRD model

total energy is converted into the desired N^{th} harmonic. The reference source is used to toggle the SRD between *ON* and *OFF* states. The inductor L and the SRD minority carrier lifetime force the SRD to stay *ON* for a short while even though the source polarity would normally turn the diode *OFF*. The short t_t turn the SRD *OFF* quickly when inductor's current i_L and stored charges have vanished, thus, creating a sharp narrow pulse of amplitude $-E_b$. Figure 4.3 shows the conduction and depletion intervals for the impulse generator. The impulse generator inductor current $i_L(t)$ and its output voltage $e_o(t)$ equations are shown for the conduction and depletion interval for an input sinusoidal source. For the conduction interval,

$$i_L(t) = I_0 + \frac{E}{\omega L} [\cos(\alpha) - \cos(\omega t + \alpha)] - \frac{(V + V_\Phi)}{\omega L} \omega t \quad (4.2)$$

$$e_o(t) = V_\Phi$$

where V_Φ is the SRD contact potential and α , the impulse generator conduction angle. For the depletion interval,

$$i_L(t) = I_1 \exp\left(\frac{-\zeta \omega_n t}{\sqrt{1-\zeta^2}}\right) \cdot \left[\cos(\omega_n t) + \frac{\zeta \sin(\omega_n t)}{\sqrt{1-\zeta^2}}\right] \quad (4.3)$$

$$e_o(t) = \frac{-I_1 \sqrt{\frac{L}{C}}}{\sqrt{1-\zeta^2}} \exp\left(-\frac{\zeta}{\sqrt{1-\zeta^2}} \beta t\right) \sin(\beta t) \quad (4.4)$$

where, $\beta = \sqrt{\frac{1-\zeta^2}{LC}}$ and $\zeta = \frac{1}{2R_L} \sqrt{\frac{L}{C}}$.

Figure 4.3 shows the plotted impulse generator conduction and depletion interval waveforms. When in conduction interval, the output voltage is the SRD contact potential V_Φ and when the impulse generator is in depletion or impulse interval, the output voltage is a sharp pulse in time of amplitude $-E_b$. The dashed lines on $e_o(t)$ depletion interval, show the damped waveform expected if the load R_L is replaced by a resonant circuit.

Figure 4.3. Pulse generator conduction and depletion interval waveforms

The SRD multiplier efficiency can be stated as,

$$\frac{P_{out}}{P_{in}} = \{\xi_{(cw \rightarrow imp)}\} \cdot \{\xi_{(imp \rightarrow cw)}\} \cdot \{\xi_{resonator}\} \cdot \{\xi_{filter}\} = \xi_{multiplier}, \quad (4.5)$$

where $\xi_{(cw \rightarrow imp)}$ is the input to impulse power efficiency and $\xi_{(imp \rightarrow cw)}$, the impulse to output power efficiency.

The SRD multiplier efficiency can be characterized by separating the circuit losses into two sections, firstly, by the analysis of the reference CW signal conversion into impulses and secondly, by the maximum power that can be extracted from the impulses into the final desired output tone. The CW to impulse conversion has the following four important losses to consider,

- Recombination losses, $(\omega\tau \neq \infty)$;
- Matching network losses, $(Q_u \neq \infty)$;
- Diode switching losses, $(t_t \neq 0)$;
- Series resistance losses, $(R_s \neq 0)$.

The recombination losses are due to a finite τ and are considered negligible if one ensures that $\omega\tau \gg 1$. The matching network losses are also considered negligible. The two others losses are discussed to characterize impulse generator efficiency $\xi_{(cw \rightarrow imp)}$. It has been shown [23] that the efficiency loss due to the SRD transition from an *ON* and *OFF* state is

$$\xi_{(trans)} = \frac{1}{1 + \frac{N \cdot V_{br}}{t_p}}, \quad (4.6)$$

where, $N = 1/2F_{in}t_p$ and V_{br} is the SRD reverse breakdown voltage. The impulse duration t_p is approximatively equal to $t_p \approx \pi\sqrt{LC_r}$. The efficiency loss due to series resistance R_s is

$$\xi_{(R_s)} = \frac{1}{1 + \frac{P_{loss}}{P_{out}}} \quad (4.7)$$

with,

$$P_{loss} = \frac{R_s}{t_1} \int_0^{t_1} i_{cond}^2(t) dt + \frac{R_s}{n/\omega} \int_{t_1}^T i_{depl}^2(t) dt, \quad (4.8)$$

where, n is the multiplication factor and ω the output angular frequency. The first and second integrations are for the impulse generator conduction and depletion current respectively. The depletion integral can be ignored because the current is much lower during the impulse than the conduction interval. The output power is given by Hamilton [20],

$$P_{out} = \frac{1}{2} F_{in} L I_1^2 \{1 - e^{-(2\pi\zeta/\sqrt{1-\zeta^2})}\} \quad (4.9)$$

Consequently, the CW to impulse conversion efficiency is

$$\xi_{(cw \rightarrow imp)} = \xi_{(trans)} \cdot \xi_{(R_s)} = \frac{1}{1 + \frac{N \cdot V_{br}}{I_p}} \cdot \frac{1}{1 + \frac{P_{loss}}{P_{out}}}. \quad (4.10)$$

There are also two important losses when the impulse is converted subsequently into a CW at $n \cdot F_{in}$,

- Series resistance losses, ($R_s \neq 0$);
- Resonant structure and output filter losses, ($Q_u \neq \infty$).

The total power in the impulse train is

$$P_{imp} = P_{in} \cdot \xi_{(cw \rightarrow imp)} = \frac{\pi \zeta E_b^2 F_{in} C_r}{\sqrt{1-\zeta^2}} \approx \pi \zeta E_b^2 F_{in} C_r = \frac{E_b^2}{4N Z_o}, \quad (4.11)$$

where $\zeta = \frac{1}{2Z_o} \sqrt{\frac{L}{C_r}}$. The power at the n^{th} harmonic P_n , using the spectrum of the comb generator circuit is,

$$P_n = \frac{C_n^2}{2R'} \frac{1}{(1 + \frac{R_s}{R_L})^2} \quad (4.12)$$

where, $R' = Z_o/2n$ is the impedance seen by the impulse generator through a Z_o quarter wave transmission line. C_n is the n^{th} harmonic Fourier coefficient of the comb generator and expressed as

$$C_n = C_o \frac{\cos(x \cdot \pi/2)}{1-x^2}$$

with $C_o = 2E_b/(\pi N)$ and $x = 2F_{out}t_p$. The efficiency $\xi_{(imp \rightarrow cw)}$ is then found by dividing the power at the wanted harmonic P_n by the total impulse power P_{imp} ,

$$\xi_{(imp \rightarrow cw)} = \frac{P_n}{P_{imp}} = \frac{C_n^2}{Z_o} \cdot \frac{n(1/1 + R_s/R')^2}{\pi \zeta E_p^2 F_{in} C_r} = \left\{ \frac{4}{\pi} \cdot \frac{x \cos(x \cdot \pi/2)}{1 - x^2} \cdot \frac{1}{1 + 2R_s/Z_o} \right\}^2 \quad (4.13)$$

The filter and resonator efficiency losses are generally caused by conductor loss σ_c and dielectric dissipation σ_d and can be easily computed via a transmission line software package. As an engineering rule, and from previous designs by the author, the SRD multiplier coupled with a good multiplier design produces a conversion loss (L_c) in the neighborhood of $20 \log(n)$.

4.3 Crystal Reference

To produce a good harmonic generator, the reference performance is crucial. Indeed, the reference is multiplied up considerably and used, in our application, to phase lock the divided-down DRO at the 3 GHz IF frequency. Thus, the reference signal $y_i(t)$ has to have an output spectrum as clean as possible for the PLL to lock on and achieve low phase noise and minimum peak deviation. To minimize adverse effects due to the large multiplication factor (N) of the reference, the following reference oscillator criteria should be followed:

- Fundamental oscillator;
- Excellent short and long term stability;
- Minimal phase noise, decreasing rapidly to the noise floor.

The crystal reference to be multiplied to provide the reference signal $y_i(t)$ to lock the DRO is a 100 MHz ovenized controlled crystal oscillator (OCXO). This

reference has excellent phase noise and stability performance and the output frequency is the crystal oscillator fundamental. A harmonic oscillating reference (i.e. 20 MHz multiplied by 5) should be avoided. Such a reference would show strong tones, 20 MHz apart, at the final multiplier output instead of the desired 100 MHz tone spacing. This could cause the PLL to lock on to a wrong reference signal (i.e. $y_i(t) \pm 20$ MHz) when the DRO is powered up.

4.3.1 Reference Spectrum

The reference signal spectrum would ideally be a Dirac delta $\delta(\omega)$ function at 100 MHz as an input to the reference multiplier, but this is not practical. The OCXO used has very low level spurs that are adequate for the fundamental harmonic generation. Figure 4.4 shows the 100 MHz reference output spectrum and Figure 4.5 presents the same spectrum viewed under a high resolution bandwidth to show objectionable reference spurs.

Figure 4.4. 100 MHz input reference with normal resolution bandwidth

Considering that the main spur is 82 dBc lower than the fundamental and 43.3 MHz away, its unlikely that it can cause a meaningful disturbance at the final multiplier output. The reference output power is 10 dBm at 100 MHz and the second harmonic is 45 dBc lower in power.

Figure 4.5. 100 MHz input reference with high resolution bandwidth

4.3.2 Reference Short Term and Long Term (Aging) Stability

From manufacturers' specification sheets, the OCXO short term stability is ± 100 ppb from -40° to $+70^\circ$ degree Celsius. Longer term stability, or aging, is within ± 1 ppm for the first year and smaller than ± 3 ppm over a ten years span. When initially powered, the internal oven brings the reference signal frequency F_{ref} to ± 200 ppb of the center frequency F_0 within 5 minutes. While warming up, the total OCXO current drawn is 400 mA and drops to 100 mA in steady state operation. The short term stability performance translates into a 2400 Hz peak to peak deviation at the 12 GHz PLDRO output.

<i>Offset frequency</i>	L_{ssb} OCXO (dBc/Hz)	$L_{ssb} y_i(t)$ (dBc/Hz)
1 Hz	-60	-30.5
10 Hz	-90	-60.5
100 Hz	-120	-90.5
1 kHz	-140	-110.5
10 kHz	-150	-120.5
> 100 kHz	-170	-140.5

Table 4.1. 100 MHz OCXO and 3 GHz $y_i(t)$ expected phase noise in (dBc/Hz)

4.3.3 Reference Phase Noise

In a PLL, reference phase noise is the main noise contributor within the loop bandwidth. Thus, for the PLDRO to maintain excellent noise performance, the reference phase noise has to be minimal. Crystal oscillators (XO) are known to have excellent phase noise performance while still being affordable. The OCXO has a SC-cut that improves the phase noise L_{ssb} and the short term stability. The OCXO L_{ssb} and the PLL reference signal $y_i(t)$ L_{ssb} should be distinguished. In our application, the phase detection is evaluated at IF frequency. The 100 MHz crystal is multiplied to 3 GHz via the SRD frequency multiplier and compared to the divided-down DRO frequency $y_o(t)$. The multiplication factor "N" degrades the PLL input reference signal $y_i(t)$ phase noise according to

$$L_{ssb}(y_i(t)) = L_{ssb}(OCXO) + 20 \cdot \log(N). \quad (4.14)$$

According to Equation 4.14, the OCXO phase noise degradation is 29.5 dB. If a sampling phase detector were used, the phase noise degradation would be for a multiplication factor of N=120 or 41.6 dB. Table 4.1 presents the OCXO and $y_i(t)$

L_{ssb} phase noise in dBc/Hz for various frequency offsets.

4.4 Multiplier Filter Design and Measured Performances

The output band-pass filter (*BPF*) is designed with a 2-D field solver software. The BPF is a 5th order interdigital type with a Chebyshev 0.5 dB equal ripple response. This filter topology is preferred over other printed or lumped structures because of its small dimensions and good repeatability at this frequency band. The filter is centered at $F_0=3$ GHz and has a 400 MHz passband. The filter is printed on a 10 mil substrate with dielectric permittivity $\epsilon_r = 3.6$. The substrate loss tangent is $\tan \delta = 0.09$. Although lossy, this substrate has the advantage of being already used in mass production in SMT processes. Figure 4.6 and Figure 4.7 show the filter simulated and measured scattering parameters respectively.

Figure 4.6. 3 GHz band-pass filter simulated scattering parameters

Figure 4.7. 3 GHz band-pass filter measured scattering parameters

4.5 Frequency Multiplier Measured Parameters

The frequency multiplier measured performances are as expected. The circuit is multiplying the 100 MHz OCXO signal to provide a PLL reference signal $y_i(t)$ centered at 3 GHz with 0 dBm output power. According to individual insertion loss (I_L) and insertion gain (I_G) measurements, the final output power targeted was 3 dBm. The lossy substrate, D.C. path leakages, component variations and lossier multiplier all contribute to the 3 dB power shortage. While lower than expected, the multiplier output power is sufficient to drive the mixer RF port. For the phase detector to operate properly, the LO port needs to be driven hard with a single tone. Hence, the reference signal $y_i(t)$ which has a 100 MHz spaced comb of frequencies, is fed to the RF port. The divided-down DRO output, with a single dominating 3 GHz tone, is then applied to the mixer's LO port. Figure 4.8 presents the measured multiplier chain with associated insertion gains and losses.

Figure 4.8. Measured multiplier chain

4.5.1 Output Spectrum

Ideally, the reference multiplier output spectrum would be a single tone at 3 GHz and all the 100 MHz energy would be transferred to this desired signal. Obviously, we have to deal with losses, parasitics and non-linearities that do not exactly follow an ideal behavior for a specific application. As a result, the output spectrum becomes more like a comb of frequencies centered at 3 GHz with undesired 100 MHz spaced tones. It is possible to improve the reference multiplier output spectrum by introducing a low loss, narrow band BPF that would reject the 100 MHz tones, but this filter would introduce manufacturing issues and added cost. However, the PLL do not require the reference $y_i(t)$ to have a clean spectrum. The PLL itself acts as a very sharp BPF that cleans up everything that is beyond the loop bandwidth. Figure 4.9 presents the measured broadband output spectrum of the frequency multiplier, and Figure 4.10, the 700 MHz output spectrum of the multiplier.

Figure 4.9. Frequency multiplier broadband output spectrum

4.5.2 Actual and Expected Multiplied Phase Noise

According to Table 4.1, the OCXO phase noise has to be degraded by 29.5 dB to include the $N=30$ frequency multiplication. Thus, the $y_i(t)$ phase noise would be computed easily. However, with larger offsets from the carrier (i.e. > 500 kHz), the active devices' noise floor may dominate the decreasing phase noise of the reference. Consequently, the device noise figure (NF) has to be added to the phase noise floor. The active devices used add 10 dB of noise to the floor. The new noise floor is then -130 dBc/Hz and begins at 30 kHz offset versus -140 dBc/Hz and 100 kHz offset when the NF is not accounted for. Figure 4.11 shows the 100 MHz and 3 GHz expected phase noise and Figure 4.12, the measured 3 GHz multiplied reference L_{ssb} phase noise along with the spectrum analyzer phase noise floor.

Figure 4.10. Frequency multiplier 700 MHz output spectrum

Figure 4.11. 100 MHz OCXO and 3 GHz expected phase noise L_{ssb}

Figure 4.12. 3 GHz measured L_{ssb} phase noise

Chapter 5

Phase Detector, Loop Filter and Sub-Circuits

5.1 Introduction

This chapter initially discusses practical views on the PD sensitivity. The PD gain measurement set up is detailed, and K_1 is measured in order to compute the synchronization bandwidth K . Then, the optimum loop noise bandwidth $F_{n_{3dB}}$ crossover point is measured. With a damping constant chosen for optimum noise performance, the natural angular frequency ω_n is found. Then, the loop filter time constants are established. The open and closed loop transfer functions $H_o(\omega)$ and $H(\omega)$ are then plotted with the Matlab[©] simulation package and discussed. The phase margin ϕ_m is computed to evaluate the loop stability. To conclude the chapter, the design, simulation and measurement of the functional sub-circuits are reviewed to get the complete PLDRO design picture.

Parameter	Min.	Typ.	Max.	Units
LO to RF Range	-	1.5 - 4.5	-	GHz
IF Range	-	DC - 1.5	-	GHz
Conversion Loss (L_c)	-	8.5	10	dB
Noise Figure (NF)	-	8.5	10	dB
LO to RF Isolation	29	40	-	dB
LO to IF Isolation	27	35	-	dB
RF/IF Input Power	-	-	13	dBm
LO Input Power	-	-	27	dBm

Table 5.1. Hittite mixer HMC213MS8 specifications

5.2 Phase Detector

The phase detector implemented on the PLDRO prototype is an ultra-miniature double-balanced passive mixer from Hittite. The HMC213MS8 mixer uses GaAs Schottky diodes and operates up to 4.5 GHz. The choice of a passive mixer is intended to minimize noise impairment while detecting phase error and to insure that the PD is a non-major noise contributor within the loop bandwidth. Table 5.1 shows the HMC213MS8 manufacturer's specifications.

Usually, manufacturers do not supply any form of D.C. phase detection parameters required to compute the PD sensitivity K_1 . Thus, to establish a discrete value for the PD gain, the mixer sensitivity has to be characterized in a separate test fixture. For RF and microwave operation, the phase detector sensitivity can be measured accurately with a phase shifter, a signal generator and a voltmeter. Figure 5.1 presents the setup to measure the PD sensitivity.

 Figure 5.1. Typical phase detector K_1 measurement setup

The LO port is driven by a phase-shifting 15 dBm tone and the RF port is driven by a fixed-phase 0 dBm tone, both at 3 GHz. A quadrature condition occurs at the mixer's LO and RF port when the variable phase shifter is set to zero (i.e. the D.C. output is null). The PD slope is found by varying the phase shifter in the linear region and sampling the D.C. component for each given phase shift. Then, the sensitivity K_1 is found by calculating the slope of the extrapolated line. From Table 5.2, the PD sensitivity is computed for its linear region. The corresponding samples that provide the maximum linear shift are Sample 10 and Sample 2. From a linear extrapolation,

$$K_1 = \frac{-69.21 \text{ mV} - 74.63 \text{ mV}}{-21.62 - 19.86} = 3.47 \frac{\text{mV}}{\text{degree}} = 0.198 \frac{\text{V}}{\text{rad}} \quad (5.1)$$

5.3 Loop Filter Analysis

The loop filter plays a crucial role in determining the quantity of the close-in noise a PLL will show at its output. Indeed, by adjusting the loop filter parameters τ_1 , τ_2 and the loop gain K , the loop noise bandwidth $F_{n_{3dB}}$ moves in frequency to achieve the best possible phase noise from the PLDRO prototype. The loop filter $F(s)$ can be fully characterized when the parameters K , ζ and ω_n are known. The

	Display Reading	Phase Shift(°)	D.C. Output(mV)
Sample 1	83	64.3	+97.02
Sample 2	84	70.14	+74.63
Sample 3	85	75.98	+51.82
Sample 4	86	81.82	+28.74
Sample 5	87	87.65	+7.56
Sample 6	87.4	90	0
Sample 7	88	93.52	-14.75
Sample 8	89	99.30	-35.17
Sample 9	90	105.18	-52.95
Sample 10	91	111.62	-69.21
Sample 11	92	116.86	-84.34
Sample 12	93	122.7	-96.07

Table 5.2. Measured PD output D.C. component versus LO & RF phase shift

loop filter consists of a gain stage K_2 followed by the integrator with phase lead correction network. The gain stage provides an additional degree of freedom to adjust the synchronization bandwidth K . The gain K_2 is set to 5.6 via resistors R_F and R_G , which corresponds to 5.1 k Ω and 1.1 k Ω respectively as seen on Figure 5.2. The synchronization bandwidth is found by multiplying the individual loop gains. Table 5.3 recalls the measured gains needed to compute K . K is evaluated as

$$K = K_1 \cdot K_2 \cdot \frac{K_3}{4} = \{0.198 \frac{V}{rad}\} \cdot \{5.6\} \cdot \{126\pi \cdot 10^3 \frac{rad/s}{V}\} = 438908 \frac{rad}{s}. \quad (5.2)$$

For a typical PLL fixed frequency application, ζ should be set between 0.3 & 0.8 depending on the $H(j\omega)$ roll-off required. For the PLDRO application, ζ is set to 0.5 and corresponds to the optimum equivalent noise bandwidth point for a loop with an integrator with a phase lead correction network. The last parameter to be set to evaluate $H(j\omega)$ is ω_n . In order to establish the natural angular frequency, the loop

Parameter	Measured	Units
K_1	0.198	Volt/rad
K_2	5.6	N/A
K_3	$503\pi \cdot 10^3$	rad/s/Volt
$K_3/4$	$126\pi \cdot 10^3$	rad/s/Volt

Table 5.3. Measured loop gains

filter noise bandwidth $F_{n_{3dB}}$ has to be determined. Then, ω_n can be found since the damping constant is known. The loop filter noise bandwidth $F_{n_{3dB}}$ is found at the intersection point where the VCO phase noise crosses the in-band PLL phase noise. To measure adequately the optimum intersection point, the VCO phase noise is plotted from 10 kHz to 10 MHz, as well as a temporary wide band closed loop on the same scale. The intersection point defines the desired frequency $F_{n_{3dB}}$ and the experiment showed that it has to be set to 325 kHz. Then, from Smith [1], with $\zeta < 1$, ω_n is found,

$$\omega_n = \frac{2\pi \cdot F_{n_{3dB}}}{(1 - 2\zeta^2 + (2 - 4\zeta^2 + 4\zeta^4)^{1/2})^{1/2}} \quad (5.3)$$

$$= \frac{2\pi \cdot 325 \cdot 10^3}{(1 - 2(0.5)^2 + (2 - 4(0.5)^2 + 4(0.5)^4)^{1/2})^{1/2}} \quad (5.4)$$

$$= 1.604 \cdot 10^6 \frac{rad}{s}. \quad (5.5)$$

The loop filter components should now be defined according to

$$\omega_n = \sqrt{\frac{K}{\tau_1}} \quad (5.6)$$

and

$$2\zeta\omega_n = \frac{K\tau_2}{\tau_1}. \quad (5.7)$$

Then, with an arbitrary capacitor value of $C=390$ pF,

$$R1 = 435 \Omega \sim 430 \Omega \quad (5.8)$$

$$R2 = 1592 \Omega \sim 1600 \Omega \quad (5.9)$$

The open and closed loop transfer functions $H_o(j\omega)$ and $H(j\omega)$ are plotted in magnitude and phase, and are presented on Figure 5.3. With a damping constant set to 0.5, the product $2\zeta\omega_n$ is located at the same angular frequency point as $1/\tau_2$. The open loop phase shift is then -135° and the natural angular frequency ω_n is found to be $1.6 \cdot 10^6$ rad/s. The 3 dB cut-off noise bandwidth is located at $2.04 \cdot 10^6$ rad/s in accordance with Equation 5.3. The phase margin ϕ_m is found at $2\zeta\omega_n$ and has a value of 45° . Figure 5.2 shows the implemented loop filter with component values.

Figure 5.2. Implemented loop filter topology with component values

5.4 Functionality Sub-Circuits

This section discuss the design and measured performance of the remaining blocks used for the PLDRO prototype. While some sub-circuits are not essential to

Figure 5.3. Open and closed loop transfer functions

render the push-push PLDRO prototype functional, they were primarily implemented to meet typical LO requirements for broadband microwave radios.

5.4.1 3-dB Hybrid Coupler

To close the phase locked loop, the DRO output signal has to be fed back into the PD. At microwave frequencies sampling can be implemented with different topologies. Whether sampling is done via microstrip coupled lines, a T-junction, a resistive network or a directional coupler, the main purpose is to take some power from the main source and redirect it towards another circuit. For the PLDRO application, a 3-dB hybrid coupler was designed [24],[25] to sample the 12 GHz DRO output and

transfer half of the signal power to the divide-by-4 circuit. It may sound exaggerated to sample the DRO power to this extent but, since it is difficult to predict with certainty the final push-push DRO output power, one may prefer to have more than enough power to operate the divide-by-4 circuit. If, for instance, the power level is too high and can damage the circuit, a resistor network is easily implemented. The design is centered at 12 GHz and has a 33% fractional bandwidth. Figures 5.4 and 5.5 show the 3-dB hybrid simulated and measured scattering parameters. The 3-dB hybrid isolated port has a 50 ohm load to prevent any isolated port leakage from being reflected back in to the coupler.

Figure 5.4. 3-dB hybrid simulated scattering parameters

At 12 GHz, the 3-dB hybrid presents 6 dB insertion loss and -24 dB input match. This is in good agreement with simulation results where the insertion loss is 4.5 dB and the input match -35 dB. The measurement differences are mainly due to the fact that the connectors and the coaxial-to-microstrip transition were not de-embedded from the circuit.

Figure 5.5. 3-dB hybrid measured scattering parameters

5.4.2 Divide-by-4 Circuit and Gain Stage

The purpose of this circuit is to sample the 12 GHz signal from the 3-dB hybrid output and divide it down to 3 GHz. It is important to remember that this 3 GHz signal becomes the "VCO feedback" or the $y_o(t)$ signal to be locked to the multiplied reference signal $y_i(t)$. The divider is a packaged HMC365-MMIC from Hittite. The manufacturer does not specify what divider topology is used to perform the division function but, it can be shown that a simple circuit [26] can perform the frequency division function. Figure 5.6 presents a conventional block diagram for a regenerative divider topology. The divider circuit can be explained easily by adapting it to our application. The output frequency F_{out} needed to lock the loop has to be 3 GHz. Considering an input frequency F_{in} of 12 GHz, the divide ratio becomes $N=4$. The internal multiplier becomes a tripler and provides a fixed frequency $F=9$ GHz to the mixer. The mixer output frequency of interest, F_{out} , is the difference between F_{in} and F . Other mixing products and harmonics are filtered out. Obviously, this is

Figure 5.6. Conventional microwave divide-by-N topology

Parameter	Conditions	Min.	Typ.	Max.	Units
Max. Input Freq.	-	13	14	-	GHz
Min. Input Freq.	Sine Wave	-	0.2	0.5	GHz
Input Power Range	$F_{in} = 11 \text{ to } 13 \text{ GHz}$	-5	> -8	+3	dBm
Output Power	$F_{in} = 13 \text{ GHz}$	2	5	-	dBm
Reverse Leakage	Terminated Outputs	-	45	-	dB
$L_{ssb}(100 \text{ kHz Offset})$	$P_{in} = 0 \text{ dBm}, F_{in} = 6 \text{ GHz}$	-	-151	-	dBc/Hz
Supply Current	-	-	110	-	mA

Table 5.4. Hittite frequency divider HMC365SG8 specifications

a simple steady state analysis but sufficient to understand the fundamental division concept. Table 5.4 presents the manufacturer's divide-by-4 specifications.

The square wave divider output waveform has to be amplified and filtered to meet the PD mixer's LO requirements. Indeed, the divided-down 3 GHz signal $y_o(t)$ becomes the "LO" drive to the passive phase detector mixer and requires typically a 15 dBm sinusoidal waveform to operate properly. A 17 dBm P_{1dB} HBT MMIC gain block is used to increase the divide-by-4 output drive before the 3 GHz BPF filtering.

The filter selects the fundamental tone and rejects most of the power present at other harmonics. Thus, a 3 GHz sinusoidal waveform of 15 dBm output power is present at the mixer LO port for phase detection. Figure 5.7 shows the PLDRO feedback topology that divides the DRO frequency for phase detection purposes.

Figure 5.7. Feedback circuit topology

5.4.3 12 GHz Band-Pass Filter

The 12 GHz BPF is implemented at the PLDRO output before the final buffering stage. The purpose of filtering the PLDRO output is to reduce the harmonic and sub-harmonic level contents. All of the unwanted tones are expected to be attenuated considerably through this element. The filter is a 4th order Tchebychev with 0.5 dB in-band ripple and 1200 MHz passband. The implementation technique is parallel coupled lines on microstrip. The filter insertion loss is 5 dB and rejects the 6 GHz push-push DRO fundamental and its third harmonic by more than 60 dBc. Figures 5.8 and 5.9 show the 12 GHz BPF simulated and measured scattering parameters respectively.

Figure 5.8. 12 GHz band-pass filter simulated scattering parameters

Figure 5.9. 12 GHz band-pass filter measured scattering parameters

While it may not be necessary to reduce the harmonics and sub-harmonics to this extent in a radio design, the BPF addition shows that the output spectrum undesired tones can be easily attenuated.

5.4.4 Output Buffer Stage

The output buffer is implemented on the PLDRO prototype to reduce any form of pulling from the output load Z_L . Indeed, the buffer is designed with two cascaded elements, with each one providing 22.5 dB reverse gain S_{12} . Hence, a total

of 45 dB isolation acts as a huge attenuator for any reflected signal at the PLDRO output port. Without the buffer, the DRO sensitivity to Z_L could cause the PLL to fail to track the DRO, reduce the acquisition bandwidth and even completely kill the oscillation frequency. The buffer stage is also implemented to provide enough output drive to be used in most radios and operates in a fully saturated mode to minimize output power variations due to temperature or manufacturing.

The designed buffer consists of two low noise NE32584C-PHEMT device from NEC, with scattering parameters provided in Appendix C, Table C.2. The devices are matched using double-stub matching networks to -10 dB over a 4 GHz frequency band. The measured buffer has 20 dB gain at 12 GHz and 12 dBm P_{1dB} . The buffer amplifies the 0 dBm DRO output signal by 20 dB, but saturates at 15 dBm or P_{5dB} . The reverse gain S_{12} of 44 dB provides excellent isolation to the DRO. Thus, load pulling has practically no effect on the loop behavior. Figure 5.10 presents the simulated buffer scattering parameters and Figure 5.11, the simulated source and load stability circles from 6 GHz to 18 GHz on an expanded Smith chart.

Figure 5.10. Output buffer simulated scattering parameters

Figure 5.11. Output buffer simulated stability circles

Chapter 6

Push-Push PLDRO Closed Loop Performance

6.1 Introduction

In this chapter, the push-push PLDRO closed loop performance is analyzed with a major emphasis on the frequency spectrum tone levels and phase noise. Initially, the spectrum analyzer (*SA*) limits in a low phase noise environment are discussed. Then, the frequency spectrum and phase noise are measured and discussed in a phase-locked and a free-running environment. Finally, acquisition, tracking and mechanical tuning are discussed. The complete push-push PLDRO block diagram is shown in Figure 6.1. The measured data can be referred to this block diagram to assess correctly at which point on the prototype a specific measurement is taken. For frequency multiplication and division, the generally accepted $20 \log(N)$ rule is used by the author to compare and predict the phase noise degradation or improvement

Figure 6.1. Complete push-push PLDRO block diagram

for a given signal.

6.2 HP8564 Spectrum Analyzer Performance Analysis

The measured data are taken from an Agilent 8564 spectrum analyzer. This instrument has a "Phase Noise" soft key option that measures phase noise density around the carrier. While interesting and user friendly, this feature does not distinguish whether the jitter is coming from the signal phase or amplitude. Consequently, it may induce measurement errors in the sense that AM noise is not

de-embedded from the PM noise. However, in a microwave oscillator, the PM noise is usually the dominant noise factor close to the carrier. The AM noise does not generally interfere with the PM noise below 500 kHz offset from the carrier. The spectrum analyzer 130 dBc maximum dynamic range is expected to impede the prototype phase noise at large frequency offsets from the carrier (i.e. 1 MHz to 10 MHz). This is taken into account when discussing phase noise plots, and a dashed line shows the actual expected phase noise if the instrument had a better dynamic range. The instrument internal LO dictates the lowest possible measurable phase noise. Indeed, if the device under test (*DUT*) has a phase noise density much lower than the instrument LO phase noise, the measured noise from the instrument will be its own phase noise and obviously not very helpful to characterize the DUT. Figure 6.2 presents the LO phase noise from the Agilent 8564 spectrum analyzer for various frequencies of operation. Thus, this instrument, while not ideal because of its limited dynamic range close to the carrier, should give reasonably good estimates of the phase noise if one knows how to interpret the measured data.

6.3 Push-Push PLDRO Output Power and Frequency

The exact output frequency of the PLDRO is dictated by the 100 MHz reference. The measured PLDRO output frequency is $F_{Lock}=11.9999967$ GHz viewed in a 2 MHz span and at room temperature. This is not in agreement with the OCXO stability of ± 100 ppb, which correspond to a ± 1200 Hz window at 12 GHz. The measured output frequency is -3300 Hz away from the 12 GHz center frequency. A frequency counter should be used to measure and characterize the PLDRO short term frequency drift instead of the spectrum analyzer. This instrument would have

Figure 6.2. Agilent 8564 spectrum analyzer phase noise floor

shown the output frequency well within specifications, especially at room temperature. However, If the SA were set to a smaller frequency span (i.e. 100 kHz instead of 2 MHz), the frequency reading from the instrument would probably be within specifications.

The PLDRO output power expected was 15 dBm from full saturation of the output buffer second stage. The measured power of 14.17 dBm on the SA is attenuated by a 1.0 dB cable loss. Thus, the actual measured power is 15.17 dBm.

6.4 12 GHz Broadband Spectrum without 12 GHz BPF

In this section, the output PLDRO spectrum is measured and discussed without the 12 GHz output BPF. Each figure is presented under various frequency spans to add emphasis to specific tone rejection. Figure 6.3 shows the PLDRO under a 40 GHz span view. The desired tone is located at 12 GHz and the 24 GHz second harmonic is rejected by 23 dBc. Figure 6.4 presents the 12 GHz desired tone with the 6 GHz push-push fundamental and its 18 GHz third harmonic. The push-push fundamental is rejected by 37.67 dBc while the third harmonic is 41.5 dBc below the desired signal. Figure 6.5 shows the 12 GHz PLDRO output with a 7 GHz frequency span to put emphasis on the tones generated by the frequency divider. This divider produces 3 GHz spaced tones around the carrier. The 9 GHz tone is -62.5 dBc and the 15 GHz tone is higher in amplitude at -54.5 dBc. The divider, consequently, adds power on the 6 GHz push-push fundamental seen at the output, but the measurement distortion is minimal considering the 6 GHz tone generated by the divider is approximately 20 dB below the 6 GHz push-push fundamental.

Figure 6.3. 40 GHz PLDRO output spectrum without 12 GHz BPF

Figure 6.4. 14 GHz PLDRO output spectrum without 12 GHz BPF

Figure 6.5. 7 GHz PLDRO output spectrum without 12 GHz BPF

6.5 12 GHz Broadband Spectrum with 12 GHz BPF

In this section, the output PLDRO spectrum is measured and discussed with the 12 GHz output BPF in place. This filter is intended to reduce the 6 GHz push-push fundamental and its 18 GHz third harmonic. The undesired tones at 9

GHz and 15 GHz of the divider are also expected to be suppressed considerably by this filter. Figure 6.6 presents the 12 GHz frequency viewed in a 14 GHz span. The filter did reduce the unwanted 6 GHz and 18 GHz tones by 20 dBc. This reduction is well below the filter measured scattering parameters rejection of more than 60 dBc. Also, the filter did not reduce the 9 GHz and the 15 GHz tones generated by the divider as seen in Figure 6.7. From the filter transfer function, these tones should have been reduced by about 45 dBc. Knowing that the filter itself performs well (Ref: Fig. 5.9), the worse than expected tone reduction is probably due to the fact that the circuit is not correctly isolated, and a proper housing for the PLDRO prototype will have to be implemented to improve rejection. Another important factor to consider is a possible coupling through the D.C. lines, reaching to the buffer stage and bypassing the 12 GHz filter. To reduce the unwanted tones coupling through the D.C. lines, simple series inductors or more elaborate filter designs could be implemented. The filter insertion loss at 12 GHz can be deduced by comparing both signals when the filter is incorporated. The measured filter insertion loss is in the neighborhood of 5 dB, in agreement with simulated and measured data.

Figure 6.6. 14 GHz PLDRO output spectrum with 12 GHz BPF

Figure 6.7. 7 GHz PLDRO output spectrum with 12 GHz BPF

6.6 12 GHz Close-in Spectrum

The PLDRO close-in spectrum view is of interest because it helps determine the 3 dB loop bandwidth $F_{n_{3dB}}$, the loop stability, the noise density around the carrier and the presence of any undesired spurs. Since the PLDRO uses a 100 MHz reference to lock the free-running DRO, it is probable that the multiplied 100 MHz spurs could show up at the output because of finite isolation. Electrically, the 100 MHz spurs have two RF paths to follow in order to be present at the output. The first RF path is from the multiplier output into the phase detector, then through two reverse amplifiers, back into the divider and finally through the 3-dB hybrid. This path has 120 dB attenuation. The second RF path is from the the multiplier output, into the phase detector and through the loop filter. This path, is considered to be highly selective and narrow-band due to the PLL loop filter. Thus, the 100 MHz spurs are unlikely to be measurable at the PLDRO output for either RF path. Figure 6.8 shows the 12 GHz spectrum under a 250 MHz span.

Figure 6.8. Push-push PLDRO 250 MHz output spectrum

The spurs are showing up at the output at -72 dBc and spaced 100 MHz from the PLDRO center frequency. The 100 MHz spurs were expected to be present at the output but below -100 dBc, according to the first RF path isolation of -120 dBc plus some leakage. While the reference spurs are worse than expected, this is well within commercial spur specification of -65 dBc. To reduce the reference spurs at the output spectrum, the reference multiplier and the push-push DRO should be shielded to improve the overall isolation.

The PLDRO noise bandwidth $F_{n_{3dB}}$ can be approximately measured by looking in a 2 MHz span. From Figure 6.9, it is possible to detect the VCO noise and the in-band noise separation. The VCO noise drops quickly in the neighborhood of 360 kHz offset, while the in-band noise, which is closer-in to the carrier, would tend to flatten out over this frequency point. Obviously, if the loop were under damped, it would be easier to accurately find the loop bandwidth. The 360 kHz measured point is close to the previously measured 325 kHz $F_{n_{3dB}}$. To recall, the 325 kHz was measured with the PLDRO locked into a wide loop bandwidth and compared to the

DRO free-running phase noise.

Figure 6.9. Push-push PLDRO 2 MHz output spectrum

6.7 Free-Running Push-Push DRO Phase Noise at 3 GHz and 12 GHz

In this section, the 3 GHz multiplier and divided-down DRO output phase noise along with the 12 GHz push-push DRO phase noise is measured and discussed. For a system perspective, the integrated phase noise is also measured and presented in Table 6.1. The 3 GHz reference multiplier signal $y_i(t)$ is plotted on the same scale as the divided-down 3 GHz DRO signal $y_o(t)$. Figure 6.10 shows the phase noise of both signals. The thick line is the instrument noise floor at 3 GHz. The SA 130 dBc dynamic range at 3 GHz does not limit the reference phase noise measurement at large offset frequencies. Indeed, the multiplier reference noise with the NF contributors was expected to reach a floor at -130 dBc. However, better dynamic range would have shown the multiplier reference floor levelling at -130 dBc and being steady while

the divided-down DRO would have followed the thick dashed line to the instrument dynamic range limit.

Figure 6.10. 3 GHz reference and divided-down DRO L_{ssb} phase noise

The 12 GHz push-push DRO free-running phase noise has to be characterized to be able to correctly set the filter loop bandwidth. The phase noise is plotted from 10 kHz to 10 MHz offset with the divided-down DRO output on the same scale on Figure 6.11.

Figure 6.11. 3 GHz divided-down and 12 GHz DRO L_{ssb} phase noise

The 12 GHz signal has a larger phase noise density than its divided-down counterpart. This is in agreement with the frequency division and phase noise relation. One should see a 12 dB improvement in phase noise on the divided-down DRO signal. At 100 kHz offset, the phase noise improvement is actually 12 dB, in agreement with the $20\log(N)$ rule. Closer to the carrier (i.e. <40 kHz), the noise difference spreads out. The measurement close to the carrier are more or less valid because the 12 GHz DRO signal is jittery and difficult to characterize adequately. For offsets larger than 400 kHz, the phase noise difference tends to be reduced. At 1 MHz offset, the 12 dB improvement is only 3 dB. This is explained by the SA limited dynamic range. The instrument floor is adding to the 3 GHz divided-down DRO and reduces the expected 12 dB noise difference.

6.8 Phase Locked Push-Push DRO Phase Noise

The previous section discussed the push-push DRO free-running phase noise along with its divided-down signal $y_o(t)$ and the multiplied reference $y_i(t)$. The objective of phase locking the 12 GHz push-push DRO to the 100 MHz crystal reference is to improve its short term stability. By locking the DRO to the reference, a considerable amount of phase jitter is removed. Figure 6.12 presents the 12 GHz PLDRO output phase noise and the HP8564 spectrum analyzer noise floor. Figure 6.13 compare the phase locked and free-running 12 GHz DRO. RF radio system architects often need to compute the local oscillator integrated phase noise. The integrated phase noise is the total LO noise within a specified bandwidth measured in radians or degrees. It is convenient to have the integrated phase noise to compare different local oscillators. Indeed, it is tedious to tell which LO has less phase noise when the

noise density is specified at various frequency offsets. To understand to what extent the phase lock circuit reduces the DRO phase jitter, the integrated phase noise for the free-running and the locked DRO are measured. The multiplied 3 GHz reference and the divided-down DRO integrated phase noise are also measured and shown in Table 6.1 for various frequency bandwidths.

Figure 6.12. 12 GHz PLDRO L_{ssb} phase noise with corresponding HP8564 L_{ssb} phase noise floor

Figure 6.13. Locked and free-running 12 GHz DRO output phase noise comparison

Section Under Test	Integrated Noise (rad.)	Phase Noise Density
12 GHz PLDRO	0.0036	114.6X less
12 GHz DRO (10 kHz to 10 MHz)	0.4126	
12 GHz PLDRO	0.0038	1.9X more
3 GHz REF. (100 Hz to 10 MHz)	0.0020	
12 GHz DRO	0.4126	25.5X more
3 GHz DRO (10 kHz to 10 MHz)	0.0162	
12 GHz DRO	0.4126	257.9X more
3 GHz REF. (10 kHz to 10 MHz)	0.0016	
3 GHz DRO	0.0888	49.3X more
3 GHz REF. (1 kHz to 10 MHz)	0.0018	

Table 6.1. 12 GHz push-push PLDRO integrated phase noise

The phase lock circuitry does reduce the DRO phase noise considerably. From 10 kHz to 10 MHz offset from the carrier, the integrated phase noise is reduced by a factor of 114.6. If it were possible to measure the 12 GHz DRO closer to carrier (i.e. 1 kHz or lower), the phase lock circuitry would be seen to reduce the phase noise by a much larger factor. The free-running DRO is too jittery to measure closer than 10 kHz but, a measurement from 1 kHz would have shown a higher density of noise from the DRO. Hence, a larger reduction in phase noise is achieved when locked. Another point of interest is to compare the multiplied 3 GHz reference $y_i(t)$ to the actual 12 GHz PLDRO phase noise plotted in Figure 6.14. From 100 Hz to 10 MHz offset, the 12 GHz PLDRO presents 1.9 times more integrated phase

noise. If one wanted to compare both signals, it is obvious to tell which one is effectively noisier. But, to tell to what extent one signal is noisier than the other one, a numerical integration of each plot is required. The SA integrated noise feature does this integration and gives the answer in radians or degrees. With the integrated phase noise, the noise density is quickly verified and quantified. Then, the LO noise contribution can be easily incorporated into the link budget.

Figure 6.14. 3 GHz $y_i(t)$ and 12 GHz PLDRO output phase noise with corresponding HP8564 noise floor

6.9 Tracking, Acquisition and Mechanical Tuning Bandwidth

This section discusses tracking, acquisition and mechanical tuning bandwidth of the prototyped 12 GHz PLDRO. The phase lock circuitry tracks the divided-down free-running DRO $y_o(t)$ and locks it to the reference signal $y_i(t)$. However, the

DRO can not be tuned further than 2.5 MHz, limited by its voltage control design. Thus, if the DRO oscillation condition changes to the point that it is off frequency by more than the 2.5 MHz tuning capacity, the PLL will not be able to keep the DRO locked to the reference signal. Hence, for the DRO just outside the tuning bandwidth, the PLL tries to acquire the signal but fails. Figures 6.15 and 6.16 present the PLDRO output when the DRO is detuned ± 1.5 MHz.

Figure 6.15. 12 GHz PLDRO in acquisition mode, DRO detuned -1.5 MHz

Figure 6.16. 12 GHz PLDRO in acquisition mode, DRO detuned +1.5 MHz

In Figures 6.15 and 6.16, the center of the chart is located at 12 GHz. The tone present at this point corresponds to the 4th harmonic of $y_i(t)$. The other frequency modulated spurs are generated by the DRO output. Since the DRO is unlocked by 1.5 MHz, the PD output generates a 375 kHz sinusoidal beat note. This is an excessive modulation bandwidth for this DRO. Consequently, the DRO output generates frequency modulated spurs at its output which are related in amplitude to those of Bessel functions.

From Chapter 2, Equation 2.72, the PLL with a perfect integrator with phase lead correction network will always acquire, unless the signal to acquire is outside the VCO tuning range. The prototyped PLDRO used a high gain loop filter with phase lead correction network. This loop filter is considered to behave close to a perfect integrator and should follow the acquisition pattern of Figure 2.12(P.30). The tested PLDRO is able to acquire the signal over the entire tuning range of the DRO. If the DRO had a wider tuning bandwidth (i.e. ≥ 15 MHz), one could expect the PLDRO to acquire the signal across the DRO tuning bandwidth.

The mechanical tuning bandwidth is also of interest. In a production environment, it is difficult to keep the DRO frequency of oscillation within the desired frequency bandwidth. Thus, it is a necessity, in volume production, to install a mechanical tuner to adjust the frequency of oscillation. As a rule of thumb, a mechanical tunability of 1% is generally sufficient to compensate for the DRO frequency variations. A good tuner design should allow the DRO frequency to be set without difficulty to $F_0 = F_{Lock} - ElecBW/2$, without being too sensitive. The implemented tuner moves the DRO frequency over a 85 MHz span. This corresponds to a 0.71% fractional bandwidth. The mechanical tuner tunes smoothly across the band and

does not affect the amplitude of oscillation. The tuning element is made of solid brass and has self locking threads that prevent any frequency detuning from vibrations. For the PLDRO prototype, the free-running DRO frequency F_0 is set to 11.99875 GHz according to Equation 3.26. Figure 6.17 presents a plot of the DRO mechanical tuning bandwidth.

Figure 6.17. Push-push DRO mechanical tuning bandwidth

Chapter 7

Conclusion

7.1 Summary

The objective of this thesis was to investigate a new low cost PLDRO topology that could easily be manufacturable and result in an excellent local oscillator solution for the next generation of broadband wireless applications.

Chapter 2 discussed the phase locked loop fundamentals. The theory was intended to familiarize the reader with the PLL building blocks, linear operation and natural acquisition for a second order loop. The chapter also discussed various loop filter topologies. The integrator with phase lead correction network was selected for the 12 GHz PLDRO prototype.

Chapter 3 discussed the push-push dielectric resonator oscillator design, simulation and measured performance. The dielectric resonator $TE_{01\delta}$ electromagnetic fields were derived and the resonant frequency was computed, using the transcendental equation for the actual dielectric resonator dimensions. The fundamental

6 GHz oscillator design and the push-push concept were analyzed and simulated. The push-push DRO sensitivity constant, pushing figure, phase noise and frequency spectrums were measured.

Chapter 4 discussed the reference multiplier theory, design and measured performances. The step recovery diode multiplier theory and design was presented and the efficiency discussed. The crystal 100 MHz reference spectrum, stability and phase noise was discussed, as was the multiplied 3 GHz reference signal. The overall multiplier chain was measured and its conversion loss established.

Chapter 5 examined the phase detector, the loop filter and all the sub-circuits designs to render the PLDRO fully functional and implementable for a wireless radio. The phase detector measurement setup was discussed and the sensitivity constant measured. The loop filter design was detailed with a step-by-step methodology. The sub-circuit design, simulation and measured data were also discussed.

Chapter 6 discussed the 12 GHz push-push PLDRO prototyped. A discussion on the instrument used for the measurements detailed the limits of the instrument and how this affected the measured data. The output frequency and power was analyzed. The PLDRO frequency spectrums at various point on the circuit showed good harmonic rejections and low levels of unwanted tones. The phase noise and the integrated phase noise was measured and discussed in free-running and phase locked environments. A discussion on frequency tracking, acquisition and mechanical tuning bandwidth concluded the chapter.

7.2 Contribution of Thesis

This thesis demonstrated a new PLDRO approach using push-push DRO in combination with an IF frequency mixer and a divide-by-4 prescaler. This is, to the author knowledge, a new topology for commercial and military PLDROs. Indeed, commercially available PLDROs use fundamental DROs instead of push-push DROs. Also, the phase comparison is implemented at the final output frequency through a sampling phase detector most of the time.

This work presented a push-push approach to reduce oscillator sensitivity to manufacturing. The push-push fundamental oscillates at half the output frequency, thus considerably reducing the sensitivity to parasitics, the DR position and the influence of active devices on the frequency of oscillation.

This work presented phase detection and locking circuitry at 3 GHz IF. This was intended to reduce design sensitivity and improve production reliability. The phase detection at 12 GHz realized with a sampling phase detector is generally weak and has unpredictable PD sensitivity. This 3 GHz IF approach, however, provides PD sensitivity consistency by setting the desired power level to the RF and LO port of the mixer. A good PLDRO design should minimize the VCO modulation sensitivity and maximize the PD sensitivity in order to minimize phase noise and reduce sensitivity to microphonics. The designed prototype presented excellent PD sensitivity and minimal VCO modulation sensitivity.

7.3 Further Studies

The present work raised questions which would need to be answered in future work for this type of PLDRO.

The push-push DRO electrical tuning bandwidth was below expectations. The author expected a tuning bandwidth from 10 MHz to 15 MHz, but the prototyped DRO had only 2.5 MHz tuning bandwidth. From the author's previous designs on DRO, the average tuning bandwidth for a drain-to-gate fundamental DRO around 12 GHz would be about 10 MHz to 20 MHz. The push-push topology might be harder to pull, or a different tuning circuit may have to be implemented to improve tunability.

The DRO reduced tuning bandwidth has limited the research on acquisition. While the theory of a perfect integrator with phase lead correction network ensures infinite signal acquisition, the author's previous work on PLDRO has shown acquisition bandwidth limitations. In this work, the acquisition was measured and found to agree with the perfect integrator theory. If the DRO tuning bandwidth were in the 10 MHz to 15 MHz range, the PLDRO acquisition would have been tested to a better extent. Further work is required on the DRO tuning bandwidth to fully characterize the acquisition characteristics for this push-push PLDRO concept.

The prototype PLDRO had 100 MHz spurs above the predicted power level. A proper housing needs to be designed to improve isolation from the 3 GHz reference multiplier and the push-push DRO to prevent leakage and coupling. The broadband PLDRO spectrum when fed into the 12 GHz BPF had harmonic content higher than predicted. The output buffer is thought to have picked up RF signals through its D.C. bias lines. More research and investigation is needed to resolve these issues.

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Appendix A

Dielectric Resonator Resonant Frequency

Maple Script for "Dielectric Resonator Resonant Frequency Computation":

Input Variables: radius (a); length (L); dielectric constant (ϵ_r).

Output: resonant frequency (F_0).

Measured DR parameters:

$$a=4.3307 \times 10^{-3} \text{m} ; L=3.0226 \times 10^{-3} \text{m} ; \epsilon_r=46.2 ; c=3 \times 10^8 \text{m/s}.$$

Propagation constant outside the dielectric region is imaginary (medium = air):

$$\alpha = \sqrt{\left(\frac{2.405}{a}\right)^2 - \left(\frac{2\pi f}{c}\right)^2}. \quad (\text{A.1})$$

Propagation constant inside the dielectric region is real (medium = dielectric):

$$\beta = \sqrt{\left(\frac{\epsilon_r 2\pi f}{c}\right)^2 - \left(\frac{2.405}{a}\right)^2}. \quad (\text{A.2})$$

The possible frequency range ($f1_{puck}$ to $f2_{air}$) for this solution has to be within the dielectric or air wavelength " c_{ϵ_r} " or " c " respectively,

$$f1_{puck} = \frac{c(2.405)}{2\pi\sqrt{\epsilon_r}a} \quad (A.3)$$

$$= 3.901 \text{ GHz} \quad (A.4)$$

$$f2_{air} = \frac{c(2.405)}{2\pi a} \quad (A.5)$$

$$= 26.515 \text{ GHz}. \quad (A.6)$$

The transcendental equation 3.19 is then computed,

$$\begin{aligned} EQ := \tan\left(\frac{1}{2}\sqrt{.4386511360 \cdot 10^{-15} \epsilon_r f^2 - 5.784025 \frac{1}{a^2}} L\right) = \\ \frac{\sqrt{5.784025 \frac{1}{a^2} - .4386511360 \cdot 10^{-15} f^2}}{\sqrt{.4386511360 \cdot 10^{-15} \epsilon_r f^2 - 5.784025 \frac{1}{a^2}}}. \end{aligned}$$

The roots of the transcendental equation represent the possible solutions to this equation:

$$\begin{aligned} FreqRes_Root := \text{RootOf}\left(\tan\left(\frac{1}{2}\sqrt{\frac{.4386511360 \cdot 10^{-15} \epsilon_r Z^2 a^2 - 5.784025}{a^2}} L\right) \right. \\ \left. \sqrt{\frac{.4386511360 \cdot 10^{-15} \epsilon_r Z^2 a^2 - 5.784025}{a^2}} \right. \\ \left. - \sqrt{\frac{-5.784025 + .4386511360 \cdot 10^{-15} Z^2 a^2}{a^2}}\right). \end{aligned}$$

Only one solution can solve the transcendental equation. The resonant frequency found by MapleV is,

$$F_0 = 5.387 \text{ GHz} \quad (A.7)$$

This result agrees with theoretical expectations of a solution to within 10% of the actual desired resonant frequency of 6 GHz. This computed result is within 10.21% of the targeted 6 GHz self resonance.

Appendix B

Matlab Script for the Loop Filter Analysis

```

% Date April/28/03
% This script plots the open and closed loop transfer functions in magnitude and phase
% for the 12 GHz Push-Push PLDRO. Loop Gain "K" is established at 3 GHz where the
% phase detection takes place.
w1=1e5:1000:1e8;
w2=1e5:1000:1e8;
w3=1e5:1000:1e8;
% K1-> Phase Detector gain (V/rad) ; K2-> Loop Amplifier Gain ; K3 -> (1/4)*VCO Gain (rad/s/V)
K1=0.198;K2=5.6;K3=395840;
% K -> Synchronization Gain
K=K1*K2*K3;
% Integrator parameters
R1=430;R2=1600;C=390e-12;
% Time constants
t1=R1*C;t2=R2*C;
% Damping factor
Zeta=(K*t2)/(2*sqrt(K/t1)*t1);
% Natural angular frequency
O_n=sqrt(K/t1);
% Noise bandwidth
F_n=(2*Zeta*O_n)/(2*3.14159);
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% Open Loop Ho(s) %%%%%%%%%%%%%%
N1=K*(1+i*w1*t2); % See EQ(2.43)
D1=(t1*(i*w1).^2);
h01=(N1)./(D1);
module_h01=abs(h01);
module_h01_db=10*log10(module_h01);
phase_h01=57.2957795*angle(h01); %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% Closed Loop H(s) %%%%%%%%%%%%%%
A=(K/t1);% (Omega_n)^2
B=K*(t2/t1);% 2*Zeta*Omega_n
h1=(B*(w1)+A)./(w1.^2+B*(w1)+A);
module_h1=abs(h1);
module_h1_db=10*log10(module_h1);
h2=(B*(i*w1)+A)./((i*w1).^2+B*(i*w1)+A);
phase_h2=57.2957795*angle(h2);

subplot(4,1,1);
% hold on;
semilogx(w1,module_h01_db, ylabel('|Ho(s)| (dB)'), grid; % title('Loop Filter Transfer Function F(s)');
subplot(4,1,2);
semilogx(w1,phase_h01, ylabel('Ho(s) (deg.)'), grid;
subplot(4,1,3);
semilogx(w2,module_h1_db, ylabel('|H(s)| (dB)'), grid;
subplot(4,1,4);
semilogx(w3,phase_h2, xlabel('Angular Frequency in rad/s'), ylabel('H(s) (deg.)'), grid;

```

Appendix C

Active Device Scattering Parameters

<i>Freq. (GHz)</i>	<i>S11 (M, P)</i>	<i>S21 (M, P)</i>	<i>S12 (M, P)</i>	<i>S22 (M, P)</i>
2	0.933 ; -47.607	5.045 ; -42.992	0.339 ; +63.174	0.351 ; -37.001
3	0.877 ; -68.320	4.717 ; -61.370	0.055 ; + 1.978	0.335 ; -49.232
4	0.808 ; -87.155	4.453 ; -79.598	0.068 ; +41.075	0.334 ; -62.513
5	0.750 ; +72.459	4.194 ; +81.665	0.079 ; +29.118	0.306 ; -81.534
6	0.678 ; +49.307	3.895 ; +63.961	0.087 ; +17.565	0.278 ; +83.550
7	0.620 ; +27.350	3.595 ; +47.255	0.094 ; + 6.898	0.243 ; +70.188
8	0.586 ; + 5.818	3.308 ; +31.528	0.098 ; - 3.979	0.207 ; +54.237
9	0.561 ; -13.937	3.072 ; +16.842	0.101 ; -13.283	0.171 ; +39.289
10	0.536 ; -34.520	2.882 ; + 2.187	0.105 ; -22.691	0.164 ; +20.114
11	0.526 ; -56.793	2.704 ; -12.515	0.109 ; -32.306	0.155 ; - 0.121
12	0.549 ; -76.724	2.608 ; -28.137	0.112 ; -40.945	0.160 ; -17.281
13	0.589 ; +86.390	2.392 ; -42.967	0.115 ; -49.881	0.151 ; -42.325
14	0.614 ; +71.978	2.263 ; -57.082	0.120 ; -58.258	0.170 ; -59.816
15	0.624 ; +54.857	2.150 ; -72.458	0.125 ; -68.792	0.200 ; -80.830
16	0.639 ; +35.830	2.011 ; -88.176	0.129 ; -80.172	0.237 ; +81.791
17	0.667 ; +19.792	1.836 ; +77.099	0.129 ; +88.464	0.265 ; +67.797
18	0.699 ; + 8.802	1.683 ; +63.800	0.128 ; +78.734	0.270 ; +54.487
19	0.698 ; - 0.258	1.606 ; +50.560	0.133 ; +68.318	0.267 ; +43.788
20	0.695 ; - 7.976	1.474 ; +37.476	0.122 ; +54.931	0.313 ; +30.085
21	0.706 ; -28.235	0.517 ; +22.643	0.139 ; +47.186	0.289 ; +10.863
22	0.704 ; -47.245	1.466 ; + 5.283	0.141 ; +32.599	0.291 ; - 4.024

Table C.1. MESFET "AFM04P3" scattering parameters

<i>Freq. (GHz)</i>	<i>S</i> 11 (<i>M, P</i>)	<i>S</i> 21 (<i>M, P</i>)	<i>S</i> 12 (<i>M, P</i>)	<i>S</i> 22 (<i>M, P</i>)
1	0.987 ; - 18.65	6.432 ; +161.14	0.014 ; +77.38	0.502 ; - 14.91
2	0.958 ; - 36.35	6.243 ; +143.49	0.027 ; +65.71	0.496 ; - 28.84
3	0.925 ; - 53.13	5.999 ; +126.61	0.038 ; +55.04	0.487 ; - 41.96
4	0.879 ; - 69.42	5.734 ; +110.09	0.048 ; +44.64	0.474 ; - 54.20
5	0.821 ; - 84.79	5.417 ; + 94.24	0.056 ; +34.90	0.454 ; - 65.25
6	0.757 ; - 99.35	5.121 ; + 79.85	0.062 ; +26.33	0.430 ; - 75.31
7	0.708 ; -113.22	4.892 ; + 66.26	0.068 ; +18.60	0.413 ; - 84.85
8	0.674 ; -127.54	4.754 ; + 53.02	0.074 ; +10.86	0.401 ; - 94.21
9	0.628 ; -141.15	4.617 ; + 39.77	0.078 ; + 2.80	0.389 ; -102.27
10	0.605 ; -157.21	4.599 ; + 25.65	0.083 ; - 5.30	0.370 ; -111.19
11	0.549 ; -174.62	4.503 ; + 11.83	0.086 ; -14.51	0.330 ; -121.08
12	0.513 ; +165.35	4.291 ; - 2.24	0.087 ; -23.36	0.283 ; -133.16
13	0.504 ; +145.18	4.193 ; - 15.42	0.087 ; -32.46	0.248 ; -149.27
14	0.504 ; +126.44	4.123 ; - 29.96	0.088 ; -43.35	0.229 ; -165.01
15	0.517 ; +109.11	4.106 ; - 45.03	0.087 ; -54.72	0.225 ; +179.28
16	0.527 ; + 91.65	4.001 ; - 60.55	0.086 ; -66.36	0.224 ; +161.59
17	0.530 ; + 74.05	3.888 ; - 75.22	0.085 ; -79.11	0.208 ; +142.58
18	0.543 ; + 57.36	3.785 ; - 89.66	0.083 ; -93.10	0.212 ; +121.91

Table C.2. PHEMPT "NE584C" scattering parameters

Appendix D

Thermal Noise Derivation

Thermal noise is best explained using Planck's black-body radiation law,

$$v_n = \sqrt{\frac{4hfBR}{\exp^{hf/kT} - 1}}, \quad (\text{D.1})$$

where,

$h = 6.546 \times 10^{-34}$ J-sec is Planck's constant;

$k = 1.380 \times 10^{-23}$ J/°K is Boltzmann's constant;

T is the temperature in degrees kelvin (K);

B is the bandwidth of the system in Hz;

F is the center frequency of the bandwidth in Hz;

R is the resistance, in ohms.

Assume a resistor R at a given temperature T . The electrons in this resistor are in random motion with a kinetic energy proportional to the temperature. These random motions produce small, random voltage fluctuations at the resistor terminals [8]. This voltage, v_n has a zero mean value, but a nonzero root mean square

(*RMS*) value. Usually $hf \ll kT$. Using a Taylor exponential series expansion for the first two terms gives

$$\exp^{hf/kT} - 1 \simeq \frac{hf}{kT}. \quad (\text{D.2})$$

Equation D.1 can then be rewritten as,

$$v_n = \sqrt{4kTBR}. \quad (\text{D.3})$$

Equation D.3 is known as the "Rayleigh-Jeans approximation" and commonly used in microwave engineering [27]. This noise is independent of frequency and has a constant power spectral density. It is often referred as "White Noise". In order to find the noise power P_n in this resistor within a given bandwidth B , a Thévenin equivalent circuit consisting of a noiseless resistor and a random voltage source are connected to a load resistor R_L , via an ideal BPF, to provide maximum noise power transfer to the load:

$$P_n = \left(\frac{v_n}{2R}\right)^2 R \quad (\text{D.4})$$

$$= kTB. \quad (\text{D.5})$$

Thermal noise or "White Noise" is considered to be the lowest noise density measurable. At ambient temperature, the noise power in a one Hertz bandwidth is,

$$P_n \text{ (dBm)} = 10 \log(kT/0.001) \quad (\text{D.6})$$

$$= -173.86. \quad (\text{D.7})$$

Appendix E

PLDRO Prototype Layout List

Figure E.1. 3 GHz reference multiplier layout

Figure E.2. 12 GHz push-push DRO layout

Figure E.3. Loop filter layout

Figure E.4. Wilkinson combiner layout

Figure E.5. 3-dB hybrid layout

Figure E.6. 3 GHz band-pass filter layout

Figure E.7. 12 GHz band-pass filter layout

Figure E.8. Output buffer layout

Appendix F

PLDRO Prototype Picture List

Figure F.1. Test setup at C.R.C.

Figure F.2. 12 GHz push-push PLDRO complete prototype

Figure F.3. 12 GHz push-push DRO: close-up view