Analysis of Phase Noise in Distributed Oscillators

by

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Abstract

This thesis presents a frequency-domain analytical method for predicting the phase noise in distributed oscillators, a new type of oscillator for use in high frequency integrated circuit designs. The method is based on a linear model which is extended to account for nonlinear effects. Analysis of the model yields computational formulae for predicting distributed oscillator phase noise. The correctness and accuracy of derived formulae are verified by simulation in advanced design system (ADS). It is found that the phase noise predictions from the derived formulae are in good agreement with those observed during simulation, which in turn are within acceptable limits. The maximum error between calculated and simulated phase noise figures is about 2.9dB.

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To
my parents
and my husband

Table of Contents

Chapter 1 Introduction	1
1.1 Background	1
1.2 Motivation	2
1.3 Contributions	3
1.4 Thesis Outline	3
 Chapter 2 Oscillator Principles and Configurations	 5
2.1 Introduction	5
2.2 Oscillator Applications	6
2.3 Oscillator Principles	9
2.3.1 Oscillator Classification	9
2.3.2 Oscillation Criterion	10
2.4 Performance Parameters in Designing Oscillators	11
2.5 Oscillator Configurations	15
2.5.1 LC oscillators	15
2.5.2 Ring Oscillators	17
2.5.3 Relaxation Oscillators	19
2.5.4 Distributed Oscillators	20
2.6 Comparison of Different Oscillator Configurations	21

2.7	Summary	23
 Chapter 3 Analysis of Distributed Amplifiers and Oscillators		24
3.1	Introduction.....	24
3.2	Analysis of Distributed Amplifiers	25
3.2.1	Distributed Amplifier Configuration	25
3.2.2	Impedance Matching.....	27
3.2.3	Distributed Amplifier Operation.....	30
3.2.4	Loaded Transmission Line Characteristics	31
3.2.5	Distributed Amplifier Gain	35
3.3	Analysis of Distributed Oscillators.....	40
3.3.1	Distributed Oscillator Configuration	40
3.3.2	Oscillation Condition	40
3.3.3	Biasing	43
3.3.4	Tuning Considerations	43
3.4	An Approach to Distributed Oscillator Design.....	44
3.4.1	Design with Lumped Elements.....	44
3.4.2	Replacement of Lumped Elements with Transmission Lines.....	46
3.5	Summary	47
 Chapter 4 Analysis of Phase Noise in Distributed Oscillators		49
4.1	Introduction.....	49
4.2	Phase Noise Overview	50
4.2.1	Phase Noise Definition	50
4.2.2	Phase Noise Effects in Communication Systems	52
4.2.3	Noise Sources in MOSFET Devices.....	54
4.2.3.1	Thermal Noise.....	54

4.2.3.2	Flicker Noise	56
4.2.3.3	Shot Noise	57
4.3	Phase Noise in Distributed Oscillators	58
4.3.1	The Linear Oscillator Model.....	58
4.3.2	Analysis of Phase Noise in Distributed Oscillators	60
4.3.2.1	Additive Noise	60
4.3.2.2	Mixing Noise	63
4.3.2.3	Power Supply and Substrate Noise	65
4.3.3	Discussion	66
4.4	Summary	68
 Chapter 5 Verification through Simulation		69
5.1	Introduction.....	69
5.2	Transmission Line Modeling	70
5.3	An Example of Designing a Distributed Oscillator	72
5.4	Phase Noise Calculation and Simulation	79
5.4.1	Calculation	79
5.4.2	Simulation	80
5.4.3	Comparison of Calculated and Simulated Phase Noise.....	82
5.5	Summary	83
 Chapter 6 Conclusions		84
6.1	Summary	84
6.2	Future Work	85
 Appendix A Simplification of Eq. (3.26)		87

Appendix B TSMC 0.13μm CMOS Interconnect Stack Simplification.....	89
Appendix C Simulation Setups in Momentum.....	91
Appendix D Parameters for Calculating Phase Noise.....	94
Appendix E HB Simulation Results	96
References.....	99

List of Tables

Table 5.1	Parameters of driving transistor (design with lumped elements)	74
Table 5.2	Parameters of driving transistor (design with transmission lines).....	77
Table 5.3	Parameters for a 10GHz 4-stage distributed oscillator phase noise calculation	80
Table 5.4	Comparison of phase noise for 4-stage distributed oscillators operating at three different frequencies	82
Table 5.5	Comparison of phase noise for 4-stage and 5-stage distributed oscillators operating at the same frequency	82
Table D.1	Parameters for a 14GH 4-stage distributed oscillator phase noise calculation	94
Table D.2	Parameters for a 18GHz 4-stage distributed oscillator phase noise calculation	94
Table D.3	Parameters for a 10GHz 5-stage distributed oscillator phase noise calculation	95

List of Figures

Fig. 2.1	Basic block diagram of PLL	6
Fig. 2.2	Block diagram of a PLL-based clock recovery circuit	7
Fig. 2.3	Clock recovery from random data	7
Fig. 2.4	Block diagram of a PLL-based frequency synthesizer	7
Fig. 2.5	Oscillator classification.....	9
Fig. 2.6	Block diagram of a feedback oscillator	10
Fig. 2.7	Dependence of frequency stability on phase slope	13
Fig. 2.8	LC oscillator basic structures (a) Colpitts oscillator (b) Hartley oscillator (c) Clapp oscillator.....	16
Fig. 2.9	Block diagram of a 3-stage single-ended ring oscillator	17
Fig. 2.10	Schematic of an inverting gain stage	18
Fig. 2.11	Block diagram of a 4-stage differential ring oscillator	18
Fig. 2.12	A single stage of differential ring oscillator	18
Fig. 2.13	Emitter-coupled multivibrator	19
Fig. 2.14	Block diagram of a distributed oscillator.....	20
Fig. 3.1	Basic configuration of a distributed amplifier	26
Fig. 3.2	One gain stage of a distributed amplifier.....	26
Fig. 3.3	An equivalent model for artificial gate line or drain line as a constant- k low-pass filter	27

Fig. 3.4	An m-derived half section.....	29
Fig. 3.5	Distributed amplifier including m-derived half sections	29
Fig. 3.6	Inductors realized by transmission lines in distributed amplifier	30
Fig. 3.7	Lumped-element equivalent circuit for the transmission line	31
Fig. 3.8	Equivalent circuit of one segment of loaded gate line.....	33
Fig. 3.9	Equivalent circuit of one segment of loaded drain line	34
Fig. 3.10	Illustration of signal path containing the n^{th} transistor in a N-stage distributed amplifier	35
Fig. 3.11	Distributed amplifier with compensating capacitors C_{add}	38
Fig. 3.12	Distributed amplifier based oscillator	40
Fig. 3.13	Current source biasing scheme	43
Fig. 3.14	Distributed oscillator with lumped inductors.....	45
Fig. 4.1	Output spectra of (a) ideal, noise-free and (b) practical oscillators.....	51
Fig. 4.2	Illustration of phase noise definition	51
Fig. 4.3	Down conversion in an ideal receiver.....	52
Fig. 4.4	Reciprocal mixing effect in a practical receiver	53
Fig. 4.5	Phase noise effect from transmitter.....	54
Fig. 4.6	Equivalent models for the thermal noise in a MOSFET.....	55
Fig. 4.7	The linear oscillator model	58
Fig. 4.8	Noise shaping in a linear oscillatory system.....	59
Fig. 4.9	Additive noise originating in the signal propagation path.....	60
Fig. 4.10	Noise component transferring due to intermodulation effects.....	65
Fig. 5.1	A simplified interconnect cross-section of $0.13\mu m$ CMOS technology	71
Fig. 5.2	CPS geometry and dimension.....	71

Fig. 5.3	RLC model of 100 μ m CPS.....	72
Fig. 5.4	Schematic of a 10GHz distributed oscillator with lumped elements.....	73
Fig. 5.5	S-parameter S_{21} for a 10GHz distributed oscillator with lumped elements	75
Fig. 5.6	HB simulation results for a 10GHz distributed oscillator with lumped elements	75
Fig. 5.7	A transistor configuring as a capacitor	77
Fig. 5.8	Schematic of a 10GHz distributed oscillator with CPSs	78
Fig. 5.9	S-parameter S_{21} for a 10GHz distributed oscillator with CPSs.....	78
Fig. 5.10	HB simulation results for a 10GHz 4-stage distributed oscillator with CPSs.....	79
Fig. 5.11	HB simulation test bench.....	81
Fig. 5.12	Phase noise result by HB simulation	81
Fig. B.1	Illustration of interconnect stack simplification	89
Fig. C.1	Substrate layer definition	92
Fig. C.2	Illustration for thick metallization layer mapping	92
Fig. C.3	Port properties for CPS	93
Fig. E.1	HB simulation results for a 14GHz 4-stage distributed oscillator with CPSs	96
Fig. E.2	HB simulation results for a 18GHz 4-stage distributed oscillator with CPSs	97
Fig. E.3	HB simulation results for a 10GHz 5-stage distributed oscillator with CPSs	98

List of Symbols and Abbreviations

Resistor

Inductor

Capacitor

Transmission line

Diode

NMOS transistor

PMOS transistor

Inverter

Current source

Supply voltage V_{dd}

Ground

AC	Alternating Current
ADS	Advanced Design System
BiCOM	Bipolar CMOS
CMOS	Complementary Metal Oxide Semiconductor
CPS	CoPlanar Stripline
DC	Direct Current
EM	ElectroMagnetic
EOS	Electrical Over-Stress
f_c	Transmission Line Cutoff Frequency
FET	Field Effect Transistor
f_T	Transistor Cutoff Frequency
GaAs	Gallium Arsenide
g_m/G_m	Transconductance
HB	Harmonic Balance
HEMT	High Electron Mobility Transistor
IC	Integrated Circuit
IF	Intermediate Frequency
LO	Local Oscillator
LPF	Low-Pass Filter
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PD	Phase Detector
PFD	Phase and Frequency Detector

PLL	Phase-Locked Loop
RF	Radio Frequency
Si	Silicon
SiO ₂	Silicon Dioxide
SSB	Single Side Band
T	Temperature
VCO	Voltage-Controlled Oscillator
W/L	Width/Length of MOSFET Device

1.1 Background

Voltage-controlled oscillators (VCO's) play an essential role in communication systems, especially as components of phase-locked loops (PLLs), clock recovery circuits and frequency synthesizers. Their operating frequencies have had to keep up with the ever-increasing demands of high-frequency and microwave applications, a situation which has led to the development of a new type of oscillator, the distributed oscillator. The concept of the distributed oscillator shares its origin with that of the broadband distributed amplifier. A distributed amplifier achieves a higher gain-bandwidth product by absorbing the parasitic capacitances of transistors into transmission lines and effectively trades larger delay for a better gain-bandwidth product. Correspondingly, a distributed oscillator can operate at frequencies close to transistor's cutoff frequency f_T [WuHa01].

In 1992, Z. Skvor proposed a distributed oscillator based upon a distributed amplifier operating in reverse gain mode [SkSa92]. In 1998, the same group described the experimental realization of a 4GHz device having a 1-3.5GHz tuning range and good

spectral purity. The device consisted of 4 GaAs p-type high electron mobility transistors (HEMTs) connected with microstrip lines [DiSk98]. In 1999, an alternative design based on a distributed amplifier operating in forward gain mode was described by B. Kleveland and his colleagues. An implementation based upon $0.18\ \mu\text{m}$ CMOS technology achieved 16.6GHz operation (but without tuning ability), and exhibited a measured phase noise of -110dBc/Hz at 1 MHz offset [KiDi99][KiDi01]. In 2001, H. Wu and A. Hajimiri implemented a 10GHz CMOS distributed oscillator with a tuning range of 12% and phase noise of -103dBc/Hz at 600 kHz offset, and also a 12GHz bipolar oscillator with a tuning range of 26% and phase noise of -99dBc/Hz at 600kHz offset. Both distributed oscillators were designed by using the distributed amplifier in forward gain mode and fabricated in a $0.35\ \mu\text{m}$ BiCOMS process [WuHa01].

1.2 Motivation

The work mentioned above forms a limited survey of some of those aspects of distributed oscillators which are of practical interest, namely their tuning capability, operating frequencies, and technology choices. However, the quoted distributed oscillator phase noise figures are based only on measurement results. It would seem that no theoretical work has been done on this important topic and it is the purpose of this thesis to remedy this situation. The availability of closed-form formulae that accurately predict the phase noise of distributed oscillators would not only be welcomed by engineers working in the field, but its development would improve our understanding of the operation of these devices. The present work is intended to be a step toward the realization of these goals. The work in this thesis adopts the topology of distributed oscillators based on a distributed amplifier in forward gain mode, which is as same as that of [KiDi99][KiDi01][WuHa01].

1.3 Contributions

The contributions of this thesis work can be summarized as follows:

A frequency-domain analytical method was employed for the purpose of predicting phase noise in distributed oscillators. The method is founded upon a linear model, which is then extended to take important nonlinear effects into consideration. The analysis yielded closed-form formulae to be used for predicting distributed oscillator phase noise. Formulae are directly related to actual design parameters and therefore offer not only a practical design tool but also a clearer physical understanding of the relation between design choices and oscillator quality.

The correctness and accuracy of the theoretical phase noise predictions were verified by using harmonic balance (HB) simulation in advanced design system (ADS). It is found that the phase noise calculated using the derived formulae is in a good agreement with the phase noise observed in simulation. Both follow the same pattern with acceptable errors.

1.4 Thesis Outline

This thesis has six chapters and is organized in the following manner.

Chapter 2 begins with a review of oscillator applications which mainly focus on introducing the major applications of oscillator in clock recovery circuits and frequency synthesizers. The fundamental principles of oscillator operation are then outlined. Key performance parameters, which are of importance to measure oscillator characteristics, are listed and discussed. The three most commonly used oscillator configurations, namely LC,

ring, relaxation oscillators, and one novel configuration of distributed oscillator are introduced. The features of the four introduced oscillator configurations are compared and summarized.

In chapter 3, the analysis of distributed amplifiers is dealt with first. Once a conceptual background for distributed amplifiers has been established, the analysis of the distributed oscillators is commenced. A practical approach for designing these oscillators is presented.

In chapter 4, phase noise is first defined and then its effects in communication systems are described. Noise sources in MOSFET devices are important contributors to oscillator phase noise, and they are studied as well. Further attention is confined to the analysis of phase noise in distributed oscillators. A frequency-domain analysis method is employed for predicting the phase noise in distributed oscillators and the principle issues related to its occurrence in these oscillators are discussed - the result of this analysis is a set of closed-form formulae to be used in predicting phase noise performance.

In chapter 5, transmission line modeling as an important part of distributed oscillator design is described. A 10GHz distributed oscillator is used as an example to show the procedure which takes one from circuit design to phase noise calculation and simulation. The main objective is to validate by simulation the accuracy of phase noise predictions using the closed-form formulae of chapter 4. Five oscillators are examined and their calculated and simulated phase noise figures are compared.

Chapter 6 as the conclusion part, it summarizes the work involved in this thesis. Suggestions for future work are made.

Oscillator Principles and Configurations

2.1 Introduction

The oscillator is an integral part of many electronic systems. A wide-ranging knowledge of oscillator applications, their operating principles and an appreciation of the factors affecting their performances, in addition to available configurations, is a necessary prerequisite to the successful circuit designs. The next section (2.2) contains a by no means inclusive survey of applications in which oscillators play important roles. General principles of oscillators are reviewed in section 2.3 and important performance parameters and their influences upon circuit design in section 2.4. Section 2.5 introduces some specific oscillator configurations - in particular, LC oscillators, ring oscillators, relaxation oscillators and distributed oscillators. A comparison of the performance characteristics of the various oscillators, based on a review of available publications, is assembled in section 2.6.

2.2 Oscillator Applications

The oscillator has a wealth of applications. Just three are the generation of system timing clock signals, the generation of carrier signal to be modulated in amplitude or frequency to transmit information, and the production of the periodic sweep signals used in converting analog voltage or current data into frequency or used in display systems. In addition, a fourth, of great interest to the communication engineers, is their uses in complex signal-processing systems such as PLLs [Gre84]. Therefore, it is appropriate to concentrate on an examination of this particular utilization so that the influences of oscillator characteristics may be more clearly appreciated.

Fig. 2.1 Basic block diagram of PLL

PLLs are analog building blocks used extensively in many analog and digital systems. Basic structure of a PLL is shown in Fig. 2.1. There are three principal components, a phase detector (PD), a low-pass filter (LPF) and a voltage-controlled oscillator arranged in a negative feedback configuration, the most important of which is the VCO. With reference to the block diagram of Fig. 2.1, the principle of operation of a PLL may be described as follows: the PD generates an output voltage with an average value proportional to phase difference between the input signal and the output of the VCO. The output voltage of PD is filtered by the LPF to suppress high-frequency components and then is applied to the VCO to control VCO's oscillation frequency. The feedback is negative in the sense that the loop reacts to reduce any change in the PD output. This results in the output of VCO

being synchronized with the input signal. When this happens, the PLL is said to be locked to the input signal frequency.

A brief look at two major applications of PLLs, namely clock recovery and frequency synthesis, is as follows.

Fig. 2.2 Block diagram of a PLL-based clock recovery circuit

Fig. 2.3 Clock recovery from random data

Fig. 2.4 Block diagram of a PLL-based frequency synthesizer

Fig. 2.2 shows a block diagram of clock recovery circuit which is made by a basic block diagram of a PLL through feeding PD with data. The basic function of clock recovery circuit is to produce a timing clock signal from a stream of binary data. In many systems, data is transmitted and retrieved asynchronously, that is without any explicit timing signal accompanying the data. For example, in optical communications, a stream of data propagates through a fiber with no accompanying clock. In order to process data synchronously at receiver end, the timing information (clock) must be recovered from the data. Fig. 2.3 illustrates the recovered clock signal from a data stream by the system of Fig 2.2 [Raz961].

The block diagram of a PLL operating as a frequency synthesizer is shown in Fig. 2.4. It is seen that by introducing a programmable frequency divider into the feedback loop of PLL, between the VCO output and the phase and frequency detector (PFD) input, PLL can be made into a basic frequency synthesizer. N is division ratio of the frequency divider. The actual signal frequency provided by the loop into the PFD is $1/N$ times the VCO frequency. When PLL is locked on an external reference frequency (usually a crystal oscillator is used as the reference frequency source), the two inputs of the PFD are at the same frequency, it means $f_{ref} = f_{out}/N$. In other words, the frequency of VCO output is obtained with the value of $f_{out} = Nf_{ref}$. By varying the frequency divider ratio, N , a frequency synthesizer can derive a large number of discrete frequencies. Such frequency synthesizers find many applications. For example, in radio frequency (RF) transceivers, this architecture is commonly used to generate the local oscillator (LO) at a programmable frequency that tunes the transceiver to the desired channel by adjusting the value of N .

In applications of phase-locked systems, whether in a clock recovery circuit or in a frequency synthesizer, if the input signal or the building blocks of a PLL exhibit noise, then the output signal will be contaminated by noise. In general, all the loop components may contribute noise. It is found that the phase noise of VCO is typically much more significant than that of other loop components. Therefore, VCO's performance plays an essential role in determining the quality of PLL's output. Because of this situation, phase noise has long been the subject of theoretical and experimental investigation.

2.3 Oscillator Principles

2.3.1 Oscillator Classification

Fig. 2.5 Oscillator classification

An oscillator is a circuit that is able to generate a periodic output signal without using a periodic input source and in this sense it may be thought of as a DC-to-AC converter. Oscillators come in a variety of different types. Categorically, they can be classified into tuned and untuned oscillators. Tuned oscillators, such as crystal, RC, LC, and distributed types, generate output signals which are nearly sinusoidal. And they are usually real-

ized by using some kind of frequency-selective or tuned circuit in a feedback configuration. It needs to be mentioned that the distributed oscillator, as a new type of oscillator, has just emerged for the integrated circuit design in recent years and as yet there are no published books available to address its characteristics. The reason that it is classified as a tuned type here is because of its sinusoidal-like output waveform. On the other hand, untuned devices such as relaxation and ring oscillators generally produce triangle wave and square wave outputs. They operate by alternately charging and discharging an energy storage element (normally a capacitor), and rely on the threshold switching characteristics of the circuit rather than on a frequency-selective element to determine the oscillator waveform. Fig. 2.5 shows a classification diagram of oscillators [AlHo87][JoMa97].

2.3.2 Oscillation Criterion

Fig. 2.6 Block diagram of a feedback oscillator

The task of the oscillator is to generate a periodic waveform having a specified frequency and a constant amplitude, both of which satisfy designated tolerances. The principles of operation of an oscillator circuit can be explained in terms of a feedback system as shown in Fig. 2.6. This diagram consists of an amplifier, a feedback network, and a summing junction. See Fig. 2.6, $X_i(j\omega)$, $Y_o(j\omega)$, and $X_f(j\omega)$ are the input, output and feedback signals, $A(j\omega)$ and $\beta(j\omega)$ are the amplifier and feedback network transfer functions. For an actual oscillator, there is no input signal $X_i(j\omega)$, but one has been included in the

theoretical model of the diagram as an aid to understand the principles of operation, and especially the introduction of noise. The closed-loop transfer function of the circuit of Fig. 2.6 is found as

$$\frac{Y_o(j\omega)}{X_i(j\omega)} = \frac{A(j\omega)}{1 - A(j\omega)\beta(j\omega)} \quad (2.1)$$

If at a specific frequency ω_0 , the loop gain $A(j\omega_0)\beta(j\omega_0)$ is unity, the circuit has a corresponding closed-loop gain of infinity. That is, at this frequency the circuit will have a finite output for zero input signal, which is by definition an oscillator. For steady oscillation at frequency ω_0 , the following two conditions must exist simultaneously:

- (1) The magnitude of the open-loop transfer function, $|A(j\omega_0)\beta(j\omega_0)|$, must be equal to unity.
- (2) The phase shift of the entire loop, $\angle A(j\omega_0)\beta(j\omega_0)$, must be equal to 2π if a positive feedback is considered (or π if a negative feedback is considered).

The above two conditions described in terms of magnitude and phase separately are called Barkhausen criterion [SeSm82]. It is noted that the above oscillation criterion is satisfied at a unique frequency ω_0 , otherwise locking to multiple harmonic frequencies is possible.

2.4 Performance Parameters in Designing Oscillators

When an oscillator is designed, there are some specifications of primary importance to the oscillator designer [Raz01].

a. Operating Frequency

The operating frequency is determined by the target application.

b. Tuning Range and VCO Gain K_{vco}

Tuning range is the range of output frequencies that the VCO oscillates at over the full range of the control voltage. A VCO must have a tuning range sufficient to overcome process and temperature-induced frequency perturbations, and it also needs to meet the frequency-range specifications of the design.

The VCO gain, K_{vco} , is also a very important parameter in VCO designs. In order to achieve the best noise performance, K_{vco} must be minimized. On the other hand, the requirement of $K_{vco} \geq (\omega_2 - \omega_1)/(V_2 - V_1)$ needs to be satisfied, thus ensuring enough tuning range. V_1 , V_2 are the minimum and maximum control voltages and $\omega_2 - \omega_1$ is the tuning range.

c. Output Signal Purity

The degree of purity required of an oscillator's output is application-dependent, but it is especially significant in digital and analog communication systems. Ideally, the spectrum of an oscillator's output is a single impulse at the operating frequency. But practically, it is a central impulse at ω_0 surrounded by noise skirts. To compare one circuit's noise behavior to that of another, it is necessary to quantify the noise somehow. In the time domain, the parameter used to quantify signal purity is called jitter, and in the frequency domain, phase noise. Usually, the quality factor Q is related to the oscillator's phase noise performance and there are several common definitions of Q .

For a resonator-based oscillator, Q is generally defined as 2π times the ratio of the stored energy and the dissipated energy per cycle.

$$Q = 2\pi \cdot \frac{\text{Energy stored}}{\text{Energy dissipated per cycle}} \quad (2.2)$$

Q can be also defined as the ratio of the center frequency and the two-sided -3dB bandwidth B . This definition shows the frequency selectivity.

$$Q = \frac{\omega_0}{B} \quad (2.3)$$

Frequency stability can be characterized by the third definition of Q as given below

$$Q = \frac{\omega_0}{2} \cdot \frac{d\phi}{d\omega} \quad (2.4)$$

Fig. 2.7 Dependence of frequency stability on phase slope

It is noted that, for a steady oscillation, the loop will oscillate at the frequency for which the total phase shift around loop must be zero or 2π . When there is a phase change due to a variation in one of the circuit components, if $d\phi/d\omega$ is large, the resulting change in frequency will be small, as shown in Fig. 2.7. In other words, Q is a measure of

the ability of closed-loop system to oppose variations in the frequency of oscillation [SeSm82].

A linear model that is typically used for phase noise is Leeson's model [Lee66]. According to this model, the output noise power spectral density $S_\phi(\Delta\omega)$ of the oscillator is defined as

when $\Delta\omega < B/2$

$$S_\phi(\Delta\omega) = \left(\frac{\omega_0}{2Q\Delta\omega} \right)^2 \cdot S_{\Delta\theta} \quad (2.5)$$

when $\Delta\omega > B/2$

$$S_\phi(\Delta\omega) = S_{\Delta\theta} \quad (2.6)$$

where B is two-sided -3dB bandwidth. $\Delta\omega$ is the offset frequency from carrier. And $S_{\Delta\theta}$ is input noise power spectral density.

Based on the Eq. (2.5), it can be seen that the following factors have the effects on noise power observed at the output of oscillators: (1) oscillation frequency; (2) quality factor; (3) input noise resulting from both internal and external noise sources. The internal sources are thermal noise, flicker noise and shot noise. External noise originates from the power supply and substrate.

d. Output Amplitude

A large oscillation amplitude makes the output less sensitive to the noise, and it is expected that this can be achieved. There are however trade-offs amongst output amplitude, power consumption and even tuning range, that must be considered.

e. Power Consumption

It goes without saying that oscillators should be designed with minimal power consumption in mind. Energy use has a direct effect upon cost, chiefly in terms of battery life.

f. Monolithic Integration and Fabrication Cost

The performance of a circuit should be the primary concern in the engineer's mind, but not the only concern. The monolithic integration and fabrication cost of the circuit are also important.

It is impossible for an engineer to meet all specifications while designing an oscillator. Compromises are needed according to the different applications.

2.5 Oscillator Configurations

Four oscillator configurations are selected for closer scrutiny, namely LC oscillators, ring oscillators, relaxation oscillators and distributed oscillators. The first three of these are well-known and have been used widely in communication, data transmission and synchronous systems. The distributed oscillator has been proposed in recent years as a promising alternative in high-frequency and microwave applications.

2.5.1 LC oscillators

In the past few years, the monolithic inductor has gradually come to be used for the implementation of passive resonant circuits in CMOS technology. An LC oscillator may be realized by using a single transistor and a parallel LC tank. The operating frequency is given by

$$f_{osc} = \frac{1}{2\pi\sqrt{LC}} \quad (2.7)$$

This frequency can be varied by adjusting the inductor and capacitor values. But in the case of a monolithic oscillator, one does not have a choice and must tune the oscillator by varying the capacitance of a varactor. A varactor, or voltage-controlled capacitor, is a reverse-biased diode whose capacitance can be modified by changing the magnitude of the reverse bias.

Fig. 2.8 LC oscillator basic structures (a) Colpitts oscillator (b) Hartley oscillator (c) Clapp oscillator

Three representative LC oscillators are shown in Fig. 2.8 (a), (b), and (c) [Raz01]. The Colpitts oscillator shown in Fig. 2.8 (a) is the most commonly used of these because of a combination of good phase noise characteristics and the fact that the tapped capacitor structure lends itself easily to IC implementation. The Hartley oscillator of Fig. 2.8 (b) is complementary to the Colpitts oscillator, having inductors and capacitors swapped. The Clapp oscillator shown in Fig. 2.8 (c) is seen to be a modification of the Colpitts circuit, with a capacitor placed in series with the inductor.

2.5.2 Ring Oscillators

Fig. 2.9 Block diagram of a 3-stage single-ended ring oscillator

The simplest ring oscillator is made up of an odd number of inverting gain stages arranged with a total phase shift of 180° in a negative feedback loop as shown in Fig. 2.9. A minimum of three stages should be used to ensure reliable oscillation. The CMOS inverter given in Fig. 2.10 is a simple way of implementing an inverting gain stage. The oscillation frequency is easily deduced.

$$f_{osc} = \frac{1}{2NT} \quad (2.8)$$

where N is the number of inverting gain stages and T the delay time of a single inverting gain stage.

Fig. 2.10 Schematic of an inverting gain stage

Fig. 2.11 Block diagram of a 4-stage differential ring oscillator

Fig. 2.12 A single stage of differential ring oscillator

Voltage control of the ring oscillator's frequency can be done by making the time delay of its inverting gain stages voltage-controlled.

In fact, the inverting stage shown in Fig. 2.10 is not usually employed in CMOS designs since any noise in the power-supply voltage will cause the oscillation frequency to have jitter. This poor power-supply rejection is perhaps the major source of jitter in integrated oscillators. Therefore, it is extremely important that the frequency of oscillation is independent of the power-supply voltage if low jitter is required [JoMa97].

Instead, a differential implementation is chosen to obtain better power-supply rejection. Fig. 2.11 shows the block diagram of a 4-stage differential ring oscillator. It is noted that the outputs of the last stage are interchanged before feeding them back to the input to achieve the inversion required in the loop. An even number of stages can be used in this configuration, the advantage of which is that the outputs of the middle inverter will give a quadrature output as compared with the last inverter. A simple gain stage is diagrammed in Fig. 2.12 [Raz01].

2.5.3 Relaxation Oscillators

Fig. 2.13 Emitter-coupled multivibrator

Relaxation oscillators, also called multivibrators or charge-discharge oscillators, are the most commonly used oscillators in monolithic IC design. They operate by alternately charging and discharging an energy storage element (usually a capacitor) between two internally set threshold voltage levels within the circuit. The output frequency of such an oscillator is inversely proportional to the value of the timing capacitor.

Based on their circuit configurations, relaxation oscillators can be classified into three categories: RC relaxation oscillators which use resistive charge and discharge paths for the timing capacitor, constant-current charge and discharge oscillators which use current sources to charge and discharge the timing capacitor, and emitter-coupled multivibrators which use symmetrical charge and discharge paths for a timing capacitor connected across the emitters of a differential gain stage. The most popular relaxation oscillator is the emitter-coupled multivibrator, as shown in Fig. 2.13 [AbMe83][Gre84], which is a subclass of the constant-current charge and discharge oscillators. In many monolithic designs, they are preferred over constant-current type because of the inherent symmetry of their output waveforms and a higher frequency capability.

2.5.4 Distributed Oscillators

Fig. 2.14 Block diagram of a distributed oscillator

A novel oscillator structure, which has just been proposed in recent years, is the distributed oscillator. The direct ancestor of this device, which is suitable for very high frequency and microwave applications, is the distributed amplifier.

Fig. 2.14 shows the block diagram of a distributed oscillator which is made by adding an input-output feedback loop to a distributed amplifier. A more detailed discussion of distributed amplifiers and oscillators appears in chapter 3 of this thesis.

2.6 Comparison of Different Oscillator Configurations

In the previous section 2.5, four oscillator configurations, namely, LC, ring, relaxation, and distributed types, were presented. Each of these oscillators has advantages and disadvantages related to electrical performance and complexity.

LC oscillators are commonly used in CMOS integrated circuit design because they have excellent inherent phase noise or jitter properties due to the frequency-selective nature of LC tank circuitry [Gre84]. They have found a wide range of applications in communication, data transmission, and synchronous logic systems. In order to operate at higher frequencies, the product of the values of tank components L and C must be decreased. However, the inductor loss, parasitic capacitances of transistors, and loading from the next stage do not scale at the same rate. This results in the choice of even smaller inductance values and a correspondingly larger power dissipation for a given oscillation amplitude, and more stringent constraints on the tuning capability [WuHa01]. The additional drawback of LC oscillators is that the on-chip inductor takes up a large area.

One of the most popular ways of realizing an integrated VCO is to use a ring oscillator. Since ring oscillators have the advantages of ease of integration, low cost and providing multi-phase output signals easily, they are becoming widely adopted in PLLs used in the applications of RF or microprocessors to provide clock, data recovery, synchronization, and frequency synthesis [AlPa01]. But they suffer from poor phase noise performance.

Another alternative is the relaxation oscillators. In contrast to LC oscillators, they require only one energy storage element, and they rely on the nonlinear characteristics of the circuit rather than on a frequency-selective component to define an oscillatory waveform [Gre84]. Usually the operating frequency is inversely proportional to the capacitor value and directly proportional to a current or voltage level, so that the frequency is easily controlled by a single external component. The relaxation oscillators can also be made to generate quadrature outputs with little difficulty - this feature is a great advantage in PLL applications. And these circuits have recently become common because they are easy to fabricate as monolithic integrated circuits. Nevertheless, this type of oscillator is rarely used in high-performance transceivers because of the inadequate spectral purity of its output signals [Lee98].

As for the distributed oscillators, due to originating from broadband distributed amplifiers, the big advantage is its ability to operate at frequencies close to the transistor cutoff frequency. Since the transmission lines are incorporated into the circuits, distributed oscillators are easy to be integrated in monolithic technology. Furthermore, although most of commercially available VCOs are tunable over one octave frequency range, it has been

theoretically proved that those based on distributed amplifiers can be tuned over a decade of bandwidth [SkSa92].

2.7 Summary

This chapter has provided a review of oscillators. The major applications of oscillators in modern communication systems, the operation principles of oscillators, performance parameters and a variety of oscillator configurations have been described. The new concept of the distributed oscillator has been introduced. A literature review based on comparison of the features and limitations of four oscillators summarized the advantages and disadvantages of each, regarding electrical performance and complexity. There is no one 'best' oscillator. It depends on the application whether a particular type is the most suitable.

Analysis of Distributed Amplifiers and Oscillators

3.1 Introduction

The distributed amplifier was first proposed in 1948 in a paper by Ginzton et al. [GiHe48], but the underlying concepts can be traced back to a patent of Percival in 1937 [Per37]. The concept of the distributed amplification is therefore well over a half century old.

Distributed amplifiers have an advantage of wide-band amplification over their conventional counterparts that are especially important in modern high-frequency communication systems. Attempts to attain increased gain of conventional amplifiers by increasing FET transconductance usually lead to increased input capacitance. This difficulty is nonexistent in the case of distributed amplifiers since distributed amplifiers employ a topology in which the gain stages are connected such that their capacitances are separated, yet the output currents still combine in an additive fashion. Series inductive elements are used to separate capacitances at the inputs and outputs of adjacent gain stages, thus offering a means of combining the transconductance of several FET's without combining their

input capacitances. The distributed nature of amplifier capacitances leads to a desirably wide bandwidth [BaGu00].

An oscillator based upon the distributed amplifier may be achieved by making an input-output feedback connection. Such an oscillator will display many of the attributes of the corresponding amplifier. A very important one of these, in the light of the constant need for ever-higher frequencies, is a capability of operation near to the transistor cutoff frequency f_T .

The goal of this chapter is to develop an intuitive understanding of the underlying principles and describe the important issues affecting distributed amplifiers and oscillators, and thus to establish the background necessary to the study of more advanced topics in the next chapter. This chapter starts off with section 3.2 on the analysis of distributed amplifiers. Then section 3.3 presents the analysis of distributed oscillators derived from distributed amplifiers. In section 3.4, a practical design approach relevant to this oscillator is considered.

3.2 Analysis of Distributed Amplifiers

3.2.1 Distributed Amplifier Configuration

The basic configuration of a distributed amplifier is depicted in Fig. 3.1. In this approach, the input and output capacitances of transistors are combined with lumped inductances L_g and L_d to form two artificial transmission lines. The input artificial transmission line connecting to the transistor gate terminals is referred to as the gate line, and the output artificial transmission line connecting to the transistor drain terminals is referred to as the drain line. Both gate and drain lines are terminated by matching imped-

ances having values equal to the line characteristic impedances, Z_g and Z_d . Gate and drain lines are coupled by the transistor transconductances. Node 1 and node 2 are the input and output terminals of amplifier.

Fig. 3.1 Basic configuration of a distributed amplifier

One gain stage of a distributed amplifier shown in Fig. 3.2 consists of one transistor and inductors with values of $L_g/2$ and $L_d/2$ connected in series at transistor's gate and drain terminals.

Fig. 3.2 One gain stage of a distributed amplifier

3.2.2 Impedance Matching

Fig. 3.3 An equivalent model for artificial gate line or drain line as a constant- k low-pass filter

In the basic distributed amplifier configuration of Fig. 3.1, all ports should be image impedance matched to the artificial transmission lines to eliminate reflection. An m -derived half section will be developed for this purpose. To this end, one starts by assuming that both gate and drain lines are as a constant- k low-pass filter as shown in Fig. 3.3. When both ends are matched at their image impedance Z_i , the impedance looking into the artificial transmission lines is given by [Poz90]

$$Z_{line} = \sqrt{\frac{L_{lump}}{C_{fet}}} \sqrt{1 - \frac{\omega^2 L_{lump} C_{fet}}{4}} \quad (3.1)$$

where L_{lump} represents the lumped inductance L_g or L_d , and C_{fet} represents the input or output capacitance of the driving transistor.

Eq. (3.1) suggests the definition of an artificial transmission line's cutoff frequency ω_c at which no signal travels along the transmission line.

$$\omega_c = \frac{2}{\sqrt{L_{lump} C_{fet}}} \quad (3.2)$$

or

$$f_c = \frac{1}{\pi \sqrt{L_{lump} C_{fet}}} \quad (3.3)$$

And a nominal characteristic impedance, R_0 , is expressed as

$$R_0 = \sqrt{\frac{L_{lump}}{C_{fet}}} = k \quad (3.4)$$

where k is a constant.

In terms of these definitions, Eq. (3.1) can be written as

$$Z_{line} = R_0 \sqrt{1 - \frac{\omega^2}{\omega_c^2}} \quad (3.5)$$

Eq. (3.5) indicates that artificial transmission line impedance Z_{line} is a function of the frequency, but the dependence is very weak for $\omega \ll \omega_c$ and approximately equal to the constant R_0 , and exhibits a strong deviation from R_0 as $\omega \rightarrow \omega_c$. Therefore, it is impractical to realize a direct and wide band image impedance matching from transmission lines to a given source or resistive load. Thus, the m-derived half section of Fig. 3.4 [Poz90] is adopted to be inserted between lines and input port, output port and resistive matching load.

Such a half section can greatly improve the impedance match, while allowing simple resistive terminations to be used. The component values in Fig. 3.4 are related to the artificial transmission line inductances and capacitances by

$$L_{m1} = \frac{m L_{lump}}{2} \quad (3.6)$$

$$L_{m2} = \frac{(1 - m^2)L_{lump}}{2m} \quad (3.7)$$

$$C_m = \frac{mC_{fet}}{2} \quad (3.8)$$

It is found that a value of $m = 0.6$ yields optimal matching. The resulting modified circuit is given in Fig. 3.5 [PrBe88].

Fig. 3.4 An m-derived half section

Fig. 3.5 Distributed amplifier including m-derived half sections

It is essential to have matching networks for designing broadband distributed amplifiers. However, operating frequencies of distributed oscillators involved in this work are much less than transmission line's cutoff frequency f_c , so in the following analysis of distributed amplifiers and oscillators, the matching network is not used and transmission line impedance will be assumed to have a nominal characteristic impedance.

3.2.3 Distributed Amplifier Operation

Fig. 3.6 Inductors realized by transmission lines in distributed amplifier

In practice, the inductors, which have appeared as series-connected lumped elements thus far, are realized by actual transmission lines for easy integration. In Fig. 3.6, the original lumped inductors having values of L_g and L_d have been replaced by the transmission lines having segment lengths of l_g and l_d , so that one has $L_g = \bar{L}_g \cdot l_g$ and $L_d = \bar{L}_d \cdot l_d$. The quantities $\bar{L}_g$ and $\bar{L}_d$ denote the inductances of gate line and drain line per unit length (see section 3.2.4).

An input signal V_{in} applied at node 1 of Fig. 3.6 will propagate along the gate line to the matched load Z_g , where it will be absorbed. As this signal travels down the gate

line, it excites each transistor and gives rise a drain current approximately equal to $g_m V_{in}$. Because the impedances seen by the transistor drain on either side of the drain line are equal, the drain current of each transistor will divide into two equal parts. One-half of the drain current flows right to the output load Z_L , and the other flows left to the matched load Z_d . If the phase velocities on the gate and drain lines are identical, all drain current contributions from the stages arrive in phase at the output load Z_L and the maximum voltage is developed. However, partial or complete cancellation of the contributions at the drain termination on the left occurs because the currents flowing in this direction are not in phase. Such cancellation leads to the situation of the current flowing to Z_d being less than that appearing across the output load. Such net current as remains can be absorbed by the matched load.

3.2.4 Loaded Transmission Line Characteristics

Since the transmission line is a component of fundamental importance in distributed amplifiers, further and more-detailed study of their characteristics important to that application is warranted. The propagation constant and characteristic impedance are two important parameters to describe transmission line characteristics.

Fig. 3.7 Lumped-element equivalent circuit for the transmission line

Since transmission line length is a considerable fraction of a wavelength, or many wavelengths, it must be treated as a distributed-parameter network, where voltages and currents can vary in magnitude and phase over its length. The short piece of length Δl of transmission line can be modeled as a lumped element circuit as shown in Fig. 3.7 [Poz90] where $\bar{L}$ and $\bar{R}$ are the series inductance and resistance per unit length of the line. Likewise, $\bar{C}$ and $\bar{G}$ give the shunt capacitance and conductance per unit length.

The complex propagation constant of a transmission line, γ , is defined by

$$\gamma = \alpha + j\beta = \sqrt{(j\omega\bar{L} + \bar{R})(j\omega\bar{C} + \bar{G})} \quad (3.9)$$

where α , β represent the attenuation and phase constants of the transmission line.

The characteristic impedance of the modeled line is defined as

$$Z_0 = \sqrt{\frac{j\omega\bar{L} + \bar{R}}{j\omega\bar{C} + \bar{G}}} \quad (3.10)$$

The γ and Z_0 above have been defined for a general transmission line, one which exhibits loss effects such as dissipation caused by line resistivity. But in most practical cases, such loss is small, resulting in a simplification for above results. So when $\bar{R} \approx 0$ and $\bar{G}$ is very small, the expression for γ may be approximated as [Lad89]

$$\gamma = \alpha + j\beta \approx \frac{\bar{G}}{2} \sqrt{\frac{\bar{L}}{\bar{C}}} + j\omega\sqrt{\bar{L}\bar{C}} \quad (3.11)$$

And so

$$\alpha \approx \frac{\bar{G}}{2} \sqrt{\frac{\bar{L}}{\bar{C}}} \quad (3.12)$$

$$\beta \approx \omega \sqrt{\bar{L}\bar{C}} \quad (3.13)$$

For low loss, the characteristic impedance Z_0 reduces approximately to

$$Z_0 \approx \sqrt{\frac{\bar{L}}{\bar{C}}} \quad (3.14)$$

In a distributed amplifier, the gate and drain lines are loaded at intervals by the gates and drains of the transistors. The expressions for γ and Z_0 will now have to be modified to reflect this. Before starting, a model for a loaded gate line must be defined. The one that will be used is that of Fig. 3.8 [Lad89].

Fig. 3.8 Equivalent circuit of one segment of loaded gate line

C_{in} is the FET input capacitance and R_{in} its input resistance. Taking advantage of Eqs. (3.12) and (3.13) will require that the series connection of C_{in} and R_{in} be transformed to an equivalent parallel connection with respect to any angular frequency ω .

The admittance of the series connection of C_{in} and R_{in} is given approximately by

$$Y \approx \omega^2 C_{in}^2 R_{in} + j\omega C_{in} \quad (3.15)$$

Using the results of Eqs. (3.12), (3.13) and (3.14), the modifications necessitated by loading result in attenuation constant α_g , phase constant β_g and characteristic impedance Z_g for the gate line.

$$\alpha_g \approx \frac{\omega^2 C_{in}^2 R_{in}}{2l_g} \sqrt{\frac{\bar{L}_g}{\bar{C}_g + C_{in}/l_g}} \quad (3.16)$$

$$\beta_g \approx \omega \sqrt{\bar{L}_g (\bar{C}_g + C_{in}/l_g)} \quad (3.17)$$

$$Z_g \approx \sqrt{\frac{\bar{L}_g}{\bar{C}_g + C_{in}/l_g}} \quad (3.18)$$

where $\bar{L}_g$, $\bar{C}_g$ are the series inductance and parallel capacitance of gate line per unit length.

Fig. 3.9 Equivalent circuit of one segment of loaded drain line

Turning to the drain line, one segment of which is shown in Fig. 3.9 [Lad89]. Using Eqs. (3.12), (3.13) and (3.14) again, α_d , β_d , Z_d are obtained as

$$\alpha_d \approx \frac{1}{2R_{ds}l_d} \sqrt{\frac{\bar{L}_d}{\bar{C}_d + C_{out}/l_d}} \quad (3.19)$$

$$\beta_d \approx \omega \sqrt{\bar{L}_d(\bar{C}_d + C_{out}/l_d)} \quad (3.20)$$

$$Z_d \approx \sqrt{\frac{\bar{L}_d}{\bar{C}_d + C_{out}/l_d}} \quad (3.21)$$

where $\bar{L}_d$, $\bar{C}_d$ are the series inductance and parallel capacitance of drain line per unit length. C_{out} , R_{ds} are the output capacitance and resistance of the driving transistor.

3.2.5 Distributed Amplifier Gain

Fig. 3.10 Illustration of signal path containing the n^{th} transistor in a N -stage distributed amplifier

In Fig. 3.10, consider the signal path from input node 1 to output node 2 (dashed line) which contains the n^{th} transistor of a N -stage distributed amplifier. One can write the gate input of this transistor as

$$V_{in,n} = V_{in} e^{-\gamma_g \left(n - \frac{1}{2}\right) l_g} \quad (3.22)$$

where $\gamma_g = \alpha_g + j\beta_g$ is the complex propagation constant of the loaded gate line.

When $V_{in,n}$ excites the gate of the n^{th} transistor, it gives rise to a drain current i_n of approximately $g_m V_{in,n}$. i_n can be written as

$$i_n = -g_m \cdot V_{in,n} = -g_m \cdot V_{in} \cdot e^{-\gamma_g \left(n - \frac{1}{2}\right) l_g} \quad (3.23)$$

where g_m is the transistor small-signal transconductance.

A current i_n then flows into the drain line with one half going in each direction as shown in Fig. 3.10. The two flows are equal because the impedances seen by the transistor drain on either side are equal to the loaded drain line characteristic impedance Z_d . The component of $i_n/2$ going to the left is dissipated by the matching impedance Z_d , and that going to the right reaches the output (node 2), that is

$$i_{out,n} = \frac{1}{2} i_n \cdot e^{-\gamma_d \left(N - n + \frac{1}{2}\right) l_d} \quad (3.24)$$

where $\gamma_d = \alpha_d + j\beta_d$ is the complex propagation constant of the loaded drain line.

The voltage applied to the external load $Z_L = Z_d$ is

$$\begin{aligned} V_{out,n} &= i_{out,n} \cdot Z_L = i_{out,n} \cdot Z_d \\ &= -g_m \cdot \frac{Z_d}{2} \cdot V_{in} \cdot e^{-\gamma_g \left(n - \frac{1}{2}\right) l_g} \cdot e^{-\gamma_d \left(N - n + \frac{1}{2}\right) l_d} \end{aligned} \quad (3.25)$$

The total output voltage of the N -stage distributed amplifier is the superposition

$$\begin{aligned}
 V_{out} &= \sum_{n=1}^N V_{out,n} \\
 &= \sum_{n=1}^N -g_m \cdot \frac{Z_d}{2} \cdot V_{in} \cdot e^{-\gamma_g \left(n - \frac{1}{2}\right) l_g} \cdot e^{-\gamma_d \left(N - n + \frac{1}{2}\right) l_d} \\
 &= -g_m \cdot \frac{Z_d}{2} \cdot V_{in} \cdot \frac{e^{-\gamma_d N l_d} - e^{-\gamma_g N l_g}}{\gamma_g l_g - \gamma_d l_d}
 \end{aligned} \tag{3.26}$$

The derivation of Eq. (3.26) is presented in Appendix A.

The voltage gain of the distributed amplifier is defined as

$$A_v = \frac{V_{out}}{V_{in}} \tag{3.27}$$

A_v may be calculated by substituting (3.26) into (3.27)

$$\begin{aligned}
 A_v &= -g_m \cdot \frac{Z_d}{2} \cdot \frac{e^{-\gamma_d N l_d} - e^{-\gamma_g N l_g}}{\gamma_g l_g - \gamma_d l_d} \\
 &= -g_m \cdot \frac{Z_d}{2} \cdot \frac{e^{-(\alpha_d + j\beta_d) N l_d} - e^{-(\alpha_g + j\beta_g) N l_g}}{(\alpha_g + j\beta_g) l_g - (\alpha_d + j\beta_d) l_d}
 \end{aligned} \tag{3.28}$$

If the gain is to be the maximum possible, the phase delay per segment of the loaded gate line must be equal to that of the loaded drain line. That is, one must have $\beta_g l_g = \beta_d l_d = \beta l$. To achieve this requirement, first, the lengths of gate and drain lines are made to be equal to $l_g = l_d = l$. Then, using identical structure for both gate and drain lines can lead to $\bar{L}_g = \bar{L}_d = \bar{L}$ and to $\bar{C}_g = \bar{C}_d = \bar{C}$. Since each transistor's input capacitance C_{in} is greater than its output capacitance C_{out} , an extra capacitor $C_{add} = C_{in} - C_{out}$ is connected at each drain output to compensate for this difference. See Fig. 3.11. By doing these, $\beta_g = \beta_d = \beta$ is satisfied.

Fig. 3.11 Distributed amplifier with compensating capacitors C_{add}

Generally, the characteristic impedance of the loaded gate line Z_g and that of the loaded drain line Z_d are made to be equal to $Z_0 = 50\Omega$. All requirements above lead to further modifications of the expressions for α_g , β_g , Z_g , α_d , β_d , and Z_d

$$\alpha_g \approx \frac{\omega^2 C_{in}^2 R_{in}}{2l} \sqrt{\frac{\bar{L}}{\bar{C} + C_{in}/l}} = \frac{\omega^2 C_{in}^2 R_{in} Z_0}{2l} \quad (3.29)$$

$$\beta_g \approx \omega \sqrt{\bar{L}(\bar{C} + C_{in}/l)} = \omega Z_0(\bar{C} + C_{in}/l) \quad (3.30)$$

$$Z_g = Z_0 \approx \sqrt{\frac{\bar{L}_g}{\bar{C}_g + C_{in}/l_g}} = \sqrt{\frac{\bar{L}}{\bar{C} + C_{in}/l}} \quad (3.31)$$

$$\alpha_d \approx \frac{1}{2R_{ds}l} \sqrt{\frac{\bar{L}}{\bar{C} + (C_{out} + C_{add})/l}} = \frac{Z_0}{2R_{ds}l} \quad (3.32)$$

$$\beta_d \approx \omega \sqrt{\bar{L}(\bar{C} + (C_{out} + C_{add})/l)} = \omega Z_0(\bar{C} + C_{in}/l) \quad (3.33)$$

$$Z_d = Z_0 \approx \sqrt{\frac{\bar{L}_d}{\bar{C}_d + (C_{out} + C_{add})/l_g}} = \sqrt{\frac{\bar{L}}{\bar{C} + C_{in}/l}} \quad (3.34)$$

The distributed amplifier voltage gain Eq. (3.28) can now, to some degree, be simplified as

$$A_v = -g_m \cdot \frac{Z_0}{2} \cdot \frac{e^{-\alpha_d Nl} - e^{-\alpha_g Nl}}{\alpha_g l - \alpha_d l} \cdot e^{-j\beta Nl} \quad (3.35)$$

Intuitively, the gain of a distributed amplifier may be increased by increasing the number of stages. But of course there is a practical limit to the number of stages. An optimum number of stages which maximizes gain can be derived by differentiating Eq. (3.35) with respect to N [BePr84], and making the resultant expression equal to zero.

$$N_{opt} = \frac{\ln \frac{\alpha_d}{\alpha_g}}{\alpha_d l - \alpha_g l} \quad (3.36)$$

Eq. (3.36) indicates that the optimum number of stages is strongly dependent upon the gate and drain line attenuation constants. That there should be an upper limit to the number of stages in a distributed amplifier has an easy intuitive explanation - when the input signal propagates along the gate line, each transistor receives a smaller amount of energy than does the previous one because the signal is attenuated as it traverses the gate line and an analogous process occurs on the drain line. Additional stages not only decrease the excitation of the last device but also increase the overall attenuation on the drain line. Thus, the overall gain of the amplifier begins to decrease with further addition of stages. Therefore, the gain increases with additional stages until the optimum number of stages is reached [BePr84].

3.3 Analysis of Distributed Oscillators

3.3.1 Distributed Oscillator Configuration

A distributed oscillator is constructed by feeding the output connection (node 2) of a distributed amplifier back to its input (node 1) as shown in Fig. 3.12. One visualizes the oscillation period as the sum of the round-loop transmission line delay and one transistor delay - the path is indicated by a dashed line in the figure. The purpose of using coupling capacitor C_{couple} in the feedback path is to allow the gate and drain lines to be biased independently.

Fig. 3.12 Distributed amplifier based oscillator

3.3.2 Oscillation Condition

In a steady state operation, the large signal open-loop gain of the distributed oscillator will be unity. Since there is no frequency-selective element in the feedback path, the expression of open-loop gain of a distributed oscillator will be the same as that of the incorporated distributed amplifier. The small-signal gain expression for a distributed amplifier (see Eq. (3.35)) may be used to deduce the large-signal open-loop gain expres-

sion for distributed oscillator by simply replacing the small-signal transconductance g_m with its large signal counterpart G_m as defined in [ClHe71]. This leads to

$$G_m \cdot \frac{Z_0}{2} \cdot \frac{e^{-\alpha_d Nl} - e^{-\alpha_g Nl}}{\alpha_g l - \alpha_d l} \cdot e^{-j\beta Nl} = -1 \quad (3.37)$$

Eq. (3.37) can be used to determine the phase and magnitude conditions which must be satisfied by the oscillator. The phase condition can be obtained by

$$e^{-j\beta Nl} = -1 \quad (3.38)$$

which implies

$$Nl\beta = \pi \quad (3.39)$$

When $\beta = 2\pi f/v$ is substituted into Eq. (3.39), it is found that oscillation frequency is

$$f_0 = \frac{v}{2Nl} = \frac{1}{2Nl\sqrt{\bar{L}\bar{C}_t}} = \frac{1}{2N\sqrt{LC_t}} \quad (3.40)$$

where $v = 1/\sqrt{\bar{L}\bar{C}_t}$ is the phase velocity in the transmission line, $\bar{L}$ and $\bar{C}_t = \bar{C} + C_{in}/l$ are the inductance and capacitance per unit length of the loaded transmission lines, L and $C_t = C + C_{in}$ are the inductance and total capacitance of one segment of the loaded transmission lines, C is the parasitic capacitance of one segment transmission line.

Substituting the expression for the loaded line characteristic impedance Eq. (3.31) or Eq. (3.34) into Eq. (3.40) gives

$$f_0 = \frac{Z_0}{2NL} \quad (3.41)$$

or

$$f_0 = \frac{1}{2NZ_0C_t} \quad (3.42)$$

The first three factors on the left side of Eq. (3.37) make up the magnitude part which may be used to determine G_m and thus the oscillation amplitude V_{amp} .

The following relation is true

$$G_m \cdot \frac{Z_0}{2} \cdot \frac{e^{-\alpha_d Nl} - e^{-\alpha_s Nl}}{\alpha_s l - \alpha_d l} = 1 \quad (3.43)$$

And so

$$G_m = \frac{1}{\frac{Z_0}{2} \cdot \frac{e^{-\alpha_d Nl} - e^{-\alpha_s Nl}}{\alpha_s l - \alpha_d l}} \quad (3.44)$$

The amplitude associated with G_m is found from [Lee98].

$$G_m \approx \frac{2I_{bias}}{V_{amp}} \quad (3.45)$$

where I_{bias} is drain to source bias current.

That is

$$V_{amp} \approx \frac{2I_{bias}}{G_m} = I_{bias} Z_0 \cdot \frac{e^{-\alpha_d Nl} - e^{-\alpha_s Nl}}{\alpha_s l - \alpha_d l} \quad (3.46)$$

3.3.3 Biasing

Fig. 3.13 Current source biasing scheme

Based on Eq. (3.46), oscillation amplitude is a function of bias current I_{bias} . In order to control oscillation amplitude easily and avoid electrical over-stress (EOS), Current source biasing is needed in distributed oscillators. The biasing scheme is given in Fig. 3.13. Tuning of this oscillator can also benefit from such a biasing scheme.

3.3.4 Tuning Considerations

Oscillator tunability is obviously necessary in many applications such as in PLLs. In addition to this requirement, a general ‘rule of thumb’ to use when designing a voltage-tunable oscillator is that one should augment the frequency-range bounds of the original design by an additional $\pm 20\%$ to compensate for process variations and for modeling approximations.

In a distributed oscillator like that of Fig. 3.12, the parasitic capacitances of the transistors can exhibit varactor-like behavior, their values will depend to some degrees upon applied voltages. This effect can be used to achieve the desired voltage-control over frequency. And an AC coupling capacitor C_{couple} is applied in the feedback to isolate DC

signal, so tuning can be achieved by changing DC voltages on the gate line and the drain line independently to change parasitic capacitances from transistors.

When DC voltages of gate line and drain line are adjusted to tune the oscillation frequency, it is necessary to keep a constant DC operating point by using a current source biasing shown in Fig. 3.13. Otherwise, the change of DC voltage may vary the transconductance, output resistance of the transistor, and oscillation amplitude.

3.4 An Approach to Distributed Oscillator Design

Based on the analysis of distributed amplifiers and oscillators in section 3.2 and 3.3, this section discusses an approach to design distributed oscillator from the lumped elements to transmission lines. The design procedure commences with a lumped-element approximation to the final circuit, the computed values being appropriate to the design goals, and then the lumped elements will be replaced by transmission lines which are easily integrated.

3.4.1 Design with Lumped Elements

Initially, the centre frequency f_0 and the number of stages N of an oscillator having the topology of Fig. 3.14 are specified, and then using the results of the previous two sections, the circuit parameters suitable to these requirements are determined. It is assumed at the outset that both artificial gate and drain lines will be matched to $Z_0 = 50\Omega$. In particular, the constraints developed in section 3.2.5 which guarantee equal phase velocities on both lines will be accepted here, namely that $L = L_g = L_d$ and $C_{add} = C_{in} - C_{out}$. One can use Eq. (3.41) and Eq. (3.42) to determine L and C_t (for lumped design, $C_t = C_{in}$ in Eq. (3.42)).

$$L = \frac{Z_0}{2Nf_0} \quad (3.47)$$

$$C_{in} = \frac{1}{2Nf_0Z_0} \quad (3.48)$$

Fig. 3.14 Distributed oscillator with lumped inductors

Driving transistor's size determination is a very important phase during the design. C_{in} is one factor used to determine the driving transistor's size. Another factor is oscillation amplitude V_{amp} since the amplitude (referring to Eq. (3.46)) is decided by bias current I_{bias} , Z_0 , the number of stage N , and driving transistor's size related parameters, such as C_{in} and R_{ds} . To meet both C_{in} requirement and amplitude specification, DC simulation followed by calculated confirmation through Eq. (3.46) needs to be done to find out the appropriate driving transistor's size and bias current I_{bias} . Doing DC simulation and calculation is actually an iterative process, one that begins with the designer supplying reasonable estimates of the parameter values.

Once the transistor's size is known, its output capacitance C_{out} can be obtained, and hence the additional capacitance added to the drain line is $C_{add} = C_{in} - C_{out}$.

3.4.2 Replacement of Lumped Elements with Transmission Lines

The next step is to replace the lumped inductors of the artificial transmission lines with actual transmission line segments. The additional capacitors C_{add} can be realized by transistors.

The replacement of the lumped inductors by transmission line segments involves finding the length of these. A practical way of solving this problem is to use simulation to model an unit length of $100\mu m$ (arbitrary) transmission line as a lumped π -type network made up of a series inductor L_π , a series resistor R_π and two end capacitances C_π to ground. Once L_π has been found, it can be used with the already-known value of L to find the segment length l .

$$l = 100\mu m \cdot \frac{L}{L_\pi} \quad (3.49)$$

Since transmission lines are equivalent to the inductors with parasitic end capacitances which contribute a certain amount of phase shift to affect the oscillation frequency and the characteristic impedances of gate and drain lines. Thus, in order to keep an identical center frequency f_0 and meanwhile meet matching requirement, Eq. (3.48) is then changed to

$$C_t = C_{in} + C = \frac{1}{2Nf_0Z_0} \quad (3.50)$$

The parasitic capacitance C is in turn related to L_π and C_π by

$$C = 2C_\pi \cdot \frac{L}{L_\pi} \quad (3.51)$$

For the design here, the value of C_{in} from Eq.(3.48) needs to subtract C . This results in a new value of C_{in} which is used to recompute the transistor size, and so C_{add} and then I_{bias} .

Using the values of the lumped elements determined in the previous section, the circuit parameters such as the length of each segment of transmission line as well as the transistor sizes have been determined.

3.5 Summary

This chapter has presented a theoretical analysis of distributed amplifiers. The configuration of the distributed amplifier has been described and its operation principles introduced. Transmission lines are critical components in distributed amplifier and their propagation constant and characteristic impedance are described by considering the loaded transistor's parasitics. An amplifier voltage gain expression that will turn out to be a useful design tool in analyzing the distributed oscillators has been derived. Maximum gain-assuring constraints upon the gate and drain transmission line characteristics and the corresponding design constraints were deduced. Also it is found that the number of stages that may be used in distributed amplifiers is limited due to the inherent losses from the loaded gate line and drain line.

A distributed oscillator circuit was then created by introducing feedback between the input and output connection of a distributed amplifier. Its behavior too was analyzed.

The oscillation condition was derived in terms of the gain of the incorporated amplifier and this led to analytical expressions for the amplitude and the frequency. The tuning technique was explored as well. Finally, a practical approach to design a distributed oscillator was introduced.

Analysis of Phase Noise in Distributed Oscillators

4.1 Introduction

Phase noise is of major concern in oscillators because the presence of even low level of noise in an oscillator may result in serious degradation of its output spectrum and thus timing (jitter) properties. Due to the importance of the problem, considerable efforts have been expending in understanding phase noise and in developing analytical and experimental techniques for its characterization. And an accurate means of quantifying phase noise would be a highly desirable tool for the circuit designers.

The objective of this chapter is to analyze and predict phase noise in distributed oscillators by employing the circuit topology presented in chapter 3. First, in section 4.2 definition of phase noise is established and the effects of phase noise in communication systems are overviewed. Phase noise is due to a considerable extent to MOSFET behavior, and noise sources in MOSFET devices are also studied. Section 4.3 begins with the introduction of a linear analysis model for a generalized oscillator, one which is then applied to the distributed oscillators. The result of this development leads to a closed-form expres-

sion for additive phase noise, which can be extended to include the effects of mixing (intermodulation) noise resulting from circuit nonlinearity. The dependence of phase noise upon design parameters is also discussed.

4.2 Phase Noise Overview

4.2.1 Phase Noise Definition

An ideal sinusoidal oscillator output voltage is described as a pure sine wave of constant frequency and amplitude, it is expressed as

$$V(t) = V_0 \sin \omega_0 t \quad (4.1)$$

where V_0 is the nominal amplitude of the signal, and ω_0 is the nominal angular frequency of oscillator.

For this ideal oscillator operating at ω_0 , the spectrum should just display an impulse as shown in Fig. 4.1 (a). In practice, it is impossible to have such an ideal output, which will always be accompanied by a certain amount of noise. The output is therefore more realistically expressed as

$$V(t) = V_0 [1 + A(t)] \sin [\omega_0 t + \phi(t)] \quad (4.2)$$

where $A(t)$ and $\phi(t)$ respectively denote the noise amplitude and phase.

The noise amplitude $A(t)$ can be eliminated using a limiter. Unfortunately the phase term $\phi(t)$, which cannot be reduced in the same manner, has a major impact on system performance. $\phi(t)$ may be discrete or random. The discrete signal is called spurious, and random phase fluctuation is commonly called phase noise.

For a practical oscillator, a central impulse at the desired frequency ω_0 will be accompanied by noise 'skirts' on either side as shown in Fig. 4.1 (b), which is a somewhat idealized diagram of this situation ('real' noise skirts are rather irregular).

Fig. 4.1 Output spectra of (a) ideal, noise-free and (b) practical oscillators

Fig. 4.2 Illustration of phase noise definition

Phase noise is a frequency-domain view of the noise spectrum around the oscillator signal, while jitter is a time-domain measure of the timing accuracy of the oscillator period. The frequency-domain depiction of phase noise has a much stronger intuitive appeal than that does the equivalent time-domain description. One can easily see the offending frequency components and their energies relative to that of the central fre-

quency. The single side band (SSB) phase noise is the common measure of oscillator phase instability. By this way, phase noise can be defined as a ratio of output SSB noise power $P_{noise}(\Delta\omega)$ (in an unit bandwidth at a certain offset frequency $\Delta\omega$ from carrier frequency) and carrier power P_c . It is customary to express this ratio as a logarithm having units of dBc/Hz (dBc means decibels relative to carrier power).

Referring to Fig. 4.2, the explicit formula for phase noise $L(\Delta\omega)$ is expressed as

$$L(\Delta\omega) = 10 \cdot \log \frac{P_{noise}(\Delta\omega)}{P_c} \quad (4.3)$$

4.2.2 Phase Noise Effects in Communication Systems

In clock recovery and data acquisition systems, the clock timing jitter added to the expected data jitter narrows the effective decoding window, further reducing the maximum operating frequency of the system and increasing bit error rates.

In wireless communication systems, any local oscillator phase noise occurring in a transceiver has important effects on both the reception and transmission of signals.

Fig. 4.3 Down conversion in an ideal receiver

In receivers, an LO is used to down convert the output of a RF amplifier to an intermediate frequency (IF) signal prior to demodulation. Ideally, the down-conversion process consists of the receiver's mixer multiplying the RF input by the LO signal, followed by the extraction of the IF signal using a low-pass filter, as shown in Fig. 4.3.

Fig. 4.4 Reciprocal mixing effect in a practical receiver

But in a real situation of receiver, the desired signal may be accompanied by a strong interfere from an adjacent channel, and the LO exhibits finite phase noise when two signals are mixed with LO output, then IF output will consist of two overlapping spectra, with the desired signal suffering from significant noise due to the tail of the interfere. This effect is called “reciprocal mixing” and it is illustrated in Fig. 4.4.

As shown in Fig. 4.5, phase noise in transmitter can thus cause interference with nearby frequency channels. A noiseless receiver detects a weak signal at ω_2 , while an adjacent transmitter generates a powerful signal at ω_1 with phase noise. Thus, the desired signal is degraded by the phase noise tail from the transmitter. For this reason, maximum LO phase noise levels are set. For example, the North American Digital Cellular standard ‘IS-54’, which covers systems using carrier frequencies in the 900MHz range, limits the

phase noise to a maximum of 115dB below the carrier power at a 60kHz offset from the carrier [Raz98].

Fig. 4.5 Phase noise effect from transmitter

4.2.3 Noise Sources in MOSFET Devices

The three principal types of noise in solid-state devices are thermal noise, flicker noise, and shot noise.

4.2.3.1 Thermal Noise

Thermal noise, a fundamental physical phenomenon in any linear passive resistor, is caused by the random thermal motion of the electrons in a resistive medium. The thermal noise of a MOSFET is a combination of that due to channel resistance, bulk resistance and parasitic drain, gate, source resistance thermal noise contributions. Of these, it is only the channel resistance thermal noise which receives attention in most MOSFET models. The noise can then be modeled by a current source as shown in Fig. 4.6 (a). For a device in saturation, the mean square of this noise current can be expressed as [GrTe86]

$$\overline{i_{nt}^2} = 4kT \cdot \frac{2}{3}g_m \cdot \Delta f \quad (4.4)$$

where $k = 1.38 \times 10^{-23} \text{ J/K}$ is Boltzmann's constant. T is the absolute temperature in degrees Kelvin. g_m is the small-signal transconductance at the operating point. Δf is the noise bandwidth in hertz.

Fig. 4.6 Equivalent models for the thermal noise in a MOSFET

In most circuits, it is convenient to assume that $\overline{i_{nt}^2}$ is caused by a voltage source connected to the gate of a MOSFET as shown in Fig. 4.6 (b). This gate-referred noise voltage source is given by [GrTe86]

$$\overline{v_{nt}^2} = \frac{8}{3} \cdot \frac{kT}{g_m} \cdot \Delta f \quad (4.5)$$

According to Eqs. (4.4) and (4.5), it is shown that the noise spectral density $\overline{i_{nt}^2}/\Delta f$ or $\overline{v_{nt}^2}/\Delta f$ is independent of frequency, and this independence is found to be maintained up to 10^{13} Hz. Thus, thermal noise may be regarded as the source of white noise.

However, the above model is not valid in the MOSFET linear region. For instance, for the drain voltage $V_{ds} = 0$, it predicts $\overline{i_{nt}^2} = 0$. Whereas $\overline{i_{nt}^2}$ should be $4kTg_{do}$, where g_{do} is the drain-source conductance at $V_{ds} = 0$ [Fox93].

The results discussed so far are for long-channel FETs. It is found experimentally that short-channel devices can be significantly noisier than what long-channel theory would suggest. One reason is due to short-channel effects such as velocity saturation. Another is that the hot-carrier effects due to the large electric fields presented in short-channel devices near the drain. The effects of these can be modeled by an equivalent ‘carrier temperature’ that is higher than the lattice temperature, so it is not surprising that short-channel devices may produce higher thermal noise than that predicted by long-channel theory. Thus, for short-channel FETs, the factor of 2/3 in Eq. (4.4) used for long-channel FETs in saturation will be larger [Tsi87] [WaHe94].

4.2.3.2 Flicker Noise

Flicker noise, also known as $1/f$ noise, is mainly caused by traps associated with contamination and crystal defects. These traps capture and release carriers in a random fashion and the time constants associated with the process give rise to a noise signal with energy concentrated at low frequency [GrMe93]. In a MOSFET device, extra electron energy states exist at the boundary between the Si and SiO₂. These can trap and release electrons from channel, and hence introduce noise [GrTe86].

A usable model of this noise phenomenon is a current source in parallel with the channel resistance (similar to Fig. 4.6 (a)). The mean square current of the noise source is described by [GrMe93]

$$\overline{i_{nf}^2} = K_1 \cdot \frac{I_d^\alpha}{f} \cdot \Delta f \quad (4.6)$$

where K_1 is a device-dependent constant, I_d is the drain bias current and α is a constant with the value varying from 0.5 to 2.

Alternatively, flicker noise can be represented by its gate-referred voltage source, in series with the transistor gate terminal (similar to Fig. 4.6 (b)). It is expressed by

$$\overline{v_{nf}^2} = \frac{K}{C_{ox}WL} \cdot \frac{1}{f} \cdot \Delta f \quad (4.7)$$

where K depends on the temperature and fabrication process. Typically, K is equal to $3 \times 10^{-24} V^2 \cdot F$. W and L represent the transistor's width and length, and C_{ox} is the transistor's gate oxide capacitance per unit area.

In most cases, the gate-referred noise voltage is nearly independent of the bias conditions. Eq. (4.7) shows that $1/f$ noise is inversely proportional to the transistor area and C_{ox} . In a typical submicron CMOS device, the corner frequency of $1/f$ noise may be as high as 1MHz [Tsi87].

4.2.3.3 Shot Noise

Shot noise is caused by the fluctuations in the current flowing across a PN junction. Its mean square associated with a junction current I is given by [GrTe86]

$$\overline{i_{ns}^2} = 2qI\Delta f \quad (4.8)$$

where $q = 1.6 \times 10^{-19} C$ is the electronic charge.

The shot noise spectral density $\overline{i_{ns}^2}/\Delta f$ is constant as a function of frequency and it is that of wide-band white noise, which gets worst with increasing average current. For a MOSFET, it exhibits shot noise in the subthreshold region due to the leakage current I_l flowing in the channel. This noise can be expressed as

$$\overline{i_{ns}^2} = 2qI_l\Delta f \quad (4.9)$$

Also, when the dimension of a MOSFET is scaled down, the gate oxide thickness is reduced. The resulting increase in gate leakage current due to tunneling leads to an increase in shot noise. In practice, shot noise associated with the above two current effects is usually small and can be negligible.

4.3 Phase Noise in Distributed Oscillators

The main noise sources in CMOS oscillators are thermal noise originating in passive and active devices, flicker noise from the MOSFETs, and supply and substrate noise. The flicker noise of the transistors and supply and substrate noise are relevant at small offset frequencies [HePi00], thus they are disregarded in this work. Only the dominant noise source, thermal noise, will be considered. A frequency-domain analytical method is employed for the purpose of predicting phase noise in distributed oscillators. A first-order linear model of oscillatory system is used as a foundation to develop the basic linear noise prediction formulae, which are then extended to account for noise due to nonlinear effects as well.

4.3.1 The Linear Oscillator Model

Fig. 4.7 The linear oscillator model

Fig. 4.7 shows the simplest small-signal linear model for a generalized oscillator [Raz962]. It will be assumed that the Barkhausen criterion is satisfied. The summing junction

tion at the input is not present in a practical device, but it has been placed in this model to facilitate a simplified theoretical development. Each noise source in this oscillator is modeled as an input signal. At frequencies close to that of the carrier, $\omega = \omega_0 + \Delta\omega$, the noise power spectral density is shaped by

$$\left| \frac{Y_o}{X_i} [j(\omega_0 + \Delta\omega)] \right|^2 = \frac{1}{(\Delta\omega)^2 \cdot \left| \frac{dH(j\omega)}{d\omega} \right|^2} \quad (4.10)$$

The spectrum of input noise is shaped by this function as shown in Fig. 4.8.

Fig. 4.8 Noise shaping in a linear oscillatory system

If the open-loop transfer function $H(j\omega)$ is written in the polar form $H(j\omega) = A(\omega) \cdot e^{j\phi(\omega)}$, one finds that its derivative is

$$\frac{dH(j\omega)}{d\omega} = \left(\frac{dA(\omega)}{d\omega} + jA(\omega) \cdot \frac{d\phi(\omega)}{d\omega} \right) \cdot e^{j\phi(\omega)} \quad (4.11)$$

And when $\omega \approx \omega_0$, $A(\omega) \approx 1$, it can be obtained that

$$\left| \frac{dH(j\omega)}{d\omega} \right|^2 = \left(\frac{dA(\omega)}{d\omega} \right)^2 + \left(\frac{d\phi(\omega)}{d\omega} \right)^2 \quad (4.12)$$

Thus, Eq. (4.10) takes the form

$$\left| \frac{Y_o}{X_i} [j(\omega_0 + \Delta\omega)] \right|^2 = \frac{1}{(\Delta\omega)^2 \cdot \left[\left(\frac{dA(\omega)}{d\omega} \right)^2 + \left(\frac{d\phi(\omega)}{d\omega} \right)^2 \right]} \quad (4.13)$$

4.3.2 Analysis of Phase Noise in Distributed Oscillators

The amplitude behavior of an oscillator is essentially nonlinear. However, it is found that the linear analysis can be very useful to model the oscillator's phase noise behavior. Additive phase noise characteristics in oscillators are linear and so linear method can be used to analyze this aspect of its operation. This will now be done, and then the capability of treating mixing (intermodulation) noise contributions will be added. The analysis of phase noise here adopts the circuit topology of a distributed amplifier based oscillator, which is as same as that of [KIDi99][KIDi01][WuHa01].

4.3.2.1 Additive Noise

Additive noise consists of independent contributions occurring along the output path. Each component can be calculated using Eq. (4.10) or Eq. (4.13).

Fig. 4.9 Additive noise originating in the signal propagation path

In the ensuing study of additive noise in distributed oscillators using the linear oscillator model, it is assumed that the signal amplitude at the circuit's internal nodes is small and that therefore a linear approximation of circuit behavior will be valid. The noise shaping function of Eq. (4.13) obtained previously by using a linear system assumption will be utilized to derive an expression for phase noise which is mainly attributed to the presence of thermal noise in the signal path.

Fig. 4.9 shows a CMOS distributed oscillator where the thermal noise of each transistors is modeled as the current sources I_{noise1} , I_{noise2} , ..., and I_{noiseN} , each being directly connected to the drain line. The impedance seen by the modeled current source at its connection point is $Z_d/2$ ($= Z_0/2$). The each resulting noise voltage appearing here travels along the drain line and through feedback emerges at node 1 as an equivalent input noise, assuming that $l_g = l_d = l$, their power densities are expressed as

$$|V_{in, noise1}|^2 = I_{noise1}^2 \cdot \left(\frac{Z_0}{2}\right)^2 \cdot \left(e^{-\alpha_d \left(N-1 + \frac{1}{2}\right)l}\right)^2 \quad (4.14)$$

$$|V_{in, noise2}|^2 = I_{noise2}^2 \cdot \left(\frac{Z_0}{2}\right)^2 \cdot \left(e^{-\alpha_d \left(N-2 + \frac{1}{2}\right)l}\right)^2 \quad (4.15)$$

...

$$|V_{in, noiseN}|^2 = I_{noiseN}^2 \cdot \left(\frac{Z_0}{2}\right)^2 \cdot \left(e^{-\alpha_d (1/2)l}\right)^2 \quad (4.16)$$

where $I_{noise}^2 = 4kT \cdot \frac{2}{3}g_m$ is the drain-current-referred thermal noise power spectral density of a MOSFET. For the short-channel devices, the noise power may be higher, a situation corresponding to the factor $2/3$ having an actual value of up to 0.873 [Raz962].

If the reasonable assumption that $I_{noise1} = I_{noise2} = \dots = I_{noiseN} = I_{noise}$ is made, the total input noise power density at node 1 due to currents $I_{noise1}, \dots, I_{noiseN}$ may be deduced

$$|V_{in, noise, total}|^2 = I_{noise}^2 \cdot \left(\frac{Z_0}{2}\right)^2 \cdot \sum_{n=1}^N \left(e^{-\alpha_d \left(N-n+\frac{1}{2}\right)l} \right)^2 \quad (4.17)$$

Substitution of Eq. (4.17) into Eq. (4.13) yields an output noise power density, namely

$$\begin{aligned} |V_{out, noise}|^2 &= \frac{|V_{in, noise, total}|^2}{(\Delta\omega)^2 \cdot \left[\left(\frac{dA(\omega)}{d\omega} \right)^2 + \left(\frac{d\phi(\omega)}{d\omega} \right)^2 \right]} \\ &= \frac{I_{noise}^2 \cdot \left(\frac{Z_0}{2}\right)^2 \cdot \sum_{n=1}^N \left(e^{-\alpha_d \left(N-n+\frac{1}{2}\right)l} \right)^2}{(\Delta\omega)^2 \cdot \left[\left(\frac{dA(\omega)}{d\omega} \right)^2 + \left(\frac{d\phi(\omega)}{d\omega} \right)^2 \right]} \end{aligned} \quad (4.18)$$

According to Eq. (4.18), the distributed oscillator open-loop transfer function which is that of a distributed amplifier is needed. Referring to Eq. (3.35), its amplitude and phase components are

$$A(\omega) = -g_m \cdot \frac{Z_0}{2} \cdot \frac{e^{-\alpha_d Nl} - e^{-\alpha_g Nl}}{\alpha_g l - \alpha_d l} \quad (4.19)$$

$$\phi(\omega) = -\beta Nl \quad (4.20)$$

The derivatives of above amplitude and phase components required by Eq. (4.18) are

$$\frac{dA(\omega)}{d\omega} = -g_m \cdot \frac{Z_0}{2} \cdot \left[\frac{NC_{in}^2 R_{in} Z_0 \omega e^{-\alpha_g Nl}}{\alpha_g l - \alpha_d l} - \frac{C_{in}^2 R_{in} Z_0 \omega (e^{-\alpha_d Nl} - e^{-\alpha_g Nl})}{(\alpha_g l - \alpha_d l)^2} \right] \quad (4.21)$$

$$\frac{d\phi(\omega)}{d\omega} = -N\sqrt{L(C + C_{in})} = -NZ_0(C + C_{in}) \quad (4.22)$$

where C is the parasitic capacitance from one segment of transmission line.

4.3.2.2 Mixing Noise

The above analysis of additive phase noise proceeds under the assumption of a linear feedback system. However, oscillators are actually nonlinear devices because amplitude limiting is a nonlinear process. One side-effect of this nonlinearity is the mixing of the noise in the signal path with the carrier signal. There is a substantial noise energy in harmonics whose frequencies are near to carrier frequency ω_0 and these components are involved in the creation of mixing noise, or intermodulation noise.

In general, the response of a nonlinear circuit to an input signal $V_{in}(t)$ is

$$V_{out}(t) = \sum_{i=0}^n a_i V_{in}^i(t) \quad (4.23)$$

If an input includes carrier and noise components, it may be written as

$$V_{in}(t) = A_0 \cos \omega_0 t + A_n \cos \omega_n t \quad (4.24)$$

where A_0 and ω_0 are the amplitude and frequency of the carrier. A_n and ω_n are the amplitude and frequency of noise.

The output will contain components at the harmonics of the two input frequencies and at the sum and difference frequencies of those harmonics.

In the case of oscillators, assume the third-order approximation, this leads to the nonlinear input/output relationship

$$V_{out}(t) = a_0 + a_1 V_{in} + a_2 V_{in}^2 + a_3 V_{in}^3 \quad (4.25)$$

The important noise components in the output spectrum will be those due to intermodulation and will appear at the frequencies ω_n , $\omega_0 + \omega_n$, $\omega_0 - \omega_n$, and $2\omega_0 - \omega_n$. When the frequency of noise source ω_n is small, the resulting noise components at frequencies $\omega_0 - \omega_n$ and $\omega_0 + \omega_n$ will appear in band and noise component at frequency $2\omega_0 - \omega_n$ will be out of band. For this case, it is assumed that noise amplitudes are much smaller than the signal amplitude. Therefore, the noise contributions from the frequencies $\omega_0 - \omega_n$ and $\omega_0 + \omega_n$ can be negligible. For the case of the noise source frequency ω_n close to carrier frequency ω_0 , the resulting noise components at frequencies $\omega_0 - \omega_n$ and $\omega_0 + \omega_n$ will be out of band. Only the components of ω_n and $2\omega_0 - \omega_n$ are dominant and depend on the noise shaping properties of the feedback oscillatory system. These two components will have approximately equal magnitude. Thus, intermodulation has the effect of duplicating noise components originating below (above) ω_0 to symmetrical positions above (below) this frequency as shown in Fig. 4.10 [Raz962].

This effect is accounted for by doubling the output noise power density predicted by Eq. (4.18). The total output noise power density after adjustment due to intermodulation effects is

$$|V_{out, noise, total}|^2 = \frac{2 \cdot I_{noise}^2 \cdot \left(\frac{Z_0}{2}\right)^2 \cdot \sum_{n=1}^N \left(e^{-\alpha_d \left(N-n+\frac{1}{2}\right)\tau} \right)^2}{(\Delta\omega)^2 \cdot \left[\left(\frac{dA(\omega)}{d\omega} \right)^2 + \left(\frac{d\phi(\omega)}{d\omega} \right)^2 \right]} \quad (4.26)$$

Fig. 4.10 Noise component transferring due to intermodulation effects

4.3.2.3 Power Supply and Substrate Noise

As scaling of COMS technology along with the design of analog circuits and large complex digital signal processing components on the same die, due to the high-level of interactions between the noisy digital blocks with the noise sensitive analog parts through various propagation mechanisms, it is highly possible that the large signal switching transients of the digital circuits corrupt the performance of analog sub-block. Crosstalk from digital circuits on analog components is mostly via substrate. Oscillators as the part of analog circuits operate under the global supply and ground buses, thus suffering from both power supply and substrate noise [HeRa98][HeRa99]. Therefore, phase noise caused by the power supply and substrate noise becomes increasingly significant. In order to remedy the above problems, many noise isolation techniques, such as physical separation, ground shield, trench oxide isolation, deep N-well, P-substrate guard ring, N-well guard ring, double guard ring, and Kelvin grounding, have been developed.

4.3.3 Discussion

Based on the phase noise definition by Eq. (4.3) and analysis above, distributed oscillator phase noise can be expressed as

$$\begin{aligned}
 L(\Delta\omega) &= 10 \cdot \log \frac{|V_{out, noise, total}|^2}{V_c^2} \\
 &= 10 \cdot \log \frac{2 \cdot I_{noise}^2 \cdot \left(\frac{Z_0}{2}\right)^2 \cdot \sum_{n=1}^N \left(e^{-\alpha_d \left(N-n+\frac{1}{2}\right) l} \right)^2}{(\Delta\omega)^2 \cdot \left[\left(\frac{dA(\omega)}{d\omega} \right)^2 + \left(\frac{d\phi(\omega)}{d\omega} \right)^2 \right] V_c^2} \quad (4.27)
 \end{aligned}$$

At a constant carrier power V_c^2 , phase noise is a function of $|V_{out, noise, total}|^2$. The term $dA(\omega)/d\omega$ is negligible compared to $d\phi(\omega)/d\omega$ at frequencies close to ω_0 and $(Z_0/2)^2$ is a constant. Furthermore, the following dependencies were established earlier in section 4.3.2.1.

$$I_{noise}^2 \propto g_m \quad (4.28)$$

$$\sum_{n=1}^N \left(e^{-\alpha_d \left(N-n+\frac{1}{2}\right) l} \right)^2 \propto R_{ds} \cdot N \quad (4.29)$$

$$(d\phi(\omega)/d\omega)^2 \propto N^2 \cdot (C + C_{in})^2 \quad (4.30)$$

Based on Eqs. (4.28), (4.29), and (4.30), an approximate expression for the phase noise with respect to the circuit parameters may be

$$L(\Delta\omega) \propto 10 \cdot \log [g_m \cdot R_{ds} \cdot N / (N^2 (C + C_{in})^2)] \quad (4.31)$$

To provide the reader more insight, two representative cases are described.

Case 1: The distributed oscillators designed at the different frequencies but having the same topology and the same number of stages N .

The frequency of a distributed oscillator is given by $f = 1/(2 \cdot N \cdot Z_0 \cdot (C + C_{in}))$. Here N and Z_0 are both constants. It can be seen that the operating frequency can be controlled by driving transistor input capacitance C_{in} and parasitic capacitance C from each segment of transmission line. One must keep in mind that if C_{in} changes, the length of transmission line must be adjusted correspondingly to change its equivalent inductance, thus satisfying the requirement of $Z_0 = 50\Omega$. Meantime, the change of transmission line will also result in a change of C which is directly proportional to C_{in} . In other words, one can change the oscillation frequency by using different transistor sizes (changing C_{in}). It is observed that the higher the operating frequency, the smaller will be C_{in} . Smaller input capacitance corresponds to a smaller g_m and a larger R_{ds} . Theoretical calculation shows that the resulting effects due to the changes of g_m and R_{ds} can be cancelled out. Therefore $(C + C_{in})^2$ is a dominant term in the expression of Eq. (4.31). Thus, the worse phase noise performance is predicted at the higher oscillating frequency.

Case 2: Two distributed oscillators designed to operate at the same frequency but having different numbers of stages N .

The equation $f = 1/(2 \cdot N \cdot Z_0 \cdot (C + C_{in}))$ indicates that to have the same frequency, the product of N and $C + C_{in}$ must be identical in both cases. One can observe that if the oscillator is realized with more stages N , a smaller C_{in} (and therefore transistor

size) will be necessary. There will be more noise sources from the increased number of stages, but each will contribute a lower noise amplitude because of its smaller g_m value which results from its smaller size. An oscillator with fewer stages will in turn have fewer noise sources, but ones generating larger amplitudes. Theoretical calculation shows that two oscillators will have almost the same input noise power. Meantime, the values of $d\phi(\omega)/d\omega$ for both oscillators are identical. It means that two oscillators will have the same effect on the noise transferring. Therefore, it is expected that the phase noise from these two oscillators will give about the same performance despite a different number of stages employed.

4.4 Summary

Phase noise generated by oscillators that are to be used in communication applications is a matter of great concern. This chapter has dealt with some important issues related to phase noise in the distributed oscillators.

Phase noise in distributed oscillator has been explored in the frequency domain by analyzing both linear and nonlinear conditions. As a result, the analytical formulae are derived for predicting the distributed oscillator phase noise. Upon the discussion of derived formulae, the plausible reasons for the worsening of phase noise performance with increasing frequency was presented when oscillators have the same number of stages operating at the different frequencies, as was the reasons for little or no-effect on phase noise while oscillators have the different number of stages operating at the same frequency.

Verification through Simulation

5.1 Introduction

In chapter 4, analytical formulae for the phase noise of distributed oscillators were developed. In this chapter, the accuracy of those analytical formulae is demonstrated by HB simulation in ADS. The process used for the design is a $0.13\mu m$ silicon CMOS technology.

In designing distributed oscillators, special attention should be paid to the modeling of the transmission lines since the lossy nature of silicon substrate can have a strong effect on their operation. This modeling is the subject of section 5.2. Then it is followed by an example which makes use of a 10GHz distributed oscillator as a concrete aid to obtain better understanding on design process in section 5.3. In section 5.4, the methods of phase noise calculation and simulation are illustrated by using that same 10GHz oscillator as a test case. Section 5.4 ends with the comparison of calculated and simulated phase noise for five test cases. Three of these are 4-stage oscillators designed for operation at different

frequencies, while the others are 4-stage and 5-stage designs having identical operating frequency.

5.2 Transmission Line Modeling

As illustrated in Fig. 3.12, the design of a distributed oscillator incorporates with transmission lines, which are components of great importance in distributed oscillator realization and must be designed with great care. In this work, the coplanar stripline (CPS) is chosen because of its physical simplicity. A CPS is made up of just one signal line parallel with one ground line adjacent to it. Fewer pads and less area are required than for a coplanar waveguide which consists of one signal line along with two ground lines adjacent to it.

As illustrated in section 3.2.4, the short piece of length of a transmission line was modeled as a lumped element circuit as given in Fig. 3.7. In practical, it is required to use a field simulator in order to obtain sufficiently accurate line parameters due to physical complexities. In the present case, a $100\mu m$ CPS segment is used as a starting point, and its behavior is simulated in Momentum, a planar electromagnetic (EM) simulator which can be used for passive circuit analysis. Momentum can work with ADS to compute S-, Y-, and Z-parameters of general planar circuits. Various transmission lines can be analyzed quickly and accurately with Momentum.

Before a Momentum simulation of a CPS is commenced, a series of parameters associated with the interconnect stack, substrate, CPS dimension, and other simulation details must be defined. Fig. 5.1, a simplified interconnect cross-section of $0.13\mu m$ CMOS technology with an embedded CPS, shows that the stripline components are sur-

rounded by multi-layer dielectrics and routed on metal 8 with thickness of $0.9\mu m$ (TSMC $0.13\mu m$ CMOS interconnects cannot be revealed, just the method of its simplification is detailed in Appendix B). CPS located at the top metal takes advantage of a low metal resistance and a larger separation from the substrate, thus serving to reduce losses associated with the silicon substrate. The top view of the CPS in Fig. 5.2 shows its geometry and dimension. The details of laying out a CPS with finite thickness, and the details of Momentum simulation setups may be found in Appendix C.

Fig. 5.1 A simplified interconnect cross-section of $0.13\mu m$ CMOS technology

Fig. 5.2 CPS geometry and dimension

When the suitable parameters have been identified, the S-parameters of the $100\mu m$ CPS can be obtained and used by the tool of spice model generator in ADS to produce the lumped π -type RLC network model shown in Fig. 5.3.

Fig. 5.3 RLC model of $100\mu m$ CPS

5.3 An Example of Designing a Distributed Oscillator

Based on the circuit topology of Fig. 3.14 and the discussion of section 3.4, circuit parameters, such as transistor size, lumped element values or transmission line lengths, can be decided in terms of design goals.

In the following, an example of a 10GHz distributed oscillator with 50Ω matching requirement is used to provide a case study to illustrate the procedure of determining circuit parameters.

Oscillator is first designed with lumped elements and the schematic of the 4-stage oscillator is shown in Fig. 5.4 where the current source is used as biasing circuit. As required, the operating frequency of 10GHz and characteristic impedances of artificial gate line and drain line are made to be equal to 50Ω . The inductances in artificial gate line

and drain line are denoted by L_g and L_d respectively. If it is further required that the two be equal ($L_g = L_d = L$), Eq. (3.47) may be used to find their common value L

$$L = \frac{Z_0}{2Nf_0} = \frac{50}{2 \cdot 4 \cdot 10 \times 10^9} = 625 \text{ pH} \quad (5.1)$$

Fig. 5.4 Schematic of a 10GHz distributed oscillator with lumped elements

The input (gate) capacitance C_{in} of each driving transistor is given by Eq. (3.48)

$$C_{in} = \frac{1}{2Nf_0Z_0} = \frac{1}{2 \cdot 4 \cdot 10 \times 10^9 \cdot 50} = 250 \text{ fF} \quad (5.2)$$

As introduced in section 3.4.1, driving transistor's size and bias current I_{bias} are determined by both C_{in} and amplitude specification V_{amp} (0.5-0.6V in this design). Iterative DC simulation followed by calculated confirmation through Eq. (3.46) is needed. Several mA of I_{bias} as a reasonable start point is used in this case. The parameters which lead to optimal satisfaction of these requirements are listed in Table. 5.1.

Table 5.1 Parameters of driving transistor (design with lumped elements)

Parameter	Value
Transistor width	$6 \times 31.5\mu m$
Transistor length	$0.13\mu m$
R_{in}	8Ω
C_{in}	$250fF$
C_{out}	$153fF$
$g_{ds}(1/R_{ds})$	$5.66mS$
I_{bias}	$3.9mA$

The additional capacitance C_{add} can be calculated from the data in Table 5.1.

$$C_{add} = C_{in} - C_{out} = 250fF - 153fF = 97fF \quad (5.3)$$

Oscillation amplitude can be calculated by substituting the corresponding parameters listed in Table 5.1 into Eq. (3.46), it is found that $V_{amp}=0.54V$.

Once values for all of the components in Fig 5.4 are determined, an open-loop S-parameter simulation is done to verify whether there is a sufficient open-loop gain for oscillation to occur, and a closed-loop HB simulation is used to confirm that the desired oscillation frequency and amplitude will be achieved. Fig. 5.5 gives the simulation result of S-parameter S_{21} , which is the small signal open-loop gain. It is evident that the gain near 10GHz is about 11.52dB. Fig. 5.6 gives the HB simulation results which show an oscillation frequency of 9.62GHz and an amplitude of 0.58V.

Fig. 5.5 S-parameter S_{21} for a 10GHz distributed oscillator with lumped elements

Fig. 5.6 HB simulation results for a 10GHz distributed oscillator with lumped elements

The next step is the replacement of the lumped inductances with CPS segments. The length l of each segment can be determined by using the results obtained for a lumped π -type RLC network model of the $100\mu m$ CPS, as described in section 5.2.

The length of one segment l is found by scaling

$$l = 100\mu m \cdot \frac{L}{L_\pi} = 100\mu m \cdot \frac{625pH}{58pH} = 1078\mu m \quad (5.4)$$

Since CPS consists of parasitic capacitance C , a correction to C_{in} is necessary to make both the matching to a 50Ω terminated resistance and the maintenance of a centre frequency $f_0 = 10$ GHz. The parasitic capacitance C is also found by scaling

$$C = 2C_\pi \cdot \frac{L}{L_\pi} = 2 \cdot 2.7fF \cdot \frac{625pH}{58pH} = 58fF \quad (5.5)$$

The corrected value of the input capacitance of driving transistor is now calculated

$$C_{in} = \frac{1}{2nf_0Z_0} - C = 250fF - 58fF = 192fF \quad (5.6)$$

The same procedure as in lumped element design is used for resizing the driving transistor and adjust bias current due to the change of input capacitance C_{in} . The corresponding parameters for optimized driving transistor and bias current are given in Table 5.2.

The corrected value of C_{add} will be

$$C_{add} = C_{in} - C_{out} = 190fF - 118fF = 72fF \quad (5.7)$$

Gate capacitance of a transistor can be used to implement the relatively small capacitance C_{add} by connecting transistor's drain and source terminals with bulk as shown in Fig. 5.7. This capacitance is determined by transistor size.

Table 5.2 Parameters of driving transistor (design with transmission lines)

Parameter	Value
Transistor width	$6 \times 24.5\mu m$
Transistor length	$0.13\mu m$
R_{in}	7Ω
C_{in}	$190fF$
C_{out}	$118fF$
$g_{ds}(1/R_{ds})$	$5.13mS$
I_{bias}	$3.87mA$

Fig. 5.7 A transistor configuring as a capacitor

Schematic of a 10GHz distributed oscillator with CPSs is given in Fig. 5.8 where CPS segments are not shown in schematic and they are laid out in Momentum, just boxes labelled with S2P as data items are used to gather each CPS segment S-parameter data simulated by Momentum. Because transistor size is reduced, the open-loop gain must be checked again to make sure a sufficient gain. The simulation result of S-parameter S_{21} is

shown Fig. 5.9. One can see that the gain is about 10.56dB around 10GHz. HB simulation results for an oscillation frequency of 9.7GHz and an oscillation amplitude of 0.49V are given in Fig. 5.10.

Fig. 5.8 Schematic of a 10GHz distributed oscillator with CPSs

Fig. 5.9 S-parameter S_{21} for a 10GHz distributed oscillator with CPSs

Fig. 5.10 HB simulation results for a 10GHz 4-stage distributed oscillator with CPSs

5.4 Phase Noise Calculation and Simulation

In this section, the previous 10GHz 4-stage distributed oscillator continues to be used as the procedure of phase noise calculation and simulation is illustrated.

5.4.1 Calculation

The phase noise calculation proceeds as follows. For the above 10GHz distributed oscillator, Table 5.3 lists a series of parameters for calculating phase noise. First, at 1MHz offset frequency the additive phase noise power is found by substituting the appropriate parameters into Eq. (4.18), and then the result is doubled to account for intermodulation

effects, as described in chapter 4. The resulting figure is the total output noise power density. The voltage amplitude of carrier can be calculated by Eq. (3.46), from which the carrier power can be found. The phase noise is shown to be equal to -98.7dBc/Hz at a 1MHz offset from the carrier frequency.

Table 5.3 Parameters for a 10GHz 4-stage distributed oscillator phase noise calculation

Parameter	Value
N number of stage	4
f_0	10GHz
Δf	1MHz
Z_0	50 Ω
g_m	49.82mS
R_{in}	7 Ω
C_{in}	190fF
$g_{ds}(1/R_{ds})$	5.13mS
I_{bias}	3.87mA

5.4.2 Simulation

The oscillator phase noise can be measured by HB simulation. For the 10GHz distributed oscillator designed above, one begins with an accurate Momentum simulation of a segment length of the CPS, S-parameter data of which obtained will be used for the oscillator analysis by HB simulation. This distributed oscillator itself is shown in the schematic of Fig. 5.8, and the HB simulation test bench in Fig.5.11. The simulation yields data for the plot of Fig. 5.12, the phase noise is -96.6dBc/Hz.

Fig. 5.11 HB simulation test bench

Fig. 5.12 Phase noise result by HB simulation

5.4.3 Comparison of Calculated and Simulated Phase Noise

To verify the accuracy of theoretical phase noise analysis in chapter 4, more cases are examined by simulation. In simulation, the following two type cases discussed in chapter 4 are considered:

(1) 4-stage distributed oscillators are designed to operate at three different frequencies.

(2) Two distributed oscillators, one with 4-stage and one with 5-stage, are designed to operate at the same frequency.

Table 5.4 Comparison of phase noise for 4-stage distributed oscillators operating at three different frequencies

Desired frequency GHz	Actual frequency GHz	Phase noise calculation dBc/Hz 1M offset	Phase noise simulation dBc/Hz 1M offset	Error calculation/ simulation dB
10.0	9.7	-98.7	-96.6	2.1
14.0	13.6	-96.2	-93.3	2.9
18.0	17.4	-94.5	-91.6	2.9

Table 5.5 Comparison of phase noise for 4-stage and 5-stage distributed oscillators operating at the same frequency

Desired frequency GHz	Actual frequency GHz	Phase noise calculation dBc/Hz 1M offset	Phase noise simulation dBc/Hz 1M offset	Error calculation/ simulation dB
10.0 (N=4)	9.7 (N=4)	-98.7	-96.6	2.1
10.0 (N=5)	9.8 (N=5)	-99.0	-97.2	1.8

Table 5.4 and Table 5.5 list the calculated and simulated phase noise figures for the two cases mentioned above. The corresponding parameters used for calculating phase noise are to be found in Appendix D and HB simulation results in Appendix E.

The data in Table 5.4 show that as the frequency increases, the calculated phase noise worsens. The phase noise seen in the simulation follows the same pattern. The maximum error between the calculated and simulated results is 2.9 dB.

The data in Table 5.5 show that for two distributed oscillators operating at the same frequency, the calculated and simulated phase noise figures are almost alike. The maximum error between the calculated and simulated results is 2.1 dB.

5.5 Summary

The correctness and accuracy of theoretical predictions for distributed oscillator phase noise developed in chapter 4 are verified by HB simulation in ADS. On comparing the phase noise obtained from calculation based on the derived formulae and simulation, it is seen that both follow the same pattern and show acceptable errors. The maximum phase noise error between calculation and simulation results is about 2.9dB.

6.1 Summary

The literature review on the topic of distributed oscillators, new concept oscillators based on the broadband distributed amplifiers, has indicated that phase noise analysis of this oscillator is still lacking despite some other developments reported. Upon this situation, the purpose of this thesis was to develop a theoretical approach of predicting phase noise in distributed oscillators.

This thesis has presented a theoretical analysis of distributed amplifiers and oscillators. Their configurations, the principles of operation and the issues related to the circuit characteristics were addressed. This study provided the necessary knowledge for further work on phase noise analysis in distributed oscillators.

Phase noise analysis began with the description of a linear model for a generalized oscillator, noise shaping function of which was applied to the distributed oscillator under a linear assumption to account for additive phase noise. The mixing effects from circuit non-

linearity were then analyzed and included to obtain the final result. As a consequence, the closed-form formulae have been derived for predicting phase noise in distributed oscillators. Based on the derived formulae, the phase noise dependence on circuit parameters was also discussed to provide better understanding.

The verification of theoretical predictions on distributed oscillator phase noise was carried out by HB simulation. In this part, modeling of transmission line was a key issue. The CPS was chosen for the transmission line design, and its lumped π -type RLC network model was obtained by using Momentum and spice model generator. Five test cases, namely three 4-stage distributed oscillators operating at the three different frequencies and also two oscillators in 4-stage and 5-stage respectively operating at the same frequency, were examined by comparing their calculated and simulated phase noise. The results showed that both followed the same pattern and the maximum error is about 2.9dB.

Not only does this work provide a design guideline for engineers working in this field, but also it helps one develop a deeper understanding of distributed oscillator phase noise.

6.2 Future Work

The research work involved in this thesis as the first attempt has explored the analysis of distributed oscillator phase noise. Even though the theoretical predictions of phase noise have been confirmed by simulation, it would still be a good idea to confirm these results with actual physical measurements. In other words, measurements of actual silicon implementations of the five test cases should be carried out to further check the correctness and accuracy of theoretical work.

Besides phase noise, the tuning is another important topic in oscillator design. The development of new frequency control techniques, ones which will lead to wider tuning range, has always been desirable and welcomed.

Appendix A

Simplification of Eq. (3.26)

Eq. (3.26) can be rewritten as

$$\begin{aligned}
 V_{out} &= \sum_{n=1}^N V_{out,n} \\
 &= \sum_{n=1}^N -g_m \cdot \frac{Z_d}{2} \cdot V_{in} \cdot e^{-\gamma_g(n-1/2)l_g} \cdot e^{-\gamma_d(N-n+1/2)l_d} \\
 &= -g_m \cdot \frac{Z_d}{2} \cdot V_{in} \cdot e^{(\gamma_g l_g - \gamma_d l_d)/2} \cdot e^{-\gamma_d N l_d} \cdot \sum_{n=1}^N e^{(\gamma_d l_d - \gamma_g l_g)n}
 \end{aligned} \tag{A.1}$$

Let $A = \gamma_d l_d - \gamma_g l_g$ and $B = \gamma_d l_d + \gamma_g l_g$, Eq. (A.1) becomes

$$\begin{aligned}
 V_{out} &= -g_m \cdot \frac{Z_d}{2} \cdot V_{in} \cdot e^{-(A+B)N/2} \cdot e^{-A/2} \cdot \sum_{n=1}^N e^{nA} \\
 &= -g_m \cdot \frac{Z_d}{2} \cdot V_{in} \cdot e^{-(A+B)N/2} \cdot e^{-A/2} \cdot e^A \cdot \frac{1 - e^{NA}}{1 - e^A} \\
 &= -g_m \cdot \frac{Z_d}{2} \cdot V_{in} \cdot \frac{e^{A/2}}{1 - e^A} \cdot (e^{-(A+B)N/2} - e^{(A-B)N/2}) \\
 &= -g_m \cdot \frac{Z_d}{2} \cdot V_{in} \cdot \frac{e^{-(A+B)N/2} - e^{(A-B)N/2}}{e^{-A/2} - e^{A/2}} \cdot \frac{e^{-B/2}}{e^{-B/2}} \\
 &= -g_m \cdot \frac{Z_d}{2} \cdot V_{in} \cdot \frac{e^{-(A+B)N/2} - e^{(A-B)N/2}}{e^{-(A+B)/2} - e^{(A-B)/2}} \cdot e^{-B/2}
 \end{aligned} \tag{A.2}$$

Now substitute A and B back to Eq. (A.2)

$$\begin{aligned}
 V_{out} &= -g_m \cdot \frac{Z_d}{2} \cdot V_{in} \cdot e^{-(\gamma_d l_d + \gamma_g l_g)/2} \cdot \frac{e^{-\gamma_d N l_d} - e^{-\gamma_g N l_g}}{e^{-\gamma_d l_d} - e^{-\gamma_g l_g}} \\
 &= -g_m \cdot \frac{Z_d}{2} \cdot V_{in} \cdot \frac{e^{-\gamma_d N l_d} - e^{-\gamma_g N l_g}}{e^{(\gamma_g l_g - \gamma_d l_d)/2} - e^{(\gamma_d l_d - \gamma_g l_g)/2}}
 \end{aligned} \tag{A.3}$$

In Eq. (A.3), by applying Taylor extension to the term $e^{(\gamma_g l_g - \gamma_d l_d)/2} - e^{(\gamma_d l_d - \gamma_g l_g)/2}$ in denominator, it becomes

$$e^{(\gamma_g l_g - \gamma_d l_d)/2} - e^{(\gamma_d l_d - \gamma_g l_g)/2} = \gamma_g l_g - \gamma_d l_d \tag{A.4}$$

Substituting Eq. (A.4) into Eq. (A.3) turns out

$$V_{out} = -g_m \cdot \frac{Z_d}{2} \cdot V_{in} \cdot \frac{e^{-\gamma_d N l_d} - e^{-\gamma_g N l_g}}{\gamma_g l_g - \gamma_d l_d} \tag{A.5}$$

Appendix B

TSMC 0.13 μm CMOS Interconnect Stack Simplification

There are a number of layers in 0.13 μm CMOS interconnects. When transmission line embedded in interconnect stack is modeled to extract its equivalent circuit by simulation, it is not necessary to define each layer of interconnects. For the purpose of saving the simulation time, the layers can be simplified by the following way.

Fig. B.1 Illustration of interconnect stack simplification

Fig. B.1 illustrates the simplification of two layers into one layer. In Fig. B.1(a) d_1 , d_2 , ϵ_1 , and ϵ_2 represent the thicknesses and dielectric constants of two layers. A is horizontal area of dielectric. C_1 and C_2 are parasitic capacitances from two dielectric layers, respectively. Their values can be calculated by

$$C_1 = \frac{\epsilon_1 A}{d_1} \quad (B.1)$$

$$C_2 = \frac{\epsilon_2 A}{d_2} \quad (B.2)$$

Fig. B.1(b) is the equivalence of Fig. B.1(a), dielectric thickness $d = d_1 + d_2$, ϵ_e is equivalent dielectric constant of ϵ_1 and ϵ_2 , and C_e is equivalent parasitic capacitance of parallel C_1 and C_2 . C_e can be calculated by

$$C_e = \frac{\epsilon_e A}{d} \quad (B.3)$$

It is true that

$$C_e = C_1 \parallel C_2 = \frac{C_1 C_2}{C_1 + C_2} \quad (B.4)$$

Substituting Eqs. (B.1), (B.2), and (B.3) into Eq. (B.4) results in an expression for

ϵ_e

$$\epsilon_e = \frac{\epsilon_1 \epsilon_2 d}{\epsilon_1 d_2 + \epsilon_2 d_1} = \frac{\epsilon_1 \epsilon_2 (d_1 + d_2)}{\epsilon_1 d_2 + \epsilon_2 d_1} \quad (B.5)$$

Appendix C

Simulation Setups in Momentum

The following setups need to be specified before a Momentum simulation of a CPS gets started.

1. CPS with the Finite Thickness

Since it is assumed that conductors are infinite thin metal sheets in Momentum, a little trick involving vias is required to layout CPS with the finite thickness. First, the line is drawn as a rectangle on the layer 'cond', the rectangle is then copied to the layers 'cond2' and 'hole'. Meantime, the cooperation of interconnect definition is needed to complete the CPS with the finite thickness.

2. Interconnect Definition

The interconnect definition is made up of the definition of substrate layers and metallization layers.

Substrate layer definition is as follows: define each layer's dielectric constant and thickness. Fig. C.1 gives the parameters for a simplified stack.

For the metallization layer definition, especially for the line with the finite thickness, the metallization layer needs to be mapped to the interconnect stack as shown in Fig.

C.2 where the two sheets of metal (cond and cond2) with via (hole) connecting together, and the height of the via is defined by the height of the $d_3 = 0.9\mu m$.

Free space	
$\epsilon_4 = 5.7$	$d_4 = 0.88\mu m$
$\epsilon_3 = 4.2$	$d_3 = 0.9\mu m$
$\epsilon_2 = 3.2$	$d_2 = 6.2\mu m$
$\epsilon_1 = 11.9$	$d_1 = 675\mu m$
Ground	

Fig. C.1 Substrate layer definition

Free space		
$\epsilon_4 = 5.7$	$d_4 = 0.88\mu m$	Strip: cond2 Cond=5.8e7
$\epsilon_3 = 4.2$	$d_3 = 0.9\mu m$	Via: hole Cond=5.8e7
$\epsilon_2 = 3.2$	$d_2 = 6.2\mu m$	Strip: cond Cond=5.8e7
$\epsilon_1 = 11.9$	$d_1 = 675\mu m$	
Ground		

Fig. C.2 Illustration for thick metallization layer mapping

Note that the conductivity of the conductor and via is set by Sigma (Re, Im) in terms of bulk conductivity as a complex number. Here enter 5.8e7 for the real part and 0 for the imaginary part respectively.

3. Ports

Ports can inject energy into a circuit and they are necessary in order to analyze the behavior of transmission lines. When the ports are applied to the transmission lines, their properties need to be assigned.

Fig. C.3 shows assigned ports for CPS.

Fig. C.3 Port properties for CPS

4. Mesh

A mesh is a pattern of rectangles and triangles that is applied to a design in order to break down the design into small cells. The mesh computes the current within each cell and identifies any coupling effects in the circuit during simulation. From these calculations, S-parameters are then calculated for the circuit.

A mesh is required for simulation. Creating a mesh consists of two parts: defining mesh parameters and precomputing the mesh. It is not necessary to set up mesh parameters. Default parameters will be used instead. Precomputing the mesh is done before simulation in order to view the mesh. Otherwise, the mesh can be computed as part of the simulation process.

Appendix D

Parameters for Calculating Phase Noise

Table D.1 Parameters for a 14GHz 4-stage distributed oscillator phase noise calculation

Parameter	Value	Parameter	Value
f_0	14GHz	R_{in}	7 Ω
Δf	1MHz	C_{in}	137fF
Z_0	50 Ω	$g_{ds}(1/R_{ds})$	4.32mS
g_m	41.43mS	I_{bias}	3.67mA

Table D.2 Parameters for a 18GHz 4-stage distributed oscillator phase noise calculation

Parameter	Value	Parameter	Value
f_0	18GHz	R_{in}	7 Ω
Δf	1MHz	C_{in}	106fF
Z_0	50 Ω	$g_{ds}(1/R_{ds})$	3.79mS
g_m	35.81mS	I_{bias}	3.60mA

Table D.3 Parameters for a 10GHz 5-stage distributed oscillator phase noise calculation

Parameter	Value	Parameter	Value
f_0	10GHz	R_{in}	7 Ω
Δf	1MHz	C_{in}	151fF
Z_0	50 Ω	$g_{ds}(1/R_{ds})$	4.16mS
g_m	40.52mS	I_{bias}	3.20mA

Appendix E

HB Simulation Results

Fig. E.1 HB simulation results for a 14GHz 4-stage distributed oscillator with CPSs

Fig. E.2 HB simulation results for a 18GHz 4-stage distributed oscillator with CPSs

Fig. E.3 HB simulation results for a 10GHz 5-stage distributed oscillator with CPSs

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