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**A COMPARISON OF IMPLEMENTATION ASPECTS IN OVERSAMPLED
ANALOG TO DIGITAL CONVERTERS
FOR USE IN ISDN SUBSCRIBER LOOPS**

by

THOMAS A. D. RILEY, B.E.Sc

**A thesis submitted to the
Faculty of Graduate Studies and Research
in partial fulfilment of the requirements
for the degree of
Master of Engineering**

**Ottawa-Carleton Institute for Electrical Engineering
Department of Electronics
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April, 1989**

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The undersigned recommend to the faculty of Graduate Studies
and Research the acceptance of the thesis:

"A Comparison of Implementationk Aspects in
Oversampled Analog to Digital Converters for Use in
ISDN Subscriber Loops"

submitted by Thomas Riley in partial fullfillment of the
requirements for the degree of Master of Engineering.

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ABSTRACT

This thesis considers the use of an oversampled ADC in a U-interface device for the ISDN. It describes some fundamental limits on the performance of the oversampled ADC. The limits considered are noise in the analog circuitry, the effects of non-ideal Opamps and quantization noise. The thesis describes methods to simulate these limits and explores the design compromises available to select oversampled ADC structures and gain coefficients in these structures that reduce the impact of the limits using any given technology. In the course of this exploration, new structures are introduced that are shown to allow improved oversampled ADC performance.

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List of Symbols

ADC	Analog to Digital Converter
ANSI	American National Standards Institute
C, C1, C2, C3	capacitors values used in a circuit analysis
C_{fb}	feedback capacitor from opamp output to opamp input in a switched capacitor integrator
C_{ffi}	feed forward (sampling) capacitor in a switched capacitor integrator
D_i	decimation filter gain for an FFT bin used in coder output analysis
DAC	Digital to Analog Converter
FFC	a parameter for modeling of non-ideal integrators which describes the instantaneous clock and signal feed through at the time TACT
FFT	Fast Fourier Transform
E	error signal in a block diagram

f_s	the sampling frequency in a switched capacitor implementation of a coder
G1, G2, G3, G4	the gains of the first second third and fourth integration stage of a coder respectively in a coder block diagram
H1, H2, H3, H4	block diagram gains for an ideal switched capacitor integrator
IIR	an Infinite Impulse Response filter
ISDN	Integrated Services Digital Network
K	quantizer gain used in linearized analysis of a coder structure
MRT	the minimum resolvable time in any given SPLICE simulation
NBW	the number of bins included in the 80kHz bandwidth of an FFT coder output analysis
NFREQ	the bin where the input sinusoid appears in an FFT coder output analysis
P_q	quantization noise power of an FFT bin in coder output analysis

Q	quantization noise
SNR	ratio of signal power to noise power over a specified band width
SNR _a	a signal to noise ratio of a coder where the signal power is the square of the rms value of a sinusoid and the noise power is the noise produce by opamps and KT/C noise in the bandwidth from 20kHz to 60kHz
SNR _p	a signal to noise ratio of a coder where the signal power is the square of the rms value of a sinusoid and the noise power is the quantization noise produced by the coder in an 80kHz bandwidth
SRM	a parameter for modeling of non-ideal the integrators describing the slew rate in the negative direction
SRP	a parameter for modeling of non-ideal the integrators describing the slew rate in the positive direction

T	sampling period of the switched capacitor clock
TACT	the beginning of the settling phase of a switched capacitor integrator
TPER	the end of the settling phase of a switched capacitor integrator
Tx	the transmit side of a transeiver
V0, V1, V2, V3, V4	the system reference voltages of the first second third and fourth integration stages of a coder respectively
VB1, VB2, VB3, VB4	appropriate bias voltages for opamps
V _i	a the value of an FFT bin resulting from a FFT coder output analysis
Vn1	the KT/C noise of a switched capacitor integrator that occurs in the band width from 20kHz to 60kHz once aliasing of broad band noise has been taken into account

V_{n2}	the input referred noise of an opamp that occurs in the band width from 20kHz to 60kHz once aliasing of broad band noise has been taken into account
$V_{o1}, V_{o2}, V_{o3}, V_{o4}$	the output voltages of the first second third and fourth integration stages of a coder respectively
V_r	the physical reference voltage used in the switched capacitor implementation of a coder
X	input signal in a block diagram
Y	output signal in a block diagram
Y_1, Y_2	one of two possible output signals in a block diagram
z	the delay operator
α_{nn1}	a ratio to refer V_{n1} to the coder input
α_{nn2}	a ratio to refer V_{n2} to the coder input
$\Delta V_{o1}, \Delta V_{o2}, \Delta V_{o3}$	the per cycle change in integrator output voltage recorded during a coder simulation

$\phi 1$ the sampling phase of a switched
capacitor integrator

$\phi 2$ the acting phase of a switched
capacitor integrator

Chapter 1

Introduction

1.1 Research Goals

The primary research goal of this thesis is to explore the fundamental limits on the performance of the oversampled ADC when used as an input analog to digital converter in an ISDN U-interface context. The limiting factors considered are the noise in the analog circuitry, the effects of non-ideal opamps and the quantization noise of the oversampled ADC.

The secondary goals set with the intent to meet the primary goal are:

- i) to find new or existing structures of oversampled ADC's that are insensitive to the factors that traditionally limit the performance of an oversampled ADC and, by virtue of this insensitivity, achieve better performance, and
- ii) to find methods of analysis or simulation that can evaluate the sensitivity of various oversampled ADC structures.

1.2 Thesis Organization

Chapter 2 provides the context in which the oversampled ADC (coder) must operate for use in the U-interface. Particular details of the U-interface implementation for which the coder is intended affect the coder design. These details are discussed in terms of the constraints and the opportunities for innovation that they create. Chapter 2 is a necessary step toward the research goals in that it limits the scope of the possible coder structures investigated, allowing more in depth analysis of the remaining structures.

Chapter 3 provides an introduction to oversampled analog to digital conversion and selected analysis methods from the literature that are used in the analysis of quantization noise. These concepts are necessary background to understand the oversampled ADC in principle before introducing the second order effects of non-ideal circuit elements. Chapter 3 also establishes a common nomenclature and system level representation of the oversampled ADC so that structures from diverse sources can be compared.

Chapter 4 introduces coder structures and tuning strategies proposed for evaluation with justification for their selection. Some of the structures introduced are from the

literature. Other new structures are introduced and compared to existing structures. Each structure and tuning strategy is examined for its potential to meet performance goals set in chapter 2. Structures that show little potential are not considered further.

Chapter 5 provides the coarse evaluation of the coder structures. This evaluation involves simulation and analysis of the sensitivities of various structures to analog sources of noise and quantization noise. This provides enough information to rule out further consideration of some previously selected coder structures.

Chapter 6 presents simulation methods with increased accuracy intended to include some effects present in integrated circuit implementation but omitted in the simulations of chapter 5. This simulation method is verified and then used to continue the evaluation of chapter 5 in more detail while taking these non-ideal effects into account.

Finally, chapter 7 summarizes the findings of the thesis with respect to the research goals set out in chapter 1. Options to pursue these goals further are also presented.

Chapter 2

Problem Definition

2.1 General

In recent years there has been growing interest in the telecommunications industry about the introduction of the ISDN (Integrated Services Digital Network) that allows data and digitized voice to be transmitted over the existing, installed base of twisted pair copper wiring. To allow these features to be provided in standard products from multiple vendors, an ANSI standard has been developed^[1] specifying the requirements for compatible network interface circuits. The specification requirement to use echo cancellation has a significant impact on the requirements for the ADC.

When an echo cancellation technique is used both the far end received signal and the reflection of the transmitted signal will appear at the input to a line termination device simultaneously. The echo must then be subtracted from the total signal. Since the echo can have a much larger amplitude (up to 40dB) than the far end signal, this requires a high precision, low noise subtraction and a precise, accurate prediction of the echo. To accomplish this, echo prediction is typically calculated digitally, and

the subtraction is made in the digital domain. This demands a similarly precise and linear ADC. This chapter is devoted to defining the requirements of such an ADC in this environment.

2.2 The Target Environment

Figure 2.1 summarizes the environment in which the ADC is targeted to operate. The analog hybrid is located off chip, allowing the use of low-noise high-precision passive components. The complete analog to digital conversion process consists of a sigma delta modulator or coder and a decimation filter. The decimation filter, echo cancellation, DAC, transmit filter and detection are all implemented in one CMOS integrated circuit. Although other alternatives to this architecture are considered in this thesis, the availability of components to perform the on chip functions of this architecture has a significant impact on the immediate utility of any coder structure considered. Consequently, a discussion of the decimation filter and its impact on the coder is in order.

Figure 2.1
Environment Related to the ADC

2.3 The Decimation filter

The decimation filter desired for this application is typically a FIR filter with one zero at dc to provide linear equalization and the rest of the zeros at frequencies above 80kHz. The high frequency zeros combine to provide attenuation up to 110dB to remove signal components above 40kHz so that the output can be resampled (decimated) at 80kHz. A piecewise linear approximation of a typical envelope (i.e. high frequency zeros not included) of the desired decimation filter frequency response is shown in Figure 2.2. To be compatible with the implementation of the decimation filter in the target environment, the input to

the decimation filter is required to be one bit at 10.24 MHz (see Figure 2.1). This constrains the sampling frequency and number of output levels for the coder.

Figure 2.2
Typical Frequency Response Envelope

2.4 2B1Q Line Code

Since many characteristics of the 2B1Q line code (signal) simultaneously being transmitted and coming into the coder

(ADC) are known, some discussion of these is also in order so that possibilities of optimizing the coder to these characteristics can be explored.

The 2B1Q line code requires detection of a 4 level symbol at 80,000 symbols per second. Thus, the coder must have a bandwidth of at least 40 kHz to accommodate baud rate sampling. However, in order to avoid problems from noise aliased back into the base band, frequency components above 40kHz must be severely attenuated. Since the decimation filter cannot be ideal, some attenuation is tolerated between 40kHz and 80kHz. This is discussed more thoroughly in chapter 3.

Since the input signal is a 2 bit code consisting of only 4 predefined symbols, it is desirable to have some gain control in the hybrid so that the rms signal levels representing these symbols are near an optimal level at the input to the oversampled ADC so that the signal to noise ratio of the ADC is high but the ADC is not saturated.

Another feature that is unique to this application is that the combined near and far end signal level at the coder input varies over a range of only 10 dB due to the high level of the echo present. As the input signal level varies

over this 10 dB range, the required^[2] quantization noise and non-linear error, or harmonics, range from -35 dB at maximum input signal level (in the case of a short line) to -75 dB at the minimum input signal level (in the case of a long line). Consequently, SNR at maximum input signal level alone is not really an appropriate figure of merit in this application. The significance of this feature is that it is acceptable to have some degradation of coder performance as the signal level increases approaching saturation. It is discussed further in chapter 6 in the context of examining the performance of specific coders.

Chapter 3

Oversampled ADC Background

3.1 Principles of Operation

The principles of operation of oversampled ADC's are well presented by Tewksbury and Hallock[3]. As with any type of ADC quantization noise is unavoidably introduced. The critical feature of oversampled ADC's is that the oversampling allows a reduction of the quantization noise without increasing the complexity (i.e. number of bits) of the ADC.

The two techniques, relevant to this thesis, used to minimize the effects of this quantization noise are commonly categorized[3] as follows:

i) Noise Shaping Coders

As illustrated in Figure 3.1, some intuitive feeling can be obtained for the noise shaping coder by observing that the error(E) between the input signal(X) and the fed-back output signal(Y) is integrated N times for an N -th order coder. Thus, there is a large "gain" at low frequencies between the error voltage, E , and the coder output, Y . This assures that the fed-back

signal keeps the low frequency components of the error small and hence moves the quantization noise to higher frequencies. Typically this noise can then be removed by low pass filtering in the decimation filter block.

ii) Predictive Coders

Figure 3.2 Shows a typical N-th order predictive coder. Here the quantization noise is added to the prediction error signal(E). Hence, the quantization noise introduced is added only to the prediction error. As the order of the coder is increased both the prediction error and its associated quantization noise are reduced compared to the input signal.

It has been shown[3] that equivalent noise shaping functions can be achieved using either of these techniques. In practice, the choice of an appropriate combination of noise shaping and predictive coding depends on the sensitivity of a particular structure to various second order effects which result from non-ideal circuit elements. New approaches to both of these techniques, and combinations thereof, that take into account these second order effects are discussed extensively in this thesis.

Figure 3.1
Ritchie Structure Noise Shaping Coder

The large gain between the error voltage E and the output Y reduces the error in closed loop operation

Figure 3.2
Integrating Predictive Coder

Since only the error voltage E is quantized and E is small compared to the input signal, the quantization error in E is also small compared to the input signal

3.2 Analytical Techniques for Oversampled ADC's

3.2.1 Linear Analysis in the z Domain

By making appropriate assumptions, many phenomena of oversampled ADC's can be adequately predicted with standard linear signal processing techniques.[3][4][5] To make this simplification, the quantizer shown in Figure 3.3 must be modeled as shown in Figure 3.4 with the assumptions that the quantization noise is:

- i) additive to the signal being quantized,
- ii) uncorrelated to the input signal , and
- iii) uniformly distributed over the quantization interval.

Given these assumptions about the quantization noise, the design process can be simplified to one of designing a filter to minimize either:

- i) the in-band quantization noise for noise shaping coders, or
- ii) the prediction error for predictive coders.

Candy[4][5] and Tewksbury[3] provide excellent examples of how this type of analysis can be performed. The analysis for

a first order noise shaping coder is repeated here to establish a common nomenclature used throughout this thesis. As illustrated in Figures 3.3 and 3.4, the nomenclature introduced for use in this thesis is:

Y is the output signal. It is interpreted (mathematically) by the decimation filter as a dimensionless number usually either a +1 or a -1 for single bit quantizers.

V_{01} is the output voltage of the first (or only) integrator.

V_1 is the change in V_{01} produced by the switch control, the reference voltage and the integration constant of the integrator. For example, in Figure 3.5 V_1 is $V_r(C_2/C_{fb})$ and thus has units of Volts.

G_1 is simply the (dimensionless) integration constant of the integrator, C_1/C_{fb} in this example.

X is the input voltage.

K is the quantizer gain having units of Volts^{-1} . It is indeterminate for a one bit quantizer.

Similarly, for higher order coders, the values V_2 , G_2 , Vo_2 , V_3 , G_3 and Vo_3 would correspond to the second and third stages respectively.

Figure 3.3
First Order Noise Shaping Coder

Figure 3.4
A Simple Model for the Quantizer

The quantizer has an indeterminate gain K . Since it depends only on the sign and not the magnitude its input signal V_{o1} , an approximation of its linearized gain would approach infinity as the magnitude of V_{o1} is reduced.

Figure 3.5
A Typical Integration Stage

Solving for Y in Figure 3.4 gives:

$$Y = \frac{K \cdot G1 \cdot X + (1 - z^{-1})Q}{K \cdot V1 + (1 - z^{-1})} \quad (3.1)$$

Substituting

$$z^{-1} = e^{-j\omega T} \quad (3.2)$$

where T is the sampling period, gives the normalized frequency response which can in turn be integrated over the desired bandwidth to obtain the noise power and hence the SNR for a given input sinusoid.

Unfortunately, if the coder contains a single bit quantizer, this simple linear model fails in several ways:

- i) With a single bit quantizer, the output for each clock cycle can be interpreted as a +1 or a -1 for any amplitude of input to the quantizer depending only on the sign of the input to the quantizer. Consequently, any approach to determine a linearized gain for the quantizer requires an estimate of the probability density function of the signal at the quantizer input.

Without a known quantizer gain, the signal levels cannot be determined and hence it is not possible to determine whether or not the integrators will saturate.

- ii) As the amplitude of the input signal is increased beyond a certain point, which depends on the integrator gains and in some cases the integrator saturation levels, the quantization noise starts to grow more rapidly than the signal and the SNR drops off rapidly.

Work by Gray^[5] provides an exact solution for some of these cases where the linear model fails. However, it suffers from some problems in that it requires a complicated analysis which may or may not be soluble for each different configuration considered. To date a solution has been found^[5] for only a first order coder with dc inputs.

Some work done at the University of North Carolina ^[6] explains these cases where the linear model fails. The approach taken there is to develop two linearized gains as a function of the input signal level, one gain for the quantization noise and one gain for the signal. However, the model presented is weak in several areas:

- i) It applies only to sinusoidal input signals.

- ii) As in the work by Gray, it requires a complicated analysis which may or may not be soluble for each different configuration considered.
- iii) It requires the assumption that the probability distribution of the integrated quantization noise at the quantizer input is Gaussian, which may not be valid.

Because of these difficulties with analytical techniques, the most practical approach to studying a wide variety of coder structures, at the present time, is to perform simulations in the time domain.

3.2.2 Simulations in the Time Domain

Because of the difficulties associated with an indeterminate quantizer gain for single bit quantizers, it is more convenient to simulate the coder using a high level language to create a dedicated simulator, or to use a general purpose simulator such as SPLICE 1.7[8] with user defined models to represent the integrators. Such a simulator can be used to generate a stream of +1's and -1's resulting from a given input. This can also be used to detect signal levels in the integrators to predict whether or not they will saturate.

By simulating a sine wave, applied to the input of the coder, an output bit stream will be generated that will include the original sine wave plus quantization noise. Taking the FFT of this stream will provide an estimate of the power spectral density of the combined sine wave and quantization noise. The total power of the quantization noise is then given by:

$$P_q = \sum_i (D_i \cdot |V_i|)^2 \quad (3.3)$$

where

$$i = 1 \dots \frac{N}{2}, \quad i \neq NFREQ$$

D_i is the gain of the decimation filter for each component of the FFT

$|V_i|$ is the magnitude of each component of the FFT

N is the number of points in the FFT, and

$NFREQ$ is the frequency component of the FFT containing the input sine wave.

Figure 3.6 shows the combined effect of the decimation filter and the noise shaping for a second and third order

coder. Clearly, summing noise components over a bandwidth of 80kHz provides a slightly conservative but simplified estimate of the sum in (2) above as:

$$P_q = \sum_i |V_i|^2 \quad (3.4)$$

where:

$$i = 1 \dots NBW, \quad i \neq NFREQ$$

V_i is each component of the FFT

NBW is the number of frequency components of the FFT in the 80kHz bandwidth, and

NFREQ is the frequency component of the FFT containing the input sine wave.

Estimates using a piecewise linear estimation of the decimation filter envelope shown in Figure 3.6 indicate that the estimate of an 80kHz bandwidth is conservative by only about 4dB for a second order coder and in error by a negligible amount for a third order coder. Figure 3.6 shows the combined noise shaping effect of both coder and

decimation filter. To allow comparison of the three cases considered on the same graph, all the curves are normalized to 0dB at 40kHz.

To avoid problems with spectral smearing^[9] of the input sine wave, it is desirable to select the period of the input sine wave to be an integral multiple of the sampling period.

Figure 3.6
Effect of the Decimation filter

3.3 Other Sources of Noise

In addition to quantization noise there are also fundamental limits on noise performance imposed by thermal noise and $1/f$ noise in the opamp's and switches. Referring back to Figure 3.5, it can be seen that during ϕ_1 , a noise charge is added to the signal charge sampled in the sampling capacitor(s) due to KT/C noise. Also during ϕ_1 , a noise voltage is added to the previous output of the opamp due to the opamp noise. During ϕ_2 , the output voltage of the opamp has an added noise voltage due to the opamp noise the KT/C noise of the switched capacitor resistors. The goal of this section is to find an expression to approximate the effect of these noise sources referred to the input of the coder.

The following considerations are taken into account in the development of the approximations in Appendix 1.

- i) Coefficients relating the structure dependent requirements of a given coder are separated from the technology dependent noise source magnitudes of the circuit elements used to implement the coder. These coefficients can be factored out of the traditional noise analysis.

These structure dependent coefficients can then be used as technology independent figures of merit for comparing different coder structures.

- ii) Factors produced by repeatedly used circuit elements, such as switched capacitor resistors are separated into the structure dependent coefficients, including the number of times that circuit element is repeated, leaving a technology dependent noise magnitude depending only on the characteristics of the circuit element.
- iii) The structure dependent coefficients refer the noise magnitudes to the input of the coder for comparison with the input signal level.

The fundamental limits, produced by switch and opamp noise and referred to the coder input, are discussed in more detail in Appendix 1. The material presented there applies to the input stage of a general sigma delta coder. It meets the above considerations by evaluating the following technology dependent noise magnitudes:

V_{n1} the in-band KT/C noise of the input signal sampling capacitor, and

V_{n2} the in-band thermal and 1/f noise of the opamp used to implement the integrator.

The signal to noise ratio for the analog sources of noise can then be estimated using:

$$SNR_a = 10 \text{Log} \left(\frac{X^2}{(\alpha_{nn1} \cdot V_{n1})^2 + (\alpha_{nn2} \cdot V_{n2})^2} \right) \quad (3.5)$$

where X is the rms input voltage, and each α represents a factor to refer all instances of the corresponding noise magnitudes back to the input of the coder.

This simple formula can be used to refer the input noise of circuit elements of any switched capacitor integrator to the integrator input. For the coders considered in this thesis, the noise shaping action of each stage of the coder causes the first stage to be the dominant noise source in the circuit.

Chapter 4

Structures for Use in the Target Environment

4.1 Introduction

Many attempts have been made to find ways to improve the performance of oversampled ADC's. Representative approaches from the literature are presented here to establish a common nomenclature and introduce ideas referred to extensively or developed further in this thesis.

This chapter also introduces new coder structures proposed for further analysis. The operation of each coder structure is explained along with the potential improvements they may be able to achieve.

The objective of this chapter is to establish which of the known or new structures are suitable for use in the target environment defined in Chapter 2.

4.2 Ritchie Structure with Delaying Integrators

This type of structure has been well studied with the principal difficulty being the determination of appropriate coefficients to provide optimal performance, and stability for second and higher order coders. Two approaches to the

problem of maximizing SNR while maintaining stability and non-saturating integrator signal levels are presented in the literature.[3][10]

Figure 4.1 and Table 4.1 show the coefficients resulting from one approach to tuning a Ritchie structure of order 1 to 4 denoted SDD1 to SDD4 respectively. SDDN is an abbreviation of Sigma Delta, Delaying Integrators, Order. These coefficients were obtained[3] in the frequency domain by moving all poles of the denominator of the linear transfer function to as high a frequency as possible. They do not take into account the effects of saturation or the possibility that the quantizer gain may not be equal to 1, however, and consequently had to be modified to less than optimal values to work in the bread board.

Table 4.2 shows the coefficients for a third order Ritchie structure, shown in Figure 4.2, optimized by, another approach, repetitive search type simulations in the time domain[10]. In this case the Ritchie structure was simulated to include clipping at each integrator. The approach to find optimal coefficients in this case is then an optimization problem with each trial of the coefficients requiring one time domain simulation of the structure.

Figure 4.2
Sigma Delta Modulator with Delaying Integrators, Third Order, SDD3

Table 4.2
Coefficients for SDD3

Coefficient	Value
G1	0.10
G2	0.40
G3	0.80
V1	0.625
V2	0.60
V3	1.75

4.3 Ritchie Structure with Non-Delaying Integrators

Figure 4.3 shows an alternative version of the traditional Ritchie structure using non-delaying integrators. The non-delaying switched-capacitor integrators can be implemented by reversing the clock phases of the two switches on the input side of C_1 in the integration stage shown in Figure 3.5. This results in an inverting switched capacitor integrator with no delay in the feedforward path. There remains a delay, however, in the path fed back from the quantizer and in the original input stage. Rather than representing all these delays individually, they are manipulated using block diagram techniques to a single delay at the quantizer input. The second order version of this structure has been extensively studied by Candy[4] using a similar block diagram representation. Within this thesis, this structure is denoted SDND2.

It is anticipated that the signal levels in the integrators can be reduced using non-delaying integrators by providing feedback to each integrator with less delay. This can be seen by noting that there are 2 delays from the first

integrator to the quantizer and back in the structure of Figure 4.1 but only one in the Ritchie structure with non-delaying integrators.

Given the coder structure of Figure 4.3, it is desirable to investigate the possibility of extending this structure to a third order coder with non-delaying integrators (SDND3) as shown in Figure 4.4. Since the number of delays in the loop can be reduced from 3 to 1 in a third order coder, it is anticipated that any improvement, compared to a coder with delaying integrators, will be more noticeable in a third order coder than in a second order coder where the number of delays can be reduced only from 2 to 1. The linearized transfer function of this coder structure is:

$$Y = \frac{K \cdot G1 \cdot G2 \cdot G3 \cdot X + (1 - z^{-1})^3 Q}{K \cdot z^{-1} \cdot (V1 \cdot G2 \cdot G3 + V2 \cdot G3 \cdot (1 - z^{-1}) + V3 \cdot (1 - z^{-1})^2) + (1 - z^{-1})^3} \quad (4.1)$$

Selection of appropriate coefficients for this structure has not been widely studied in third or higher order structures. The possibility for improved performance using a non-delaying third order structure is investigated in this thesis.

The process of tuning the third order version of this structure is started in the frequency domain by selecting coefficients to move the poles of the denominator of the

linear transfer function to high frequencies while maintaining roots of this denominator within the unit circle of the z plane. This portion of the tuning strategy is taken from [11]. Other portions of the tuning strategy are new as discussed below.

The first new portion of the tuning strategy for this third order coder structure results from the discussion of signal level scaling (see section 4.7) From signal level scaling, it can be assumed that a third order coder structure will have only two degrees of freedom to try to optimize the noise shaping function while maintaining stability. If the process is started by assuming that $V_1=V_2=V_3$, and that G_1 is a scaling factor for the input signal, then we are left with a two dimensional search for an optimal stable tuning as a function of G_2 and G_3 . As with previous attempts, this search can be pursued initially in the frequency domain and finally in the time domain or strictly in the time domain. Unlike previous attempts, the tuning of a third order coder can now be considered a two dimensional search rather than a three dimensional search. Consequently, assessing the effects of integrator saturation can be deferred until after the optimal frequency response is found.

The second new portion of the tuning strategy suggests an efficient means of determining stability for a wide range of input signal levels. Rather than attempting to find a linearized gain as a function of input signal level, one attempts to show that the coder is stable for a wide range of quantizer gain and hence a wide range of signal levels at the quantizer input. Since computation of the roots of a third order polynomial can be quite efficient, stability can be efficiently assessed in the frequency domain without making any assumptions about the quantizer gain. Since false assumptions about the magnitude of the quantizer gain could indicate that regions of the search space for optimal values of G_2 and G_3 are unstable when in fact they are stable, this new approach allows a more complete search in the frequency domain before going to the time domain simulations.

It should be noted that although this systematic tuning strategy has been identified here, it has not been carried out for a third order coder. After a conventional and incomplete search, $G_2=0.33$ and $G_3=0.6$ are selected as values that provide sufficient stability and performance to allow further evaluation of the coder structure. With these

values, a few points calculated in the root locus as a function of K indicate that the output Y is stable provided that $0.15 < KV_1 < 1.5$.

Figure 4.3
Sigma Delta Modulator with Non-Delaying Integrators, Second Order
SDND2

Figure 4.4
Sigma Delta Modulator with Non-Delaying Integrators, Third Order,
SDND3

4.4 Digital Integrating Predictor

A structure as proposed by Yukawa[12][13], and denoted SD2DIP in this thesis, is shown in Figure 4.5. By placing the DAC (V_0) of the classical predictive coder after the integrator rather than before the integrator (see also Figure 3.2), the integrating function can be implemented digitally. Either a digital or analog integrating predictor can be used to reduce the total change in integrator output voltage for each clock cycle. The resulting reduction in the integrator output voltage swing reduces the slew rate requirements on the opamp used to implement the analog integrator. (See Figure 4.5.) By performing the integration digitally with an up/down counter, the integration can be performed without dc offset and with infinite gain at dc.

Another extension of SDND2 and the digital integrating predictor proposed by Yukawa[12][13] is to produce a third order coder with a digital integrating predictor of the input signal and second order noise shaping. A corresponding block diagram for SD3DIP is shown in Figure 4.6.

One problem that must be faced with either SD2DIP or SD3DIP is that the input stage opamp sees a large load in the capacitors implementing the DAC of the predictor. This

results from the large capacitor ratios required to implement the DAC. Consequently, in tuning SD3DIP, the criteria chosen is the minimization of the number of bits in the digital logic used to implement the integrating predictor. Since there is no adequate, general purpose means of predicting signal levels, the minimization is achieved by repeated time domain simulation as in reference 14.

If the single bit output is used as shown in Figure 4.6, then the linear transfer function that results is:

$$Y = \frac{K \cdot G1 \cdot G2 (1 - z^{-1})^1 X + (1 - z^{-1})^3 Q}{K \cdot z^{-1} (V0 \cdot G2 + V1 \cdot G2 \cdot (1 - z^{-1}) + V2 \cdot (1 - z^{-1})^2) + (1 - z^{-1})^3} \quad (4.2)$$

which has a zero in the response to X at $\omega = 0$. This can be used with the existing or similar decimation filter structure and a different impulse/frequency response to simplify the decimation filter by removing the required first order differentiating function at frequencies below 30kHz that is indicated in Figure 2.2.

As can be seen in Figures 4.5 and 4.6, the digital predictor (Y2) can be used directly as the coder output rather than the single bit output (Y1). If Y2 is taken to be the coder output, a multi-bit representation of the input signal is available to reduce the power spectral density of the

quantization noise of the coder. Since the quantization noise reduction results from the increased number of levels in the DAC, the magnitude of the reduction in quantization noise power is proportional to the square of the number of signal levels that the predictor can provide through the DAC. This reduction is "white" rather than noise shaped in that it occurs evenly over the frequency band from dc to the sampling frequency. This noise reduction can then ease the attenuation requirements of the decimation filter. However, the increased number of bits at the input to the decimation filter complicate its structure.

Using the multi-bit output has a characteristic that is disadvantageous in the target environment. The characteristic is that one order of the noise shaping function is lost resulting in only a second order noise shaping function for a third order coder. Consequently, white reduction in quantization noise produced by using the multi-bit predictor as the output has to be compared to the loss of an order of the noise shaping function when deciding which output to use. Simulations performed as in Chapter 5 show that with a sampling frequency of 10.24MHz and a bandwidth of 80kHz, the loss of an order of noise shaping is more significant than the white reduction in quantization noise. However, use of

the predictor as the coder output is not necessarily disadvantageous if the ratio of sampling frequency to bandwidth is lower or when the number of bits in the predictor is higher.

The use of the predictor output, Y_2 , as a multi-bit representation of the input signal has some interesting potential for other applications. However, for the reasons discussed above, it is not suitable for this application. Therefore, use of the predictor as the coder output will not be considered further in this thesis and all further analysis concerns the single bit output, Y_1 .

Figure 4.5
Second Order Digital Integrating Predictor
SD2DIP

Table 4.3
Coefficients for SD2DIP

Coefficient	Value
G1	1.000
V0	0.225
V1	0.225

Figure 4.6
Third Order Digital Integrating Predictor, SD3DIP

Table 4.4
Coefficients for SD3DIP

Coefficient	Value
G1	1.000
V0	0.1125
V1	0.225
V2	0.225

4.5 Zeros in the Base Band of the Noise Shaping Function

Reported work with bread boarded circuits[15] has shown that it is possible, using simple linear theory, to position the zeros of the noise shaping transfer function at desired positions within the base band of the coder frequency

response rather than at dc. The zeros are moved away from dc by providing additional feedforward paths in the coder which result in nulls at the desired frequencies. This ability to control position of zeros is particularly attractive when a narrow band decimation filter is used. The coder can then maximize signal to quantization noise ratio within the bandwidth of the decimation filter.

The major disadvantage of this approach when CMOS switched capacitor circuitry is used is that the zeros are to be located at low frequencies relative to the clock frequency. With the structure proposed[15], this results in a high sensitivity to capacitor mismatch. Consequently, this structure is not considered further in this thesis.

Another possible structure variation would be to place a switched capacitor in parallel with the integrating capacitor of each integrator thus creating "leaky" integrators. The desired frequency response can be achieved but the ratio of largest to smallest capacitor exceeds 128 and is therefore clearly impractical without the use of special circuit techniques.

4.6 FIR Predictor

In this section, a simple FIR filter as the predictor of the input signal is introduced. It is investigated in an attempt to avoid large capacitance values at the input stage of the coder (resulting from a digital integrating predictor) without losing the advantage of reduced opamp slewing requirements.

Figure 4.7 shows a new second order coder structure, denoted SDND2P3. The linearized transfer function of the circuit is identical to that of SDND2 except that V_1 is replaced by the prediction value $V_1 \cdot f(z)$ where:

$$f(z) = \frac{1 + z^{-1} + z^{-2}}{3} \quad (4.3)$$

This change results in no significant difference in the magnitude of the noise shaping function within the 80kHz bandwidth of the coder. Its anticipated benefits are expected primarily to show up as reduced opamp slew rate requirements.

Similarly, Figure 4.8 shows a third order coder with the FIR predictor consisting of two and four taps and denoted SDND3P2 and SDND3P4 respectively. The prediction value $V1 \cdot f(z)$ is obtained by assigning:

$$f(z) = \frac{1 + z^{-1}}{2} \quad (4.4)$$

for a two tap predictor and

$$f(z) = \frac{1 + z^{-1} + z^{-2} + z^{-3}}{4} \quad (4.5)$$

for a four tap predictor.

Each of the two prediction values mentioned above has three functional elements that could be implemented in different ways:

- i) the delay operators
- ii) the tap coefficients, which are all $V1/i$ where i is the number of taps in the prediction value, and
- iii) the summing of the tap coefficients.

It is assumed that each delay operator will be implemented digitally since this can be done with a single flip-flop.

Since the prediction value generates a analog voltage based on samples from the output bit stream, some digital to analog conversion process is required. The question then arises of how to implement these functional elements in such a way as to minimize the impact of capacitor mismatch on the linearity of the DAC.

The summing of the predictor function can be realized either by digital or analog circuitry. A digital implementation would require a multibit DAC to convert the predictor to the analog form required by the coders switched capacitor circuitry. Since the predictor is placed in the feedback path, any nonlinearities introduced can not be attenuated by the coder noise shaping action. Where the multi-bit DAC would normally introduce nonlinearities due to mismatch of capacitor values used in its structure, such a mismatch occurring in an analog implementation of the summing function can result in only a minor variation of the tap coefficients.

The reason for this is that the analog implementation can use one simple, single bit DAC for each tap coefficient. Consequently, an analog implementation of the tap coefficients and the summing function can be performed without

nonlinearities arising from capacitor mismatches. This can be a significant advantage of these structures when compared to structures that have a multibit DAC in the feedback path.

Figure 4.7
3 Bit FIR Predictor, SDND2P3

Figure 4.8
2 Bit FIR Predictor, SDND3P2 and 4 Bit FIR Predictor, SDND3P4

4.7 Internal Signal Level Scaling

Another issue that affects all the structures discussed so far is the selection of signal levels to avoid saturation of the integrators. This saturation is undesirable because it could lead to harmonic distortion or another source of noise in the circuit.[10]

Figure 4.9 shows a block diagram of a typical second order noise shaping coder where K (as illustrated in Figure 3.4)

is the indeterminate quantizer gain. Since K assumes either a 1 or a -1 value depending only on the sign of the quantizer input signal, any desired scaling factor can be assigned to the quantizer. A modified block diagram can then be drawn corresponding to a new circuit with reduced signal levels. For example, in Figure 4.10, a factor of $1/2$ has been extracted from the quantizer and multiplied back through the preceding stages to reduce the signal levels by a factor of $1/2$. Identical performance at low input signal levels can be observed while larger input signal levels can be tolerated before integrator saturation occurs. Similarly, V_2 and G_2 could both be changed by some factor to change the signal level of only the second integrator without changing the value of V_1 or the frequency response of the coder. Thus changing V_2 while leaving G_2 constant is really equivalent to changing G_2 and adjusting the signal level of the second integrator. This feature allows the designer to choose tuning parameters and signal levels of each stage independently of each other and the frequency response of the coder as a whole. In the tuning for optimum frequency response one degree of freedom is therefore removed.

This process of scaling down signal levels can be continued until integrator saturation is no longer a limiting factor

and SNR performance, with noiseless components, is limited only by the quantization noise. In any analog circuit there are always certain sources of noise which depend on the technology and circuit techniques used. Consequently, in a given circuit the SNR due to analog sources of noise can be improved only by an increase in signal level. An increase in signal level causes, on the other hand, an increased signal distortion due to circuit nonlinearities. The existing trade offs are further discussed in Chapter 6.

Figure 4.9
A Typical Second Order Coder

Figure 4.10
The Same Coder with Signal Levels Reduced By 1/2

For the same input signal, this coder produces the same output sequence as the coder in figure 4.9 above. This is a key feature of the tuning strategy implemented in Chapters 5 and 6.

4.8 Structures with Multibit Output

There are a number of structures[16][17][18][19][20] that produce a multibit output. The increased number of bits at the output provides opportunities to reduce the high frequency attenuation requirements of the decimation filter but they are not the object of investigation in this thesis, as stated in Chapter 2.

Chapter 5

Simulations with a Technology Independent Integrator Model

5.1 Introduction

Although methods of linear analysis discussed in chapter 3 are useful for initial analysis, to include the effects of integrator saturation or an adequately versatile model for the comparator requires a time domain simulation. The principal advantage of a time domain simulation is that the comparator can be modeled quite simply for any of the predictive or noise shaping coder structures considered. The principal disadvantages are the required simulation time and the problem of converting the time domain results to the frequency domain to evaluate the SNR.

Consequently, the object of this chapter is to perform time domain simulations to determine performance capabilities and integrator signal levels for the various coder structures under consideration. This evaluation can be accomplished with simplified (near) ideal element simulations and thus can be seen as structure dependent rather than technology dependent. Since these evaluations require relatively short simulation times, they can be used as a preliminary step to

rule out any obviously inadequate structures before going on to the more detailed, time consuming, technology dependent simulations described in chapter 6.

5.2 Test Method

5.2.1 General

By assuming the ideal opamps with clipping are used, it is possible to describe the operation of a noise shaping or predictive coder with two sets of difference equations - one for the events that occur at the end of ϕ_1 and another for the events that occur at the end of ϕ_2 . (ϕ_1 and ϕ_2 are as illustrated in Figure 3.5) Provided that there is no continuous feedback from one integrator to another or from the quantizer to the input of an integrator, these equations have closed form expressions. They can readily be solved, for each time step, in a dedicated simulation program where the quantizer is the only noise source present. A 2048 time step simulation and FFT based coder output frequency analysis takes approximately 2 minutes. This time includes an overhead for simultaneous graphics generation on an IBM-PC-XT with an 8087 arithmetic coprocessor running at 8MHz clock frequency.

A more flexible approach is to incorporate the difference equations into a series of models in a general purpose simulator. This is the approach taken in Chapter 6.

5.2.2 Use of Windowing with the FFT

In simulation, it is possible to set the signal period to be an exact multiple of the sampling period and hence eliminate spectral smearing with respect to the input signal. Similarly, since the input signal is a pure sinusoid with a frequency less than $1/2$ the sampling frequency (f_s), aliasing does not occur.

The quantization noise, on the other hand, is both undersampled (by the FFT) and has a continuous spectral density. Hence, it is subject to misrepresentation by the FFT due to both spectral smearing and aliasing. There are, however, some factors that favour use of the FFT with a rectangular window. Since the quantization noise has small components at low frequencies and at frequencies near the sampling frequency, the effect of aliasing is usually not detectable with ideal element simulations. Since the spectral density of the quantization noise is continuous, spectral smearing is usually not a problem.

Figures 5.1 and 5.2 show two types of anomalies that can occur.

Figure 5.1 shows an example of an FFT taken on a bit stream where the number of 1's in a sample sequence is not equal to the number of -1's. The dc bias of the input signal under ideal element simulation conditions can readily be set to exactly zero. Consequently, any temporary divergence from zero dc bias in a finite sample sequence of the output bit stream can be considered an "end effect" that would normally be corrected by a window. With the anomaly that results from this condition, a flat spectral density appears in the FFT results. The anomaly could result from the rectangular window response to the slight dc bias or the FFT response to an impulse. The flat spectral density which is characteristic with this anomaly can be easily avoided by monitoring the dc bias of the sample sequence. When the dc bias of the sample sequence is not zero, the simulation can be continued through one or more cycle(s) of the sampling frequency clock until the number of 1's equals the number of -1's before performing the FFT on the resulting sample sequence.

Figure 5.2 shows another anomaly that occurs in third order coders. This shows the 20dB per decade roll off in the lower frequency range. The roll off, as discussed in[9], is a

result of noise occurring close to $f_s/2$. The noise does not fit into one of the FFT bins causing frequency domain smearing due to application of the rectangular window in the time domain. Since this anomaly cannot be predicted before computing the FFT, the only alternative is to return to the simulation and continue for another clock cycle. This can shift the FFT window one sample later in time. Since the anomaly occurs rarely, and it results from an end effect, a shift of only one clock cycle usually produces useful results.

Although these anomalies can also be avoided by the use of an appropriate window, the approach used here for ideal element simulations is to reject results where these anomalies occur. The motive for this approach comes from the fact that the rectangular window does not spectrally smear the input sinusoid. Thus the input sinusoid occupies 1 rather than 5 FFT bins. With a sampling frequency of 10.24MHz and a bandwidth of 80kHz, there are only 16 bins over which to sum the in-band noise power in a 2048 point FFT. If 1 rather than 5 bins are lost (from the noise summation) to the input signal, then there are 15 rather than 11 points over which to sum the noise power, resulting in less error and greater statistical confidence in the

results. The same or greater statistical confidence could potentially be achieved by increasing the length of the sample sequence but this substantially increases the simulation time and consequently reduces the efficiency of the simulations.

Figure 5.1
First Type of Anomalous Result

Since the anomaly can be predicted before evaluating the FFT, it can be avoided by using a sample sequence where the number of 1's equals the number of -1's.

Figure 5.2
Second Type of Anomalous Result

Since this type of anomaly cannot be predicted before evaluating the FFT, the FFT must be evaluated to determine if the anomaly will occur.

5.3 Test Program

5.3.1 Reference for Input Signal Levels

The convenience of representing oversampled ADC input signal levels in dB is well established in the literature[16][17][20][21]. What is not so well established is the appropriate selection of a reference (0dB) level. There appear to be three potential candidates. Two have been found in the literature and one is introduced here.

One approach is simply to use the ratio of the rms voltage of the input sinusoid to the physical reference voltage as follows:

$$20 \text{Log} \left(\frac{X}{V_r} \right) \quad (5.1)$$

where X and Vr are the input signal and physical reference voltage of the first integration stage of the coder as illustrated in Figure 3.5. Unfortunately, this approach can result in an arbitrary shift of the 0dB point for a given coder structure in the following way. For example, if Vr was reduced by a factor of 2 and C2 (in Figure 3.5) was increased by a factor of 2, the 0dB point of any of the curves in Figures 5.3 to 5.8 would be shifted by 6dB

although the coder with a given input signal level produces exactly the same output bit stream. This could produce a horizontal shift in the curves of Figures 5.3 to 5.8 that depends on the implementation of the coder structure rather than the structure itself. Since the goal of this chapter is to compare coder structures independently of their implementation, it is undesirable to allow this somewhat arbitrary horizontal shift.

Another approach that attempts to avoid this arbitrary shift is to select the 0dB point as the input signal level which produces the maximum SNR. The immediate advantages of this approach are that it does not depend on implementation details or signal level scaling. The difficulties of this approach lie in determining exactly where the peak SNR occurs as a function of input signal level. Many simulations are required to find the input signal level which produces the peak SNR especially when attempting to take into account the statistical variations when SNR is calculated from several finite sample sequences. This approach becomes even further clouded when the signal level producing peak SNR depends on the frequency and shape (sinusoid vs square vs actual 2B1Q symbols etc.) of the input signal.

The approach taken here has four advantages compared to previous work reported in the literature:

- i) The 0dB level is determined from the coder structure and is therefore known before performing any simulations. This avoids the problem of finding the input signal level which produces SNR_p .
- ii) The 0dB level is independent of any of the signal level scaling operations discussed in section 4.7. Consequently, figures 5.3 to 5.8 apply to the coder structures considered for any signal levels in the integrators.¹
- iii) The 0dB level is independent of the physical reference voltage. Consequently, any change in the physical reference voltage and capacitor ratio used to implement V_1 , the system reference voltage, does not require rescaling of Figures 5.3 to 5.8.
- iv) The 0dB level corresponds to a continuous stream of 1's in the output bit stream. Since the rms value of a stream of -1's or, in fact, any stream of 1's and -1's will have the same rms value, the relative input level

¹ This statement is tempered somewhat in section 5.4.2 for third order coders where saturation of the integrators can play a vital role in the stability of coder structure.

axis of Figures 5.3 and 5.8 provides a measure of the signal strength relative to the total signal strength available in the bit stream. This can provide useful information in design of the decimation filter or evaluation of coder structures as will be discussed in section 5.4.2.

The introduction of this new 0dB level obtains these advantages by referring the input signal level to the output bit stream. With a bit stream of +1's and -1's the rms output of the coder is 1 for all input signals^[7]. From Figures 3.4 and 3.5, it can be seen that the conversion gain of the coder is given by $G1/V1$ in terms of the block diagram or $C1/(Vr C2)$ in terms of the actual implementation of the first integration stage. Thus, the input signal level that would use up all of the available rms output signal would be $V1/G1$ (Volts) or $(Vr C2)/C1$ (Volts). This dc voltage level is the rms signal level that is taken as the reference (0dB) voltage.

5.3.2 SNR Performance Measures

The time domain simulations are performed to determine SNR_p , the maximum SNR for the coder structure considered, as a function of relative input level. The SNR at any input level

is calculated as the power of the input sinusoid divided by the power of the noise and non-linear error (harmonics) within the 80kHz bandwidth of the coder. In this thesis, another performance measure, DR_{65} is introduced as a measure of dynamic range of the input signal. It is defined as the ratio of the maximum input signal level resulting in an SNR greater than 65dB to the minimum input signal level satisfying the same condition.

5.3.3 Relative Signal Levels

To qualitatively compare the sensitivity of various structures to the effects of opamp non-linearity and bandwidth, it is necessary to know the maximum and rms voltage levels at the output of each integrator, denoted V_{o1} , V_{o2} , etc. Another value of interest is the integrator output voltage variation from one time step to the next. Over the period of the simulation, it is then possible to determine minimum, maximum and rms values for these voltages denoted ΔV_{o1} , ΔV_{o2} etc. These two sets of voltages can be used as figures of merit to compare different coder structures and the effect of tuning. The proper signal level scaling can therefore be determined to prevent saturation of the integrators and/or to prevent exceeding the slew rate

limits of the opamp's. In order to provide comparisons based on tuning parameters independently from signal level scaling, these voltages are presented for each integrator relative to the value of the reference voltage. The maximum amplitudes of V_{oi} and ΔV_{oi} voltages corresponding to peak signal to noise ratio (SNR_p) are of primary interest to select appropriate levels of voltage scaling.

5.3.4 Sensitivities to Analog Sources of Noise

In this section, a method of employing several of the methods developed earlier in this thesis is discussed. Having performed coder simulations with any given system reference voltage, it is possible to observe the coder signal levels corresponding to that reference voltage. Then, by employing the signal level scaling operations developed in section 4.7, it is possible to select larger values of V_1 and G_1 that will increase the signal levels to the maximum that can be used without saturating the integrators. This operation will reduce the sensitivities to analog sources of noise, α_{nn1} and α_{nn2} introduced in section 3.3 and Appendix 1, to their minimum value. To evaluate these minimum values, some assumptions about the implementation details have to be made.

The assumptions made in calculation of the α_{nn1} and α_{nn2} values shown in tables 5.1 and 5.2 are:

- i) that the integrators are single ended, as opposed to fully differential, and saturate at ± 2.5 Volts,
- ii) that the maximum available reference voltage is ± 2.5 Volts, and
- iii) that the desired input sinusoid producing SNR_p is 1 Volt rms.

With this set of assumptions applied consistently to all structures considered, these sensitivities form a useful figure of merit to compare different coder structures. The maximum values that can be used for $V1$ and $G1$ ($V1_{max}$ and $G1_{max}$) are presented in the tables. Knowing these coder parameters allows calculation of the best possible α_{nn1} and α_{nn2} for each structure. The calculated noise sensitivities that result from using $V1_{max}$ and $G1_{max}$ in equation (A1.17) are shown in Tables 5.1 and 5.2 along with the simulation results to compare the potential performance of coder structures.

5.4 Simulation Results

5.4.1 Second Order Coders

Since the second order coders have the indeterminate gain properties discussed in section 4.7, only one tuning parameter is available as far as the frequency response is concerned. It is convenient then to look at performance and signal levels as a function of G_2 in order to determine optimum value of this tuning parameter for each structure. Appendix 2 contains figures to show the SNR and signal levels in the integrators as a function of G_2 for the three second order coders considered. The optimal value of G_2 , found in Appendix 2, is 0.5 for the delaying structure with no predictor, SDD2. This agrees with the work of Lamkemeyer et al[11]. The optimal value of G_2 found for the non-delaying structure without a predictor, SDND2, is 1.0 which agrees with the work of Candy[4].

Additional performance analysis results are presented in Table 5.1. The values of G_2 are chosen to evaluate each structure where it is optimally tuned and to allow comparisons to test chips fabricated at Mitel Semiconductor.

The simulation results presented in table 5.1 indicate that a nondelaying version of a coder does not significantly differ from the delaying integrator version.

Based on the simulation results presented in Table 5.1, clearly the best second order coder is SDND2P3 with $G_2=0.5$. It has both the highest performance and, in most cases, the lowest signal levels relative to the reference voltage. Although the integrator output signal levels of the second integrator are higher in the non-delaying version with or without the predictor, this is not as undesirable as high integrator output signal levels in the first stage because errors introduced in the second integrator can be noise shaped by the first integrator.

Table 5.1 Performance and Signal Levels
Second Order Coders

Coder Structure		SDD2	SDND2	SDND2	SDND2P3	SDND2P3
Figure		5.3	5.4	5.5	5.4	5.5
G2		0.50	0.33	1.00	0.33	0.50
SNR _p	(dB)	71	74	72	78	78
DR ₆₅	(dB)	10	8	11	11	14
V1 max		0.72	0.61	0.94	0.61	0.74
G1 max		0.48	0.44	0.63	0.45	0.50
α_{nn1}	(dB)	5.1	4.9	5.0	4.9	5.0
α_{nn2}	(dB)	12.5	13.0	11.0	12.8	12.3
Vo1/V1	rms	1.24	1.96	0.84	1.88	1.32
Vo1/V1	max	2.74	3.76	2.09	3.64	2.92
ΔVo1/V1	rms	0.84	0.80	0.84	0.32	0.32
ΔVo1/V1	max	1.74	1.88	1.80	0.84	0.96
Vo2/V2	rms	0.80	1.24	1.76	1.00	1.20
Vo2/V2	max	2.11	2.84	4.99	2.48	3.92
ΔVo2/V2	rms	0.68	0.92	1.32	0.80	0.80
ΔVo2/V2	max	1.56	2.24	3.09	1.88	1.96

The structures under consideration are:

- SDD2 Sigma Delta modulator with Delaying integrators, 2nd order
- SDND2 Sigma Delta modulator with Non-Delaying integrators, 2nd order
- SDND2P3 Sigma Delta modulator with Non-Delaying integrators, 2nd order and a Predictor using 3 bits from the bit stream
- G2 represents the tuning of the frequency response

Table 5.1 (Continued)

The simulation conditions are:

Input	
Sinusoid	35kHz
Noise	
Bandwidth	80kHz , and
FFT Length	2048 points

Table 5.1 (Continued)

The criteria evaluated are as follows:

Figure	indicates the figure where a plot of SNR vs. relative input signal level is presented. (See section 5.3.1 for an explanation of relative input level)
SNR _p	indicates the peak SNR as a function of relative input signal level. (See section 5.3.2)
DR ₆₅	indicates the range of relative input signal levels that produce an SNR greater than 65dB. (See section 5.3.2)
V1 max	indicates the maximum value of system reference voltage that will not saturate a single ended switched capacitor integrator that has ± 2.5 Volt power supplies.
G1 max	indicates the maximum gain of the first switched capacitor integrator that will allow an input sinusoid of 1V rms without saturating the bit stream or the integrators.
α_{nn1} and α_{nn2}	indicate approximately the sensitivity to KT/C noise and opamp noise respectively. (See section 3.3 and Appendix 1)
Vo1/V1 and Vo2/V2	indicate the signal levels at the integrator output stages relative to the system reference voltage where rms indicates the rms value and max indicates the maximum value observed in the course of the simulation.
$\Delta Vo1/V1$ and $\Delta Vo2/V2$	indicate the change in integrator output voltage per clock cycle relative to the system reference voltage where rms indicates the rms value and max indicates the maximum value observed in the course of the simulation.

Figure 5.3
SNR vs Input Level
SDD2

Figure 5.4
 SNR vs Input Level
 A Comparison of SDND2 and SDND2P3 Same with
 the Same Tuning Parameter

Figure 5.5
SNR vs Input Level
A Comparison of SDND2 and SDND2P3 with G_2
Near its Optimal Value for Each Coder

5.4.2 Third Order Coders

For the third order, Ritchie structure coders, there was no further effort to optimize the tuning beyond selecting coefficients which move the poles of the linear transfer function to high frequencies and then several trial and error iterations to find appropriate signal levels in the time domain simulations. (See section 4.3 for details.) Nevertheless as shown in Table 5.2 better SNR_p and DR_{65} can be obtained both by using non-delaying integrators and by using an FIR predictor of the input signal.

With the Digital Integrating Predictor (DIP) structure, referenced to the least significant bit of the predictor, it is interesting to note that the reduction of signal levels claimed to be an advantage of this structure are produced more by voltage scaling of the signal levels than by the DIP structure itself. In fact, the FIR predictor produces comparable results for the same reason. Consistent with the concept that the digital integrating predictor achieves reduced slew rate and saturation level requirements by scaling, are the high sensitivities to analog sources of noise as indicated by the a_{nn1} and a_{nn2} noise coefficients presented. Due to these problems and the lack of a

dependable tuning strategy, the digital integrating predictor structure is not considered further in this thesis.

As with the second order coders, the best contender appears to be the non-delaying Ritchie structure with an FIR predictor. Consequently, the delaying integrator coder, SDD3, is not considered further as a candidate for implementation.

SDND3P4 is also the coder structure that can accommodate the largest signal level in the output bit stream. The relative-input-level reference adopted in section 5.3.1 highlights the fact that while the second order coders can accommodate signal levels in the bit stream up to 3dB below the total bit stream rms value, most of the third order coders can accommodate signal levels as large as only 10dB below the bit stream except SDND3P4 which can accommodate signal levels in the bit stream as large as 7dB below the bit stream.

As indicated in[22], the clipping effect of the integrators is required to maintain the stability of the circuit. Although the signal levels of the integrators can be scaled as discussed in section 4.7, the clipping action is required to allow the circuit to rapidly extinguish the noisy

modes[4] that arise in these third order coders. Consequently, the maximum value recorded in the course of the simulation reflects the saturation level of the integrator not the behaviour of the coder structure and "clip" is recorded in the table.

Table 5.2 Performance and Signal Levels

Third Order Coders

Coder Structure		SDD3	SDND3	SDND3P2	SDNDP4	SD3DI P
G2		0.33	0.33	0.33	0.33	0.33
G3		0.34	0.60	0.60	0.60	0.60
SNR _p	(dB)	82	86	89	89	87
DR ₆₅	(dB)	14	24	25	32	30
V1 max		0.90	0.75	0.75	0.75	0.23
G1 max		0.26	0.23	0.25	0.30	1.00
a_{nn1}	(dB)	4	4	3	3	12
a_{nn2}	(dB)	16	17	16	15	25
Vo1/V1	rms	1.01	1.12	1.03	0.77	1.07
Vo1/V1	max	2.58	clip	2.99	1.93	3.07
Δ Vo1/V1	rms	0.96	0.95	0.56	0.27	1.29
Δ Vo1/V1	max	1.36	1.44	1.40	0.85	2.20
Vo2/V2	rms	1.95	1.05	0.92	0.77	1.02
Vo2/V2	max	clip	2.73	2.47	2.12	2.82
Δ Vo2/V2	rms	0.98	1.12	0.97	0.97	1.29
Δ Vo2/V2	max	1.70	2.11	1.87	1.61	2.55
Vo3/V3	rms	1.68	1.20	1.09	0.95	8*
Vo3/V3	max	3.82	clip	3.24	2.21	11*
Δ Vo3/V3	rms	3.95	1.31	1.25	1.28	1*
Δ Vo3/V3	max	3.52	2.64	2.48	2.27	1*

* Note: binary output of digital integrator

Table 5.2 (Continued)

The structures under consideration are:

SDD3	Sigma Delta modulator with Delaying integrators, 3rd order
SDND3	Sigma Delta modulator with Non-Delaying integrators, 3rd order
SDND3P2	Sigma Delta modulator with Non-Delaying integrators, 3rd order and a Predictor using 2 bits from the bit stream, and
SDND3P4	Sigma Delta modulator with Non-Delaying integrators, 3rd order and a Predictor using 4 bits from the bit stream.

The simulation conditions and criteria evaluated are the same as with the second order coders.

Figure 5.6
SNR vs Input Level
SDD3

Figure 5.7
SNR vs Input Level
A Comparison of SDND3, SDND3P2 and SDND3P4

2 of/de 2

MicroD

Figure 5.8
SNR vs Input Level
SD3DIP

Chapter 6

Simulations With a Technology Dependent Integrator Model

6.1 Introduction

In this chapter a model for simulating several effects common in switched capacitor integrators is introduced. The effects are feedforward capacitance in the circuit, slew-rate-limited exponential or damped-sinusoid settling, and dc non-linearity. This model allows efficient, system level simulation of many of the impairments resulting from non-ideal performance of circuit components. Methods to extract these impairments from detailed device level simulation or, preferably, from actual components are also presented.

To take these impairments into account in the design process, it is desirable to be able to simulate their effect at the system performance level before committing to fabricate the circuit. Since system level simulations often require a length of tens of thousands of clock cycles, doing this with a device level simulator such as SPICE[23] would take an unacceptable length of time. Consequently, such simulations are often performed by executing a program written in a high level language. This type of simulation

usually omits second order impairments such as non-linearity and slew rate limiting due to a lack of models that can efficiently capture their effects.

A model is introduced in this chapter to resolve this conflict between simulation speed and detail of simulation. The model simulates the behaviour of a sampled data integrator with a series of parameters, extracted from the results of a device level simulator, SPICE. This approach has then been implemented as an electrical model using SPLICE[8] as the system level behavioural simulator. A flow chart of this approach is shown in Figure 6.1.

The model addresses two general classes of non-ideal integrator behaviour. The first class is a static error stored in a lookup table. The second class of non-ideal behaviour relates to the settling behaviour of the integrator. Since the settling behaviour of an integrator will in general be highly dependent on the nature of the opamp used to implement the integrator, two parameter sets are available in the model. One parameter set is for single pole opamps while the other is for two pole opamps. The approach to model the first class of error is discussed in section 6.2. The approaches to model the second class of error are discussed in section 6.3.

Figure 6.1
Proposed User Environment

6.2 Effects of Finite Opamp Gain

If settling of the integrator output was allowed to be fully completed before the beginning of the next clock cycle, the value to which the output would settle is determined by a fixed, non-linear relationship between the output node voltage and the voltage at the inverting input to the opamp. This relationship results from the opamp open loop gain as a function of the voltage at the output of the opamp as well as any non-linearities in the feedback capacitor. The model introduced in this chapter stores this relationship in a lookup table such that every ideal V_{ol} is mapped to a non-ideal V_{ol} through a linear interpolation of the lookup table. The ideal integrator output voltage V_{ol} is based on the usual integrator equation:

$$V_{ol} = V_{ol}z^{-1} + G_1Xz^{-1} + V_1Yz^{-1} \quad (6.1)$$

where X , Y , G_1 , and V_1 are the coder input voltage, coder output bit, coder input gain and coder system reference voltage as defined in section 3.2.

This ideal V_{ol} is then used to look up the non-ideal V_{ol} .

Figure 6.2 shows an example of a possible lookup table. The table is a series of x and y co-ordinates with the x co-ordinate being the ideal or target Vol and y being the non-ideal Vol produced in the simulation. The difficulty is in establishing the relationship between the target Vol and the non-ideal Vol. Possible approaches to obtain this relationship are:

- i) For each point on the curve perform a transient simulation or test and then record the non-ideal Vol. This approach can be considered the most theoretically complete in that all non-linear effects, except charge sampling on the input capacitors, can be captured and lumped into the one curve. However, it requires many test points and is consequently time consuming to simulate or test. In parts of the curve where the open loop opamp gain is high, it is also difficult to detect the difference between the ideal Vol and the non-ideal Vol accurately enough to reflect the true gain of the opamp. The difference between these two values of Vol could well be less than the convergence noise in a simulation or, in a test, less than the instrument precision/accuracy.

- ii) Replace the capacitors with resistors and obtain a dc transfer curve relating the input voltage to the output voltage. This is well suited for simulation. However, it misses the effects of stray capacitances at the inverting input to the opamp.
- iii) By recording the opamp dc, or low frequency, gain as a function of dc output voltage and then calculating the error in the finite gain dc transfer curve from a linear interpolation of this gain, a curve can be obtained with similar limitations as in ii) above.

As discussed in section 6.5, approach i) is used in the model verification. Approach ii) is used in section 6.6 to characterize the integrators to be used in the target environment.

The use of a single non-linear mapping can not include simulation of the effects of a non-linear sampling capacitance. However this could be built into the model for future work or even used as a separate model.

Figure 6.2
Typical Lookup Table

6.3 Effects of Finite Opamp Bandwidth and Slew Rate Limiting

Two separate behavioural models are required to cover the behaviour of the opamps considered in this thesis. For single pole, folded cascode opamps of the type shown in Figure 6.3 the transient response is modeled as an exponential rise with the time constant determined by the output resistance of the opamp and the capacitance of the load. The opamp in the SDD3 test chip is of this type. For two pole, pole splitting opamps of the type shown in Figure 6.4 the transient response is modeled as a second order damped sinusoid. opamp1 and opamp2 discussed in section 6.6 are both of the pole splitting type. Both of these models

include a separate slew rate limit for both positive and negative changes in integrator output voltage. These slew rate limits provide another source of non-linearity in noise shaping oversampled coders.

Figure 6.3
Single Pole Folded Cascode opamp

Figure 6.4
Two Pole, Pole splitting opamp

The SPLICE models discussed in this chapter are characterized by a transient response that begins at the beginning of ϕ_2 , and ends at the end of ϕ_2 . The models use TACT to denote the instant ϕ_2 begins and TPER to denote the instant ϕ_2 ends. Between the two time instants, the integrator circuit looks as shown in Figure 6.5. The linear response does not continue beyond TPER into the next cycle because as ϕ_2 falls the circuit changes to that shown in Figure 6.6 and the voltage at V_n is instantaneously driven to the same value as that at the non-inverting opamp input. The result of this is a 'freezing' of the output at time TPER as shown in Figure 6.7 for the two pole amplifier model and Figure 6.8 for the single stage amplifier model. In each of these figures the time for each phase has been deliberately reduced to less than what would be normally used to emphasize the 'freezing' effect.

During the time between TACT and TPER the model puts out a value which is an ideal linear response limited by a fixed slew rate as in [24]. For the two pole amplifier model, the transient response related parameters are: damped frequency of oscillation, damping factor, positive slew rate and negative slew rate, and feedforward capacitance ratio producing a response as shown in Figure 6.9.

For the two stage amplifier model, the relationship between the damping factor, the slew rate and the damped frequency of oscillation is such that at the time when the model switches from slewing to ringing, the derivative of the ringing equation is equal to the slew rate and the second derivative of this equation is equal to 0. This provides a smooth transition from slewing to ringing. For the single stage model the conditions are only that the change in transient response from slewing to an exponential response occurs when the first derivative of the exponential is equal to the slew rate.

There is a special case when the MRT, minimum resolvable time, of the simulation is large enough that TACT and TPER occur in the same MRT. In this case, the value at TPER is calculated based on a settling time of TPER-TACT and hence it is possible to observe the effects of small changes in clock timing without resorting to a small MRT. It also allows long simulations for oversampled ADC's or SC filters to be carried out with only two MRT's per clock cycle. This is the mode in which the model has been most commonly used.

Figure 6.5
Integrator During $\phi 2$
Between the Times TACT and TPER

Figure 6.6
Integrator at the End of $\phi 2$
At the Time TACT

Figure 6.7
Ringing with Slew Rate Limiting

Figure 6.8
Slew Rate Limited Exponential Response

Figure 6.9
Combined Effects

6.4 Weaknesses of the Model

The equations used in the model do not allow simulation of the several effects such as:

- i) the effects of non-linear sampling capacitors,
- ii) the effects of clock feed through (charge injection) where stray capacitances of the switches couple some of the clock signal through to the output signal, and
- iii) the simultaneous effect of the non-linearity on the transient response of the opamp.

6.5 Verification of the Model

A complete verification of the model is unavailable at the present time due to a lack of test chips to compare simulated versus actual results. However, with the one test chip that is available a comparison between simulated and actual results is presented. In the case studied, the simulated results indicate that the non-ideal opamp's are the dominant source of error in the test chip.

The test chip is an implementation of SDD3 (Sigma Delta modulator with Delaying integrators, 3rd order) as defined in Chapter 5. It uses folded cascode opamps of the type shown in Figure 6.3.

The look up table used to simulate the first integrator of this coder is shown in Table 6.1. Except for the value at an ideal output voltage of 0, the simulated %error values in column 2 of Table 7.1 are obtained from time domain simulation^[14] as discussed in section 5.2i). The %error for 0 Volts output is obtained from the small signal ac gain of the opamp. Other points are interpolated into the table to provide some non-linearity for signals larger than 0.5V. Figure 6.10 shows the error in the lookup table used to simulate the non-ideal settling voltage of the integrators.

The positive and negative slew rate and the time constant for the transient response of the single stage opamp are 52.7 V/ μ s, 53.0 V/ μ s and 20ns respectively. All three values are derived from large signal transient simulations ^[14].

A comparison between the simulated and measured^[25] results is shown in Table 6.2. The results show substantial agreement between the measured and simulated results, indicating that the effects simulated are, in fact, the

dominant sources of noise in this particular circuit. It is interesting to compare the laboratory results and the simulation results of this chapter to the ideal element simulations of the same SDD3 structure in Chapter 5. To make this comparison with different sampling frequencies, it is necessary to use the same f_s/B ratio of 128 as in Chapter 5 but now $f_s=5\text{MHz}$ so that $B=40\text{kHz}$. The noise shown in Table 6.2 can then be integrated from dc to 40kHz giving an SNR of 58dB or 64dB for the simulated and measured results respectively. When compared to the SNR_p of 82dB resulting from the ideal element simulation, it can be seen that the non-ideal opamp model provides a substantial improvement in accuracy of the performance estimate.

Although it is clear that the model can provide improved simulation accuracy in some cases, the absolute accuracy of the simulation model should also be considered. Neither the laboratory measurements nor the simulation are completely free of systematic and random error. Consequently, evaluation of the absolute accuracy of the simulation with only these results is difficult. At this point, the best that can be said is that the laboratory results represent

the better estimate of the actual coder performance. The simulation results have many more sources of systematic error. Examples are:

- i) fitting the SPICE MOS transistor model to the actual process,
- ii) the lack of charge conservation in the SPICE algorithm, and
- iii) fitting the SPICE simulation results to the behavioural model.

Since these errors could accumulate in a manner that suggests the performance will be either better or worse than the actual performance, it can be concluded from the results in Table 6.2 the behavioural model, in this particular case, is too pessimistic. A more complete evaluation of the behavioural model is left for future work as well characterized test environments and a wider variety of test chips become available.

In addition to improvements in accuracy, the non-ideal model provides opportunities for improvements in the understanding of the effects of non-ideal circuit elements. For example, it may not be obvious that non-linearities in the

integrators can give rise to a white noise floor in the bit stream output but the simulation shows this effect quite clearly. The actual source of this noise floor is that the input signal and the quantization noise are both high level signals. Consequently, when they are summed and passed through a non-linearity, a mixing action occurs due to intermodulation distortion which results in multiple spectral copies of the quantization noise, each shifted by a multiple of the input sinusoid frequency. The role of the simulation model in investigating this type of behaviour is to verify analytical techniques or at least to develop a better intuitive understanding of the interaction between various sources of non-ideal behaviour.

For this purpose, the absolute accuracy of the simulation method is not as important as its ability to represent the fundamental characteristics of the circuit operation. Since the goal of this research, is to develop that understanding, the model can be quite useful without being highly accurate. For example, the relative performance of the coder structures is of primary interest when the model is used to evaluate coder structures that will all face the same

impairments in implementation. Consequently, the multiple inaccuracies listed above are acknowledged but are not considered an obstacle to the rest of the work.

Table 6.1

Look Up Table For SDD3 Simulation

Ideal	Reported	Interpolated	Non-Ideal
Vout	Error	Error	Vout
(Volts)	(%)	(%)	(Volts)
-2.25	2.5	2.5	-2.19375
-2.00		1.6	-1.96800
-1.75	1.0	1.0	-1.73250
-1.50		0.7	-1.48875
-1.25	0.6	0.6	-1.24250
-1.00		0.5	-0.99520
-0.75		0.4	-0.74730
-0.50		0.3	-0.49850
-0.25		0.3	-0.24925
0.00	0.3	0.3	0.00000
0.25		0.3	0.24925
0.50		0.3	0.49850
0.75		0.4	0.74700
1.00		0.5	0.99500
1.25	0.7	0.7	1.24125
1.50		.2	1.48200
1.75	2.5	2.5	1.70625
2.00		4.0	1.92000
2.25	6.0	6.0	2.11500

Figure 6.10
Error in Finite Gain dc Transfer Curve
opamp used in SDD3 Simulation

Table 6.2

Comparison of Simulated vs Measured Results

	Simulated	Measured
Input Voltage (Volts Peak)	2.5	2.5
Input Frequency (kHz)	17.5	17.5
Sampling frequency (MHz)	5	5
Number of FFT Points	16384	16384
Noise Floor * $_{dB/\sqrt{Hz}}$	-104	-110
Harmonics: *		
Second (dB)	-65	-60
Third (dB)	-60	-60
Fourth (dB)	-60	-60

Notes: * Referred to 2.5Vp (1.76 Vrms) sinusoidal input signal

6.6 Use of the Model in the Target Environment

In this section, the technology dependent effects of non-ideal opamps are introduced to some of the coder structures of Chapter 5. The structures considered are the second and third order Ritchie structure coders with non-delaying integrators and FIR predictors. For the second order coders, only the coders with $G2=0.33$ are considered. It would be interesting to evaluate each of the second order coder structures at the optimal tuning as determined in Chapter 5 but time constraints and the availability of test chips with $G2=0.33$ dictate that the second order coders be evaluated only with $G2=0.33$.

To proceed with this evaluation, two steps are taken:

- i) Clearly, to determine the effects of non-ideal opamps some characterization of each opamp is required. Since opamp designs are new, this characterization is carried out by simulation in SPICE with the best available parameters for the process at the time.
- ii) Once the opamp characteristics are established the issue of selecting appropriate signal levels for each integrator output must be resolved. This results in a

trade off between replicated quantization noise produced at high signal levels against the traditional analog sources of noise at low signal levels.

6.6.1 Opamp Characterization

The goal of characterization in this section is simply to establish the parameters needed for simulation as described in sections 6.2 and 6.3. For this purpose, the lookup table is obtained from the SPICE simulation of the finite gain dc transfer curve for the opamp used as described in section 6.2ii). The error in the lookup tables is shown in Figures 6.11 and 6.12 for opamp1 and opamp2.

The transient response parameters are estimated from SPICE large signal transient response for the positive and negative slew rates (SRP and SRM respectively), damped frequency of oscillation, ω_d , and damping factor, ζ . Since both opamp1 and opamp2 are pole splitting opamps of the type shown in Figure 6.4, the transient response of the integrators is not very sensitive to the capacitive load on the amplifier output. Consequently, the same opamp

characteristics can be used for different circuit configurations with slightly different loads. The results are summarized in Table 6.3.

Table 6.3
Opamp Transient Response Characteristics

	Opamp1	Opamp2
Model Type	Pole Splitting Figure 6.4	Pole Splitting Figure 6.4
ω_d (rad/sec)	$6.3 \cdot 10^8$	$9.0 \cdot 10^7$
ζ	0.4	0.8
SRP (Volts/sec)	$2.0 \cdot 10^8$	$3.7 \cdot 10^7$
SRM (Volts/sec)	$-2.0 \cdot 10^8$	$-2.0 \cdot 10^8$
V_n (uV rms) *	8	2.5

* In-band opamp noise referred to opamp input includes broadband noise (and its aliases) and 1/f noise in the bandwidth from 20kHz to 60kHz. The in-band noise is calculated from SPICE simulations of the opamp.

There are a number of problems with the parameters used here:

- i) The feedforward capacitance ratio can depend significantly on the circuit configuration rather than the opamp characteristics and can be determined practically only by post layout simulation for each circuit configuration of interest. Based on a SPICE simulation of SDND3, with stray capacitances for the switch transistors and opamps but not including routing capacitances, FFC was chosen to be 0.2 for all the simulations in this section.
- ii) The characteristics have some known deficiencies. The SPICE parameters used for the transistor model are taken from an early stage of Mitels $2\mu\text{m}$ process characterization and are not fully verified. The characteristics in Table 6.3 are also based on a limited sample size (one positive large signal transient and one negative large signal transient) rather than a best fit to a large sample size.
- iii) For opamp2 the model is not really adequate. When slewing negatively, the response appears to be that of a single pole opamp. However, when slewing positively,

the response overshoots as a typical two pole amplifier and then settles negatively in a single pole response. Although the model cannot cover this behaviour, by carefully selecting the opamp characteristics, it can capture the unbalanced nature of the opamp settling characteristics. The approach used here is to use a much larger magnitude for the negative slew rate of opamp2 than it actually has.

Figure 6.11
Error in the Lookup Table for Opamp1

Figure 6.12
Error in the Lookup Table for Opamp2

6.6.2 Simulation Results

Simulation results for peak SNR, SNR_p , of the coders of Chapter 5 are presented in Table 6.4 along with the calculated noise from analog sources, SNR_a . Here the signal to quantization noise and harmonics are combined before taking the ratio SNR_p . Both ratios are presented for the reference voltage shown. (Unlike the simulations in Chapter 5, signal levels have a major impact on the coder performance with the non-ideal models in this chapter.) The table also provides a reference to the appropriate figure to see the relative amount of harmonics and noise generated.

Table 6.4

Coder Performance with Technology Dependent Integrator Model

Coder Structure	Ideal* SNR (dB)	SNR_p (dB)	SNR_a (dB)	SNR_p (dB)	SNR_a (dB)	V1 (V)	Fig. Number
		Opamp1		Opamp2			
SDND2	74	73	87	40	91	0.6	6.13
SDND2P3	78	73	84	56	88	0.6	6.14
SDND3	86	56	87	56	91	0.75	6.15
SDND3P2	89	86	86	59	89	0.75	6.16
SDND3P4	89	87	89	57	87	0.75	6.17

* SNR evaluated from ideal element simulations in Chapter 5.

Table 6.4 (Continued)

The structures under consideration are:

SDND2	Sigma Delta modulator with Non-Delaying integrators, 2nd order
SDND2P3	Sigma Delta modulator with Non-Delaying integrators, 2nd order and a Predictor using 3 bits from the bit stream
SDND3	Sigma Delta modulator with Non-Delaying integrators, 3rd order
SDND3P2	Sigma Delta modulator with Non-Delaying integrators, 3rd order and a Predictor using 2 bits from the bit stream, and
SDND3P4	Sigma Delta modulator with Non-Delaying integrators, 3rd order and a Predictor using 4 bits from the bit stream.

The simulation conditions are:

Sampling Frequency	10.24MHz
Input Sinusoid	1.2 Vp at 10kHz
Decimation Filter	Ideal Low Pass at 80kHz (applied in frequency Domain)
Window function	Blackman Harris ^[9] modified per Figure 15 of [26]
Number of points in FFT	32768

Figure 6.13
Frequency Response of SDND2
Opamp1 vs Opamp2

Figure 6.14
Frequency Response of SDND2P3
Opamp1 vs Opamp2

Figure 6.15
Frequency Response of SDND3
Opamp1 vs Opamp2

Figure 6.16
Frequency Response of SDND3P2
Opamp1 vs Opamp2

Figure 6.17
Frequency Response of SDND3P4
Opamp1 vs Opamp2

As indicated in Table 6.4 the second order coder with opamp1 and signal levels corresponding to a reference voltage of 0.6V will perform acceptably.

The results presented in Table 6.4 seem to indicate that with the signal levels considered, opamp2 does not ensure expected signal to noise ratios. It should be noted however that opamp2 exhibits significantly lower noise. Consequently, proper signal level scaling can result in an overall performance improvement.

This argument is supported by the simulation results in Figure 6.18. Scaling down the internal signal levels in the coder can be achieved by reducing the reference voltages V1 and V2 as well as the input gain G1 by the same amount. (This is discussed in more detail in section 4.7.) In Figure 6.18 both the quantization noise and the analog sources of noise are plotted as a function of V1 to illustrate the available design compromises as the internal signal levels are scaled. As the internal signal levels are increased by increasing V1 and the other parameters, it can be seen that the analog sources of noise become less significant. However, the quantization noise and non-linear error resulting from non-ideal circuit components increase as the signal levels increase. Clearly, the optimal signal level

scaling occurs where the analog sources of noise are equal to the noise produced by quantization noise and non-ideal circuit elements.

Figure 6.18 indicates that opamp2 can achieve close to ideal element performance for signal levels corresponding to a reference voltage as large as 0.45 volts when a three bit feedback is used; whereas the usual single bit feedback requires attenuation of signal levels to correspond with a reference voltage of 0.15 volts or less. This reduced attenuation requirement in itself does not present a significant advantage for the three bit feedback with opamp2 because the analog noise floor is well below the quantization noise. However, the three bit feedback does have an advantage in that the best performance available is better than the best performance of the single bit feedback case because the demands made on the opamp transient response are substantially reduced.

Similar plots representing the calculated analog sources of noise and the simulated noise from opamp non-linearity as a function of the system reference voltage for the third order coders with either opamp1 (Figure 6.19) or opamp2 (Figure

6.20) are presented. They indicate that significant improvements over the third order coders are not achievable without some redesign of the opamps to achieve either:

- i) a faster transient response to reduce non-linear opamp effects at high signal levels or
- ii) lower opamp noise and lower KT/C noise to allow the signal levels to be scaled down. (lower KT/C noise also implies redesign of the opamps to drive larger capacitive loads)

Since such a redesign exceeds the scope of this thesis, the third order coders are not considered further as an immediate candidate for implementation.

To summarize then, there are three significant points to be observed from Figures 6.18 to 6.20:

- i) There is a trade off available between a high speed transient response opamp and a low noise opamp.
- ii) The selection of signal levels has an impact on coder performance even when the opamps are not fully saturating.

- iii) With the conditions considered here, the multiple bit feedback improves the coder performance in the presence of non-ideal opamps more than it degrades the coder performance in the presence of opamp noise and KT/C noise.

Figure 6.18
Second Order Coders Opamp2

Analog Sources
of Noise

SDND3 *

SDND3P2 +

SDND3P4 x

Quantization
Noise

SDND3 □

SDND3P2 △

SDND3P4 ▢

Figure 6.19
3rd Order Coders Opamp1

Analog Sources of Noise	Quantization Noise
SDND3 *	SDND3 ⊗
SDND3P2 +	SDND3P2 △
SDND3P4 x	SDND3P4 □

Figure C.20
3rd Order Coders Opamp2

Chapter 7

Conclusions and Recommendations for Further Work

7.1 Simulation Techniques

Despite attempts to find approximate or exact analytical formulae to express the in-band quantization noise, it is suggested that the best approach for arbitrary coder structures remains simulation in the time domain. The reasons for this are:

- i) the simplicity of the comparator model, and
- ii) the ability to include models for non-ideal switched capacitor integrators.

A simulation method to take into account the effects of non-ideal opamps has been developed. Its utility in evaluating the sensitivity of various coder structures to these non-ideal effects and its ability to provide results that correlate to laboratory results are demonstrated.

7.2 Coder Structures

The broad outline of this thesis can be summarized as in Figure 7.1. For example, of all the coder structures considered, SDND2P3 and seven other structures indicated in

Figure 7.1 have a single bit output. Of these eight structures, SDND2P3 shows the best performance for a second order coder and SDND3P4 shows the best performance for a third order coder. Of these two remaining structures, SDND2P3 is more suited to use with the available opamps and consequently is the structure selected for implementation.

This selection process can be described in more detail as follows. Since the scope of this thesis has been restricted to only coder structures with a single bit output, many of the new structures presented in the literature are not considered in detail. Ideal element simulations of eight coder structures selected from the literature or introduced in this thesis indicate that the best performance per opamp, for both the second and third order coders, can be obtained with the new structures introduced in this thesis. The performance per opamp is chosen as the evaluation criterion because the opamp consumes substantially more area and power than the switched-capacitor-resistors or flip-flops used to implement a FIR predictor. From the signal level results produced by the ideal circuit element simulations (Chapter 5) it could be predicted that these structures can potentially provide better performance because their reduced signal levels make the structure less sensitive to nonlinear

imperfections of the available opamps. This is confirmed by detailed simulations (Chapter 6) where opamp imperfections such as slew-rate, finite bandwidth and non-linear finite gain are included.

Although the third order structures offer the potential for the best performance overall, their performance is limited by the non-linear imperfections. For the two opamps considered, the noise and nonlinear error resulting from opamp imperfections are substantially higher than indicated by simulation with linear circuit elements. Since the non-linear effects dominate the observed noise levels, signal levels at the integrator outputs would have to be scaled down. To scale the signal levels down to the point where available opamps can be used without non-linear effects being dominant causes the analog sources of noise to dominate. This prevents any substantial improvement over a second order coder with the available opamps.

With respect to tuning the various structures, optimal tuning parameters are presented for the three second order coder structures. However, the new third order coder structures introduced in this thesis are not necessarily optimally tuned.

Figure 7.1
Summary of Coder Selection

7.3 Recommendations for Further Work

The use of internal signal level scaling has been shown as an effective method to trade off opamp slew rate limiting against opamp noise. This may allow a low signal level version of SND3P4 with correlated double sampling to reduce the impact of in-band opamp noise. It is recommended that this possibility be investigated further. If this possibility is shown to exist or if improved opamps become available, some effort to tune SDND3P4 should be undertaken using the approach outlined in Chapter 4.

Although the SD3DIP structure with single bit output is shown to be inappropriate in the context of this thesis because of its high sensitivity to analog sources of noise, in another context where this sensitivity is not a major concern, it may be further considered. Its frequency response to the input signal, low noise and known zero dc bias in the output bit stream suggest the possibility of a simplified decimation filter or echo cancellation procedure. These properties favour its use for applications requiring a zero at dc.

The new second order coder, SND2P3, is shown to have the best properties of the second order coders considered and

should be chosen for implementation. It is also recommended that this option is pursued co-operatively between Carleton Univerity and Mitel Semiconductor.

Appendix 1

Analog Sources of Noise

1.1 General

In addition to quantization noise there are also fundamental limits on noise performance imposed by thermal noise and $1/f$ noise in the opamp's and switches. These sources of noise are discussed in this appendix with the assumption that the first integration stage is the most important since noise in subsequent stages can be noise shaped in the same manner as the quantization noise.

The approach taken in this discussion is to treat the output of the first integration stage, ΔV_{01} , as a random variable sampled at the end of ϕ_1 and sampled again at the end of ϕ_2 . Each sampling action contributes to the variance of this random variable through noise from various sources. The sources of noise considered here are the in-band noise of the opamp and KT/C noise. Once the variance for each clock cycle of ΔV_{01} is known, it can be referred to the coder input by assuming a noiseless integrator and calculating the equivalent noise at the input which would produce the same variance in ΔV_{01} .

1.2 Sources of Noise

1.2.1 KT/C Noise during ϕ_1

During ϕ_1 the switches in Figure A1.1(a) on the sampling capacitors close and open, sampling a voltage V_{si} onto each sampling capacitor, C_{si} . This sampled voltage can be considered as a random variable. If we assume the noise voltage has a mean value of 0Volts, then the mean value of the sampled voltage will be V_i . Since it is usually desirable to have the bandwidth of the $R_{on}C_{si}$ time constant considerably larger than the sampling frequency, it is a suitable approximation to assume that samples of the noise voltage are uncorrelated. Then the variance of these samples is just the square of the rms noise voltage and the voltage sampled onto each capacitor is:

$$V_{si} = V_i \quad (A1.1)$$

$$\sigma_{V_{si}}^2 = V_{n1i}^2 \quad (A1.2)$$

The magnitude of the thermal noise error component for each sampling capacitor, V_{n1i} , cannot be calculated accurately without knowing the switch resistance and frequency response of the RC network but it cannot be less than KT/C_{si} for each

sampling capacitor. Thus, for an oversampled ADC, where only the fraction B/f_s of the bandwidth is used, the total in-band white noise voltage that is sampled is approximated:

$$V_{n1i} = \sqrt{\frac{kTB}{f_s C_{si}}} \quad (\text{A1.3})$$

Substituting A1.3 into A1.2 gives:

$$\sigma_{V_n}^2 = \frac{KTB}{f_s C_{si}} \quad (\text{A1.4})$$

where

f_s is the sampling frequency,
 B is the coder bandwidth,
 K is Boltzmann's constant,
 T is absolute temperature, and
 C_{si} is the value of each sampling capacitor.

It is worth while to note that this occurs before any attenuation of the signal voltage as shown in the accompanying block diagram, A1.1(b)

During ϕ_2 this sampled voltage is passed through to the output such that its effect on ΔV_{ol} is given by:

$$\Delta V_{ol} = \frac{C_{si}}{C_{fb}} V_{si} \quad (A1.5)$$

Resulting in a contribution to the variance of ΔV_{ol} of:

$$\sigma_{\Delta V_{ol}}^2 = \left(\frac{C_{si}}{C_{fb}} \sigma_{V_{si}} \right)^2 \quad (A1.6)$$

Substituting (A1.4) into (A1.6) gives the variance contributed from each sampling capacitor as:

$$\begin{aligned} \sigma_{\Delta V_{ol}}^2 &= \left(\frac{C_{si}}{C_{fb}} \right)^2 \frac{KTB}{f_s C_{si}} \\ &= \left(\frac{C_{si}}{C_{fb}} \right)^1 \frac{KTB}{f_s C_{fb}} \end{aligned} \quad (A1.7)$$

The variance contributed from all the feed forward capacitors is then:

$$\sigma_{\Delta V_{ol}}^2 = \left(\frac{C_T}{C_{fb}} \right)^1 \frac{KTB}{f_s C_{fb}} \quad (A1.8)$$

Where:

$$C_T = \sum_{i=1}^N C_{si} \quad (A1.9)$$

Consequently, it can be seen that the variance of ΔV_{ol} contributed by the sampling of the feed forward capacitors is proportional to the sum of the feed forward capacitors rather than the sum of the squares of the feed forward capacitors as might be expected.

1.2.2 Opamp Noise during $\phi 1$

At the end of $\phi 1$ the integrator is configured as shown in Figure A1.2(a) with the block diagram shown in Figure A1.2(b). Consequently the contribution to the variance caused by opamp noise sampled when the switches open is given by:

$$\sigma_{\Delta V_{ol}}^2 = V_n^2 \quad (A1.10)$$

1.2.3 KT/C Noise during $\phi 2$

Figure A1.3, shows both the sampling capacitor for the input signal and the sampling capacitor(s) for the signal fed back from the quantizer, C_{si} together with the feed back capacitor C_{fb} and opamp during $\phi 2$. The resistance of the switches can be neglected if it is assumed that the time constant formed by the switch resistance and the sampling

capacitance will be much shorter than to the sampling period. Then, similarly to section 1.2.1, the contribution to the variance of ΔV_{o1} from these sources is:

$$\sigma_{\Delta V_{o1}}^2 = \sum_{i=1}^N \left(\frac{C_{si}}{C_{fb}} \right)^2 \frac{KT B}{f_s C_{si}} \quad (\text{A1.11})$$

which reduces to

$$\sigma_{\Delta V_{o1}}^2 = \left(\frac{C_T}{C_{fb}} \right)^2 \frac{KT B}{f_s C_{fb}} \quad (\text{A1.12})$$

1.2.4 Opamp Noise during $\phi 2$

Figure A1.3 also applies to the contribution of opamp noise during $\phi 2$. As with KT/C noise during $\phi 2$, the instantaneous value of the opamp noise at the output is sampled at the end of $\phi 2$. This results in a contribution to the variance of ΔV_{o1} of:

$$\sigma_{\Delta V_{o1}}^2 = \left(\frac{C_{fb} + C_T}{C_{fb}} V_n \right)^2 \quad (\text{A1.13})$$

1.3 Refering the Noise Sources to the Input of the Coder

From the preceding sections 1.2.1 to 1.2.4 it can be seen that the total variance of the integrator output voltage, V_{o1} , will be given by adding the variances of the individual contributions. This gives:

$$\sigma_{dV_{o1}}^2 = +2 \frac{C_T}{C_{fb} f_s C_{fb}} KTB + \left(\frac{2C_{fb}^2 + 2C_T C_{fb} + C_T^2}{C_{fb}^2} \right) V_n^2 \quad (A1.14)$$

This variance can be converted to the equivalent variance at the coder input by:

$$\sigma_x^2 = \sigma_{dV_{o1}}^2 \left(\frac{C_{fb}}{C_1} \right)^2 \quad (A1.15)$$

$$\sigma_x^2 = +2 \frac{C_T}{C_1 f_s C_1} KTB + \left(\frac{2C_{fb}^2 + 2C_T C_{fb} + C_T^2}{C_1^2} \right) V_n^2$$

It can be observed at this point that each of the two terms in (A1.15) contain a part that depends on capacitor ratios and a part that depends on minimum capacitor size in the case of KT/C noise or opamp noise. If a coder structure is to be implemented with a given set of opamps and a given minimum capacitor size, the the capacitor ratio part of each term can be used as a figure of merit to compare coder structures. If α_{nn1} is defined as the sensitivity of a coder

structure to KT/C noise based on the coder input sampling capacitance and α_{nn2} is defined as the sensitivity of a coder structure to opamp noise, then (A1.15) can be rewritten as:

$$\sigma_X^2 = +(\alpha_{nn1} V_{nt})^2 + (\alpha_{nn2} V_n)^2 \quad (A1.16)$$

Where

$$\alpha_{nn1} = \sqrt{\frac{2C_T}{C_1}}$$

$$\alpha_{nn2} = \sqrt{\frac{2C_{fb}^2 + 2C_T C_{fb} + C_T^2}{C_1^2}}$$

$$V_{nt} = \sqrt{\frac{KT B}{f_s C_1}}$$

V_n = the in-band noise of the opamp.

When considering the effects of signal level scaling on the analog sources of noise discussed in this appendix, it should be noted that in the first stage of the coder, C_{fb} is the capacitor that is increased to scale down the signal level. Thus the input referred KT/C noise is not affected by signal level scaling. However, the input referred opamp noise is amplified in proportion to the square of C_{fb} , and hence the

signal level scaling, once $C_{fb} \gg C_T$.

It can also be enlightening to substitute the block diagram gains, defined in terms of capacitor ratios in section 3.2, into (A1.16). This gives:

$$\alpha_{nn1} = \sqrt{2 \left(\frac{V_1}{V_r G_1} + 1 \right)} \quad (\text{A1.17})$$

$$\alpha_{nn2} = \frac{1}{G_1} \sqrt{2 + 2 \left(\frac{V_1}{V_r} + G_1 \right) + \left(\frac{V_1}{V_r} + G_1 \right)^2}$$

This form of the equations for α_{nn1} and α_{nn2} highlight the advantage of keeping the physical reference voltage, V_r , large for a given system reference voltage, V_1 .

Figure A1.1 (a)
Circuit Diagram of the Voltage Sampled at the end of $\phi 1$

Figure A1.1 (b)
Block Diagram of the Voltage Sampled at the end of $\phi 1$

Figure A1.2 (a)
Circuit Diagram of the Opamp Noise Sampled at the end of ϕ_1

Figure A1.2 (b)
Block Diagram of the Opamp Noise Sampled at the end of ϕ_1

Figure A1.3 (a)
Circuit Diagram of the KT/C Noise Sampled at the end of ϕ_2

Figure A1.3 (b)
Block Diagram of the KT/C Noise Sampled at the end of ϕ_2

Appendix 2

Tuning of the Second Order Coder Structures

Since the second order coders considered have only one degree of freedom, it is convenient to do a coarse tuning by varying G_2 and observing the resulting signal to noise ratio and signal levels. Simulation results for the three second order coder structures with a reference voltage sufficiently low that integrator saturation is not a consideration. The details of the simulation are:

Reference Voltages	$V_1=V_2=0.25V,$
Input Gain	$G_1=1/6,$
Input Sinusoid Amplitude	$1V_p,$
Input Sinusoid Frequency	$35kHz,$ and
Sampling Frequency	$10.24MHz.$

Each point in the accompanying graphs represents the average of three values of SNR or signal level results. The SNR is determined from a 2Ksample FFT with a rectangular window and the bandwidth for noise integration ideally (ie "brick wall") low pass filtered at 80kHz.

The optimal tuning for SDD2 appears to occur when $G2=0.5$ as claimed by Lamkemeyer et al[11]. The signal levels increase rapidly for higher values of $G2$ and the performance drops off rapidly.

For SDND2 $G2=1.0$ appears to provide the best compromise of characteristics. Although the performance continues to improve for larger values of $G2$ and, surprisingly, the signal levels in the first integrator continue to decrease, the signal levels in the second integrator increase as $G2$ increases and the performance improvement becomes marginal. This is consistent with the value of $G2$ used by Candy[2]

Similarly, $G2=0.5$ provides a compromise for SDND2P3. For higher values of $G2$, the change in voltage at the output of the first integrator starts to increase rapidly and the performance improvements become marginal for $G2>0.5$.

Figure A2.1
Quantization Noise Vs G2

Figure A2.2
Vol vs G2

Figure A2.3
dVol vs G2

Figure A2.4
Vo2 vs G2

Figure A2.5
 $dVo2$ vs $G2$

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