Components for Receiver Front-Ends in SiGe Bipolar Technology

by

John W. M. Rogers, B. Eng., M.Eng., P. Eng.

A Thesis submitted to
the Faculty of Graduate Studies and Research
in partial fulfillment of the requirements for the degree of
Doctor of Philosophy

Department of Electronics
Carleton University
Ottawa, Ontario

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submitted by

John W. M. Rogers, B. Eng., M. Eng, P. Eng.

In partial fulfillment of
The requirements for the degree of
Doctor of Philosophy

Dr. Sorin Voinigescu
External Examiner

Professor Calvin Plett, Ph. D., P.Eng.
Thesis Supervisor

Professor Michel S. Nakhla, Ph. D.
Chair, Department of Electronics

Carleton University
Ottawa, Canada
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Abstract

In this thesis, techniques for reducing the supply voltage and for raising the level of integration of SiGe RFICs are studied. Methods for making circuits more robust through the use of feedback have been implemented in both VCOs and high frequency filters. This research has resulted in an improved understanding of the principles of operation of many of these circuits.

Specifically, this work discusses the design of LNAs, VCOs, filters, and mixers for 5GHz radio applications at 1.8V. A notch filter with automatic Q tuning is integrated with the LNA to provide the opportunity for image rejection. The receiver had a gain of 19.8dB, noise figure of 4.5dB, and an IIP3 of -23dBm . The VCO featured a tuning range of 600MHz and had a free running phase noise of -115.8dBc/Hz at 1MHz offset.

Detailed analysis of the operation of the notch filter was undertaken including a study of the mechanisms determining its linearity, noise performance and stability. As well, a method for automatically Q tuning the filter was analyzed and implemented to demonstrate this concept.

Also VCOs with automatic amplitude control loops were studied as the basis for the Q-tuning loop used in the filter. The detailed operation of these loops is presented along with methods to design the loops for best possible performance. VCOs topologies were also optimized for low voltage operation. The VCO work also led to a study of how phase noise is generated in these circuits, ways to better understand it, and finally how to minimize its effect on the circuit.

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Abbreviations

AC	Alternating Current
Al	Aluminum
BJT	Bipolar Junction Transistor
CAD	Computer Aided Design
DC	Direct Current
F	Noise Factor
FM	Frequency Modulation
f_t	Unity Gain Frequency
GHz	Giga-Hertz
G_m	Transistor Transconductance
K	Boltzmann's Constant
K_{vco}	VCO Gain
IC	Integrated Circuit
IR	Image Rejection
μm	Micron or micrometer
NF	Nose Figure
PLL	Phase Locked Loop
PN	Phase Noise
Q	Quality Factor
r_e	Dynamic Emitter Resistance
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
Si	Silicon
SNR	Signal to noise ratio
VCO	Voltage Controlled Oscillator

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Chapter 1: Introduction

In recent years, in many different parts of the IC community, there has been a trend to reduce the supply voltage of many products. The benefits from lowering the supply voltage should be obvious. If a certain current is needed to perform a certain function, then if that current is drawn from a lower supply voltage, less power is used. For CPUs, this means that less heat is generated, for RF circuits this means that circuits consume less power, which translates into longer battery life.

Unfortunately, it tends to be very hard to lower the supply voltage for RF circuits. Many traditional topologies for common building blocks have several stacked transistors setting a lower limit on the voltage that can be used with such circuits. As an example, the Gilbert Cell Mixer usually has a current source, a driver transistor, a set of switching transistors, and a resistive load all stacked on top of each other. This, along with many other examples, illustrates that some innovation is required if the supply voltage of RF circuits is to be dropped significantly from the now common 3.3 volts. Of course, the transistors themselves will set a lower limit on the supply that can be used. Knowing that the turn on voltage for most typical modern high-speed bipolar transistors is around 0.85 volts, it would be very difficult to design circuits with a supply lower than this value. As well, some “head room” is always required. Thus, a reasonable target would be about 1.8 volts.

Along with lower supply voltages, there is also a push towards higher frequencies as Si technology becomes faster. With the introduction of SiGe at the time of writing this document, it is not uncommon for production technologies to have f_T s higher than 50 GHz with over 200 GHz and beyond on the horizon. Along with the additional problems that higher frequencies present to the RF designer, there are also new alternatives. With receivers in the 2 GHz band, on-chip inductors and transformers are now quite realizable. As circuits progress to the 5 GHz band and beyond, inductors and transformers will become smaller and will improve in quality.

In this thesis, topologies for a low voltage LNA, Mixer, and VCO will be presented. As well, a completely integrated 5 GHz, 1.8volt superheterodyne receiver using these components has been fabricated. The job of image rejection (normally performed by off-chip SAW filters, image reject mixers or an active filter stage) will be part of the LNA, which will incorporate novel image rejection. This will reduce the current that would have to be delegated to an on-chip image filter or image reject mixer and will eliminate the need for the off-chip SAW filter. Such notch filters, if implemented on-chip, typically have poor linearity and noise figure. So the use of an LNA to perform this function, which can be made to have superior linearity and noise performance, will also reduce these difficulties.

The need for optimal performance of VCOs and image filters will be paramount to the performance of the receiver. Thus, feedback circuits to tune the VCO for optimal noise performance were developed. These circuits that set the VCO to optimal levels were also used to automatically tune the notch filter for maximum image rejection.

In order to properly implement these feedback circuits, they must be properly understood. Thus a detailed analysis of the important aspects of their design is presented, including feedback stability, and the advantages and disadvantages of the two techniques are outlined.

The filters and VCOs themselves must also be properly understood. Therefore the operation of the filter is explored in detail including limits on the amount of image rejection that can be expected, stability issues, noise issues and linearity constraints. Although the basic structures and operation of VCOs are generally known, a few points need to be clarified about their operation. Specifically, the effect of nonlinearity in the device on phase noise will be analyzed in detail. As well, a non-empirical formula for the “noise figure” of the transistor amplifier in the oscillator will be derived and presented.

1.1 Review of Some Previous Work

Recently there has been a lot of activity aimed at reducing the supply voltages of RF circuits and systems. The following references summarized in Table I are intended to give a flavor for the state of the art in the industry.

Table I: Summary of Some Recently Published Receivers

Ref	Supply (V)	Gain (dB)	IIP3 (dBm)	Power (mW)	NF (dB)	Frequency Band	Image rejection	Tech-nology	Phase Noise
[46]	0.9/1.8	14	-5.5	24/18.5	6.8	5GHz	36dB	SiGe Bipolar	N/A
[16] [49]	2	12	-2.0	37.4	5.3	5GHz	12dB	0.24 μ m CMOS	-101dBc/Hz @ 1MHz
[47]	2	54	-6.0	191	6.5	2GHz	32.2dB	0.25 μ m CMOS	-126dBc/Hz @ 1MHz
[48]	0.5-1	10 (LNA) 7 (Mixer)	-6.0 (Mixer)	18	3.5 (LNA) 16.1 (Mixer)	2GHz	N/A	0.2 μ m CMOS SOI	-110dBc/Hz @ 1MHz
[50]	1	13.5	-4.0	35	1.8 (LNA) 12 (Mixer)	2GHz	Off Chip SAW	0.5 μ m CMOS	N/A

Reference [46] deals with a low-voltage image-reject down converter consisting of an LNA and mixer stage. In this paper, the supply voltage of the mixer stage is reduced to a minimum of 0.9V by the clever use of on chip transformers to replace the driver transistors. Two versions of the receiver were built. One had a supply voltage of 1.8V and the other used a supply of 0.9V. Both used an image-reject mixer to provide image rejection. The 1.8V version used a balanced Gilbert cell mixer stage, while the 0.9V version was forced to use an unbalanced topology due to biasing constraints.

Reference [16] and [49] deal with a low voltage receiver front-end and companion synthesizer designed for wireless LAN applications. This receiver uses an on-chip image reject filter which is a 5GHz implementation of the one originally presented in [13]. The filter does not address the Q tuning issue. The frequency of the filter is adjusted using the

technique presented in [14] which uses the PLL tuning voltage for the filter as well as the VCO. This filter is quoted as providing only 12dB of image rejection. As well, a method for improving the NF of the cascode LNA topology is also presented by resonating out parasitic capacitance. The VCO was a fairly standard cross coupled structure and used inductors with ground shields.

Reference [47] deals with a transceiver architecture. There is a lot of IF circuitry on the chip as well as the RF, which accounts for the high gain and power consumption. This receiver also uses an image-reject mixer topology to provide image rejection. The VCO is implemented as a cross-coupled $-G_m$ topology using only PMOS transistors.

Reference [48] deals with some circuit blocks in SOI technology. The paper title claims that the circuits can operate down to 0.5V, however most of the performance levels are quoted at 1V. The LNA is a standard common-source configuration, and the VCO is a cross coupled $-G_m$ topology with PMOS switches and a current source applied from the rail. The mixer is a folded cascode structure where an LC tank is placed in the emitters of the switching transistors to provide a high impedance at RF without any DC voltage drop.

Reference [50] presents a more classic LNA and mixer separated by an off chip SAW filter in a standard CMOS process. The circuits have very high linearity and operate at very low voltage. Both the LNA and mixer use folded-cascode structures where an LC tank is used as an RF choke.

1.2 Outline

Issues of designing LNAs and specifically how they will be made to operate at 1.8 volt are discussed in Chapter 2 of this thesis. Mixers and techniques to make them operate with very low supply voltages will be discussed in Chapter 3. The implementation of inductors and transformers in SiGe technology will be discussed in Chapter 4. These components while non-trivial to realize in IC technologies, are nonetheless essential for

low voltage operation of RF circuits. Basic VCO theory, and how to implement them as completely integrated components, will be discussed in Chapter 5. Some issues about phase noise will be discussed as well as methods of automatic amplitude control. The problem of image rejection in superheterodyne receivers will be discussed in Chapter 6. Common ways of dealing with this problem will be reviewed. Then the use of notch filters to perform this function will be considered. As well, an automatic Q tuning scheme will be presented. Results for various experiments conducted to support this research will be discussed in Chapter 7. Conclusions and a summary of the research will be presented in Chapter 8.

Chapter 2: Low Voltage LNA Topology

The low noise amplifier is the first block in most receiver front-ends. Its job is to amplify the signal while introducing a minimum amount of noise to the signal. LNAs usually also provide some amount of filtering as they amplify signals over a relatively narrow band.

2.1 Common LNA Topologies

The two most common configurations for RF LNAs are the common-emitter configuration and the cascode configuration shown in Fig. 1. In most applications the cascode is preferred over the common-emitter topology because it can be used at higher frequencies (the extra transistor acts to reduce the Miller Effect), has superior reverse isolation (S_{12}), and is less prone to oscillations. However, the cascode also suffers from reduced linearity due to the stacking of two transistors, which reduces the available output swing and reduced noise performance.

Most LNAs employ inductive degeneration as shown in both of these figures. The purpose of this inductor is to provide a means to transform the real part of the impedance seen looking into the base to a higher impedance for matching purposes. This inductor also trades gain for linearity as the inductor is increased in size.

Fig. 1. The common-emitter and cascode configuration.

2.2 LNA Gain and Input Impedance

The gain of either amplifier at the resonance frequency of the tank in the collector, ignoring the effect of C_{μ} , is found with the aid of Fig. 2 and is given by:

$$\frac{v_{out}}{v_{in}} = \frac{-g_m R_L}{\left(1 + \frac{Z_e}{Z_{\pi}} + g_m Z_e\right)} \approx -\frac{R_L}{Z_e} \quad (1)$$

where Z_e is the impedance of the emitter degeneration. Here it is assumed that the impedance in the emitter is a complex impedance. Thus, as the degeneration becomes larger, the gain ceases to depend on the transistor parameters and becomes solely dependent on the ratio of the two impedances. This is one of the advantages of this type of feedback. Another advantage is that the circuit becomes less sensitive to temperature and process variations.

Alternatively, the gain can be written out in terms of source resistance and f_T . v_{out} can be given by:

$$v_{out} = -g_m v_{\pi} R_L = -g_m i_x Z_{\pi} R_L \quad (2)$$

Noting that i_x can also be equated to the source resistance R_s as $i_x = v_{in}/R_s$:

$$\frac{v_{out}}{v_{in}} = \frac{-g_m Z_\pi R_L}{R_s} \quad (3)$$

assuming that Z_π is primarily capacitive at the frequency of interest:

$$\left| \frac{v_{out}}{v_{in}} \right| = \frac{g_m R_L}{R_s \omega_o C_\pi} = \frac{R_L \omega_T}{R_s \omega_o} \quad (4)$$

The input impedance, again ignoring C_μ is given by:

$$Z_{in} = Z_\pi + Z_E(1 + g_m Z_\pi) \quad (5)$$

Of particular interest is the product of Z_E and Z_π . If the impedance Z_E is inductive, then when this is reflected into the base, this will become a real resistance. Thus, placing an inductor in the emitter tends to raise the input impedance of the circuit. Likewise, placing a capacitor in the emitter will tend to reduce the input impedance of the circuit and can even make it negative. Thus, placing an inductor in the emitter is very useful for matching purposes.

Fig. 2. Small-signal model used to find the input impedance.

2.3 Noise in LNAs

When the signal is first received by the radio it can be quite weak and can be in the presence of a great deal of interference. Therefore, it is essential that the LNA, which is the first part of the radio to process the signal, amplify the signal while adding a minimal amount of additional noise to it. Thus, one of the most important considerations when designing an LNA is the amount of noise present in the circuit. The following subsections discuss this important topic.

2.3.1 Basic Noise Model of the Bipolar Transistor

Ignoring flicker noise, there are three major sources of noise in a bipolar transistor. They are the base resistance, the base shot noise and the collector shot noise [1]. A simplified model for the HBT including these noise sources is shown in Fig. 3. Note that other noise sources are also present, for example emitter and collector resistance, however these noise sources often have a smaller effect and will be ignored for simplicity.

Fig. 3. An HBT model with basic noise sources.

The base resistance noise source in a bandwidth Δf is given by:

$$v_{bn}^2 = 4kTr_b\Delta f \quad (6)$$

where k is Boltzmann's constant, and T is the temperature of the circuit.

The base and collector shot noise are given by:

$$\begin{aligned} i_{bn}^2 &= 2qI_B\Delta f \\ i_{cn}^2 &= 2qI_C\Delta f \end{aligned} \quad (7)$$

where q is the charge on an electron, I_B is the quiescent base current and I_C is the quiescent collector current.

2.3.2 The Noise Figure of a Circuit

One of the most common figures of merit used to describe how noisy or quiet a circuit is, is its noise figure (NF) or noise factor (F). F can be defined as the ratio of the signal-to-noise ratio (SNR) at the input to the SNR at the output. NF is the logarithm of this value:

$$NF = 10 \log(F) = 10 \log \left(\frac{SNR_{in}}{SNR_{out}} \right) \quad (8)$$

For the purposes of developing equation (8) into a more useful form, it is assumed that all practical amplifiers can be characterized by an input referred noise model such as the one shown in Fig. 4. All noise sources in the circuit are lumped into a series noise voltage source and a parallel current noise source placed in front of a noiseless transfer function.

Fig. 4. Input-referred noise model for a device.

If the circuit has finite input impedance, then the input current will be split by some ratio α flowing into the circuit and $(1-\alpha)$ source admittance G_S :

$$SNR_{in} = \frac{\alpha^2 i_{in}^2}{\alpha i_{ns}^2} \quad (9)$$

Now the output signal to noise ratio can be found. Here it has been assumed that the input referred noise sources are correlated:

$$SNR_{out} = \frac{\alpha^2 A_i^2 i_{in}^2}{\alpha^2 A_i^2 (i_{ns}^2 + |i_n + v_n Y_s|^2)} \quad (10)$$

Thus, the noise factor can now be written in terms of the preceding two equations:

$$F = \frac{i_{ns}^2 + |i_n + v_n Y_s|^2}{i_{ns}^2} = \frac{N_{otot}}{N_{osource}} \quad (11)$$

which can also be interpreted as the ratio of the total output noise to the total output noise due to the source admittance.

In equation (11) it was assumed that the two input noise sources were correlated with each other. In general they will not be correlated with each other, but rather the current i_n will be partially correlated with v_n and partially uncorrelated. We can expand both current and voltage into these two explicit parts:

$$i_n = i_c + i_u \quad (12)$$

$$v_n = v_c + v_u \quad (13)$$

In addition, the correlated components will be related by the ratio:

$$i_c = Y_c v_c \quad (14)$$

The noise figure can now be written as:

$$NF = 1 + \frac{\overline{i_u^2} + |Y_c + Y_s|^2 \overline{v_c^2} + \overline{v_u^2} |Y_s|^2}{i_{ns}^2} \quad (15)$$

The noise currents and voltages can also be written in terms of equivalent resistance and admittance:

$$R_c = \frac{\overline{v_c^2}}{4kT\Delta f} \quad (16)$$

$$R_u = \frac{\overline{v_u^2}}{4kT\Delta f} \quad (17)$$

$$G_u = \frac{\overline{i_u^2}}{4kT\Delta f} \quad (18)$$

$$G_s = \frac{\overline{i_{ns}^2}}{4kT\Delta f} \quad (19)$$

Thus, the noise figure is now written in terms of these parameters:

$$NF = 1 + \frac{G_u + |Y_c + Y_s|^2 R_c + |Y_s|^2 R_u}{G_s} \quad (20)$$

$$NF = 1 + \frac{G_u + [(G_c + G_s)^2 + (B_c + B_s)^2] R_c + [G_s^2 + B_s^2] R_u}{G_s} \quad (21)$$

It can be seen from this equation that NF is dependent on the source impedance used in the measurement system. By convention this is usually 50Ω.

It is of interest to minimize the noise figure of an LNA. Thus, the source loading conditions that will provide the lowest possible noise figure can be determined from (20). Differentiating with respect to G_s and B_s and setting the derivative to zero yields the following two conditions for minimum noise (G_{opt} and B_{opt})...after several pages of calculus:

$$G_{opt} = \sqrt{\frac{G_u + R_u \left(\frac{R_c B_c}{R_c + R_u} \right)^2 + G_c^2 R_c + \left(B_c - \frac{R_c B_c}{R_c + R_u} \right)^2 R_c}{R_c + R_u}} \quad (22)$$

$$B_{opt} = \frac{-R_c B_c}{R_c + R_u}$$

2.3.3 Input Referred Noise Model of the Bipolar Transistor

The preceding section made use of an idealized model for an amplifier with two noise sources at the input (Fig. 4). If the model is to be applied to an actual LNA then all the noise sources must be written in terms of these two input referred noise sources as shown in Fig. 5. Starting with the model shown in Fig. 5A and assuming that the emitter is grounded with base input and collector output, the model may be determined with some analysis.

A) Physical Noise Model

B) Input Referred Noise Model

Fig. 5. Noise model for the bipolar transistor and equivalent input referred noise model.

When the input is shorted in Fig. 5B, then only the effect of v_n can be seen at the output. In this case, v_n is the only source of noise that matters (all the current from i_n is shorted to

ground) in the model, then the output noise would be (assuming that r_b is small enough to not affect the gain):

$$\overline{i_{on_tot}^2} = \overline{v_n^2} g_m^2 \quad (23)$$

Using the model in Fig. 5A and also assuming that the input is grounded leads to an output current of:

$$\overline{i_{on_tot}^2} = \overline{v_{bn}^2} g_m^2 + \overline{i_{cn}^2} \quad (24)$$

We wish to make these two models equivalent, so we set (23) equal to (24) and solve for v_n giving:

$$\overline{v_n^2} = \frac{2qI_c}{g_m^2} + 4kTr_b \quad (25)$$

where $\overline{v_{bn}^2} = 4kTr_b$ and $\overline{i_{cn}^2} = 2qI_c$. Now if the input is open circuited in Fig. 5B then only i_n can have any effect on the circuit. In this case the output noise is:

$$\overline{i_{on_tot}^2} = \overline{i_n^2} Z_\pi^2 g_m^2 \quad (26)$$

Similarly for the model in Fig. 5A:

$$\overline{i_{on_tot}^2} = \overline{i_{bn}^2} Z_\pi^2 g_m^2 + \overline{i_{cn}^2} \quad (27)$$

now solving (26) and (27) for i_n gives:

$$\overline{i_n^2} = 2qI_B + \frac{2qI_c}{g_m^2} Y_\pi^2 \quad (28)$$

where $\overline{i_{bn}^2} = 2qI_B$ and $\overline{i_{cn}^2} = 2qI_c$.

2.3.4 Noise Figure of the Bipolar Transistor Amplifier

Now that the equivalent input referred noise model has been derived it can be applied to the results in the previous section so that the optimum impedance for noise can be found in terms of transistor parameters.

The input referred noise current i_n given in (28) has two terms. One is due to base shot noise and one is due to collector shot noise. The input noise voltage v_n given in (25) also

has two terms. One is due to collector shot noise and the other is due to base resistance. Since collector shot noise is present in the expressions for both v_n and i_n , this part of the input noise current is correlated with the input noise voltage, but the other part of the input current i_n is not. Thus:

$$\overline{i_c^2} = \frac{2qI_C}{g_m^2} Y_\pi^2 \quad (29)$$

$$\overline{i_u^2} = 2qI_B \quad (30)$$

Likewise in the case of the v_n :

$$\overline{v_c^2} = \frac{2qI_C}{g_m^2} \quad (31)$$

$$\overline{v_u^2} = 4kTr_b \quad (32)$$

Now Y_c can be determined. It will be assumed that at the frequencies of interest the transistor looks primarily capacitive.

$$Y_c = \frac{i_c}{v_c} = \sqrt{\frac{\frac{2qI_C}{g_m^2} Y_\pi^2}{\frac{2qI_C}{g_m^2}}} = Y_\pi \approx j\omega C_\pi \quad (33)$$

where it is assumed that r_π is not significant at the frequencies of interest. Explicitly if $Y_c = G_c + jB_c$ then:

$$\begin{aligned} G_c &\approx 0 \\ B_c &= \omega C_\pi \end{aligned} \quad (34)$$

Thus the correlation admittance is just equal to the input admittance of the transistor.

R_c , R_u , and G_u can also be written down directly.

$$R_c = \frac{\overline{v_c^2}}{4kT} = \frac{2qI_C}{4kTg_m^2} = \frac{V_T}{2I_C} = \frac{r_e}{2} \quad (35)$$

$$R_u = \frac{\overline{v_u^2}}{4kT} = \frac{4kTr_b}{4kT} = r_b \quad (36)$$

$$G_u = \frac{\overline{i_u^2}}{4kT} = \frac{2qI_B}{4kT} = \frac{I_C}{2V_T\beta_o} = \frac{g_m}{2\beta_o} = \frac{1}{2r_\pi} \quad (37)$$

Using these equations an explicit expression for the noise figure can be now written in terms of circuit parameters:

$$NF = 1 + \frac{\frac{I_C}{2V_T\beta_o} + [G_s^2 + (\omega C_\pi + B_s)^2] \frac{V_T}{2I_C} + (G_s^2 + B_s^2) \cdot r_b}{G_s} \quad (38)$$

These equations also lead to expressions for G_{opt} and B_{opt} [2]:

$$G_{opt} = \sqrt{\frac{\frac{I_C}{2V_T\beta_o} + r_b \left(\frac{-\frac{V_T}{2I_C}(\omega C_\pi)}{\frac{V_T}{2I_C} + r_b} \right)^2 + \frac{V_T}{2I_C} \left(\omega C_\pi - \frac{\frac{V_T}{2I_C}(\omega C_\pi)}{\frac{V_T}{2I_C} + r_b} \right)^2}{\frac{V_T}{2I_C} + r_b}} \quad (39)$$

$$B_{opt} = \frac{-\frac{V_T}{2I_C}(\omega C_\pi)}{\frac{V_T}{2I_C} + r_b} \quad (40)$$

Thus G_{opt} will vary with the size of the device used. At some point it would equal $1/50\Omega$.

Thus for that size device, matching to 50Ω would also give best noise figure.

The expression for B_{opt} can be simplified if r_b is small compared to $r_e/2$. This would be a reasonable approximation over most normal operating points for a fairly large transistor:

$$B_{opt} \approx -\omega C_\pi = -\text{Im}(Z_{in}) \quad (41)$$

Thus it can be seen that the condition for maximum power transfer (resonating out the reactive part of the input impedance) is the same as the condition for providing optimal noise matching. Hence the following method can be used for matching an LNA.

2.4 Input Matching of LNAs

Since the LNA is the first component in the receiver chain, the input must be matched to drive 50Ω . Many methods for matching the input using passive circuit elements are possible with varying bandwidths and degrees of complexity, however one of the most elegant is described in [2]. The procedure is as follows:

- 1) Find the current density (current per unit of emitter area) in the process that will provide the lowest minimum NF, and set the current density in the driving transistor (Q1 in Fig. 1) to be this value regardless of the size of the device. The minimum NF for a process can be found from device measurements, but for the circuit designer, it is available from simulators like HPADS or SPICE once the models are available.
- 2) Once the current density is known, then the length of the transistor l_e should be sized so that the real part of the optimum source impedance for lowest noise figure is equal to 50Ω . If in the technology of interest, scalable models are not available, the discrete transistor that comes closest to fulfilling this requirement must be chosen. Current must be adjusted in this step to keep the current density at its optimal level determined in step 1.
- 3) Size L_{e1} , the emitter degeneration inductor, such that the real part of the input impedance is 50Ω . The use of inductive degeneration will tend to increase the real part of the input impedance. Thus, as this inductor is increased the impedance will at some point have a real part equal to 50Ω .
- 4) The last step in the matching is simply to place an inductor in series with the base. Without this inductor, the input impedance is capacitive due to C_π even with the presence of the inductor in the emitter. This inductor is sized so that it self resonates with the capacitance presented by the base at the center frequency of the design. This makes the resultant input impedance equal to 50Ω with no additional reactive component.

The technique above has several advantages over a more traditional two-component match. It is simple and requires only one additional matching component in series with the input of the transistor. It produces a relatively broad band match, and it achieves simultaneous noise and power matching of the transistor. This makes it a preferred method of matching.

There are many instances where this method cannot be applied without modification. For some designs, power constraints may not allow for the necessary current to achieve the best noise performance. In this case the design could proceed as before except with a less than optimum current density or with a transistor for which optimum noise resistance is bigger than 50Ω . In other cases the design may not provide the necessary gain required for some applications. In this case more current may be needed, or some other matching technique may have to be employed that does not require that degeneration be used. As well, linearity constraints may demand a larger amount of degeneration than this method would lead to.

2.5 Linearity in LNAs

In a perfect amplifier the output is linearly related to the input. However, in any real device the transfer function is usually a lot more complicated. This can be due to active or passive devices in the circuit, or signal swing being limited by the power supply rails. Unavoidably, the gain curve for an amplifier is never a perfectly straight line, as illustrated in Fig. 6.

Fig. 6. Illustration of the nonlinearity in an amplifier.

Mathematically any nonlinear transfer function can be written as a series expansion of power terms

$$v_{out} = k_0 + k_1 v_{in} + k_2 v_{in}^2 + k_3 v_{in}^3 + \dots \quad (42)$$

To perfectly describe the nonlinearity, an infinite number of terms is required, however in many practical circuits the first three terms are sufficient to characterize the circuit with a fair degree of accuracy.

One common way of characterizing the linearity of a circuit is called the two tone test. In this test an input consisting of two sine waves is applied to the circuit.

$$v_{in} = v_1 \cos \omega_1 t + v_2 \cos \omega_2 t \quad (43)$$

When this tone is applied to the transfer function given in (42), the result is a number of terms[3] summarized in Table II:

Table II: Frequency components generated by a nonlinearity.

Frequency	Component Amplitude
DC	$k_0 + \frac{k_2}{2}(v_1^2 + v_2^2)$
ω_1	$k_1 v_1 + k_3 v_1 \left(\frac{3}{4} v_1^2 + \frac{3}{2} v_2^2 \right)$
ω_2	$k_1 v_2 + k_3 v_2 \left(\frac{3}{4} v_2^2 + \frac{3}{2} v_1^2 \right)$
$2\omega_1$	$\frac{k_2 v_1^2}{2}$
$2\omega_2$	$\frac{k_2 v_2^2}{2}$
$\omega_1 \pm \omega_2$	$k_2 v_1 v_2$
$\omega_2 \pm \omega_1$	$k_2 v_1 v_2$
$3\omega_1$	$\frac{k_3 v_1^3}{4}$
$3\omega_2$	$\frac{k_3 v_2^3}{4}$

$2\omega_1 - \omega_2$	$\frac{3}{4}k_3v_1^2v_2$
$2\omega_2 - \omega_1$	$\frac{3}{4}k_3v_1v_2^2$

Of all the above unwanted terms the last two are the most troublesome, since they fall in the band of the desired outputs and cannot be easily filtered out. These two tones are usually referred to as third order intermodulation terms (IM3 products).

For most linearity tests, the two inputs are set to the same amplitude. Therefore if $v_1=v_2=v_i$, then the fundamental is given by:

$$fund = k_1v_i + \frac{9}{4}k_3v_i^3 \quad (44)$$

For small signals this can be approximated as:

$$fund = k_1v_i \quad (45)$$

The intermodulation terms are given by:

$$IM3 = \frac{3}{4}k_3v_i^3 \quad (46)$$

Note that for small v_i the fundamental rises linearly (20dB/dec) and that the IM3 terms rise as the cube of the input (60dB/dec). Thus, a theoretical voltage where these two tones will be equal (referred to as the third order IM3 intercept point) can be defined:

$$\frac{\frac{3}{4}k_3v_{IP3}^3}{k_1v_{IP3}} = 1 \Rightarrow v_{IP3} = 2\sqrt{\frac{k_1}{3k_3}} \quad (47)$$

This point cannot actually be measured, due to the fact that by the time this point was reached, the amplifier would have long since stopped working properly. Therefore, it is useful to describe a quick way to extrapolate it at a given power level.

Fig. 7. Distortion for Varying Power Levels

Assume that a device with power gain G has been measured to have an output power at the fundamental frequency of P_1 and a power at the IM3 frequency of P_3 for a given input power of P_i , as illustrated in Fig. 7. Further assume that OIP3 is the power of the third order intermodulation point at the output and IIP3 is the power of the intermodulation point at the input. Now, on a log plot (for example when power is in dBm) of P_3 and P_1 versus P_i , the IM3 terms have a slope of three and the fundamental terms have a slope of one. Therefore:

$$\frac{OIP3 - P_1}{IIP3 - P_i} = 1 \quad (48)$$

$$\frac{OIP3 - P_3}{IIP3 - P_i} = 3 \quad (49)$$

and also noting that:

$$G = OIP3 - IIP3 = P_1 - P_i \quad (50)$$

These equations can be solved to give:

$$IIP3 = P_1 + \frac{1}{2}[P_1 - P_3] - G \quad (51)$$

2.5.1 Exponential Nonlinearity in the Bipolar Transistor

In bipolar transistors one of the most important nonlinearities present is the basic exponential characteristic of the transistor itself. The basic stage to be considered is shown in Fig. 8.

Fig. 8. Bipolar transistor with degeneration to improve IIP3.

The transistor base has a bias applied to it and an ac signal superimposed. Summing the voltages in the base emitter path:

$$v_s + V_S = v_{be} + V_{BE} + R_E(I_C + i_c) \quad (52)$$

where V_{BE} and v_{be} are the DC and ac voltages across the base emitter junction of the transistor.

Extracting only the small signal components from this equation gives:

$$v_s = v_{be} + R_E i_c \quad (53)$$

Also, from the basic properties of the junction[1]:

$$I_C + i_c = I_S e^{\frac{V_{BE} + v_{be}}{V_T}} = I_S e^{\frac{V_{BE}}{V_T}} e^{\frac{v_{be}}{V_T}} = I_C e^{\frac{v_{be}}{V_T}} \quad (54)$$

solving (54) for v_{be} gives:

$$v_{be} = V_T \ln \left(1 + \frac{i_c}{I_C} \right) \quad (55)$$

now making use of the math identity:

$$\ln(1+x) = x - \frac{1}{2}x^2 + \frac{1}{3}x^3 \dots \quad (56)$$

and taking (55) and expanding it, using (56) and substituting it back into (53) we get:

$$v_s = R_E i_c + v_T \left[\frac{i_c}{I_C} - \frac{1}{2} \left(\frac{i_c}{I_C} \right)^2 + \frac{1}{3} \left(\frac{i_c}{I_C} \right)^3 \dots \right] \quad (57)$$

Noting that $v_T/I_C = r_e$ and rearranging we get:

$$v_s = (R_E + r_e) i_c - \frac{1}{2} r_e \frac{i_c^2}{I_C} + \frac{1}{3} r_e \frac{i_c^3}{I_C^2} \dots \quad (58)$$

This can be further manipulated to give:

$$\frac{v_s}{(R_E + r_e)} = i_c - \frac{1}{2} \frac{r_e}{(R_E + r_e)} \frac{i_c^2}{I_C} + \frac{1}{3} \frac{r_e}{(R_E + r_e)} \frac{i_c^3}{I_C^2} \quad (59)$$

This is the equation that we need, but it is in the wrong form. It needs to be solved for i_c .

Thus, a couple more relationships are needed. Given:

$$y = a_1 x + a_2 x^2 + a_3 x^3 \quad (60)$$

the following can be found:

$$x = b_1 y + b_2 y^2 + b_3 y^3 \quad (61)$$

where:

$$\begin{aligned} b_1 &= \frac{1}{a_1} \\ b_2 &= -\frac{a_2}{a_1^3} \\ b_3 &= \frac{1}{a_1^3} (2a_2^2 - a_1 a_3) \end{aligned} \quad (62)$$

Therefore (59) can now be re-written as a function of i_c :

$$i_c = \frac{v_s}{R_E + r_e} + \frac{1}{2I_C} \left(\frac{r_e}{R_E + r_e} \right) \left(\frac{v_s}{R_E + r_e} \right)^2 + \left[\frac{1}{2I_C^2} \left(\frac{r_e}{R_E + r_e} \right)^2 - \frac{1}{3I_C^2} \left(\frac{r_e}{R_E + r_e} \right) \right] \left(\frac{v_s}{R_E + r_e} \right)^3 \quad (63)$$

Now the third order intercept voltage can be determined:

$$v_{IP3} = 2 \sqrt{\frac{k_1}{3k_3}} = 2 \sqrt{\frac{1}{3} \left(\frac{1}{|R_E + r_e|} \right) \frac{6I_C^2 (|R_E + r_e|)^5}{r_e |2R_E - r_e|}} = 2\sqrt{2} v_T \frac{|R_E + r_e|^2}{\sqrt{r_e^3 |2R_E - r_e|}} \quad (64)$$

This very useful equation can be used to estimate the linearity of gain stages.

2.5.2 Non-linearity in the Output Impedance of the Bipolar Transistor

Another important non-linearity in the bipolar or CMOS transistor is the output impedance such as in the case of a current source. With this circuit, the base of the transistor is biased with a constant voltage and the current into the collector is supposed to remain constant for any output voltage. Of course the transistor has a finite output impedance so there is some finite ac current that flows through the transistor as shown in Fig. 9. However, the important issue is that the transistor's output impedance will change with applied voltage and therefore it can also introduce non-linearity.

Fig. 9. Bipolar transistor as a current source.

The output impedance of a transistor is given by [1]:

$$r_{o_static} = \frac{V_A}{I_C} \quad (65)$$

where V_A is the early voltage of the transistors. With an ac current i_c being applied to transistor's collector it can be written as a function of ac current i_c .

$$r_{o_dynamic}(i_c) = \frac{V_A}{I_C + i_c} \quad (66)$$

Now the ac collector emitter voltage can be written as (we assume for this analysis that there is no other significant impedance in the circuit other than the transistor output resistance):

$$v_{ce} = i_c r_{o-ac} = \frac{i_c V_A}{I_C + i_c} = V_A \frac{\frac{i_c}{I_C}}{1 + \frac{i_c}{I_C}} \quad (67)$$

now using the relationship:

$$\frac{x}{1+x} = x - x^2 + x^3 - x^4 + x^5 \dots \quad (68)$$

(67) can be written out as a power series:

$$v_{ce} = V_A \left(\frac{i_c}{I_C} \right) - V_A \left(\frac{i_c}{I_C} \right)^2 + V_A \left(\frac{i_c}{I_C} \right)^3 = r_{o-DC} i_c - \frac{r_{o-DC}}{I_C} i_c^2 + \frac{r_{o-DC}}{I_C^2} i_c^3 \quad (69)$$

The intermodulation current can now be easily determined.

$$i_{IP3} = 2 \sqrt{\frac{k_1}{3k_3}} = 2 \sqrt{\frac{1}{3} \frac{r_{o-DC}}{r_{o-DC}} \frac{I_C^2}{r_{o-DC}}} = \frac{2I_C}{\sqrt{3}} \quad (70)$$

Thus the output intermodulation voltage is just:

$$v_{OP3} = \frac{2I_C}{\sqrt{3}} r_o \quad (71)$$

This is a fairly intuitive result. As the DC current is increased, the ac current is a smaller percentage of the total and therefore the circuit behaves more linearly. Thus, the designer has two choices if the current source isn't linear enough. They can either increase the current or increase the output impedance. In addition, it should be noted that this relationship only holds true provided that the transistor doesn't start to saturate. If it does the non-linearity will get much worse.

2.5.3 High Frequency Non-Linearity in the Bipolar Transistor.

There are many frequency dependent components that can reduce the linearity of a circuit, but one of the most troublesome is the base-collector junction capacitance. This capacitance is often highly non-linear which can be detrimental to the linearity of the system, especially in circuits with low supply voltages, because of the increased value of this capacitance under low reverse bias.

This capacitor's effect is particularly significant in the case of a standard (non cascode) common-emitter amplifier. In this configuration, due the Miller effect C_μ is multiplied by the gain of the amplifier and appears between the base and emitter.

The value of C_μ as a function of bias voltage is given by:

$$C_\mu(V) = \frac{C_{\mu 0}}{\left(1 - \frac{V}{\psi_o}\right)^{\frac{1}{n}}} \quad (72)$$

Where $C_{\mu 0}$ is the capacitance of the junction under zero bias, ψ_o is the built in potential of the junction and n is usually between 2 and 5. If the impedance of this parasitic diode starts to become significant then this can be a limiting source of non-linearity in the circuit. Since this diode's behavior is highly process dependent and hard to model, there is little benefit in deriving detailed equations for it. Rather, the designer must rely on simulation and detailed models to predict its behavior accurately.

2.6 Low Voltage Topologies for LNAs

Of the two configurations described so far, the common-emitter would seem ideally suited to low voltage operation. However, if the improved properties of the cascode are required at lower voltage, then the topology must be modified slightly. This has led some designers to “fold” the cascode as shown in Fig. 10 [4]. With the use of two additional LC tanks and one very large coupling capacitor, the cascode can now be operated down to a very low voltage. This approach does have drawbacks. First, it uses two additional inductors which will use a lot of die area, and second, the coupling capacitor in this circuit C_{large} has to be an extraordinary size, since this part of the circuit has to drive a low impedance. One designer using this technique built an LNA centered at 1.9GHz and used a $C_{\text{large}} = 60\text{pF}$! This capacitor will use significant die area and will contribute to reduced gain due to considerable parasitic capacitance to the substrate. In the design just mentioned with a capacitance of 60pF, the parasitics could be as high as 3pF or larger. The other drawback present with any folding scheme is that the current can no longer be reused by both transistors. Thus, this technique will use approximately twice the current

of an unfolded cascode although it could be used at half the voltage to result in comparable power consumption.

Fig. 10. A folded cascode LNA.

In this work, an alternative to the above topology is proposed. This solution involves magnetic rather than electric coupling between the two stages with a transformer as shown in Fig. 11. In this circuit, L_p and L_s form the primary and secondary windings of an on-chip transformer. Note that there is no longer any need for the coupling capacitor and the transformer, although slightly larger than a regular inductor, will nevertheless use much less die area than two individual inductors.

Fig. 11. Magnetically coupled cascode topology.

2.7 Conclusions

This chapter has introduced a review of basic circuit theory dealing with the design of low noise amplifiers. Noise and linearity in RF circuits have been discussed. Methods for implementing low voltage LNAs have been proposed. Formulas for NF_{min} , NF , and G_{opt} and B_{opt} have been derived. The linearity due to many elements in the bipolar transistor has been discussed. Formulas for IIP3 have been derived. This chapter has also served as background for the research in this thesis. Chapter 6 will make use of the theory on LNAs and use them as a basic element to build filters.

Chapter 3: A Low Voltage Mixer Topology

Mixers are the next RF building block to be considered in this work. They take the input radio-frequency signal and convert it to a lower frequency by multiplying it with a reference frequency. Mixers are one of the hardest building blocks to operate at low voltages because they usually employ many stacked transistors. The following section details the operation of a basic double-balanced mixer typically employed in Si and SiGe technologies and reviews some work done in order to make them operate at low voltages.

3.1 Basic Mixer Operation

Mixers can be made out of the LNAs that have already been discussed and some form of controlled inverter. One of the simplest forms of a mixer is shown in Fig. 12. The bottom of the mixer is simply a differential implementation of a gain stage that has already been considered. The amplified current from the gain stage is then passed into the ideal inverter stage. This stage has a gain of either plus or minus one depending on the control signal. If the control signal is assumed to be a square wave, then this will have the effect of multiplying the current coming out of the gain stage (Q1, Q2) by plus or minus one alternately. Multiplying a signal by another signal will cause the output to have components at various frequencies. Thus, this can be used to move the signal from one frequency to another.

Fig. 12. Simple conceptual schematic of a doubly balanced mixer.

3.2 Mixer Gain

The square wave just discussed can be written as the sum of an infinite number of sine waves. If the square wave is assumed to have a fundamental frequency of ω_{LO} then the signal can be described by:

$$LO = \frac{4}{\pi} \sin(\omega_{LO}t) + \frac{4}{3\pi} \sin(3\omega_{LO}t) + \frac{4}{5\pi} \sin(5\omega_{LO}t) + \frac{4}{7\pi} \sin(7\omega_{LO}t) + \dots \quad (73)$$

Now each one of these tones will get multiplied by the RF output signal from the gain stage. The frequency component of the most interest is due to the product of the RF signal with the fundamental of the square wave.

$$IF = \frac{4}{\pi} \sin(\omega_{LO}t) \cdot \cos(\omega_{RF}t) \quad (74)$$

Now using trigonometric identities results in:

$$IF = \frac{4}{2\pi} (\sin(\omega_{LO}t - \omega_{RF}t) + \sin(\omega_{RF}t + \omega_{LO}t)) \quad (75)$$

In the case of an up-conversion mixer, the higher frequency component is of interest, while in the case of a down-conversion mixer, the lower frequency is of interest. Usually

filtering is used to remove the unwanted sideband and as much of the unwanted frequency components as possible. Thus, the gain of the mixer is equal to the gain of an equivalent amplifier multiplied by a factor of $2/\pi$ or about -3.9dB compared to what the gain of the amplifier would have been. In practice, the mixer LO may be driven with a sine wave that provides full switching only at the peak of the sine wave rather than with a square wave. In this case, the $4/\pi$ factor becomes unity and the gain factor becomes simply $1/2$ or -6dB . For a smaller sine wave the gain becomes even less.

One figure of merit that is commonly measured in mixers is the amount of RF feed-through. Since the mixer switches the RF signal back and fourth between the differential outputs, on average the RF signal present at the top of the mixer is ideally zero. However, in practice, due to transistor mismatch or imbalance some RF signal will appear at the output.

3.3 A Practical Implementation of a Mixer

In order to make the mixer discussed so far practical, the ideal gain element must be replaced by a practical implementation. The most common way to do this is the use of four switches which are alternately turned on and off to take the relevant currents to one side or the other of the top of the mixer. These transistor switches are normally placed in a cascode configuration. A classic doubly balanced mixer is shown in Fig. 13.

Fig. 13. A classic doubly-balanced mixer topology.

3.4 Mixer Noise Figure

Mixer noise figure is somewhat more complicated to define, compared to that of an LNA, because of the frequency translation involved. Therefore, for mixers a slightly modified definition of noise figure is used. Noise factor for a mixer is defined as:

$$F = \frac{N_{\text{tot}}(\omega_{\text{IF}})}{N_{\text{source}}(\omega_{\text{IF}})} \quad (76)$$

where $N_{\text{tot}}(\omega_{\text{IF}})$ is the total output noise at the IF frequency and $N_{\text{source}}(\omega_{\text{IF}})$ is the total output noise due to the source at the IF frequency. Now the source generates noise at all frequencies and many of these frequencies will produce noise at the output frequency due to the mixing action of the circuit. Usually the two dominant frequencies are the input frequency and the image frequency.

To make things even more complicated, single side band noise figure, or double side band noise figure are defined. The difference between the two definitions is the value of the denominator in (76). In the case of double side band noise figure, all the noise due to

the source at the output frequency is considered (noise at the input and image frequencies). In the case of single side band noise figure, only the noise at the output frequency due to the source that originated at the RF frequency is considered. Thus, using the single side band noise figure definition, even an ideal noiseless mixer would have a noise figure of 3dB. This is because the noise of the source would be doubled in the output due to the mixing of the RF and image frequency noise on top of each other.

For this same reason, mixers tend to be much noisier than LNAs. Noise sources in the circuit get translated to different frequencies and this often “folds” noise into the output frequency. Generally, mixers have two frequency bands where noise is important:

- 1) Noise already present at the IF frequency: The transistors and resistors in the circuit will generate noise at the IF frequency. Some of this noise will make it to the output and corrupt the signal. For example, the collector resistors will add noise directly at the output IF frequency.
- 2) Noise at the RF and image frequencies: Any noise present at the RF and image frequencies will also be mixed down to the IF frequency. For instance, the collector shot noise of Q1 at the RF frequency and at the image frequency will both appear at the IF frequency at the output.

Also note that noise over a cycle of the LO is not constant. The LO’s purpose is to switch the upper quad transistors from cutoff to saturation. In both of these two states the transistors will add very little noise because they have no gain. However, any real LO will have a finite rise and fall time. Thus, for some portion of the period of the LO these transistors will be on and in the active region. During this time, noise in the LO will be amplified and passed into the output.

3.5 Large Signal Behavior of the Differential Pair

The upper four transistors in the mixer, or the upper quad, consist of two differential pair amplifiers driven by a large signal. These transistors must be properly biased and be

completely switched in order for the mixer to work properly. The differential pair will require an input voltage swing of about $4-5 V_T$ for the transistors to be hard switched one way or the other. Therefore the LO should be at least 100mV peak for complete switching. In practice usually more like 300mV would be better. However, if the LO voltage is made too large, then a lot of current has to be moved into and out of the bases of the transistors during transitions. This can lead to spikes in the signals and can actually slow the switching process down. Thus, too large a signal can be just as bad as too small a signal.

Another problem that is of concern is the parasitic capacitance on node V_d , as shown in Fig. 14. The transistors have to be turned on and off which means that any capacitance in the emitter has to be charged and discharged. Essentially, the input transistors behave like a simple rectifier circuit as shown in Fig. 14(B). If the capacitance on the emitters is too large, then V_d will stop following the input voltage and the transistors will start to be active for a smaller portion of the cycle as shown in Fig. 14 (C) (since V_d is higher than it should be, it takes longer for the transistor to saturate and it saturates for a smaller portion of the cycle). This will lead to waveform distortion.

Fig. 14. Large signal behavior of the differential pair. (A) Schematic representation. (B) Diode rectifier model. (C) Waveforms illustrating the problem of slewing.

3.6 A Low Voltage Mixer Topology

Defining a low voltage mixer topology is a problem that has already been solved [46] and the circuit is shown in Fig. 15. For the purposes of this work, this topology will be borrowed and implemented more as a means of completing the rest of the receiver rather than as an attempt to show any novelty in and of itself.

Note that in this mixer, the driver transistor of the mixer shown in Fig. 15 has been replaced with a transformer. This may reduce the gain of the mixer and therefore also degrade the noise performance, but is expected to improve its linearity. As well, for the purposes of this work, if the receiver is designed to have a 1GHz IF, then this makes it possible to replace R_L with an LC tank instead of a resistor to provide a load for the

mixer. The AC ground for transistors Q1 through Q4 will be provided by a center tap in the transformer, where a current source is connected to provide bias. As well, the primary of this transformer L_p and C_1 could form the tank at the collector of the cascode LNA.

Fig. 15. A low voltage mixer topology.

3.7 Conclusion

The basic theory of operation of the balanced cross-coupled mixer was reviewed. A method for allowing these mixers to operate at low voltage has been previously proposed by Long. This method will be used later in this work to demonstrate a full receiver operating at low supply voltage.

Chapter 4: The Use of Inductors and Transformers in Circuits

4.1 Basic Inductor Structures

Of all the passive structures used in RF circuits, inductors and transformers or baluns are the most difficult to realize monolithically with high Q. In Si, they suffer from the presence of lossy substrates and high resistivity metal. However, over the past few years much research has been done in efforts to improve fabrication methods for building inductors, as well as modeling, so that better geometries could be used in their fabrication [30]-[41].

Traditionally, inductors were made as square spirals, as shown in Fig 16, due to limitations in modeling and simulation tools. Square inductors, however, have less than optimum performance due to the ninety degree bends present in the layout that add to the resistance of the structures. A more optimum structure is shown in Fig 17. Since this inductor is made circular it has less series resistance. Furthermore, this geometry also is more symmetric than traditional inductors (its S-parameters look the same from either side) thus it can be used in differential circuits without the need to have two inductors to get good symmetry between the two halves of the circuit. As well, bias can be applied through the axis of symmetry of this structure at its center if needed. Biasing at this point is not possible in a single-ended design, as it destroys the single-ended performance of the inductor.

Fig 16. A conventional single ended inductor layout.

Fig 17. A circular differential inductor layout.

4.2 Some Basic Lumped Models for Inductors

The basic pi model for a regular inductor is shown in Fig. 18[17]. R_s models the series loss in the windings, C_w models the inter-winding capacitance, C_{sub} and R_{sub} model the

capacitance to the substrate and substrate losses, and C_{oxide} models the oxide capacitance. Note that in a regular inductor, both sides are not symmetrical due in part to the added capacitance on one side of the structure due to the underpass. The underpass connects the metal at the center of the planar coil with metal at the periphery.

Fig. 18. Basic Pi Model for a regular Inductor.

The model for the symmetric, or so called differential inductor is shown in Fig. 19 [41]. Here, the model is broken into two parts with the center at the axis of symmetry where a bias can be applied if desired. Note also that since the two halves of the spiral are interleaved, there is magnetic coupling between both halves of the device. This is modeled by K .

Fig. 19. Basic Model for a differential inductor.

4.3 The Quality Factor (Q) of an Inductor

The Q of an inductor is the imaginary part of the impedance of the structure divided by the real part of the impedance of the structure.

This seems like a fairly simple definition, however confusion may occur when trying to determine what the impedance is. Traditionally, we have assumed that one port of the inductor is grounded. In this case we can define the impedance seen from port 1 to ground (in terms of Z parameters) as follows [40]:

$$Z_{Port1} = Z_{11} - \frac{Z_{12}Z_{21}}{Z_{22}} \quad (77)$$

Equivalently if we look from port 2 to ground the impedance becomes:

$$Z_{Port2} = Z_{22} - \frac{Z_{12}Z_{21}}{Z_{11}} \quad (78)$$

Note that referring to Fig. 19 or Fig. 20 this effectively grounds out one set of C_{oxide} , R_{sub} and C_{sub} . Thus, the Q will not necessarily be the same looking from both ports. In fact the Q will be marginally higher in the case of a regular structure looking from the side with no underpass as there will be less loss. Also, note that the side with no underpass will have a higher self-resonance frequency as well.

In a lot of circuit applications designers want to use inductors in a differential configuration. This means that both ends of the inductor are connected to active points in the circuit and neither side is connected to ground. In this case, we can define the impedance seen between the two ports as:

$$Z_{Diff} = Z_{11} + Z_{22} - Z_{12} - Z_{21} \quad (79)$$

In this case, the substrate capacitance and resistance from both halves of the inductor are in series. Thus, when the inductor is excited in this mode it experiences less loss and will give a higher Q. Thus the differential Q is usually higher than the single ended Q. The self-resonance of the inductor in this mode will also be higher than the self-resonance frequency looking from either side to ground. In addition, the frequency at which the differential Q peaks is usually higher than for the single ended excitation. Care must be

taken, therefore when optimizing an inductor for a given frequency, to keep in mind its intended configuration in the circuit.

4.4 Some Notes About the Proper Use of Inductors

Designers are very hesitant to place a non-symmetric component, such as a regular inductor, across a differential circuit. For this reason, they usually make use of two regular inductors to form their inductance. In this case, the center of the two inductors is ac grounded and the effective circuit differential Q for the two inductors is equal to their individual single ended Qs. To illustrate this point, take a simplified model of an inductor with only substrate loss as shown in Fig. 20. In this case, the single ended Q is given by:

$$Q_{SE} = \frac{R}{\omega L} \quad (80)$$

and the differential Q is given by:

$$Q_{Diff} = \frac{2R}{\omega L} \quad (81)$$

Fig. 20. Simplified inductor model with only substrate loss.

Fig. 21. Two simplified inductors connected in series with only substrate loss.

Now if two inductors are placed in series, as shown Fig. 21 (center parasitics not shown) the differential Q of the overall structure is given by:

$$Q_{Diff2} = \frac{2R}{2\omega L} = \frac{R}{\omega L} = Q_{SE} \quad (82)$$

Thus, the differential Q of the two inductors is equal to the single ended Q of one of the inductors by itself. Thus, the advantage of using symmetric structures should be obvious. Note that here substrate losses have been assumed to dominate. If the series resistance is dominant in the structure, then using this configuration will see less advantage. However, due to the mutual coupling of the structure this configuration would still be preferred as it makes more efficient use of chip area.

If using a differential inductor in a differential circuit, the designer would probably use only one structure. In this case, the effective Q of the circuit will be the differential Q of the inductor. Note that this is due to the way the inductor is connected, and if a regular inductor were used in its place, the circuit would see its differential Q as well.

When using a regular inductor with one side connected to ground, the side with the underpass should be the side that is grounded as the effective Q and the self resonance frequency will be higher.

4.5 Transformers

Transformers in Si are as yet not all that common. They are more complicated than inductors and therefore harder to model in many cases. Transformers or baluns consist of two interwound spirals that are magnetically coupled. An example layout is shown in Fig. 22. In this figure, two spirals are interwound in a 2:1 turns ratio structure. The structure can be characterized by a primary and secondary inductance and a mutual inductance or coupling factor which describes how efficiently energy can be transferred from one spiral to the other.

Fig. 22. Example layout of a circular 2:1 turns ratio transformer.

Transformers can be modeled much like inductors. They have a capacitance to the substrate and substrate losses. The metal has series resistance and the coils have interwinding capacitance. As well, there is a coupling factor between the two coils that describes the coupling between the spirals. A simplified model for a transformer that captures most of these effects is shown in Fig. 15.

Fig. 23. Basic model of transformer or ballun.

Traditionally, when transformers are measured and characterized, the S_{21} for the device is reported. Although correct, this leaves the designer who would use the structure with little information about how the device will behave in an integrated circuit application where the transformer will almost certainly be loaded with impedances other than 50Ω . It would seem to be more useful to extract an inductance and Q for both windings, and plot the coupling (K factor) for the structure instead.

The mutual inductance (M) of a transformer and the coupling factor (K) for the structure are both measures of the efficiency of energy transfer between the coils. They are related by [37]:

$$K = \frac{M}{\sqrt{L_p L_s}} \quad (83)$$

If the S-parameters of the structure are measured and the Z-parameters extracted, then the mutual inductance can be found from:

$$M = \frac{Z_{12}}{j\omega} = \frac{Z_{21}}{j\omega} \quad (84)$$

As well the primary and secondary inductance and loss can be estimated from:

$$\begin{aligned} Z_{11} &= R_p + j\omega L_p \\ Z_{22} &= R_s + j\omega L_s \end{aligned} \quad (85)$$

where R_p and R_s are the equivalent series loss in the primary and secondary at any given frequency and L_p and L_s are the equivalent primary and secondary inductance at any given frequency. It is assumed here that the transformer can be modeled at a single frequency using the model shown in Fig. 24.

Fig. 24. Narrow band equivalent model for a transformer.

4.6 Conclusions

The design and layout of on-chip inductors and transformers was discussed in this chapter. The ability to optimize these structures as well as build accurate models to predict their performance is essential to the design of the other circuits discussed in this thesis. Transformers are particularly important to the design of low-voltage mixers as was shown in the previous chapter. They will also be essential in low-voltage VCO design, and filter design. Example models have also been presented for transformers and alternative “figures of merit” for these structures have been proposed that are more useful in an IC context.

Chapter 5: A Low Voltage VCO Topology

5.1 Introduction

On-chip VCOs have been a subject of intense research in the past few years as designers struggle to meet phase noise requirements using low Q (quality factor) on-chip inductors [18]-[28]. However, as technologies progress and begin to provide thicker metallization, and especially with the introduction of Cu interconnects into some advanced processes [29]-[32], inductor performance will continue to improve. (Higher Q inductors are desirable as they lead to lower loss oscillators with lower phase noise. Low phase noise is desirable in order to reduce the amount of reciprocal mixing in a receiver.) Undoubtedly on-chip VCOs will also become more widely used in receiver ICs, especially in low-cost ICs. Higher degrees of integration are desirable because they lead to lower manufacturing cost due to reduced board complexity. As well, recent trends have shown the desire for low supply voltages in RF components, as this will lead to lower power consumption and therefore longer battery life. Furthermore, lower voltages and less current means that products can be made to require fewer battery cells leading to lighter, more compact devices.

Achieving good phase noise from VCOs at lower voltages is among the hardest challenges facing the RF designer. This is because to some degree, the phase noise of the VCO is dependent on the output power and therefore, on the voltage swing of the oscillator. As the supply voltage drops, then so does the available voltage swing to the oscillator. In fact, many VCOs cannot even operate at lower supplies due to transistor stacking in the circuit.

5.2 Basic Operation of the $-G_m$ VCO

Some designers have used differential Colpitts common-collector [23][27] and common-base [24][25] VCOs with good results. They usually provide good output power, are insensitive to parasitics and have good phase noise performance. However, compared to

the simpler negative transconductance ($-G_m$) oscillator that has been gaining popularity over the last few years [18][20][26][28][7], they are a complicated circuit with complicated biasing requirements. Thus, for this work it is proposed to use the $-G_m$ topology, due to its intrinsically simple biasing scheme, with some modifications. A simple example of this VCO is shown in Fig. 25. Transistors Q1 and Q2 form a negative resistance generator in parallel with an LC tank that sets the frequency of oscillation. Varactors are used in place of fixed capacitors to provide a tuning scheme. The supply voltage is fed into the circuit through the center tap of a symmetric differential inductor. A single inductor is preferred in this circuit because of the superior Q and reduced chip area compared with two inductors connected in series.

Fig. 25. A basic topology for the $-G_m$ voltage-controlled oscillator.

To understand how Q1 and Q2 form a negative resistance, it is helpful to look at their small signal model as shown in Fig. 26.

Fig. 26. Small signal equivalent model for the negative resistance cell in the negative resistance oscillator.

An expression for the amount of current that flows into the circuit can be written as follows:

$$I_i = \frac{V_i}{r_{e1} + r_{e2}} + g_{m1} V_{\pi1} - g_{m2} V_{\pi2} \quad (86)$$

Now if it is assumed that both transistors are biased identically then $g_{m1} = g_{m2}$, $r_{e1} = r_{e2}$, $V_{\pi1} = -V_{\pi2}$, and the equation can be solved for $Z_i = V_i/I_i$.

$$Z_i = \frac{-2}{g_m} \quad (87)$$

Thus, the oscillator can be redrawn conceptually as shown in Fig 27. It consists of a resonator with some equivalent parallel loss R_T and active loss canceling circuitry.

Fig 27. Conceptual drawing of the $-G_m$ oscillator.

Thus, in this circuit a necessary condition for oscillation is that:

$$R_T > \frac{2}{g_m} \Rightarrow R_T g_m > 2 \quad (88)$$

this is a more relaxed condition for start up than the Colpitts circuit which needs more gain in order to start. This is undoubtedly a large factor leading to the popularity of this circuit with CMOS designers who have to deal with lower g_m than in bipolar circuits.

5.3 Oscillator Amplitude

Provided that (88) is satisfied, the oscillator will begin to oscillate. The oscillations will continue to grow until the transistor non-linearities reduce the gain until the losses and the negative resistance are of equal value.

For a more quantitative analysis of the amplitude of oscillation of the circuit, we first start with a transistor being driven by a large sinusoidal voltage, as shown in Fig. 28 [7]. We start by breaking the loop, applying a voltage to the bases of the transistors, and looking at the collector currents that result.

Fig. 28. Short tail pair with a large sinusoidal voltage applied to the base.

We can see from Fig. 28 that this is just a differential pair with a large voltage applied across the input. The formula that relates current to voltage is well known [1] and is given by:

$$i_c(\theta) = \frac{I_{Tank}}{1 + e^{\frac{V_{Tank} \cos(\theta)}{V_T}}} \quad (89)$$

We find the fundamental component of the current by solving the following integral:

$$i_{fund} = \frac{2}{\pi} \int_{\theta=0}^{\theta=\pi} \frac{I_{Tank}}{1 + e^{\frac{V_{Tank}}{V_T} \cos(\theta)}} \cos(\theta) d\theta \quad (90)$$

It can be shown, provided $V_{Tank}/V_T > 8$ (which is reasonable for most practical oscillator amplitudes) that:

$$\frac{i_{fund}}{I_{Tank}} \approx \frac{2}{\pi} \quad (91)$$

Thus, if the parallel resistance of the resonator is R_T , the peak voltage developed across the resonator differentially will be given by:

$$V_{Tank} = i_{fund} R_T = \frac{2}{\pi} I_{Tank} R_T \quad (92)$$

If the current source in Fig. 28 is replaced with a resistor then the derivation is slightly more complicated. Since the total current flowing through the oscillator will change over a cycle (with minimum current at the zero crossings and maximum current at the voltage peaks) (89) can be modified to take into account the resistor.

$$i_c(\theta) \approx \frac{\frac{V_B + \left| \frac{V_{Tank} \cos(\theta)}{2} \right| - V_{BEQ}}{R_{Bias}}}{1 + e^{\frac{V_{Tank}}{V_T} \cos(\theta)}} = \frac{I_{BQ} + \left| \frac{V_{Tank} \cos(\theta)}{2} \right|}{1 + e^{\frac{V_{Tank}}{V_T} \cos(\theta)}} \quad (93)$$

where R_{Bias} is the tail resistor that is serving as a current source, I_{BQ} is the quiescent bias current before oscillations begin, V_{BEQ} is the quiescent base emitter voltage of Q1 or Q2 and $V_{Tank} \cos(\theta)$ is the instantaneous voltage applied to the bases of Q1 and Q2 (see Fig. 28). It is assumed that V_{BEQ} is constant in this expression, which is a good approximation for the half cycle when the transistor is on. In the other half cycle the denominator will force the expression to zero for any reasonable value of V_{Tank} ($V_{Tank} \gg V_T$), so the approximation will not seriously effect the shape of the resulting waveform. The two current waveforms for each case are illustrated in Fig. 29.

Fig. 29. Collector Current waveforms for current source and resistive tail differential pairs.

This expression can be used to find the average DC operating current in the circuit (which will be higher than the quiescent current). This current also depends on the final amplitude of the VCO.

$$I_{Tank} = \frac{1}{2\pi} \int_0^{2\pi} \frac{I_{BQ} + \frac{|V_{Tank} \cos(\theta)|}{2R_{Bias}}}{1 + e^{\frac{V_{Tank} \cos(\theta)}{V_T}}} d\theta \approx I_{BQ} + \frac{V_{Tank}}{\pi R_{Bias}} \quad (94)$$

The fundamental component of the current can also be extracted from (94) as before.

$$i_{fund} = \frac{2}{\pi} \int_0^{\pi} \left[\frac{I_{BQ} + \frac{|V_{Tank} \cos(\theta)|}{2R_{Bias}}}{1 + e^{\frac{V_{Tank} \cos(\theta)}{V_T}}} \right] \cos(\theta) d\theta \approx \frac{2}{\pi} I_{BQ} + \frac{V_{Tank}}{4R_{Bias}} \quad (95)$$

This allows us to determine the ratio of average current to current at the fundamental:

$$k = \frac{i_{fund}}{I_{Tank}} = \frac{\frac{2}{\pi} I_{BQ} + \frac{V_{Tank}}{4R_{Bias}}}{I_{BQ} + \frac{V_{Tank}}{\pi R_{Bias}}} \quad (96)$$

In the limit of large and small V_{Tank} it can be seen that k is bounded by:

$$\frac{2}{\pi} \leq k \leq \frac{\pi}{4} \quad (97)$$

The oscillation amplitude can therefore once again be given in terms of DC current as:

$$V_{Tank} = i_{fund} R_T = k I_{Tank} R_T \quad (98)$$

Thus, equations to predict oscillation amplitude have now been derived. By comparing equations (98) and (97) to (91), it can be seen that a given amount of DC current will lead to more current at the fundamental frequency in the case of the resistive tail as opposed to the current tail.

5.4 Phase Noise and the $-G_m$ VCO.

Due to the importance of phase noise to receiver performance, a brief review will be given here in an effort to clarify a few points.

5.4.1 Linear or Additive Phase Noise

If we treat the oscillator as a linear feedback system as shown in Fig 30, then we can deal with noise around the carrier. This noise is injected into the tank from the transistors and can be modeled as an input $n_{in}(t)$ as shown. The noise is then shaped by the feedback action of the loop and the output spectrum of the noise can be described by the well known Leeson's formula.

$$\left| \frac{N_{OUT}(s)}{N_{IN}(s)} \right|^2 = \frac{\omega_o^2}{4Q^2(\Delta\omega)^2} \quad (99)$$

where Q is the loaded quality factor of the tank, ω_0 is the frequency of oscillation and $\Delta\omega$ is the frequency offset from the carrier. This formula is derived in detail in a number of sources [33][34].

Fig 30. Linear model of an oscillator showing noise shaping.

This formula does not deal with any of the other sources of noise in the oscillator. Specifically, there is no frequency translation of noise sources in this analysis. Thus, an input noise source at frequency $\omega_0 + \Delta\omega$ can cause noise (phase or amplitude) only at that same frequency.

This formula also requires a method to compute the input noise power of the oscillator N_{IN} in order to make it useful.

If the transistors and bias were assumed to be noiseless, then the only noise present would be due to the resonator losses. Since the total resonator losses are due to its finite resistance, which has an available noise power of kT , then in this case:

$$|N_{IN}(s)|^2 = kT \quad (100)$$

The transistors and the bias will add noise to this minimum. Note that since this is not a simple amplifier with a clearly defined input and output, it would not be appropriate to define the transistor in terms of a simple noise figure. As an example, consider the bias noise in the case of the $-G_m$ oscillator which will be passed on to the resonator from the tail current source when the transistors Q1 and Q2 are switched. If ρ is the fraction of a cycle during which the transistors are completely switched, i_{nt} is the noise current injected into the oscillator from the tail during this time. During transitions the transistors act like an amplifier, thus collector shot noise i_{cn} from Q1 and Q2 dominates the noise during this time. The total input noise becomes:

$$|N_{IN}(s)|^2 \approx kT + \frac{i_m^2 R_p}{2} \rho + i_{cn}^2 R_p (1 - \rho) \quad (101)$$

where R_p is the equivalent parallel resistance of the tank. Thus, we can define an excess noise factor for the oscillator as excess noise injected by noise sources other than the losses in the tank:

$$F = 1 + \frac{i_m^2 R_p}{2kT} \rho + \frac{i_{cn}^2 R_p (1 - \rho)}{kT} \quad (102)$$

Note that as the Q of the tank increases, R_p increases and noise has more gain to the output, therefore increasing F . For a low noise design it is possible to filter out all high frequency noise from the bias.

Phase noise is also normalized to the output power. Thus, the formula can be re-written in a more conventional form:

$$PN = \left(\frac{\omega_o}{(2Q\Delta\omega)} \right)^2 \left(\frac{FkT}{2P_s} \right) \quad (103)$$

where P_s is the power in the oscillator tone, k is Boltzmann's constant, and T is the temperature of the circuit. Note here that the extra $\frac{1}{2}$ is due to the assumption that noise power injected into the oscillator is divided equally between phase noise and amplitude noise.

5.4.2 Low Frequency Noise Mixing

In any oscillator, and especially in a voltage-controlled oscillator, there are components that cause the frequency to vary with the applied voltage (namely varactors used to tune the oscillator). Any noise present on the terminals of the varactors will therefore get FM modulated around the carrier. Note that this mechanism is present even in fixed oscillators to some extent because of junction capacitance in the transistors. The output of the VCO disturbed by a noise source at frequency ω_n is given by:

$$v_{out}(t) = \cos(\omega_o t) + \frac{v_n K_{VCO}}{2\omega_n} [\cos(\omega_o + \omega_n)t - \cos(\omega_o - \omega_n)t] \quad (104)$$

where K_{VCO} is the gain of the VCO, and v_n is the applied noise voltage. Here we have normalized the noise voltage to a magnitude of unity. Thus the phase noise contribution of this noise source is given by:

$$PN = \left(\frac{v_n K_{VCO}}{2\omega_n} \right)^2 \quad (105)$$

NOTE: This noise mechanism generates phase noise. It does not generate amplitude noise so there is no need for an extra factor of $1/2$ in this formula.

It is interesting to note that there is another form of noise that can contribute amplitude noise, but no phase noise directly. Assume that some noise source were to disturb the bias current, then the output wave form would have the form:

$$v_{out}(t) = \cos(\omega_o t) (1 + v_n K \cos(\omega_n t)) \quad (106)$$

In this we have AM modulation and amplitude noise is generated.

5.4.3 Nonlinear Noise

The third type of noise in oscillators is due to the non-linearity in the transistor mixing noise to other frequencies. For instance, assume that there is a noise at some frequency f_n close to the carrier. This noise will get mixed with the oscillation tone, f_o to another sideband at $2f_o - f_n$ as shown in Fig 31. Note that this is the only term that falls close to the carrier, all the rest fall out of band and are therefore of much less interest.

Fig 31. Conceptual figure to show the effect of nonlinear mixing.

Fig. 32. A transistor driven by a large sinusoid in the presence of noise.

The magnitude of this noise can be estimated with the following analysis. The analysis begins by considering a transistor being driven by a large sinusoidal voltage and a small noise source as shown in Fig. 32. The exponential current-voltage relationship of the transistor can be described by the following power series:

$$i_C \approx I_C \left(1 + \frac{v_i}{V_T} + \frac{1}{2} \left(\frac{v_i}{V_T} \right)^2 + \frac{1}{6} \left(\frac{v_i}{V_T} \right)^3 + \dots + \frac{1}{n!} \left(\frac{v_i}{V_T} \right)^n \right) = k_0 + k_1 v_i + k_2 v_i^2 + \dots + k_n v_i^n \quad (107)$$

Note that truncation after only a few terms is not possible since the oscillation amplitude v_i can be much greater than V_T . Now let us assume that the input is given by:

$$v_i = v_o \cos(\omega_o t) + v_n \cos(\omega_n t) \quad (108)$$

where v_o is the fundamental tone in the oscillator and v_n is some small noise source at some frequency ω_n . Substituting (108) into (107), the components at frequency ω_n can be extracted and are given by:

$$i_{\omega_n} \approx k_1 v_n + \frac{6}{4} k_3 v_n v_o^2 + \frac{30}{16} k_5 v_n v_o^4 + \frac{140}{64} k_7 v_n v_o^6 + \frac{630}{256} k_9 v_n v_o^8 + \frac{2772}{1024} k_{11} v_n v_o^{10} + \dots \quad (109)$$

assuming that $v_o \gg v_n$. Note the constants can be derived as a series, or computed with the aid of a software package. The third order intermodulation term can likewise be extracted from (107) and (108) and is given by:

$$i_{2\omega_o - \omega_n} \approx \frac{3}{4} k_3 v_n v_o^2 + \frac{20}{16} k_5 v_n v_o^4 + \frac{105}{64} k_7 v_n v_o^6 + \frac{504}{256} k_9 v_n v_o^8 + \frac{2310}{1024} k_{11} v_n v_o^{10} + \dots \quad (110)$$

Note that as the number of terms gets large, the ratio of the i^{th} term of (109) and the i^{th} term of (110) approaches 1. As a result:

$$0 < \frac{i_{2\omega_o - \omega_n}}{i_{\omega_n}} < 1 \quad (111)$$

For most practical oscillation amplitudes the ratio in (111) will be approximately 1. Leeson's formula can provide the amplitude of the linear noise, which is present at frequency ω_n . If it is further assumed that there is equal linear noise content at both ω_n and $2\omega_o - \omega_n$ then this excess noise is added on top of what was already accounted for in the linear analysis. Since these noise sources are uncorrelated, the powers rather than voltages must be added and this means that about 3dB of noise is added to what is predicted by the linear analysis. Thus, the noise content at an offset frequency is:

$$PN = \left(\frac{A\omega_o}{(2Q\Delta\omega)} \right)^2 \left(\frac{FkT}{2P_s} \right) + \left(\frac{v_{nl}K_{VCO}}{2\Delta\omega} \right)^2 \quad (112)$$

where A is approximately $\sqrt{2}$. Note that in this derivation it has been assumed that flicker noise is insignificant at the frequencies of interest. This may not always be the case especially in CMOS designs. In addition, this formula is no longer valid once the noise floor is reached. At this point the noise will become flat.

5.5 Some Notes on Low Frequency Noise and Varactor Placement

As can be seen from the last section, low frequency noise can be very important in the design of VCOs. Thus, the designer should be very careful as to how the varactors are placed in the circuit. Take, for instance, the circuit shown in Fig 33. Suppose that a low frequency noise current were injected into the tank, either from the transistors Q1 or Q2 or the current source at the top of the tank. This current will see an impedance equal to the output impedance of the current source in parallel with the transistor loading (two forward biased diodes in parallel). This would be given by:

$$R_{Load} = r_{cur} // r_{e1} // r_{e2} \approx \frac{r_e}{2} \quad (113)$$

where r_{cur} is the output impedance of the current source and the transistors are assumed to be identical.

This impedance given by (113) could easily be in the tens of ohms. Compare this to the circuit shown in Fig. 25. In the case of Fig. 25, noise currents have only the DC series

resistance of the inductor coil over which to develop a voltage. Thus, if low frequency noise starts to dominate in the design, this topology would obviously be the better choice.

Fig 33. An oscillator topology sensitive to low frequency noise.

There are some circumstances for which a topology like the one shown in Fig 33 are unavoidable. As an example, over the last while a new form of varactor known as the CMOS accumulation mode varactor which requires both positive and negative voltages has become popular in CMOS and BiCMOS technologies [35][36]. When using such a varactor there is no choice but to place it in the circuit without the terminals connected to V_{cc} .

5.6 A Low Voltage Version of the $-G_m$ VCO

In order to reduce the supply voltage required for this circuit, it is proposed to DC decouple the bases of Q1 and Q2 from the collectors using capacitors. Then, the current source can be removed and mirroring the base of each transistor can set the bias. This removes any transistor stacking and allows this circuit to be operated at a voltage only slightly higher than the turn on voltage of the transistors. The circuit with these modifications and biasing is shown in Fig. 34. Alternatively, the bases can be coupled to

the collectors by use of a transformer rather than capacitors as shown in Fig. 35. The transformer can be given a turns ratio greater than unity to reduce the swing on the base. The transformer has the added advantage that the bias may be provided at the center tap avoiding the need for RF blocking resistors. The removal of these resistors along with the addition of a capacitor on the bias line keeps the noise injected into the oscillator to a minimum. However, when the current source is removed from the tail of the VCO this makes the current very hard to control. When the VCO starts up, the circuit will tend to draw huge current pulses from the supply. Thus, to some degree the transistor size will determine the average current from the supply. Nevertheless, as the supply voltage comes close to one volt there is little other choice.

A more conservative approach is to use a resistor in the tail, as shown in Fig. 36. In this case, the voltage swing is controlled with the addition of diodes across the tank and noise from the bias is cleaned up with the addition of a capacitor. The current through the oscillator is limited with the use of a resistor R_{E1} rather than a current source, because the resistor needs much less headroom to accommodate it. As well, the resistor may be less noisy than a current source. Furthermore, to keep the amplitude of the oscillation constant, clamping diodes may be placed across the tank preventing the amplitude from growing beyond $1.8V_{pp}$. This keeps noise from causing amplitude fluctuations in the oscillator. These fluctuations would otherwise tend to get modulated by the VCO and upconverted around the carrier and converted into phase noise.

Note also that as the voltage supply is lowered on these circuits, the available range for the tuning voltage is also reduced, making it harder to achieve a given range of oscillating frequencies. The designer has few alternatives to counter this problem. The inductance can be decreased and the capacitance increased to a point (sacrificing phase noise in the process), but beyond this, it may be that the tuning requirements are the deciding factor on how low the voltage can be dropped.

Fig. 34. Modified low voltage $-G_m$ voltage-controlled oscillator with biasing. Capacitor coupling version.

Fig. 35. Modified low voltage $-G_m$ voltage-controlled oscillator with biasing. Transformer coupled version.

Fig. 36. Schematic of a low voltage VCO.

5.7 Automatic Amplitude Control for VCOs

To get the best performance from a VCO, it needs to be biased at an optimum level. Unfortunately, due to process variations etc., it is very difficult to do this without some form of feedback around the VCO. The following two sections describe two possible methods for providing this feedback. In each, a circuit topology for some test VCOs that were built are described.

5.7.1 The VCO With Analog Control Loop

A basic VCO core (although not a low voltage one) with an analog control loop is shown in Fig. 37. Transistors Q3 and Q4 are used to limit the swing of the oscillator to slightly more than one V_{BE} . Once the oscillation amplitude reaches this level, these transistors start to turn on briefly at the top and bottom of the oscillator's swing, loading the tank with their dynamic emitter resistance. This will effectively de-Q the circuit and prevents the signal from growing any larger. This will prevent transistors Q1 and Q2 from entering saturation. However, if transistors Q3 and Q4 have to be heavily turned on to limit the swing, they will also start to affect the phase noise performance of the circuit.

Fig. 37. VCO topology with analog control loop.

The transistors Q3 and Q4 limit the amplitude of the oscillation directly, but are also the basis for the second mechanism that is used to make sure that the VCO is operating at an optimal level. Once these transistors start to turn on, they start to draw current I_f . Their collectors are connected back to the source of the PMOS device M1. The gate of M1 is connected to a reference that is generated by a bandgap circuit (omitted from the diagram for simplicity). Q3 and Q4 then steal current away from M1 causing the current in Q6 to be reduced. This in turn reduces the current in the VCO. Since the VCO amplitude is related to its current, this in turn reduces the amplitude of the VCO until the transistors Q3 and Q4 just barely turn on. This ensures that the VCO always draws just enough current to turn on these transistors and no more, even though the reference currents may vary for any number of reasons. The reference current through M1 must therefore be set higher than the optimum, as the loop can only work to reduce the current through the oscillator, but can never make it higher. Note that it is important that initial start up current for the oscillator be reasonably close to the final value needed. If the current is

too high, then the limiting transistors will have to be turned on for a large portion of the cycle and they will cause the phase noise to degrade. However under normal operation they should not degrade the phase noise performance by more than a couple of dB beyond that which could be achieved without the limiters under ideal conditions.

The loop can be drawn conceptually as shown in Fig. 38. The point P shown in Fig. 37 acts as a summing node for the three currents I_{in} , I_{bias} , and I_f . The current mirror amplifies this current and produces the tank current, which is taken by the VCO core and produces an output voltage proportional to the input tank current. The limiting transistors at the top of the tank convert the VCO amplitude into a current that is fed back to the input of the loop.

Fig. 38. Conceptual drawing of the AAC feedback loop.

The transfer function for the various blocks around the loop can now be derived. In the current mirror, a capacitor C_1 is included to reduce the power used by Q7. C_2 has been placed in the circuit to limit the frequency response of the circuit. It creates a dominant pole in the system (this helps to control the effect of parasitic poles on the system) and limits the frequency response of the loop. The transfer function for this part of the loop is given by:

$$A_1(s) = \frac{I_{Tank}(s)}{I_{bias}(s)} \approx \frac{\frac{g_{m6}}{C_2} \left(s + \frac{g_{m7}}{C_1} \right)}{s^2 + \left(\frac{g_{m7}}{C_1} + \frac{g_{m6}}{C_2} \right) s + \frac{g_{m6}g_{m7}}{C_1C_2}} \quad (114)$$

This equation has a dominant pole at:

$$P \approx \frac{g_{m6}}{C_2} \quad (115)$$

The behaviour of the oscillator must also be determined in so far as it effects the behaviour of the loop. We have already shown that the VCO amplitude can be approximated by (92). This formula has obvious limitations in describing certain aspects of oscillator performance. Specifically, for large amplitudes the oscillation amplitude will cease to grow with increasing current and for low current the VCO will not start. More importantly, this expression also fails to capture the frequency response of the oscillator amplitude.

For the purposes of this analysis, the oscillator tank is treated as a resonator with a pulse of current applied to it by transistors Q1 and Q2 each half cycle. From this simple model the transient behaviour of the circuit can be determined. The resonator forms a time constant $R_T C_{var}$ that is equivalent to a pole in the response of the oscillation amplitude versus bias current. This pole can be used to give frequency dependence to (92).

$$A_2(s) = \frac{V_{Tank}(s)}{I_{Tank}(s)} = \frac{2}{\pi C_{var}} \left(\frac{1}{s + \frac{1}{R_T C_{var}}} \right) \quad (116)$$

This pole can also be written in terms of the Q and frequency of oscillation:

$$P = \frac{1}{C_{var} R_T} = \frac{\omega_{osc}}{2Q} \quad (117)$$

It is interesting to note that a tank with higher Q will respond slower, and therefore have a lower frequency pole than a low Q oscillator. This makes intuitive sense, since it is up to the losses in the tank to cause a change in amplitude.

The last part of the loop consists of the limiting transistors. This is the hardest part of the loop to characterise, because by their very nature, the limiters are very non-linear. The transistor base is essentially grounded while the emitter is attached to the tank of the oscillator. In the scheme that has been shown, the base is connected to a voltage higher than the tank voltage. For any reasonable applied tank voltage, the current will form narrow pulses with large peak amplitude. Thus, this current will have strong harmonic

content. This harmonic content will lead to a non-zero DC current, which is the property of interest. Finding it requires solving the following integral.

$$I_{C_AVE} = \frac{1}{2\pi} \int_0^{2\pi} I_S e^{\frac{V_{Tank} \sin(\theta)}{2V_T} + \frac{V_{BEQL}}{V_T}} d\theta = I_S e^{\frac{V_{BEQL}}{V_T}} I_0\left(\frac{V_{Tank}}{2V_T}\right) \quad (118)$$

Where $I_0(x)$ is a modified Bessel function of the first kind of order zero, V_{BEQL} is the quiescent bias voltage of the limiters, and I_S is the saturation current. For fairly large $V_{Tank}/2V_T$ there is an approximate solution:

$$I_{C_AVE} \approx \frac{I_S e^{\frac{V_{BEQL}}{V_T}} \cdot e^{\frac{V_{Tank}}{2V_T}}}{\sqrt{2\pi \frac{V_{Tank}}{2V_T}}} \quad (119)$$

Now we can write the gain of this part of the loop, which is a non-linear function of V_{Tank} (all other parts of the loop were described by linear functions):

$$A_3(s) = 2 \frac{\partial I_{C_AVE}}{\partial V_{Tank}} = \frac{I_S e^{\frac{V_{BEQL}}{V_T}} \cdot e^{\frac{V_{Tank}}{2V_T}}}{\sqrt{\pi V_T V_{Tank}}} - \frac{I_S e^{\frac{V_{BEQL}}{V_T}} \cdot e^{\frac{V_{Tank}}{2V_T}}}{\sqrt{\frac{\pi}{V_T} V_{Tank}^{\frac{3}{2}}}} \quad (120)$$

Here it is assumed that this part of the loop has poles at significantly higher frequency than the one in the VCO and the one in the mirror.

These equations can be used to design the loop and demonstrate the stability of this circuit. The capacitor C_2 is placed in the circuit to create a dominant and controllable pole P_1 significantly below the other pole P_2 . Generally the frequency of P_2 and gain of $A_2(s)$ are set by the oscillator requirements and are not adjustable. For more stability, the loop gain can be adjusted by either changing the gain in $A_1(s)$ (by adjusting the ratio of the current mirror) or by adjusting the gain of $A_3(s)$ (this can be done by changing the size of the limiting transistors Q3 and Q4). Reducing the gain of the loop is a less desirable alternative than adjusting P_1 because as the loop gain is reduced its ability to settle to an exact final value is reduced.

5.7.2 The VCO With Digital Control Loop

The VCO core for the digital loop is shown in Fig. 39. It uses degeneration resistors as current sources. Compared to current sources, these resistors need much less voltage

headroom to operate properly, which means that V_{ref} can be reduced. Thus, the amplitude of the VCO can be allowed to grow to almost twice the value in the previous design without saturating the tank transistors Q1 and Q2. The problem with using a resistor as a current source is that there is no convenient way to make it adjustable. Thus, a set of resistors with transistor switches can be used in this topology. The switches provide many possible settings for the value of the degeneration resistance. One non-switched resistor R_f is also included to avoid a state where all resistors are open. As well, in this topology two sets of identical varactors are included which are connected to a digital control signal. Thus there are three selectable frequency bands shown here. This is done in an effort to keep the K_{VCO} smaller, which in general, reduces phase noise, and has other beneficial implications on the PLL design. Since in the analog design, the limiters also provide an advantage in that they suppress amplitude fluctuations, two versions of this core are shown with and without limiters. Limiters are shown as transistors Q3 and Q4.

Fig. 39. VCO topology with adjustable degeneration resistors.

The switchable resistors were chosen to be binary weighted. Thus, if the signals that drive the switches are considered digital bits, then the resulting digital word can be thought of as a number between 0 and 2^n-1 and the total resistance is inversely proportional to the value of this word. The switchable resistor and fixed resistor values are usually chosen so that the ratio of the maximum to minimum resistance was roughly a factor of 6:1. This range was chosen so that the best degeneration value could still be chosen under any extremes of temperature, process, or frequency variation with margin.

The complete feedback loop is shown in Fig. 40. The peak detector output is fed into two comparators, which are used to produce two digital signals: count up and count down. These are then fed into a 6 bit counter which responds to these two signals and produces an output between 0 and 63. This output is then used to make adjustments in the VCO. Note that the counter is designed so that it will not cycle. Thus, for example, if it receives a count up signal when it is at a count of 63 then it will not go to a count of zero. This takes care of the possibility that if more or less degeneration is required than can be provided that the loop will not cycle slip and become unstable.

Fig. 40. The Digital AAC loop.

Unlike the analog loop, instability due to the system poles is not really a concern in this design, as the clock frequency creates a dominant and very low frequency pole at $1/f_{clk}$. Of more concern is whether or not the loop will be able to find a final value. There must be a value of degeneration that will allow the peak detector to put out a value between V_{Hi} and V_{Low} , or V_{Hi} and V_{Low} must be sufficiently far apart to guarantee that at least one value of V_{peak} will fall between these two values. If there is insufficient resolution, then the loop could “hunt” between two adjacent counts continuously.

5.8 Conclusions

In this chapter, methods for the design of on-chip VCOs have been reviewed. A method for biasing a $-G_m$ VCO so that it may operate using a supply voltage as low as 1 volt has been proposed. As well, two methods to optimally bias the VCO for best phase noise performance with feedback have been discussed. These VCOs are an essential part of almost any receiver. The phase noise of an oscillator was reviewed as well, including nonlinear effects, and a noise factor for the transistor has been defined to help determine how much extra noise is added due to active circuitry. Since VCO performance is very sensitive to the quality of the passives used in its construction, the design of on-chip inductors and transformers has been discussed in a previous chapter. Next, we will make use of the understanding of VCOs developed here to help build on-chip filters.

Chapter 6: The Problem of Image Rejection

6.1 Basic Theory

An RF signal consists of a carrier with information modulated on it. The task of the receiver front-end is to take this information and mix it either to base band or to some intermediate frequency (IF) where it can be more easily processed. A receiver in which the signal is taken directly to base band is called a Homodyne or direct conversion receiver. Although simpler than a receiver that takes the signal to some IF first, (called a superheterodyne receiver) direct conversion receivers suffer from numerous problems including DC offsets because much of the information is close to DC and also because of LO self mixing [5]. Thus, although there has been much work recently on direct conversion receivers, superheterodyne receivers are still more generally accepted in industry and will be the type considered in this work.

A superheterodyne receiver takes the desired RF input signal and mixes it with some reference signal to extract the IF as shown in Fig 41. The problem is that a signal on the other side of the LO, the image, at the same distance from the LO will also mix down “on top” of the desired frequency. Thus, before mixing can take place, this unwanted image frequency must be removed. Typically, this is done with a filter that attenuates the image.

Fig 41. Translation of the RF signal to an IF in a superheterodyne receiver.

Thus, a typical superheterodyne receiver front-end consists of a low noise amplifier (LNA), an image filter, a mixer, and a VCO as shown in Fig 42. The image filter is required to suppress the unwanted image frequency, which is located a distance of two intermediate frequencies (IFs) away from the desired radio frequency [6].

Fig 42. A block level diagram of a superheterodyne receiver front-end.

Currently, off-chip passive filters, such as surface acoustic wave (SAW) filters or ceramic filters, are used for image rejection in the low GHz frequency range. These filters represent a major impediment to raising the level of integration of wireless radios, since they cannot be easily implemented monolithically. Their use also complicates the design of the receiver front-end. The LNA must be designed to drive 50Ω as its output comes off chip. Matching from the LNA to the filter must therefore be performed either on-chip or on the board. The filter must then be matched to the mixer input, which must also be driven by 50Ω . This also means that large RF signals are present on two bond wires in the package used for the receiver. Since bond wires are a major source of signal coupling, this will lead to increased signal coupling between ports in the receiver. Additional pins must be included to accommodate the filter, leading to more expensive packages. These filters themselves also represent a significant fraction of the overall cost of the receiver front-end.

6.2 An Image Reject Mixer

An alternative to using an image reject filter is to use an image reject mixer for cancellation of the image. The topology for such a mixer is shown in Fig 43[7][5]. Note that the low pass filter (LPF) is shown here as part of the IR mixer. However, in practical

applications the filter may be implemented after the addition of the two signals has been performed. In this example the RF signal enters the mixer accompanied by an image. It is assumed that the LO is high-side injected and therefore the image is at a higher frequency than the desired RF signal. If the LO were low side injected then the 90° phase shift would have to be moved to the other path and the mixer would reject the other side, or alternatively, the signals could be subtracted at the output.

6.2.1 The Basic Operation of the Image Reject Mixer

The ideal requirements are that a phase shift of exactly 90° is generated in the signal path and that the LO has perfect quadrature output signals. In a perfect system there is also no gain mismatch in the signal paths. In a real circuit implementation, there will be imperfections, therefore, an analysis of how much image rejection can be achieved for a given phase and amplitude mismatch is now performed. This analysis is based loosely on that presented in [9]. Although a different architecture is used in this case, the result ends up being identical.

Fig 43. Block diagram of an image-reject mixer including phase and gain errors.

The analysis proceeds as follows:

- 1) The input signal is mixed with the quadrature LO signal through the I and Q mixers to produce signals V_1 and V_2 after filtering. V_1 and V_2 are given by:

$$V_1 = \frac{1}{2} \sin(\omega_{LO} - \omega_{RF})t - \frac{1}{2} \sin(\omega_{IM} - \omega_{LO})t \quad (121)$$

$$V_2 = \frac{1}{2} \cos[(\omega_{LO} - \omega_{RF})t + \phi_{\epsilon 1}] + \frac{1}{2} \cos[(\omega_{IM} - \omega_{LO})t - \phi_{\epsilon 1}] \quad (122)$$

- 2) Now V_1 experiences an amplitude error relative to V_2 and V_2 experiences a phase shift that is not exactly 90° to give V_3 and V_4 respectively.

$$V_3 = \frac{1}{2} (1 + \Delta A) \sin(\omega_{LO} - \omega_{RF})t + \frac{1}{2} \sin(\omega_{IM} - \omega_{LO})t \quad (123)$$

$$V_4 = \frac{1}{2} \sin[(\omega_{LO} - \omega_{RF})t + \phi_{\epsilon 1} + \phi_{\epsilon 2}] + \frac{1}{2} \sin[(\omega_{IM} - \omega_{LO})t - \phi_{\epsilon 1} + \phi_{\epsilon 2}] \quad (124)$$

- 3) Now V_3 and V_4 are added together. The component of the output due to the RF signal is denoted V_{RF} and is given by:

$$V_{RF} = \frac{1}{2} (1 + \Delta A) \sin(\omega_{IF}t) + \frac{1}{2} \sin(\omega_{IF}t + \phi_{\epsilon 1} + \phi_{\epsilon 2}) \quad (125)$$

$$V_{RF} = \frac{1}{2} (1 + \Delta A) \sin(\omega_{IF}t) + \frac{1}{2} \sin(\omega_{IF}t) \cos(\phi_{\epsilon 1} + \phi_{\epsilon 2}) + \frac{1}{2} \cos(\omega_{IF}t) \sin(\phi_{\epsilon 1} + \phi_{\epsilon 2}) \quad (126)$$

- 4) The component due to the image is denoted V_{IM} and is given by:

$$V_{IM} = -\frac{1}{2} (1 + \Delta A) \sin(\omega_{IF}t) + \frac{1}{2} \sin(\omega_{IF}t) \cos(\phi_{\epsilon 2} - \phi_{\epsilon 1}) + \frac{1}{2} \cos(\omega_{IF}t) \sin(\phi_{\epsilon 1} - \phi_{\epsilon 2}) \quad (127)$$

- 5) It is only the ratio of the magnitudes that are important. These are given by:

$$|V_{RF}|^2 = \frac{1}{4} \left[[\sin(\phi_{\epsilon 1} + \phi_{\epsilon 2})]^2 + [(1 + \Delta A) + \cos(\phi_{\epsilon 1} + \phi_{\epsilon 2})]^2 \right] \quad (128)$$

$$|V_{RF}|^2 = \frac{1}{4} \left[1 - (\cos(\phi_{\epsilon 1} + \phi_{\epsilon 2}))^2 + (1 + \Delta A)^2 + 2(1 + \Delta A) \cos(\phi_{\epsilon 1} + \phi_{\epsilon 2}) + (\cos(\phi_{\epsilon 1} + \phi_{\epsilon 2}))^2 \right] \quad (129)$$

$$|V_{RF}|^2 = \frac{1}{4} \left[1 + (1 + \Delta A)^2 + 2(1 + \Delta A) \cos(\phi_{\epsilon 1} + \phi_{\epsilon 2}) \right] \quad (130)$$

$$|V_{IM}|^2 = \frac{1}{4} \left[(\sin(\phi_{\epsilon 1} - \phi_{\epsilon 2}))^2 + [-(1 + \Delta A) + \cos(\phi_{\epsilon 2} - \phi_{\epsilon 1})]^2 \right] \quad (131)$$

$$|V_{IM}|^2 = \frac{1}{4} \left[1 - (\cos(\phi_{\epsilon 2} - \phi_{\epsilon 1}))^2 + (1 + \Delta A)^2 - 2(1 + \Delta A) \cos(\phi_{\epsilon 2} - \phi_{\epsilon 1}) + (\cos(\phi_{\epsilon 1} + \phi_{\epsilon 2}))^2 \right] \quad (132)$$

$$|V_{IM}|^2 = \frac{1}{4} \left[1 + (1 + \Delta A)^2 - 2(1 + \Delta A) \cos(\phi_{\epsilon 2} - \phi_{\epsilon 1}) \right] \quad (133)$$

- 6) Therefore the image rejection ratio is given by:

$$IRR = 10 \log \frac{|V_{RF}|^2}{|V_{IM}|^2} = 10 \log \left[\frac{1 + (1 + \Delta A)^2 + 2(1 + \Delta A) \cos(\phi_{\epsilon 1} + \phi_{\epsilon 2})}{1 + (1 + \Delta A)^2 - 2(1 + \Delta A) \cos(\phi_{\epsilon 2} - \phi_{\epsilon 1})} \right] \quad (134)$$

If there is no phase imbalance or amplitude mismatch, then this equation approaches infinity, and so ideally this system will reject the image perfectly and it is only the nonideality of the components that cause finite image rejection.

6.2.2 Implementation of Phase Shifters

By looking at the previous analysis it is easy to see that there is a need to implement very accurate phase shifting networks if a reasonable amount of image rejection is to be achieved. One of the best ways to do this is with the use of polyphase filters [11]. A polyphase filter driven by a source is shown in Fig 44. The filter is designed such that at a particular frequency, all outputs are 90° out of phase with each other. The filter also has the property that with each additional stage, phase shifts become more precisely 90° even with a certain amount of tolerance on the parts. Thus, when they are used in an image-reject mixer, if more image rejection is required, then polyphase filters with more stages can be employed. The drawback is that with each additional stage there is some loss through the filter putting a practical upper limit on the number of stages that can be used. The frequency at which the phase shift is exactly 90° is given by

$$\omega = \frac{1}{RC} \quad (135)$$

Fig 44. An N stage polyphase filter.

6.3 On-Chip Image Reject Filters

So far, few on-chip implementations of image rejection filters have been reported [13]-[16]. However, if the effort is made to integrate the filter, then the signal never has to leave the chip before reaching the IF stage in the receiver chain. Thus, a simpler, cheaper package can be used and the costly off-chip filter is eliminated. In this work notch filters will be considered for the duty of image rejection. The main advantage to using a notch filter over a bandpass filter is that with only a two pole filter good image rejection can be achieved, while in the case of a bandpass filter six or eight poles would be needed for even reasonably high IF frequencies. The draw back to notch filters is they only reject one frequency so for instance if the LO signal has strong harmonic content then there can be multiple “image” frequencies that a notch filter could not help to filter out. Note that image filtering does not help with in-band blockers. These must be dealt with by making the receiver sufficiently linear so these interferers are not a problem.

6.3.1 Basic Operation of an Image Reject Filter

The following is a proposal for the addition of notching action to a conventional LNA topology. Previous image reject receiver designs have followed the LNA with an additional stage, which performed the image rejection for the receiver [13]. In the approach disclosed here, the conventional topology for a cascode LNA shown in Fig. 45 is modified by replacing the inductor L_{e1} with a resonator. The LC resonator will be centered at the notch frequency and will therefore present a high impedance to the emitter of the driving transistor. A high impedance here will mean that the driver will have a very low gain (ideally a zero gain) at the image frequency. Thus, the LNA will reflect the image. Below the resonance frequency of the LC tank, the resonator will look inductive and will have an impedance close to that of the actual inductor placed in the circuit. Thus, in the pass band the LNA will still look like an LNA with inductive degeneration. Note as well that due to the capacitor at some frequency beyond resonance

the emitter will have a net capacitance associated with it. This will lead to some negative resistance generated in the base. Thus the circuit will not be unconditionally stable at these frequencies.

Fig. 45. A traditional cascode LNA configuration.

Unfortunately, there will be losses associated with the proposed LC resonator that will seriously impact its effectiveness. To reduce these losses, some form of active circuitry must be added in addition to a simple capacitor in parallel with the inductor. This idea is shown conceptually in Fig. 46. This circuitry must add negative resistance to the circuit to compensate for the losses in the LC resonator. A simple way to implement this is to add feedback around two series capacitors as shown in Fig. 47. Note that one of the capacitors, C_{f2_var} must be implemented using a tunable capacitance to make the filter tunable. Due to process variations, the current I_{sharp} may need to be tuned as well to ensure perfect cancellation of the losses in the resonator.

Fig. 46. LNA with image rejection shown with ideal components.

Fig. 47. Complete LNA with image rejection and biasing shown.

The capacitor C_{cp} unfortunately, has to be quite large in order not to affect the performance of the filter. It can therefore have a large parasitic capacitance to ground. An alternative to capacitive coupling is to use inductive coupling as shown in Fig. 48.

Fig. 48. Complete LNA with image rejection and biasing shown using transformer coupling.

The last two figures have shown the filter implemented with a Collpits style negative resistance. However, there is no reason why this resonator cannot also be built out of a $-G_m$ style resonator as shown in Fig. 49.

Fig. 49. Complete LNA with image rejection and biasing shown using transformer coupling and a $-G_m$ resonator.

6.3.2 Analysis of the LNA with Notching Action

When dealing with filters and high-Q resonators, stability is always a concern. In particular, with the circuit topology shown in Fig. 46, beyond the notch frequency there will be a large negative resistance generated looking into the base of Q1 due to the presence of the capacitance C_E in the resonator. The following analysis can also be used to show the operation of the circuit, but equations often generate less insight than a qualitative description of the circuit.

For the purposes of this analysis, the simplified small-signal model for the circuit shown in Fig. 50 will be used. Here the complex resistance is reflected into the base and is

placed in series with the transistor's input impedance Z_π . The output is modeled as a simple voltage-controlled current source driving the tank at the collector of the cascode transistor. For the purposes of this analysis the cascode is assumed to have a current gain of one with no phase shift.

Fig. 50. Simple model of the LNA for analysis.

From this diagram, it is easy to see that the input impedance of the amplifier is given by:

$$Z_{in} = Z_\pi + Z_E(1 + g_m Z_\pi) \quad (136)$$

If the transistor's impedance is assumed to be capacitive, and the emitter impedance is composed of a perfect inductor L_E , then this expression can be rewritten as:

$$Z_{in} = \frac{1}{sC_\pi} + sL_E + g_m \frac{sL_E}{sC_\pi} = \frac{1}{sC_\pi} + sL_E + g_m \frac{L_E}{C_\pi} \quad (137)$$

Thus, as shown in the LNA chapter, it can be seen that inductive degeneration can generate positive resistance looking into the base. Similarly, capacitive degeneration generates negative resistance looking into the base. In fact, one of the major reasons why capacitive degeneration of amplifiers is not commonly used is because this negative resistance can lead to instability. Fortunately for this work, negative resistance is only generated above the notch frequency. After the notch frequency, the overall resistance will be negative over a narrow frequency band if the inductance and capacitance ratio is chosen properly in this circuit. Since the input will resonate in the passband frequencies before the input resistance goes negative, the circuit can be designed to be stable. Nevertheless, a more rigorous analysis follows.

The transfer function, $T(s)$, for this circuit can be derived using Fig. 50. With only minimal effort, it can be shown that:

$$T(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{-g_m Z_\pi Z_T}{Z_E(1 + g_m Z_\pi) + Z_\pi + R_S} \quad (138)$$

If the general case is now assumed where Z_T and Z_E are assumed to be parallel LCR tanks, and Z_π is assumed to be a resistor in parallel with a capacitor then the transfer function can be derived. After some manipulation:

$$Z_\pi = \frac{r_\pi}{C_\pi r_\pi s + 1} \quad (139)$$

$$Z_E = \frac{\frac{s}{C_E}}{s^2 + \frac{s}{R_E C_E} + \frac{1}{L_E C_E}} \quad (140)$$

$$Z_T = \frac{\frac{s}{C_1}}{s^2 + \frac{s}{R_1 C_1} + \frac{1}{L_p C_1}} \quad (141)$$

Substituting these expressions into the transfer function given in (138) and after much manipulation:

$$T(s) = \frac{-g_m \left(s^3 + \frac{s^2}{C_E R_E} + \frac{s}{L_E C_E} \right)}{\left(s^2 + \frac{s}{C_1 R_1} + \frac{1}{L_p C_1} \right) \left[C_\pi R_S s^3 + \left(1 + \frac{C_\pi}{C_E} + \frac{R_S}{r_\pi} + \frac{C_\pi R_S}{C_E R_E} \right) s^2 + \left(\frac{1}{C_E R_E} + \frac{1}{r_\pi C_E} + \frac{g_m}{C_E} + \frac{R_S}{R_E C_E r_\pi} + \frac{C_\pi R_S}{L_E C_E} \right) s + \left(\frac{1}{L_E C_E} + \frac{R_S}{L_E C_E r_\pi} \right) \right]} \quad (142)$$

Examining (142), stability must be ascertained. In order to do this, the pole locations for (142) must be determined. This is a fifth order system with five poles. Two of the poles are from the tank at the collector of the cascode transistor and are safely in the left half plane.

The remaining poles are difficult to solve analytically, so instead they are plotted with the assistance of Matlab in Fig. 51. It can be seen that even as R_E approaches infinity (as is the intention in this application) the poles will remain in the left half plane. In fact, the

circuit losses would have to be highly over compensated to drive them into the right half plane (an equation for this will follow shortly). From the plot it is easy to see that only if the losses in the emitter tank are overcompensated, will the system become unstable. In practice however, there should be some margin or the system may in fact start oscillating.

The zeros can also be determined from (142) as well. Again, letting R_E approach infinity and setting the numerator equal to zero, it is found that there are zeros at:

$$s_{1,2,3,4,5} = 0, \pm \frac{1}{L_E C_E}, \infty, \infty \quad (143)$$

Equation (143) shows clearly that the zeros of the system are placed at the frequency where the tank in the emitter resonates as expected.

Fig. 51. Plot of the poles of the filter showing potential instability.

6.3.3 Some Simple Image Rejection Formulas

Formulas for the amount of image rejection for the circuit of Fig. 46 will now be developed. Noting that well below resonance, an LC tank will have an impedance given roughly by the reactance of the inductor, and well above resonance it will have an

impedance roughly that of its capacitor we can develop the following equations. First, the gain in the pass band G_{PB} of the filter is given by:

$$G_{PB} = \frac{Z_L}{Z_e} = \frac{R_1}{\omega_{PB} L_E} \quad (144)$$

since the tank at the collector is resonating and the tank in the emitter is below resonance.

The gain in the stop band G_{SB} is given by:

$$G_{SB} = \frac{Z_L}{Z_e} = \frac{1}{\omega_{SB} C_1 R_{Tot}} \quad (145)$$

where the tank at the collector is at a frequency above its resonance frequency and the tank in the emitter is now resonating with total resistance R_{Tot} which is made up of tank losses R_E and negative resistance generated by active circuitry as shown in Fig. 46.

Thus, R_{Tot} can be approximated as:

$$R_{Tot} = \frac{R_E R_{neg}}{R_E + R_{neg}} \quad (146)$$

In the case of the $-G_m$ cell in Fig. 49 with a transformer present with inductance ratio N_L , R_{Tot} is given by:

$$R_{Tot} = \frac{R_E R_{neg}}{R_E + R_{neg}} = \frac{-2N_L R_E}{g_m R_E - 2N_L} \quad (147)$$

where g_m is the tranconductance of either Q3 or Q5 in Fig. 49.

Thus the image rejection IR can be approximated as:

$$IR = 20 \log \left(\frac{G_{PB}}{G_{SB}} \right) = 20 \log \left[\frac{R_1 \omega_{SB} C_1}{\omega_{PB} L_E} \left(\frac{R_E R_{neg}}{R_E + R_{neg}} \right) \right] \quad (148)$$

Again in the case of the $-G_m$ cell with a transformer:

$$IR = 20 \log \left[\frac{R_1 \omega_{SB} C_1}{\omega_{PB} L_E} \left(\frac{-2N_L R_E}{g_m R_E - 2N_L} \right) \right] \quad (149)$$

This formula shows that the image rejection can be made infinite with proper adjustment of g_m , but this is not true because there will always be some finite amount of signal leakage due to the presence of C_μ . If the filter is perfectly tuned, then only this parasitic path will remain. In this case the gain derivation is as follows. Signal leaks through C_μ , causing a current to flow into the cascode transistor:

$$i = \frac{v_{in}}{\frac{1}{g_m} + \frac{1}{j\omega C_\mu}} \quad (150)$$

This current is passed onto the load which has a reactive impedance and develops a voltage there:

$$v_{out} = \frac{i}{j\omega C_1} = \left(\frac{v_{in}}{\frac{1}{g_m} + \frac{1}{j\omega C_\mu}} \right) \left(\frac{1}{j\omega C_1} \right) \quad (151)$$

thus:

$$\frac{v_{out}}{v_{in}} = \frac{1}{\frac{j\omega C_1}{g_m} + \frac{C_1}{C_\mu}} \quad (152)$$

the magnitude of this expression gives the minimum achievable stop band gain for the circuit:

$$G_{SB\min} = \frac{1}{\sqrt{\left(\frac{\omega_{SB} C_1}{g_m} \right)^2 + \left(\frac{C_1}{C_\mu} \right)^2}} \quad (153)$$

Therefore the minimum image rejection that can be achieved is:

$$IR_{\min} = 20 \log \left(\frac{R_1}{\omega_{PB} L_E} \sqrt{\left(\frac{\omega_{SB} C_1}{g_m} \right)^2 + \left(\frac{C_1}{C_\mu} \right)^2} \right) \quad (154)$$

6.3.4 Interpretation of Filter Stability

The stability analysis in section 6.3.2 though reassuring, fails to provide much design insight into the problem of making the filter stable. In this section a simpler interpretation of stability will be presented. The fundamental problem is non-trivial: how to stabilize an LC resonator specifically designed to have infinite Q? After all, an LC oscillator design begins with a resonator with infinite Q [5][7]. The mechanism for damping the oscillation must come from either the source or load impedance. In previous work, the cascode transistor provided damping for the resonator. In this circuit, the source impedance must damp the filter as shown in Fig. 52.

For perfect notching, the negative resistance must equal the tank losses R_E , so in the case of a $-G_m$ resonator:

$$\frac{2}{g_m} = R_E \quad (155)$$

Thus the optimal current must be:

$$I_{sharp_opt} = \frac{2V_T}{R_E} \quad (156)$$

To start an oscillation:

$$\frac{2}{g_m} = R_E // R_s \quad (157)$$

therefore, for oscillations to start, a current of:

$$I_{sharp_osc} = \frac{2V_T(R_E + R_s)}{R_E R_s} \quad (158)$$

is required. The ratio of these two currents is then given by:

$$\frac{I_{osc}}{I_{notch}} = 1 + \frac{R_E}{R_s} \quad (159)$$

Thus, if the source resistance is smaller than the tank resistance R_E then the tank can be safely tuned to provide infinite Q and still have ample damping. However, if the tank resistance is smaller than the source resistance, then even a small error in tuning the tank to infinite Q could result in oscillation.

Fig. 52. Illustration of how the filter is damped without diminishing image rejection.

6.3.5 Linearity of the Filter

The filter resonator has to process signals just as the rest of the receive path does. If a very large signal is present on the resonator it will cease to work correctly. Large signals will tend to change the effective g_m of the transistors in the resonator, for example Q3 and Q4 of Fig. 49, and therefore the negative resistance. Thus, as signals get larger, we can expect degradation in the amount of image rejection that the circuit delivers.

As shown previously, if a transistor is driven with a voltage source v_{in} and has no degeneration then:

$$i_c = I_C \left[1 + \frac{v_{in}}{V_T} + \frac{1}{2} \left(\frac{v_{in}}{V_T} \right)^2 + \frac{1}{6} \left(\frac{v_{in}}{V_T} \right)^3 + \dots \right] \quad (160)$$

we now find the g_m of this circuit without making a small signal assumption:

$$g_m = \frac{di_c}{dv_{in}} = I_C \left[\frac{1}{V_T} + \frac{v_{in}}{V_T^2} + \frac{1}{2} \frac{v_{in}^2}{V_T^3} + \dots \right] = g_{mss} \left[1 + \frac{v_{in}}{V_T} + \frac{1}{2} \frac{v_{in}^2}{V_T^2} + \dots \right] \quad (161)$$

Provided that v_{in} remains relatively small, this takes on the small-signal value g_{mss} of I_C/V_T . However, as the signal grows this value changes.

Thus, in the case of the $-G_m$ resonator, the amount of negative resistance generated is:

$$\frac{R_{neg}}{R_{negss}} = \frac{\frac{-2}{g_m}}{\frac{-2}{g_{mss}}} = \left[1 + \frac{v_{in}}{V_T} + \frac{1}{2} \frac{v_{in}^2}{V_T^4} + \dots \right]^{-1} \quad (162)$$

The voltage across the resonator is twice that across either Q3 or Q4 so ($v_{res} = 2v_{in}$):

$$\frac{R_{neg}}{R_{negss}} = \frac{\frac{-2}{g_m}}{\frac{-2}{g_{mss}}} = \left[1 + \frac{v_{res}}{2V_T} + \frac{1}{2} \cdot \frac{v_{res}^2}{4V_T^4} + \dots \right]^{-1} \quad (163)$$

Therefore, as a voltage of about $2V_T$ is applied to the resonator its effectiveness will degrade. Since at the image frequency the input will appear almost entirely across the resonator, this means that the filter can tolerate about -16dBm at the input (assuming 50Ω) or about 30dBmV before starting to suffer serious reduction in image rejection.

Note depending on the particular standard that a radio is being designed for, the image filter may have to handle larger signals than what is indicated by (163). However, if resistors were added to the circuit to degenerate the transistors Q3 and Q4 of Fig. 49 then signal size could be increased and the linearity would improve.

6.3.6 Noise Added Due to the Filter

As has already been discussed, there are three major sources of noise in an LNA, base shot noise, collector shot noise, and base resistance of Q1 in Fig. 49. In the filter there is the additional noise due to the active circuitry in the emitter.

Noise due to the base resistance of Q1 is in series with the input voltage, so it sees the full amplifier gain. The output noise due to base resistance is given by:

$$v_{no,r_b} \approx \sqrt{4kTr_b} \cdot \frac{R_1}{Z_{L_E}} \quad (164)$$

Collector shot noise is in parallel to collector signal current, and is directly sent to the output load resistor.

$$v_{no,I_C} \approx \sqrt{2qI_C R_1} \quad (165)$$

Base shot noise can be converted to input voltage by considering the impedance Z_{eq} it sees. If $Z_{eq} = (R_S + \text{matching} + r_{bl}) || Z_\pi$ then:

$$v_{no,I_B} \approx \sqrt{\frac{2qI_C}{\beta_o} Z_{eq}} \cdot \frac{R_1}{Z_{L_E}} \quad (166)$$

If we assume that the noise produced by the resonator is dominated by the collector shot noise in the case of the $-G_m$ style resonator, then the output noise current is given by (see Fig. 49):

$$I_{out,notch} \approx \sqrt{\left(\sqrt{2q \frac{I_{sharp}}{2}} \right)^2 + \left(\sqrt{2q \frac{I_{sharp}}{2}} \right)^2} = \sqrt{2qI_{sharp}} \quad (167)$$

This noise current is passed through the transformer and is injected into the emitter and is then passed on up into the collector. Thus:

$$v_{no,I_{sharp}} \approx \sqrt{2qI_{sharp}} \cdot \frac{R_1}{N_L} \quad (168)$$

Therefore the noise present at the output relative to the noise that would have been present without the notch is:

$$\Psi \approx \frac{2qI_{sharp} \cdot \left(\frac{R_1}{N} \right)^2 + \frac{2qI_{C7}}{\beta_o} Z_{eq}^2 \cdot \left(\frac{R_1}{Z_{L_E}} \right)^2 + 2qI_{C7} R_1^2 + 4kTr_b \cdot \left(\frac{R_1}{Z_{L_E}} \right)^2}{\frac{2qI_{C7}}{\beta_o} Z_{eq}^2 \cdot \left(\frac{R_1}{Z_{L_E}} \right)^2 + 2qI_{C7} R_1^2 + 4kTr_b \cdot \left(\frac{R_1}{Z_{L_E}} \right)^2} \quad (169)$$

This is the same as for an LNA except with an additional term due to I_{sharp} , thus the LNA built with the filter can never be as quiet as a true LNA.

6.4 Automatic Q Tuning for the Notch Filter

The notch filters discussed here and in the references cannot be considered much more than a curiosity unless they can be tuned automatically on-chip. The current through the resonator must be set precisely so that the losses are perfectly cancelled to get a deep notch. Too much or too little and the image rejection will suffer. On previous

experiments the notch was tuned manually by adjusting the current flowing through the resonator.

As a starting point, consider a VCO with no loading as shown in Fig. 53. The VCO will form the basis of the Q tuning circuit for the filter. A simple current mirror sets the current through the VCO with a resistor as the reference. If the resonator current is set above that necessary for perfect cancellation of the losses, the circuit will oscillate.

Fig. 53. A resonator without damping which oscillates if there is enough current.

Now consider the circuit of Fig. 53 modified to include two sensing transistors $Q3$ and $Q4$ as shown in Fig. 54. They are biased at a very low quiescent point so that they are operating almost in class B mode. Note that this is essentially the same circuit as the analog AGC for the VCO previously discussed. The only difference is that here the transistors are biased so that they turn on as soon as there is any swing rather than waiting until it reaches some fraction of a V_{BE} . Thus, it is tuned perfectly to the point where the circuit will have just enough current to cancel its own losses, but no more.

Now the reference is also used to control the current flowing to the filter itself, as shown in Fig. 55. If the components used in building the oscillator are the same as those used in the filter, then the point at which the oscillator is perfectly tuned will also be the perfect

Q tuning point for the filter and the filter now has an automatic Q tuning mechanism. However, if the VCO and the filter have exactly the same frequency, then the VCO will inject noise at the image frequency. Thus, some small offset must be made to the VCO operating frequency. This can be done by adding a small capacitor (a few percent of the total resonator capacitance) to the VCO resonator.

Fig. 54. A resonator with feedback to control the current.

Fig. 55. The oscillator as a master to the filter slave.

6.5 Conclusions

In this chapter, the problem of image rejection in superheterodyne receivers has been reviewed. Traditional methods for dealing with this problem as well as more novel on-chip notch filter solutions were presented. The notch filter presented in this work is integrated with an LNA topology, which gives it a distinct circuit topology to previous work. The operation of this circuit was discussed in detail. A method for automatically tuning notch filters has been proposed here.

Chapter 7: Experiments

This chapter contains a collection of experimental results based on the theory developed in the previous chapters. The first few experiments consisted of components of the receiver, which are used to demonstrate the concepts developed in the previous chapters. The final experiment is a completely integrated receiver front-end.

7.1 A 1.8V 5GHz VCO with Transformer Coupled Feedback

This experiment consisted of a completely integrated VCO with transformer coupled feedback. As discussed in chapter 5, a 2:1 circular transformer was used to increase the voltage swing of the VCO. Resistive emitter degeneration was used to increase the amplitude swing and diode clamps were used to prevent amplitude fluctuations. The VCO core drew 2.78mA from a 1.8V supply, and operated between 5GHz and 5.6GHz. The phase noise was measured to be -116dBc/Hz at a 1MHz offset.

7.1.1 Transformer Design

This design demonstrated the use of on-chip transformers in silicon as a technique for low voltage operation. A circular symmetric transformer with a turns ratio of 2:1, shown in Fig. 56, was used for this design. As discussed in Chapter 4, this structure is optimal for differential applications because both primary and secondary have a point of symmetry at which a bias can be applied without affecting RF performance [40]. Note also that a circular structure will provide the lowest loss, design rules permitting. The actual dimensions of the structure were optimized with the help of the simulator ASITIC [17].

Fig. 56. Drawing of a circular 2:1 transformer.

The structure was measured as a two port with one terminal on the primary side and one terminal on the secondary side grounded. The Z parameters were extracted from the measured S parameters and used to find the equivalent primary inductance L_p and equivalent primary loss R_p . This involved using the narrow band model for the transformer shown in Fig. 24 and repeated in Fig. 57 and knowing that:

$$Z_{11} = R_p + j\omega L_p \quad (170)$$

Similarly:

$$Z_{22} = R_s + j\omega L_s \quad (171)$$

Fig. 57. Narrow band model used to characterize transformers.

Thus, the inductance of the primary and secondary and the primary and secondary single ended Q can be determined as shown in Table III.

Table III: Inductance and Q for the Coils of a Transformer

$L_s = \frac{\text{Im}(Z_{22})}{j\omega}$ (172)	$L_p = \frac{\text{Im}(Z_{11})}{j\omega}$ (173)
$Q_s = \frac{\text{Im}(Z_{22})}{\text{Re}(Z_{22})}$ (174)	$Q_p = \frac{\text{Im}(Z_{11})}{\text{Re}(Z_{11})}$ (175)

The mutual inductance can also be extracted:

$$M = \frac{Z_{12}}{j\omega} = \frac{Z_{21}}{j\omega} \quad (176)$$

Additionally, the measured data can be used to fit a broadband model as described in section 4.5 such as the one shown in Fig. 58, a variation on Fig. 23. It is modeled as two inductors, but with the addition of the coupling coefficient k between them, and interwinding capacitance C_{IW} from input to output. In addition, the inductors are broken in two so that the center tap for biasing both the primary and secondary can be included. Normally, test structures are measured as 2-port structures with the other two ports grounded. Thus, the primary and secondary would each have one terminal grounded, and if the device is assumed to be symmetric, this is sufficient to extract the transformer model. The values for the model are given in Table IV.

Fig. 58. Simplified model for the transformer.

Table IV: Values for the transformer model built

Model Parameter	Value
R_{sp}	1.15Ω
L_p	$1.22nH$
L_s	$0.53nH$
R_{ss}	0.872Ω
Cox/sub (primary)	$77.5fF$
Cox/sub (secondary)	$51.5fF$
R_{sub} (primary)	61.2Ω
R_{sub} (secondary)	16.68Ω
C_{TW}	$1.8fF$
k	0.513

7.1.2 VCO Circuit Design

The basic VCO design is a cross-coupled $-G_m$ topology as described in section 5.6 and shown in Fig. 36 and repeated here as Fig. 59. In this design the feedback is provided by a transformer rather than either directly coupling the bases to the collectors or by using capacitors in the feedback path as discussed in detail in Chapter 5 section 5.6. Buffers were included in the circuit so that the VCO would have a low output impedance to drive other circuits or test equipment without loading the tank and decreasing its Q .

The transformer used in the VCO was characterized as a test structure in a previous run of the process in order to create a model to use in the VCO design. The k factor for the transformer was 0.54 at 5GHz. Fig. 61 shows the inductance and Q for the primary and secondary windings. As can be seen from the plot, the Q of the primary is about 10 at the frequency of interest, and the Q of the secondary is about 8. The inductance of the primary and secondary are about 1.7nH and 0.7nH at 5.5GHz. Thus, the structure has been optimized for best performance over the frequency band of interest.

Fig. 61. Inductance and Q for the coils of the transformer.

Fig. 62. Tuning curve of the VCO.

The VCO itself was characterized as well. It operated from a nominal power supply of 1.8V and the VCO core drew a current of 2.78mA. Buffers that drew an additional 3.4mA were added to the circuit to drive the test equipment. The circuit had a 600MHz tuning range or about 12% and the tuning curve is shown in Fig. 62.

The VCO was simulated with a simple ac noise simulation to find the major sources of noise over the course of a complete oscillation cycle as the biases on the transistors changed and therefore determine the “noise figure” that should be used when characterizing it as described by equation (102). In Fig. 63 a plot of the noise produced by the tank loss and the noise produced by other major noise sources is shown. Note that only the transistor noise sources for Q1 have been plotted, and the noise due to Q2 would be the mirror image of the ones for Q1. As discussed, during the zero crossings, the noise due to the resistor R_{E1} in the tail is suppressed by the symmetry of the circuit, but becomes more important as the voltage swing grows towards the peak. From inspection of the graph it can be seen that the noise figure in this case should be approximately 3dB as the tank losses and other noise sources are almost equal. Inserting this information back into equation (112) and assuming that the limiters in this design remove all low frequency noise, gives a phase noise prediction of -117.1dBc/Hz at 1MHz offset. The

phase noise of the circuit was also measured as shown in Fig. 64 and was -115.8dBc/Hz at a 1MHz offset. This is extremely close to the value predicted using simple theory. The difference is most likely due to some low frequency noise, which has not been completely eliminated, affecting the varactor.

Fig. 63. Noise simulation of the VCO showing noise over a cycle.

Fig. 64. Plot showing the VCO phase noise at 1MHz offset.

Thus, in this section a completely integrated VCO with transformer coupled feedback has been presented. The circuit has a phase noise of -116 dBc/Hz at 1 MHz offset, consumes 4.9 mW from a 1.8 V supply and has a tuning ratio of about 12%. This circuit was also used to test the phase noise theory developed earlier in Chapter 5.

7.2 A Completely Integrated 1.8 Volt 5 GHz Tunable Image Reject Notch Filter

This experiment demonstrates the operation of the integrated image-reject notch filter as discussed in Chapter 6. The filter circuitry is combined with a standard LNA topology, thereby minimizing the additional current required to perform this function on-chip. This prototype circuit exhibited the following performance: 70 dB of image rejection, a NF of 4.2 dB, 14 dB of gain in the pass band, and an IIP3 of -6 dBm.

7.2.1 Circuit Design

As discussed in Chapter 6, the circuit shown in Fig. 65 provides notching action in a conventional LNA topology.

Fig. 65. LNA circuit with resonator placed in the emitter to provide a high impedance at the undesired image frequency.

Here, the Colpitts form of feedback is implemented to provide negative resistance around two series capacitors (C_{f1} and C_{f2_var}) as shown in Fig. 65. Capacitor C_{f2_var} is implemented using a varactor to make the filter tunable. Due to process variations, the current I_{sharp} will need to be tuned as well to ensure perfect cancellation of the losses in the resonator.

In the design of the circuit, two inductors (L_b , L_e) are used to provide simultaneous noise and power matching of the circuit in the pass band. The procedure for doing this is described in detail in Chapter 2. The tank formed by L_T and C_T is tuned to the pass band frequency and will provide some additional image rejection for the filter.

For the purposes of measurement, an output buffer was added to drive the measurement equipment in the test circuit. Emitter follower Q4 formed the buffer. In an actual application where the filter would drive a mixer on the same chip, the buffer would be removed.

7.2.2 Experimental results

The test circuit was fabricated in a state of the art SiGe technology with 50 GHz f_t . All components, including the input inductor, were fabricated on-chip. Care was taken in the layout of the circuit to ensure that signal tracks were kept as short as possible. Thick metal traces were used to provide a low inductance path to ground. The inductors were simulated and designed using ASITIC. As well, many tiedowns were used in an attempt to isolate the inductors from the rest of the circuit. A photomicrograph of the circuit is shown in Fig. 66. The chip measured approximately 0.6 mm by 0.5 mm, including pads.

The circuit was measured by wafer probing only. Using a network analyzer, the pass band gain was found to be 14 dB and the filter provided almost 56 dB of attenuation at the image frequency. Thus, the filter provides almost 70 dB of image rejection. A plot of the filter response taken from the network analyzer is shown in Fig. 67. Overlaid on the same figure, is a plot of the simulated response of the circuit with and without the notch circuitry for comparison. One can also see from this plot that if the notch is removed the circuit would have a gain of about 3dB at the image frequency.

Fig. 66. Photomicrograph of the notch filter.

The pass band was centered at 4.6 GHz and the notch can be varied from a frequency of about 6.3 to 6.8 GHz. The plot of the notch frequency tuning characteristic is shown in Fig. 68. It can be seen from this plot that the tuning characteristic is quite linear. This is due to the excellent high-Q varactors available in this process. The varactors employ a graded doping profile, which gives them a linear C-V curve. The result is a very linear tuning curve for the filter as well.

Fig. 67. Plot of the filter response showing 70dB of image rejection.

The notch was tuned by adjusting I_{sharp} to cancel all the losses in the circuit. It was found that in this case, a current of approximately 4mA was required to tune out the loss in the tank. This current varied slightly across the tuning range of the filter. Nevertheless, with proper adjustment the image rejection was maintained across the entire tuning range.

Fig. 68. Plot of the filter notch frequency response.

The input matching was done using on-chip inductors and was therefore poor compared to schemes using high-quality off-chip passive components. However, an S_{11} of -7.5 dB was achieved, showing that very little gain is lost in the circuit due to input mismatch.

The IIP3 was measured using a spectrum analyzer and applying two tones to the input in the pass band. It was found to be -6 dBm for this circuit. A higher value could be achieved if more degeneration or current were used.

The noise figure was measured to be 4.2 dB. The presence of the notch reduces the pass band gain of this circuit as can be seen in Fig. 67, which directly impacts the noise figure. Simulation showed the notch circuitry added about 1.5 dB to the noise figure compared to what could otherwise be achieved if the resonator was removed. Table V summarizes the measurements for this circuit.

Table V: Summary of Filter Performance

Parameter	Performance
S_{11} (series matching inductor on-chip)	-7.5 dB
Current through Q1 (LNA)	6 mA
Current through Q3 (resonator)	4 mA
Supply Voltage	1.8 Volts
IIP3	-6 dBm
Gain (4.6 GHz)	14 dB
Image Rejection	70 dB
Notch Tuning Range	6.3-6.8 GHz
Noise Figure	4.2 dB

Thus, in this section a 5 GHz completely integrated notch filter has been realized in a SiGe process with 50 GHz f_t . The filter uses no off-chip components and is suitable for wireless applications for which a high degree of integration is desirable. The filter provides good gain, an excellent image rejection of almost 70 dB and is tunable over a 500 MHz bandwidth. Since the filter is implemented as part of the LNA, little additional circuitry is required. This experiment verifies the general theory presented in Chapter 6 showing that a notch filter can be implemented using one of the basic topologies shown in this chapter.

7.3 An Image Filter Using On-Chip Transformer

In addition to the first experiment on image filters a second filter was also built. This one used a transformer, rather than a capacitor to couple the filter into the LNA as discussed in Chapter 6. As well, this filter used a common emitter LNA rather than the cascode configuration. This prototype circuit exhibited the following performance: 46 dB of image rejection, a NF of 5 dB, 8 dB of gain in the pass band, and an IIP3 of 2 dBm.

7.3.1 Circuit Design

The circuit shown in Fig. 69 provides notching action and is an alternative to the design presented earlier in this chapter. The main differences between this circuit and the previous one are that instead of a capacitor, a transformer was used to couple the resonator into the LNA, and the cascode was removed to explore the possibility of going to lower voltages in later experiments.

A transformer with a turns ratio greater than unity can have many advantages for the design of the notch filter. In Chapter 6 it was shown that:

- 1) A turns ratio greater than unity will increase the stability margin of equation (159).
- 2) It will increase the input power required to saturate the resonator as discussed in Section 6.3.5.
- 3) It will reduce the noise contribution from the notch resonator as discussed in Section 6.3.6.

Once more, for the purposes of measurement, an output buffer was added to drive the measurement equipment in the test circuit. Emitter follower Q4 formed the buffer. In an actual application in which the filter would drive a mixer on the same chip, the buffer would be removed.

Fig. 69. Image reject filter with transformer coupled resonator.

7.3.2 Experimental results

The test circuit was fabricated in a state of the art SiGe technology with 50 GHz f_t . All components were fabricated on-chip. Care was taken in the layout of the circuit to ensure that signal tracks were kept as short as possible. A photomicrograph of the circuit is shown in Fig. 70. The chip measured approximately 0.6 mm by 0.5 mm including pads.

The circuit was measured by wafer probing only. Using a network analyzer, the pass band gain was found to be 8 dB, and the filter provided almost 38 dB of attenuation at the image frequency. Thus, the filter provides almost 46 dB of image rejection. The removal of the cascode allowed more feed through of signal due to decreased isolation. As well, the addition of the transformer led to increased degeneration. This, coupled with the Miller effect reduced the gain of this design with respect to the previous one. Thus, overall, less image rejection was achieved. A plot of the filter response taken from the network analyzer is shown in Fig. 71.

Fig. 70. Photomicrograph of the notch filter with on-chip transformer.

Fig. 71. Plot of the filter response showing 56dB of image rejection.

The removal of the cascode transistor and the addition of the transformer allowed the probe to provide the correct amount of inductance for an almost perfect input match in this case. A plot of S_{11} is shown in Fig. 72.

Fig. 72. Plot of the filter response showing 56dB of image rejection.

Since the gain of this design was greatly reduced, the noise figure of this design suffered and, even with the removal of the on-chip inductor in the base, was 5 dB. The linearity was of course helped by the additional degeneration and the IIP3 was measured as 2 dBm. The current in this case was 4 mA for the LNA and 4.5 mA for the resonator when the notch was perfectly tuned. The circuit operated from a 1.8 V supply.

The notch in this circuit was tunable just as in the first experiment. A plot of notch frequency versus tuning voltage is shown in Fig. 73. As well, the notch linearity was studied for this circuit. A signal was applied at the notch frequency and the amount of image reject with increasing signal power was recorded. The results are shown in Fig. 74. From this plot it can be seen that the filter can tolerate an input power of about 37 dBmV at the image frequency before the circuit starts to lose image rejection. Driving into a perfect open circuit this would correspond to a voltage of about 141 mV rms at the input. This would also be developed across the transformer primary. At the secondary

this would be about 45 mV rms (the transformer has an inductance ratio of about 1.7:0.7 and a $k = 0.54$). This would correspond to about 22.5 mV rms across the transistor or about 33 mV (the capacitor ratio of C_1 and C_{var} is about 1:1) peak, which is pretty close to a V_T which is what we expect from the results in Section 6.3.5. The results of this experiment are summarized in the following table. Note also in this figure that the image rejection peaks before degrading. This is most likely due to the notch current being tuned slightly beyond the optimum at low signal levels, then passing through the perfect point before degrading as the negative resistance starts to decrease.

Table VI: Summary of Filter Performance

Parameter	Performance
S_{11}	-21 dB
Current through Q1 (LNA)	4 mA
Current through Q3 (resonator)	4.5 mA
Supply Voltage	1.8 Volts
IIP3	2 dBm
Gain (4.6 GHz)	8 dB
Image Rejection	46 dB
Notch Tuning Range	5.7-5.9 GHz
Noise Figure	5 dB

Fig. 73. Plot of the filter frequency response.

Fig. 74. Plot of image rejection versus signal power.

In summary, a 5 GHz completely integrated notch filter has been realized in a SiGe process with 50 GHz f_t . The filter uses no off-chip components and is suitable for wireless applications for which a high degree of integration is desirable. The filter

provides a gain of 8 dB, an image rejection of almost 56 dB and is tunable over a 400 MHz bandwidth. Since the filter is implemented as part of the LNA, little additional circuitry is required.

7.4 A Study of Digital and Analog Automatic-Amplitude Control Circuitry for Voltage-Controlled Oscillators

This experiment presents both analog and digital automatic-amplitude control techniques for voltage-controlled oscillators as discussed in the VCO chapter. These feedback mechanisms help to keep the VCOs at an optimum level for best phase noise performance over temperature, process and voltage variations and these experiments were used to validate the theory presented in the VCO chapter. The VCOs were fabricated in a 50GHz SiGe BiCMOS process. They use MOS varactors and achieve a 600MHz tuning range in the 2GHz band. The phase noise of the VCO with analog control was measured to be -99 dBc/Hz at a 100 kHz offset from the carrier. The digital loop allows for a more optimised VCO core that achieves a phase noise of -108.5 dBc/Hz at a 100 kHz offset in a low gain mode. The VCOs draw between 4 mA and 8 mA from a 3.3 volt supply.

The equations developed in section 5.7 can be used to design the analog loop and demonstrate the stability of this circuit. The capacitor C_2 is placed in the circuit to create a dominant and controllable pole and to clean up noise from the bias. However, its frequency cannot be too close to the frequency of the other pole in the VCO, or a design with little phase margin will result. This could lead to instability, especially if there is uncertainty as to the Q of the VCO or additional phase shift from other components. Generally the pole frequency and gain of $A_2(s)$ in the oscillator are not adjustable because these values are set through the design of the oscillator and are chosen to give the VCO best possible performance. Thus the designer is left with the possibility of adjusting the pole frequency and gain of $A_1(s)$ and $A_3(s)$. The pole frequency of $A_1(s)$ can be set to any value the designer likes, provided that the capacitor can be made large enough conveniently. This frequency is usually set lower than the frequency of P_2 because making the frequency too high can result in other less controllable poles determining system stability. If the designer still does not feel that the design is stable enough, the

loop gain can be adjusted by either changing the gain in $A_1(s)$ (by adjusting the ratio of the current mirror) or by adjusting the gain of $A_3(s)$ (this can be done by changing the size of the limiting transistors Q3 and Q4). Reducing the gain of the loop is a less desirable alternative than adjusting P_1 because, as the loop gain is reduced its ability to settle to an exact final value is reduced. The digital loop does not involve these trade-offs as it is simply a one pole system.

In the digital feedback loop six bits was chosen in the VCO core to provide good resolution over this span. More bits could easily be added if needed although it would get harder to guarantee a monotonic curve. Each count and its corresponding resistance for this design are shown in Fig. 75.

Fig. 75. Total degeneration resistance related to a binary word applied to the degeneration switches.

For the design using the digital loop, a peak detector was designed as shown in Fig. 76 and used to detect the amplitude of the VCO output signal. It was designed to draw minimal current and C_{peak} was sized to minimise the ripple on the output voltage while still allowing a fast response. Since the tank DC level is one V_{BE} less than V_{cc} , and the desired swing is $2V_{\text{BE}}$, the peak voltage on one side of the tank is V_{cc} when the VCO is operating at the proper level. Thus the desired output from the peak detector is $V_{\text{cc}} - 2V_{\text{BE}}$. Two references are generated which are compared to the peak detector output. The reference level generator produces two voltages separated by an offset V_{Hi} and V_{Low} .

The offset compensates for the fact that the VCO amplitude cannot be set with infinite precision using only six bits.

Fig. 76. Diagram of the peak detector and the reference generator.

7.4.1 Experimental Results

A prototype of the analog controlled VCO was fabricated on a test chip along with many other circuit building blocks. The digitally-controlled VCO was fabricated in a subsequent run in the process and was embedded in a completely integrated cable tuner. Both circuits were packaged in a TQFP forty pin package for evaluation and were mounted on test boards. A photomicrograph of each VCO is shown in Fig. 66. They use differential octagonal spiral inductors with patterned ground shields. The inductors were designed with the help of ASITIC[17] and have a measured differential Q of about 15 at 2.4 GHz. The chip area used by the analog VCO core and associated circuitry was approximately 1.2 mm X 0.8 mm. The digital VCO circuitry consumed an area measuring about 1.0 mm X 0.6 mm.

A) Analog AAC VCO Design

B) Digital AAC VCO Design

Fig. 77. Photomicrographs of the VCOs.

The VCO outputs were buffered so they could drive various circuits and test equipment. Generally, any circuits to which the VCOs were connected were optimized to reduce any loading on the tank. Measurements reported here are on the raw performance of VCOs, however they have also been demonstrated in a synthesizer. In the case of the digitally controlled VCO, the loop bandwidth of the synthesizer was adjusted to be very narrow for VCO characterization. The circuits ran from a 3.3 V supply, drew 4 mA in the case of the analog loop (designed for a swing of 0.9V) and 8 mA of current in the case of the digitally controlled loop (designed for a swing of 1.8 V). The output power of the VCO varied slightly across the operating band, however this was due to the frequency response of certain elements in the signal path on the board. The tuning characteristic of both VCOs versus control voltage is shown in Fig. 78. Note that most of the tuning range is achieved between 2 V and 3.3 V. This is due to the tuning characteristic of the varactors in this process. In some processes the varactor tuning curves can be centered around a voltage other than zero volts which would be beneficial, as it would center the tuning curve closer to the mid point between ground and V_{CC} . However, these varactors do produce a very nice linear curve, which is good for the synthesizer design. The K_{VCO} as measured from this graph is about 500 MHz/Volt. The use of digitally controlled banks

of varactors in the case of the digital VCO allowed the K_{VCO} to be reduced in this design while maintaining about the same tuning range. In this case, the low tuning band had a K_{VCO} of 180 MHz/Volt, the mid-band had a K_{VCO} of 200 MHz/volt and the high-band had a K_{VCO} of 250 MHz/volt.

Fig. 78. Plot of the VCO frequency vs. tuning voltage.

The phase noise of the analog controlled circuit was measured with a phase noise measurement system using a discriminator method as well as with a spectrum analyzer. Both methods gave consistent results. Multiple samples of each version of the circuit were measured at different points in the tuning range. The phase noise was found to vary by no more than a couple of dB for all samples tested. The best performance was achieved with the digitally controlled VCO without limiters in the low gain mode. A plot of its phase noise showing a performance of -108.5 dBc/Hz is shown in Fig. 79. Tables 1 through 3 show the phase noise performance of the three designs at various carrier frequencies. Note that the analog controlled loop has the worst performance due to its reduced amplitude. It measures between -97 dBc/Hz and -99 dBc/Hz. The digitally controlled loop without limiters gives the best number of -108.5 dBc/Hz, but the phase noise becomes worse at higher frequencies and is -96 dBc/Hz right at the top. The

digital loop with limiters gives the best overall results with a constant -104 dBc/Hz, except in the very high gain region. This demonstrates the importance of suppressing amplitude fluctuations in VCOs with high gain and shows that the amplitude fluctuations have become the dominant noise mechanism.

Table VII: Phase noise for the analog controlled VCO.

Frequency (GHz)	K_{VCO} (MHz/V)	Phase Noise @100kHz offset (dBc/Hz)
2.0	0	-99
2.2	500	-97
2.4	500	-97

Table VIII: Phase noise for the digitally controlled VCO with no limiters. (HL1 and HL2 are band select control voltages as shown in Fig. 39.)

Frequency (GHz)	K_{VCO} (MHz/V)	HL1 (V)	HL2 (V)	Phase Noise @100kHz offset (dBc/Hz)
1.736	0	0	0	-108.5
1.935	180	0	0	-102
1.935	0	3.3	0	-100
2.088	200	3.3	0	-99
1.998	0	3.3	3.3	-100.5
2.088	0	3.3	3.3	-100
2.188	250	3.3	3.3	-98
2.238	250	3.3	3.3	-96

Table IX: Phase noise for the digitally controlled VCO with limiters.

Frequency (GHz)	K_{VCO} (MHz/V)	HL1	HL2	Phase Noise @100kHz offset (dBc/Hz)
1.716	0	0	0	-104.5
1.945	180	0	0	-104
1.945	0	3.3	0	-104
2.04	200	3.3	0	-104
1.988	0	3.3	3.3	-104
2.24	250	3.3	3.3	-100

The phase noise was also measured over a -50°C to 100°C temperature range. The phase noise was found to be almost constant over this range, changing by only a couple of dB. This residual variation is due to changes in the V_{BE} with temperature. The result of this measurement is shown in Fig. 80. Observations of the counter in the digital loop confirmed that it was adapting the current for these changes in temperature.

Fig. 79. VCO spectrum showing best phase noise results.

Fig. 80. Plot of the VCO power and phase noise at 100 kHz offset vs. temperature.

Thus, this section has presented VCOs with both analog and digital automatic-amplitude control loops. A best phase noise of -108.5 dBc/Hz at 100 kHz offset was achieved with

the digital loop in a low gain mode. The VCOs had a very wide tuning range and using banks of varactors was found to reduce the K_{VCO} without affecting overall tuning range. The phase noise was almost constant over a temperature range of -50°C to 100°C . The design of the feedback automatic-amplitude control circuitry that helps to achieve this performance has been demonstrated to illustrate the concepts presented in section 5.7. A loop similar to the one studied here will be used in the complete receiver circuit discussed next.

7.5 A 5GHz Completely Integrated RF Front-End with On-Chip Image Filter with Automatic Q-Tuning and On-Chip VCO

This experiment presents a notch filter with Q tuning combined with a mixer and VCO to form a completely integrated receiver front-end. The receiver schematic is shown in Fig. 81. This receiver uses a VCO just like the one described in section 7.2. The filter in the receiver, however uses a $-G_m$ style resonator unlike the previous designs and has an automatic Q tuning circuit with master VCO. The design of this Q tuning circuit as well as a similar experiment have already been discussed. The LNA is transformer-coupled into the mixer as described in Chapter 3. The mixer develops an output across a resistive load and output buffers (not shown) are used to drive the measurement equipment. Note also that the presence of the master and the LO means that there are two VCOs operating on this chip, however their frequencies are widely spaced so VCO pulling is not an issue here.

Fig. 81. Schematic of the entire receiver front-end.

7.5.1 Experimental Results

The filter was first tested by itself. In this preliminary experiment the VCO and mixer were not present and the filter output was simply buffered with a follower in order to characterize the filter response with the network analyzer. Unfortunately, due to a layout error, the frequency of the notch was higher than anticipated, however the circuit still showed very good attenuation in the stop band of between 36 and 44 dB. In this case, unlike the previous circuits, no manual adjustment of the current was required to maintain the image rejection across the band. A plot of the filter response is shown in Fig. 83.

The notch was tunable between 9.9 GHz and 10.7 GHz and is plotted in Fig. 84. A photomicrograph of the test circuit is shown in Fig. 82.

Fig. 82. Photomicrograph of the 5 GHz filter test circuit.

Fig. 83. Plot of the filter response.

The filter test circuit was submitted to microsurgery in an attempt to adjust the notch frequency to a much more reasonable value. A micro capacitor was added to the circuit using the technique described in [51] to reduce the frequency. A plot of the adjusted filter response is shown in Fig. 85. This resulted in the notch having a more reasonable frequency of between 8.2-8.6 GHz. However, since the master and slave were no longer matched the Q tuning circuit no longer functioned.

A plot showing the voltage that can be tolerated by the filter before it starts to lose image rejection is shown in Fig. 86. From this figure it can be seen that, for a voltage larger than about 35 dBmV image rejection degrades. This corresponds to an rms voltage of about 112 mV. The transformer reduces this value down to about 72 mV through a turns ratio and with a $k = 0.54$ this is down to 36 mV. Therefore, each transistor sees about 18 mV rms or about 25 mV peak. This agrees with the discussion of linearity in section 6.3.5.

Fig. 84. Plot of notch frequency versus tuning voltage before microsurgery.

Fig. 85. Plot of the filter response after microsurgery.

Fig. 86. Plot of image rejection versus signal power.

The entire receiver was fabricated in a 75 GHz SiGe process. The chip measured 1.2 mm by 1.8 mm and a die photo is shown in Fig. 87. The chip drew 21.6 mA from a 1.8V supply excluding IF buffers. The RF passband was centered at 5.1 GHz and the front-end had a gain of 19.8 dB. Thus, with a minimum attenuation of 36 dB in the stop band, this provided the receiver with a minimum image rejection of 56 dB. This value can be compared to a value calculated with the aid of equation (154), which gives a rough estimate of 57 dB for best case image rejection. Thus, one can see that this formula is slightly pessimistic, but it also shows that we are close to the best image rejection we can expect from this circuit given the parasitic feed through of signals. Unfortunately, the VCO frequency and notch frequency were both in error, so the frequency plan of the receiver was incorrect, yet the circuit still demonstrated the principles. The intended RF frequency was 5.1 GHz, the LO frequency was intended to be 6.1 GHz and notch frequency was intended to be 7.1 GHz for an IF frequency of 1 GHz. Port to port isolation was also measured and is summarized with the rest of the receiver performance in the following table.

Fig. 87. Photomicrograph of the 5GHz receiver.

Table X: Summary of Receiver Performance

Parameter	Performance
Supply Voltage	1.8 V
Current	21.6 mA
Image Rejection	> 56 dB
Conversion Gain	19.8 dB
IIP3	-11.5 dBm
RF Frequency	5.1 GHz
VCO Tuning Range	5.1-5.6 GHz
Notch Tuning Range	10-10.8 GHz
Notch Tuning Range after Microsurgery	8.2-8.6 GHz
LO-RF Isolation	>60 dB
LO-IF Isolation	> 50 dB
RF-IF Isolation	> 50 dB
Noise Figure @ 350 MHz IF frequency	4.5 dB

Therefore, a completely integrated receiver front-end has been realized in a 75 GHz SiGe technology. The receiver features an on-chip notch filter with automatic Q-tuning circuit and low voltage VCO. The Q tuning circuit allows the filter to provide good image rejection, without the requirement for manual current adjustment and a deep notch was observed across the tuning band.

7.6 Conclusions

This chapter has presented a number of experiments to support and demonstrate the theory described in the rest of this thesis. The first experiment was a completely integrated VCO with transformer-coupled feedback. This circuit was also used to test the phase noise theory developed earlier in Chapter 5. The second experiment was a 5 GHz completely integrated notch filter. The filter used no off-chip components and is suitable for wireless applications for which a high degree of integration is desirable. This experiment verified the general theory presented in Chapter 6 showing that a notch filter can be implemented using one of the basic topologies shown in this chapter. The third experiment presented VCOs with both analog and digital automatic-amplitude control loops. The VCOs had a very wide tuning range and, using banks of varactors was found to reduce the K_{VCO} without affecting overall tuning range. The design of the feedback circuitry that helps to achieve this performance has been demonstrated to illustrate the concepts of automatic amplitude control presented in Section 5.7. Finally, a completely integrated receiver front-end has been realized. The receiver features an on-chip notch filter with automatic Q-tuning circuit and low-voltage VCO. The Q-tuning circuit allows the filter to provide good image rejection, without the requirement for manual current adjustment and a deep notch was observed across the tuning band. This demonstrates the concepts of automatic Q tuning presented in Chapter 6.

Chapter 8: Conclusions and Summary

In this thesis the receiver was a vehicle for developing a better understanding of many aspects of high frequency RF circuit performance. The research has been aimed at developing techniques for lowering the supply voltage of RF circuits, raising the integration level of receivers, and increasing the degree of robust performance of circuits through the use of feedback. While attempting to achieve these goals insight into the design of many of these circuits has been gained as well.

Aspects of VCO phase noise have been studied in detail including the noise factor term in Leeson's equation and the effects of nonlinearity of transistors on phase noise. This analysis led to a better understanding of the noise sources in the oscillator that are important contributors to phase noise, and an improved understanding of how these noise sources cause phase noise.

Methods for VCO automatic amplitude control have also been studied and a new digital method has been proposed and demonstrated in a test circuit. These methods of amplitude control form a feedback loop. The operation of this loop has been analyzed in detail so that issues with the loop, such as stability can be properly understood. A significant outcome is the understanding of the role of the loop poles in avoiding instability. Further, the understanding of these loops provided the necessary building blocks to create the Q-tuning circuit for the notch filter.

VCOs were also optimized for low voltage operation. The VCO in the final receiver design used a transformer to provide larger voltage swing at lower voltages. The transformer was designed to have a 2:1 turns ratio to facilitate the operation of the VCO at 1.8V.

A new topology for an on-chip image filter has been developed and implemented. This filter makes use of a modified LNA with a resonator in the emitter of the driver transistor to provide a high impedance at the unwanted image frequency. Aspects of the filter

design have been explored, including linearity and noise constraints. Stability of the filter has also been analyzed to determine when the filter will go unstable and therefore allow the designer to make sure this does not happen.

In addition, a method for automatically Q-tuning the image filter was presented. Since the filter requires precise current adjustment, it would be impossible to set this current accurately in the presence of process tolerance in an integrated circuit. Thus, a VCO master with feedback is used to set the current of the slave/matched filter and therefore allow exact tuning of the filter current.

Finally, the filter and VCO were also integrated with a low voltage mixer that completed the front-end architecture. This mixer made use of a transformer in place of driving transistors so that transistor stacking was minimized.

8.1 Summary of Contributions

The following is a summary of contributions made during the course of this research:

Phase noise in VCOs has been studied in detail. Specifically the effects of varactors on the phase noise of high gain VCOs has been analyzed. Ways to reduce this effect have been presented. The noise figure and excess gain terms in Leeson's formula have been derived from first principals [24][25][57][55].

Both analog and digital automatic amplitude control techniques for VCOs have been presented[54][56][61][55]. Analysis of the stability and relative performance of these two techniques has been presented.

Methods for integrating a high-frequency notch filter have been studied [53][52][55][60]. One particular topology has been developed, analyzed and explored in several implementations.

Integrating notch filters and VCOs with superheterodyne receiver front-ends have been studied [53][58].

Techniques to lower the supply voltage of voltage-controlled oscillators have been studied [59][57][58]. Specifically the tail current source has been replaced

with a resistor to lower headroom requirements. AAC can be performed in this design using the digital AAC loop developed in this work.

A master slave method for automatically Q tuning on-chip filters for high Q has been presented [58][62].

8.2 Future Work

As with any project, there are always many additional experiments that could be run as well as refinements to the design that could be implemented. Here are a few suggestions for future work that could continue from this research:

The filter currently does not have automatic frequency tuning, so this should be added. A simple PLL could be designed to control the frequency of the master VCO and therefore the frequency of the notch filter as well. Alternatively, a PLL could be designed for the LO on the chip and the control voltage from this PLL could be scaled and also applied to the filter, removing the need for an additional PLL on the chip.

Work could be done to design a synthesizer incorporating the VCO. One would of course, be necessary in an actual application.

This work has demonstrated a notch filter, however it may be possible using similar techniques to build a band pass filter. Techniques for building a band pass filter could be explored based on the current filter designs in this work.

It would be possible to build on the theory presented here and perform additional studies on the linearity and signal handling capability of these filters. The resonators could be modified to include degeneration so that they could handle larger signals before entering saturation. This could be studied in detail.

The digital AAC circuit was only demonstrated in a test VCO, and was never explored as an alternative Q-tuning circuit to the analog implementation presented here. In a future

design, the digital AAC loop could replace the analog one and a comparison of the accuracy of each loop could be compared.

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