MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS
STANDARD REFERENCE MATERIAL 1010a
(ANSI and ISO TEST CHART No. 2)

National Library
of Canada

Acquisitions and
Bibliographic Services Branch

395 Wellington Street
Ottawa, Ontario
K1A 0N4

Bibliothèque nationale
du Canada

Direction des acquisitions et
des services bibliographiques

395, rue Wellington
Ottawa (Ontario)
K1A 0N4

Vous liez votre référence

Vous liez votre référence

NOTICE

The quality of this microform is heavily dependent upon the quality of the original thesis submitted for microfilming. Every effort has been made to ensure the highest quality of reproduction possible.

If pages are missing, contact the university which granted the degree.

Some pages may have indistinct print especially if the original pages were typed with a poor typewriter ribbon or if the university sent us an inferior photocopy.

Reproduction in full or in part of this microform is governed by the Canadian Copyright Act, R.S.C. 1970, c. C-30, and subsequent amendments.

AVIS

La qualité de cette microforme dépend grandement de la qualité de la thèse soumise au microfilmage. Nous avons tout fait pour assurer une qualité supérieure de reproduction.

S'il manque des pages, veuillez communiquer avec l'université qui a conféré le grade.

La qualité d'impression de certaines pages peut laisser à désirer, surtout si les pages originales ont été dactylographiées à l'aide d'un ruban usé ou si l'université nous a fait parvenir une photocopie de qualité inférieure.

La reproduction, même partielle, de cette microforme est soumise à la Loi canadienne sur le droit d'auteur, SRC 1970, c. C-30, et ses amendements subséquents.

Canada

PLATINUM SALICIDE PROCESS FOR BiCMOS APPLICATIONS

by
Khalid Sheergar

**A thesis submitted to the
Faculty of Graduate Studies and Research
in partial fulfillment of the requirements for the degree of
Master of Engineering**

**Ottawa-Carleton Institute for Electrical Engineering
Department of Electronics
Faculty of Engineering
Carleton University**

September 1993

© copyright 1993, M. K. Sheergar

National Library
of Canada

Acquisitions and
Bibliographic Services Branch

395 Wellington Street
Ottawa, Ontario
K1A 0N4

Bibliothèque nationale
du Canada

Direction des acquisitions et
des services bibliographiques

395, rue Wellington
Ottawa (Ontario)
K1A 0N4

Your file Votre référence

Our file Notre référence

The author has granted an irrevocable non-exclusive licence allowing the National Library of Canada to reproduce, loan, distribute or sell copies of his/her thesis by any means and in any form or format, making this thesis available to interested persons.

L'auteur a accordé une licence irrévocable et non exclusive permettant à la Bibliothèque nationale du Canada de reproduire, prêter, distribuer ou vendre des copies de sa thèse de quelque manière et sous quelque forme que ce soit pour mettre des exemplaires de cette thèse à la disposition des personnes intéressées.

The author retains ownership of the copyright in his/her thesis. Neither the thesis nor substantial extracts from it may be printed or otherwise reproduced without his/her permission.

L'auteur conserve la propriété du droit d'auteur qui protège sa thèse. Ni la thèse ni des extraits substantiels de celle-ci ne doivent être imprimés ou autrement reproduits sans son autorisation.

ISBN 0-315-89863-1

Canada

Name KHALID SHEERGAR

Dissertation Abstracts International is arranged by broad, general subject categories. Please select the one subject which most nearly describes the content of your dissertation. Enter the corresponding four-digit code in the spaces provided.

0544

U·M·I

SUBJECT TERM

SUBJECT CODE

Subject Categories

THE HUMANITIES AND SOCIAL SCIENCES

COMMUNICATIONS AND THE ARTS

Architecture . . . 0729
Art History . . . 0377
Cinema . . . 0900
Dance . . . 0378
Fine Arts . . . 0357
Information Science . . . 0723
Journalism . . . 0391
Library Science . . . 0399
Mass Communications . . . 0708
Music . . . 0413
Speech Communication . . . 0459
Theater . . . 0465

EDUCATION

General . . . 0515
Administration . . . 0514
Adult and Continuing . . . 0516
Agricultural . . . 0517
Art . . . 0273
Bilingual and Multicultural . . . 0282
Business . . . 0688
Community College . . . 0275
Curriculum and Instruction . . . 0727
Early Childhood . . . 0518
Elementary . . . 0524
Finance . . . 0277
Guidance and Counseling . . . 0519
Health . . . 0680
Higher . . . 0745
History of . . . 0520
Home Economics . . . 0278
Industrial . . . 0521
Language and Literature . . . 0279
Mathematics . . . 0280
Music . . . 0522
Philosophy of . . . 0998
Physical . . . 0523

Psychology . . . 0525
Reading . . . 0535
Religious . . . 0527
Sciences . . . 0714
Secondary . . . 0533
Social Sciences . . . 0534
Sociology of . . . 0340
Special . . . 0529
Teacher Training . . . 0530
Technology . . . 0710
Tests and Measurements . . . 0288
Vocational . . . 0747

LANGUAGE, LITERATURE AND

LINGUISTICS

Language . . . 0679
General . . . 0289
Ancient . . . 0290
Linguistics . . . 0291
Modern . . . 0401
Literature . . . 0294
General . . . 0295
Classical . . . 0297
Comparative . . . 0298
Medieval . . . 0316
Modern . . . 0591
African . . . 0305
American . . . 0352
Asian . . . 0355
Canadian (English) . . . 0593
Canadian (French) . . . 0311
English . . . 0312
Germanic . . . 0315
Latin American . . . 0313
Middle Eastern . . . 0314
Romance . . . 0314
Slavic and East European . . . 0314

PHILOSOPHY, RELIGION AND

THEOLOGY

Philosophy . . . 0422
Religion . . . 0318
General . . . 0321
Biblical Studies . . . 0319
Clergy . . . 0320
History of . . . 0322
Philosophy of . . . 0469
Theology . . . 0323

SOCIAL SCIENCES

American Studies . . . 0323
Anthropology . . . 0324
Archaeology . . . 0326
Cultural . . . 0327
Physical . . . 0310
Business Administration . . . 0272
General . . . 0770
Accounting . . . 0454
Banking . . . 0338
Management . . . 0385
Marketing . . . 0501
Canadian Studies . . . 0503
Economics . . . 0505
General . . . 0508
Agricultural . . . 0509
Commerce-Business . . . 0510
Finance . . . 0511
History . . . 0358
Labor . . . 0366
Theory . . . 0351
Folklore . . . 0578
Geography . . . 0351
Gerontology . . . 0578
History . . . 0578
General . . . 0578

Ancient . . . 0579
Medieval . . . 0581
Modern . . . 0582
Black . . . 0328
African . . . 0331
Asia, Australia and Oceania . . . 0332
Canadian . . . 0334
European . . . 0335
Latin American . . . 0336
Middle Eastern . . . 0337
United States . . . 0585
History of Science . . . 0398
Law . . . 0615
Political Science . . . 0616
General . . . 0617
International Law and . . . 0814
Relations . . . 0452
Public Administration . . . 0626
Recreation . . . 0627
Social Work . . . 0938
Sociology . . . 0631
General . . . 0628
Criminology and Penology . . . 0629
Demography . . . 0630
Ethnic and Racial Studies . . . 0700
Individual and Family . . . 0344
Studies . . . 0709
Industrial and Labor . . . 0999
Relations . . . 0453
Public and Social Welfare . . . 0453
Social Structure and . . . 0453
Development . . . 0453
Theory and Methods . . . 0453
Transportation . . . 0453
Urban and Regional Planning . . . 0453
Women's Studies . . . 0453

THE SCIENCES AND ENGINEERING

BIOLOGICAL SCIENCES

Agriculture . . . 0473
General . . . 0285
Agronomy . . . 0475
Animal Culture and . . . 0476
Nutrition . . . 0359
Animal Pathology . . . 0478
Food Science and . . . 0479
Technology . . . 0480
Forestry and Wildlife . . . 0817
Plant Culture . . . 0777
Plant Pathology . . . 0746
Plant Physiology . . . 0306
Range Management . . . 0287
Wood Technology . . . 0308
Biology . . . 0309
General . . . 0379
Anatomy . . . 0329
Biostatistics . . . 0353
Botany . . . 0369
Cell . . . 0793
Ecology . . . 0410
Entomology . . . 0307
Genetics . . . 0317
Limnology . . . 0416
Microbiology . . . 0433
Molecular . . . 0778
Neuroscience . . . 0472
Oceanography . . . 0786
Physiology . . . 0760
Radiation . . . 0425
Veterinary Science . . . 0996
Zoology . . . 0425
Biophysics . . . 0996
General . . . 0425
Medical . . . 0996

EARTH SCIENCES

Biogeochemistry . . . 0425
Geochemistry . . . 0996

Geodesy . . . 0370
Geology . . . 0372
Geophysics . . . 0373
Hydrology . . . 0388
Mineralogy . . . 0411
Paleobotany . . . 0345
Paleoecology . . . 0426
Paleontology . . . 0418
Paleozoology . . . 0985
Polymology . . . 0427
Physical Geography . . . 0368
Physical Oceanography . . . 0415

HEALTH AND ENVIRONMENTAL

Sciences . . . 0768
Environmental Sciences . . . 0566
Health Sciences . . . 0300
General . . . 0992
Audiology . . . 0567
Chemotherapy . . . 0350
Dentistry . . . 0769
Education . . . 0758
Hospital Management . . . 0982
Human Development . . . 0564
Immunology . . . 0347
Medicine and Surgery . . . 0569
Mental Health . . . 0570
Nursing . . . 0380
Nutrition . . . 0354
Obstetrics and Gynecology . . . 0381
Occupational: health and . . . 0571
Therapy . . . 0419
Ophthalmology . . . 0572
Pathology . . . 0382
Pharmacology . . . 0573
Pharmacy . . . 0574
Physical Therapy . . . 0575
Public Health . . . 0575
Radiology . . . 0575
Recreation . . . 0575

Speech Pathology . . . 0460
Toxicology . . . 0383
Home Economics . . . 0386

PHYSICAL SCIENCES

Pure Sciences . . . 0485
Chemistry . . . 0749
General . . . 0486
Agricultural . . . 0487
Analytical . . . 0488
Biochemistry . . . 0738
Inorganic . . . 0490
Nuclear . . . 0491
Organic . . . 0494
Pharmaceutical . . . 0495
Physical . . . 0754
Polymer . . . 0405
Radiation . . . 0605
Mathematics . . . 0986
Physics . . . 0606
General . . . 0608
Acoustics . . . 0748
Astronomy and . . . 0607
Astrophysics . . . 0608
Atmospheric Science . . . 0748
Atomic . . . 0607
Electronics and Electricity . . . 0798
Elementary Particles and . . . 0759
High Energy . . . 0609
Fluid and Plasma . . . 0610
Molecular . . . 0752
Nuclear . . . 0756
Optics . . . 0611
Radiation . . . 0463
Solid State . . . 0346
Statistics . . . 0984

Applied Sciences

Applied Mechanics . . . 0346
Computer Science . . . 0984

Engineering . . . 0537
General . . . 0538
Aerospace . . . 0539
Agricultural . . . 0540
Automotive . . . 0541
Biomedical . . . 0542
Chemical . . . 0543
Civil . . . 0544
Electronics and Electrical . . . 0348
Heat and Thermodynamics . . . 0545
Hydraulic . . . 0546
Industrial . . . 0547
Marine . . . 0794
Materials Science . . . 0548
Mechanical . . . 0743
Metallurgy . . . 0551
Mining . . . 0552
Nuclear . . . 0549
Packaging . . . 0765
Petroleum . . . 0554
Sanitary and Municipal . . . 0790
System Science . . . 0428
Geotechnology . . . 0796
Operations Research . . . 0795
Plastics Technology . . . 0994
Textile Technology . . . 0994

PSYCHOLOGY

General . . . 0621
Behavioral . . . 0384
Clinical . . . 0622
Developmental . . . 0620
Experimental . . . 0623
Individual . . . 0624
Personality . . . 0625
Physiological . . . 0989
Psychobiology . . . 0349
Psychometrics . . . 0632
Social . . . 0451

The undersigned recommend to the Faculty of Graduate Studies and Research
the acceptance of the thesis:

"Platinum Salicide Process for BiCMOS Applications"

submitted by Khalid Sheergar in partial fulfillment of the requirements for the
degree of **Master of Engineering**

Thesis Supervisors:

Dr. Abdalla Naem

Dr. Tom Smy

Dr. Jim Wight

**Chairman,
Department of Electronics**

September 1993

ABSTRACT

A platinum silicide process for submicron BiCMOS applications has been developed using rapid thermal processing. Platinum silicide's growth kinetics, phase growth sequence and impurity snow-plowing effect have been studied. Platinum silicide (PtSi) was formed on various types of substrates. The results were characterized using various physical analyses. New test masks were designed and laid out. The silicide process was successfully implemented in a full NMOS process flow to investigate the impact of PtSi on MOS transistors and ring oscillators. Platinum silicided Schottky barrier diodes and p-n junctions were also fabricated and characterized.

The growth of PtSi was observed to follow an Arrhenious relationship with an activation energy of 1.65 eV. The phase growth sequence was observed to be $\text{Pt} \rightarrow \text{Pt}_2\text{Si} \rightarrow \text{PtSi}$. During PtSi formation, impurities, specifically arsenic, boron and phosphorus, were observed to snow-plow resulting in high impurity concentrations at the PtSi/Si interface. The lowest specific contact resistivity of PtSi to p^+ Si achieved was $1.2 \times 10^{-7} \Omega\text{-cm}^2$ for a boron dose of $5 \times 10^{15} \text{ cm}^{-2}$ at 20 KeV, whereas for PtSi to n^+ Si, the lowest contact resistivity achieved was $1.4 \times 10^{-7} \Omega\text{-cm}^2$, for an arsenic dose of $7 \times 10^{15} \text{ cm}^{-2}$ at 50 KeV. The ideality factor of Schottky barrier diodes formed by PtSi on n^- Si and with p^+ guard ring was found to be 1.04. The leakage current level was about $3 \mu\text{A}/\text{cm}^2$ at a reverse bias of 5 volts. The ideality factor of platinum silicided area intensive p-n junctions was calculated as 1.01. The leakage current in this case was of the order of $27 \text{ nA}/\text{cm}^2$ at a reverse bias of 5 volts. The silicided process was successfully implemented using gate oxide as a side-wall spacer oxide. The silicided process was found to increase the MOS transistor current drive by 10-20 percent and ring oscillator speed by about 30 percent, using a very thin PtSi film of 500 Å.

ACKNOWLEDGMENT

I would like to take this opportunity to thank my supervisors, Dr. Tom Smy of Carleton University and Dr. Abdalla Naem of Northern Telecom Limited for their valuable guidance and insight into the subject matter. I would also like to thank Dr. Garry Tarr for his assistance in device fabrication and Dr. Dave Walkey for his help in device testing. The staff at the Carleton IC fabrication facility, Mr. Lyall Berndt, Mrs. Carol Adams, Mr. Yaz Fujimoto and Mr. Rick Shelley need also to be commended for their outstanding support. Thanks are also due to Drs. Louise Weaver, Martinee Simard Normandin and Brian Oliver of Northern Telecom Limited for their assistance in TEM, AES, RBS and SIMS analyses. I would also like to acknowledge Dr. I. D. Calder and Dr. G. Jolly of Northern Telecom Limited for their help in process simulation and temperature characterization of the sputtering system respectively. The financial support for this research provided by the Department of Electronics and Northern Telecom Limited is sincerely appreciated without which this work would not have been possible. Last but not the least, I wish to acknowledge my family for their support, understanding and patience.

TABLE OF CONTENTS

ABSTRACT	i
ACKNOWLEDGMENT	ii
TABLE OF CONTENTS	iii
LIST OF FIGURES	v
LIST OF TABLES	xi
LIST OF SYMBOLS AND ABBREVIATIONS	xii
Chapter 1 Introduction	1
Chapter 2 Application of Platinum Silicide in BiCMOS Technology	15
2.1 Impurity Redistribution	15
2.3 Platinum Silicide as a Source/Drain and Emitter Contact Material	19
2.3 Platinum Silicide as a Schottky Barrier Metal	20
Chapter 3 Experimental procedure	26
3.1 Sample preparation	26
3.2 Physical characterization	29
3.2.1 Auger electron spectroscopy (AES)	29
3.2.2 Rutherford backscattering analysis (RBS)	29
3.2.3 Transmission electron microscopy (TEM)	30
3.2.4 Secondary ion mass spectroscopy (SIMS)	30
3.3 Test Structure Design	31
3.4 Device Processing	32
Chapter 4 Results	35
4.1 Physical Analyses	35
4.1.1 Auger depth profiles	35
4.1.2 Rutherford backscattering spectra	39
4.1.3 Impurity snow-plowing effect for platinum silicide	42
4.1.4 Transmission electron microscopy micrographs	44
4.2 Electrical Analysis	47
4.2.1 PtSi sheet resistance on undoped wafers	47

4.2.2	PtSi sheet resistance on doped wafers	49
4.2.2.1	Arsenic doped wafers	49
4.2.2.2	Phosphorus doped wafers	53
4.2.2.3	Boron doped wafers	56
4.2.3	Contact resistances	59
4.2.4	Devices	66
4.2.4.1	Schottky barrier diodes	67
4.2.4.2	PN junctions	70
4.2.5	Salicided NMOS transistors	72
Chapter 5	Discussions	76
5.1	PtSi metallurgy	76
5.2	Impurity snow-plowing effect	81
5.3	Contact resistance	84
5.4	Devices	85
5.4.1	Schottky barrier diodes	85
5.4.2	PN junctions	85
5.4.3	Salicided NMOS transistors	86
Chapter 6	Conclusion	87
REFERENCES		92
APPENDICES		96
Appendix I	(Test structure layout)	97
Appendix II	(Device process flow)	102
II.1	Process flow for contact chain, Kelvin structure, Van-der-Pauw structure, Schottky barrier diodes and PN junctions	102
II.2	Process flow for Carleton NMOS technology	105
Appendix III	(Additional sheet resistance plots)	107

LIST OF FIGURES

<u>FIGURE NO.</u>	<u>DESCRIPTION</u>	<u>PAGE NO.</u>
1.1	Schematic representation of the current flow and parasitic resistances in the source/drain region of a conventional MOS transistor .	2
1.2	Junction spiking as a result of high temperature sintering of an Al-Si system.	4
1.3	a) Metal-Si interface before reaction and b) interface moves into the bulk of the Si after silicide formation.	5
1.4	MOS transistor showing Ti self aligned silicide (SALICIDE) technology implementation. Gate and S/D can be seen as shorted due to Ti silicide overgrowth on side-wall spacers.	9
1.5	Impurity profiles: a) before silicidation, (b) depletion of impurity at the TiSi_2/Si interface after TiSi_2 formation.	11
2.3.1	Reduction in storage time of a Schottky clamped transistor.	20
2.3.2	a) BJT in saturation, b) BJT with Schottky clamp diode, and c) IC implementation of a salicided Schottky clamp diode.	22
3.1.1	Cross sectional view of a typical tungsten halogen lamp heated Rapid Thermal Processing (RTP) System.	27
3.1.2	Typical RTP thermal cycle for a $500^\circ\text{C}/10\text{ sec}$ anneal.	28
3.3	Cross-section of a MOS device at various stages of salicidation (a) after side-wall spacer etch and (b) after silicide patterning.	34
3.4	Use of gate oxide, as against conventional side wall spacers, to isolate the gate, S/D region of a MOS transistor during PtSi formation.	34
4.1.1.1	AES depth profiles of Pt-Si structures annealed at 350°C for various RTP times, showing the silicide growth from Pt film to Pt_2Si (metastable phase) to PtSi (stable phase).	37
4.1.1.2	AES depth profiles of Pt-Si structures annealed at 400°C for	

	various RTP times, showing the silicide growth from Pt film to Pt ₂ Si (metastable phase) to PtSi (stable phase).	37
4.1.1.3	AES depth profiles of Pt-Si structures annealed for 10 sec. at various RTP temperatures, showing the silicide growth from Pt film to Pt ₂ Si (metastable phase) to PtSi (stable phase).	38
4.1.1.4	AES depth profile of a Pt film annealed in an oxygen contaminated RTP ambient at 500° C for 10 sec. O ₂ pile-up at the Pt/PtSi interface can be clearly seen.	38
4.1.2.1	RBS spectra of Pt-Si structure annealed at 350° C for various RTP times, showing the silicide phase growth sequence from Pt to Pt ₂ Si (metastable phase) to PtSi (stable phase).	40
4.1.2.2	RBS spectra of Pt-Si structure annealed at 400° C for various RTP times, showing the silicide phase growth sequence from Pt to Pt ₂ Si (metastable phase) to PtSi (stable phase).	40
4.1.2.3	RBS spectra of Pt-Si structure annealed for 10 sec at various RTP temperatures, showing the silicide phase growth sequence from Pt to Pt ₂ Si (metastable phase) to PtSi (stable phase).	41
4.1.3.1	SIMS impurity depth profile of two samples doped with 5E15 cm ⁻² of As ⁺ at 50 KeV. One of the samples was deposited with 550±50 Å of Pt and annealed at 550°C for 10 sec. As ⁺ pile-up at PtSi/Si interface can be clearly seen.	41
4.1.3.2	SIMS impurity depth profile of two samples doped with 5E15 cm ⁻² of B ⁺ at 10 KeV. One of the samples was deposited with 550±50 Å of Pt and annealed at 550°C for 10 sec. B ⁺ pile-up at PtSi/Si interface can be clearly seen.	43
4.1.3.2	SIMS impurity depth profile of two samples doped with 1E16 cm ⁻² of P ⁺ at 30 KeV. One of the samples was deposited with 550±50 Å of Pt and annealed at 550°C for 10 sec. P ⁺ pile-up at PtSi/Si interface can be clearly seen.	43
4.1.4.1	TEM micrograph of the cross-section of a sputtered Pt film.	45
4.1.4.2	TEM micrograph of the cross-section of a sample annealed at a RTP cycle of 350°C/10 sec. The top layer is Pt whereas the bottom layer is Pt ₂ Si.	45

4.1.4.3	TEM micrograph of the cross-section of a sample annealed at a RTP cycle of 400°C/10 sec. The top layer is Pt ₂ Si whereas the bottom layer is PtSi.	46
4.1.4.4	TEM micrograph of the cross-section of a sample annealed at a RTP cycle of 500°C/10 sec.	46
4.2.1.1a	Sheet resistance of PtSi on an undoped wafer, as a function of temperature at constant annealing times of i) 10 sec., ii) 15 sec., and iii) 20 sec.	48
4.2.1.1b	Sheet resistance of PtSi on an undoped wafer as a function of annealing time at constant temperatures.	48
4.2.2.1a	R _{sh} of Pt-Si structure as a function of temperature for constant RTP anneal times on wafer implanted with 5E15 cm ⁻² of As ⁺ at 50 keV and activated at 1050° C/30 sec. The as-deposited Pt thickness was 550±50 Å.	50
4.2.2.1b	R _{sh} as a function of anneal times at constant RTP temperatures on wafer implanted with 5E15 cm ⁻² of As ⁺ at 50 keV and activated at 1050° C/30 sec. The as-deposited Pt thickness was 550±50 Å.	50
4.2.2.1.2a	R _{sh} of PtSi as a function of temperature for a fixed RTP anneal time of 10 sec, formed on wafer implanted with various As ⁺ doses and activated at 1050° C/30 sec. In all the cases, the starting Pt thickness was 550±50 Å.	51
4.2.2.1.2b	R _{sh} of PtSi as a function of temperature for a fixed RTP anneal time of 10 sec, formed on wafer implanted with various As ⁺ doses. No implant and activation anneal was done. In all the cases, the starting Pt thickness was 550±50 Å.	51
4.2.2.2.1a	R _{sh} of Pt-Si structure as a function of temperature for constant RTP anneal times, on wafer implanted with 1E16 cm ⁻² of P ⁺ at 30 keV and activated at 1050° C/30 sec. The as-deposited Pt thickness was 550±50 Å.	54
4.2.2.2.1b	R _{sh} as a function of anneal times at constant RTP temperatures, on wafer implanted with 1E16 cm ⁻² of P ⁺ at 30 keV and activated at 1050° C/30 sec. The as-deposited Pt thickness was 550±50 Å.	54
4.2.2.2.2a	R _{sh} of PtSi as a function of temperature for a fixed RTP anneal	

	time of 10 sec., formed on wafer implanted with various P ⁺ doses and activated at 1050° C/30 sec. In all the cases, the starting Pt thickness was 550±50 Å.	55
4.2.2.2.2b	R _{sh} of PtSi as a function of temperature for a fixed RTP anneal time of 10 sec., formed on wafer implanted with various P ⁺ doses. No implant and activation anneal was done. In all the cases the starting Pt thickness was 550±50 Å.	55
4.2.2.3.2a	R _{sh} of Pt-Si structure as a function of temperature for constant RTP anneal times, on wafer implanted with 3E15 cm ⁻² of B ⁺ at 10 keV and activated at 1050°C/30 sec. The as-deposited Pt thickness was 550±50 Å.	57
4.2.2.3.1b	R _{sh} as a function of anneal times at constant RTP temperatures, on wafer implanted with 5E15 cm ⁻² of B ⁺ at 10 keV and activated at 1050° C/30 sec. The as-deposited Pt thickness was 550±50 Å.	57
4.2.2.3.2a	R _{sh} of PtSi as a function of temperature for a fixed RTP anneal time of 10 sec., formed on wafer implanted with various B ⁺ doses and activated at 1050° C/30 sec. In all cases, the starting Pt thickness was 550±50 Å.	58
4.2.2	Sheet resistance of PtSi as a function of As ⁺ , B ⁺ and P ⁺ doses. As ⁺ was implanted at 50, B ⁺ at 10 and P ⁺ at 30 KeV. Implant activation cycle was 1050°C/30 sec. In all the cases, PtSi formation was done under identical conditions.	58
4.2.3.1	Contact resistance versus contact area for Al-PtSi - p ⁺ Si and Al -p ⁺ Si contacts. The B ⁺ dose was 5E15 cm ⁻² at 20 KeV and the implant activation cycle was 1050°C/30 sec. The as-deposited Pt thickness was 550±50 Å and the RTP anneal cycle was 550°C/10 sec.	62
4.2.3.2	Contact resistance versus contact area for Al-PtSi to n ⁺ Si and Al to n ⁺ Si contacts. The As ⁺ dose was 5E15 cm ⁻² at 50 KeV and the implant activation cycle was 1050°C/30 sec. The as-deposited Pt thickness was 550±50 Å and the RTP anneal cycle was 550°C/10 sec.	62
4.2.3.3	Comparison between contact resistances of Al-PtSi - p ⁺ Si and Al -PtSi to n ⁺ Si contacts. The B ⁺ dose was 5E15 cm ⁻² at 20 KeV and the As ⁺ dose was 5E15 cm ⁻² at 50 KeV. The implant activation	

	cycle was 1050°C/30 sec.	64
4.2.3.4	Contact resistance of Al-PtSi and Al to p ⁺ polysilicon as a function of contact area. The B ⁺ dose was 5E15 cm ⁻² at 20 KeV and the implant activation cycle was 1050°C/30 sec. The as-deposited Pt thickness was 550±50 Å and the RTP anneal cycle was 550°C/10 sec.	65
4.3.1.1	Schottky diode structures, (a) without p ⁺ guard ring and (b) with p ⁺ guard ring.	68
4.3.1.1	I-V characteristics of a typical Schottky barrier diode with p ⁺ guard ring. The area of the diode was 2500 μm ² . I _E is in A per cm ² .	69
4.3.1.2	I-V characteristics of a typical Schottky barrier diode without p ⁺ guard ring. The area of the diode was 2500 μm ² . I _E is in A per cm ² .	69
4.3.2.1	I-V characteristics of a typical p ⁺ n junction. The area of the diode is 2500 μm ² . I _E is in A per cm ² .	71
4.3.3.1	I _D -V _{DS} characteristics of a typical unsilicided NMOS transistor with L/W = 10 μm/75 μm. I _D shown is in per micron width of the channel.	74
4.3.3.2	I _D -V _{DS} characteristics of a typical silicided NMOS transistor with L/W = 10 μm/75 μm. I _D shown is in per micron width of the channel.	74
4.3.3.3	I _D -V _{DS} characteristics of a typical unsilicided NMOS transistor with L/W = 5 μm/75 μm. I _D shown is in per micron width of the channel.	75
4.3.3.4	I _D -V _{DS} characteristics of a typical silicided NMOS transistor with L/W = 5 μm/75 μm. I _D shown is in per micron width of the channel.	75
5.1.1	Plot of PtSi thickness growth versus √annealing time at 350°C and 400°C in RTP.	79
5.1.2	Plot of Pt diffusivity at 350°C and 400°C versus reciprocal of temperature.	79
5.2.1	Schematic showing the impurity snow-plowing mechanism during PtSi growth.	82
I.1	Layout of a typical contact chain structure	98

I.2	Typical layout of the Kelvin structure	98
I.3a	Typical layout of a Schottky diode without p ⁺ guard ring	99
I.3b	Typical layout of a Schottky diode with p ⁺ guard ring	99
I.4a	Typical layout of a pn junction (area intensive)	100
I.4b	Typical layout of a pn junction (edge intensive)	101
I.5	Typical layout of a Van-der-Pauw structure	101
III.1.1a	Sheet resistance of Pt-Si structure as a function of temperature for constant RTP anneal times, on wafer implanted with 4E16 cm ⁻² of As ⁺ at 50 keV and activated at 1050° C/30 sec.	108
III.1.1b	Sheet resistance as a function of anneal times at constant RTP temperatures, on wafer implanted with 4E16 cm ⁻² of As ⁺ at 40 KeV and activated at 1050° C/30 sec.	108
III.1.2a	Sheet resistance of Pt-Si structure as a function of temperature for constant RTP anneal times, on wafer implanted with 1E16 cm ⁻² of As ⁺ at 50 keV and activated at 1050° C/30 sec. The as-deposited Pt thickness was 550±50 Å.	109
III.1.2b	Sheet resistance as a function of anneal times at constant RTP temperatures, on wafer implanted with 1E16 cm ⁻² of As ⁺ at 50 keV and activated at 1050° C/30 sec. The as-deposited Pt thickness was 550±50 Å.	109
III.1.3a	Sheet resistance of Pt-Si structure as a function of temperature for constant RTP anneal times, on wafer implanted with 7E15 cm ⁻² of As ⁺ at 50 keV and activated at 1050° C/30 sec. The as-deposited Pt thickness was 550±50 Å.	110
III.1.3b	Sheet resistance as a function of anneal times at constant RTP temperatures, on wafer implanted with 7E15 cm ⁻² of As ⁺ at 50 keV and activated at 1050° C/30 sec. The as-deposited Pt thickness was 550±50 Å.	110
III.2.1a	Sheet resistance of Pt-Si structure as a function of temperature for constant RTP anneal times, on wafer implanted with 2E16 cm ⁻² of P ⁺ at 30 keV and activated at 1050° C/30 sec. The as-deposited Pt thickness was 550±50 Å.	111

III.2.1b	Sheet resistance as a function of anneal times at constant RTP temperatures, on wafer implanted with $2\text{E}16\text{ cm}^{-2}$ of P^+ at 30 keV and activated at $1050^\circ\text{ C}/30\text{ sec}$. The as deposited Pt thickness was $550\pm50\text{ \AA}$.	111
III.2.2a	Sheet resistance of Pt-Si structure as a function of temperature for constant RTP anneal times, on wafer implanted with $7\text{E}15\text{ cm}^{-2}$ of P^+ at 30 keV and activated at $1050^\circ\text{ C}/30\text{ sec}$. The as-deposited Pt thickness was $550\pm50\text{ \AA}$.	112
III.2.2b	Sheet resistance as a function of anneal times at constant RTP temperatures, on wafer implanted with $7\text{E}15\text{ cm}^{-2}$ of P^+ at 30 keV and activated at $1050^\circ\text{ C}/30\text{ sec}$. The as deposited Pt thickness was $550\pm50\text{ \AA}$.	112
III.3.1a	Sheet resistance of Pt-Si structure as a function of temperature for constant RTP anneal times, on wafer implanted with $3\text{E}15\text{ cm}^{-2}$ of B^+ at 10 keV and activated at $1050^\circ\text{ C}/30\text{ sec}$. The as-deposited Pt thickness was $550\pm50\text{ \AA}$.	113
III.3.1b	Sheet resistance as a function of anneal times at constant RTP temperatures, on wafer implanted with $3\text{E}15\text{ cm}^{-2}$ of B^+ at 10 keV and activated at $1050^\circ\text{ C}/30\text{ sec}$. The as deposited Pt thickness was $550\pm50\text{ \AA}$.	113
III.3.2a	Sheet resistance of Pt-Si structure as a function of temperature for constant RTP anneal times, on wafer implanted with $7\text{E}15\text{ cm}^{-2}$ of B^+ at 10 keV and activated at $1050^\circ\text{ C}/30\text{ sec}$. The as-deposited Pt thickness was $550\pm50\text{ \AA}$.	114
III.3.2b	Sheet resistance as a function of anneal times at constant RTP temperatures, on wafer implanted with $7\text{E}15\text{ cm}^{-2}$ of B^+ at 10 keV and activated at $1050^\circ\text{ C}/30\text{ sec}$. The as deposited Pt thickness was $550\pm50\text{ \AA}$.	114

LIST OF TABLES

<u>TABLE NO.</u>	<u>DESCRIPTION</u>	<u>PAGE NO.</u>
1.1	Comparison of refractory and noble metals and their silicides.	7
1.2	Metals for silicide/salicide application.	8
1.3	Widely used silicides, their resistivity, selective etchant and silicon consumption.	8
2.3	Schottky Barrier Heights (ϕ_b) of various silicides to n and p type silicon	23
4.2.3.1	Al-PtSi to Si contact resistance as a function of implant dose and contact window size.	64
4.2.3.2	Al-PtSi to poly-Si contact resistance as a function of implant dose and contact window size.	65
4.3.1	Ideality factor, saturation leakage current (A/cm^2), current at reverse bias of 5 volts (A/cm^2) and effective barrier height of Schottky barrier diodes.	68
4.3.2	Ideality factor, saturation leakage current/ cm^2 and current/ cm^2 at reverse bias of 5 volts for p^+n diodes.	71
4.3.3	Matrix of platinum salicided NMOS transistors.	72
5.1.1	PtSi thickness formed as a function of temperature and time calculated from RBS analyses.	81
5.2.1	Integrated dopant concentration before and after silicidation for typical implant recipes of As^+ , B^+ and P^+ .	82
I.1	Test structures and their sizes.	97

LIST OF SYMBOLS AND ABBREVIATIONS

<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>UNITS</u>
A	Amperes	—
Å	Angstrom	10^{-8} cm
A^*	Effective Richardson constant	$120 \text{ A/cm}^2 \cdot \text{K}^2$
β_{npn}	Current gain of a BJT	—
l	Dimensional scaling factor	—
μ	Micron	10^{-4} cm
ρ_c	Specific contact resistivity	$\Omega\text{-cm}^2$
ρ	Sheet resistivity	$\Omega\text{-cm}$
Al	Aluminum	—
As ⁺	Arsenic	—
B ⁺	Boron	—
BHF	Buffered hydrofluoric acid	—
BJT	Bipolar junction transistor	—
Ci	Impurity concentration at silicide/Si interface if no dopant redistribution occurs.	atoms/cm ² .
Ci'	Impurity concentration at silicide/Si interface when dopant redistribution occurs.	atoms/cm ² .
Co	Cobalt	—
CoSi ₂	Cobalt -disilicide	—
DI	De-ionized	—
eV	Electron volt	1.61×10^{-19} volt
H	Hydrogen	—
H ₂ O	Water	—
H ₂ O ₂	Hydrogen peroxide	—

H₂SO₄	Sulfuric acid	—
HCl	Hydrochloric acid	—
HF	Hydrofluoric acid	—
HNO₃	Nitric acid	—
I_B	Base current of a BJT	mA
IC	Integrated circuit	—
K	Kelvin	—
k	Boltzmann's constant	1.38x10⁻²³J/k
k	Voltage scaling factor	—
MoSi₂	Molybdenum disilicide	—
n	Nano	10⁻⁹
N, N₂	Nitrogen (gas)	—
NH₄OH	Ammonium hydroxide	—
NiSi₂	Nickle disilicide	—
O, O₂	Oxygen	—
p	Pico	10⁻¹²
P+	Phosphorus	—
PdSi₂	Palladium silicide	—
Pt	Platinum	—
Pt₂Si	Platinum silicide (metastable phase)	—
PtSi	Platinum silicide (stable phase)	—
R	Resistance	Ω
R_{ac}	Accumulation layer resistance of MOS transistor	Ω/sq.
R_{diff}	Diffusion resistance	Ω
R_{sh}	Diffusion sheet resistance	Ω/sq.
R_{sp}	Spreading resistance	Ω/sq.
RIE	Reactive ion etching	—

RTA	Rapid thermal annealing	_____
RTP	Rapid thermal processing	_____
Sb	Antimony	_____
S/D	Source/drain of MOS transistor	_____
SF₆	Sulphur hexafluoride	_____
Si	Silicon	_____
SiO₂	Silicon-dioxide	_____
Ti	Titanium	_____
TiN	Titanium nitride	_____
TiSi₂	Titanium disilicide	_____
TTL	Transistor-transistor logic	_____
V_{BE}	Base-emitter voltage of a BJT	volts
V_{CB}	Collector-base voltage of a BJT	volts
V_{CC}	Collector voltage of a BJT	volts
W	Tungsten	_____

CHAPTER 1

Introduction

Ever since the device scaling laws [9-12] were proposed, the microelectronics technology has been characterized by a continuing trend towards miniaturization. The scaling of the active device dimensions allow for lower power dissipation and higher speed. Hence, the number of devices per chip can be drastically increased.

Due to scaling, the RC time constant product of an interconnect does not change; however, the device speed increases rapidly with scaling factor. Hence, interconnection propagation delay becomes increasingly dominant as λ (scaling factor) increases. Also, despite the reduction in the device dimensions, the area of silicon occupied by an individual IC has increased as more and more devices are integrated into the chip. As a result, the interconnect delays do not scale down linearly with the device size, but rather scale-up with increasing chip area. For example Saraswat et al. [13] have calculated that for 1 mm Al interconnect, the interconnection time delays are of the same order of magnitude as the delay of a CMOS inverter gate for an IC with an area of 10 mm².

Another most important factor in device degradation comes from the parasitic resistances in series with the channel as illustrated in figure 1.1. These include both the contact resistance (R_{co}) and diffusion resistance (R_{diff}). Ng and Lynch [14] have indicated the additional two components contributing to the series resistance as shown in figure (1.1). These are the accumulation layer resistance (R_{ac}) and the spreading resistance (R_{sp}). It can be seen that the current after leaving the channel, instead of spreading into the source/drain junction, prefers to follow the accumulation layer in the small part of the gate-junction overlap, due to low resistance of the accumulation layer as compared to the spreading resistance in the vicinity of the junction. These resistance components are a strong function of the doping gradient of the S/D junction and the gate voltage. The diffusion resistance component is given by

$$R_{diff} = \frac{R_{sh}}{W} L \quad (1.1)$$

where, R_{sh} is the sheet resistance /square, L the distance from contact hole to the gate edge and W the width of the transistor.

Figure (1.1): Schematic representation of the current flow and parasitic resistances in the source/drain region of a conventional MOS transistor [14]

The contact resistance R_{co} is defined as the resistance between the metal and the diffusion region under the leading edge of the contact. This includes the contributions from both, the metal-semiconductor interface and from the diffusion region under the contact. Modeling the contact by a transmission line (neglecting the resistivity of the metal itself and lateral current crowding effects), the contact resistance can be expressed as [14]:

$$R_{co} = \frac{\sqrt{R_{sh} \rho_c}}{W} \cdot \coth\left(L_c \sqrt{\frac{R_{sh}}{\rho_c}}\right) \quad (1.2)$$

where, L_c is the contact hole length and ρ_c the specific contact resistivity. For small contact holes (small L_c) and high contact resistivity (ρ_c), the contact resistance scales with the square of the scaling factor. This relation imposes restrictions on the choice of the metallization agent. The contact metal for sub-micron applications should therefore have very low contact resistance.

Presently, for integrated circuits having feature size in excess of 5 μm and junction depth over 2 μm , aluminum is the primary metallization agent being used. At such level of integration, generally the contact area is large enough so as not to have any appreciable effect on contact resistance and hence, the device performance. Even for feature sizes lower than 5 μm , aluminum is still being largely used as contact and as a final metallization agent. This is because of its ability to reduce native oxide, ease of deposition, good adherence to oxide, high conductivity, low cost and process compatibility. However, the barrier height of Al/Si contact (0.65-0.70 eV for Al-n type and 0.45-0.50 eV for Al-p type) is known to be very sensitive to the interface properties [15]. Also, a significant aging effect may be observed in the electrical characteristics of the contacts [15]. The low eutectic temperature of aluminum-silicon system plus the high solubility of silicon in aluminum also leads to problems like junction spiking during high temperature sintering, as shown in figure (1.2). Thus shallow junctions will be shorted. This puts a serious limitation on use of aluminum as a sole metallizing agent in sub-micron devices where contact area is very small and

Figure (1.2): Junction Spiking as a result of high temperature sintering of an Al-Si system.

junctions depth is in the range of 0.1-0.2 μm .

In order to overcome some of these problems, silicon based aluminum alloys have been used. The Si added to the Al satisfies the Si solid solubility requirements when the Al is sintered, so that no Si is dissolved from the contacts. However during cooling, the dissolved silicon comes out of solutions in two forms [16] as :

- a) silicon precipitates on nucleation sites such as pre existing silicon particles, grain boundaries, or steps in dielectric, or
- b) epitaxial growth on exposed areas of the Si substrate.

These precipitates may contain a large quantity of aluminum, and are believed to be the prime reason for high (of the order of $10^6 - 10^5 \Omega\text{-cm}^2$) contact resistivity of $\text{Al}_{1-x}\text{Si}_x$ to n^+ Si. In the scaled down devices, this would lead to an unacceptably high series resistance which scales as square of the scaling factor as per equation 1.2.

Since the early 1970s, in most commercial MOS transistors, the metal gate has been replaced by polysilicon. Use of polysilicon as a gate material allowed the source and drain junctions to be formed after gate patterning by diffusion or ion implantation. This is followed by a high temperature anneal to activate the dopants. In this way the source and drain areas can be formed self-aligned to the gate increasing the packing density and circuit performance. Also, polysilicon has good thermal and chemical stability.

The achievable sheet resistivities of polysilicon doped with P^+ or As^+ are in the range of 500-1000 $\mu\Omega\text{-cm}$. With the production of the 256K DRAMs in 1980s, it was evident that the polysilicon gate technology was limited due to propagation delays caused by the high resistivity of the gate material. With the then achievable polysilicon sheet resistance of 30-60 Ω/sq . [17], it was apparent that the advantage of further scaling would be offset by the interconnect resistance at the gate level.

In order to address these interconnected problems, silicide technology was proposed as a possible alternative because of its low resistivity and the ease with which it can be formed and patterned. Silicides are also stable throughout the device processing and usage. Silicide formation by the interaction of a metal film with the underlying silicon causes the silicide/silicon interface to move into the bulk of the silicon as shown in figure 1.3 and is therefore free of contamination and surface imperfection. This would then result in lower contact resistance between the silicide film and the underlying silicon.

Figure 1.3: a) Metal-Si interface before reaction, and (b) interface moves into the bulk of the Si after silicide formation.

During the last decade, interest in silicide has led to investigations which could be grouped in the following major categories [17]:

- a) studies aimed at understanding the physical properties of the silicides, kinetics of their formation and phase growth sequence,

- b) the use of silicides as Schottky barrier and ohmic contacts in integrated circuit technology, and finally
- c) the use of silicides as a low resistivity contact metallization for the gates and diffusion areas.

Though most of the elements in the periodic table react with silicon to form one or more forms of silicides, very few silicides are suitable for integrated circuit fabrication. Some of the criteria for any silicide to be useful for sub-micron technology can be summarized as:

- low resistivity,
- ease of silicide/salicide formation,
- absence of reaction with SiO_2 at the silicidation temperature,
- absence of lateral silicide formation,
- availability of a suitable etchant with good etch selectivity of the metal to its silicide for pattern generation,
- minimum silicon consumption during silicide formation as the junction depth is small,
- thermal stability at subsequent processing temperatures and at device operating conditions,
- compatibility with existing processing steps,
- no or minimal reaction with Al as final metallization metal,
- should not contaminate the devices,
- low stress, and
- should form reliable Schottky barrier diode

The above criteria narrow down the useful silicides to the silicon rich silicides in order to have thermal stability during silicidation and its usage. This can be further classified in to two categories: the refractory metal silicides and noble/near noble metal silicides. Table 1.1 compares the two groups of metal silicides.

On comparison of these two groups of silicides on the basis of the above listed criteria, the refractory metal silicides appear to be good for gate and source/drain metallization. The noble/near noble metal silicides are appropriate for Schottky barriers to n-type

TABLE 1.1: Comparison of Refractory and Noble Metals and their Silicides [17].

Property	Refractory Metal (From group IV A, V A & VI A)	Noble Metal (From group VIII)
Resistivity of the metal	Decreases with the atomic number in a period and in a group	Nearly the same for all ($7.5 \pm 2.5 \mu\Omega\text{-cm}$)
Resistivity of the silicide	Increases with the atomic number in a period and in a group	No correlation with the atomic number. Almost same for all metals ($25 \pm 10 \mu\Omega\text{-cm}$)
Schottky barrier of silicide to n type silicon	Almost same for all the metals ($0.55 \pm 0.05 \text{ eV}$)	Greater than half the silicon gap energy and increases with the atomic number
Silicidation temperature	$> 600^\circ \text{C}$	$300^\circ \text{C} - 800^\circ \text{C}$
Diffusing specie	Silicon	Metal
High temperature stability	Good	Satisfactory

and good ohmic contact to p-type silicon. It may be noted though that all of these silicides are good as ohmic contact to heavily doped silicon irrespective of dopant type. In this case the depletion width becomes so narrow that it becomes transparent to electrons which can tunnel through it.

Table 1.2 lists silicidation temperature, lowest binary eutectic temperature and resistivity of some of the silicides from these two groups which could be useful in sub-micron

silicide/salicide application. From this table, it can be inferred that from the refractory metal group, only TiSi_2 meets most of the selection criteria.

TABLE 1.2: Metals for Silicide/Salicide Applications [17].

Silicide	Silicidation Temperature ($^{\circ}\text{C}$)	Lowest Binary Eutectic Temp. ($^{\circ}\text{C}$)	Sheet Resistivity ($\mu\Omega\text{-cm}$)
Refractory Metals			
MoSi_2	1000	1410	120-130
NbSi_2	900	1295	~60
TiSi_2	800	1330	13-15
Noble/Near Noble Metals			
CoSi_2	700	1195	15-20
PtSi	500	850	28-38
Pd_2Si	300	720	30-35
NiSi_2	800	966	~50

Table 1.3: Widely used silicides, their resistivity, selective etchant and silicon consumption.

Silicide	Selective Etchant	ρ_c ($\mu\Omega\text{-cm}$)	Si used/ $\text{\AA}$ of metal	Silicide formed per $\text{\AA}$ of metal
TiSi_2	$\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:5\text{H}_2\text{O}$	13-15	2.26	2.37
CoSi_2	$3\text{HCl}:\text{H}_2\text{O}_2$	15-20	3.64	3.56
PtSi	$3\text{HCl}:\text{HNO}_3$	28-38	1.33	1.90

Presently, TiSi_2 is widely used in microelectronic fabrication to reduce the resistivity of polysilicon as well as diffusion areas, and as a contact to the gate and the source/drain regions. This is due to its low resistivity, compatibility with the current process steps,

thermal stability, minimal reaction with aluminum and low threat of contamination. However TiSi_2 is unsuitable for sub-micron applications where contacts are small, junctions are shallow, and dielectric thicknesses small. This is for various reasons as explained below:

- i) TiSi_2 has affinity for O, N, C and H. Hence it will getter these elements in the silicide increasing its sheet resistance. This will ultimately result in higher contact resistance which is already crucial in submicron regime.
- ii) Since Si is the diffusing specie during TiSi_2 formation, it tends to diffuse from the gate and the source/drain region into the Ti overlayer, and forms a silicide bridge over the spacer region as shown in figure 1.4, resulting in gate-S/D short. This undesirable lateral silicide

Figure (1.4): MOS transistor showing Ti self aligned silicide (SALICIDE) technology implementation. Gate and S/D can be seen as shorted due to Ti silicide overgrowth on side-wall spacers.

growth can be controlled by forming the silicides in N_2 ambient and using a two-step recipe. In a typical case [18], Ti is allowed to react with the underlying silicon for 30 seconds at 700°C using RTP in a nitrogen ambient. The TiN formed as the top layer and any unreacted Ti is then etched off to give a TiSi_2 sheet resistance of $5\Omega/\text{sq.}$ for a starting Ti film thickness of $500\text{ \AA}$. A second RTA anneal is performed at 800°C for 30 seconds to

stabilize the film and reduce its sheet resistance to $2\Omega/\text{sq}$. This introduces additional process steps, the process window becomes narrow and the process complex.

iii) It is formed at higher reaction temperature. In submicron devices, this would result in higher contact resistance due to depletion of dopant from the silicide/silicon interface. Most serious is the possible interaction between Ti and the oxide during the first annealing step, forming Ti oxide all over and shorting the entire wafer. This occurs quite often when there is a large fluctuation in the RTA temperature.

iv) It also suffers from higher silicon consumption. The silicon consumption for 1 Å of metal during silicides formation is listed in Table 1.3. This would result in loss of junction in submicron devices where junctions are quite shallow, bringing the TiSi interface closer to the junction depletion region. This would result in excessive leakage current.

v) Due to the decrease in the line width, the size of the oxide side wall spacer will be reduced as well. Since Ti reduces silicon oxide, this raises a question for use of TiSi_2 which will reduce the thin oxide side-wall spacer and bridge the gate and the source/drain region.

vi) TiSi_2 is less resistant to hydrofluoric acid (HF) etch. Consequently, processes like opening the contact windows in the dielectric and HF acid cleaning before Al metallization become difficult.

vii) Perhaps the most important of all the problems is the re-distribution of dopants [18] after TiSi_2 formation. Figure 1.5 (a) shows the impurity profile of a sample before silicidation, whereas figure 1.5 (b) gives the impurity profile after TiSi_2 formation. C_i represents the silicide/Si interface impurity concentration if no dopant redistribution occurs, whereas C_i' represents the actual interface impurity concentration when dopant redistribution occurs. It is clear from figure 1.5 (b) that the depletion of dopants has

Figure (1.5): Impurity profiles: a) before silicidation, (b) depletion of impurity at the TiSi_2/Si interface after TiSi_2 formation.

occurred at the TiSi_2/Si interface after TiSi_2 formation. For example, after TiSi_2 formation on As^+ and B^+ doped Si, accumulation of impurities at the Ti/TiSi_2 interface and depletion of impurities at the TiSi_2/Si interface has been reported [19]. This would give a very high contact resistance for small contacts and the very purpose of using the silicide technology would be lost.

Due to these serious limitations of TiSi_2 for its use in submicron technology, a renewed effort is being made to reconsider the silicides of noble/near noble metal especially PtSi and CoSi_2 as a possible alternative to TiSi_2 . These silicides have not received much attention so far because of limited data available in the literature concerning them, possible material contamination, the difficulties encountered in sintering them using conventional furnace annealing and in patterning [17]. Moreover, noble/near noble metal silicides exhibited low thermal stability [17] as compared to the silicides of the refractory metals. These silicides though have distinct advantages such as a high resistance to HF acid etch and less lateral silicidation. Their resistance to dry etch is also considerably higher [8]; three times that of TiSi_2 . These advantages are very much desirable even in today's submicron process.

The resistivity of cobalt silicide ($15\text{-}20\ \mu\Omega\text{-cm}$) is little higher than that of TiSi_2 ($13\text{-}15\ \mu\Omega\text{-cm}$), but it has a higher resistance to HF acid and plasma etching. Its dry etch selectivity to SiO_2 is observed to be 35:1 in SF_6 plasma [20]. However, like TiSi_2 , complete silicidation is achieved at a high temperature of about $700^\circ\text{-}750^\circ\text{C}$. At this temperature, Si becomes the dominant diffusing specie and like TiSi_2 , it also suffers from lateral overgrowth and a bridge between the gate and the source/drain region. This lateral overgrowth can be eliminated as in the case of TiSi_2 by using a two step annealing and using TiN as a capping layer [21]. However the temperature window becomes narrow as in the case of TiSi_2 and the process complicated. The CoSi_2 system also suffers from large silicon consumption as seen from Table 1.3.

On the other hand, PtSi has a high resistance to both HF acid and dry etching. Dry etch selectivity to SiO₂ being 33:1 [8] in SF₆ plasma. It consumes the minimum silicon of all the three silicides shown in Table 1.3. The reaction temperature of PtSi formation is low (475°-500° C) and Pt is the diffusing specie [8]. Thus the Pt-Si reaction would not suffer from lateral silicidation. PtSi formation has a favorable reaction with As⁺ and B⁺ doped silicon and is therefore suitable for deep sub-micron applications. Its high resistivity of about 28-38 μΩ-cm will not have any appreciable effect when minimal silicon consumption and favorable dopant redistribution (snow plowing) is considered.

Platinum silicide has therefore attracted interest for BiCMOS technology in the deep submicron regime because it can form reliable Schottky barrier diodes to n⁻ silicon and reproducible ohmic contacts can be formed at low reaction temperatures. Moreover, PtSi consumes minimal silicon which makes it look attractive for sub-micron technology where junctions will be shallow. Therefore, the objectives of this thesis are to:

- 1) understand the kinetics of platinum silicide formation and its phase growth sequence,
- 2) quantify the dopant redistribution (snow-plowing) effect of platinum silicide for arsenic, boron and phosphorus,
- 3) fabricate contact resistance test structures to examine the effect of snow-plowing on platinum silicided ohmic contacts to p⁺, n⁺ silicon and polysilicon,
- 4) fabricate and characterize electrically, platinum silicided Schottky barrier diodes with and without p⁺ guard ring structure,
- 5) implement the self-aligned silicided (SALICIDED) process in a full NMOS process flow to investigate the impact of platinum silicide on NMOS transistors with regard to their current drive capability and speed,
- 6) study the contamination issues, if any, of platinum silicide in IC fabrication technology.

The complete study will be done using rapid thermal processing (RTP). To the best of our knowledge, a detailed study like this has not been done yet, using RTP.

Chapter 2 is dedicated to a discussion of the applications of PtSi in BiCMOS technology. This is done on the bases of its impurity redistribution effect and low leakage Schottky barrier diode formation. Its importance in reducing the contact resistance to moderately and lightly doped junctions of BiCMOS devices in deep submicron region is also emphasized. In Chapter 3, the experimental procedure and the rapid thermal processor are described. Chapter 4 deals with the results obtained from these experiments. These results are analyzed in Chapter 5. Finally in Chapter 6, conclusions are drawn on the bases of experimental results presented in Chapter 4 and their analyses in Chapter 5. Recommendations on future work in this area are also highlighted in Chapter 6.

CHAPTER 2

Applications of Platinum Silicide in BiCMOS Technology

As discussed from the perspective of its application in submicron technology, among various silicides, platinum silicide appeared to be most promising. It was also pointed out that PtSi forms very reliable and low leakage Schottky barrier diodes. Hence in the deep submicron regime and particularly in BiCMOS technology, PtSi would play a critical role. This chapter is therefore dedicated to discussing the distinctive properties of PtSi. These include impurity snow-plowing effect and low leakage Schottky barrier diode formation. Its importance in reducing the contact resistance to moderately and lightly doped junctions of BiCMOS devices in deep submicron region will also be argued.

2.1 Impurity Redistribution

A definite amount of silicon is consumed to form any stable metal silicide. Normally, silicide is formed on implanted silicon. The impurities which previously resided in the silicon consumed in silicide formation will either be pushed into silicon and will accumulate

at the silicide/silicon interface, or will diffuse into the growing silicide through the grain boundaries in the silicide. This will depend on the diffusion coefficient of a particular impurity in the metal silicide and in the silicon and also on the solid solubility limit of a particular impurity in the silicide and in the silicon. There may be three distinct cases as discussed below:

- i) if the diffusion coefficient of the impurity in silicide is smaller than that in the silicon, the impurity which previously resided in the silicon will be seen to pile up at the growing silicide/silicon interface. This effect in literature is referred to as 'impurity snow-plowing' or 'accumulation',
- ii) if the diffusion coefficient of the impurity in silicide is equal to that in the silicon, the impurity which previously resided in the silicon consumed during silicide formation will remain in the silicide. However, if the quantity of the impurity exceeds the solid solubility limit of the impurity in the silicide, the excess impurity will show up on the silicide surface. The concentration of the impurity at the silicide/silicon interface will not change, and
- iii) if the diffusion coefficient of the impurity in the silicide is much higher than that in the silicon, not only the impurity previously residing in the silicon consumed during silicidation, but also the impurity from the silicide/silicon interface will diffuse into the growing silicide. This would result in the reduction in the concentration of the impurity at the silicide/silicon interface. This effect in literature is referred to as 'impurity depletion'. Again depending on the solid solubility limit of the impurity in the silicide, some impurity might show up on the silicide surface.

The accumulation of impurities at the silicide/Si interface as mentioned above has technological importance. This is due to increase in the dopant concentration at the silicide/silicon interface which results in lowering the contact resistance between the silicide

and the silicon or altering the effective barrier height of silicide to silicon. Lowering contact resistance is crucial for faster and denser circuits as pointed out in chapter I, whereas modifying the effective barrier height permits flexibility and innovation in circuit design. As an example, this technique can be used in tailoring the Schottky clamp diode performance in BiCMOS technology.

Increasing or decreasing the effective barrier height was first proposed and demonstrated by Shannon [23] for unreacted metal contacts to silicon which was implanted with low energy ions. A similar effect has also been observed with some silicide-silicon contacts using different metal silicides. Jeffrey B. Bindell [24] has demonstrated a barrier height reduction of up to 200 mV for PtSi to n-Si Schottky diodes with little degradation of reverse current characteristics .

Peter W. Lew and C.R. Helms [25] have studied the effect of platinum silicide thickness and annealing temperature on arsenic redistribution. The as deposited Pt thicknesses used were 200 Å, 500 Å and 1000 Å. The silicidation temperatures were 400°C and 500°C for 30 min. in furnace anneal. In all cases As⁺ appeared at the PtSi-Si interface. More As⁺ was found at the surface for higher temperature anneal. This might be due to the difference in diffusivity of Pt and As⁺ at higher temperature. As⁺ redistribution was higher for thicker PtSi films. This can be accounted for in terms of higher silicon consumption for thicker Pt films and consequently larger quantity of As⁺ available for redistribution.

M. Witmer and T.E. Seidel [26] studied the redistribution of implanted As⁺ and Sb⁺ (antimony) following metal silicide formation of Pt, Pd and Ni. Investigation with Rutherford backscattering analysis revealed that after the formation of silicide, Sb⁺ was always found in the silicide layer near the surface, whereas, PtSi and Pd₂Si caused a partial rejection of As⁺ for implanted doses of 2E15 cm⁻² and higher. This would result in the accumulation of As⁺ at the silicide-silicon interface. The results are discussed in terms of solid solubility limit as discussed above and the impurity-metal compound formation.

Akira Kikuchi and Shojiro Sugaki [27] have demonstrated the redistribution of implanted phosphorus (P^+) after platinum silicide formation and the characteristics of Schottky barrier diode. Spreading resistance measurement showed that the implanted P^+ atoms piled up near the PtSi-Si interface during PtSi formation. This phenomenon caused a reduction in the effective barrier height of PtSi to Si Schottky barrier diode. The higher the implant dose was, the larger was the reduction in the effective barrier height. This is quite obvious because of the fact that the higher P^+ implant dose will result in higher redistributed P^+ atoms at the PtSi-Si interface.

C.Y. Wei et al. [28] have studied the redistribution of p-type dopants (boron and indium) during Pt_xSi growth as a function of annealing time using secondary ion mass spectroscopy. During the early stages of the silicide growth, B^+ and indium was seen to pile up at the Pt_xSi -Si interface and concurrently getter to the defect sites located at the moving Pt- Pt_xSi interface. Even after completion of silicide formation, the dopants continued to out-diffuse to the surface via an enhanced mechanism due to defects and/or grain boundaries. No evidence of a 'snow-plow' effect was observed for either boron or indium at an implant dose of $2E13\text{ cm}^{-2}$. This could be either due to low implant dose used in this study or the longer furnace anneal cycle. Hence it is worth repeating the experiment with various implant doses and RTP anneal to form the silicide.

The snow-plowing effect in the case of PtSi can be used in advanced processing to make lightly doped junctions (LDJ) which will still have an ohmic contact. Drain engineering of hot carrier resistant MOSFETs is one of the major issue in advanced IC processing. The LDJ structure will help in reducing the hot carrier effect and minimize the short channel effects. This is due to low impurity concentration used in the junctions. In this case, the lateral impurity diffusion under the gate is minimal and also the peak electric field is confined in the LDJ region away from the gate region. This helps to suppress the hot carrier effect. On the other hand, the impurity accumulation at the silicide/silicon interface

caused by PtSi formation would reduce the contact resistance of silicide to LDJs. The formation of silicide on the LDJ will also help in reducing the diffusion resistance component of the junction. Therefore low doping concentration in the junction areas will not affect either the current drive or the speed of the MOS transistors.

2.2 Platinum Silicide as a Source/Drain and Emitter Contact Material

Very few studies have been reported so far on the results of the contact between PtSi and Si. A comprehensive study of microstructural and electrical properties of thin PtSi films has been carried out by Anderson and Reith [29]. In this study the specific contact resistance was studied for different deposition methods (sputtering and e-beam evaporation), surface preparation (chemical cleaning and/or sputter etching), annealing conditions (in-situ while depositing or using external furnace), and furnace ambient (clean as well as contaminated). The specific contact resistance obtained was in the range of 10^{-3} - 10^{-6} $\mu\Omega\text{-cm}^2$ for a contact area of approximately $2000 \mu\text{m}^2$. The high specific contact resistances in spite of large contact area are related to the poor quality of the evaporated Pt. and surface preparation. This and perhaps the contaminants introduced in the furnace anneal, may explain the high contact resistance obtained in that study. It is therefore evident that the microstructure and the electrical properties of PtSi thin film are sensitive to surface preparation techniques, the deposition method, dopant species and surface concentration.

S.S. Cohen et al. [30] have extensively studied the PtSi contacts to B^+ and As^+ doped silicon, also using a furnace anneal. In this study, the effect of dopant concentration, at the implant dose range of $1\text{-}8\text{E}15 \text{ cm}^{-2}$ at 20 KeV for boron and at 80 KeV for arsenic, was analyzed using $3 \times 3 \mu\text{m}^2$ contact Kelvin structure and about 400 Å of sputtered platinum. The specific contact resistance value of a PtSi contact to p-type Si obtained varied from $1.25 \times 10^{-6} \mu\Omega\text{-cm}^2$ for a B^+ implant dose of $1\text{E}15 \text{ cm}^{-2}$ to about $1.8 \times 10^{-7} \mu\Omega\text{-cm}^2$ for an implant dose of $6\text{E}15 \text{ cm}^{-2}$. The specific contact resistance value of PtSi to n-type Si was

observed to vary from $8 \times 10^{-7} \mu\Omega\text{-cm}^2$ for an As^+ implant dose of $2\text{E}15 \text{ cm}^{-2}$ to about $2 \times 10^{-7} \mu\Omega\text{-cm}^2$ for As^+ implant dose of $8\text{E}15/\text{cm}^2$. It is evident from this study that the specific contact resistance decreases with increase in implant dose for both B^+ and As^+ doped Si. The snow plowing effect was observed even for implant doses smaller than $4\text{E}15 \text{ cm}^{-2}$ in case of both B^+ as well as As^+ implanted junctions. No detrimental effect of the PtSi on Al used as a final metal was observed.

2.3 Platinum Silicide as a Schottky Barrier Metal

Among other properties, the suitability of any silicide for sub-micron, especially BiCMOS applications, depends on its reliability of Schottky barrier formation. A Schottky diode is basically similar in structure to an abrupt one sided p-n junction. However, it is a majority carrier device and has a low turn-on voltage. This makes these diodes very attractive and useful for future generation of high speed integrated circuits.

Figure 2.3.1: Reduction in the storage time of a Schottky clamped transistor [31].

If a Schottky diode is connected between the base and the collector of a bipolar transistor, the low turn-on voltage of the Schottky barrier diode can be used to prevent the bipolar transistor from going into deep saturation. In this case, the effect of the Schottky diode is to shunt the excess base current through the diode, thus reducing the excess charge transit time of the combination by one order of magnitude when compared to a transistor without Schottky diode as shown in figure 2.3.1 [31]. Figure 2.3.2 shows a bipolar transistor with and without a Schottky clamp diode and the basic integrated circuit implementation of the Schottky clamp diode with bipolar transistor. Without a Schottky diode the collector-base voltage of the BJT is given by

$$V_{CB} = V_{CC} - \beta_{npn} I_B R - V_{BE} \quad (2.3.1)$$

where β_{npn} is the current gain of the transistor.

For a sufficiently large base current, the collector base junction becomes forward biased, and the transistor goes into saturation region of operation. This would then increase the base storage time of the BJT and would result in slow switching response. This excess base current can be shunted by connecting the Schottky barrier between the base and the collector and an inherently fast switching response can be achieved.

Table 2.3 gives the Schottky barrier heights of various silicides to n and p type Si. It can be seen that the noble/near noble metal silicides, particularly of platinum, has high barrier height of 0.87 eV to n type Si and therefore would give very low leakage current. Hence, its silicide could prove very useful as Schottky barrier to n type Si and ohmic contact to p type Si. PtSi Schottky barriers have long been used in semiconductor industry in high speed TTL as clamping devices. However, very little data is available in the literature on the performance of the Schottky barriers fabricated using RTA.

Figure (2.3.2): a) BJT in saturation, b) BJT with Schottky clamp diode, and c) IC implementation of salicided Schottky clamp diode.

TABLE 2.3: Schottky Barrier Heights (ϕ_b) of various Silicides to n and p type Silicon [17,32].

Refractory Silicides	Barrier Height		Noble/Near Noble Metal Silicides	Barrier Height	
	(ϕ_{b_n}) eV	(ϕ_{b_p}) eV		(ϕ_{b_n}) eV	(ϕ_{b_p}) eV
TiSi ₂	0.6	0.5	CoSi ₂	0.64	0.46
MoSi ₂	0.55	0.55	PtSi	0.87	0.23
NbSi ₂	0.55	0.55	Pd ₂ Si	0.74	0.36
			NiSi ₂	0.7	0.4

D. Moy et al. [33] have demonstrated the effect of processing conditions on the characteristics of PtSi Schottky barrier diodes. In this study various contact openings and surface preparation techniques including BHF (buffered hydrofluoric acid) and RIE (reactive ion etching) etching were used. The study showed that each component has a distinct effect on the quality of the PtSi films and hence the Schottky barrier diode performance. Contacts etched by RIE resulted in better Schottky barrier diodes with less variation in the electrical properties of the devices. The ideality factor of the diodes fabricated was in the range of 1.05-1.07 with barrier heights of about 0.82-0.84.

B. Y. Tsaur [34] has evaluated the effect of interface structure on the electrical characteristics of PtSi-Si Schottky barrier contacts. In this study large diodes having area of about $9.4 \times 10^5 \mu\text{m}^2$ utilizing a shallow PtSi-Si contacts about 200 Å deep have been fabricated. The ideality factor obtained was 1.02 with a reverse leakage current of about 5 nA at -10 volts and a high breakdown voltage of over -90 volts. In this study alternate layers of Pt and Si were deposited and reacted to form a total PtSi thickness of about 1500 Å. This resulted in the formation of very shallow contacts in spite of a thick PtSi layer and did not pose any limitation on the thickness of the PtSi layer.

In a study conducted by E. K. Broadbent et al [35], ultra shallow p⁺/n junctions of about 70 nm were fabricated with self aligned PtSi using RTA. The I-V characteristics were near ideal having an ideality factor of 1.06 with a reverse bias leakage of 2 nA/cm². at -5 volts and breakdown voltage lower than -40 volts.

R. C. Ellwanger et al. [36] have fabricated PtSi Schottky barrier using RTA in oxygen/nitrogen ambient. The diode in this study were much improved in performance compared to those fabricated using a conventional furnace. The improvement basically came from the thick oxide formation over the PtSi in RTA as compared to the thin oxide formation in the conventional furnace. This gave the PtSi formed using RTA, a better etch resistance while etching the unreacted Pt over the oxide in aqua regia.

From the foregoing discussion, it can be inferred that for the future generation of integrated circuit fabrication technology, silicide of platinum would prove quite useful. It is also noticed that majority of the studies carried out so far make use of conventional furnace for silicide formation. Due to thermal budget constraint of future generation of deep submicron devices, rapid thermal processing would be inevitable. So quite a few studies have been done to study the PtSi growth kinetics and phase growth sequence using rapid thermal processing. However, to the best of our knowledge, a comprehensive study using rapid thermal annealing has not been done so far to study the snow-plowing effect for PtSi, effect of implant dose on silicide formation and sheet resistance, contact resistance of PtSi to n⁺, p⁺ Si and polysilicon with different doses of As⁺ and B⁺, electrical characteristics of Schottky barrier diodes with and without p⁺ guard ring, area and edge intensive p-n junctions and their comparison with Schottky barrier diode, the improvement in current drive and speed of silicided NMOS transistors. The following study has therefore concentrated on all these areas using rapid thermal processing. The PtSi growth kinetics and phase growth sequence has also been done so as to compare our results with those published in various literature.

Chapter 3 describes briefly the construction of a rapid thermal processor, the sample preparation techniques for PtSi growth kinetics and phase growth sequence experiments and also for the electrical characterization of PtSi film on doped samples with various doses of arsenic, boron and phosphorus. Various physical characterization techniques used are also briefly described in this chapter. Test structure design, mask generation has also been described. Process flow for these test structure has also been presented. The salicided NMOS transistor were fabricated using Carleton's NMOS process which has also been described. In order to investigate the lateral silicide growth, no side wall spacers were used. The results of these various studies are presented in chapter 4. These results are analyzed in the chapter 5. Finally in chapter 6, conclusions are presented and future work in these areas are highlighted.

CHAPTER 3

Experimental Procedure

3.1 Sample Preparation

To study the growth kinetics and phase growth sequence of platinum silicide, 2" Single crystal <100> oriented, 2-8 Ω -cm, p-type Si wafers were used. For snow-plowing effect experiments, 6" single crystals, <100> oriented, 13-17 Ω -cm wafers implanted with following species and doses as supplied by Northern Telecom Electronics Limited, Ottawa were used.

a) Arsenic

- i) 4 E16 cm⁻² at 40 KeV, ii) 1 E16 cm⁻² at 50 KeV,
- iii) 7 E15 cm⁻² at 50 KeV and iv) 5 E15 cm⁻² at 50 KeV.

b) Phosphorous

- i) 2 E16 cm⁻² at 30 KeV, ii) 1 E16 cm⁻² at 30 KeV, and
- iii) 7 E15 cm⁻² at 30 KeV.

c) Boron

- i) 7 E15 cm⁻² at 10 KeV, ii) 5 E15 cm⁻² at 10 KeV, and
- iii) 3 E15 cm⁻² at 10 KeV.

About 200 Å of cap oxide was deposited following the implant. The implant activation was carried out in an A. G. Associate Heat Pulse Model 210 at 1050° for 30 seconds. The cap oxide was then etched in 10:1 DI:HF solution and the wafers diced in quarters to be ready for platinum deposition.

Just prior to loading the wafers in MRC Model 620 sputtering system, wafers were given a one minute dip in dilute HF solution (HF:H₂O :: 1:10) to remove the native oxide, followed by 30-60 seconds DI water rinse. The undoped wafers also received a 1 min. in-situ sputter etch in 8 mTorr Argon pressure at 100 watts of RF power to remove any left over traces of native oxide. Subsequently, 550±50 Å of platinum was deposited at 8 mTorr Argon pressure and 100 watts of RF power (The base pressure being 5 x 10⁻⁷ Torr). The wafers were then cleaved in small pieces measuring about 2 cm x 2 cm and annealed in the RTP for various times and at various temperatures to form platinum silicide. A cross section of a typical rapid thermal processing system is shown in figure 3.1.1.

Figure (3.1.1): Cross sectional view of halogen heated Rapid Thermal Processing (RTP) System.

It consists of a chamber made from quartz tube which is heated by two rows of tungsten halogen lamps, one at the top and the other at the bottom. The wafer is transported to the chamber through a flat quartz stand attached to the chamber door. The wafers are heated by the radiation energy of the lamps. The wafer temperature is monitored through a chromel-alumel thermocouple embedded in a T-shaped silicon piece and pre-calibrated to represent the temperature of the wafer being processed. The operating temperature range is 300° - 1150° C with an accuracy of $\pm 7^\circ$ C. The heating rate is quite fast. It is of the order of 100°- 150° C per sec. A typical RTP annealing cycle of 500° C for 10 sec. is illustrated in figure 3.1.2. A maximum annealing time of 300 sec. can be attained.

Figure (3.1.2): Typical RTP thermal cycle for an 500° C/10 sec anneal.

Before loading the wafer, the chamber was purged with N₂ gas to expel any air present, the constituents of which are likely to contaminate the wafer, thereby hindering the salicidation process. The wafer is then loaded and heated by the radiation energy of the halogen lamp banks. As the chamber is quite small, the ambient condition can be controlled very efficiently.

3.2. Physical Characterization

3.2.1. Auger electron spectroscopy (AES)

AES has the capability of analyzing the energies of Auger electrons and measuring their intensities. The Auger electrons are generated by a high energy electron beam, as are secondary and backscattered electrons. However, Auger electrons are emitted only at discrete energies which are ultimately characteristic of the elements in the sample. Thus AES with sputter depth profiling can be used to study the phase growth progression qualitatively and to measure the oxygen, carbon and nitrogen contaminants level. A Phi 545 scanning Auger micrograph was used. The electron beam was set at 1 μ A and 5 KeV while the samples were sputtered with a 2 KeV Ar ion beam at 5×10^{-5} Torr Ar pressure. The ion beam was rastered over a couple of millimeters to flatten the sputter crater and hence increase the depth resolution.

3.2.2 Rutherford Back scattering spectrometry (RBS)

RBS analysis provides both qualitative and quantitative information of the layers. RBS depends upon the scattering of energies (MeV) ion beams from sample atoms; the mass energy of the scattered ions and the concentration of a particular element is deduced from the energy distribution of ions. The elemental depth distribution can be determined in a non-destructive fashion and the RBS technique provides absolute concentration with a accuracy of a few percentage points. RBS analyses were carried out on Van-de Graaff accelerator at Queen's University to study the phase growth, layer thickness and stoichiometry. The analysis employed a 2.275 MeV He^+ beam at 20° glancing angle. The beam spot diameter on the sample was 1 to 2 mm. Measurements were carried out at a chamber pressure of 2×10^{-7} Torr. Secondary electrons were suppressed by applying 90 V positive bias to the sample.

3.2.3 Transmission electron microscopy (TEM)

TEM analysis were carried out using a JEOL 2000FX STEM with 200 KeV electron beams to obtain cross-sectional views in order to study the various phases of the silicide layers and their thicknesses and determine the silicide/Si interface quality.

3.2.4 Secondary ion mass spectroscopy (SIMS)

Energetic ion bombardment of the surface causes atoms to be ejected from the sample by the sputtering process. A fraction of the ejected species are either positive or negative ions. This fraction is mass analyzed in a mass spectrometer to determine the elemental composition of the material from the sample surface. Because of the high sensitivity of the mass spectrometer, small traces of an element can be detected. All elements, even hydrogen, can be detected with SIMS. Moreover, element isotope ratios can be measured with a precision of better than $\pm 1.0\%$. Because of the sputtering nature of the technique, measurements of the ion currents as a function of time provides a depth-composition profile, from the original surface into the bulk of the material.

The instrument used for SIMS analysis in this study is a Cameca IMS-3f ion microscope. The IMS-3f can provide ion images with a spatial resolution of 0.5 μm . Three implants doses; $5 \times 10^{15} \text{ cm}^{-2}$ at 50 KeV of As^+ , $5 \times 10^{15} \text{ cm}^{-2}$ at 10 KeV of B^+ and $1 \times 10^{16} \text{ cm}^{-2}$ at 30 KeV of P^+ were chosen for SIMS analysis. Two samples were prepared from each implant recipe. One of the sample from each set was used as a reference sample for impurity profile before silicidation. The other sample from each set was deposited with $550 \pm 50 \text{ \AA}$ of Pt and annealed at 500°C for 10 sec. to form PtSi. Both of these samples were analyzed for impurity profile using SIMS analysis.

3.3 Test Structure Design

In order to evaluate the performance of the PtSi contacts and Schottky barrier diodes as well as to develop a salicide process, a test structure mask was designed and laid out using LEDIT layout software. The size of each die was 140 x 140 mil. The following test structures were incorporated;

- a) Contact chain (49 links) using PtSi contacts to p^+/n^+ Si, p^+/n^+ poly. Each chain had 98 contacts. The contact sizes were $2.5 \times 2.5 \mu\text{m}$, $3.75 \times 2.5 \mu\text{m}$, $3.75 \times 5 \mu\text{m}$ and $5 \times 5 \mu\text{m}$;
- b) Kelvin structures having PtSi contact sizes of $2.5 \times 2.5 \mu\text{m}$, $2.5 \times 3.75 \mu\text{m}$, $3.75 \times 3.75 \mu\text{m}$, $5 \times 5 \mu\text{m}$ and $3.75 \times 5 \mu\text{m}$ to p^+/n^+ Si and p^+/n^+ poly;
- c) Van- der- Pauw structure to evaluate the sheet resistance of p^+ , n^+ , poly silicon and PtSi;
- d) Schottky barrier diodes without guard ring in sizes ranging from $25 \mu\text{m}^2$ to $2500 \mu\text{m}^2$;
- e) Schottky barrier diode with p^+ guard ring with sizes from $25 \mu\text{m}^2$ - $2500 \mu\text{m}^2$;
- f) Area intensive platinum salicided p-n junctions with sizes from $140625 \mu\text{m}^2$ - $15625 \mu\text{m}^2$;
- g) Edge intensive platinum salicided p-n junctions with sizes from $7375 \mu\text{m}^2$ - $12375 \mu\text{m}^2$;
- h) Platinum salicided source/drain and gate NMOS transistors of various sizes;
- j) MOS capacitor having an area of $1600 \mu\text{m}^2$;

A detailed list of the above test structure along with their layout is included in Appendix I.

The LEDIT layout mask was used to generate patterns on 2" x 2" photographic plate for each layer on a 'David Mann 1600' pattern generator. The PG (photographic) plate so

generated was used to make a copy on a contact printer. Each copy was then stepped four times on a 'Jade Corporation' stepper to give 196 die on 2 1/2" x 2 1/2" plates.

3.4 Device Processing

In order to keep the process simple, three sets of wafers were used. Single crystal, <100> oriented, 3-7 Ω -cm, p type wafer were used to fabricate PtSi contacts to n^+ Si and n^+ polysilicon using contact chain and Kelvin structures, Van-der-Paw structures to measure the sheet resistance of n^+ diffused regions and n^+ p area and edge intensive diodes. Single crystal, <100> oriented, 10-50 Ω -cm, n type wafers were used fabricate PtSi contacts to p^+ Si and p^+ polysilicon using contact chain and Kelvin structures, Van-der-Paw structures to measure the sheet resistance of p^+ diffused regions and p^+ n area and edge intensive diodes. PtSi Schottky barrier diodes were formed on n^- substrate. The process flow for the fabrication of these structures is appended in Appendix II. The implantation were carried out at 'Implant center, California' and the following doses of As^+ and B^+ were used.

- i) Boron - $1E15, 3E15$ and $5E15 \text{ cm}^{-2}$ at 20 KeV
- ii) Arsenic- $3E15, 5E15$ and $7E15 \text{ cm}^{-2}$ at 50 KeV.

For fabrication of NMOS devices, single crystal, <100> oriented, 2-4 Ω -cm, p type wafers were used. The NMOS devices were fabricated using conventional Carleton's NMOS processes flow which is also described in Appendix II. In this process P^+ diffusion was used instead of implantation. The salicide (self-aligned silicide/polycide) process is described below.

The salicide process differs from the only gate silicidation process in that the source and drain regions are also silicided in addition to gate, without any need for an extra masking step. In a conventional salicide process, a conformal CVD oxide is deposited on gate, source and drain region after the gate is patterned. This oxide is then dry etched anisotropically to yield a structure with side-wall spacer oxide as shown in figure 3.3(a).

This requires a dry etch process with good selectivity of oxide to silicon or polysilicon. It is interesting to note here that the source and drain junctions can be implanted after the side wall spacer etch. This can also be done in two stages, a light implant after gate patterning and a second implant after side wall spacer etch. These would make the submicron devices resistant to punch through and hot electron effects. Pt is then deposited on this structure and annealed to form silicide on gate, source and drain region. The unreacted Pt on the oxide is then etched away in hot aqua regia. The cross section of the structure after patterning the silicide is shown in figure 3.3 (b).

The objective of our NMOS device fabrication was two fold. Firstly, to investigate the current drive capability of silicided NMOS as compared to an unsilicided one. Secondly, to investigate, if any, the lateral overgrowth of PtSi on side-wall spacers which would bridge the gate and source drain region rendering the device useless. Another objective was to simplify the silicide process by using the gate oxide as a side wall spacer oxide, to isolate the gate and S/D areas of a MOS transistor as shown in figure 3.4. This is possible because Pt is the diffusing specie during the silicide formation and Pt does not react with the oxide at the silicidation temperature. We tried various thickness of PtSi to estimate the maximum extent which can be formed without any short between the gate and source/drain region of MOS transistor with a gate dielectric thickness of 500 Å.

(a)

(b)

**Figure 3.3: Cross-section of MOS device at various stages of salicidation
(a) after side-wall spacer etch and (b) after silicide patterning.**

Figure 3.4: Use of gate oxide as a side wall spacer, to isolate the gate and source/drain region of a MOS transistor during Pt silicide formation.

CHAPTER 4

Results

4.1 Physical Analyses

4.1.1 Auger Depth Profiles

AES depth profiles of Pt-Si reaction at various RTP anneal cycles are presented in figures 4.1.1.1 through 4.1.1.14. Figure 4.1.1.1 gives the Pt and Si depth profiles showing silicide phase progression for samples annealed at 350° C and for various RTP anneal times. The reaction is seen to start at the Pt-Si interface with Pt diffusing into Si to react and form Pt₂Si. After a 10 to 15 sec anneal, two phases, Pt and Pt₂Si are observed. After a 20 sec. anneal, all the Pt is converted to Pt₂Si. For a 40 sec. anneal, part of Pt₂Si is converted to the stable PtSi phase and after a 70 sec. anneal, almost all the Pt₂Si is transformed to PtSi. Thus, there are three distinct phases observed in the Pt-Si reaction, viz. Pt, Pt₂Si and PtSi.

* Results from chapter 4 and chapter 5 were published in 'Very large scale Metal Interconnect Conference (VMIC)' proceedings, June 1993.

In none of the above cases, were all the three phases observed concurrently as can be seen from figure 4.1.1.1.

Figure 4.1.1.2 shows the depth profile for samples annealed at 400° C for various RTP anneal times. It is observed that all the Pt is converted to Pt₂Si in just 10 sec., as compared to 20 sec. at 350° C, as seen earlier. This translates to a growth rate of approximately two times faster at 400° C, as compared to at 350° C. After a 20 sec. anneal, all the Pt₂Si is converted to PtSi. Here also we did not see all the three phases simultaneously.

At 500° C, all the Pt is converted to stable phase of PtSi in mere 10 sec. anneal giving a growth rate about twice as fast as at 400° C. The silicide phase growth progressions at various temperatures for a fixed RTP anneal time of 10 sec. are illustrated in figure 4.1.1.3.

All the AES depth profiles exhibit uniform Pt and Si concentration levels qualitatively corresponding to Pt, Pt₂Si and PtSi. The absolute values of concentration levels for Pt, Pt in Pt₂Si and Pt in PtSi differ from 100 percent, 67 percent and 50 percent respectively. This might be due to noise within Auger electron intensity peak windows.

The film thickness can be calculated from the AES depth profile by multiplying the sputter time with the pre-calibrated sputter rate. This would generally be true for a homogeneous film structure. In the case of metal-Si reaction, as the structure is multilayer with different amounts of metal and Si, it is difficult to calculate the thickness of the various layers due to the fact that the various phases sputter at different rates.

All the AES depth profiles show small levels of contamination with carbon and oxygen in the reacted film as can be seen in figures 4.1.1.1 through 4.1.1.3. The oxygen peak at the surface may be due to a thin oxide layer at the surface of the reacted film. The carbon contamination might be from the sputter film deposition ambient.

Figure 4.1.1.1: AES depth profiles of Pt-Si structures annealed at 350°C for various RTP times, showing the silicide growth from Pt film to Pt₂Si (metastable phase) to PtSi (stable phase).

Figure 4.1.1.2: AES depth profiles of Pt-Si structures annealed at 400°C for various RTP times, showing the silicide growth from Pt film to Pt₂Si (metastable phase) to PtSi (stable phase).

Figure 4.1.1.3: AES depth profiles of Pt-Si structures annealed for 10 sec. at various RTP temperatures, showing the silicide growth from Pt film to Pt₂Si (metastable phase) to PtSi (stable phase).

Figure 4.1.1.4: AES depth profile of a Pt film annealed in an oxygen contaminated RTP ambient at 500° C for 10 sec. O₂ pile-up at the Pt/Pt₂Si interface can be clearly seen.

As stated earlier, maximum of only two of the three phases viz. Pt, Pt₂Si and PtSi are observed to exist simultaneously. This is true in case of clean Pt deposition and annealing conditions. If the original Pt film or the annealing ambient is contaminated with over 10 percent of oxygen content, then all the three phases may exist concurrently as can be seen in the AES depth profile of figure 4.1.1.4 In this case the RTP ambient was contaminated with oxygen. Initially, the reaction started successfully at the Pt-Si interface with Pt diffusing into Si to form Pt₂Si. In the mean time O₂ also diffuses through Pt. and accumulates under the top Pt surface. As soon as the O₂ front in excess of 10 atomic percentage meets the Pt-Pt₂Si, the diffusion of Pt is impeded, preventing further formation of Pt₂Si any further. However, the Pt from the Pt₂Si can still diffuse into Si to form PtSi till all the Pt₂Si is consumed. In this way we could see all the three phases: Pt, Pt₂Si and PtSi simultaneously.

4.1.2 Rutherford Backscattering Spectra

The RBS spectra shown in figures 4.1.2.1 through 4.1.2.3 are in good qualitative agreement with the AES depth profiles of the previous section regarding the silicide phase growth sequence. The spectra's plateaus corresponding to Pt, Pt₂Si and PtSi are distinctly visible. The surface energies for Pt and Si are well defined and the progressive increase in the Pt signal width as a function of annealing temperature and/or annealing time is clearly visible, indicating the increase in Pt silicide thickness.

Figure 4.1.2.1 shows the RBS spectra for samples annealed at 350° C for various RTP anneal times. After a 10 sec. anneal, 400 Å of Pt₂Si has been formed at the expense of Pt film. In a 20 sec. anneal, 720 Å of Pt₂Si has been formed at the expense of complete Pt film of about 500 Å. After a 40 sec. anneal, 320 Å of PtSi is formed at the expense of Pt₂Si film and after a 70 sec. anneal, 690 Å of PtSi is formed.

Figure 4.1.2.1: RBS spectra of Pt-Si structure annealed at 350°C for various RTP times, showing the silicide phase growth sequence from Pt to Pt₂Si (metastable phase) to PtSi (stable phase).

Figure 4.1.2.2: RBS spectra of Pt-Si structure annealed at 400°C for various RTP times, showing the silicide phase growth sequence from Pt to Pt₂Si (metastable phase) to PtSi (stable phase).

Figure 4.1.2.3: RBS spectra of Pt-Si structure annealed for 10 sec at various RTP temperatures, showing the silicide phase growth sequence from Pt to Pt_2Si (metastable phase) to PtSi (stable phase).

Fig. (4.1.3.1): SIMS impurity depth profile of two samples doped with $5\text{E}15 \text{ cm}^{-2}$ of As^+ at 50 KeV. One of the samples was deposited with $550 \pm 50 \text{ \AA}$ of Pt and annealed at 550°C for 10 sec. As^+ pile-up at PtSi/Si interface can be clearly seen.

The RBS spectra for samples annealed at 400° C for various RTP anneal times are shown in figure 4.1.2.2. After a 10 sec. anneal, all of the Pt film is converted to 700 Å of Pt₂Si and after 20 sec., all of the Pt₂Si is converted to 800 Å of stable PtSi. The silicide growth rate at 400° C anneal is twice as fast as at 350° C for similar anneal times which are in complete agreement with the AES results of preceding section.

The growth rate of PtSi at 500° C anneal is about two times faster than that at 400° C as demonstrated by the RBS spectra of figure 4.1.2.3 wherein spectra of Pt-Si reaction at 350° C, 400° C and 500° C are presented for constant anneal time of 10 sec. At 350° C, only part of the Pt film is converted to Pt₂Si. At 400° C, all the Pt is converted to Pt₂Si whereas at 500° C, all of the Pt film is converted to stable PtSi film.

The thickness-time dependence of Pt-Si reaction as derived from the RBS analyses will be discussed in chapter 5.

Using the theoretical atomic densities of silicon and platinum and the measured Pt and PtSi thicknesses, it was calculated that 1 Å of Pt reacts with 1.33 Å of Si to give approximately 1.9 Å of PtSi. This rate of Si consumption is about 75 percent of that for TiSi₂ formation and 65 percent of that for CoSi₂ formation.

4.1.3 Impurity Snowplowing Effect

The impurity depth profiles of two samples, one silicided and the other unsilicided, as measured by SIMS are presented in figure 4.1.3.1. Both samples were implanted with 5E15 cm⁻² of As⁺ @ 50 KeV and RTP annealed at 1050°C/30 sec in N₂ ambient to repair implant damage and activate the dopants. The silicided sample was made by depositing 550±50 Å of Pt and annealing at a RTP cycle of 550°C/10 sec in N₂ ambient to form PtSi. The silicided sample shows higher As⁺ concentration (about a factor of 2) at the PtSi-Si interface as compared to the unsilicided sample.

Fig. (4.1.3.2): SIMS impurity depth profile of two samples doped with $5E15$ cm⁻² of B⁺ at 10 KeV. One of the samples was deposited with 550 ± 50 Å of Pt and annealed at 550° C/10 sec. B⁺ pile-up at PtSi/Si interface can be clearly seen.

Fig. (4.1.3.3) SIMS impurity depth profile of two samples doped with $1E16$ cm⁻² of P⁺ at 30 KeV. One of the samples was deposited with 550 ± 50 Å of Pt and annealed at 550°C for 10 sec. P⁺ pile-up at PtSi/Si interface can be clearly seen.

Figure 4.1.3.2 gives the impurity depth profile of two samples implanted with $5 \times 10^{15} \text{ cm}^{-2}$ of B^+ @ 10 KeV. The implant damage anneal and activation was done under identical condition as for the case of As^+ . One of the two samples was also deposited with $550 \pm 50 \text{ \AA}$ of Pt and annealed at $550^\circ\text{C}/10 \text{ sec}$ RTP cycle to form PtSi. It is clearly seen that the concentration of B^+ at the PtSi-Si interface of the silicided sample is almost an order of magnitude higher when compared with the concentration at the same depth of the unsilicided sample.

Similarly, figure 4.1.3.3 gives the impurity depth profile of two samples implanted with P^+ @ 30 KeV. The implant damage and activation anneal, and silicidation was done under identical condition as for the As^+ case. P^+ also appeared to pile up at the PtSi-Si interface as seen by the higher P^+ concentration at the interface as compared to unsilicided sample. Some of P^+ is also seen to pile up at the silicide surface.

4.1.4 Transmission Electron Microscopy (TEM)

The TEM micrograph of the cross section of as-deposited Pt film and reacted at $350^\circ\text{C}/10 \text{ sec}$, $400^\circ\text{C}/10 \text{ sec}$ and $500^\circ\text{C}/10 \text{ sec}$ are presented in figures 4.1.4.1, 4.1.4.2, 4.1.4.3 and 4.1.4.4, respectively.

Pt was sputtered at 100 watts of power and 8 mTorr of Ar pressure. The sputtered Pt film has a columnar structure as seen in figure 4.1.4.1. The thin layer seen between Pt film and the substrate is probably amorphous silicon as the wafer was sputter etched before Pt deposition. The TEM micrograph in figure 4.1.4.2 is for sample annealed at a RTP cycle of $350^\circ\text{C}/10 \text{ sec}$. The bottom layer is of Pt_2Si and the top layer is of the unreacted Pt, which is in good agreement with AES and RBS analyses of sections 4.1.1.1 and 4.1.2.1. The sample annealed at 400°C for 10 sec has a double layer with Pt_2Si as the top layer and PtSi as the bottom layer as illustrated in the TEM micrograph of figure 4.1.4.3.

20 nm

Figure 4.1.4.1: TEM micrograph of the cross-section of a sputtered Pt film.

Figure 4.1.4.2: TEM micrograph of the cross-section of a sample annealed at a RTP cycle of 350°C/10 sec. The top layer is Pt whereas the bottom layer is Pt₂Si.

Figure 4.1.4.3: TEM micrograph of the cross-section of a sample annealed at a RTP cycle of 400°C/10 sec. The top layer is Pt_2Si whereas the bottom layer is PtSi.

Figure 4.1.4.4: TEM micrograph of the cross-section of a sample annealed at a RTP cycle of 500°C/10 sec.

The TEM cross section micrograph shown in figure 4.1.4.4 is of a fully silicided sample annealed at a RTP cycle of 500° C/10 sec. A single PtSi layer with columnar grain structure can be clearly seen.

4.2 Electrical Analysis

The sheet resistance of the silicides is one of the most important criteria for their suitability as a metallization agent in integrated circuit fabrication. Sheet resistance (R_{sh}) values were measured on four-point probe and plotted as a function of anneal temperature for a constant time and as a function of time for a constant temperature. As the non uniformity in the thickness of the as-deposited Pt film was of the order of 12-18%, all the sheet resistance values are normalized to an average sheet resistance of 3.5 Ω /sq., corresponding to 550 Å of Pt film.

4.2.1 PtSi sheet resistance on undoped wafers

Starting with a sheet resistance of 3.5 Ω /sq., it can be seen from figure (4.2.1.1a), that the R_{sh} varies from 1.6 to 3.2 Ω /sq., up to a temperature of 500° C for 10 sec. of anneal time, indicating transformation of as-deposited platinum film to the metastable phase of Pt₂Si. The R_{sh} value then converges to about 2.9 Ω /sq., at higher temperature or longer anneal times indicative of stable phase of PtSi. The sheet resistance then remains constant up to 550° C. A slight increase in R_{sh} is observed at 600° C, where upon the R_{sh} steadily goes down up to 900° C. The decrease at higher temperatures is due to the excessive grain growth of the PtSi. At 925° C, the R_{sh} increases very rapidly indicating initiation of the breakdown of PtSi film due to 'agglomeration', which is observed in very thin films. Agglomeration essentially refers to an irreversible change of thin films from a continuous state to a discontinuous island type of microstructure when subject to high temperature. This normally occurs at temperature above that of re-crystallization and grain growth.

Figure (4.2.1.1a): Sheet resistance of PtSi on undoped wafer as a function of RTP temperature, at constant annealing time of i) 10 sec., ii) 15 sec. and iii) 20 sec.

Figure (4.2.1.1b): Sheet resistance of Pt-Si on undoped wafer as a function of annealing time at constant RTP temperatures.

Figure (4.2.1.1b) gives a plot of R_{sh} as a function of time at constant temperature. It can be seen that the R_{sh} value does not converge to a stable value at 350° C even after very long anneal time indicating incomplete formation of a stable phase. This was confirmed by Auger analysis for the sample annealed for 70 sec as shown in figure 4.1.1.1. For all other cases the R_{sh} value converges to a stable value within 10-20 sec. of anneal time. The R_{sh} then remains fairly stable even after a prolonged anneal time of 120 sec.

4.2.2 PtSi sheet resistance on doped wafers

4.2.2.1 As⁺ doped wafers

The sheet resistance of the Pt-Si structure as function of temperature for fixed RTP anneal times of 10, 15 and 20 sec., formed on wafer doped with $5 \times 10^{15} \text{ cm}^{-2}$ of As⁺ at 50 KeV are shown in figures 4.2.2.1.1a. It can be seen from this figure that similar to the case of PtSi formed on an undoped wafer, here also the R_{sh} of Pt-Si reaction varies initially up to a temperature of 525° C and RTP anneal time of 10 sec. The R_{sh} value then converges to about 3.0 $\Omega/\text{sq.}$ at higher temperatures or longer RTP anneal times. The slightly higher temperature of 550° C (for an anneal time of 10 sec) required to stabilize the R_{sh} as compared to 500° C in the case of PtSi formed on undoped wafer may probably be due to the retardation of Pt diffusion by the heavy As⁺ concentration on the surface. Again a slight increase in R_{sh} at 600° C similar to one in the case of PtSi formed on undoped wafer is also seen here. This is due to the diffusion of Si at a temperature of 600° C through the grain boundaries of PtSi. PtSi film on As⁺ doped wafer is seen to breakdown at 900° C as indicated by the rapid rise in R_{sh} as compared to 925° C for the case of PtSi on undoped wafer.

The variation of R_{sh} as a function of time at constant RTP temperatures of 350° C- 600° C is plotted in figure 4.2.2.1.1b. It is seen that the R_{sh} value converges to a final value of

Figure (4.2.2.1.1a): R_{sh} of Pt-Si structure as a function of RTP temperatures for constant anneal times, on wafer implanted with $5E15 \text{ cm}^{-2}$ of As^+ at 50 keV and activated at $1050^\circ\text{C}/30 \text{ sec}$. The as-deposited Pt thickness was $550 \pm 50 \text{ \AA}$.

Figure (4.2.2.1.1b): R_{sh} of PtSi as a function of anneal times at constant RTP temperatures, on wafer implanted with $5E15 \text{ cm}^{-2}$ of As^+ at 50 keV and activated at $1050^\circ\text{C}/30 \text{ sec}$. The as-deposited Pt thickness was $550 \pm 50 \text{ \AA}$.

Figure (4.2.2.1.2a): R_{sh} of PtSi as a function of RTP temperature for a fixed annealing time of 10 sec, formed on wafer implanted with various As^+ doses and activated at $1050^\circ C/30$ sec. In all the cases, the starting Pt thickness was $550 \pm 50 \text{ \AA}$.

Figure (4.2.2.1.2b): R_{sh} of PtSi as a function of temperature for a fixed RTP anneal time of 10 sec., formed on wafer implanted with various As^+ doses. No implant and activation anneal was done. In all the cases, starting Pt thickness was $550 \pm 50 \text{ \AA}$.

3.0Ω/sq., at different times depending on RTP temperatures. For example it converges after 10 sec, at a RTP temperature of 550° C as compared to 80 sec at a RTP temperature of 350°C. This indicates that the stable phase at 550° C is formed in just 10 sec as compared to 80 sec at a RTP temperature of 350° C. However, in all the cases, once the stable PtSi phase is formed, the R_{sh} value remains fairly constant even after prolonged anneal time.

Figures (III.1.1a, 2a and 3a) in Appendix III give similar plots of R_{sh} as a function of temperature at constant anneal times of 10, 15 and 20 sec as well as a function of RTP anneal times at constant temperatures, for PtSi formed on wafer implanted with 4E16 cm⁻², 1E16 cm⁻² and 7E15 cm⁻² of As⁺ at 50 KeV. The trend in variation of R_{sh} as a function of temperature or as a function of time were very much similar to those shown above. However, as shown in figure 4.2.2.1.2a, the final sheet resistance of PtSi formed on highly doped wafer (4E16 cm⁻²) was observed to be 3.6Ω/sq., a 10-15% increase as compared to the final sheet resistance of PtSi formed on wafers doped with a dose of 1E16 cm⁻² or lower. This can be linked to high As⁺ concentration on the PtSi surface, formed on wafer doped with high dose of 4E16 cm⁻².

Figure 4.2.2.1.2b gives the R_{sh} of PtSi as a function of temperature for an RTP anneal time of 10 sec on wafers implanted with As⁺ at 50 KeV and with various doses. In this case, no implant damage and activation anneal was done. No noticeable deviation in R_{sh} was observed for doses lower than 4E16 cm⁻² of As⁺. The final R_{sh} in the case of sample implanted with a dose of 4E16 cm⁻² of As⁺ was observed to be 4.1 Ω/sq., as compared to 3.6 Ω/sq. on a similar sample but with an implant damage and activation anneal at a RTP cycle of 1050° C/30 sec. Additional figures are appended in Appendix III under figure numbers III.1.1b, III.1.2b and III.1.3b for other As⁺ doses.

This higher R_{sh} might be due to higher As⁺ surface concentration on the sample which was not subjected to implant anneal. Unlike TiSi₂ [18], where the silicidation reaction is completely inhibited if the underlying silicon film is implanted with 1E16 cm⁻² of As⁺, we

notice that the formation of PtSi is not hindered on wafers implanted with doses as high as $4\text{E}16\text{ cm}^{-2}$ of As^+ .

4.2.2.2 P^+ doped wafers

The sheet resistance of PtSi versus annealing temperature for constant annealing time of 10, 15 and 20 sec., is depicted in figure (4.2.2.2.1a) for a phosphorus (P^+) dose of $1\text{E}16\text{ cm}^{-2}$ @ 30 KeV. The sheet resistance is seen to stabilize at $3.35\text{ }\Omega/\text{sq.}$ for an anneal cycle of $550^\circ\text{ C}/10\text{ sec.}$, or at lower temperature for longer anneal time. The R_{sh} then keeps increasing slowly upto a temperature of about 700° C . This may be due to diffusion of P^+ into the Si thereby reducing the interface concentration of P^+ . The R_{sh} value is seen to drop off quickly to about $2.7\text{ }\Omega/\text{sq.}$ at 800° C indicating an excessive grain growth. The film is seen to break up at about 900° C as evidenced by rapid increase in R_{sh} . There is no difference observed in the characteristics of PtSi formed on other P^+ doped Si with doses of $2\text{E}16\text{ cm}^{-2}$ and $7\text{E}15\text{ cm}^{-2}$ at 30 KeV as can be seen in figures III.2.1a and III.2.2a respectively of Appendix III.

Figure 4.2.2.2.1b gives the R_{sh} of PtSi formed on P^+ doped Si as a function of annealing time at constant temperatures ranging from 350° C to 600° C for a P^+ dose of $1\text{E}16\text{ cm}^{-2}$ at 30 KeV. Once the PtSi formation is completed, the sheet resistance remains constant even after prolonged annealing time of up to 100 sec. which is similar to the case of PtSi formation on undoped wafer.

Similar response was noticed for R_{sh} of PtSi formed on Si with P^+ doses of $1\text{E}16\text{ cm}^{-2}$ and $7\text{E}15\text{ cm}^{-2}$ at 30 KeV as shown in Appendix III under figure numbers III.2.1b and III.2.2b respectively.

Figure 4.2.2.2.2a gives the R_{sh} of PtSi as a function of temperature for a RTP anneal time of 10 sec on wafers implanted with P^+ at 30 KeV and with various doses. Implant damage and activation anneal was done at an RTP cycle of $1050^\circ\text{ C}/30\text{ sec.}$ It is observed from this

Figure (4.2.2.2.1a): R_{sh} of Pt-Si structure as a function RTP temperature for constant annealing times, on wafer implanted with $1E16 \text{ cm}^{-2}$ of P^+ at 30 keV and activated at $1050^\circ \text{C}/30 \text{ sec}$. The as-deposited Pt thickness was $550 \pm 50 \text{ \AA}$.

Figure (4.2.2.2.1b): R_{sh} as a function of anneal times at constant RTP temperature, on wafer implanted with $1E16 \text{ cm}^{-2}$ of P^+ at 30 keV and activated at $1050^\circ \text{C}/30 \text{ sec}$. The as-deposited Pt thickness was $550 \pm 50 \text{ \AA}$.

Figure (4.2.2.2a): R_{sh} of PtSi as a function of RTP temperature for a fixed annealing time of 10 sec, formed on wafer implanted with various P^+ doses and activated at $1050^\circ\text{C}/30\text{ sec}$. In all cases the starting Pt thickness was $550 \pm 50 \text{ \AA}$.

Figure (4.2.2.2b): R_{sh} of PtSi as a function of RTP temperature for a fixed annealing time of 10 sec, formed on wafer implanted with various P^+ doses. No implant and activation anneal was done. In all case the starting Pt thickness was $550 \pm 50 \text{ \AA}$.

figure that the final R_{sh} of PtSi formed on a wafer doped with $2E16 \text{ cm}^{-2}$ of P^+ is slightly higher than that of R_{sh} of PtSi formed on lower P^+ doses of $1E16 \text{ cm}^{-2}$ and $7E15 \text{ cm}^{-2}$. This can be linked to higher P^+ concentration on PtSi surface.

Figure 4.2.2.2b gives the R_{sh} of PtSi as a function of temperature for an RTP anneal time of 10 sec on wafers implanted with P^+ at 30 KeV and with various doses. No implant damage and activation anneal was done. It is observed from this figure that the final value of R_{sh} of PtSi increases with the implanted dose. Also, in all these cases when no implant activation anneal was done, the R_{sh} of PtSi was higher than those of PtSi formed on similar implanted dose of P^+ but subjected to implant damage and activation anneal prior to Pt deposition. We have seen before, that during PtSi formation on P^+ doped wafers, some of the P^+ also piles up at the silicide surface. Therefore, these higher R_{sh} might be due to increasing P^+ surface concentration with higher implant doses. Also, the surface concentration will be higher in unannealed sample as compared to samples where implant damage and activation anneal was done.

4.2.2.3 B^+ doped wafers

The sheet resistance of Pt-Si structure as a result of 10, 15 and 20 sec annealing at various temperatures is illustrated in figure (4.2.2.3.1a) for a boron (B^+) dose of $5E15 \text{ cm}^{-2}$ at 10 KeV. Once the PtSi formation is complete, the R_{sh} stabilizes at a value of $2.92 \Omega/\text{sq.}$ for an anneal cycle of $550^\circ \text{C}/10 \text{ sec.}$ or at lower temperature for longer anneal time. The R_{sh} then keeps decreasing slowly up to a temperature of about 875°C indicating the process of grain growth. The rapid increase in R_{sh} at 900°C indicates the PtSi film breakdown due to agglomeration, as explained earlier. There is no difference observed in the characteristics of PtSi formed on other B^+ doped Si with doses of $3E15 \text{ cm}^{-2}$ and $7E15 \text{ cm}^{-2}$ except the value of R_{sh} on formation of stable phase of PtSi as can be seen in figures III.3.1a and III.3.2a respectively of Appendix III.

Figure (4.2.2.3.1a): R_{sh} of Pt-Si structure as a function temperatures for constant RTP anneal times, on wafer implanted with $3E15 \text{ cm}^{-2}$ of B^+ at 10 keV and activated at $1050^\circ\text{C}/30 \text{ sec}$. The as-deposited Pt thickness was $550 \pm 50 \text{ \AA}$.

Figure (4.2.2.3.1b): R_{sh} as a function of anneal times at constant RTP temperatures, on wafer implanted with $5E15 \text{ cm}^{-2}$ of B^+ at 10 keV and activated at $1050^\circ\text{C}/30 \text{ sec}$. The as deposited Pt thickness was $550 \pm 50 \text{ \AA}$.

Figure (4.2.2.3.2a): R_{sh} of PtSi as a function of temperature for a fixed RTP anneal time of 10 sec, formed on wafer implanted with various B^+ doses and activated at $1050^\circ\text{C}/30$ sec. In all cases the starting Pt thickness was $550 \pm 50 \text{ \AA}$.

Figure (4.2.2): Sheet resistance of PtSi as a function of As^+ , B^+ and P^+ doses. As^+ was implanted at 50, B^+ at 10 and P^+ at 30 KeV. Implant activation cycle was $1050^\circ\text{C}/30$ sec and PtSi was formed at a RTP cycle of $550^\circ\text{C}/10$ sec in all the cases.

Figure 4.2.2.3.1b gives the R_{sh} of PtSi formed on B⁺ doped Si as a function of annealing time at constant temperatures ranging from 350° C to 600° C for a dose of 5E15 cm⁻² at 10 KeV. Once the PtSi formation is completed, the R_{sh} remains fairly constant even after prolonged annealing time of up to 100 sec., which is similar to the case of PtSi formation on undoped wafer.

Similar response was noticed for R_{sh} of PtSi formed on Si with B⁺ doses of 5E15 cm⁻² and 7E15 cm⁻² at 10 KeV as shown in Appendix III under figure numbers III.3.1b and III.3.2b, respectively.

R_{sh} of PtSi as a function of temperature for an RTP anneal time of 10 sec., on various samples, is plotted in figure 4.2.2.3.2a. The wafers were implanted with different doses of B⁺ at 10 KeV and annealed at a RTP cycle of 1050° C/30 sec. before PtSi formation. Here also, we see that the R_{sh} of PtSi is an increasing function of implant dose. This suggests an increasing surface concentration of B⁺ with increasing implant dose..

The variation of R_{sh} of PtSi as a function of As⁺, B⁺ and P⁺ impurity doses is illustrated in figure (4.2.2). In all the cases, the implant activation anneal was done at an RTP cycle of 1050° C/30 sec. The as-deposited Pt thickness was 550±50 Å and the RTP reaction cycle was 550° C/10 sec. The R_{sh} of PtSi is seen to increase as the implantation dose increases for all three cases of impurities. This is due to increasing impurity concentration, with the increasing dose, at the PtSi surface. It is also observed from this figure that the R_{sh} of PtSi on As⁺ doped wafer is relatively higher compared to R_{sh} of PtSi on P⁺, which is higher compared to R_{sh} of PtSi on B⁺ doped wafer. Hence, higher the atomic mass of the specie, higher the sheet resistance for identical dose.

4.2.3 Contact Resistance

The test vehicles used for evaluating the contact resistance of PtSi to silicon (n⁺ or p⁺) are those of a four terminal Kelvin structure and contact chain having 98 contacts in series.

Unfortunately, some of the contacts on contact chain were not opened after the contact window etching step. Consequently, the contact chain structures were abandoned. Therefore, the results presented here are those extracted from four terminal Kelvin structures. One of such structure is shown in Appendix I. The structure contains four terminals, two of which (diagonally opposite) are used for forcing current through the contacts and the other two for sensing the voltage across the silicide-silicon interface and the underlying shallow junction. HP 4145 semiconductor parameter analyzer was used for this purpose. A current of -2 mA to +2 mA was used while simultaneously measuring the voltage, to eliminate the effect of rectifying junction in case there exists one. Likewise, in order to compensate for the misalignment errors of the contact window, the measurements were repeated with the current and the potential sensing probes interchanged [37]. The contact resistance was extracted from the slope of the I-V curve at zero current. The specific contact resistivity ' ρ_c ' was then evaluated as

$$\rho_c = A \times \text{Slope} \quad (4.2.3)$$

where A denotes the contact area.

It is worth noting that the Kelvin method enables an accurate measurement of contact resistance as it involves only one contact. The contact resistance thus measured though, also contains the contribution from the junction underneath the contact. This would not however, affect our contact resistance comparison as this contribution will be common to all the technologies. The contact window was made to completely overlap the diffusion area to ensure that the extracted contact resistivity is a true representation of the actual contact resistivity of the contact [37]. Contacts to n⁺ silicon, p⁺ silicon, n⁺ and p⁺ polysilicon were evaluated. The effect of the dopant implantation dose was also studied.

Figure 4.2.3.1 shows the measured contact resistances (R_{co}) of Al-PtSi and that of Al to p⁺ diffused region in Si. In each case, measurements were made on approximately 40 identically fabricated test elements on two wafers. It is seen that the contact resistance of Al-PtSi to p⁺ diffusion is about an order of magnitude lower than that of Al to p⁺ diffused Si. R_{co} is also seen to vary inversely to the contact area.

The bar graph of figure 4.2.3.2 gives the comparison between R_{co} of Al-PtSi and that of Al to n⁺ diffused Si. The Al-PtSi contact resistance is about 40-50 percent lower as compared to that of Al to n⁺ diffused Si. Again R_{co} is seen to vary inversely as the contact area.

The average specific contact resistivity of Al-PtSi system to p⁺ diffused Si was calculated to be $3.0 \times 10^{-7} \Omega\text{-cm}^2$ as compared to $1.0 \times 10^{-6} \Omega\text{-cm}^2$ for Al to p⁺ diffused Si. The average specific contact resistivity of Al-PtSi contacts to n⁺ diffused Si was observed to be $6.0 \times 10^{-7} \Omega\text{-cm}^2$ as compared to $1.0 \times 10^{-6} \Omega\text{-cm}^2$ for Al contacts to n⁺ diffused Si.

Figure 4.2.3.3 gives the R_{co} of Al-PtSi contacts to p⁺ diffused Si and that of Al-PtSi contacts to n⁺ diffused Si. The R_{co} of Al-PtSi contacts to p⁺ diffused region is lower than that of Al-PtSi contacts to n⁺ diffused region. This is due to the lower barrier height of 0.25 eV for the earlier structure as compared to 0.87 eV for the latter structure.

The contact resistances of Al-PtSi to p⁺ diffused region in Si and that of Al-PtSi to n⁺ Si as a function of implant dose of B⁺ and As⁺ are listed in Table 4.2.3.1. As can be seen from the Table 4.2.3.1 that in case of B⁺, starting with a dose of $1.0 \times 10^{15} \text{ cm}^{-2}$, the contact resistance R_{co} decreases upto a dose of $3 \times 10^{15} \text{ cm}^{-2}$. Any further increase in B⁺ dose does not seem to affect the contact resistance. What this means is that at a dose of $3 \times 10^{15} \text{ cm}^{-2}$, the B⁺ concentration at the PtSi/Si interface after silicide formation has reached its solid solubility limit in Si. Any higher dose implant than this would result in out diffusion of B⁺ to the silicide and consequently evaporate from the silicide surface. This can be investigated by SIMS analysis of a sample implanted with B⁺ at a dose of $3 \times 10^{15} \text{ cm}^{-2}$ prior

Fig.(4.2.3.1): Contact resistance versus contact area for Al-PtSi-p⁺ Si and Al-p⁺ Si contacts. The B⁺ dose was 5E15 cm⁻² at 20 KeV and the implant activation cycle was 1050°C/30 sec. The as-deposited Pt thickness was 550±50 Å and the silicidation RTP anneal cycle was 550°C/10s.

Fig. (4.2.3.2) Contact resistance versus contact area for Al-PtSi - n⁺ Si and Al-n⁺ Si contacts. The As⁺ dose was 5E15 cm⁻² at 50 KeV and the implant activation cycle was 1050°C/30 sec. The as-deposited Pt thickness was 550±50 Å and the silicidation RTP anneal cycle was 550°C/10 sec.

to silicide formation. SIMS impurity profile of a silicided sample which was implanted with $5 \times 10^{15} \text{ cm}^{-2}$ of B^+ prior to silicide formation (refer figure 4.1.3.2), shows that the B^+ concentration has reached to about $8 \times 10^{20} \text{ cm}^{-3}$ at the PtSi/Si which is about the limit of boron solubility in Si. The integrated dopant concentration after PtSi formation has also decreased (Table 5.2.1) after silicide formation which indicates that once the B^+ concentration at the PtSi/Si interface reaches the solid solubility limit, the excess B^+ will diffuse to the PtSi surface from where it out diffuses.

For the case of Al-PtSi to n^+ diffused Si, it is seen from the Table 4.2.3.1 that the contact resistance (R_{co}) does not seem to saturate even at higher As^+ dose of $5 \times 10^{15} \text{ cm}^{-2}$. This can be understood in terms of solid solubility limit of As in Si. Since the solid solubility limit of As^+ in Si is much higher than that of B^+ , the PtSi/Si interface concentration does not reach the solid solubility limit of As^+ in Si. As a result, the contact resistance steadily decreases from an As^+ implant dose of $3.0 \times 10^{15} \text{ cm}^{-2}$ to $7.0 \times 10^{15} \text{ cm}^{-2}$. This would also partly explain the limited difference of about 50 percent, between the contact resistance of Al-PtSi to n^+ and p^+ Si for similar doses of As^+ and B^+ , despite the much higher difference in barrier height of the two structures.

Figure 4.2.3.4 shows the result of measured contact resistances (R_{co}) of Al-PtSi and that of Al to p^+ poly-Si. No appreciable difference has been observed in the contact resistance of Al-PtSi to p^+ diffusion and that of Al to p^+ diffused Si. R_{co} is seen to vary inversely to the contact area.

The contact resistances of Al-PtSi to p^+ and n^+ poly-Si as a function of implant dose of B^+ and As^+ are summerized in Table 4.2.3.2. Unlike the earlier case of PtSi contacts to diffused Si region, here the contact resistance is steadily decreasing with implant dose in the case of contacts to p^+ polysilicon. In the case of contacts to n^+ polysilicon, it is difficult to comment on the trend of variation of R_{co} due to non availability of data for As^+ dose of

Fig.(4.2.3.3) Comparison between contact resistances of Al-PtSi - p⁺ Si and Al -PtSi to n⁺ Si contacts. The B⁺ dose was 5E15 cm⁻² at 20 KeV and the As⁺ dose was 5E15 cm⁻² at 50 KeV. The implant activation cycle was 1050°C/30 sec.

Table 4.2.3.1: Al-PtSi to Si Contact resistance as a function of implant dose and contact window size.

Contact Size (μm^2)	B ⁺ dose at 20 KeV (cm ⁻²)			As ⁺ dose at 50 KeV (cm ⁻²)		
	1.0 E15	3.0 E15	5.0 E15	3.0 E15	5.0 E15	7.0 E15
6.3	6.6	4.38	4.16	18	9.53	8.36
9.4	2.58	1.75	1.55	10.9	5.05	1.21
14.1	1.46	1.25	1.20	7.75	4.88	1.12
18.8	1.32	1.21	1.25	7.25	3.01	0.6
25.0	1.20	1.13	1.12	5.75	2.89	0.56
R _{sh} ($\Omega/\text{sq.}$)	106	40.7	31.5	70	50	45

Figure (4.2.3.4): Contact resistance of Al-PtSi and Al to p⁺ polysilicon as a function of contact area. The B⁺ dose was 5E15 cm⁻² at 20 KeV and the implant activation cycle was 1050°C/30 sec. The as-deposited Pt thickness was 550±50 Å and the RTP anneal cycle was 550°C/10 sec.

Table 4.2.3.2: Al-PtSi to poly Si Contact resistance as a function of implant dose and contact window size.

Contact Size (μm^2)	B ⁺ dose at 20 KeV (cm ⁻²)			As ⁺ dose at 50 KeV (cm ⁻²)		
	1.0 E15	3.0 E15	5.0 E15	3.0 E15	5.0 E15	7.0 E15
6.3	N.A.	N.A.	N.A.	40	N.A.	5.87
9.4	45.27	N.A.	N.A.	19.5	N.A.	N.A.
12.5	35.28	2.5	N.A.	14.5	N.A.	2.75
14.1	34.26	3.8	1.4	17	N.A.	2.48
25.0	19.71	7.88	3.64	N.A.	N.A.	N.A.
R _{sh} ($\Omega/\text{sq.}$)	562	126	70	350	199	128

N.A.: Not available due to difficulties in opening the contact windows.

5E15 cm⁻². This data was not available due to either the contact windows not being opened properly before Pt deposition or due to presence of oxide between PtSi and Al films.

4.3 Devices

To study the PtSi Schottky barrier diode and p-n junctions, the I-V characteristics were recorded from 0-0.7 volts for forward characteristics. The forward I-V characteristics were plotted on semilog scale (ln J vs. V) from which the gradient of the linear region was calculated to deduce the 'ideality factor' of the diode. The gradient line was extrapolated to intercept the current axis to get the 'saturation leakage current'. The reverse characteristics were also plotted on semilog scale from 0 to -6 volts. The current were normalized to per unit area in cm². The currents at a reverse bias of 5 volts were recorded in terms of $\mu\text{A}/\text{cm}^2$ to compare with published results.

From the experimental data, the ideality factors for the Schottky barriers and PN junctions were calculated. The ideality factor of a Schottky barrier 'n' is given by

$$n = \left(\frac{q}{kT} \right) \left(\frac{\partial V}{\partial (\ln J)} \right) \quad (4.3.1)$$

where q is the electron charge (1.61 E-19 Coulomb), k is the Boltzmann's constant and T is the ambient temperature in K. ($\partial V / \partial (\ln J)$) is the inverse of the slope of the linear portion of the forward I-V characteristic of the diode drawn on semilog scale.

The effective barrier height ' Φ_b ' is given by

$$\Phi_b = \left(\frac{kT}{q} \right) \ln \left(A A^* \frac{T^2}{J_0} \right) \quad (4.3.2)$$

where, A is the area of the diode, A^* is the Richardson's constant ($\sim 20 \text{ A/K}^2\text{.cm}^2$) and J_0 is the saturation leakage current deduced by extrapolating the slope line to intercept the current axis of the forward I-V characteristics of the diode drawn on semilog scale.

The saturation leakage current, the reverse-biased leakage current at -5 volts were calculated in terms of current / cm^2 . All the tests were carried out at ambient temperature of 27°C . These tests were conducted only on two wafers. The devices on all the (refer Appendix II) remaining wafers were misprocessed, and therefore their results are not included here.

4.3.1 Schottky barrier diodes

Table 4.3.1 gives the experimental results of ideality factor, saturation leakage current, reverse bias leakage current at -5 volts and effective barrier height measured from Schottky diodes of various sizes. The results presented here are both for diodes with and without p^+ guard ring. The results are averaged over 35 devices from each category.

As seen from Table 4.3.1, the ideality factor for diodes with p^+ guard ring is in the range of 1.04-1.06, whereas the ideality factor of diodes without p^+ guard ring is in the range of 1.08-1.11. This mean the performance of PtSi to n^- Si Schottky diodes fabricated with p^+ guard ring are very close to ideal. The saturation leakage current and reverse current at -5 volts for Schottky diodes without p^+ guard ring is about three to six times higher than those of diodes with p^+ guard ring. This is due to the high electric field at the periphery of the diodes without p^+ guard ring as shown in figure 4.3.1.1. The p^+ guard ring structure reduces this edge effect in order to obtain an ideal I-V characteristics. This is the reason the ideality factor is close to unity for diodes with p^+ guard ring as compared to diodes without p^+ guard ring.

The Φ_b shown in the Table is the effective barrier height deduced from the saturation leakage current using equation 4.3.2. The barrier height of PtSi to n^- Si is 0.87 eV. The

Table 4.3.1: Ideality factor, saturation leakage current ($\mu\text{A}/\text{cm}^2$), current at reverse bias of -5 volts ($\mu\text{A}/\text{cm}^2$) and effective barrier height of Schottky barrier diodes.

Area (μm^2)	With p ⁺ guard ring				Without p ⁺ guard ring			
	n	I _s ($\mu\text{A}/\text{cm}^2$)	I _r @ -5 volts ($\mu\text{A}/\text{cm}^2$)	ϕ_b (eV)	n	I _s ($\mu\text{A}/\text{cm}^2$)	I _r @ -5 volts ($\mu\text{A}/\text{cm}^2$)	ϕ_b (eV)
625	1.04	0.939	3.20	0.80	1.09	2.945	20.07	0.78
976.6	1.05	1.06	3.69	0.80	1.11	3.26	13.82	0.77
1406.3	1.06	1.01	4.69	0.80	1.09	2.9	8.46	0.78
2500	1.06	1.32	4.84	0.79	1.08	2.4	8.8	0.78

Figure 4.3.1.1: Schottky diode structures, (a) without p⁺ guard ring and (b) with p⁺ guard ring.

Figure 4.3.1.2: I-V characteristics of a typical Schottky barrier diode with p^+ guard ring. The area of the diode was $2500 \mu\text{m}^2$. I_E is in mA/cm².

Figure 4.3.1.3: I-V characteristic of a typical Schottky barrier diode without p^+ guard ring. The area of the diode was $2500 \mu\text{m}^2$. I_E is in mA/cm².

lower effective barrier height stems from image-force lowering of the barrier height and perhaps to some extent, due to the snow-plowing effect of the PtSi at the PtSi/Si interface.

The I-V characteristics of $2500\text{ }\mu\text{m}^2$ typical PtSi Schottky barrier diodes with and without p^+ guard ring are presented in figures 4.3.1.2 and 4.3.1.3, respectively. The voltage was varied from -6 volts to 0.8 volts to cover both operation regimes of the Schottky diode. I_E represents current per cm^2 of the diode area. The reverse bias leakage current at -5 volts in case of diodes without p^+ guard ring is about three times higher than that of diodes with p^+ guard ring.

4.3.2 p-n junctions

The ideality factor, saturation leakage and reverse bias leakage are tabulated in Table 4.3.2 for both area and edge intensive diodes. It can be seen from Table 4.3.2 that ideality factor of PtSi area intensive diode is very close to unity. Thus the behavior of PtSi p-n junctions are closed to that of an ideal diode. The saturation leakage current and the current at reverse bias is an increasing function of the area of the diode. For edge intensive diode, the currents are about a order of magnitude higher than those of area intensive diodes. This is due to the concentration of high electric field at the diode edges and consequently higher leakage.

The I-V characteristics of $140625\text{ }\mu\text{m}^2$ typical p^+n diode is presented in figures 4.3.2.1. The voltage was varied from -6 volts to 0.8 volts to cover both the operation regimes of the diode. I_E represents current per cm^2 of the diode area. The low reverse leakage current/ cm^2 at -5 volts can be witnessed.

When we compare the I-V characteristics of a typical Schottky barrier diode of figure 4.3.1.1 with that of a typical p^+n junction in figure 4.3.2.1, we notice that the forward current of a Schottky barrier is about an order of magnitude higher than that of p^+n junction

TABLE 4.3.2: Ideality factor, saturation leakage current and current at reverse bias of 5 volts for p+n diodes.

Area Intensive				Edge Intensive			
Area	n	Is	Ir @ -5	Area	n	Is	Ir @ -5
(μm^2)		(pA/cm ²)	(nA/cm ²)	(μm^2)		(pA/cm ²)	(nA/cm ²)
35156	1.01	48.2	22.7	9687.5	1.02	261	123
62500	1.01	53.3	28	—	—	—	—
140625	1.01	62.2	31.3	—	—	—	—

Figure 4.3.2.1: I-V characteristic of a typical p+n junction. The area of the diode was 2500 μm^2 . I_E is in mA/cm².

for the same voltage. This is because the Schottky barrier diode is a majority-carrier current device whereas a p-n junction is a minority-carrier current device. Consequently, the forward voltage drop will be much less in a Schottky barrier diode than that in a PN junction for the same current. The breakdown voltage of PtSi Schottky barrier diode and that of p⁺n junctions fabricated were in the range of 80-90 volts.

4.3.3 Salicided NMOS Transistors

To evaluate the effect of Pt salicide on MOS transistors, NMOS transistors which were both, short and wide and short and narrow were fabricated. The sizes are listed in Appendix I. The Carleton NMOS process flow is presented in Appendix II. The device

TABLE 4.3.3: Salicided NMOS Matrix.

Wafer No.	as-deposited Pt (Å)	PtSi formed (Å)
F-92-01	Control wafer without PtSi	
F-92-05	255±20	500±40
F-92-06	400±40	780±80
F-92-07	450±45	870±90

were silicided self aligned to gate and S/D region after gate and S/D patterning. No side-wall spacers were used. As the gate oxide thickness used in the process was 500 Å, three different thicknesses of the silicide were formed as tabulated in Table 4.3.3. This strategy was deliberately used to study PtSi formation on gate and S/D areas of NMOS without side-wall spacer technology.

It was noticed from the electrical characterization that the gate and S/D regions on NMOS transistors of wafer numbers F-92-06 and F-92-07 were shorted due to thick PtSi formation. Hence the result presented here are from wafer number F-92-05, which had only 500 ± 40 Å of PtSi formed. The normal silicide thickness used in other technologies is about 1000 Å.

Figure 4.3.3.1 gives the I_D - V_{DS} characteristics for V_{GS} from 0 - 5 volts of an NMOS transistor with a ratio of $L/W = 10 \mu\text{m}/75 \mu\text{m}$. I_D - V_{DS} characteristics of a similar transistor which was silicided is presented in figure 4.3.3.2. I_D plotted is per micron width of the channel of the transistor in either case. These characteristics indicate no bridges formed between gate and S/D regions. It is also seen from these two plots that the current level for silicided NMOS is about 10 percent higher than that of the wafer which was not silicided. Thus the decrease in the contact and diffusion area resistance has resulted in an increased current drive of the silicided transistor.

Figure 4.3.3.3-4 give similar I_D - V_{DS} characteristics of an NMOS transistor with $L/W = 5 \mu\text{m}/75 \mu\text{m}$ from an unsilicided and silicided wafer, respectively. Here also the current level of silicided transistor is about 12 percent higher than that of unsilicided wafer. As I_D is an inverse function of channel length, the drain current in figure 4.3.3.4 must therefore, be two times higher than that in figure 4.3.3.2. As the junction depth is constant for both the devices and the fact that short channel effects do not scale linearly with the channel length, we see that I_D do not scale linearly with the channel length. As the short channel effect is a larger more dominant in $5 \mu\text{m}$ transistor than in $10 \mu\text{m}$, a higher I_D than expected theoretically, is obtained in $5 \mu\text{m}$ NMOS transistor.

Figure 4.3.3.1: I_D - V_{DS} characteristic of a typical unsilicided NMOS transistor with $L/W = 10 \mu\text{m}/75 \mu\text{m}$. I_D shown is in per micron width of the channel.

Figure 4.3.3.2: I_D - V_{DS} characteristic of a typical salicided NMOS transistor with $L/W = 10 \mu\text{m}/75 \mu\text{m}$. I_D shown is in per micron width of the channel.

Figure 4.3.3.3: I_D - V_{DS} characteristic of a typical unsilicided NMOS transistor with $L/W = 5 \mu\text{m}/75 \mu\text{m}$. I_D shown is in per micron width of the channel.

Figure 4.3.3.4: I_D - V_{DS} characteristic of a typical silicided NMOS transistor with $L/W = 5 \mu\text{m}/75 \mu\text{m}$. I_D shown is in per micron width of the channel.

CHAPTER 5

Discussion

5.1 PtSi Metallurgy

From the AES and RBS analyses, it is revealed that under clean platinum deposition and annealing conditions, the silicidation reaction starts at the interface. Initially platinum diffuses to the interface to react with underlying silicon to form a metastable phase of platinum silicide (Pt_2Si) until all the platinum is consumed. The formation of the stable phase of platinum silicide (PtSi) then starts at the interface at higher temperatures or prolonged anneal times till all the Pt_2Si is converted to PtSi . The phase growth sequence of Pt-Si reaction can be summarized as:

It can also be seen that at any given time during the growth reaction, a maximum two out of three phases of Pt, Pt_2Si and PtSi are present. This is in contrast to PtSi formation in furnace anneal, where all the three phases have been observed to co-exist [35]. However, the contamination in the as-deposited film or in the annealing ambient can not only change the co-existence of different phases, as demonstrated earlier in figure (4.1.1.3), but also completely inhibit the silicide formation even at much higher temperatures and/or prolonged anneal times [8].

The starting sheet resistance of 550 Å of as-deposited Pt film was 3.5Ω/sq. The final sheet resistance of the stable phase of platinum silicide (PtSi) was 3.08Ω/sq., for a thickness of about 1050 Å of PtSi. This gives a resistivity of 33 μΩ-cm. In PtSi formation, 1 Å of Pt film reacts with 1.33 Å of Si to give approximately 1.9 Å of PtSi film.

The R_{sh} value is unstable in the initial period of reaction, indicative of metastable phase formation of Pt_2Si . Once the stable phase of PtSi is formed, the R_{sh} value stabilizes at the above referred value. The R_{sh} value of PtSi was observed to be stable up to a temperature of 900° C for undoped wafers when the R_{sh} increases rapidly due to breakdown of the silicide film. For wafer doped with As^+ , B^+ , the R_{sh} value goes steadily down even after silicide formation is complete. This might be due to continuous grain growth of PtSi. On the other hand, for the wafers doped with P^+ , after the silicide formation, the R_{sh} steadily increases up to a temperature of 700°C and then rapidly falls off to a minimum value at about 875°C. The increase in R_{sh} after silicide formation might be due to diffusion of the P^+ either into bulk of the silicon or into the silicide from the PtSi-Si interface. The reduction in R_{sh} at temperatures beyond 700°C might be due to grain growth of the PtSi which more than compensates for the increase in R_{sh} due to decrease in the impurity concentration at the PtSi-Si interface. The quantity of implant dose or the implant energy did not appear to have any effect on the temperature stability of these films unlike for the

2 of/de 2

MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS
STANDARD REFERENCE MATERIAL 1010a
(ANSI and ISO TEST CHART No. 2)

case of TiSi_2 , where high surface impurity concentration of Si completely inhibits the silicide formation .

A thin silicon oxide is invariably formed on the PtSi. The thickness of this oxide varies directly with the anneal time and temperature. The simultaneous formation of this surface oxide is beneficial for pattern generation. The wet etch selectivity of unreacted platinum to PtSi with surface oxide in 50% Aqua regia was found to be in excess of 5:1.

The PtSi formation and its phase growth sequence mentioned above applies to clean platinum deposition and annealing conditions. Any presence of native oxide on the silicon surface before Pt deposition will completely inhibit the PtSi formation even at higher temperatures and/or prolonged anneal times as Pt does not reduce the native oxide. On the other hand, if any contamination such as oxygen is present in the annealing ambient, full silicidation of the available Pt will not be realized. In this case, initially, the reaction will start at the Pt-Si interface, with the Pt diffusing into silicon to form Pt_2Si . In the mean time oxygen will diffuse from annealing ambient into Pt film and proceed towards the Pt-Si interface. The moment the oxygen front meets the Pt-Si interface, Pt diffusion will cease. This will impede further reaction to form Pt_2Si . However, the reaction will still proceed at the Pt_2Si -Si interface, to form the stable phase of PtSi. Hence, under these circumstances, all the three phases of Pt, Pt_2Si and PtSi could be simultaneously occurring, as shown in AES spectra of figure (4.1.1.4) and TEM micrograph of figure (4.1.1.4).

The thicknesses of PtSi formed at different temperatures and times are listed in Table 5.1.1. The growth of the PtSi thickness is plotted as a function of the square root of the annealing time ($\sqrt{t}$) for annealing temperatures of 350° C and 400° C in figure (5.1.1). A parabolic time dependence is observed. So the growth of PtSi can be expressed as

$$L = \sqrt{Dt} \quad \text{for } t > t_1 \quad (5.1.2)$$

Figure (5.1.1): Plot of PtSi thickness growth versus $\sqrt{\text{annealing time}}$ at 350°C and 400°C in RTP.

Figure (5.1.2): Plot of Pt diffusivity at 350°C and 400°C versus reciprocal of temperature

TABLE 5.1.1: PtSi thickness formed as a function of temperature and time, calculated from RBS analyses.

RTP Cycle (°C/sec.)	PtSi Thickness formed (Å)	RTP Cycle (°C/sec.)	PtSi Thickness formed (Å)
350/20	0	400/10	0
350/40	450	400/15	770
350/70	650	400/20	930

where L is the thickness of PtSi formed in cm., t is the annealing time in sec., D is the diffusivity of Pt through Pt_2Si during PtSi formation, and t_1 is the time required to complete the Pt_2Si formation as the formation of PtSi does not begin until all the Pt is converted to Pt_2Si .

The diffusivity of Pt is calculated from the slope of the thickness- $\sqrt{\text{time}}$ dependence plot in figure (5.1.1). The diffusivities as calculated are $3.394E^{-12}$ and $5.118E^{-11}$ $\text{cm}^2/\text{sec.}$ at 350°C and 400°C , respectively. These values of D obtained are an order of magnitude higher than those reported in the literature for furnace anneal [1-5]. Figure (5.1.2) shows the natural logarithm of the diffusivities at 350°C and 400°C plotted as a function of the reciprocal of RTA temperature in $^\circ\text{K}$. The RTA temperature stability was very poor for temperatures below 350°C . On the other hand, the diffusion of Pt being high at 450°C , it was difficult to extract the diffusivity of Pt at 450°C . Therefore, only two data points are used to represent a straight line. Assuming the growth of the PtSi follows the Arrhenious relationship of the form

$$D(T) = D_o \exp\left(\frac{-E_a}{kT}\right) \quad (5.1.3)$$

where k is the Boltzmann constant, D_o is a constant, T is the absolute temperature and E_a the activation energy. E_a can be calculated from the slope of the Arrhenious plot and is

found to be 1.65 eV which is in good agreement with the reported value of 1.8 ± 0.1 eV for RTP anneal and 1.6 ± 0.1 eV for furnace anneal. The pre-exponential factor (D_0) calculated was 95 cm²/sec. This value is D_0 is one order of magnitude higher than that reported for furnace anneal [1]. This contrast might be either due to the difference in initial nucleation of the silicide because of the presence of a thin native oxide layer between Pt and underlying Si, or due to inaccuracy in measuring the substrate temperature. Since during the formation of PtSi, Pt is the dominant diffusing specie [8], the activation energy calculated above is that of Pt diffusion through Pt₂Si.

5.2 Impurity Snow-plowing effect

Platinum silicide formation results in impurity pile up at the PtSi-Si interface as shown in figures (4.3.1-4.3.3). This is true for the three types of impurities investigated, viz. As⁺, B⁺ and P⁺. In general, impurity redistribution can be explained in terms of low solubilities of As⁺, B⁺ and P⁺ in PtSi. A model based on these assumptions will be described below. Consider the stages of PtSi formation as illustrated in figure (5.2.1a-c). Initially, Pt will diffuse through the Pt-Si interface to react with Si to form Pt₂Si. The impurity which previously resided in the Si used in Pt₂Si formation will be redistributed at two possible sites, one at the Pt₂Si-Si interface and the other in the growing Pt₂Si. This would depend on the diffusion rate of impurity in the growing Pt silicide and that of Pt into Si. Since the diffusion rate of Pt is much higher than that of the impurity, most of the impurity will be piled-up at the growing silicide-silicon interface. Nevertheless, some impurity will diffuse into the growing silicide. As the reaction proceeds further, more and more impurity will be available for redistribution. Most of this impurity will pile up at the growing silicide-silicon interface and the remaining will diffuse into the growing PtSi. The impurity which diffused into the PtSi will either reside in the PtSi film or appear at the silicide surface from where it will out diffuse. This will depend on the solid solubility limit of a particular impurity in the PtSi film. Once PtSi formation is complete, any further heating would cause additional

Figure (5.2.1): Schematic showing the impurity snow-plowing mechanism during PtSi growth.

Table 5.2.1: Integrated dopant concentration before and after silicidation for typical implant recipes of As⁺, B⁺ and P⁺.

Implant Specie	Dose and energy (cm ⁻² at KeV)	Integrated dopant concentration (cm ⁻²)		(b/a)x100 (%)
		before silicidation ^a	after silicidation ^b	
As ⁺	4E16 at 40	4.02E16	1.51E16	37.56
As ⁺	5E15 at 50	4.35E15	1.64E15	37.7
P ⁺	1E16 at 30	1.02E16	1.28E16	125*
B ⁺	5E15 at 10	3.82E15	2.55E15	66.75

^b This also includes the impurities in the Pt silicide film.

* The concentration greater than 100 percent might be due to miscalibration.

diffusion of the impurities from the PtSi-Si interface. This, depending on the diffusion rate of the impurity in the silicide and in the bulk Si, would be redistributed between these two areas. The impurities which entered into PtSi may show up at the PtSi surface and out diffuse there from, depending on the solid solubility of the impurity in PtSi. The impurity profile were measured by SIMS analysis before and after PtSi formation on samples doped with typical doses of As⁺, B⁺ and P⁺. Table 5.2.1 gives the summary of the implant condition, dose, integrated impurity concentration before and after silicidation for As⁺, B⁺ and P⁺. The integrated impurity concentration before silicidation as shown in the Table corresponds to that of after implant and activation anneal at an RTP cycle of 1050°C/30 sec. The last column gives the integrated impurity concentration after silicidation as a percentage of concentration before silicidation. It can be seen from the above table that in case of As⁺ and B⁺, the remaining integrated dopant concentration after PtSi formation is about 37.7% and 66.75% of the original concentration. This indicates that As⁺ and B⁺ diffuse out from the silicide film. This suggests the low solid solubility limit of As⁺ and B⁺ in the PtSi film.

On the other hand, in the case of P⁺, the integrated dopant concentration after PtSi formation is almost equal to the starting dopant concentration. This implies that the solid solubility limit of P⁺ in PtSi is much higher than that in case of As⁺ and B⁺, so that all of the redistributed P⁺ remains in the PtSi and most of it at the PtSi surface. As noticed from figure (4.5.1) that this higher surface concentration of P⁺ at the surface results in higher sheet resistance of PtSi film due to increase electron scattering effect.

The diffusion mechanism for impurity redistribution and ultimately pile-up at the PtSi-Si interface and to some extent at the PtSi surface agrees well with the experimental results presented in the previous chapter. The model described here differs from similar models described earlier in the literature [24-26] in the sense that all of those models assumes both Pt and Si as the diffusing species. It has now been well established [8] that during PtSi formation, Pt is the diffusing specie. Hence the model described here is more realistic.

5.3 Contact Resistance

The contact resistance (R_c) of Al-PtSi to p^+ diffused silicon is much lower than that of Al to p^+ diffused Si. This is because the barrier height of PtSi to p^+ Si is 0.25 eV, lower than the barrier height of Al to p^+ Si which is 0.4 eV. The other major contribution to lowering the R_c of Al-PtSi to p^+ Si comes from the impurity snow-plowing effect of PtSi during its formation.

The As^+ pile up at the PtSi/Si interface helped to reduce the contact resistance of Al-PtSi to n^+ diffused Si by as much as 30-40 percent than that of Al to n^+ Si. This is despite the higher barrier height of 0.87 eV for PtSi to n^- Si.

The calculated contact resistivity of Al-PtSi contact to p^+ diffused silicon varied from $2.4 \times 10^{-7} \Omega\text{-cm}^2$ for a boron dose of $1E15 \text{ cm}^{-2}$ to $1.4 \times 10^{-7} \Omega\text{-cm}^2$ for a boron dose of $5E15 \text{ cm}^{-2}$. Thus in the range of boron implant dose investigated, not much difference was observed in the contact resistivity of Al-PtSi to p^+ diffused silicon. This suggests that during PtSi formation, the PtSi/Si interface has reached the solid solubility limit of boron at the lowest dose of $1E15 \text{ cm}^{-2}$. Any further increase in B^+ dose did not significantly reduced the contact resistance. However, the contact resistivity achieved here is better than what is achievable in other technologies. On the other hand the contact resistivity of Al-PtSi contact to n^+ diffused silicon varied from $1.4 \times 10^{-6} \Omega\text{-cm}^2$ for an arsenic dose of $3E15 \text{ cm}^{-2}$ to $1.4 \times 10^{-7} \Omega\text{-cm}^2$ for an arsenic dose of $7E15 \text{ cm}^{-2}$. More data at doses higher than $7E15 \text{ cm}^{-2}$ are needed to verify if there is any room for the reduction of the contact resistance of PtSi to n^+ -Si.

The contact resistivity of Al-PtSi contact to p^+ polysilicon calculated varied from $4.8 \times 10^{-6} \Omega\text{-cm}^2$ for boron dose of $1E15 \text{ cm}^{-2}$ to $2.0E-7 \Omega\text{-cm}^2$ for boron dose of $5E15 \text{ cm}^{-2}$. On the other hand, the contact resistivity of Al-PtSi contact to n^+ polysilicon varied from $2.5 \times 10^{-6} \Omega\text{-cm}^2$ for an arsenic dose of $3E15 \text{ cm}^{-2}$ to $3.5 \times 10^{-7} \Omega\text{-cm}^2$ for an arsenic dose of $5E15$

cm^{-2} . The polysilicon was deposited on $0.5\ \mu\text{m}$ of thermal oxide. Moreover, the polysilicon deposited was very grainy. The high resistivity at lower implant dose of B^+ and As^+ may be explained in terms of enhanced diffusion and limited quantity of impurities available. Due to limited quantity of impurity available at lower dose and rapid diffusion through the grain boundaries of polysilicon, most of the impurities would accumulate at the polysilicon/ SiO_2 interface and the polysilicon surface would be depleted of implanted impurities. This is also evident from the high sheet resistance values at lower dose. At high doses however, due to abundant quantity of impurities available and limited thickness of $0.5\ \mu\text{m}$ of polysilicon, the implanted impurity is available at the polysilicon surface. This is evident from the lower sheet resistance values at higher doses. This surface impurity of polysilicon gets snow-plowed during PtSi formation, which is evident from the lower contact resistances at higher implant doses.

5.4 Devices

5.4.1 Schottky barrier diodes

The ideality factor of platinum silicided Schottky diodes fabricated with p^+ guard ring was in the range of 1.04-1.06 which is close to ideal. The saturation leakage current was about $1\ \mu\text{A}/\text{cm}^2$, whereas the current at reverse bias of 5 volts was about $4\ \mu\text{A}/\text{cm}^2$.

On the other hand, the ideality factor of PtSi Schottky diodes fabricated without p^+ guard ring was in the range of 1.08-1.10. The saturation leakage current was about $3.0\ \mu\text{A}/\text{cm}^2$ which is about three times higher than for Schottky diodes with p^+ guard ring. The reverse bias leakage current at 5 volts varied from $8\text{-}20\ \mu\text{A}/\text{cm}^2$ for diodes area ranging from $2500\text{-}625\ \mu\text{m}^2$. The higher leakage current in this type of diodes results from high and sharp electric field in the depletion region in the silicon.

5.4.2 PN junctions

The ideality factor for area intensive platinum silicided P⁺N junctions fabricated was in the range of 1.01-1.02. The closer the ideality factor is to unity, the more ideal will be the behavior of the p-n junction. This resulted in low saturation leakage current of 50 pA/cm². The reverse bias leakage current at -5 volts was on an average 27 nA/cm² which is comparable with what is achievable in other existing technologies [39].

As expected, the forward current per unit area for the PtSi Schottky diode was also higher than in p-n junction for same value of the forward voltage. This is because a Schottky barrier diode is a majority-carrier current device as compared to a p-n junction which is a minority-carrier current device. Consequently the forward voltage drop in a Schottky barrier diode is much lower than in a p-n junction.

5.5 Salicided NMOS transistors

The drain current of salicided NMOS transistor is about 8-12 percent higher than that of an unsilicided NMOS transistor under the same bias conditions. In absence of side-wall spacer, very thin PtSi film (about 500 Å) was formed. Hence if the normal PtSi thickness (1000 Å of TiSi₂ is being used presently in the industry) is used, a greater increase in drain current can be achieved. This increase in drain current in salicided transistor comes from the reduction of parasitic resistances in series with the junctions, as explained in chapter 1, and from the reduction of source/drain contact resistances.

The 11 stage platinum salicided NMOS ring oscillator fabricated resulted in a 28 percent increase in frequency over that of an unsilicided one. The frequency of salicided oscillator was 22.5 MHz as compared to 17.5 MHz for an unsilicided one. The L/W ratio of individual transistor was 5 µm/5 µm.

CHAPTER 6

Conclusion and Recommendations

6.1 Conclusion

A platinum silicide process suitable for BiCMOS applications has been developed. Platinum silicide formation occurring from the interaction of a platinum film with a silicon substrate has been studied in detail owing to its ability to form stable ohmic and Schottky barrier contacts. Platinum film deposited on doped and undoped single crystal silicon substrates was then made to react with the underlying silicon using a wide range of rapid thermal annealing (RTA) cycles. The reacted film was characterized using various techniques. A four-point probe was used to measure silicide sheet resistance and hence, resistivity. Transmission electron microscopy (TEM) was used to study the layer microstructure, film thickness, grain size and platinum-silicide/silicon interface quality. Auger electron spectroscopy was used for investigating contaminants in as-deposited and reacted films as well as the phase growth sequence. Rutherford back-scattering analysis was used to investigate the phase growth sequence, layer thicknesses and surface dopant

concentration. Secondary ion mass spectroscopy was used for evaluating dopant profile before and after the platinum silicide formation.

A Van-der-Pauw structure was used to characterize diffused region sheet resistance. Kelvin structures were used to characterize the contact resistance to p^+/n^+ silicon and p^+/n^+ polysilicon. Platinum silicided Schottky barriers were fabricated to characterize their electrical performance. Silicided p-n junctions, both area and edge intensive, were also fabricated to characterize their electrical performance and for comparison with Schottky barrier diodes. Silicided NMOS devices were fabricated to characterize their electrical performance and to investigate platinum silicide overgrowth and lateral silicidation. Ring oscillator were used to study the impact of silicidation on circuit speed.

The AES, RBS and TEM analyses carried out were consistent with one another. They clearly demonstrate the phase growth sequence and growth kinetics of PtSi formation. The reaction is found to start at the Pt/Si interface. Initially, a metastable phase of platinum silicide (Pt_2Si) is formed until all of the platinum film is consumed. The growth of the final and stable phase (PtSi) then starts at the Pt_2Si/Si interface and proceeds towards the surface until the entire Pt_2Si is converted to PtSi. The phase growth sequence thus can be summarized as $Pt \rightarrow Pt_2Si \rightarrow PtSi$. This phase growth sequence is observed to be independent of any variation in RTA cycle, film thickness or the type of wafer on which the silicide is formed. No simultaneous existence of Pt, Pt_2Si and PtSi was observed, except when the silicide formation was impeded by either impurities in the original film or in the RTA ambient. The resistivity of PtSi film was determined to be $33 \mu\Omega\text{-cm}$. Agglomeration of PtSi film was observed to occur around 850°C to 875°C . This in no way is disadvantageous for PtSi to be used for contact metallization in submicron IC fabrication as the higher limit is critical even for existing $TiSi_2$ technology [40]. Moreover, in submicron technology, a lower thermal budget would be necessary to maintain the integrity of the shallow junctions.

The growth of PtSi was observed to follow an Arrhenious type of relationship with activation energy of 1.65 eV.

Platinum silicide formation also resulted in impurity pile-up at the PtSi/Si interface. All the three impurities implanted in this study viz. As⁺, B⁺ and P⁺ were observed to accumulate at the PtSi/Si interface during PtSi formation. The impurity pile-up in the case of silicided samples resulted in impurity concentration about a factor of 2 higher than that in case of unsilicided sample. A qualitative model has been presented for this pile-up on the basis of diffusion and solid solubility of the impurities in the growing silicide and in the Si. The model presented agreed well to the experimental data extracted using SIMS analysis. The ability of PtSi to form good ohmic contact, due to its snow-plowing effect, can be utilized in submicron technology to form lightly doped junctions (LDJ).

The impurity pile-up resulted in reduced contact resistance of PtSi to n⁺ and p⁺ Si. The specific contact resistivity of PtSi to p⁺ Si was in the range of $1.3 \times 10^{-7} \Omega\text{-cm}^2$ to $2.4 \times 10^{-7} \Omega\text{-cm}^2$ for the range of B⁺ doses used. Contact resistance saturation was observed for a B⁺ dose of $3 \times 10^{15} \text{ cm}^{-2}$ and higher. This was explained on the basis of solid solubility limit of B⁺ in Si. For PtSi to n⁺ Si, the contact resistance values measured were in the range of $1.4 \times 10^{-6} \Omega\text{-cm}^2$ to $1.4 \times 10^{-7} \Omega\text{-cm}^2$ for the As⁺ doses used in this study. No contact resistance saturation was observed even for the highest As⁺ dose of $7 \times 10^{15} \text{ cm}^{-2}$ used. The lower achievable values are comparable with the existing technologies.

The Pt silicided Schottky barrier diodes formed with p⁺ guard ring resulted in close to ideal behavior. The average ideality factor recorded was 1.04 and a reverse bias leakage current of about $4 \mu\text{A/cm}^2$ at -5 volts. This very low reverse leakage current is due to higher barrier height of PtSi to n⁻ Si. The ideality factor of platinum silicided p-n junction was observed to be 1.01 with a leakage current of 40 nA/cm^2 at a reverse bias of -5 volts.

The salicidation of gate, source and drain resulted in considerable reduction in the resistance in series with the contacts. This is crucial for achieving higher device speed. For an 11 stages ring oscillator built using salicided NMOS technology resulted in about a 30 per cent increase in speed. This was achieved using only 260 Å of as-deposited Pt film, which would give about 500 Å of PtSi. The performance can be further enhanced using thicker as-deposited Pt film and hence thicker PtSi film. As Pt is the diffusing specie in the PtSi formation reaction and since the reaction temperature is low (in the order of 500° C), there is no silicide overgrowth problem with this metallizing scheme. This was demonstrated by saliciding the NMOS transistors without side wall spacers. This is clearly in contrast to existing technologies where extra processing steps are mandatory to avoid silicide overgrowth and hence avoid bridging the gate and S/D region of MOS transistors.

The wet etch selectivity of Pt to PtSi is in excess of 5:1 for PtSi formed using rapid thermal processing. The dry etch selectivity is in the order of 33:1 [8] which is good for pattern generation in submicron technology. Also the high resistance of PtSi to HF etch, in contrast to existing silicides, is an advantage for use in the industry.

The results of this study demonstrate that PtSi can be a very promising candidate for IC fabrication technology specially in deep submicron regime as the post silicidation temperature will have to be lowered to maintain the shallow junction integrity.

6.2 Recommendations for future work

Due to various limitations, all the test structures fabrication was carried out in one single lot. As such, the process was not optimized for any single test structure. This was the reason for inconsistent results for PtSi contacts to polysilicon. Though the results achieved were still very promising for PtSi contacts to diffused Si, PtSi to n⁺ Schottky barriers and Pt silicided PN junctions, the process needs to be optimized for each structure to exploit the full potential of PtSi technology in deep submicron technology.

To reliably reproduce PtSi ohmic contact and maintain their integrity during usage, Al diffusion (as Al is still used as final metal) through the PtSi film should be studied in detail. A logical step would then be to explore the formation of epitaxial PtSi.

PtSi should be investigated as a diffusion source to form uniform and reliable shallow junctions. In this case implantation is to be carried out through PtSi. X-ray diffraction analysis can then be used to investigate the knock-on Pt atoms.

REFERENCES

- 1) Marc Wittmer, "Growth Kinetics of Platinum Silicide", J. Appl Phys., 54(9), Sept. 1983, pp. 5081-5086.
- 2) J. B. Bindell et al, "An analytical Study of Platinum Silicide Formation", Thin Solid Films, 37(1976), pp. 441-452.
- 3) J. T. Pan and I. A. Blech, "In situ Study of Film Stress and Kinetics of Platinum Silicide Formation on Silicon", Thin Solid Films, 113(1984), pp. 129-134.
- 4) C. A. Cider et al, "Platinum silicide formation under ultrahigh vacuum and controlled impurity ambients", J. Appl Phys., 52(4), April 1981, pp. 2860-2868.
- 5) C. Canali et al, "Pt₂Si and PtSi formation with high purity Pt thin films", Appl Phys. Lett., vol. 32, No. 1, July 1977, pp. 43-45.
- 6) C. G. Hopkins et al, "The kinetics of platinum silicide formation using cw lamp annealing", Mat. Res. Soc. Symp. Proc., vol. 25(1984), pp. 87-91.
- 7) J. Van der Spiegel, "Fast radiative processing of platinum silicide", J. Appl. Phys., 57(2), 15 Jan. 1985, pp. 607-609.
- 8) A. A. Naem, "Platinum silicide formation using rapid thermal processing", J. Appl. Phys., 64(8), Oct. 1988, pp. 4161-4167.
- 9) R. H. Dennard et al, "Design of Ion Implanted MOSFETS With Very Small Physical Dimensions", I. E. E. E. Journal of Solid State Circuits, Vol. SC-9, pp. 256, 1974.
- 10) J. R. Brews et al, "Generalized Guide for MOSFETS Miniaturization", I. E. E. E. Electron Device Letters, EDL-1, pp. 2, 1980.
- 11) P. K. Chatterjee et al, "The Impact of Scaling Laws on the Choice of N-channel or P-channel for MOS VLSI", I. E. E. E. Electron Device Letters, EDL-1, pp. 220, 1980.

- 12) G. Baccarani et al, "Generalized Scaling Theory and its Application to a 1/4 Micrometer MOSFET Design", IEEE Trans. On Electron Devices, ED-31, pp 452, 1984.
- 13) K. C. Saraswat and F. Mohammadi, "Effect of Scaling Interconnections on the Time Delay of VLSI Circuits", IEEE Trans. On Electron Devices, ED-29, pp. 645, 1982.
- 14) K. K. Ng and W. T. Lynch, "The Impact of Intrinsic Series Resistance on MOSFET Scaling", IEEE Trans. on Electron Devices, ED-34(3), pp. 503, 1987.
- 15) S. S. Cohen et al, "Al-0.9% Si/Si Ohmic Contacts to Shallow Junctions", Journal of Electrochemical Society, Vol. 129, No. 6, pp. 1335, 1982.
- 16) Dipankar Pramanik, "Aluminium Metallization for ULSI", Solid State Technology, pp. 73-79, 1990.
- 17) S. P. Murarka, "Silicides for VLSI applications", Academic Press, New York, 1983.
- 18) A. A. Naem, "Salicides for Microelectronic Technology", Intl. Microelectronic Conference, 1991, Egypt.
- 19) K. Maex et al, "Stability of As and B doped Si with respect to Overlaying CoSi₂ and TiSi₂ Thin Films", J. Mater. Res., Vol 4, No. 5, pp. 1209, 1989.
- 20) A. Naem, "Formation of Cobalt Silicide by Rapid Thermal Annealing", Northern Telecom Ltd., Private Communication.
- 21) A. C. Berti and V. Bolkhovskiy, "A Manufacturable Process for the Formation of self aligned Cobalt Silicide in a sub-micrometer CMOS Technology", Proceeding of VMIC Conf., pp. 267, June 1992.
- 22) C. Mallerdeau et al, "Characterization of TiSi Ohmic and Schottky Contact by Rapid Thermal Annealing Technology", J. Electrochemical Society, 1985.
- 23) J. M. Shannon, "Reducing the effective height of a Schottky barrier using low energy ion implantation", Appl. Phys. Lett. 24, 369 (1974), pp. 369-372.

- 24) Jeffery B. Bindell et al, "Ion-implanted low-barrier PtSi Schottky barrier diodes", I.E.E.E. Transaction on electron devices, vol. ED-27, No. 2, Feb. 1986, pp. 420-425.
- 25) Peter W. Lew and c. R. Helms, "Effect of platinum silicide thickness and annealing temperature on arsenic redistribution", J. Appl. Phys., 56(12), 15 Dec. 1984, pp. 3418-3427.
- 26) M. Wittmer and T. E. Seidel, "The redistribution of implanted dopants after metal-silicide formation", J. Appl. Phys., 49(12), Dec. 1978, pp. 5827-5834.
- 27) Akira Kikuchi and Shojiro Sugaki, "Redistribution of Implanted Phosphorus after Platinum Silicide formation and the Characteristics of Schottky Diodes", J. Appl. Phys., 53(5), May 1982, pp. 3690-3693.
- 28) C. Y. Wei et al, "The effect of Pt_xSi growth on the redistribution of p-type dopants in silicon", Thin Solid Films, 104(1983), pp. 221-225.
- 29) R. M. Anderson and T. M. Reith, "Microstructural and Electrical Properties of Thin PtSi Films and their Relationship to Deposition Parameters", J. Electrochem Soc.; Solid State Science and Technology, pp. 1337, Oct. 1975.
- 30) S. S. Cohen et al, "Platinum Silicide Ohmic Contacts to Shallow Junctions in Silicon", J. Applied Phys., 53(12), pp. 8856, Dec. 1982.
- 31) I.C. Technology, Chapter 14, pp. 644.
- 32) P. Rosser and G. Tomkins, "Silicides for VLSI Interconnects", Vacuum, vol.. 35, Nos. 10-11, 1985, pp. 419-434
- 33) D. Moy et al, "Effect of Processing Conditions on the Characteristics of Platinum Silicide Schottky Barrier Diodes", Solid State Electronics, Vol. 31, No. 5, pp. 843, 1988.
- 34) B. Y. Tsaur et al, "Effect of interface structure on the electrical characteristics of PtSi-Si Schottky barrier contacts", Thin Solid Films, 93(1982), pp. 331, 1982.
- 35) E. K. Broadbent et al, "Self aligned silicided (PtSi and CoSi₂) ultra-shallow p+ /n junctions", I.E.E.E. Electron device Lettet, vol. EDL-6, No.3, July 1987, pp. 318-320.

- 36) R. C. Ellwanger, "Rapid thermal annealed platinum silicide for self aligned bipolar applications", Proc. of 3rd Intl. I.E.E.E. VMIC, July 9-10, 1986, I.E.E.E. Cat. No. 86CH2337-4 pp. 457.
- 37) W. M. Loh et al, "Analysis and scaling of Kelvin resistors for extraction of specific contact resistivity", I.E.E.E. Electron Device Letter, vol. EDL-6, No. 3, March 1985, pp. 105-108.
- 38) Hiroki Muta and Daizaburo Shinoda, "Solid-solid reaction in Pt-Si system", J. Appl. Phys., Vol. 43, No. 6, June 1972, pp.2913-2915.
- 39) Chih-Shih Wei et al, "Comparison of cobalt and titanium silicides for salicide process and shallow junction formation", International Conference on VLSI Metal Interconnects, June 12-13, 1989, pp 241-250.
- 40) Chih-Yuan Lu et al, "Process limitation and device design tradeoffs of self-aligned TiSi_2 junction formation in submicrometer CMOS devices", I.E.E.E. Trans. on Electron Devices, vol 38, No. 2, Feb 1991, pp 246-254.

APPENDICES

APPENDIX I

Test Structure Layout

Table I.1: Test Structure and their sizes.

Test Structure	Sizes (μm^2)	Figure No.
Contact Chain	6.3, 14.1, 25, 18.75	I.1
Kelvin Structure (Si)	6.3, 9.4, 14.1, 18.8, 25	I.2
Kelvin Structure (Poly)	6.3, 9.4, 12.5, 14.1, 25	
Schottkies (with/without p⁺ guard)	625, 976.6	I.3 a, I.3b
pn junctions (area intensive)	35156	I.4a
pn junctions (edge intensive)	9687.5	I.4b
Van-der-Pauw	1600	I.5
NMOS Transistors	L/W ($\mu\text{m}/\mu\text{m}$) = 20/75, 10/75, 5/75, 2.5/75, 5/5 and 2.5/2.5	I.6

Figure (I.1): Layout of a typical Contact chain Structure

Figure (I.2): Typical Layout of the Kelvin Structure

Figure (I.3a): Typical Layout of a Schottky diode without p⁺ guard ring.

Figure (I.3b): Typical Layout of a Schottky diode with p⁺ guard ring.

Figure (I.4a): Typical Layout of a pn junction (area intensive)

Figure (I.4b): Typical Layout of a pn junction (edge intensive)

Figure (I.5): Typical Layout of a Van-der-Pauw structure.

Figure (I.6): Typical Layout of a MOS Transistor.

APPENDIX II

Process Steps for fabrication of Test Structures

II.1 Process flow for Contact chain, Kelvin structure, Van-der-Pauw structure, Schottky diodes and PN junctions

- 1) Deposit 0.6 μ m of field oxide
Temp = 1100° C Time = 60 min Dry O₂

- 2) Back side Ohmic contact diffusion and drive in
Group A: Phosphorus Diffusion
Temp = 1000° C Time = 10 min.
Drive in Temp = 1075° C Time = 10 min. in wet O₂

Group B: Boron Diffusion
Temp = 1000° C Time = 5 min.
Drive in Temp = 1075° C Time = 15 min. in O₂

- 3) Polysilicon Deposition (Undoped)
Thick = 0.5 μ m Temp = 630° C

4) Pattern polysilicon for implant P. E. 01

5) Pattern Oxide for implant P. E. 02

6) Grow implant mask oxide
Temp = 900° C Time = 60 min. in Dry O₂

7) Implant

Group A

Wafer #	Energy (KeV)	Dose (cm ⁻²)
NK1 - NK4	50	As 3E15
NK5 - NK8	"	" 5E15
NK9 - NK12	"	" 7E15

Group B

Wafer #	Energy (KeV)	Dose (cm ⁻²)
PK13 - PK16	10	B 1E15
PK17 - PK20	"	" 3E15
PK21 - PK24	"	" 5E15

8) Implant activation and anneal
Temp = 1050° C Time = 30 sec. in N₂

9) LOTOX Deposition
Temp = 400° C Time = 15 min.

10) Open Contact Windows P. E. 03

11) Sputter deposit 500 Å of Pt

12) RTA for Silicidation
Temp = 550° C Time = 10 sec.

13) Etch unreacted Pt

- 14) Deposit 500Å of TiW
- 15) Deposit 1.2 µm of Al on both sides
- 16) Pattern Al on the front
- 17) Anneal Al in N₂
Temp = 450° C Time = 20 min.

P. E. 04

II.2 Process flow for Carleton NMOS technology

- 1) Deposit .08 μm of pad oxide
Temperature = 1100°C Time = 20 min. in Dry O₂
- 2) Deposit .08 μm of silicon nitride
Temperature = 820°C Time = 10 min. in 37.6% SiH₂Cl₂ and 35.3% NH₃.
- 3) Open device well P. E. mask CU-150-01.
- 4) Grow 1.0 μm of field oxide
Temperature = 1100°C Time = 10 min. in Dry O₂
Time = 180 min. in O₂ + pyrogenic H₂O
Time = 30 min. in O₂ + 25% HCl.
- 5) Etch nitride and pad oxide
- 6) Grow .05 μm of gate oxide
Temperature = 1100°C Time = 15 min. in O₂.
- 7) Deposit 0.4 μm of polysilicon
Temperature = 625°C Time = 30 min. in 25.6% SiH₄.
- 8) Gate P.E. mask CU-150-02.
- 9) Source/Drain oxide etch back
Time = 50 sec. in buffered HF at 20°C.
- 10) Source/Drain Diffusion
Temperature = 1000°C Time = 2 min. in POCl₃.
- 11) Source/Drain drive in
Temperature = 1075°C Time = 10 min. in O₂.
- 12) Deposit platinum on wafers F-92-05,06 and 07
wafer # F-92-05 thickness = 255 $\pm$ 25 Å
wafer # F-92-06 thickness = 420 $\pm$ 40 Å
wafer # F-92-07 thickness = 475 $\pm$ 45 Å
- 13) Form platinum silicide

Temperature = 400°C Time = 20 sec. in N₂.

Temperature = 550°C Time = 10 sec. in N₂.

- 14) Etch unreacted platinum

Temperature = 75°C Time = 30 sec. in aqua regia.

- 15) Deposit 0.5 μm of BPSG on wafer # F-92-01
and LOTOX on wafer # F-92-05,06 and 07

BPSG deposition:

Temperature = 406°C Time = 18.5 min. in 5.2% SiH₄, 13.6% SiH₄/PH₃,
27.5% O₂ and 52.3% TMB.

BPSG drive in

Temperature = 900°C Time = 20 min. in N₂.

LOTOX deposition:

Temperature = 406°C Time =

- 16) Contact P.E.

mask CU-150-03 (dark field).

- 17) Deposit 1.0 μm of aluminum on front side.

- 18) Metal P.E.

mask CU-150-04.

- 19) Back poly/oxide removal.

- 20) Top metal anneal.

Temperature = 450°C Time = 20 min. in H₂.

- 21) Deposit 0.5 μm of aluminum on back side.

APPENDIX III

Figure (III.1.1a): Sheet resistance of Pt-Si structure as a function of temperatures for constant RTP anneal times, on wafer implanted with $4E16 \text{ cm}^{-2}$ of As^+ at 40 keV and activated at $1050^\circ \text{C}/30 \text{ sec}$. The as-deposited Pt thickness was $550 \pm 50 \text{ \AA}$.

Figure (III.1.1b): Sheet resistance as a function of anneal times at constant RTP temperatures, on wafer implanted with $4E16 \text{ cm}^{-2}$ of As^+ at 40 keV and activated at $1050^\circ \text{C}/30 \text{ sec}$. The as deposited Pt thickness was $550 \pm 50 \text{ \AA}$.

Figure (III.1.2a): Sheet resistance of Pt-Si structure as a function of temperatures for constant RTP anneal times, on wafer implanted with $1\text{E}16\text{ cm}^{-2}$ of As^+ at 50 keV and activated at $1050^\circ\text{C}/30\text{ sec}$. The as-deposited Pt thickness was $550\pm50\text{ \AA}$.

Figure (III.1.2b): Sheet resistance as a function of anneal times at constant RTP temperatures, on wafer implanted with $1\text{E}16\text{ cm}^{-2}$ of As^+ at 50 keV and activated at $1050^\circ\text{C}/30\text{ sec}$. The as deposited Pt thickness was $550\pm50\text{ \AA}$.

Figure (III.1.3a): Sheet resistance of Pt-Si structure as a function of temperatures for constant RTP anneal times, on wafer implanted with $7E15 \text{ cm}^{-2}$ of As^+ at 50 keV and activated at $1050^\circ \text{C}/30 \text{ sec}$. The as-deposited Pt thickness was $550 \pm 50 \text{ \AA}$.

Figure (III.1.3b): Sheet resistance as a function of anneal times at constant RTP temperatures, on wafer implanted with $7E15 \text{ cm}^{-2}$ of As^+ at 50 keV and activated at $1050^\circ \text{C}/30 \text{ sec}$. The as deposited Pt thickness was $550 \pm 50 \text{ \AA}$.

Figure (III.2.1a): Sheet resistance of Pt-Si structure as a function of temperatures for constant RTP anneal times, on wafer implanted with $2E16 \text{ cm}^{-2}$ of P^+ at 30 keV and activated at $1050^\circ \text{C}/30 \text{ sec}$. The as-deposited Pt thickness was $550 \pm 50 \text{ \AA}$.

Figure (III.2.1b): Sheet resistance as a function of anneal times at constant RTP temperatures, on wafer implanted with $2E16 \text{ cm}^{-2}$ of P^+ at 30 keV and activated at $1050^\circ \text{C}/30 \text{ sec}$. The as deposited Pt thickness was $550 \pm 50 \text{ \AA}$.

Figure (III.2.2a): Sheet resistance of Pt-Si structure as a function of temperatures for constant RTP anneal times, on wafer implanted with $7 \times 10^{15} \text{ cm}^{-2}$ of P^+ at 30 keV and activated at $1050^\circ \text{C}/30 \text{ sec}$. The as-deposited Pt thickness was $550 \pm 50 \text{ \AA}$.

Figure (III.2.2b): Sheet resistance as a function of anneal times at constant RTP temperatures, on wafer implanted with $7 \times 10^{15} \text{ cm}^{-2}$ of P^+ at 30 keV and activated at $1050^\circ \text{C}/30 \text{ sec}$. The as deposited Pt thickness was $550 \pm 50 \text{ \AA}$.

Figure (III.3.1a): Sheet resistance of Pt-Si structure as a function of temperatures for constant RTP anneal times, on wafer implanted with $3 \times 10^{15} \text{ cm}^{-2}$ of B^+ at 10 keV and activated at $1050^\circ \text{C}/30 \text{ sec}$. The as-deposited Pt thickness was $550 \pm 50 \text{ \AA}$.

Figure (III.3.1b): Sheet resistance as a function of anneal times at constant RTP temperatures, on wafer implanted with $3 \times 10^{15} \text{ cm}^{-2}$ of B^+ at 10 keV and activated at $1050^\circ \text{C}/30 \text{ sec}$. The as deposited Pt thickness was $550 \pm 50 \text{ \AA}$.

Figure (III.3.2a): Sheet resistance of Pt-Si structure as a function of temperatures for constant RTP anneal times, on wafer implanted with $7E15 \text{ cm}^{-2}$ of B^+ at 10 keV and activated at $1050^\circ \text{C}/30 \text{ sec}$. The as-deposited Pt thickness was $550 \pm 50 \text{ \AA}$.

Figure (III.3.2b): Sheet resistance as a function of anneal times at constant RTP temperatures, on wafer implanted with $7E15 \text{ cm}^{-2}$ of B^+ at 10 keV and activated at $1050^\circ \text{C}/30 \text{ sec}$. The as deposited Pt thickness was $550 \pm 50 \text{ \AA}$.

END

2 0 7 9 4

FIN