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The Design of a High-Frequency Voltage-Controlled Oscillator in BiCMOS Using On-Chip Inductors

by

Matthew K. Maguire, B.Eng.

A thesis submitted to the Faculty of Graduate Studies and Research
in partial fulfillment of the requirements for the degree of
Master of Engineering

Ottawa-Carleton Institute for Electrical Engineering
Department of Electronics, Carleton University
Ottawa, Ontario
May, 1995

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submitted by

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in partial fulfillment of the requirements
for the degree of Master of Engineering.

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Abstract

The design of a monolithic LC voltage-controlled oscillator implemented in silicon BiC-MOS technology suitable for applications such as mobile radio is presented in this thesis. The object of this work is the design of a VCO capable of GHz operating frequencies and low phase noise. A significant portion of this work is directed toward the development of models which facilitate the prediction of oscillator performance and phase noise characteristics. The relationship between quality factor, tuning range, and phase noise are investigated. The circuit is based on a Gilbert cell structure which utilizes two LC tuned circuits with different resonant frequencies. Inductors are implemented as square planar spirals on a layer of silicon oxide. An experimental version of the circuit realized a tuning range of 37 MHz with a center frequency of 1.5 GHz. The results of the simulation of oscillator performance and phase noise are contrasted to the measured characteristics of the fabricated circuit.

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List of Symbols and Abbreviations

Amplifier

Battery

Bipolar transistor (nnp)

Capacitor

Current source

Diode

Ground terminal

Inductor

Inverter

NMOS transistor

PMOS transistor

Potentiometer

Resistor

Schmitt trigger

Sinusoidal voltage source

Summer

Switch

Tapped inductor

Varactor

Voltage source

ac	alternating current
β	dc current gain
BATMOS	Bipolar Analog Telecom MOS
BiCMOS	Bipolar CMOS
BER	Bit error rate
BJT	Bipolar junction transistor
BNR	Bell Northern Research
BPSK	Binary-phase-shift-keying
CAD	Computer assisted drafting
CMC	Canadian Microelectronics Corporation
CMOS	Complementary Metal Oxide Semiconductor
dc	Direct current
DDFS	Direct digital frequency synthesizer
Δf	Bandwidth in hertz
DFFT	Fast Fourier transform
f_m	Modulating frequency
f_T	Unity-gain bandwidth
GaAs	Gallium arsenide
g_m	small-signal transconductance
IC	Integrated circuit
IF	Intermediate frequency
I/O	Input-output
k	Boltzmann constant
NMOS	N-channel MOS
NTE	Northern Telecom Electronic
PLL	Phase-locked loop
ppm	Parts-per-million
PSD	Power spectral density
q	Electron charge
Q	Quality factor
QPSK	Quadrature-phase-shift-keying
RFC	Radio frequency choke

T	Temperature, °Kelvin
VCO	Voltage-controlled oscillator

Chapter 1

Introduction

The requirements for modern portable radio transceivers include low power consumption, low cost and operation at frequencies in the GHz range. The implementation of a single-chip radio transceiver presents a major challenge for current technology. The phase locked loop (PLL) can be realized as an inexpensive integrated circuit component, and as a result, PLL frequency synthesizers are used frequently in miniature radio transceivers. This work focuses on the design of one of the central components of a PLL, the voltage-controlled oscillator (VCO).

Current technology has facilitated the implementation of monolithic VCOs, but these are limited to digital architectures using CMOS technology. The maximum reported speed of CMOS VCOs is about 900 MHz [Th]. Recent advances in silicon technology have resulted in the fabrication of on-chip inductors with quality factors (Q) of about 8. VCOs in the 1 to 2 GHz frequency range can now be realized using on-chip LC tuned circuits. The use of this technique should result in improved phase noise performance and high frequency stability compared to previous monolithic designs.

This thesis studies the trade-offs involved in VCO design and proposes a monolithic VCO implementation using on-chip LC tuning circuits.

1.1 Thesis Outline

Chapter 2 presents a discussion of VCO techniques including suitability for monolithic implementation. A comparison of existing methods in terms of maximum operating frequency, power dissipation, area, sensitivity to process variations, and phase noise is developed. Design issues and considerations are explored. Parameters for VCO design including power consumption, linearity, spectral purity, monolithic implementation, and tuning range are presented. A brief discussion of synthesizer techniques is included.

Design considerations for an LC VCO are presented in Chapter 3. Criteria for oscillation are considered, and a simple oscillator model is used as a basis for oscillator design and analysis. Methods of oscillator analysis using open-loop and closed-loop equivalent circuits are discussed. The operation of the circuit is described, and a small-signal model of the oscillator circuit is developed. The relationship between tuning range and Q is investigated. A discussion of oscillator phase noise and models used for its analysis are pre-

sented. A procedure for the prediction of phase noise is proposed.

Chapter 4 focuses on the design and implementation of the LC VCO circuit. Utilization of the BATMOS process using on-chip inductors is considered. A distributed model for the on-chip inductors is introduced. A detailed description of the phase noise simulation process is provided. The results of post-layout simulations and phase noise simulations are presented.

Experimental results for the fabricated circuit are reported in chapter 5. These include the phase noise measurement test procedure, the measured phase noise, and a summary of VCO performance. Chapter 6 is a summary of the work and makes recommendations for future endeavours in this area.

Chapter 2

Techniques for Monolithic VCO Implementation

Since the VCO is an essential component in an indirect frequency synthesizer, it is useful to discuss this synthesis technique so that requirements for high performance VCOs can be understood in the context of their most common application. It is also useful to present an overview of synthesizer techniques so that the rationale for the use of indirect frequency synthesis can be appreciated.

The main focus of this chapter is a discussion of VCO architectures. Desirable parameters for VCO design are described. A number of VCO configurations are discussed, and are characterized in terms of their suitability for monolithic implementation, high frequency capability, temperature stability, phase noise, linearity, and tuning range. Advantages and limitations of recent high-speed VCO implementations are contrasted to those of the proposed VCO architecture.

2.1 Frequency Synthesis Techniques

The front-end of a cellular radio receiver incorporates a frequency synthesizer which provides channel selection and tunability. A frequency synthesizer is a device that generates a large number of frequencies from a single reference frequency [Smi]. There are three general classes of frequency synthesizer techniques: direct analog synthesis, indirect synthesis, and direct digital synthesis.

2.1.1 Direct Frequency Synthesis

In direct frequency synthesis, the frequency of a reference oscillator is translated directly, using analog techniques. Analog synthesis techniques consist of frequency division, mixing, multiplication, and filtering [Rei]. Fast frequency switching, fine frequency resolution, low phase noise, and the highest operating frequencies are achieved by this method [Smi]. However, considerable hardware is required, power consumption is high compared to the other techniques, and spurious frequency components can appear at the output due to non-linear mixing. Filtering requirements, large size, and high power consumption make this method unsuitable for monolithic synthesizer realizations.

2.1.2 Direct Digital Frequency Synthesis

Direct digital frequency synthesizers (DDFS) use digital techniques to directly synthesize the output waveform. A reference oscillator is used as a clock for the digital operation. N samples of a sine wave are stored in memory, and are output at a uniform rate to a digital-to-analog converter. A block diagram of a DDFS is shown in Figure 2.1 [Smi].

Advantages of DDFS include fast frequency switching, fine frequency resolution, low power consumption and low phase noise [Smi]. However, they are limited to relatively low frequencies (below 100 MHz) [NS].

2.1.3 Indirect Frequency Synthesis

Indirect frequency synthesis utilizes a phase-locked loop to generate its output frequency. It consists of three basic components: a VCO, a phase detector, and a loop filter. A divide-by- N counter can be incorporated to provide an output frequency at a multiple of the reference, such that

$$f_o = Nf_r \quad (2.1)$$

Figure 2.1 Direct digital synthesizer block diagram

There are a number of difficulties associated with the use of simple PLLs. The choice of reference frequency significantly controls loop performance. The reference frequency must be small to obtain fine frequency resolution. The first problem with a low reference frequency is that a large variation in N is required to cover a broad frequency range. A large variation in N will result in a wide variation in loop dynamics. The linearized loop transfer function is directly proportional to N , so that if N varies between 1 and 1000, there will be a 60 dB variation in the open-loop gain [Smi]. Therefore, fine frequency resolution and wide tuning bandwidths are conflicting requirements.

A second problem associated with a low reference frequency is that the loop bandwidth must be less than or equal to the reference frequency. The low-pass filter must filter out the reference frequency and its harmonics present at the output of the phase detector. Therefore the bandwidth of the low-pass filter must be less than the reference frequency [Smi]. Since frequency resolution is inversely proportional to the switching speed, a low reference frequency limits the speed at which the synthesizer can change frequency.

The basic architecture of a phase-locked loop is shown in Figure 2.2. The phase detector compares the phase of divided down VCO signal f_0/N to the phase of the reference f_r , and outputs a voltage v_1 proportional to the phase difference. The difference voltage is filtered by the loop filter, and its output voltage v_2 is applied to the VCO to control its output frequency f_0 . Thus the phase and frequency of the VCO are locked to the phase and frequency of the reference signal [Wol].

Figure 2.2 Phase-locked loop block diagram

A third problem associated with a low reference frequency and the resulting low loop bandwidth is its effect on noise present in the VCO. Since VCO noise is concentrated close to the oscillator frequency, it can be interpreted as low-frequency noise in the PLL model. Since the loop functions as a high-pass filter for VCO noise, output noise due to the VCO is minimized by having the loop bandwidth as wide as possible [Smi]. Consequently, the requirement for fine frequency resolution is in conflict with the need for a wide loop bandwidth required to reduce settling time and to minimize the VCO noise contribution.

The maximum speed of programmable dividers places a limit on system performance. This can be overcome by using a fixed-modulus divider (prescaler) which is capable of gigahertz operation. The prescaler divides the output frequency by a fixed modulus M before it is applied to the programmable divider. However, this reduces the frequency resolution, since the output frequency can only be changed in increments of Mf_r .

There are several methods available to resolve the conflict between the need for fine frequency resolution and fast switching time. One technique uses a PLL synthesizer followed by a post-divider for increased frequency resolution, as illustrated in Figure 2.3 [Smi].

The output frequency is given by

$$f_o = \frac{Nf_r}{M} \quad (2.2)$$

Figure 2.3 PLL synthesizer followed by a post-divider

and the frequency resolution is

$$f = \frac{f_r}{M} \quad (2.3)$$

This is generally not a good solution since the VCO must operate at Mf_0 to obtain the required output frequency. Other techniques used to resolve the conflict between fast switching time and fine frequency resolution include multiple-loop synthesizers and fractional- N loops [Smi].

Although there are difficulties associated with the use of indirect synthesizers, PLLs are relatively inexpensive, and are suitable for a wide variety of applications including frequency modulation, demodulation, clock and carrier recovery, and frequency synthesis. Their power consumption is generally low. The integration of PLL components into a single chip realization has been reported [Kur], [Sun]. However, in most monolithic PLL implementations, loop filter components remain external to the integrated circuit.

2.2 Requirements for Monolithic High-Frequency VCOs

Small size and low power consumption are important parameters for modern mobile and hand-held transceivers. The VCO is an integral part of an indirect frequency synthesizer, and must conform to these requirements. Additional qualities of high performance VCOs include phase stability, wide tuning range, linearity of the modulation characteristic, high modulation sensitivity, and low cost. An oscillator which exhibits zero phase jitter of its output signal has perfect phase stability. VCO phase noise degrades the performance of the synthesizer outside the loop bandwidth. The modulation characteristic or modulation sensitivity is determined from the slope of the voltage-to-frequency transfer function of the VCO. Linearity of the modulation characteristic is critical for certain applications such as the use of the PLL as a modulator or frequency discriminator. Phase stability is desirable, but is usually obtained at the expense of the other VCO requirements [Gar]. The characteristics of the PLL are largely dependent on the performance of the VCO.

The trade-off between phase stability and other desirable VCO properties can be illustrated through the use of two examples. The first conflict occurs between the requirements for low phase noise and high modulation sensitivity. It will be shown in section 3.3.3.1 that phase noise can be considered as a process which results in phase modulation of the oscillator signal. A VCO with high modulation sensitivity will produce a large deviation

in its output frequency for a small change in its input voltage. This characteristic will result in increased susceptibility to phase modulation by a noise signal. A second conflict arises between the requirements for phase stability and wide tuning range. If a large tuning range is needed, multivibrators or relaxation oscillators are used. These circuits are usually characterized by high phase jitter. Circuits having a high quality factor (Q) such as crystal oscillators or LC oscillators can be used to obtain improved phase stability, but their tuning range is much lower.

2.2.1 Monolithic Implementation

In general, there are two classes of oscillator circuits; relaxation oscillators which charge and discharge a timing capacitor between two threshold voltage levels, and tuned oscillators which use LC circuits or crystals to set the frequency of oscillation.

Emitter-coupled multivibrators and ring oscillators are commonly used for integrated-circuit VCOs, examples of which are shown in Figure 2.4 [Kato]. The frequency of the R-C multivibrator is controlled by varying the charging current in the capacitor in response to the control input. The ring oscillator consists of an odd numbered ring of inverting stages connected back on itself. The frequency of oscillation is controlled by varying the gate delay in each inverter. Technologies used to implement these types of VCO include bipolar, CMOS, or NMOS. Frequencies of operation up to 7.4 GHz have been reported [SW]. Oscillators fabricated in GaAs process have been reported with speeds up to 17 GHz [Shi], but high cost of fabrication and considerable power consumption have prohibited their acceptance for integrated radio components. Until recently, limitations in silicon IC processing technology have precluded the use of on-chip inductors, and fully-integrated LC-tuned oscillators have not been realized.

Figure 2.4 Monolithic VCO implementations

2.3 A Comparison of VCO Techniques

Monolithic VCO architectures will be contrasted in terms of speed, power consumption, stability, noise characteristics, and fabrication technology.

2.3.1 Relaxation oscillators

Relaxation oscillators are the most prevalent configuration used in monolithic IC designs. They can be divided into three basic classifications: [Gre]

- 1) Emitter-coupled multivibrators
- 2) RC relaxation oscillators
- 3) Constant current charge-discharge oscillators

2.3.1.1 The Emitter-Coupled Multivibrator

The basic emitter-coupled multivibrator is shown in Figure 2.5 [Gre]. It is capable of high-frequency operation in the multigigahertz range [SW], and produces symmetrical output waveforms. The timing capacitor is alternately charged through Q_1 during one half-cycle, and through Q_2 during the other half-cycle. The voltage at the emitter of the on-transistor is clamped to $2V_{BE}$ below V_{CC} and the voltage at the emitter of the off-transistor ramps down linearly in a negative direction with a slope of I_1/C_1 for a total voltage swing of $2V_{BE}$ during each half-cycle.

The frequency of operation is given by

$$f_0 = \frac{I_1}{4C_1 V_{BE}} \quad (2.4)$$

This circuit has several features which make it a popular choice for integrated circuit designs [Gre]. It uses only npn transistors, and is capable of high-frequency operation; it can be implemented in a bipolar process which has only npn transistors available. This type of circuit exhibits the highest reported oscillation frequency (up to 7.4 GHz) [SW]. Output waveforms are symmetrical square-waves. Frequency control can be obtained by varying a control voltage or current.

Figure 2.5 Emitter-coupled multivibrator circuit

As indicated in equation 2.4, frequency is inversely proportional to transistor V_{BE} drop. At a constant collector current, V_{BE} varies at a rate of $-2 \text{ mV}/^\circ\text{C}$, resulting in a strong positive temperature coefficient of frequency. Techniques used to optimize temperature stability result in increased circuit complexity and a reduction of high-frequency capability [Gre]. Another problem inherent to this circuit is its susceptibility to timing jitter. The current in switching transistors Q_1 and Q_2 is non-linear, and the slope of these currents increases as the switching point is approached. Noise present in the current waveform will be amplified and will modulate the time at which the circuit switches, resulting in timing jitter [AM].

2.3.1.2 The R-C Relaxation Oscillator

An R-C relaxation oscillator is composed of timing elements R_1 , R_2 , and C_1 , a comparator with hysteresis (a Schmitt trigger), and a grounding switch (usually an npn transistor operated in switch mode) [Gre]. A simplified circuit using a single-comparator Schmitt trigger is shown in Figure 2.6. The output changes state when the input voltage reaches an upper switching threshold, and reverts back to the original state when the input reaches a lower switching threshold. With S_1 open, the voltage across the timing capacitor rises exponentially toward V_{CC} with time constant $\tau_1 = R_1 C_1$. With S_1 closed, the capacitor discharges

with time constant $\tau_2 = (R_1 || R_2)C_1$. The stability of this circuit is dependent on the accuracy and stability of the threshold levels for the Schmitt trigger [Gre]. The use of a dual-comparator Schmitt trigger results in some improvement in stability and high-frequency capability. At frequencies above a few hundred kilohertz, switching delays in the comparator and flip-flop sections will reduce the accuracy and stability of the oscillations [Gre], limiting the high-frequency capability of this circuit.

2.3.1.3 The Constant-Current Oscillator

The constant current oscillator is a variation of the R-C relaxation oscillator. Current sources are used to charge and discharge the timing capacitor. The basic circuit configuration is shown in Figure 2.7. C_1 is charged by the current source I_1 until the upper threshold of the Schmitt trigger is reached, at which time its output changes state and turns on current source I_2 , discharging C_1 . The operation repeats itself, producing a rectangular waveform at the output [Gre]. This circuit lacks the high-frequency capability of the emitter-coupled oscillator due to switching delays associated with the Schmitt trigger circuit.

2.3.1.4 CMOS Relaxation Oscillators

Where low power consumption and a higher level of integration are required, the use of CMOS technology offers an alternative to bipolar designs. Complementary devices can be used as active loads, replacing the collector resistors of the emitter-coupled multivibrator, and allowing higher values of voltage gain [Gre]. A simplified CMOS relaxation oscillator is shown in Figure 2.8 [FF]. Capacitor C_1 is charged by the current source I_1 and discharged by the current source I_2 .

Figure 2.6 R-C relaxation oscillator

Figure 2.7 Constant-current oscillator

Figure 2.8 CMOS relaxation oscillator

The maximum value of the output voltage is

$$V_{OH} = V_{DD} \frac{R_2}{(R_1 + R_2)} + I_2 \frac{R_1 R_2}{(R_1 + R_2)} \quad (2.5)$$

and its lowest value is

$$V_{OL} = V_{DD} \frac{R_2}{(R_1 + R_2)} \quad (2.6)$$

A number of CMOS relaxation oscillators have been described [Banu], [FL], [WA], [Th]; speeds approaching 1 GHz have been realized through the use of a high-speed charging scheme [Th]. These circuits exhibit wide tuning range, but tend to have poor linearity of the voltage-to-frequency transfer characteristic. The main disadvantage is poor temperature stability due to the temperature dependence of the transition voltage (at which the inverter output changes state) [Gre].

2.3.1.5 NMOS Relaxation Oscillators

An NMOS relaxation oscillator has been described which achieves 1.4 GHz maximum frequency. Device parasitics are used as the timing elements. A constant-current charge-discharge block and a signal-reversing feedback block are combined to produce a high-frequency relaxation oscillator [Banu]. Power consumption of NMOS oscillators is somewhat higher than CMOS.

2.3.2 Ring Oscillators

A number of ring oscillators have been reported using CMOS or NMOS technology [Th], [EA], [Ware], [SA]. The maximum reported frequency for a CMOS ring oscillator is 920 MHz [Th]; a 2.5 GHz ring oscillator has been reported using 1 μm NMOS technology [SA]. The tuning range of these circuits tends to be somewhat less than the previously described relaxation oscillators, they exhibit poor control linearity, and are sensitive to process variations [FL]. Centre frequency temperature-sensitivity is also a problem with these circuits [Ware]. The phase noise performance of ring oscillators tends to be poorer than other relaxation oscillator designs [Th].

2.3.3 Crystal Oscillators

Crystal oscillators are characterized by excellent time and temperature stability, due to the high-Q nature of quartz crystals. Q values are typically in excess of tens of thousands, resulting in very narrow tuning range. For these reasons, crystal oscillators have lower phase noise than other types.

The greatest disadvantage of crystal oscillators is that piezoelectric crystals are not compatible with silicon IC technology. They are relatively expensive, and resonant frequencies are limited to a few hundred MHz. Their switching speed is too slow for radio applications. For these reasons, they are not suited for high-frequency monolithic VCO designs.

2.3.4 LC-Tuned Oscillators

LC sinusoidal oscillators exhibit high frequency-stability, insensitivity to temperature-drift of the centre frequency, low phase noise or jitter, and high-frequency capability. Until recently, the frequency selective circuit elements, LC-tank circuits, have remained external to the monolithic integrated circuit.

Tuned oscillators are composed of two main circuit blocks, a feedback network which includes the LC tuning elements, and an amplifier which supplies the required signal gain. A simplified block diagram of a feedback oscillator is shown in Figure 2.9. The gain required to sustain oscillations is provided by the gain block $A(j\omega)$. The purpose of the feedback network $H(j\omega)$ is to provide frequency-selective circuits so that the frequency of oscillation can be controlled. It also provides the necessary phase shift so that the output signal is in phase with the input signal. The basic feedback oscillator without bias circuits is shown in Figure 2.10 [Smi]. The open-loop gain must be greater than unity at start-up, and the feedback network must provide an effective phase shift of 0° around the loop. The conditions required to sustain oscillations are called Barkhausen criteria [Gre].

The most commonly used tuned oscillator circuits are shown in Figure 2.11 [Smi]. The Colpitts oscillator of Figure 2.11 (a) has a frequency of oscillation given by

$$f_0 = \frac{1}{2\pi\sqrt{L_3\left(\frac{1}{C_1} + \frac{1}{C_2}\right)}} \quad (2.7)$$

Figure 2.9 Feedback oscillator block diagram

Figure 2.10 Basic feedback oscillator circuit

The Hartley oscillator of Figure 2.11 (b) has a frequency of oscillation given by

$$f_0 = \frac{1}{2\pi} \sqrt{\frac{1}{C_3 (L_1 + L_2)}} \quad (2.8)$$

Figure 2.11 Tuned oscillator circuits (a) Colpitts oscillator (b) Hartley oscillator

The most frequently used rf oscillator in radio receivers is the Clapp oscillator, which is a variation of the Colpitts oscillator. Frequency selection can be accomplished by tuning a variable capacitor, which can be replaced by a varactor to provide electronic tuning.

In general, tuned oscillators offer better noise performance, frequency stability, and linearity than relaxation oscillators. However, their tuning range is not as large, and until recently, the integration of inductors on silicon has not been possible.

2.4 A Summary of Current VCO Design

Table 2.1 presents a summary of recent VCOs realized in silicon monolithic form. Highest operating frequencies have been achieved using bipolar technology. Lowest reported power consumption is achieved by a CMOS implementation. The largest tuning range is reported for a bipolar emitter-coupled multivibrator [SW].

In the preceding discussion it has been mentioned that CMOS and bipolar multivibrators and ring oscillators are the most popular architectures for integrated-circuit VCO designs. However, there are restrictions associated with their use in high-speed, low-noise designs. Implementations using CMOS technology are limited to speeds at or below 1 GHz. Bipolar multivibrators are capable of multi-gigahertz operation, but suffer from temperature-sensitivity. Relaxation oscillators are susceptible to timing jitter, regardless of the technology used.

It is expected that monolithic LC-tuned VCOs will offer an alternative to current integrated circuit designs. LC oscillators typically have high spectral purity, temperature stability, and are capable of operation at frequencies above 1 GHz. Meeting the requirements for high-quality VCOs, particularly low phase noise, presents a significant challenge for integrated circuit designers.

Table 2.1 Summary of monolithic VCOs

Technology	Oscillator Type	f_T or gate length	Tuning Range	Power (mW)	Phase Noise	Temperature Stability	Reported by
NMOS	Multi-vibrator	0.75 μm	80 kHz to 1.4 GHz	50	-	-	Banu '88
	Ring oscillator	1.0 μm	1.5 to 2.5 GHz	-	-	-	Syed and Abidi '86
CMOS	Ring oscillator	1.0 μm	225 to 325 MHz	-	-	-	Enam and Abidi '90
		2.0 μm	112 to 209 MHz	-	-	400 ppm/ $^{\circ}\text{C}$	Ware et al '89
		1.2 μm	320 to 926 MHz	9.4	-83 dBc/Hz @ 100 kHz offset	-	Thamsiri-anunt '93
	Multi-vibrator	1.2 μm	1 to 80 MHz	20	< 160 ppm	90 ppm/ $^{\circ}\text{C}$	Flynn and Lidholm '92
BiCMOS	Multi-vibrator	2.0 μm	1 to 128 MHz	100	-	50 ppm/ $^{\circ}\text{C}$	Kato et al '88
		9 GHz	3 to 90 MHz	-	-	-	Kurita et al '91
Bipolar	Multi-vibrator	0.8 μm	1.99 to 7.4 GHz	70	-	1.1% 0 to 100 $^{\circ}\text{C}$	Soyuer and Warnock '92
		10 GHz	1 MHz to 1 GHz	65	-	-11000 ppm/ $^{\circ}\text{C}$	Wu '90
		3 GHz	to 500 MHz	-	-121 dBc/Hz @ 1 MHz offset	-	Verhoeven '92
		2.0 μm	50 to 250 MHz	220	-	-220 ppm/ $^{\circ}\text{C}$	Liu and Meyer '90
		3 GHz	85 to 150 MHz	48	-97 dBc/Hz @ 100 kHz offset	-1000 ppm/ $^{\circ}\text{C}$	Sneep and Verhoeven '90
	LC oscillator	10 GHz	1.68 to 1.86 GHz	70	-88 dBc/Hz @ 100 kHz offset	1.5% -40 to 85 $^{\circ}\text{C}$	Nguyen and Meyer '92

Chapter 3

Design Considerations

For a number of years planar inductors have been realized on ceramic or sapphire substrates, and in GaAs ICs. In the early development of silicon ICs, inductors implemented on silicon were characterized by low Q , low operating frequencies, and excessive chip-area consumption. These restrictions were due to lithographic limitations and poor isolation from the silicon substrate.

Recent advances in silicon IC processing technology have led to the fabrication of planar inductors with improved characteristics. Metal width and pitch in the low micrometer range allow many more inductor turns per unit area. Oxide-isolated silicon processes with multi-layer metal options allow thick oxides which help isolate the inductor from the silicon substrate. These advances have made possible the realization of planar inductors on a silicon substrate with usable Q values (from 3 to 8) [NM2]. This has facilitated the construction of monolithic LC sinusoidal oscillators which operate in the GHz frequency range. It is expected that the use of on-chip inductors with reasonable Q values will result in voltage-controlled oscillators with good high-frequency stability and phase noise performance. Due to area constraints, the size of realizable L and C elements limits the lowest operating frequencies of these circuits to a few hundred MHz. The highest operating frequencies are limited to about 2 GHz due to the f_T of the active devices (approximately 10 GHz for the BATMOS process).

Methods of sinewave oscillator analysis and the basic criteria for oscillation will be presented in this chapter. Models used for ac circuit analysis will be developed as a means of predicting the behaviour of the proposed circuit and to aid in the design process. The sources of oscillator noise will be considered, and the development of models to describe oscillator phase noise will be presented.

3.1 Conditions for Oscillation

Oscillator circuits are essentially feedback networks. A harmonic oscillator generates a sinusoidal output, and contains an amplifier which provides gain, and a feedback network containing a tuned circuit which determines the frequency of oscillation. Oscillators are inherently non-linear circuits [Smi], but linear circuit analysis may be used as a starting point in the design process. This technique can be used to predict the frequency of oscillation, but may not be particularly useful in predicting characteristics such as power output, spectral purity, frequency stability, and sensitivity to temperature and power supply variations [KBR].

3.1.1 Stability Criteria

The block diagram of a tuned oscillator circuit is shown in Figure 3.1 as a starting point in the analysis. An amplifier provides frequency-dependent forward loop gain $A(j\omega)$, and a feedback network $H(j\omega)$ provides phase shift such that the output is in phase with the input at a single frequency.

The closed-loop transfer function is given by

$$\frac{V_{OUT}}{V_{IN}} = \frac{A(j\omega)}{1 - A(j\omega)H(j\omega)} \quad (3.1)$$

Figure 3.1 Tuned oscillator block diagram.

Figure 3.2 (a) Grounded-base oscillator circuit (b) Small-signal equivalent circuit

The system will oscillate provided that $A(j\omega)\beta(j\omega) = 1$. This implies that oscillation will occur if the open-loop gain is unity and the total phase shift around the loop is 0° at the frequency of oscillation [Smi].

Figure 3.2 shows a basic Colpitts oscillator circuit and its small signal equivalent circuit. The base is considered to be at ground potential due to the large value of C_B .

To calculate the open-loop gain, it is necessary to open the feedback loop at some point, apply a signal, and measure the return signal. If the loop is opened at the transistor emitter, and the circuit modified for simplicity, the circuit of Figure 3.3 results. This is the small-signal equivalent of the open-loop circuit. The terminating impedance is the input resistance of the common-base circuit, $r_i = r_\pi / \beta$, in parallel with the emitter resistor R_E . The resistance shunting C_2 is $R_E || r_i$, and can be replaced by an equivalent resistance R_{eq} shunt-

ing C_1 and C_2 due to the capacitive transformer formed by C_1 and C_2 . The equivalent resistance reflected across the coil is given by

$$R_{eq} = \frac{r_i R_E}{r_i + R_E} \left(\frac{C_1 + C_2}{C_1} \right)^2 \quad (3.2)$$

For complex frequency s , the expression for the open-loop forward gain is given by

$$G(s) = \frac{g_m s \frac{1}{C}}{s^2 + s \left(\frac{1}{(R_{eq} \parallel R_L)C} + \frac{1}{LC} \right)} \quad (3.3)$$

where

$$C = \frac{C_1 C_2}{C_1 + C_2} \quad (3.4)$$

One of the criteria for oscillation is that the phase shift of the load impedance must be zero. This occurs at the resonant frequency, which is given by

$$\omega_0 = \frac{1}{\sqrt{L \frac{C_1 C_2}{C_1 + C_2}}} \quad (3.5)$$

Figure 3.3 Open-loop small-signal equivalent circuit

With sufficient loop gain, a pair of right-half plane poles occur, and oscillations will build up. In a practical implementation, the loop gain is chosen to be about 3, which ensures reliable oscillation start-up. The circuit is unstable for a loop gain greater than 1, and oscillations will increase in amplitude until the transistor current saturates, reducing its β and g_m . This limits the amplitude of oscillation until the loop gain averaged over each cycle is unity.

An alternate method of analysis involves obtaining the closed-loop transfer function of the small-signal equivalent of the oscillator circuit. The small-signal equivalent circuit of Figure 3.2(b) is repeated here in Figure 3.4. A small noise current I has been applied to one of the nodes.

The resulting node-current equations are

$$sL_1 I = \left(-s^2 L_1 C_1 - sL_1 g_m \right) V + \left(s^2 L_1 C_1 + s \frac{L_1}{R_L} + 1 \right) V_{OUT} \quad (3.6)$$

and

$$\left(s(C_1 + C_2) + \frac{1}{R_{eq}} + g_m \right) V - sC_1 V_{OUT} = 0 \quad (3.7)$$

Figure 3.4 Small-signal equivalent circuit of a grounded-base Colpitts oscillator

where

$$R_{eq} = \frac{r_{\pi} R_E}{r_{\pi} + R_E} \quad (3.8)$$

These expressions can be manipulated using matrix algebra to yield expressions for the poles and zeros of the circuit. The poles of the system can be found by solving the equation

$$s^3 LC_1 C_2 + s^2 \frac{LC_1}{R_{eq}} + s \left(C_1 + C_2 + \frac{L}{R_{eq} R} + g_m \frac{L}{R} \right) + \frac{1}{R_{eq}} + g_m = 0 \quad (3.9)$$

Zeros of the system are given by the expression

$$s^2 LC_1 = 0 \quad (3.10)$$

The complete transfer function is given by

$$H(s) = \frac{s^2 LC_1}{s^3 LC_1 C_2 + s^2 \frac{LC_1}{R_{eq}} + s \left(C_1 + C_2 + \frac{L}{R_{eq} R} + g_m \frac{L}{R} \right) + \frac{1}{R_{eq}} + g_m} \quad (3.11)$$

The root-locus plot of Figure 3.5 was obtained from (3.9), and the closed-loop magnitude and phase responses of Figure 3.6 were obtained from (3.11). The magnitude and phase responses were obtained using reduced g_m . It can be shown that the frequency at which the peak of the magnitude response occurs will coincide with a complex pole-pair which lies on the $j\omega$ axis. The quantity g_m was swept to obtain the root-locus plot of the dominant pole-pair. The value at which poles lie on the $j\omega$ axis corresponds to the reduced value of g_m which results in a reduction of the loop gain and a stable oscillating amplitude.

The above methods of oscillator analysis can be used as a basis for the design and analysis of the proposed oscillator structure.

Figure 3.5 Root locus plot of the Colpitts oscillator

Figure 3.6 Magnitude and phase response of the Colpitts oscillator

3.2 LC VCO Circuit Configuration

The principal objective of this work is to design and construct a monolithic LC voltage-controlled oscillator. While varactors may be used for tuning, at the time that the proposed oscillator design was initiated, varactors on silicon were not available. Since then, oscillators have been designed using on-chip varactors to provide a means of frequency control [Dau]. The use of varactors would allow the use of Clapp voltage-controlled oscillators. The tuned oscillator circuit can be modified to provide a means of electronic tuning by replacing one of the capacitors by a varactor, resulting in a VCO. Figure 3.7 shows a Clapp oscillator using a varactor diode D_1 for tuning [KBR].

The structure described by Nguyen and Meyer in [NM1] which uses characteristics inherent in the circuit configuration for frequency tuning was used to initiate the design of the VCO. A simplified schematic of the core circuit of the VCO is shown in Figure 3.8. The inductors are formed as square metal spirals on an insulating layer of silicon oxide. The circuit is essentially a Gilbert cell containing two LC-tuned circuits with different resonant frequencies. Feedback is applied to each tuned circuit using a capacitive divider. The fraction of bias current driving Q_1 or Q_4 is controlled by voltages V_{C1} and V_{C2} . This varies the frequency of oscillation between the resonant frequency of the left resonator to that of the right resonator.

Figure 3.7 Clapp voltage-controlled oscillator

Figure 3.8 Simplified oscillator schematic

If the loop is broken at the common-emitter node of transistors Q_5 and Q_6 , a test signal can be applied, which will traverse through the loop and return to the common-emitter node. Signals traversing the left and right loops are added due to the summing property of the emitter-coupled pair [NM1].

The equivalent circuit of the left feedback loop is illustrated in Figure 3.9, and is used to derive the loop gain $H_1(s)$. The resistance R_1 represents the series to parallel transformation of the series resistance of the coil L_1 . Similarly, the loop gain of the right feedback loop can be represented by $H_2(s)$. The equivalent circuit of the left loop can be combined with that of the right loop to form the small-signal equivalent of the complete circuit. The common part of H_1 and H_2 is the differential pair composed of Q_5 and Q_6 , with H_1 and H_2 applied to the bases. Thus, the Q_5 - Q_6 differential pair act to combine the two loops. The fractions of bias current applied to transistors Q_1 and Q_4 are represented by n_1 and n_2 , such that $n_1 + n_2 = 1$.

Figure 3.9 Equivalent circuit of left feedback loop

The open-loop gain of the complete circuit is

$$H(s) = n_1 H_1(s) + n_2 H_2(s) \quad (3.12)$$

This model assumes that the base of transistor Q_5 is grounded, which is not the case in the actual circuit. The actual differential pair results in interaction between the two feedback paths through the emitters, as well as two C_π s in series, which are connected between the bases of the two transistors.

A more realistic model which includes the interaction between the two feedback paths is shown in Figure 3.10. The fractions of bias current $I_{\text{bias}}/2$ that drive Q_1 and Q_4 are denoted by K , where K is a number between 0 and 1. If $K=1$, the left circuit is fully turned on while the right circuit is completely turned off; if $K=0$, the reverse situation holds. The coefficients K_1 and K_2 represent capacitive dividers such that

$$K_1 = \frac{C_3 \frac{g_m}{2}}{C_3 + \frac{C_\pi}{2} + C_6}, \quad \text{and} \quad K_2 = \frac{C_4 \frac{g_m}{2}}{C_4 + \frac{C_\pi}{2} + C_6} \quad (3.13)$$

Figure 3.10 A more realistic small-signal equivalent circuit

Capacitors C_x and C_y are defined by

$$C_x = C_1 + \frac{C_3 \left(\frac{C_\pi}{2} + C_6 \right)}{C_3 + \frac{C_\pi}{2} + C_6}, \quad \text{and} \quad C_y = C_2 + \frac{C_4 \left(\frac{C_\pi}{2} + C_5 \right)}{C_4 + \frac{C_\pi}{2} + C_5} \quad (3.13)$$

This model accounts for the emitter coupling of Q_5 and Q_6 but not for capacitive coupling. Analysis shows that a capacitance equal to $C_\pi/2$ is connected between the bases of transistors Q_5 and Q_6 . An equivalent circuit with the required changes is shown in Figure 3.11.

The transfer function is complex so it will not be written explicitly; matrix manipulation using MATLAB is used to find the poles and zeros of the system. Root-locus plots as a function of g_m can now be constructed using MATLAB.

Component Values:

$$\begin{array}{llllll} L_1=6.43 \text{ nH} & C_1=0.2 \text{ pF} & C_3=1 \text{ pF} & C_5=2.5 \text{ pF} & C_\pi/2=2 \text{ pF} & R_2=179 \text{ } \Omega \\ L_2=3.55 \text{ nH} & C_2=20 \text{ fF} & C_4=2 \text{ pF} & C_6=3 \text{ pF} & R_1=303 \text{ } \Omega & \end{array}$$

Figure 3.11 Small-signal equivalent circuit of the LC VCO

Figures 3.12 (a) to (c) show the root-locus for various K -values as the value of g_m is swept. If the circuit functions as an oscillator, the small-signal g_m would be of an appropriate value to place the poles in the right-half plane. In this case, oscillation will build up until non-linearity reduces the effective value of g_m to g_{meff} . For $K > 0.5$, oscillation is determined mainly by the left feedback loop, while for $K < 0.5$, oscillation is determined by the right feedback loop [NM1]. The frequency of oscillation can be predicted at the point where poles lie on the $j\omega$ -axis. The magnitude and phase responses for $K=1$ are plotted in Figure 3.13. An examination of the magnitude response obtained using the large-signal value g_{meff} , demonstrates that infinite gain occurs at the resonant frequency. This is in agreement with theory which predicts that at the resonant frequency, and with a loop gain greater than one, the system will be unstable and oscillations will increase in amplitude until some limiting non-linearity reduces the gain [Smi].

The magnitude response exhibits a maximum value at the zero-phase frequency. This satisfies the oscillation criteria $\text{Ph}[H(j\omega)] = 0$ and $\text{Mag}[H(j\omega)] > 1$. Reliable oscillation occurs at the zero-phase frequency of the dominant pole [NM1].

Figure 3.12 (a) Root locus plot for $K=1$

Figure 3.12 (b) Root locus for $K=0.5$ Figure 3.12 (c) Root locus for $K=0$

Figure 3.13 Magnitude and phase responses with poles on the $j\omega$ axis

Open loop magnitude and phase responses for $K=1$ and $K=0$ are plotted in Figures 3.14 (a) and (b). A number of curves are displayed as g_m is swept from its small-signal value to its large-signal value $g_{m\text{eff}}$. Using the small-signal values of g_m , loop gains of 2.7 at $K=1$ and 1.9 at $K=0$ are predicted, and are reduced to a magnitude of 1 at $g_{m\text{eff}}$. A minimum frequency of 1.976 GHz and a maximum frequency of 2.413 GHz are predicted from the results of open loop analysis. This result is in close agreement with closed loop analysis which predicts a minimum frequency of 1.971 GHz and a maximum frequency of 2.411 GHz. Further examination of these plots reveals that a small variation in phase can result in a large shift in frequency. This effect becomes worse as frequency increases. For example, a phase variation of 10° can result in a frequency shift of 45.6 MHz at 1.98 GHz, while the same phase variation can result in a frequency shift of 84.8 MHz at 2.41 GHz.

Figure 3.14 (a) Open loop magnitude and phase responses for $K=1$

Figure 3.14 (b) Open loop magnitude and phase responses for $K=0$

Multiple modes of oscillation occur when the phase response crosses zero at multiple frequencies [NM1]. This can occur if the tank circuit Q is too high, or if the tank circuit resonant frequencies are too widely separated. MATLAB simulations were used to reproduce multi-oscillation for both of these situations. The effect of increasing Q from its nominal value of 5 to a value of 50 is illustrated in the magnitude and phase responses of Figure 3.15 (a). An examination of root locus plot of Figure 3.15 (b), which illustrates the effect of Q -increase, reveals more than one natural frequency in the right-half plane. In [NM1] it is shown that multi-oscillation occurs as tank circuit Q is reduced, which is accompanied by increased tuning bandwidth. The separation of resonant frequencies beyond the allowable tuning range was accomplished by adjusting component values. The effect of increasing the separation from 385 MHz to 830 MHz is shown in Figures 3.16 (a) and (b). Results of SPICE simulations indicate that as Q is increased, it is not possible to achieve as wide a tuning range. Beyond a certain Q , each resonant circuit causes a large phase shift and multi-oscillation occurs, which cannot be avoided even with very little separation between the resonant frequencies. These results indicate a trade-off between high tank-circuit Q and wide tuning range.

Figure 3.15 (a) Multiple modes of oscillation due to a high- Q circuit

Figure 3.15 (b) Root locus due to a high-Q circuit

Figure 3.16 (a) Multi-oscillation due to increased separation of resonant frequencies

Figure 3.16 (b) Root locus plot illustrating multi-oscillation due to increased separation

3.3 Oscillator Phase Noise

An ideal oscillator will produce a pure carrier signal which exhibits zero phase jitter and frequency drift. Its output signal displayed on a spectrum analyzer would appear as a single vertical spike at the frequency of oscillation. If the frequency-determining components of the oscillator are absolutely stable, the oscillator will have no frequency drift but will still have phase noise [Und]. Phase noise can be thought of as short-term instabilities in the phase of a signal [Poole]. This produces noise sidebands which are symmetrically distributed on either side of the oscillator signal at frequencies which are offset from the carrier. The resulting power spectral density displayed on a spectrum analyzer will appear as illustrated Figure 3.17. The value of the phase noise is the noise power per Hertz at some frequency in one of the sidebands and is taken as a fraction of the total carrier power, and is usually measured in dBc/Hz [Und].

3.3.1 Sources of Oscillator Noise

Before examining the noise mechanisms present in the VCO, it is useful to explore the various sources of electronic noise arising in bipolar transistors and resistors.

Figure 3.17 Spectrum analyzer display of oscillator sidebands

3.3.1.1 Sources of Noise

Thermal noise is due to the random thermal motion of electrons in a resistor, and is directly proportional to temperature. It is unaffected by the presence or absence of direct current. Thermal noise can be represented by a voltage generator $\overline{v^2}$ in series with a noiseless resistor R , or a current generator $\overline{i^2}$ in parallel with a noiseless resistor R , as in Figure 3.18 [GM].

These thermal noise generators are given by

$$\overline{v^2} = 4kTR\Delta f \quad (3.15)$$

Figure 3.18 Equivalent representations of thermal noise

and

$$\overline{i^2} = 4kT \frac{I}{R} \Delta f \quad (3.16)$$

where k is Boltzmann's constant and Δf is the bandwidth in hertz.

Shot noise is caused by the random fluctuation of charge carriers crossing a semiconductor junction. It is present in diodes and bipolar transistors, and is associated with direct current I . If the fluctuation in I has an average value I_D , then the resulting noise current has a mean-square value

$$\overline{i^2} = 2qI_D \Delta f \quad (3.17)$$

where q is the electron charge, and Δf is the bandwidth in hertz.

Since both shot and thermal noise are independent of frequency, each has a uniform power spectral density. Noise having a flat frequency spectrum is often called white noise [GM].

Flicker noise is a low-frequency phenomenon, and occurs in all active devices and some passive elements such as carbon resistors. In bipolar transistors, flicker noise is caused mainly by traps associated with contamination and crystal defects in the emitter-base depletion layer. These traps capture and release carriers in a random fashion and give rise to a noise signal with energies concentrated at low frequencies [GM]. It is associated with direct current flow and is represented by a noise current source

$$\overline{i^2} = K_1 \frac{I^a}{f^b} \Delta f \quad (3.18)$$

where Δf is a small bandwidth in hertz, I is direct current, K_1 is a constant for the particular device, a is a constant in the range 0.5 to 2, and b is a constant approximately equal to unity [GM]. If $b=1$ in equation (3.18), then the noise spectral density has a $1/f$ frequency dependence, as shown in Figure 3.19.

Figure 3.19 Flicker noise power spectral density

Burst noise is another source of low-frequency noise, and occurs in integrated circuits and discrete transistors. It has been shown to be related to the presence of heavy-metal ion contamination [GM]. The spectral density of burst noise is given by

$$\overline{i^2} = K_2 \frac{I^c}{1 + \left(\frac{f}{f_c}\right)^2} \Delta f \quad (3.19)$$

where K_2 is a constant for the device, I is direct current, c is a constant from 0.5 to 2, and f_c is a particular frequency for a given noise process. Burst noise can occur with multiple time constants, giving rise to multiple humps in the spectrum [GM].

3.3.1.2 Bipolar Transistor Noise Model

The noise sources described in the previous section can now be combined to form a model for noise occurring in a transistor. The small-signal equivalent circuit of a bipolar transistor (BJT), including noise sources is shown in Figure 3.20 [GM]. Bipolar transistor noise sources are given by the following expressions:

$$\overline{v_b^2} = 4kTr_b\Delta f \quad (3.20)$$

Figure 3.20 Bipolar transistor small-signal equivalent circuit with noise sources

$$\overline{i_c^2} = 2qI_C\Delta f \quad (3.21)$$

$$\overline{i_b^2} = 2qI_B\Delta f + K_1 \frac{I_B^a}{f} \Delta f + K_2 \frac{I_B^c}{1 + \left(\frac{f}{f_c}\right)^2} \Delta f \quad (3.22)$$

Thermal noise in the base-spreading resistor r_b is given by (3.20). The collector current exhibits full shot noise, and is represented by the noise current generator $\overline{i_c^2}$ in (3.21). Shot noise, flicker noise, and burst noise are represented by the noise current generator $\overline{i_b^2}$ in (3.22). The input-referred noise voltage spectral density including flicker, shot, and thermal noise has been simulated, and is plotted in Figure 3.21.

Frequency f_o is the point at which the shot and thermal noise asymptote meets the flicker noise asymptote, and is called the flicker noise corner frequency. The input-referred noise rises at high frequencies due to collector current noise referred to the input. This input-referred noise rises as f^2 at high frequencies because the transistor current gain begins to fall. Frequency f_b is the point at which the high-frequency asymptote meets the shot and thermal noise asymptote [GM].

Figure 3.21 Bipolar transistor input-referred noise voltage spectral density

3.3.1.3 Oscillator Noise

Noise arises in oscillators from the various noise sources in the oscillator circuit, which can include thermal noise from resistors and lossy elements, and shot, burst, and $1/f$ noise from BJTs. Noise sources contribute to phase noise by direct up conversion of noise from baseband to the oscillation frequency due to non-linearities in the oscillator circuit [How]. At large frequency offsets from the carrier, shot noise and thermal noise contribute to a flat frequency spectrum [GM]. White noise is largely dependent on the noise figure of the oscillator and associated amplifiers. Closer to the carrier, the noise spectrum rises due to low-frequency noise, such as flicker noise and burst noise, and due to the resonant circuit. In addition, thermal noise and shot noise present in amplifiers following the oscillator circuit will increase the level of the noise floor. The oscillator noise mechanism will be discussed in detail in later sections.

3.3.2 Effect of VCO Noise on System Performance

Since a voltage-controlled oscillator is typically used as a phase-locked loop component, it is useful to examine the effect of VCO noise on the loop output. A block diagram of a basic phase-locked loop is shown in Figure 3.22 to illustrate the effect of noise from different parts of the loop. Noise from the reference and from the VCO will be used as examples.

The reference signal with its noise enters the phase detector, and noise from the reference signal appearing at the output of the detector will enter the loop filter. Noise from the reference within the loop bandwidth will not be attenuated, and will appear at the VCO control input and cause modulation of its output signal, so reference noise will only appear on the output if it is within the loop bandwidth.

Noise generated by the VCO will pass through the loop filter if it is within the loop bandwidth, but the error signal at the control input will act to reduce VCO phase noise. However, VCO noise outside the loop bandwidth will remain unaltered [Poole].

Figure 3.22 Phase-locked loop block diagram

The impact of VCO phase noise on system performance will depend on the application. Two examples will be given to illustrate the consequences of excessive phase noise on the performance of modern communications systems. In the first case, excessive phase noise can increase the bit error rate (BER) of digital communications systems, especially those using phase modulation techniques such as binary-phase-shift keying (BPSK) and quadrature-phase-shift keying (QPSK). Since oscillator noise power is concentrated close to the carrier due to $1/f$ noise, this can cause significant phase deviation, resulting in degradation of the BER [Hid]. The second situation can occur in a receiver. The local oscillator phase noise can mix with an unwanted signal to create an unwanted signal in the IF passband. Phase noise is one of the limiting factors in determining the spacing of communication channels [Smi].

The preceding discussion has emphasized the importance of phase noise reduction, and underscores the necessity for accurate modeling of phase noise so that oscillators can be designed efficiently with predictable characteristics.

3.3.3 Methods of Phase Noise Analysis

Three methods are used to characterize the phase noise mechanism present in the LC VCO. For each of these methods, a model is developed to represent the phase noise process, and the simulation of the VCO phase noise based on these models is undertaken. For a simple second-order system, models for phase noise in oscillators are well documented. A number of problems are encountered in describing the phase noise of higher order systems; the adaptation of traditional methods to characterize higher order oscillators presents a significant challenge. Simulation of phase noise presents additional difficulties.

3.3.3.1 A Noise Model Based on Phase Modulation of the Oscillator Signal

Phase noise can be considered as a process which results in phase modulation of the oscillator signal. The relationship between the power spectral density S_θ and phase noise $\theta(t)$ must be found to develop an oscillator noise model [Lee].

The output signal of an oscillator $S(t)$ can be expressed by the equation

$$S(t) = V(t) \cos(\omega_0 t + \theta(t)) \quad (3.23)$$

where $V(t)$ is the amplitude variation and $\theta(t)$ is the phase variation of the noise. Since high-quality oscillators are amplitude stable, $V(t)$ can be considered constant, and all oscillator noise is due to $\theta(t)$.

The expression for a carrier signal of amplitude V which is frequency modulated by a sine wave of frequency f_m is given by

$$S(t) = V \cos \left(\omega_0 t + \frac{ak_f}{f_m} \sin \omega_m t \right) \quad (3.24)$$

where ak_f/f_m is the peak phase deviation, a represents the peak amplitude of the noise at a specific frequency, k_f is the voltage to frequency transfer characteristic of the VCO, and f_m is the frequency of the disturbance. This expression can be expanded to give

$$S(t) = V \left(\cos(\omega_0 t) \cos \left(\frac{ak_f}{f_m} \sin(\omega_m t) \right) - \sin(\omega_0 t) \sin \left(\frac{ak_f}{f_m} \sin(\omega_m t) \right) \right) \quad (3.25)$$

If the peak phase deviation is small, ($ak_f/f_m \ll 1$) the expression for $S(t)$ is given by

$$S(t) = V \left(\cos(\omega_0 t) - \frac{ak_f}{2f_m} (\cos(\omega_0 + \omega_m)t - \cos(\omega_0 - \omega_m)t) \right) \quad (3.26)$$

For small peak phase deviation, frequency components with amplitude $Vak_f/2f_m$ are formed on each side of the carrier at frequencies $f_0 \pm f_m$. The ratio of peak sideband voltage V_n to peak carrier voltage V is [Smi]

$$\frac{V_n}{V} = \frac{ak_f}{2f_m} \quad (3.27)$$

and the ratio of noise-to-carrier power is

$$\left(\frac{V_n}{V} \right)^2 = \left(\frac{ak_f}{2f_m} \right)^2 \quad (3.28)$$

This expression represents the power in a single sideband. This result can be extended to obtain an expression for the oscillator noise-power spectral density. If the normalized power spectral density is constant over a unit bandwidth, then the power in that bandwidth is [Smi]

$$S_{\theta}(f_m) = \int_{f_m - 1/2}^{f_m + 1/2} P_{\theta}(f) df = P_{\theta}(f_m) \quad (3.29)$$

Since $P_{\theta}(f)$ is symmetrical about the carrier frequency, the resulting double-sided noise power spectral density is

$$S_{\theta}(f_m) = 2P_{\theta}(f_m) = \frac{1}{2} \left(\frac{ak_f}{f_m} \right)^2 \quad (3.30)$$

where ak_f/f_m is the peak value of the phase modulation. $S_{\theta}(f)$ is the ratio of the power in the unit bandwidth centered at f_m to the carrier power [Smi].

The preceding model for oscillator noise was used as a basis for the simulation of phase noise of the LC VCO. A noise source at a single frequency can be injected at some point in the circuit (at the base of a transistor) and a SPICE transient analysis performed. The output file generated by SPICE can then be imported into MATLAB and an FFT performed to obtain the output spectrum of the carrier plus noise. If the input-referred noise due to each transistor in the oscillator core circuit is applied to the appropriate point in the circuit, the output noise can be predicted by summing the contributions due to the individual noise sources. There are several restrictions associated with the use of this method which limit its suitability for oscillator noise analysis.

The complete oscillator circuit is simulated in SPICE using time domain analysis. The time step used in the transient analysis must be sufficiently small in order to get an accurate representation of the output frequency. The output frequency calculated from the simulation depends on the size of the time step. It was found that the time step should be no more than 1/100th of the period of the oscillation for consistent, accurate results. For instance, a time step of 10 pS is required to get an accurate analysis for an oscillator at 1 GHz.

To avoid the need for windowing, the frequency of the noise source is set at a submultiple of the carrier by some power of two, and the total simulation time is set to an exact multiple of the low frequency period. Simulation of close-to-carrier phase noise requires the injection of a relatively low-frequency noise source. For this application, thirty-two cycles of the low-frequency component were used to produce a frequency resolution of $1/32$ of the injected frequency at the carrier. Injection of noise caused a slight but unpredictable frequency shift. Using more points allowed enough frequency resolution to follow these shifts. Variation of the modulating frequency caused shifts in the centre frequency, resulting in components not in the centre of frequency bins. If less than thirty-two cycles are used a coarse plot results, as shown in Figure 3.23. The resolution is set by the total time, and the size of the time step sets the accuracy of the carrier frequency. Due to computer memory limitations the minimum injected frequency is restricted to about 6 MHz for a 1 GHz oscillator and simulation runs in excess of two hours are required. For example, for an 826.446 MHz oscillator with a noise frequency of 6.456612 MHz, the number of points required is:

$$32 \times 128 \times 826.446 / 6.456612 = 524,288 \text{ points}$$

Initially decimation was performed to move the carrier to a lower frequency (approximately 8 MHz). This involved multiplying the signal with a sinewave to mix to a lower frequency, and then filtering out the high-frequency components, and plotting the shifted spectrum in MATLAB. This approach was eventually rejected, since more accurate plots could be obtained without using frequency multiplication.

Plots of the output spectrum were obtained from the Fourier transform, showing the centre frequency and sidebands equally spaced by f_m . A noise amplitude of at least 5 mV is used to produce recognizable sidebands. This is illustrated in Figure 3.24. This is not realistic for noise amplitudes in the nanovolt range predicted by SPICE noise analysis, and therefore the sideband amplitudes must be scaled. The result of the analysis using the scaled noise amplitude predicts phase noise will be -150 dBc/Hz at 10 MHz offset from the carrier.

Since it is only possible to predict phase noise at a single frequency offset per simulation using this method, and since simulation of close-to-carrier phase noise is restricted due to memory limitations, an alternate approach is necessary to represent the oscillator noise process more accurately.

Figure 3.23 Coarse FFT spectrum

Figure 3.24 Output noise spectrum due to single tone injection

3.3.3.2 A Noise Model Based on Leeson's Method

An oscillator can be represented as an amplifier with a gain A followed by a high-Q resonant circuit, the output of which is fed back to the amplifier input, as shown in Figure 3.25. The gain of the resonant circuit has been normalized to unity, and the amplifier gain must also be unity in order for the circuit to oscillate [Smi]. This is the approach taken by Leeson [Lee].

This model represents a second-order system (a single LC tank circuit) but requires modification to represent the higher order system of the proposed circuit. (The LC VCO contains two tank circuits plus feedback components, which together with the transistor parasitics results in a sixth or higher order system.) It is useful however, to analyze this model so that it can be adapted to represent the actual circuit. $H(j\omega)$ is a bandpass filter with centre frequency at the carrier, f_o . S_θ represents the amplifier-noise-power spectral density referenced to the amplifier input [Smi]. A plot of a typical S_θ spectrum is shown in Figure 3.26. At frequencies above f_u the spectrum is flat due to white noise. As it approaches dc the spectrum rises due to $1/f$ noise. Phase modulation causes the noise to be centered around the oscillator frequency, so that $1/f$ noise dominates close-to-carrier. For the circuit of Figure 3.25, the closed-loop steady-state transfer function between the amplifier output and input is given by

$$\frac{S_\phi}{S_\theta} = \frac{1}{1 - H(j\omega)} \quad (3.31)$$

Figure 3.25 Model used to represent the phase noise of a second-order oscillator

where

$$H(j\omega) = \left(1 + jQ \left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} \right) \right)^{-1} \quad (3.32)$$

Since the distribution of noise is about the centre frequency, it is useful to replace $H(j\omega)$ by its low-pass equivalent. After manipulation of the closed-loop transfer function, the resulting expression gives the ratio of phase noise to signal power, which can be written as

$$S_{\phi}(\omega) = S_{\theta}(\omega) \left(1 + \frac{\omega_0^2}{4Q^2\omega^2} \right) \quad (3.33)$$

This expression agrees with the formula proposed by Leeson [Lee], and demonstrates that phase noise is inversely proportional to Q^2 of the resonator.

Since the proposed VCO contains dual tank and feedback circuits, the preceding model requires modification, as shown in the revised block diagram of Figure 3.27. It requires an open-loop circuit (the bandpass filters represented by $H(j\omega)$) resulting in a closed-loop system.

Figure 3.26 Amplifier-noise-power spectral density

Figure 3.27 Fourth-order model for oscillator phase noise

The model is constructed by representing the overall open-loop gain of the circuit as the sum of two transfer functions, as proposed in [NM1]. $H_1(j\omega_1)$ and $H_2(j\omega_2)$ represent two high-Q bandpass filters, with centre frequencies ω_1 and ω_2 , and are given by

$$H_1(j\omega_1) = \left(1 + jQ_1 \left(\frac{\omega_1}{\omega_0} - \frac{\omega_0}{\omega_1} \right) \right)^{-1} \quad (3.34)$$

and

$$H_2(j\omega_2) = \left(1 + jQ_2 \left(\frac{\omega_2}{\omega_0} - \frac{\omega_0}{\omega_2} \right) \right)^{-1} \quad (3.35)$$

The open-loop gain of the circuit was given previously by (3.12). This expression describes a fourth-order system with two separate bandpass filters and feedback paths. A bandpass-to-lowpass transformation can be used to obtain a relatively simple closed-loop transfer function. The ratio of the equivalent phase noise-to-signal power is given by

$$S_\phi = S_\theta \left(\left| 1 - H_1(j\omega_1) - H_2(j\omega_2) \right|^2 \right)^{-1} \quad (3.36)$$

Figure 3.28 An accurate model for oscillator phase noise prediction

The input-referred noise for a single transistor can be simulated in SPICE and multiplied by the low-pass transfer function in MATLAB. A plot of the output noise-to-signal power can be generated by summing contributions due to individual noise sources.

There are a number of problems with this approach. Since the oscillator is a closed-loop system, inputs and outputs are not clearly defined. Simulation results produced unrealistic values (too low and the wrong shape) for the noise spectrum compared to the measured phase noise in [NM1]. As discussed previously in section 3.2, the model is inaccurate, and does not account for interaction between the feedback paths. The actual transfer function is more complex and an expression which is sixth-order or higher is more realistic. The closed loop model was found but to convert to open loop requires some manipulation, so it seemed appropriate to go directly to the third method, which is a more adequate description.

3.3.3.3 A Noise Model Based on Small-Signal Analysis of the Closed Loop Circuit

The small-signal equivalent circuit of the VCO developed previously is reproduced in Figure 3.28. The resulting transfer function is sixth-order, but there are two poles at the origin which cancel with zeros at the origin, producing the net effect of a fourth-order transfer function.

The transfer function is complex so it will not be written explicitly. Matrix algebra using MATLAB was used to find the poles and zeros of the system, and the resulting frequency response can be obtained (e.g. V_1/I_1). This transfer function can be multiplied by the results of a SPICE noise analysis for a single transistor, and a plot generated which can be used to predict the phase noise of the oscillator. An examination of the plot of phase noise-to-signal power (illustrated in the next chapter) shows that it agrees with experimental

data for similar oscillators [NM1]. However, there are a number of issues to be resolved before this method can be used in an accurate prediction of phase noise. Further details of this method of simulation and results of phase noise prediction for the LC VCO are presented in the next chapter.

3.4 Summary

This chapter focused on the development of models used to describe the characteristics and performance of the proposed VCO circuit. An analysis of a simple single-transistor sinewave oscillator was presented to provide insight into the process of oscillator design and analysis. The conditions for oscillation were derived, and linear circuit analysis was used to predict the frequency of oscillation. These techniques were extended to provide a basis for the design and analysis of the proposed circuit. The simplified LC VCO circuit is composed of six transistors, and as a result, the model developed was considerably more complex than that required to describe a simple single-transistor circuit. After a number of iterations, a model was developed which adequately described the characteristics of the proposed LC VCO.

The phase noise characteristic of a VCO is an important design consideration, since its noise will have an impact on system performance. The sources of oscillator noise were examined, and methods of oscillator phase noise analysis were explored. An iterative approach was adopted to develop a suitable model to describe the noise performance of the LC VCO. Details of the phase noise simulation process, and an analysis of the issues involved in accurate prediction of oscillator phase noise will be addressed in the next chapter.

Chapter 4

Design and Implementation of the LC VCO

There are a number of trade-offs in the requirements for VCOs used in mobile radio which present a significant challenge for monolithic VCO design. Low power consumption is desirable, but reliable oscillation requires a substantial value of current for oscillation start-up. The requirement for low phase noise is in opposition to the requirements for large tuning range and high modulation sensitivity.

The design and implementation of a monolithic bipolar VCO is presented in this chapter. Oscillator design using techniques of simulation developed in the previous chapter will be presented. The frequencies of oscillation predicted by linear circuit analysis will be contrasted to quantities obtained from SPICE time-domain analysis. The suitability of these methods as a basis for the design of high-frequency VCOs will be discussed. A number of design issues will be addressed so that an optimum VCO design can be achieved within the limits of the available technology. Post-layout simulation results will be presented. These will be contrasted with measured results in the following chapter, so that the relevance of the simulation technique can be evaluated. Details of the phase noise simulation technique and results of phase noise simulations will be presented.

4.1 LC VCO Circuit Implementation

The design of the monolithic VCO is based on a circuit described by Nugyen and Meyer in [NM1]. The proposed tuning range of the circuit is 200 MHz, with a centre frequency of 1.8 GHz. The desired power consumption is 120 mW. A 0.8 μm BiCMOS process with a nominal f_T of 11 GHz is used to implement the design. The complete circuit schematic is illustrated in Figure 4.1. The operation of the oscillator core circuit has been discussed in the previous chapter. To allow for variation of the core circuit bias current, an additional I/O pad is connected to the junction of R_{13} and Q_{16} emitter so that an external current-setting resistor R_{BIAS} can be connected in parallel with R_{13} .

The operation of the remainder of the circuit will be described. Input transistors Q_{11} and Q_{12} form a differential pair which functions as a single-ended to differential converter. Emitter degeneration resistors R_3 and R_4 and diode-connected transistors Q_{24} and Q_{25} are used to lower the gain of the input stage, resulting in a large linear input range for $V_{control}$. The differential output signal is applied to the bases of Q_1 and Q_4 to control the fraction of bias current $I_{bias}/2$, which drives these transistors.

Figure 4.1 LC VCO schematic

The oscillator signal, appearing at the bases of Q_5 and Q_6 drives the bases of an output differential pair composed of Q_7 and Q_8 . A single-ended output signal is buffered by cascaded emitter-followers Q_9 and Q_{10} which drive an external $50\ \Omega$ load (not shown). The bias current for transistor Q_{10} is supplied through an external emitter resistor, R_{EXT} .

Initial component values and transistor sizes are determined by dc bias conditions. The bias current source is implemented as the starting point of the design. Bias currents are supplied by a current mirror composed of Q_{13} , Q_{14} , Q_{15} , Q_{16} , and Q_{17} . A reference current of 2 mA is supplied by Q_{13} in series with R_1 . A 4X transistor was used for Q_{13} , while other transistors in the bias configuration are scaled appropriately to provide multiples of the reference current. The bases of the current mirror transistors are biased at 1 volt. The collector voltages of transistors Q_{15} , Q_{16} , and Q_{17} are fixed at approximately 1.5 volts to ensure active-mode operation. Fine tuning of the bias currents is accomplished using emitter degeneration resistors. (Resistance values are determined from a rough calculation, assuming $V_{BE} = 0.85\text{ V}$, and final values are determined by means of a dc operating point analysis.)

There are a number of considerations to be addressed in the design of the oscillator core circuit. Low power is desirable, but sufficient current is needed to meet gain requirements to ensure oscillation start-up. Operation in the desired frequency range must be achieved using the range of inductor values available in the silicon process. A realistic model is required for the on-chip inductors, in order to predict the frequency of oscillation accurately.

Planar inductors realized in silicon IC technology have been reported by Nguyen and Meyer. The range of values are between 2 and 10 nH, and have been fabricated as square spirals of top metal on a layer of silicon oxide. The use of thick oxides isolates the inductor from the silicon substrate, which reduces reflected losses and optimizes inductor Q. Inductor quality factors between 3 and 8 have been reported [NM2].

The proposed tuning range for the monolithic VCO is 180 MHz, extending between 1.69 to 1.87 GHz; due to process variations a somewhat larger range is desirable. Process variations result in capacitor values which can vary by $\pm 10\%$ [Long]. The initial assumption regarding process variation for the inductors was pessimistic. It was originally assumed that inductor values were subject to a $\pm 10\%$ variation, however after the circuit was fabricated, further investigation revealed that the variation was only $\pm 5\%$ [Long]. Using the initial assumption of a 10% variation in frequency-determining component values, a tun-

ing bandwidth of at least 540 MHz is required to allow for the variation in frequency, resulting in a tuning range extending from 1.54 to 2.08 GHz.

Initial values for the inductors were obtained from the journal paper by Nguyen and Meyer [NM1]. Initial component values for the inductors are $L_1 = 6.5$ nH, and $L_2 = 3.7$ nH. A suitable model for the inductors is required in order to predict oscillation frequency as accurately as possible. A distributed model for the planar inductors is based on the work of J. Long [Long], and is illustrated in Figure 4.2. In this equivalent two-port circuit, L_{1a} and L_{1b} model the self inductance in the top metal segments, R_{D1} and R_{D2} represent the metal sheet resistance, and C_{OX1} , C_{OX2} and C_{OX3} model the oxide capacitance between the top metal layer and the silicon substrate. Capacitances C_{S11} , C_{S12} , and C_{S13} model the substrate capacitance and R_{S11} , R_{S12} , and R_{S13} represent the substrate resistance. Coupling capacitances between metal segments are modelled by C_{P1} , C_{P2} , and C_{P3} [NM2]. The dimensions of the spiral inductors were optimized using Touchstone microwave simulations to achieve maximum Q for the required values of inductance. Since one side of the inductor is grounded, it is modelled as a one-port. Element values obtained from Touchstone optimization are used to represent the spiral inductors in a SPICE transient analysis of the entire circuit. Final values for the inductors are $L_1 = 6.426$ nH, and $L_2 = 3.546$ nH. The dc series resistances of the inductors are 8.1Ω for L_1 , and 5.8Ω for L_2 . The Q -values of the spiral inductors are $Q_1 = 4.8$, and $Q_2 = 5.18$.

Figure 4.2 Distributed inductor model

Results of MATLAB simulations of the small-signal model of Figure 3.11 are used as a starting point to obtain the component values of the oscillator circuit. Bias current I_{bias} must provide sufficient gain to ensure oscillation start-up. Capacitors C_3 and C_6 , C_4 and C_5 , form a capacitive dividers which in part determine the initial gain of the circuit. Since these capacitors also form part of the tank circuits, their values must be selected so that the desired resonant frequencies can be realized. A value of 0.2 pF is selected for capacitor C_1 ; the parasitic capacitance of inductor L_2 is used to form capacitor C_2 . Inductor parasitics also contribute to the final values of the tuned circuit elements.

Transistor sizes for the central oscillator circuit are initially determined by an examination of plots of f_T versus collector current for the BATMOS transistors (see appendix). SPICE simulations indicate that a small-signal g_m of $0.163 \Omega^{-1}$ is necessary to produce adequate gain for oscillation build-up. Maximum f_T of the smaller transistors (1X to 4X) is achieved with collector currents of less than 2 mA, which is less than the minimum requirement for adequate gain. Plots of f_T as a function of collector current for the 15X transistors indicate a maximum f_T of 12.5 GHz is obtained with a V_{CE} of 2 V and a collector current of 4 mA. This value of current is sufficient for reliable build-up of oscillations.

Although small-signal MATLAB simulations are useful as a starting point for oscillator design, non-linear time-domain analysis is used iteratively to achieve desired operation. Time-domain analysis in SPICE is utilized to realize the required tuning range and sufficient output amplitude. Transistor sizes and bias current are varied accordingly until the frequency and amplitude of oscillation meet design specifications. Final transistor sizes are 5X for Q_1 to Q_4 , and 15X for Q_5 and Q_6 . Low bias currents are used initially to attempt to minimize power consumption. Current is increased until reliable oscillation occurs; this is accomplished with a bias current of 4.58 mA. It was impossible to realize the previously specified tuning range without excessive separation of the resonant frequencies. This can result in a "dead band", where no oscillations are produced for certain intermediate values of V_{control} . Continuous operation over a tuning range of 480 MHz is achievable, and is realized by adjusting the values of feedback capacitors C_3 to C_6 . The simulated tuning range extends between 1.54 and 2.02 GHz as V_{control} is varied between 1 and 4 volts.

4.2 Layout Considerations

Design considerations associated with the layout of a high-frequency VCO are presented in this section. Since this circuit is designed to operate at frequencies approaching 2 GHz, it is important to ensure that parasitic circuit elements such as stray capacitance and inductance are kept to a minimum. Since there is significant power dissipation in certain circuit components, it is essential to ensure that maximum current density and power dissipation are well below specified limits.

The VCO circuit is laid out using Northern Telecom Electronic's (NTE) Bipolar Analog Telecom MOS (BATMOS) technology, a 0.8 μm BiCMOS process. Fabrication is accomplished with the assistance of the Canadian Microelectronics Corporation (CMC) and Bell Northern Research (BNR). The nominal f_T for NPN bipolar devices is 11 GHz [CMC]. Polysilicon capacitors and resistors are available, which enable monolithic implementation of bipolar analog circuits with this technology. The design is accomplished using the CADENCE-EDGE design facility.

Inductors are laid out as square spirals using the top-metal layer to minimize parasitics. The length of the large inductor (6.43 nH) is 313.5 μm , and the length of the small inductor (3.55 nH) is 233.5 μm . The width of the metal segments is 15 μm , with a spacing of 1.5 μm between turns. Separation between the two inductors is 102 μm to avoid coupling due to mutual inductance between the tank circuits. Process design rules specify a maximum width of 30 μm for metal lines. This width is used for all power and ground lines to minimize series resistance and inductance, and to avoid electromigration due to maximum allowable current densities. Analog pads are used for external connections to minimize attenuation due to pad capacitance. A 45X transistor is used in an emitter-follower configuration to drive a 50 Ω load. Figure 4.3 shows the layout of the circuit as captured from the EDGE CAD design software.

Components are laid out to minimize the distance between circuit elements. Transistors in the oscillator core circuit are placed as close as possible to minimize parasitics due to stray inductance associated with extensive interconnections. Metal lines connecting feedback capacitors are formed using minimum widths, and are made as short as possible to reduce coupling due to parasitics. Interconnection between all circuit elements is kept to a minimum to reduce parasitic capacitance and inductance. The total layout area of the VCO circuit is 1160 μm x 714 μm .

Figure 4.3 Circuit layout of the LC VCO

4.3 Simulation Results

Results of post-layout simulations are presented in the following sections. A SPICE transient analysis of the circuit is used to verify operation within the design parameters. Component values used in this analysis include parasitic component values extracted from the layout and component values obtained from the Touchstone inductor model. Phase noise simulations using component values generated by the layout extraction are used to characterize the noise performance of the oscillator.

4.3.1 Post-Layout Simulation

The selection of initial component values is based on results of pre-layout time-domain simulations. After the circuit parasitics are extracted, post-layout simulations are performed. Some adjustment to values of feedback capacitors C_3 to C_6 is necessary to meet design specifications. Simulations are performed at a power supply voltage of 5 volts and a temperature of 25°C.

The plot of Figure 4.4 (a) shows the results of transient analysis in SPICE as the control voltage is swept between 1 and 4 volts. The peak-to-peak amplitude reaches a minimum value of 374 mV with a dc input of 3.1 V. The output signal is the differential sum of signals present at the bases of Q_7 and Q_8 . These signals are displayed in Figures 4.4 (b) and (c). The signal at the base of Q_8 becomes attenuated as the input voltage increases, while the signal at the base of Q_7 becomes attenuated as the input voltage decreases. These two signals are essentially added at the output, producing the minimum value of their sum at $V_{IN} = 3.1$ V. Figure 4.4 (d) shows a single cycle of the output waveform with an input voltage of 1 volt dc and Figure 4.4 (e) shows a single cycle of output the waveform with an input voltage of 4 volt dc. The waveforms shown by these plots exhibit some compression, but contain a strong sinusoidal component. A tuning range of 480 MHz is achieved between 1.54 and 2.02 GHz.

Figure 4.4 (a) Simulated VCO output using a swept dc input signal

Figure 4.4 (b) VCO signal at Q₈ base

Figure 4.4 (c) VCO signal at Q₇ base

Figure 4.4 (d) Simulated VCO output at $V_{IN} = 1.0$ volt

Figure 4.4 (e) Simulated VCO output at $V_{IN} = 4.0$ volts

The simulated modulation sensitivity K_{VCO} is illustrated in Figure 4.5. The characteristic is approximately linear and has a value of 715 MHz/V between 2.95 to 3.4 volts.

The effect of temperature variation on the oscillation frequency is investigated by performing a temperature analysis in SPICE. Temperature is varied from -40 to 27 and 85 °C. Worst case sensitivity to temperature variation is obtained in two situations. In the first case, temperature is varied between 27 to 85 °C with a dc input voltage of 3.15 volts. The oscillation frequency varied between 1.695 to 1.933 GHz, a difference of 14.0%. In the second case, temperature is varied between -40 to 27 °C with a dc input voltage of 3.25 volts. The oscillation frequency varied from 1.638 to 1.894 GHz respectively, a difference of 13.5%. These results indicate significant sensitivity to temperature variation.

The nominal power consumption of the circuit obtained from a dc operating point analysis is 125 mW. However, the power consumption of the output amplifier and buffer is 60 mW, so that the simulated power consumption of the oscillator circuit is 65 mW.

Figure 4.5 Simulated modulation characteristic

The sensitivity of this circuit to power-supply variation is investigated using SPICE time-domain analysis. Oscillations at the maximum frequency tend to die out when V_{CC} is reduced below 4.0 volts. This is due to dc biasing conditions and restrictions imposed on linear operation with a 5 volt power supply. Simulations also show frequency sensitivity to the supply voltage. Maximum frequency and tuning range was observed between 4.75 volts and 5.0 volts. Tuning range and maximum frequency decreased as V_{CC} was decreased below 4.5 volts. The simulated output power as a function of frequency is illustrated in Figure 4.6. Maximum output power is 3.41 dBm at 1.56 GHz. Minimum output power is -4.57 dBm at 1.68 GHz, due to the low gain at $V_{IN} = 3.1$ V illustrated previously in Figure 4.4 (a).

Figure 4.6 Simulated output power versus oscillation frequency

4.3.1.1 The Discrepancy between Small-Signal Analysis and Transient Analysis

It was originally intended to use small-signal analysis as a reasonably accurate first step in the design of the high-frequency VCO. However, significant discrepancies were discovered between the results of time-domain analysis and the results of small-signal analysis of the previous chapter. It was noted that small-signal analysis predicts oscillation between 1.976 GHz and 2.413 GHz, producing a tuning range of 437 MHz. In contrast to this result, transient analysis predicts oscillation between 1.54 GHz and 2.02 GHz, producing a tuning range of 480 MHz. Since SPICE transient analysis accounts for non-linearity, and includes models for the active devices used in the circuit, parasitics extracted from the layout, and distributed models for the spiral inductors with associated parasitics, it is expected that the results of this simulation technique will realistically predict the behaviour of the circuit. If this assumption is correct, then it is reasonable to assume that there is some deficiency in the model used for small-signal analysis.

There were a number of differences between the models used for transient analysis and small-signal ac analysis. In the small-signal model, active devices were modelled by a linear equivalent circuit. Transistors were replaced by voltage-controlled current sources

with C_π included as a parasitic. Other parasitic capacitances were neglected since their values were small compared to capacitors which were intended as part of the circuit. A model for the output amplifier was also omitted. While it is true that the small-signal model lacks the detail of the model used for transient analysis, the differences do not appear to be significant. There must be additional parameters which have been neglected in the construction of the small signal model, and which would account for the observed discrepancy.

It became apparent from [Plett] and the results of Fourier analysis, that the value of g_m previously used in MATLAB simulations of the small-signal model, and assumed to contain only a real component, was actually a complex value. This value was obtained by conducting a Fourier analysis of the oscillator circuit, and calculating the value of g_m for the fundamental component. For example, if the left side of the circuit of Figure 3.8 is selected ($K=1$), g_m can be calculated by dividing the small-signal collector current of the top transistor (Q_1) by the small-signal base-to-emitter voltage of the lower transistor (Q_5). Since these voltages and currents are represented both in magnitude and phase, re^{-j} and imaginary components g_{mr} and g_{mi} can be obtained from the result. An additional parameter g_{m2} can be obtained from the right side of the circuit using a similar procedure ($g_{m2} = i_{cQ4}/v_{beQ6}$). Using this example, complex values can be included in a MATLAB closed-loop analysis by replacing g_{meff} (reduced g_m) by $g_{meff} + g_{mi}$, and the value $(1-K)g_m$ by g_{m2} . A similar procedure can be used to obtain results for $K=0$.

Results of simulation show a reduction in operating frequencies if the complex g_m is incorporated in MATLAB closed loop analysis. The resulting additional phase shift reduces the minimum frequency from 1.9709 GHz to 1.7539 GHz, and reduces the maximum frequency from 2.4114 GHz to 2.0701 GHz. Although these results are not in full agreement with the results of SPICE transient analysis, they show a trend in the right direction, and provide at least a partial explanation for the inconsistency. Any additional phase shift due to the effect of higher-order harmonics have not been included in the simulations. Closer agreement between small-signal and transient analysis may result from the inclusion of these additional effects.

Since it was possible to include the effects of a complex value of g_m in closed loop analysis, it is useful to compare this with the results of a SPICE open loop analysis using complex g_m . The results of this analysis are shown in Figures 4.7 (a) and (b), where the magnitude and phase responses are plotted for evenly spaced values of g_m . These values range from the small-signal value of g_m (the top curve) to the large-signal value of g_{meff}

(the bottom curve). A magnitude of 1 corresponds to a phase of 0° for the lowest curve, as predicted by theory. Comparison of Figure 4.7 (a) with Figure 3.14 (a) shows additional phase shift due to the effect of the imaginary part of g_m . The result is an effective reduction of the resonance frequencies. For $K=1$, oscillation occurs at 1.761 GHz, and for $K=0$, oscillation occurs at 2.146 GHz. These values are reasonably close to the results of closed loop analysis.

4.3.2 Phase Noise Simulation

In this section details of the phase noise simulation technique based on the previously developed model of section 3.2.3 are presented. This method of phase noise analysis is based on the assumption that low-frequency noise present at some internal node is transferred to equally distributed noise sidebands on either side of the oscillator center frequency, at frequencies $f_0 \pm f_{noise}$. This occurs due to second-order nonlinearities in the oscillator, which cause intermodulation between the low-frequency noise and the high-frequency oscillation [Gar]. Simulation results showing the single-sided power spectral density of VCO noise are presented. These results will be contrasted to measured VCO phase noise in the next chapter.

Figure 4.7 (a) Oscillator open loop analysis using complex g_m and $K=1$

Figure 4.7 (b) Oscillator open loop analysis using complex g_m and $K=0$

4.3.2.1 Phase Noise Simulation Procedure

A diagram of the complete circuit and a simplified diagram of the oscillator core circuit are re-produced for reference in Figures 4.8 and 4.9.

Figure 4.8 LC VCO circuit diagram

Figure 4.9 Core circuit diagram

The baseband input-referred noise for a single transistor is obtained from data generated by an ac noise analysis in SPICE. Figure 4.10 illustrates the circuit used to obtain the input-referred noise of a single transistor. The collector current used is obtained from the results of a SPICE operating point analysis of the oscillator circuit. Data are obtained for transistors Q_1 to Q_4 to generate input-referred noise voltages V_{NQ1} , V_{NQ2} , V_{NQ3} , and V_{NQ4} .

Figure 4.10 Circuit used to generate input-referred noise

Figure 4.11 Oscillator small-signal circuit

Matrix algebra and MATLAB are used to obtain the transfer function derived from the small-signal circuit developed previously in Chapter 3 and reproduced in Figure 4.11. The g_m used in this model is the large-signal $g_{m\text{eff}}$ obtained iteratively from MATLAB which results in poles on the $j\omega$ axis. The value K is a dimensionless quantity and represents the fraction of bias current ($I_{\text{bias}}/2$) applied to Q_1 and Q_3 . (The fraction of bias current applied to Q_2 and Q_4 is denoted by $1-K$.) Noise voltages present at nodes V_3 and V_4 are due to individual contributions from transistors Q_1 to Q_4 due to noise currents $(g_m/2)V_{NQ1}$ to $(g_m/2)V_{NQ4}$. These will appear at the output of the oscillator core circuit (nodes V_3 and V_4 in Figures 4.8 and 4.9).

Noise voltages at a frequency f_{noise} are multiplied by the transfer function of the circuit which is evaluated at $f_0 + f_{\text{noise}}$. This effectively moves noise at a given frequency offset from dc to an equivalent offset from the carrier. The transfer function is evaluated over the range of frequencies from 1 Hz to 10 GHz referenced to the oscillator frequency.

Noise currents are injected at nodes V_1 and V_2 by multiplying the input referred noise (V_{NQ1} etc.) by $g_m/2$. These noise currents will produce noise voltages at V_3 and V_4 . For each input, the resulting noise at nodes V_3 and V_4 are correlated (e.g. V_3/V_{NQ1} and V_4/V_{NQ1}). However, the oscillations present at these nodes will differ in magnitude and phase. Noise sources due to different transistors are uncorrelated. Examples of uncorrelated noise sources are V_3/V_{NQ1} and V_3/V_{NQ2} . The total output noise power due to uncorrelated noise sources can be calculated by simply adding noise powers directly at the output.

Figure 4.12 Voltage-to-voltage transfer function of the output amplifier

Gain compression occurs in the output amplifier (composed of Q_8 , Q_9 , Q_{11} , and Q_{12}), and is illustrated in Figure 4.12. As a result, the gain from these nodes to the output of the circuit will differ from the small-signal gain. Noise present at each of these nodes will also experience the same non-linear gain. SPICE analysis has shown that the phase shift from node V_3 to the output is 180° , and from node V_4 to the output is 0° (as would be expected for a differential amplifier). Because the common-mode gain of a differential amplifier is low, and since MATLAB is used to calculate the phase noise at the output of the circuit (at V_{OUT}), it is also possible to refer both nodes V_3 and V_4 to one of these nodes, for example V_3 . This is accomplished by inverting one of the noise voltages and performing a vector addition. A phase relationship exists between oscillations at nodes V_3 and V_4 , as determined by Fourier analysis, so they can also be combined. The combined noise voltages are multiplied by the non-linear gain to obtain the output noise voltage. This noise voltage is squared to obtain the output noise power.

The total noise at the output includes white noise due to the output amplifier and driver, and thus the amplifier noise power is added to the oscillator noise power to produce the final result. The input-referred noise at the base of each transistor of the output amplifier can be simulated, and since, at the oscillator centre-frequency, this will be caused by white

noise having a flat frequency spectrum, this is evaluated at a single frequency equal to ω_0 . Thus the input-referred noise sources are denoted by V_{N1} , V_{N2} , V_{N3} , and V_{N4} . The (non-linear) gain to the input of the next stage can be determined by Fourier analysis. Each input-referred noise is multiplied by successive gains to the output, and the results added to obtain the thermal noise contribution due to the output amplifier. An example will be used to illustrate the situation. The diagram of the output amplifier is shown in Figure 4.13. The gain from V_{N1} or from V_{N2} to the collector of Q_8 is 2.55; the gain from V_{N3} to the emitter of Q_9 is 0.70; the gain from V_{N4} to V_{NOUT} is 0.92. Thus total output noise power for thermal noise is given by

$$V_{NOUT}^2 = (V_{N1} \times 2.55 \times 0.70 \times 0.92)^2 + (V_{N2} \times 2.55 \times 0.70 \times 0.92)^2 + (V_{N3} \times 0.70 \times 0.92)^2 + (V_{N4} \times 0.92)^2$$

Finally, the total phase noise-to-signal power can be determined by dividing the total mean-square noise power at the output (obtained by adding all the individual contributions) by the square of the rms carrier output voltage, and taking the $\log \times 10$ to produce the phase-noise-to-signal power referenced to the carrier in units of dBc/Hz.

Figure 4.13 Output amplifier thermal noise sources

4.3.2.2 Simulation Results

Simulations are conducted at different operating frequencies to determine the worst case phase-noise power-spectral-density (PSD) performance. Figure 4.14 (a) shows the results of phase noise analysis for a K-value of 1, and predicts that the phase noise will have a value of -82.59 dBc/Hz at 100 kHz offset from the carrier. Figure 4.14 (b) shows simulated phase noise for a K-value of 0, and predicts phase noise of -69.78 dBc/Hz at 100 kHz offset from the carrier. Figure 4.14 (c) shows simulated phase noise for a K-value of 0.5, and predicts phase noise of -82.14 dBc/Hz at 100 kHz offset from the carrier. The results of this analysis indicate that worst case phase noise occurs at the highest operating frequency of the VCO, where operation is determined mainly by the right feedback loop. This agrees with the open loop analysis which shows weaker resonance and lower slope of phase for the highest frequency (Figure 4.7).

Figure 4.14 (a) Simulated phase noise at K=1

Figure 4.14 (b) Simulated phase noise at $K=0$

Figure 4.14 (c) Simulated phase noise at $K=0.5$

The effects of inductor Q-adjustment on phase noise are shown in Figures 4.15 (a), (b), and (c). The Q was increased by a factor of 10 for each of these simulations, and results show an approximate 20 dB improvement in phase noise for each case. These results, summarized in table 4.1 are in agreement with the hypothesis that phase noise is inversely proportional to Q^2 of the resonator [Smi].

The predictions of phase noise performance will be contrasted with the measured phase noise of the LC VCO in the next chapter.

Figure 4.15 (a) Phase noise due to Q-enhancement at $K=1$

Figure 4.15 (b) Phase noise due to Q-enhancement at $K=0$

Figure 4.15 (c) Phase noise due to Q-enhancement at $K=0.5$

Table 4.1 Summary of VCO phase noise simulation

Resonator Q	K-Value	Phase Noise @ 100 kHz Offset from the Carrier (dBc/Hz)
5	0	-69.78
	0.5	-82.14
	1.0	-82.59
50	0	-90.48
	0.5	-103.5
	1.0	-102.4

4.4 Summary

The design and implementation of the LC VCO has been presented. Design issues include the requirement for sufficient current to produce start-up of oscillation, the need to use appropriate inductor and capacitor values to produce the desired operating frequency range, and accurate inductor modelling so that an accurate simulation can be performed prior to fabrication. A model for the on-chip inductors has been presented. Simulation of inductor models to obtain maximum Q has been described. Layout considerations were addressed. Post-layout simulations using models obtained from inductor simulation and from the layout extraction were conducted, and optimization was performed to achieve the desired tuning range. Post-layout simulation results were presented to characterize the performance of the oscillator. Conflicting simulation results were examined, and a partial explanation for the discrepancies was proposed. Details of the phase noise simulation procedure were presented. Results of phase noise simulation were presented, including the effect of Q-adjustment on phase noise.

The results of measurement are presented in the next chapter and are contrasted to the results of simulation, so that the feasibility of the proposed models can be examined.

Chapter 5

Experimental Results

This chapter presents the test set-up, measurement procedures and experimental results for the LC VCO. The performance of the circuit is characterized in terms of frequency of oscillation and tuning range, voltage-to-frequency transfer characteristic, power dissipation, output power, sensitivity to power supply variation, and phase noise performance. The measured results are contrasted to the predictions of the previous chapter. Discrepancies between the predicted and actual performance of the circuit will be addressed.

5.1 Experimental Set-up

The test set-up for the VCO is described in this section. The fabricated circuit was supplied by Northern Telecom Electronics through CMC in the form of loose dice and in a bonded ADX1185 package. A printed circuit board was constructed to test the packaged version. An LM78L05 regulator was used to supply 5 volts dc to the IC and a 20 K Ω potentiometer was used to vary the control input. An SMA-type wave launcher was used to couple the output signal to a 50 Ω measurement system. The circuit was enclosed in a metal case to provide shielding from external noise sources. The performance of the unpackaged dice was measured using a Summit 9000 analytical probe station. Hewlett Packard 6213A variable power supplies were used to supply V_{CC} and a variable control voltage to the circuit. A microwave bias tee was used to connect the output signal to the 50 Ω measurement system. Diagrams of the test beds are shown in Figures 5.1 and 5.2.

Figure 5.1 Wafer probe test set-up

Figure 5.2 Printed circuit board test set-up

5.2 Wafer Probe Test Results

Measurements were performed on ten unpackaged dice using the wafer probe test station. The test set-up provided the flexibility required to change individual parameters such as oscillator core bias current and power supply voltage, and provided a convenient means to test all of the devices by moving the wafer probes from one die to another.

Individual tests were conducted on each die to determine the range of operating frequencies, optimum bias current, and phase noise variation. Extensive tests were performed on two of the dice to obtain transfer characteristics, the effect of bias current variation, sensitivity to power supply variation, and phase noise measurements. All measurements were performed using a 50 Ω off-chip load.

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5.2.1 Variation in Device Characteristics

Preliminary tests were conducted on all devices to determine the variation in operating characteristics due to process variations. As shown in Figure 4.1, an external bias resistor R_{bias} can be connected in parallel with bias current setting resistor R_{13} . The additional resistor was required to produce sufficient oscillator core bias current to start up and maintain oscillations. The value of this resistor determined the tuning range of each individual device. Table 5.1 illustrates the variability of device characteristics in terms of phase noise and tuning range, and indicates the values of R_{bias} and corresponding bias current required to optimize the tuning bandwidth of the various devices. Results show a variation in tuning range between 35 MHz to 58 MHz for similar values of bias current. The maximum frequency of oscillation was 1.485 GHz at 18 mA bias current. The optimum external resistance value was 10 Ω for all devices except die #5. This particular device also exhibited the lowest output power and poorest phase noise performance.

Table 5.1 Device Variation

Die #	R_{bias} (Ω)	I_{bias} (mA)	f_{min} (GHz)	f_{max} (GHz)	Phase Noise @ 100 kHz Offset from the Carrier (dBc/Hz)	Tuning Range (MHz)
1	10	18.1	1.4394	1.4829	-73	43.5
2	10	18.1	1.4256	1.4802	-77	54.6
3	10	18.4	1.4214	1.4794	-76	58.0
4	10	17.3	1.4260	1.4780	-67	52.0
5	15	15.3	1.4403	1.4794	-62	39.1
6	10	17.8	1.4463	1.4850	-66	38.7
7	10	17.8	1.4397	1.4832	-76	43.5
8	10	17.8	1.4460	1.4849	-75	38.9
9	10	17.8	1.4484	1.4844	-75	36.0
10	10	17.8	1.4466	1.4820	-76	35.4

5.2.2 Tuning Range as a Function of Bias Current

The relationship between tuning range and oscillator bias current was investigated using die #4 by varying the value of the external bias resistor. Tuning range increased with bias current until a maximum of 50 MHz was reached at a bias current of 18 mA. Further increases in current reduced the tuning range. The maximum oscillation frequency of 1.561 GHz occurred at the lowest measured current and was reduced as current was increased. The measured results are summarized in Table 5.2. The simulated and measured results are plotted in Figure 5.3 for comparison.

Table 5.2 Variation of tuning range as a function of bias current

R_{bias} (Ω)	I_{bias} (mA)	f_{min} (GHz)	f_{max} (GHz)	Tuning Range (MHz)	Control Voltage Range (volts)
39	9.4	1.559	1.561	2	1.7 to 2.89
33	10.4	1.555	1.560	5	1.6 to 2.86
27	11.4	1.515	1.537	22	1.54 to 2.96
22	12.2	1.502	1.531	29	1.6 to 2.85
18	13.5	1.484	1.512	28	1.6 to 2.85
15	14.5	1.475	1.507	32	1.4 to 2.85
12	16.7	1.451	1.493	42	1.6 to 2.9
10	18.4	1.429	1.479	50	1.6 to 2.9
7.5	21.2	1.432	1.452	20	2.4 to 3.0

Figure 5.3 Tuning range as a function of bias current

Examination of Figure 5.3 reveals a significant discrepancy between the simulated results of the previous chapter and the measured device characteristics. Simulation predicts that with a bias current of 4.58 mA, the circuit should oscillate between 1.54 to 2.02 GHz. Initial tests conducted with no external bias resistor failed to produce oscillation start-up. A minimum external resistance of $39\ \Omega$ (corresponding to $I_{bias} = 9.4\text{ mA}$) was required to produce oscillations, resulting in a low amplitude output signal and a very limited tuning range of 2 MHz. A much larger current of 18.4 mA was required to extend the tuning range to the observed maximum of 50 MHz. Simulations also reveal that the tuning range increases as current is decreased, whereas measurements show that tuning range increases with current until a maximum is reached. Further increases in current above 18 mA result in a reduction of the tuning range.

It is possible that additional phase shifts due to parasitics and poorly modelled phase shift in transistors caused the shift in frequency. Coupling between the two inductors could also reduce the gain and require the higher current to start oscillations. It is also possible that unaccounted phase shift is responsible for the reduced tuning range.

5.2.3 Sensitivity to Power Supply Variation

The VCO sensitivity to power supply variation was measured by adjusting the power supply voltage between 4.25 and 6.75 volts. The sensitivity of tuning range and maximum frequency to supply voltage variation is plotted in Figure 5.4 (a) and (b). Simulated results are included for comparison. A $22\ \Omega$ bias resistor was used to obtain both simulated and measured results, such that at $V_{CC} = 5\text{ V}$, the bias currents had an equal value of 12 mA.

Measured results show an increase in tuning range as V_{CC} is increased until a maximum is reached at $V_{CC} = 6.5\text{ V}$. The tuning range decreases as V_{CC} is increased beyond this point. Simulated results show that the maximum tuning range coincides with the maximum frequency of operation, which occurs at about 5 volts.

The effects of power supply variation show some correspondence with results obtained by varying the bias current. The maximum tuning range occurs at $I_{\text{bias}} = 18.4\text{ mA}$ in both cases, indicating an optimum value of bias current which maximizes the tuning range.

Figure 5.4 (a) Sensitivity of tuning range to power supply variation

Figure 5.4 (b) Sensitivity of maximum frequency to power supply variation

Figure 5.4 (b) illustrates the sensitivity of maximum frequency to power supply variation. As the supply voltage is reduced, the output frequency reaches a maximum at $V_{CC} = 5$ V and decreases as V_{CC} is reduced further. Simulations show a similar maximum frequency reduction as V_{CC} is decreased below 4.75 volts.

Although it is difficult to positively identify the reasons for these observations, simulations were conducted in an attempt to explain the discrepancies between simulated and measured results. As V_{CC} is reduced below 4.5 volts, the change in dc bias causes transistors to become saturated, resulting in increased non-linearity. As the supply voltage or the current is increased, parasitic capacitances C_{π} and C_{μ} of transistors Q_5 and Q_6 are affected. As V_{CC} is increased, the reverse bias on the collector-base junction increases, reducing C_{μ} . An increase in V_{CC} from 4.5 to 6.5 volts produces a decrease in C_{μ} from 39.45 fF to 23.44 fF. Increases in the core circuit bias current have little effect on C_{μ} , but C_{π} is affected strongly. An increase in the core current from 4.58 mA to 18.53 mA results in a variation in C_{π} from 1.118 pF to 4.034 pF. A similar but less pronounced result was observed as the supply voltage was varied. As V_{CC} was increased from 4.5 volts to 6.5 volts, C_{π} increased from 1.02 pF to 1.42 pF. Since C_{π} and C_{μ} contribute to the overall tank circuit capacitance, an increase in their values will result in a reduction of the maximum frequency.

5.3 VCO Modulation Characteristic

The tuning constant of the VCO (K_{vco}) was measured by varying the control voltage between levels which produce the minimum and maximum frequencies. Since there was variation among the operating characteristics of the unpackaged devices, this measurement was performed on dice #3 and #4 which exhibit the widest tuning range. The modulation characteristics of the unbonded dice are plotted in Figure 5.5 (a). The effect of bias current on the modulation characteristic can be seen from a comparison of the modulation sensitivity of die #4 at bias currents of 12.2 mA and 18.4 mA. The tuning range can be extended by using the higher current, but linearity is compromised. The largest tuning bandwidth of 58 MHz is displayed by die #3, extending from 1.42 to 1.478 GHz. The tuning constant of the bonded circuit is illustrated in Figure 5.5 (b). The characteristic is approximately linear between 2.1 and 2.5 volts with a value of 30 MHz per volt. The tuning constant was simulated using $R_{\text{bias}} = 10 \Omega$, and is plotted in Figure 5.5 (b) for comparison.

Figure 5.5 (b) illustrates a further discrepancy between simulated and measured results. The simulated bias current was increased from 4.58 mA to 18.4 mA in an attempt to duplicate the measured results. Although the two curves are similar at the lower frequencies, the simulated tuning range is 115 MHz, extending to 1.614 GHz, while the measured tuning range is 37 MHz, extending to 1.527 GHz. The input voltage range of the circuit was limited between 1.6 and 2.95 volts, whereas the simulated input voltage range extended from 1.6 to 4.0 volts. As discussed later, these differences may be the result of inaccurate modelling.

Figure 5.5 (a) Modulation characteristic of the unbonded dice

Figure 5.5 (b) Comparison of simulated and measured modulation characteristics

5.4 Comments on Bonded VCO Test Results

Measurements on the bonded circuit show a significant improvement over previous results. Isolation from external noise sources was provided by the metal package. The device was mounted on a printed circuit board which was enclosed in a metal case; a 5-volt regulator and bypass capacitors close to the IC pins provided additional noise immunity. The tuning range was maximized using a $10\ \Omega$ bias resistor, and extended from 1.49 to 1.527 GHz. The protection against noise provided by circuit shielding resulted in an improvement in output power to -2.3 dBm.

The improvement in operating characteristics can be attributed to the elimination of parasitics associated with the test set-up required to probe the wafers. Coaxial cable was required to connect the wafer probes to power supplies and external components. Test leads form parasitic (capacitive and inductive) components which are significant at microwave frequencies. It was not possible to shield the wafer probe test set-up without building a specially constructed metal container. The absence of circuit shielding of the unpackaged dice contributed to interference from external noise sources.

The use of a microwave carrier such as the Kyocera MLC20G or MLC20S which further eliminates parasitics due to bond wire inductance and package capacitance should be considered for future designs.

5.5 VCO Output Power

The VCO output power is plotted as a function of frequency in Figure 5.6. The measured output power of the three devices tested previously is illustrated in Figure 5.6 (a), and simulated characteristics are illustrated in Figure 5.6 (b). There is considerable variation in the measured characteristics, and further disagreement between simulations and measurement. The maximum simulated output power is 5.41 dBm, whereas the maximum measured output power is -2.34 dBm. Simulations demonstrate that output power decreases with frequency, but this is not generally supported by measurement. However, both simulations and measurements demonstrate that output power increases with higher bias current. The bonded circuit displays a more constant output power as the frequency is varied, and exhibits the highest measured output power.

Figure 5.6 (a) Measured power output as a function of frequency

Figure 5.6 (b) Simulated power output as a function of frequency

5.6 VCO Power Consumption

The power dissipation of the LC VCO was measured from a 5 volt power supply and connection to a $50\ \Omega$ load. This measurement includes power dissipated by the two external resistors required for functional operation. The circuit dissipates 165 mW with a bias current of 12.2 mA and 200 mW with a bias current of 18.4 mA. This result is significantly larger than most other monolithic VCOs reported (see table 2.1). However, 60 mW is dissipated by the output buffer required to drive the output pad capacitance and the $50\ \Omega$ load. These results are in agreement with simulations which predict a power dissipation of 163 mW at 12.2 mA, and 195 mW at 18.4 mA.

5.7 VCO Output Waveform and Spectrum Analyzer Plots

The output waveform of the VCO was obtained using a Tektronix 7104 oscilloscope. This instrument is band-limited to 1 GHz, resulting in a waveform which appears attenuated from its actual amplitude. Sinusoidal waveforms which exhibit some non-linear distortion were obtained from the oscilloscope display, and are shown in Figure 5.7 (a) and (b). A non-linear output waveform was predicted by simulation, as illustrated in Figure 4.4 (d) and (e).

Figures 5.8 (a) to (c) illustrate the displayed traces of the VCO output using a Hewlett Packard model HP8595A spectrum analyzer. These plots show spectral traces obtained with a resolution bandwidth of 1 kHz and a frequency span of 500 kHz. Measurements obtained using 18 mA bias current display the highest spectral purity close to the maximum frequency of oscillation, where the highest measured output amplitude occurs. Measurements using a lower bias current of 12 mA display the highest spectral purity near the minimum frequency of oscillation, which corresponds with maximum output power. The spectral trace of the bonded circuit demonstrates the highest spectral purity. These measurements demonstrate a positive correlation between spectral purity and higher output power.

Figure 5.7 (a) Oscilloscope display of the VCO output waveform (die #3 @ 1.47 GHz)

Figure 5.7 (b) Oscilloscope display of VCO output waveform (bonded circuit @ 1.51 GHz)

Figure 5.8 (a) Spectral trace of die #4

Figure 5.8 (b) Spectral trace of die #3

Figure 5.8 (c) Spectral trace of the bonded VCO

5.8 Phase Noise Measurements

Phase noise is one of the most important criteria in the characterization of oscillators, and is a key indicator of oscillator quality. The use of the HP3048A Phase Noise Measurement System is recognized as the standard measurement technique, but an attempt to use this system was unsuccessful due to the oscillator's high phase noise. An alternate method of measurement was required to determine the phase stability of the LC VCO.

An approximate measurement technique using the HP8595A spectrum analyzer was implemented to measure the phase noise of the oscillator. This was accomplished using the following method. A resolution bandwidth of 1 kHz and an appropriate frequency span were selected. A marker was positioned at the peak of the spectral trace, and the delta marker function of the HP8595A was used to measure the loss in dB at the desired frequency offset from the carrier. The resolution bandwidth of 1 kHz contributed -30 dBc/Hz to the measurement; the measured loss was subtracted from this value to obtain a final measured result in dBc/Hz. A number of readings were taken and the results were averaged to provide estimate of the oscillator phase noise. Single-sided phase noise plots for two of the dice and the bonded circuit are shown in Figure 5.9. A bias current of 18.4 mA was used for these measurements.

Measurements taken at 100 kHz offset from the carrier were used to compare the performance of the various devices tested. There was considerable variation in the measurements depending on the device tested, bias current used, and the frequency at which the measurement was taken. Optimum phase noise performance coincides with highest output power, regardless of the current used. Worst case phase noise was -46.3 dBc/Hz for die #4 using a bias current of 12.2 mA. This improves to -58.3 dBc/Hz using a larger bias current of 17.3 mA. Best case phase noise performance using the wafer probe test bed was obtained using a bias current of 18.4 mA; the result was -67.3 dBc/Hz for die #4 and -75.3 dBc/Hz for die #3. Lowest phase noise was exhibited by the bonded circuit at -82.1 dBc/Hz, measured at 1.524 GHz. This deteriorates to -76.3 dBc/Hz at 1.504 GHz. These results are summarized in table 5.3.

In general, measured phase noise is worse than simulated except for the bonded case where the agreement is fairly good. This implies that there are other sources of noise which may have been shielded in the bonded chip. The contrast between simulated phase noise, and the phase noise of the bonded circuit measured at its maximum frequency of 1.524 GHz, is depicted in Figure 5.9 (d). Worst case phase noise predicted by simulation occurs at the highest frequency of operation, which coincides with a phase response which changes slowly as the frequency moves away from resonance. Measured results demonstrate that poorest phase noise performance occurs with lowest output power.

There are two factors which contribute to errors in simulation. The first pertains to the correct level of input noise injected into the circuit. The second is the frequency error associated with the closed loop analysis. Additional work is required to resolve these issues.

Figure 5.9 (a) Measured phase noise of die #4

Figure 5.9 (b) Measured phase noise of die #3

Figure 5.9 (c) Measured phase noise of the bonded circuit

Figure 5.9 (d) Comparison between simulated and measured phase noise

Table 5.3 Summary of phase noise measurement

Die No.	Bias Current (mA)	Frequency (GHz)	Phase Noise @ 100kHz Offset from the Carrier (dBc/Hz)
3	12.4	1.507	-66.4
	18.4	1.435	-46.4
		1.450	-64.7
		1.479	-75.3
4	12.2	1.504	-68.1
		1.524	-46.3
		1.532	-62.2
	17.3	1.424	-58.3
		1.462	-63.6
		1.470	-67.3
package	18.2	1.524	-82.1

5.9 Inconsistencies between Simulation and Measurement

It became immediately apparent during the measurement phase of this work that a considerable disparity existed between the characteristics of the circuit predicted by simulation and the results of measurement. It has been mentioned previously that the current prescribed by simulation was insufficient to produce oscillations, and had to be increased by a factor of two before even marginal behaviour could be achieved. Robust operation was accomplished only after current was increased by a factor of four. SPICE simulations were conducted to determine if the measured frequencies could be reproduced. Core circuit bias current was increased from 4.58 mA to 18.53 mA, resulting in a simulated tuning range of 115 MHz, extending from 1.499 GHz to 1.614 GHz. This is in contrast with measured results of die #3, obtained using a bias current of 18.4 mA. A maximum measured tuning range of 58 MHz was achieved, extending from 1.421 GHz to 1.479 GHz. The bonded circuit exhibited the maximum measured frequency of 1.527 GHz.

It is difficult to positively identify the reasons for these discrepancies, especially since internal nodes of the circuit are not accessible to measurement. However it is possible to speculate on the causes of the observed deficiencies.

The first proposal is that internal dc bias conditions may have been incorrect due to model inaccuracies, which could result in saturation of transistors in the core circuit. This would introduce additional non-linearity, resulting in modification of the operating characteristics of the circuit, and compromising high-frequency operation and wide tuning range. For example, the input circuit was observed to saturate for lower input voltage swings than predicted by simulations.

A second explanation for the inconsistency is that coupling between circuit elements was not considered in simulation. It was initially assumed that the separation between the spiral inductors was sufficient to minimize any stray coupling between these elements, and could be neglected in the creation of the distributed model for the on-chip inductors. In addition, capacitive and inductive coupling between metal lines used to interconnect circuit elements was also neglected. Consequently, simulations which determined the operating frequencies and tuning range may have produced erroneous results.

The third rationalization for the discrepancy is that the values of the frequency-determining components were subject to process variation. For example, an increase in inductor values by 5%, and an increase in capacitor values by 10%, will produce a 6.9% reduction in frequency, resulting in a decrease of up to 167 MHz.

5.4 Summary

The performance of the circuit was characterized in terms of frequency of oscillation and tuning range, voltage-to-frequency transfer characteristic, power dissipation, output power, sensitivity to power supply variation, and phase noise performance.

During experimental evaluation of the LC VCO, a number of inconsistencies between simulated and measured results were noted. Initial simulations predicted a frequency range of 480 MHz, extending from 1.54 to 2.02 GHz, using a total core current of 4.58 mA. When the devices were tested, this current was increased to 9.4 mA before oscillations could be produced. The circuit exhibited a very narrow tuning range of only 2 MHz using this value of current. Performance was enhanced by increasing the bias current to 18 mA where a maximum tuning range of 58 MHz extending from 1.421 to 1.479 GHz was observed for one of the devices. This resulted in a centre frequency of 1.45 GHz which is

significantly lower than the 1.8 GHz predicted by simulation. Further simulations were conducted with the same external bias resistor value ($10\ \Omega$) used in the circuit under test. A tuning range of 115 MHz from 1.499 GHz to 1.614 GHz was observed with a center frequency of 1.557 GHz. This is in contrast to the measured values stated previously. Although it has not been possible to positively identify the reasons for the observed discrepancies, a number of explanations have been proposed.

There was considerable variation in the phase noise of the devices that were tested, and proved to be contingent on output power, bias current, and immunity from external interference. Since the bonded device exhibited the most constant output power, and was shielded from external interference by the package and metal container, a comparison between its phase noise performance and simulated characteristics was considered to be relevant. Measurement at 100 kHz offset from the carrier showed a minimum phase noise of -82 dBc/Hz, with a variation of 2 dB across the frequency range. Phase noise simulations were similar for the same frequency range. However, as mentioned previously, the simulated VCO had a much broader frequency range.

Chapter 6

Conclusion

The design of a fully-integrated LC-tuned VCO was presented in this thesis. It was successfully implemented in a BiCMOS process and achieved operation in the gigahertz range. Reasonable phase noise performance was demonstrated.

Research for this work focused on the development of suitable models for the prediction of oscillator characteristics and phase noise performance. Two different approaches were taken in the development of simulation techniques used to characterize oscillator performance. The first approach utilized a small-signal equivalent circuit which was implemented as an initial step in the design process. The results of small-signal analysis were used to provide information for predicting the frequency of operation, and were a useful starting point in specifying frequency-determining component values.

In the second approach, SPICE transient analysis of the oscillator circuit was used to achieve the desired frequencies of operation and tuning range, and to realize sufficient output power. A distributed model for the spiral inductors was optimized using Touchstone to obtain component values for these elements. Final component values for the layout were obtained through fine tuning of extracted component values, so that the desired operating range and output power could be realized. Information about spectral purity, and sensitivity to temperature and power supply variations was also obtained through the use of this method.

Several considerations were required to obtain agreement between the predictions of small-signal and time-domain analyses. In order to use SPICE for open loop analysis of an oscillator circuit, the loop must be broken at some point and a voltage or current source inserted in order to perform an ac analysis of the circuit. Proper termination at the insertion point must be accomplished in order to preserve the characteristics of the circuit. Due to these difficulties, a small-signal equivalent circuit was used which replaced Gummel-Poon BJT model parameters with voltage-controlled current sources. The effect of non-linearity was considered by including a complex value of g_m in the ac model, and as a result, better agreement between small-signal and transient analysis was obtained. However, since the model used for transient analysis consists of all circuit components including extracted parasitics, and also accounts for non-linearity, this method was expected to result in better accuracy than the small-signal model.

Measurements were made and compared to the simulations. In order to start the oscillations, it was found that current had to be increased by a factor of two. An increase in current by a factor of four was required to achieve functional operation. The result was oscillation at 1.5 GHz, compared to the designed value of 1.8 GHz. Simulation using the increased current produced closer agreement with measured values. However output power and tuning range were significantly less than simulated. A shift in the values of frequency-determining components caused by process variations may have contributed to the non-ideal performance. Improvements in the modelling of coupling between the planar inductors and coupling between metal lines used to connect components should result in better correspondence between simulation and measurement. Although there were discrepancies between the simulated frequency range and measured results, phase noise simulation produced results which were more consistent with measurement.

The approach taken in this thesis demonstrated the feasibility of a monolithic tuned-circuit VCO implementation. However, the complexity of the circuit and the use of cross-coupled resonators to tune the frequency leads to higher power and poorer noise performance than would be necessary with an alternate structure. A suggested alternative is to use a single tank circuit with frequency tuning provided by an integrated varactor [Dau]. This structure provides a more suitable alternative to the design implemented in this thesis, and should result in higher circuit Q and lower phase noise.

6.1 Recommendations for Future Work

There are several modifications and alternatives that could be implemented to improve circuit performance in future designs. A simpler structure with a smaller number of reactive components can be used to reduce the effects of parasitics and minimize component mismatch due to process variation. A less complex VCO structure could be realized by the use of a single tank circuit with an integrated varactor for frequency tuning. Alternate means of tuning could be provided through the use of capacitor or inductor multipliers or scalars. A reduction in circuit complexity will enable the use of simpler models, and result in improved performance prediction.

There are several sources of error which should be considered for future designs. The accuracy of SPICE for high-frequency simulations needs to be examined. Specifically in question is the accuracy of the modelling of transistor phase shift at frequencies approaching f_T . The effect of harmonics on phase and frequency also requires further investigation. In addition, power supply noise can degrade circuit performance, and should be included

in performance analysis. To minimize the impact of power supply noise, the use of a fully differential structure should be investigated.

There are several improvements to circuit modelling which can result in better prediction of oscillator performance. The effect of bond wire inductance is significant at microwave frequencies, and is comparable in size to the inductor values used for the resonant tanks. Appropriate modelling is required to predict the effect on circuit performance. Another improvement could be obtained from the modelling of inter-inductor coupling, particularly where the separation between circuit elements is small. An additional problem is the effect of component mismatch. This can be dealt with by the use of Monte Carlo analysis. Finally, the impact of interference may be reduced by the use of circuit shielding.

In Chapter 5, the performance of the VCO was evaluated as a stand-alone component. Since this device will typically be used as part of an indirect synthesizer, it would be useful to evaluate its performance by including it in a PLL. A particular area of interest for future work is the examination of noise suppression in the loop bandwidth.

Continued research in the area of high-frequency monolithic VCO and filter design will contribute to the development of a single-chip or multi-chip module radio implementation. The use of BiCMOS technology will facilitate the combination of the high-speed capability of bipolar technology with the low power capability of CMOS for mobile radio applications.

Appendix A

BATMOS Transistor Characteristics

This section contains plots of f_T versus collector current for a range of transistor sizes available in the Northern Telecom BATMOS process. The characteristics of 1X to 45X devices are plotted for values of V_{CE} ranging from 0.5 volt to 3.0 volts.

Figure A.1 f_T versus collector current at $V_{CE} = 0.5$ V

Figure A.2 f_T versus collector current at $V_{CE} = 1$ V

Figure A.3 f_T versus collector current at $V_{CE} = 2V$

Figure A.4 f_T versus collector current at $V_{CE} = 3V$

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