Monolithic Integration of GaN HEMT with Silicon MOS Technology

by

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Abstract

This work reports on the first monolithic integration of silicon-based n-channel metal-oxide semiconductor (NMOS) transistors with GaN high electron mobility transistors (HEMT) on silicon <111> and <110> oriented silicon substrates. A windowed growth technique based on differential epitaxy was developed, which allows for GaN HEMT layers to be grown on silicon substrates while preserving regions of atomically smooth silicon for MOS fabrication. A low thermal budget fabrication process was designed that includes 2.5 μm long isolated NMOS devices alongside 0.8 μm long dual gate GaN HEMTs. Isolated NMOS devices with a gate oxide breakdown of 12.6 MV/cm and no gate leakage were successfully fabricated and tested. The performance of the GaN HEMT layers was comparable to that achieved for GaN layers grown on sapphire substrates. The saturation drain current exceeded 0.8 mA/mm with minimal current collapse, a drain breakdown voltage of 200 V and a transconductance of 191 mS/mm.

To my father

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Nomenclature

2-DEG : 2-Dimensional Electron Gas

a-Si : Amorphous Silicon

ADC : Analog-to-Digital Converter

ADS : Advanced Design System

AES : Auger Electron Spectroscopy

AFM : Atomic Force Microscopy

AlN : Aluminum Nitride

BOE : Buffered Oxide Etch

BPSG : Borophosphosilicate Glass

CAIBE : Chemically-Assisted Ion Beam Etch

CMOS: Complementary Metal-Oxide Semiconductor

CV : Capacitance-Voltage

FIB : Focussed Ion Beam

GaAs : Gallium Arsenide

GaN : Gallium Nitride

HEMT : High Electron Mobility Transistor

HFET : Heterostructure Field Effect Transistor

ICP : Inductively Coupled Plasma

LDMOS : Lateral Double-diffused MOSFET

LOCOS : Local Oxidation of Silicon

LPCVD : Low Pressure Chemical Vapour Deposition

MBE : Molecular Beam Epitaxy

MESFET: Metal Epitaxial Semiconductor Field Effect Transistor

MiM : Metal-Insulator-Metal

MOCVD : Metal-Organic Chemical Vapour Deposition

MOS : Metal Oxide Semiconductor

MOScap: MOS Capacitor

NMOS : N-type Metal Oxide Semiconductor

NRC : National Research Council

PAE : Power Added Efficiency

PECVD : Plasma-Enhanced Chemical Vapour Deposition

PMOS : P-type Metal Oxide Semiconductor

RIE : Reactive Ion Etch

RMS : Root Mean Square

RTA : Rapid Thermal Anneal

SEM : Scanning Electron Microscope

SiC : Silicon Carbide

SiN : Silicon Nitride

SIMS : Secondary Ion Mass Spectroscopy

SOI : Silicon-on-Insulator

TLM : Transmission Line Model

TMAH : Tetra-Methyl-Ammonium-Hydroxide

XPS : X-ray Photoluminescence Spectroscopy

Chapter 1

Introduction

1.1 Motivation

Gallium Nitride (GaN) transistors are an emerging technology that may soon replace GaAs devices for high-power, high-frequency applications [1]. This is due to the ability of GaN to withstand high voltage and temperatures, while maintaining high electron mobility. In order to grow heteroepitaxial GaN high electron mobility transistor (HEMT) layers, the lattice constants of the substrate and epitaxial layers must be matched in order to reduce stresses on the layers, and lower the defect density. The two primary substrates used for GaN in its development were sapphire and silicon carbide (SiC). The advantage of sapphire is that it is reasonably inexpensive compared to SiC wafers. However, because of the low thermal conductivity of sapphire, devices grown on SiC experience far superior performance due to the reduction of self-heating effects. While silicon carbide has a much higher thermal conductivity, allowing for high-performance devices, the high cost of the material makes it economically challenging to use.

Advances in epitaxy have allowed for the GaN layers to be grown on silicon <111> [2], off-cut <100> [3,4] and <110> [5] surfaces. The low cost of silicon compared to that of SiC makes it the most advantageous substrate to use, even though it

has a worse lattice mismatch to GaN and lower thermal conductivity than competing SiC substrates. Additionally, the thermal conductivity of silicon is far superior to that of sapphire substrates. Advances in epitaxy have allowed for almost stress-free and defect-free commercial GaN layers to be grown on silicon, and devices that have exceeded the 7 W/mm power level at 10 GHz and 12 W/mm at 2 GHz have been reported [6, 7].

The growth of GaN on silicon substrates presents an opportunity for the monolithic integration of silicon microelectronics with GaN HEMT structures. This integration will allow for smaller, faster, and less expensive chips, which can combine power transistors with other logic typically needed for high frequency transmit modules. In addition, the use of GaN power devices with silicon microelectronics lends itself to sensing or routing applications with built-in logic or read-out circuitry.

1.2 Thesis Objectives

The primary objective of this work is to fabricate a demonstration monolithic chip consisting of both silicon metal-oxide-semiconductor (MOS) devices and GaN power devices on a silicon <111> substrate. Overcoming the fabrication challenge of developing a joint process which yields both high-performance GaN devices, as well as MOS circuitry, is the primary goal of this work.

The National Research Council of Canada (NRC) has a well-established GaN research group, which focuses on the growth and fabrication of AlGaN/GaN HEMT devices. A mature GaN HEMT process that has already been developed at NRC has been used in combination with a custom MOS process to accomplish the integration. The MOS fabrication took place at Carleton University's Microfabrication lab. This facility, which specializes in silicon devices, is capable of making devices with a minimum feature size of 2.5 μm with in-house photomasks, and 0.8 μm with industrial

quality chrome photomasks. Additionally, an established nMOS process is run in this lab that has been adapted for use in this work. Combining the resources of both these facilities provided a unique advantage in pursuing this innovative project.

1.3 Thesis Contributions

The following is a list of the primary contributions in this work.

- Development of a windowed growth technique based on differential epitaxy which preserves an atomically smooth silicon surface for both <111> and <110> oriented surfaces following GaN growth.
- First demonstration of monolithic integration of MOS and AlGaN/GaN HEMT devices on silicon <111> and <110> substrates.
- Development of a low-temperature, gold-free joint MOS/GaN process resulting in devices of both types demonstrating good performance.

1.4 Thesis Outline

This thesis begins with a review chapter giving a summary the current state of gallium nitride technology, as well as some important developments with state-of-the-art MOS that are relevant to this work. Chapter 3 summarizes the challenges that need to be overcome in order to successfully integrate both types of devices on one chip. The methodology used in this work is based on this discussion and is presented at the end of this chapter.

Chapter 4 presents a detailed description of the windowed growth procedure, which is the critical technique developed to allow for this work to be successful. The following chapter presents the fully-detailed fabrication process for integrating the

MOS and GaN devices. TSuprem4 and Medici simulations are used to design the MOS flow [8]. The GaN process is adapted from the existing NRC process to be compatible with the MOS processing.

The results and device performance for both MOS and GaN devices are given in Chapters 6 and 7. Recommendations for improvement of the process are given as a discussion, which is followed by a conclusion that summarizes this work.

Chapter 2

Background

Gallium Nitride HEMT technology is becoming the front-runner for future high-power, high-voltage, and medium frequency applications such as cell phone infrastructure (base stations), military communications, as well as automotive and other general power conversion devices [9]. The combination of a high breakdown field, large bandgap, high mobility, and the ability to operate at elevated temperatures make GaN an ideal material for high-voltage and high-power applications. Table 2.1 gives a summary of the properties of common semiconductor materials relevant for power device applications. Diamond, a material that has a higher Johnson Figure of Merit, is plagued by poor doping control and difficulty in forming ohmic contacts [10].

The ability to form a HEMT using a GaN/AlGaN heterostructure is advantageous for several reasons; HEMT devices typically have better noise performance than MESFETs (MEtal Semiconductor Field-Effect Transistor) [9], and the mobility is high due to the formation of a 2-dimensional electron gas (2DEG), which reduces scattering effects by confining electrons away from scattering centres [9]. This makes GaN a superior choice over SiC, which to date has not demonstrated HEMTs.

The primary competitor to GaN for high-power RF applications is silicon LDMOS (Lateral Double-diffused MOSFET) technology due to its low cost. However, silicon LDMOS devices are being pushed to ultimate physical limits by present power

Material	Si	GaAs	SiC	GaN	Diamond
Bandgap (eV)	1.1	1.42	3.26	3.4	5.45
Electron Mobility (cm^2/Vs)	1350	8500	700	1000-2000	1900
Saturation Velocity ($10^7 cm/s$)	1.0	1.0	2.0	2.5	2.7
Critical Breakdown Field (MV/cm)	0.3	0.4	3.0	3.3	5.6
Thermal Conductivity ($W/cm \cdot K$)	1.5	0.43	3.3-4.5	1.3	20
Johnson Figure of Merit ($E_{br}V_{sat}/2\pi$)	1	2.7	20	27.5	50
Dielectric Constant (ε_r)	11.9	13.1	10	9.0	5.5
HEMT structures	no	yes	no	yes	no

Table 2.1: Comparison of semiconductor materials' power properties [9] [10]

and frequency demands, and hence require high-complexity modules which include linearization circuitry. GaN devices offer inherently superior linearity compared to LDMOS, reducing the need for added linearization techniques. This allows for reduced complexity, and therefore, lower cost modules [10].

2.1 Silicon Substrates

Initial demonstrations of GaN devices were grown on sapphire due to its low cost and ready availability of 2 and 4 inch substrates (Table 2.2). The primary drawback of sapphire is the poor thermal conductivity of the material, resulting in excessive heating of HEMT devices, which in turn hampers performance.

Silicon-carbide (SiC) was the next substrate to be used, and is still the best choice for high performance due to its extremely high thermal conductivity. Drawbacks of SiC are the high cost and limited diameter of the substrates.

The growth of GaN HEMT structures on high-resistivity silicon <111>-oriented surfaces was developed in 1999 by Chumbes *et al.* at Cornell [13]. Although silicon has

Substrate	GaN	AlN	Si	SiC	Sapphire
Thermal Conductivity ($W/cm \cdot K$)	1.4	3	1.5	3	0.5
Resistivity ($\Omega \cdot cm$)	$> 10^4$	$> 10^{13}$	$> 10^4$	$> 10^4$	$> 10^8$
Diameter used for Epitaxy (in)	2	2	2-8	2-3	2-4
Lattice Mismatch to GaN (%)	0	2.5	16.9	3.5	16
Thermal Expansion Mismatch to GaN $((\alpha_{L(GaN)} - \alpha_{L(x)})/\alpha_{L(x)})$	0	33	116	18.9	-25.4
Price	high	high	low	high	low

Table 2.2: Comparison of substrates available for GaN epitaxy [11] [12]

a large lattice mismatch with GaN, as well as a large thermal expansion mismatch, it provides several advantages over sapphire and SiC substrates. Table 2.2 summarizes the properties of various substrates for GaN epitaxy.

The primary advantage of using silicon as a substrate is the low cost, resulting from the years of microelectronics development using this material. Recent developments in epitaxy have also resulted in growth on 8-inch silicon substrates, compared to the maximum of 3 inches for SiC and 4 inches for sapphire [14]. This represents a step towards lower-cost GaN-on-silicon power devices.

Epitaxial growth of GaN on Si is challenging due to the large thermal expansion and lattice mismatches, but techniques to overcome this have been developed over the past decade, resulting in increased performance and reliability. Table 2.3 summarizes how the power handling capabilities of GaN HEMTs on silicon have improved over time.

The performance of GaN devices grown on SiC will always exceed that of GaN devices grown on silicon, but at a much higher cost. This is primarily due to the superior heat dissipation abilities of the substrate. The financial advantage of using silicon will certainly push SiC-based devices to the regime in which performance must

Year	Frequency	Power Density	Group
1999	4 GHz	0.5 W/mm	Cornell
2002	4 GHz	1 W/mm	CRHEA-CNRS/IEMN
2003	2 GHz	6.6 W/mm	CRHEA-CNRS/Daimler Chrysler
2004	10 GHz	7 W/mm	Triquint/Picogiga (CRHEA patent)
2004	4 GHz	12 W/mm	Nitronex
2005	2 GHz	10.2 W/mm	Nitronex
2006	18 GHz	5.1 W/mm	IEMN/Picogiga
2010	10 GHz	6.1 W/mm	Triquint

Table 2.3: Current power handling records for GaN on Si <111> substrates [13] [15] [16] [6] [7] [17] [18] [19]

be maximized. Power amplifiers delivering up to 368 W from a 60 V supply at 2 GHz have been recently reported using GaN on silicon <111> substrates [17]. However, much higher power densities have been realized with SiC substrates. Table 2.4 compares the power properties between two state-of-the-art GaN HEMTs, one grown on SiC and the other on Si. Additionally, SiC substrates may offer better stability as the lattice mismatch to the substrate is lower. The breakdown voltage may also be higher compared to silicon as there is no available leakage path through the substrate. However, breakdown voltages of greater than 1000 V have also been reported on silicon substrates [20].

Growth of GaN HEMT structures has recently been developed on off-cut <100> as well as <110> oriented silicon substrates [3] [4] [5]. This breakthrough is extremely relevant to this work as <100> and <110> are the preferred orientations for silicon microelectronics due to the lower number of interface states compared to <111>. Additionally, <110> oriented substrates are of increasing interest for state-of-the-art CMOS processes due to the large increase in hole mobility in strained devices compared to <100> oriented substrates, which have been the conventional choice in

Property	SiC (Cree)	Si (Nitronex)
Power Density at 4 GHz	32 W/mm	12 W/mm
Sheet Resistance	265 Ohms/sq	300 Ohms/sq
Sheet Charge x Mobility Product	$2.35x10^{16}$ $(Vs)^{-1}$	$2.1x10^{16}$ $(Vs)^{-1}$
Gain	16.8 dB	15.3 dB
Breakdown Voltage	Not Provided	> 200 V

Table 2.4: Comparison of properties for state-of-the-art GaN HEMTs on SiC vs Si. Values quoted at frequency of 4 GHz [7] [21]

the past [22].

2.1.1 Growth on <110> Silicon

< 110 >-oriented silicon substrates are of increasing interest for this work as GaN epi-layers can be grown on them without having to use off-cut, specially made substrates, unlike the <100> orientation. Additionally, <110>-oriented Si substrates are currently being explored for state-of-the-art CMOS fabrication as the hole mobility has been shown to increase by 160% for pMOS devices compared to conventional <100>-oriented substrates [22]. Meanwhile, the nMOS mobility is only reduced by between 49% and 34% depending on the direction of current flow [22]. Although the nMOS mobility, and hence current drive, is reduced, the large increase in pMOS performance reduces the disparity in speed between nMOS and pMOS devices, which may allow for an overall speed increase for logic applications. The primary concern for <110>-oriented substrates, especially for RF and microwave applications, is the higher noise and gate leakage compared to <100> silicon due to more electron-trapping states being present at the Si/SiO_2 interface. However, with the movement towards high-k dielectrics, which are often deposited rather than grown, the problems caused by the higher density of states can be mitigated, eliminating a major obstacle for this

technology [23].

2.2 GaN HEMT Technology Overview

GaN High Electron Mobility Transistors make use of a Schottky gate to control a device channel, formed by a vertical heterostructure of $Al_xGa_{1-x}N$ and GaN layers. The device channel in this case is a 2-dimensional electron gas (2-DEG), which is formed at the interface of the GaN and AlGaN layers. A combination of the spontaneous polarization and piezoelectric polarization of AlGaN induces the 2DEG, which is trapped by band offset [24].

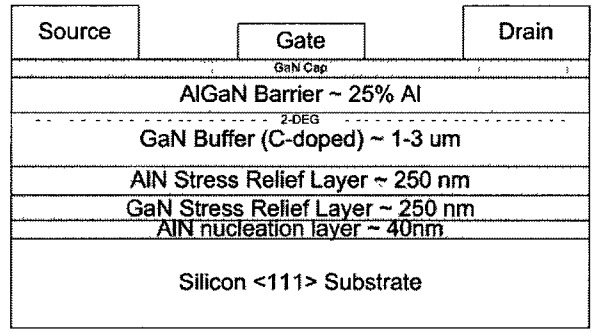


Figure 2.1: Typical GaN HEMT layer structure for growth on silicon <111> substrates

Figure 2.1 shows a typical GaN HEMT layer stack, including the location of a 2DEG. MOCVD (Metal-Organic Chemical Vapour Deposition) or MBE (Molecular Beam Epitaxy) techniques are used to grow these layers on silicon $< 111 >$ substrates. The band diagram for this structure is shown in Figure 2.2.

2.2.1 Growth and Process Description

A thin aluminum-nitride nucleation layer is used to initiate the growth of GaN on the silicon substrate. This nucleation layer is also used for stress relief between the GaN stack and the silicon substrate.

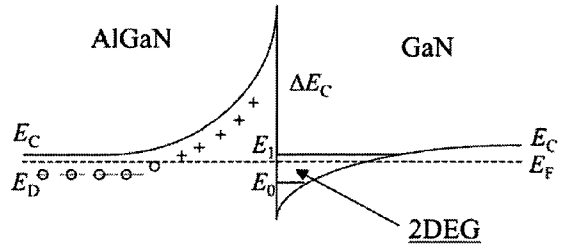


Figure 2.2: Conduction band diagram of GaN HEMT [25]

The next step in the growth process is to grow a 250 nm thick GaN layer, followed by a 250 nm thick AlN layer. This is done in order to provide a stress relief layer before the thick GaN buffer is grown. Upon relaxation after growth, micro-cracks typically form in this stress relief layer, which alleviate the stress in the GaN buffer and channel regions.

The GaN buffer layer is typically in the order of 1 μm to 3 μm thick to minimize the number of dislocations at the crystal surface. As this layer is made thicker, the quality (reduced dislocation density) improves at the cost of higher stress. This layer is typically desired to be semi-insulating such that the devices are electrically isolated. NRC uses a carbon-doping technique to improve the insulating properties of this layer [26]. Iron doping is also commonly used to improve the insulating properties of the GaN layer [27]. Often, when grown by MBE, this layer is naturally insulating.

A thin AlGaN barrier layer, typically in the order of 10-100 nm, is then grown to produce an electron-confining heterojunction that forms the 2-DEG. A piezoelectric polarization component is caused by the tensile strain resulting from the growth of AlGaN on GaN. This adds to the spontaneous polarization that already exists in the GaN. The addition of both of these polarization components gives a positive charge at the interface, which in turn results in the formation of an electron gas right below the interface. The aluminum concentration and thickness of the AlGaN determine the charge density of the 2DEG [28]. Additionally, ultra-thin pure AlN spacer layers

can be used in the cap to increase confinement.

Extremely thin (10 Å) GaN cap layers have also been deployed on the top of the structure in order to increase the Schottky barrier height of the gate contact [29]. In addition, the GaN cap layer improves reliability by preventing the oxidation of aluminum in the AlGaN barrier layer. The growth process used for this work is presented in more detail in Section 4.2.1.

Thin-film metal stacks are used to form ohmic contacts to both the source and drain. Typical strategies include the use of Ti/Al/Ti/Au or Ti/Al/Ni/Au stacks, which are subsequently rapid thermal annealed at approximately 850°C. Ohmic contacts to AlGaN/GaN are challenging because of the large bandgap, and hence, multilayer alloys are needed to provide a low work-function contact and reduce the potential barrier to the metal. Section 5.4 provides a detailed explanation of ohmic contact operation and formation. Schottky gates are formed using Pt/Au or Ni/Au stacks.

2.2.2 HEMT Operation

Unlike conventional silicon MOSFETs, the HEMT is in the "ON" state when no voltage is applied to the gate. If a potential is placed across the drain to the source, current will flow. Once a negative potential is placed on the gate, the concentration of carriers in the 2-DEG is reduced. The negative potential that fully turns off the channel is known as the pinch-off voltage. The high mobility of the 2-DEG layer allows for high transconductance, and high frequency operation. Additionally, the large bandgap (3.4 eV) results in very high breakdown voltage and higher temperature operation as electrons from the valence band need much more energy to be excited to the conduction band.

2.3 GaN Innovations

Initial development of GaN HEMT devices was plagued with an effect termed "current collapse," which refers to a sagging of transistor IV curves after sustained operation with the channel pinched off and large drain bias. The source of this collapse was attributed to surface states trapping charge on the drain side of the gate, causing a virtual-gate effect on the channel [30]. The primary technique shown to mitigate the effect of these traps is to deposit a SiN passivation layer over the entire device [9]. The SiN passivation provides atomic hydrogen to the surface, which satisfies the dangling chemical bonds forming the traps [9]. Modern devices no longer experience current collapse as the SiN passivation is universally employed. Figure 2.3 shows the effect of the SiN passivation on a sample from NRC.

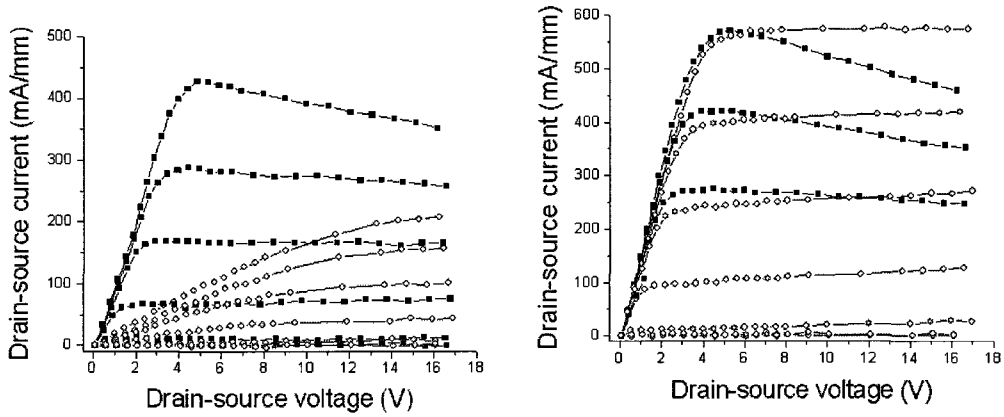


Figure 2.3: Non-passivated (left) and passivated (right) device IV curves showing mitigation of current collapse using pulsed measurements on sapphire substrates (pulsed measurement represented by squares, continuous sweep represented by circles).

Another innovation that has improved the performance of GaN devices is the introduction of a field plate. A field plate is an extension of the gate over the drain side of the device used to reduce the peak electric field that forms near the drain-side edge of the gate [9]. This has been shown to significantly increase the breakdown

field of the device and is almost always used for high-power devices [31].

2.4 Low Temperature MOS processing

The thermal budget of the MOS processing is the total amount of thermal stress that the wafer experiences. Minimizing the thermal budget is a primary obstacle in this work as will be shown in Section 3.3. Hence, in order for this technology to be commercially viable, there must be a method to fabricate state-of-the-art MOS devices while keeping the thermal budget minimized.

Historically, high temperature steps in MOS processes have been needed for the gate oxidation, as well as for annealing damage and activating dopants following implants used to form source and drain junctions. The need for increased transistor scaling and geometry minimization has forced the industry to move from a silicon-dioxide based gate dielectric to a high-k material, such as a HfO_2, HfSiO, and HfSiON [32]. This in turn has greatly reduced the thermal budget allocated to this step, as these new compounds are typically deposited using atomic layer deposition, which is performed at lower temperatures(200°C-400°C) compared to silicon oxidation.

Thermal budget minimization is also needed to reduce diffusion of implanted junctions in order to avoid short channel effects in small geometry FETs [33]. Two techniques that have been recently developed to successfully anneal and activate dopants in junctions, but not cause unwanted diffusion, are laser annealing and flash lamp annealing [34] [33]. Flash lamp, or spike annealing, involves heating the sample to elevated temperatures (between 950°C and 1200°C) for between 1 and 10 seconds. This technique has been shown to effectively form shallow junctions, allowing for technologies smaller than 50 nm, which cannot be accomplished using conventional RTA techniques. Laser annealing is an alternative to spike or flash lamp annealing that can anneal for bursts in the millisecond range, allowing for the formation of

shallower junctions [34]. This technique has been used to push MOS technology to gate lengths smaller than 30 nm.

2.4.1 Low Temperature Oxidation of Silicon

The growth of a high quality gate oxide is the most important step in fabricating silicon MOS devices. Because of the thermal budget constraints of this work, it is important to examine the minimum temperature and conditions that can be used for this step, without sacrificing device quality. Traditionally, thermal gate oxides have been grown at temperatures greater than 1000°C in order to produce a high quality film which has low leakage and high dielectric strength [35]. EerNisse *et al.* have also shown a significant stress reduction in SiO_2 layers grown at temperatures above 950°C, which is the viscous flow point of the film [36].

It has also been shown however, that quality oxide films can be grown in a two-step approach, which consists of a lower temperature deposition, followed by a post-oxidation anneal [37, 38]. Quality oxides have been demonstrated with growth temperatures as low as 800°C followed by a post-oxidation anneal at temperatures of 950°C and above, which allows for thermal relaxation to take place. The duration of these anneals vary, but the minimum time has been shown to be approximately one minute [37]. Quality is shown to improve with anneal time as well. This two-step approach could be useful in overcoming the thermal budget challenges that this particular project presents.

These processes however, have been developed on the <100> orientation of silicon. There is little literature on low temperature oxidations on the remaining two orientations, which are used in this work. Early research has shown that other orientations of silicon result in oxides that have approximately three times the quantity of interface states as well as increased growth rates [39].

2.5 Towards an Integrated Technology

Fujikawa *et al.* have grown a GaN layer on an SOI substrate consisting of a silicon <100> substrate, a buried oxide, and a thin silicon <111> top layer [40]. This process enables the recovery of a smooth silicon surface, necessary for potential MOS integration. The oxide under the top-level silicon layer acts to protect the underlying surface. An advantage of this technique is the ability to grow on a silicon <111>-oriented surface, which is bonded to a <100>-oriented substrate: the preferred orientation for MOS fabrication. HEMT layers have yet to be grown in this manner. This technique may be limited by the availability of custom SOI wafers, as it requires a highly specialized order due to the different wafer orientations and small diameter. However, this could still be more cost effective than the use of SiC substrates.

Shichijo *et al.* have integrated MOS with GaAs MESFET devices [41]. This is the first example of integrating MOS devices with III-V technology. An advantage of integrating GaAs with MOS as opposed to GaN is the ability to grow the GaAs selectively in a silicon trench at reasonably low temperatures. GaAs can be grown in the 450°C range, whereas GaN epitaxy reaches a temperature range from at least 800°C to more than 1000°C for several hours. This difference in growth temperature allows for a much more relaxed thermal budget when designing the MOS process, as the effect of the GaAs growth on the doping profile was negligible for the technology that was used at the time. Although a MOS-first approach would be better, current sub-micron technology would not be able to withstand the GaN HEMT growth step, and hence an approach discussed in Section 3.2 has been taken for this work.

An example of a combined GaN/CMOS hybrid chip has also been implemented by Matsunaga *et al.* [42]. Similar to the circuit to be implemented in this work, a dynamic gate supply voltage circuit in CMOS is used to improve the linearity and efficiency of a class-B GaN power amplifier. It is evident that the ability to integrate

both CMOS and GaN transistors on the same chip would be highly beneficial to this technology.

Chung *et al.* have recently accomplished a similar integration to that of this work by using a very different technique [43]. This is based on a wafer-bonding scheme that allows for the use of <100> oriented silicon for the MOS devices, which is currently the preferred orientation for this technology. This involves attaching two wafers together using an adhesion layer and the application of high pressure. The disadvantage to using a wafer bonding technique, however, is two-fold. Firstly, the maximum substrate size that can be bonded is very limited, currently set at one square inch. If this technology is to be economically feasible for mass production, the substrate size must be increased substantially. Secondly, the long-term reliability of such a technique has not been well-studied. This is especially important for GaN-based technology; one of its primary strengths is the ability to operate in harsh environments.

The present work, which is based on an epitaxial process that monolithically integrates both MOS and GaN technology, is better suited for commercialization, as there are no obstacles to limit scaling to much larger substrates. In addition, there is less concern about long-term reliability due to the nature of the process. The MOS devices are not based on a <100> oriented substrate, but it appears that <110> oriented silicon could house devices with comparable performance as research continues in this field.

Chapter 3

Integration Strategy and Considerations

In this chapter the primary challenges involved in the monolithic integration of GaN HEMT and MOS technologies are discussed at a strategic level without delving into a high level of detail about the process. There are multiple ways to approach the integration problem, but only a few that are able to overcome the processing obstacles are presented. It is imperative that a process be designed in which the performance of both GaN and MOS devices is not compromised. Growth, fabrication, and thermal issues are all taken into account. The strategy used to approach the integration problem in this work is then given, which is based on the qualitative observations presented here.

3.1 Growth Considerations

The first major challenge that must be considered is finding a method by which to obtain regions of atomically smooth silicon alongside active GaN layers on the same substrate. It is important that the silicon surface be of the utmost quality for a good Si-SiO_2 interface for the MOS devices. The simplest way of attempting this is to simply etch away regions of GaN on a full planar growth to expose the silicon surface. However, this does not result in an atomically smooth surface as shown in Section 4.1.

This technique could be feasible by growing on a silicon-on-insulator (SOI) wafer, and then wet etching away the silicon film and buried oxide after removing the GaN, but the availability of <111> or <110> oriented SOI is low. However, the SOI idea is attractive if the <100> orientation is specifically needed for the MOS devices, as a <111> on <100> wafer can be prepared.

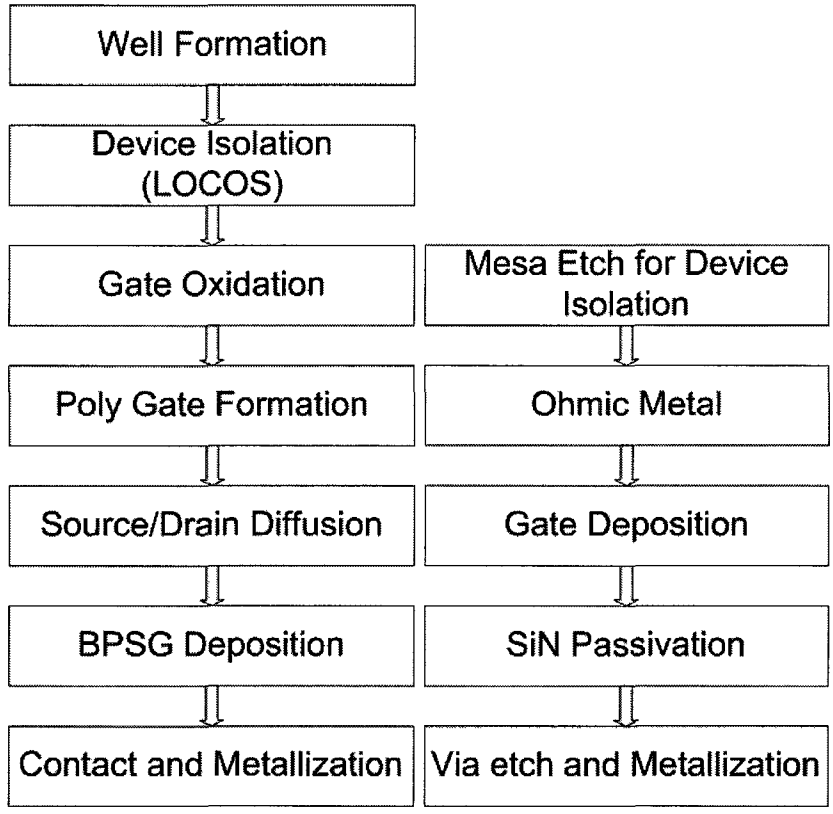
An alternative approach is to attempt selective growth, in which growth occurs only in specific areas of the silicon wafer, to preserve regions for MOS integration. This technique requires preparation of the silicon sample before growth, which may compromise the smooth silicon surface or introduce unwanted materials into the growth chamber. Although the orientation of the silicon may not be ideal for state-of-the-art CMOS, this approach may give an advantage with respect to preserving an atomically smooth surface for growth.

3.2 Processing Background

Figure 3.1 shows the main steps for both a CMOS and GaN process flow that can be performed with current technology available at Carleton University and NRC, respectively.

There are a few observations from these flows that have important consequences for integrating them. Firstly, all MOS process steps except for the contact formation and metallization require temperatures of 900°C and above. Typically, the gate and field oxidations require over 1000°C.

The GaN process is far simpler than the MOS, as it requires fewer steps and no long high-temperature exposure. The only high-temperature steps that are required are to anneal the ohmic contacts, which is typically done at 850-900°C. The only step of the GaN process that is able to withstand any of the MOS processing would be the mesa etch. After metal is deposited for the ohmic contacts, no more long-term



(a) Standard CMOS Flow (b) Standard AlGaN/GaN HEMT Flow

Figure 3.1: Primary steps for both CMOS and GaN processes

high temperature steps can be performed on the sample. The only steps of the MOS process that cannot withstand high temperatures are the back end metallization steps. This suggests that the order in which the steps are performed is not interchangeable.

A similar module in these two flows is the final back-end process, which includes the final metallization steps. Both need contact or via etches through a dielectric followed by a metal fill. Aluminum is currently used for the MOS process, and gold is used for the GaN process as it has higher resistance to electromigration. Unfortunately, gold is not compatible with the CMOS process. Some changes will need to

be made to accommodate this (see Section 5.3). Connecting both types of transistors is an important part of the back-end process. A common metal scheme must be found that satisfies the performance requirements of the devices. Additionally, Metal-Insulator-Metal (MiM) caps and spiral conductors can be included in this stage of the process.

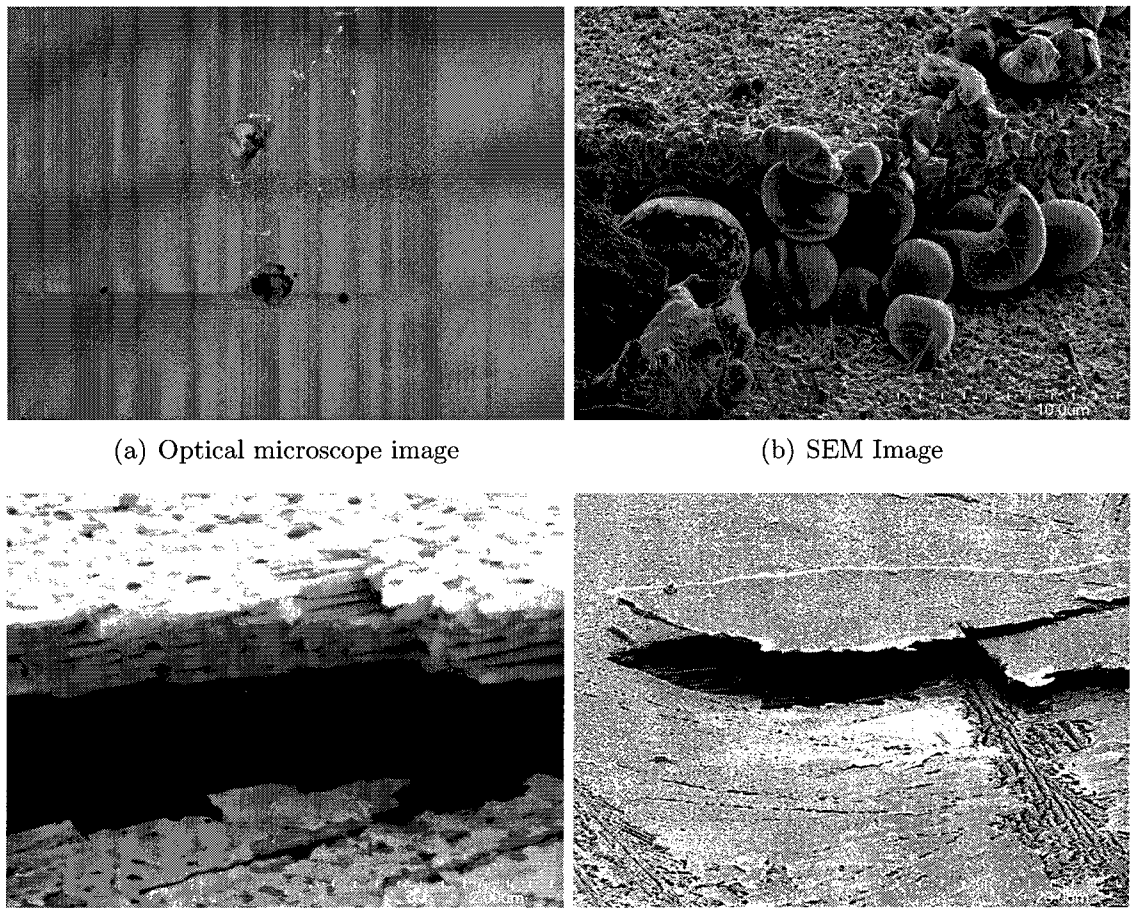
Another factor that must be accounted for is the step height expected between the silicon regions and the GaN stack, which is typically around 2 μm. This will depend on the approach used to obtain a wafer with areas for MOS and GaN devices.

Combining the processing steps also means that some thought must go into protecting the MOS or GaN regions of the chip while processing is performed on the other regions. Ideally these steps can be built into the process without much added work. A preferred solution is to use existing steps in these flows, such as thick dielectric depositions, to double as protective layers. Extra photolithography steps that protect MOS or GaN regions of the wafer while processing is performed on the other region are also needed.

3.3 Thermal Budget Considerations

From the above discussion it is clear that a major concern in integrating MOS with GaN devices is the ability of the GaN HEMT layers to withstand the thermal budget of the MOS processing. Preliminary experiments run with a standard HEMT growth on an Si <111> substrate revealed how difficult this issue would be. Pieces of the same wafer were annealed at different temperatures for 2 hours in a nitrogen environment in order to mimic the thermal stress of the MOS process. Before annealing, the samples were passivated with a thick PECVD oxide to cap the GaN and mitigate GaN decomposition. Figure 3.2 shows the resulting SEM and optical microscope images when a sample was annealed at 1000°C for 2 hours. Decomposition occurs

along line defects in the GaN as shown by the optical microscope image in Figure 3.2a. This image shows cracking along the defects as well as sites in which lift-off of the layers has occurred. Dissociation of GaN is the most likely reason and causes lifting off of different layers. This has been shown to occur at elevated temperatures [44–46]. Ga droplet formation is also shown to occur as per Figure 3.2b, which is a sign of dissociation. 3.2c and 3.2d show the lifting of layers due to GaN decomposition after the oxide has been removed.



(a) Optical microscope image

(b) SEM Image

(c) SEM Image - oxide stripped

(d) SEM Image - oxide stripped

Figure 3.2: Optical and SEM pictures of sample annealed at 1000°C

At 900°C decomposition was not observed, but was observed at 950°Cto a lesser

extent. Moreover, the extent of decomposition varied between different growth runs. This is consistent with the work of Song *et al.* [47] as well as Stonert*et al.* [48], which shows GaN is mostly stable at 900°C , after which decomposition occurs. However, a capping layer such as SiO_2 should mitigate decomposition as shown in [49] when used to suppress N dissociation from AlGaN layers during Si implant activation annealing. An AlN capping layer could be considered for this work, but would be very difficult to remove after MOS processing [50]. In addition, reducing the oxide thickness and using a higher quality deposition technique may be needed. The issue of GaN stability must be resolved before MOS fabrication is to take place. It is imperative that a process flow with a limited thermal budget be designed in this case, as this appears to be the major obstacle in successfully accomplishing this integration.

An alternative approach could be to perform the MOS fabrication prior to GaN growth altogether. This would circumvent the issue of GaN decomposition as all the high temperature processing steps could be performed prior to growth. Additionally, the gate oxidation temperature would not be limited, ensuring a high quality layer. This method however, would not be compatible with current state-of-the-art CMOS processing as the thermal budget required for GaN growth would cause unwanted diffusion of shallow junctions, limiting the device geometry and overall performance. There is also the added risk of contamination to the atomically smooth silicon surface required for GaN growth due to the increased number of processing steps performed prior to epitaxy.

3.4 Thermal Performance Considerations

In order to integrate these two technologies, thermal effects must be taken into consideration as elevated temperatures hamper device performance. Thermal simulations will be able to predict the behaviour of this chip, allowing for the intelligent layout

of different components. Previous work in [51] has shown that the thermal gradient resulting from heat generated by the GaN power device has little effect on the chip for separations greater than 20 μm from the source, due to the poor thermal conductivity of the silicon substrate. The primary issue discovered by this work is that localized heating of the GaN should be more of an issue, and hence techniques are needed to properly cool the power devices.

3.5 Final Approach

Figure 3.3 shows a cross-section of the planned co-integration process. A windowed growth technique has been developed that isolates the silicon surface and the GaN layers on the chip such that both are available for fabrication. This technique is more elegant and cost effective than using a growth on SOI or etching approach, but does have the disadvantage of using <111> or <110> oriented silicon. Chapter 4 gives a more in-depth discussion of this process.

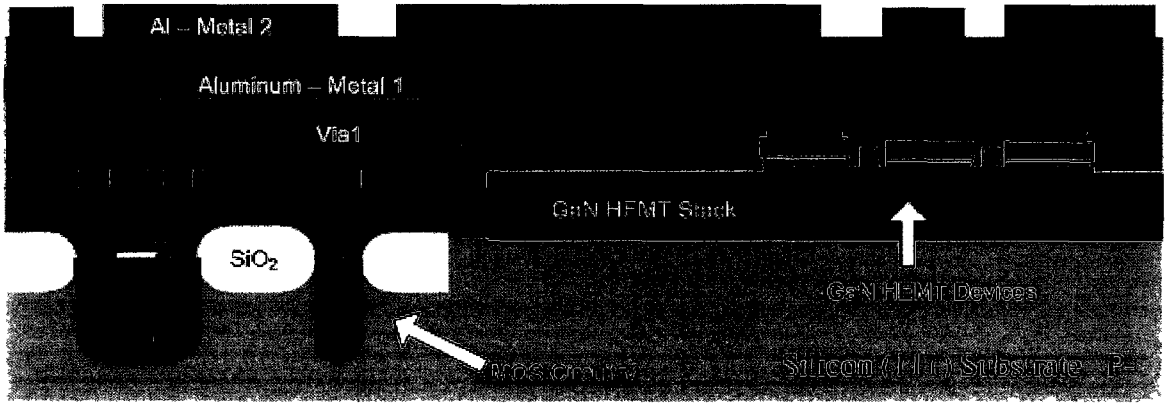


Figure 3.3: Cross section of envisioned co-integration process

The MOS devices are fabricated prior to the GaN devices as the high temperature required for the MOS processing, especially the thermal oxidations, will impact the GaN metallization. It should also be noted that due to the high temperature required for GaN growth, and the high quality of surface required, MBE growth must be

performed at the beginning of the fabrication process. It is also important to minimize possible contaminants to the silicon surface before growth in order to obtain quality GaN layers.

A joint metallization will be performed in this process in order to take advantage of the similar back-end steps. Unfortunately, gold cannot be used as it forms recombination/generation centers in silicon, resulting in leaky junctions. However, aluminium, which is typically used for MOS processing can also be used for GaN. There is a small performance penalty to pay, as gold has slightly lower resistivity and better electromigration resistance. Overcoming the topological difference on the chip between the GaN and NMOS transistors may pose challenges. The GaN HEMT structure, which is typically around 2 μm thick, has a very thin AlGaN cap layer that does not allow for the height of the GaN stack to be modified. Because of this, the topology will not be uniform and a technique such as a dielectric fill or reflow must be used to facilitate uniformity for metallization. Additionally, the difference in height of the MOS and GaN surfaces may pose future challenges for lithography.

A MOS process that does not exceed 950°C has been designed. This will mean that growing a good quality gate oxide for the MOS devices could be a challenge. An alternative approach would be to use a deposited gate dielectric as is used in modern CMOS technology as discussed in Section 2.4. In order to be certain about the thermal budget required, annealing tests as described in Section 3.3 were performed on new growths to determine the maximum temperature they can withstand, as this was found to vary between growths.

The GaN processing steps only require a small change to the metallization scheme to avoid gold. A uniform coating to protect this region will be used during the MOS fabrication.

The detailed process design is presented in Chapter 5.

Chapter 4

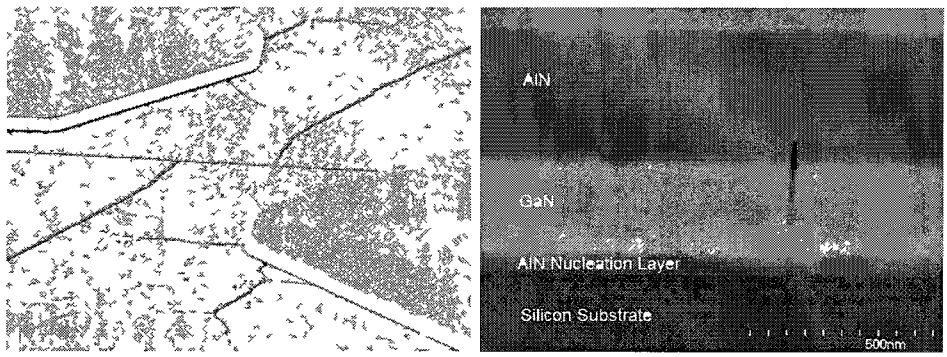
Windowed Epitaxial GaN Growth on Silicon

A primary challenge in integrating MOS devices into a typical substrate used for GaN epitaxy is to recover an atomically smooth silicon substrate for MOS fabrication. This chapter will first summarize the primary obstacles in obtaining such a surface, and present a new method developed in this work that allows for selected areas of the silicon substrate to be preserved for MOS fabrication. The electrical and mechanical properties of the resulting wafers are then discussed.

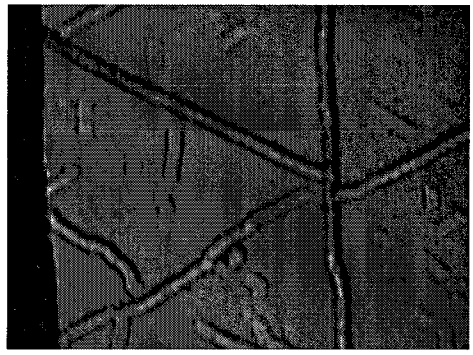
4.1 Primary Challenges

In the case of full wafer planar growth as described in Section 2.2.1, recovering a smooth silicon surface by etching the AlGaN/GaN heterostructure layer is complicated. Buried cracks in the buffer layer stack usually used to compensate the strain [52] can be translated into the silicon surface. An additional concern is the possibility of a change in silicon morphology and purity due to the Si/AlN interface used at the early stage of the growth. Figure 4.1a illustrates the pattern of buried cracks transferred into the silicon surface during Inductively Coupled Plasma (ICP)

etching to remove the AlGaN/GaN stack. Focussed Ion Beam (FIB) imaging shows that these cracks originate between the AlN and GaN stress-relief layers (Figure 4.1b) The poor silicon morphology would interfere with MOS fabrication.



(a) Etched GaN (b) FIB Section



(c) Smoothing

Figure 4.1: a SEM image of AlGaN/GaN heterostructure ICP etched down to the silicon surface. Note the poor quality of the silicon surface which includes both cracks and surface pits. b. FIB Section of wafer showing cracks originating between the stress relief layers. c. Optical microscope image of an attempted smoothing of microcracks using TMAH.

Attempting to smooth the silicon surface by wet etching using TMAH [53,54] and NH_4F [55–57] did not improve the silicon morphology. The microcracks etched into the silicon surface expose new etch planes to the crystallographic etch, which causes wider channels to form in the surface. This is demonstrated in Figure 4.1c.

Growth using maskless mesas on silicon <111> substrates using patterned AlN

nucleation layers is another option in pursuing a co-integrated technology [58]. However, there is no way to protect the exposed silicon growth from contamination during growth, making it challenging to incorporate MOS devices.

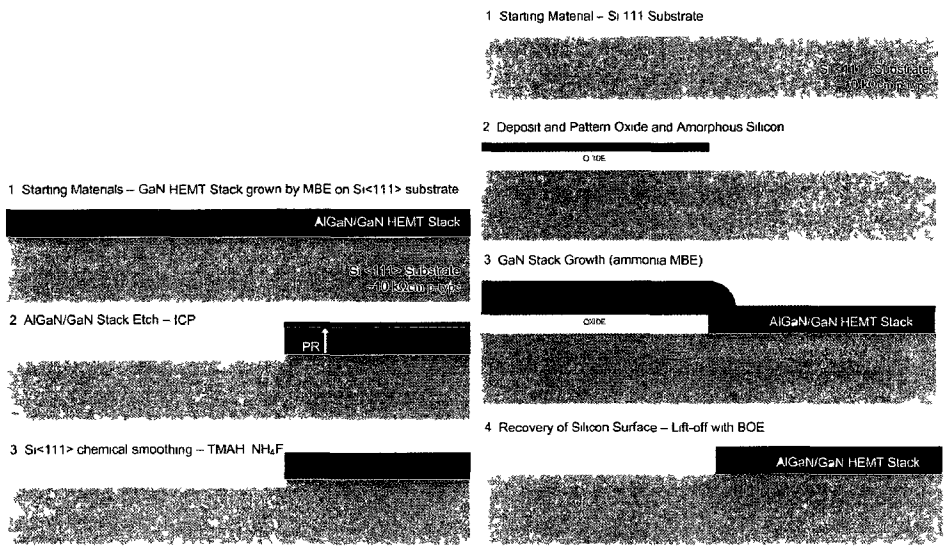
4.2 Windowed Growth

A new windowed growth technique has been developed which preserves the smooth surface of the silicon substrate during MBE growth of the GaN heterostructure [59]. Rather than attempting to recover the silicon surface after growth, this technique, known as differential epitaxy, uses a dielectric passivation to protect the surface before growth by ammonia MBE [60]. A thick dielectric coating of silicon dioxide followed by a thin amorphous silicon layer is deposited uniformly over the entire substrate. A combination of dry and wet etching is used to open up windows in the dielectric, exposing the silicon surface for epitaxy. The role of the amorphous silicon is to allow for nucleation on the surface, that in turn can be lifted off by simply wet-etching the SiO_2. In addition, the amorphous silicon prevents exposure of the SiO_2 layer during growth, as oxygen contamination in the GaN buffer layer may be an issue.

Figure 4.2 summarizes the two techniques used to isolate a smooth silicon surface. As discussed, etching and smoothing is not a viable option due to the microcracking in the GaN stress-relief layers.

Figure 4.3 shows the wafer before MBE growth. The silicon surface for epitaxy appears very smooth, which should ensure a good quality GaN HEMT. The thick silicon dioxide is used for lift-off.

Figure 4.4 shows the silicon surface after windowed growth. Note the smooth appearance in stark contrast of that to Figure 4.1, in which dry etching was used after growth of the AlGaN/GaN heterostructure. The development of this technique has been the major enabling step that allows for MOS integration with AlGaN/GaN



(a) Etch and Smooth (b) Windowed Growth

Figure 4.2: Comparison of growth techniques

HEMTs.

4.2.1 Detailed Growth Process

Dielectric Coating

The original windowed growth technique employed a 1.8 μm thick dielectric coating of silicon dioxide, followed by a 0.1 μm thick amorphous silicon layer deposited uniformly over the entire substrate. The oxide layer was deposited using a model 700 Plasmatherm PECVD system, with an RF power of 40 W and temperature of 350 °C. The a-Si layer was deposited using a custom magnetron sputtering system with a boron-doped silicon target, using a power of 100 W at room temperature. The custom system consists of guns from US Inc. (US Gun II model), an Advanced Energy MDX-1K power supply, and a CTI model CT8 cryo pump.

Due to poor adhesion of a-Si to the oxide layer in some samples, the a-Si step

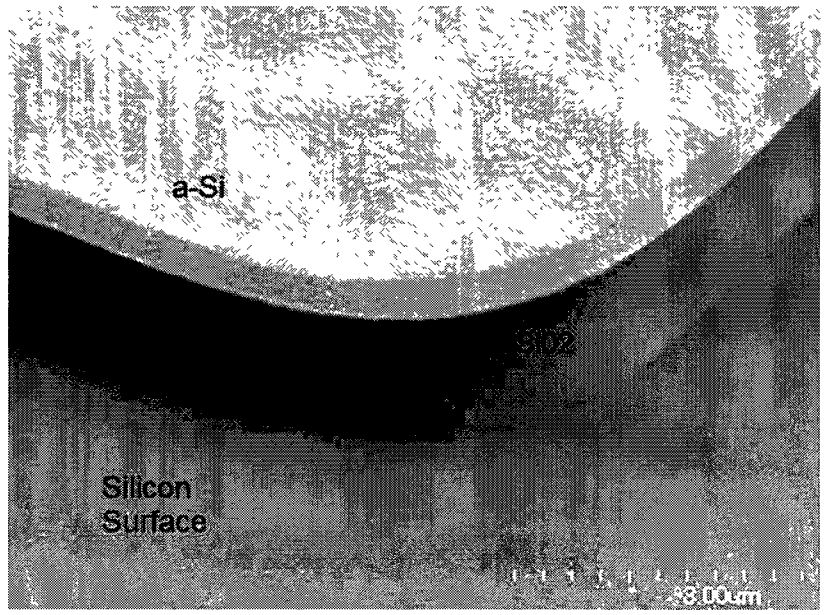
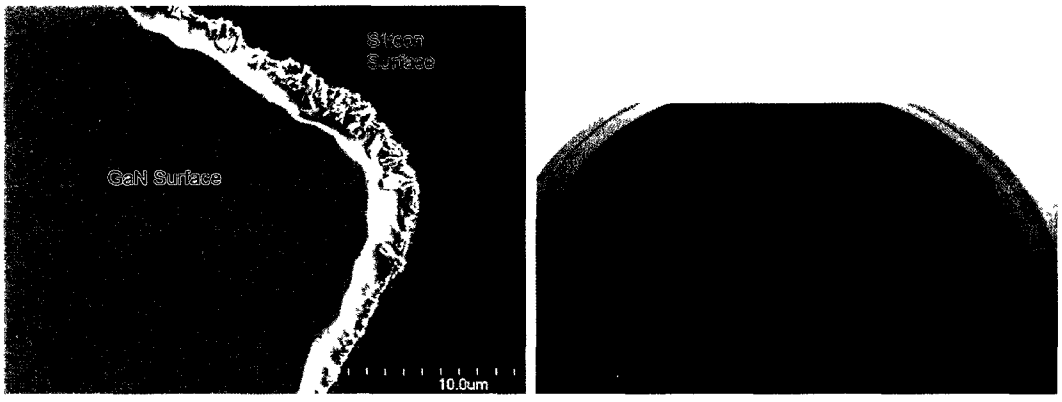


Figure 4.3: Wafer before MBE growth step. Note smooth silicon surface available for epitaxy.

was changed from room temperature sputtering to a 560°C LPCVD a-Si deposition, followed by a 1 hour anneal to crystallize the layer at 560°C. Additionally it was determined that a 1 μm oxide layer is adequate for lift-off rather than 1.8 μm, reducing the probability of oxygen outgassing.

In both cases a combination of dry and wet etching are used to open windows in the dielectric, exposing the silicon surface for nitride epitaxy such that there is no etch damage. First, an ICP etch using a C_4F_8 and O_2 chemistry is used to etch until approximately 100 nm of SiO_2 is left on the silicon areas. Next, a buffered oxide etch (BOE) with surfactant is used to etch the remaining SiO_2 down to the silicon surface. This method results in a slight undercut of the protective dielectric, but avoids plasma etch damage to the silicon surface, which may result in a poor growth quality. The slight undercut is beneficial in facilitating GaN liftoff.



(a) SEM image of GaN and Silicon on same substrate.

(b) Full wafer showing Silicon Windows.

Figure 4.4: Windowed growth images

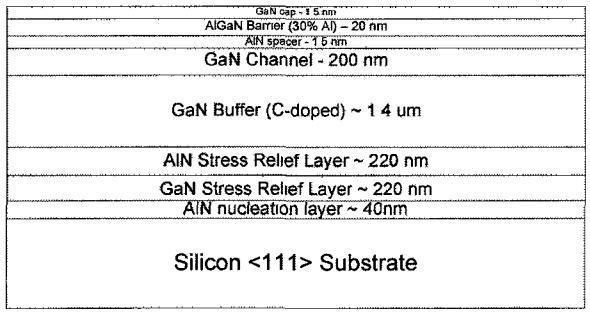
Epitaxial Growth

Samples are grown by MBE using ammonia as the nitrogen precursor. Initially, carbon-doped material was used in order to increase the resistivity of the buffer layer, however in order to simplify the growth, unintentionally-doped GaN layers were used instead. A description of both techniques is given.

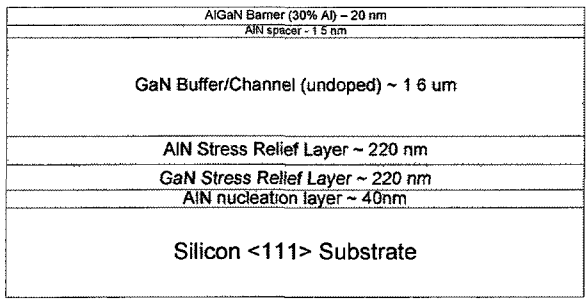
After window fabrication, but immediately prior to the growth, 2" high resistivity silicon <111> substrates are chemically cleaned and then the native oxide is removed using an HF/H_2O solution. This etch time is short so little of the SiO_2 mask is removed. Once loaded in the growth reactor, substrates are heated to about 700°C to desorb the hydrogen present at the surface, and a 7x7 surface reconstruction is observed using RHEED (Reflection High-Energy Electron Diffraction). A growth process identical to the one used in reference [61] is applied. It consists of first growing a 40 nm AlN layer at a typical growth rate of 0.1 mm/h while the growth temperature is increased from 650°C to 920°C. Then GaN and AlN stress relief layers, both about 250 nm thick, are grown at 800°C and 920°C, respectively. This technique has been shown to absorb the tensile stress due to the high lattice and thermal expansion coefficient mismatch of the silicon substrate relative to the GaN layers [61]. Next, a

thick 1.4 μm C-doped GaN buffer layer is used to improve electrical insulation [26]. The structure is completed by growing the active layer, which consists of a 200 nm undoped GaN channel, a thin AlN spacer, and an AlGaN barrier (20 nm at 30%) covered by a 2 nm GaN cap layer. The ammonia flow rate is maintained constant over the whole growth process at 200 sccm.

Unintentionally doped material (i.e. without carbon doping) follows a similar process described above except that the methane gas used to dope the GaN buffer layer with carbon is not used. The 0.2 μm undoped GaN layer is therefore not included since the entire buffer layer is unintentionally doped. Although no extra dopant is added, defects in the growth and background contamination make the buffer layer semi-insulating. In addition, no GaN cap layer is used. Figure 4.5 shows cross sections of both structures.



(a) Carbon-doped growth layer structure.



(b) Unintentionally-doped growth layer structure.

Figure 4.5: GaN layer structure for growth on silicon <111> substrates

Property	C-Doped Growth	Unintentionally-doped Growth
Sheet Resistance	442 Ohms/sq (hall bars)	445 Ohms/sq (corbino)
Mobility	$1.37x10^3$ cm^2/Vs	917 cm^2/Vs
Sheet Carrier Concentration	$1.03x10^{13}$ cm^{-2}	$1.07x10^{13}$ cm^{-2}
T-max before decomposition	<950 °C	>950 °C
Forward Current Achieved	0.60 A/mm	0.81 A/mm
Pinch-off Voltage	-5.6 V	-3.3 V
Leakage Current (Vgs=Vds=-10 V)	$1x10^{-2}$ A/mm	$1x10^{-2}$ A/mm

Table 4.1: Comparison of the properties of the best C-doped and non C-doped growth wafers

4.2.2 Windowed Growth Wafer Properties

The properties of the gallium nitride layers produced by this technique must be comparable to those for full planar growths in order for this work to be of value. The electrical properties of the windowed growth layers have been characterized using hall measurment and capacitance-voltage (CV) analysis. SIMS has also been used to examine the oxygen concentration in the buffer layers.

Hall Measurements

For the initial C-doped samples Hall bar structures were formed by first dry etching the GaN using a chemically assisted ion-beam etch (CAIBE) to form isolated mesas. This was followed by a Ti/Al/Ti/Au ohmic metallization. For the non C-doped samples, cylindrical symmetry TLM structures (Corbinos) were used to determine sheet resistance, as well as the ohmic contact resistance [62]. A Hall probe measurement on the full wafer was utilized to determine the mobility and carrier density. These properties are summarized in Table 4.1.

The sheet resistance and carrier density for the unintentionally-doped samples were very close to that of the C-doped samples, but the mobility was slightly lower.

The results for both types of growth are comparable to that of a full planar growth on silicon, suggesting that this technique does not degrade the quality of the GaN layers. These values do vary for each growth due to the variability of growth parameters that are used during the epitaxial process.

CV measurement

The free carrier density deduced from capacitance-voltage (CV) measurements is plotted in Figure 4.6 for the C-doped samples. It should be noted that these measurements were performed on a different growth wafer than that of the Hall results. The residual carrier concentration in the buffer layer is around $5x10^{14}$ cm^{-3}. This value spikes in the stress-relief layer, most likely due to impurities as a result of the sacrificial dielectric layer. A pinch-off voltage of around -4.7 V is also measured.

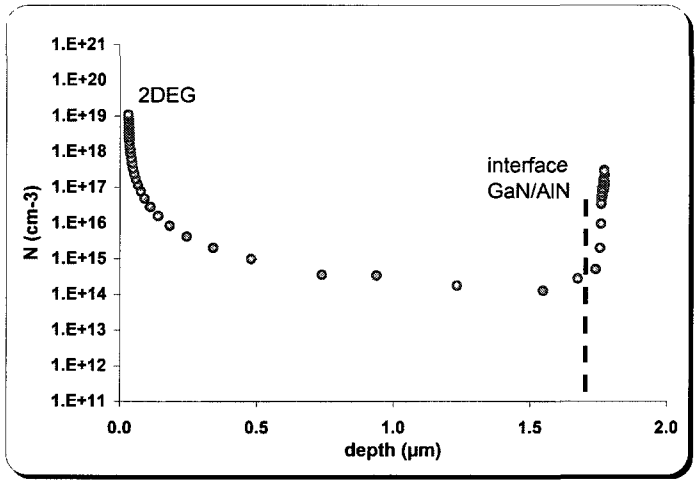


Figure 4.6: CV carrier concentration profile in the 2DEG and GaN buffer

The measurements were performed by CNRS-CHREA in France using a MDC probe station in conjunction with an Agilent 4284 LCR meter. The measurement was performed at a frequency of 10 KHz.

Other Electrical and Physical Properties

The primary electrical properties determined after fabrication of test devices are summarized in Table 4.1. These will be further investigated in Chapter 7.

An important parameter to note for this table is that the non-carbon doped material does have similar leakage current to the C-doped material at a reasonable negative bias of -10 V on the gate. However, as the gate voltage becomes more negative, the leakage current in the C-doped material remains relatively constant, while the non C-doped material becomes more leaky. This result is presented in Section 7.2.

The thermal stability of the material is also of interest. The C-doped material was found to decompose at a temperature of 900°C, whereas the unintentionally-doped growth is stable at this temperature, which will allow for a higher temperature thermal oxide growth. This is essential for making high quality MOS devices based on a thermal oxidation process. It should be noted that C-doping may not be a direct cause of thermal instability, but just a result of the C-doped growth not being optimized in this work.

SIMS Analysis of C-doped samples

Secondary ion mass spectroscopy (SIMS) is used to determine the effects of the exposed oxide on the HEMT stack, as oxygen contamination may be an issue. Outgassing of the oxygen in the SiO_2 sacrificial layer poses a concern during growth. Oxygen impurities are not desired in the GaN buffer layer, as they cause unintentional n-type doping, which reduces the insulating properties of the layer [63–66].

SIMS is used to analyze the oxygen incorporation in the GaN HEMT layers for both a full wafer epitaxial growth and the windowed growth. Figure 4.7 shows the SIMS oxygen and carbon concentration profiles for both the standard and windowed growth samples.

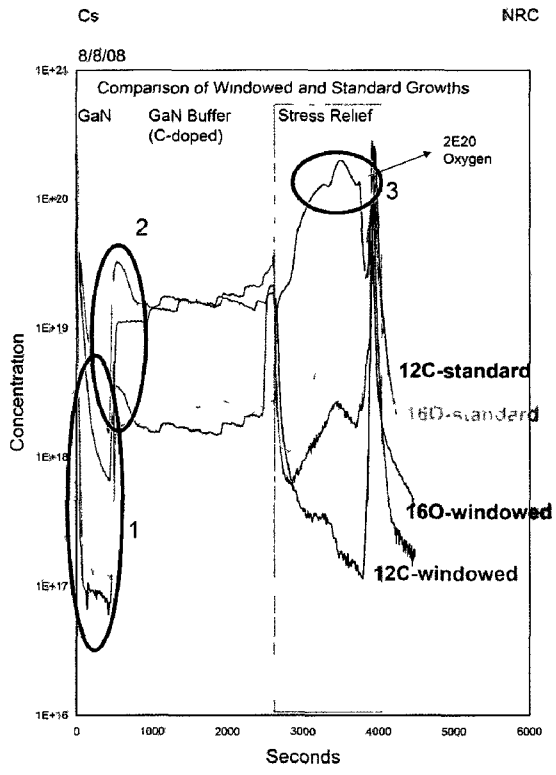


Figure 4.7: SIMS profile comparing oxygen and carbon impurity concentrations for standard and windowed growths

There are three primary areas of interest in this plot. First, it is noted that there is a very high oxygen concentration in the stress-relief layers of the windowed growth wafers, with values exceeding $2x10^{20}$ atm/cm^3, compared to $8x10^{18}$ atm/cm^3 in the standard growth (region 3). During the early stages of growth, the side of the SiO_2 sacrificial layer is exposed, resulting in O contamination. As the growth continues, the stress relief layer eventually covers the sacrificial layer, stopping the exposure of the oxygen to the HEMT layers.

Second, the buffer layer, which is the primary region of interest for oxygen incorporation, has very similar levels of carbon and oxygen compared to the standard growth. Elevated levels of carbon are found in regions 1 and 2, both close to the undoped GaN, as shown in Figure 4.7. These increased levels should not affect the

performance of the devices, as the buffer layer is the region of more critical importance. The primary source of oxygen contamination is thought to be the methane source (99.99% pure) used for carbon doping. This is shown in the SIMS profile as the carbon and oxygen concentrations mirror one another. Other sources of oxygen impurities include residual oxygen from the MBE chamber and the ammonia source.

4.3 Silicon Surface Properties

Auger spectroscopy is used at the silicon surface to verify that the sacrificial layer is fully lifted off, and that the growth process has not left surface contamination. Atomic force microscopy (AFM) results show an RMS roughness of 0.12 nm on a 5x5 μm^2 area of the silicon surface, and 0.17 nm on a 25x25 μm^2 region. This demonstrates the effectiveness of this technique in preserving a smooth silicon surface during the GaN epitaxy, as the roughness stays fairly consistent as the scan area is increased. The surface roughness as quoted by the manufacturer for new wafers is below 1 nm [67]. Etching the GaN layers and then smoothing the silicon surface would not allow for this level of smoothness.

4.4 Silicon <110>

As discussed in Section 2.1.1, <110> oriented substrates are of increasing interest for state-of-the-art CMOS fabrication. Windowed growth on these substrates has also been achieved by making some slight alterations to the growth procedure described in 4.2.1.

The primary difference in growth technique is to initiate the growth of the first AlN buffer layer at a higher temperature (820°C) and at a very low ammonia flow (1 sccm). Once one monolayer is formed, the growth is briefly interrupted and the temperature

Property	479LA	479LB	455LA	455LB	455LC	455LD	455LE
Sheet Resistance [Ω/sq]	538	516	693	556	657	718	1041
Mobility [cm^2/Vs]	812	961	469	693	606	487	396
Sheet Carrier Concentration [cm^{-2}]	$1.30x10^{13}$	$1.27x10^{13}$	$1.93x10^{13}$	$1.62x10^{13}$	$1.57x10^{13}$	$1.78x10^{13}$	$1.51x10^{13}$

Table 4.2: Comparison of the properties of 110 windowed growths. 479L batch grown at NRC, 455L batch grown at CRHEA. Note that due to the windowed growth geometry, numbers are not exact, but can be used to compare between substrates

and ammonia flow are both ramped up to 930°C and 200 sccm respectively. For the case of <111> substrates, the initial temperature is much lower (600°C) and both the flow and temperature are ramped up gradually. This difference in growth is needed, as the lattice mismatch is much larger with silicon <110> substrates, so care must be taken to form a high-quality 2-D AlN monolayer before growth can proceed [68]. Table 4.2 summarizes the properties of the two samples that were grown using this technique. It should be noted that due to the geometry of the windowed growth the values cannot be accurately measured and hence, should only be used as an indication of the quality compared to the other samples.

4.5 Conclusion

A windowed growth technique which exposes a smooth silicon surface after GaN HEMT layer growth has been developed and characterized. A 2-DEG with comparable electrical properties to full-wafer growths has been achieved for both C-doped and non C-doped samples. Auger spectroscopy and atomic force microscopy analysis have shown that the exposed silicon windows are impurity-free and very smooth, which are essential requirements for MOS integration. By contrast, etching of GaN results in defects at the silicon surface. Growth on both <111> and <110> oriented

substrates has been achieved as well. The <110> orientation is of particular interest as it may allow for future state-of-the art MOS devices to be integrated, making this technology more industrially relevant.

Chapter 5

Process Design

This chapter presents the detailed design and fabrication of the monolithic GaN/CMOS chip. The general strategy used to integrate the required process steps has been presented in Chapter 3. The design of the combined process will be discussed, starting with the development of the MOS process and followed by a description of the GaN process. Next, the back-end processing and metallization will be summarized. This Chapter concludes with a discussion of improvements needed for a second iteration of the process design, resulting from the first set of fabricated devices.

The process used to generate the final result shown in Figure 3.3 can be divided into four major steps: silicon surface preparation, MOS processing, GaN processing, and metallization. The silicon surface preparation technique was already presented in Chapter 4. Two different processes were developed for the NMOS devices in this work. Originally, a higher temperature isolated design was used, but due to issues with thermal decomposition of GaN, a more conservative enclosed device geometry without full isolation was used in order to obtain preliminary results. Next, a second iteration of the process was performed in order to achieve proper device isolation without a high thermal budget, as well as mitigate performance issues that were seen in the first successful run. The GaN process design is rather straightforward, as the device characteristics are primarily defined by the growth scheme described in the

previous chapter. The primary alteration to the device formation scheme developed at NRC was the development of a gold-free ohmic metallization, which is presented here.

5.1 NMOS Design

Although it would have been beneficial to have both PMOS and NMOS devices integrated in this chip, using strictly NMOS for this project greatly reduced the complexity, cost, and fabrication time. Altering the process flow to include PMOS devices is fairly straightforward and could be performed in future runs. An NMOS process flow which accommodates the GaN structures needed to be designed. Due to the thermal expansion mismatch between the silicon substrate and the GaN layers, as well as the decomposition of the GaN material at elevated temperatures, an NMOS process which minimizes the thermal budget was desired.

The NMOS process architecture deviates slightly from standard techniques due to the thermal limitations of the GaN material. In order to reduce the stress on the wafers during the process, the high temperature steps were kept to a minimum; this involved using a retrograde p-well, using a thin field oxide to reduce long furnace cycles, and minimizing the rapid thermal anneals by using a joint metallization. A possible local oxidation of silicon (LOCOS) NMOS process was drawn up based on previous work performed in the Carleton Microfabrication facility, as well as Tsuprem4 [69] simulations to design the extra steps needed. Hand calculations to determine the proper threshold and doping levels were performed in the beginning, but quickly became inconsistent with TSuprem4 simulation results. Medici simulations were also performed to determine the transistor characteristics, and subsequently to develop a circuit model. An example Tsuprem4 input file for this process is presented in appendix A.

The outline of the proposed NMOS process flow can be found in Figure 5.1. The MOS processing steps began with a wafer that had the GaN HEMT layers in place, as well as a smooth silicon surface. It should be noted that metallization took place at the end of the process, so the MOS circuitry is formed and then insulated with borophosphosilicate glass (BPSG) before the GaN devices are formed.

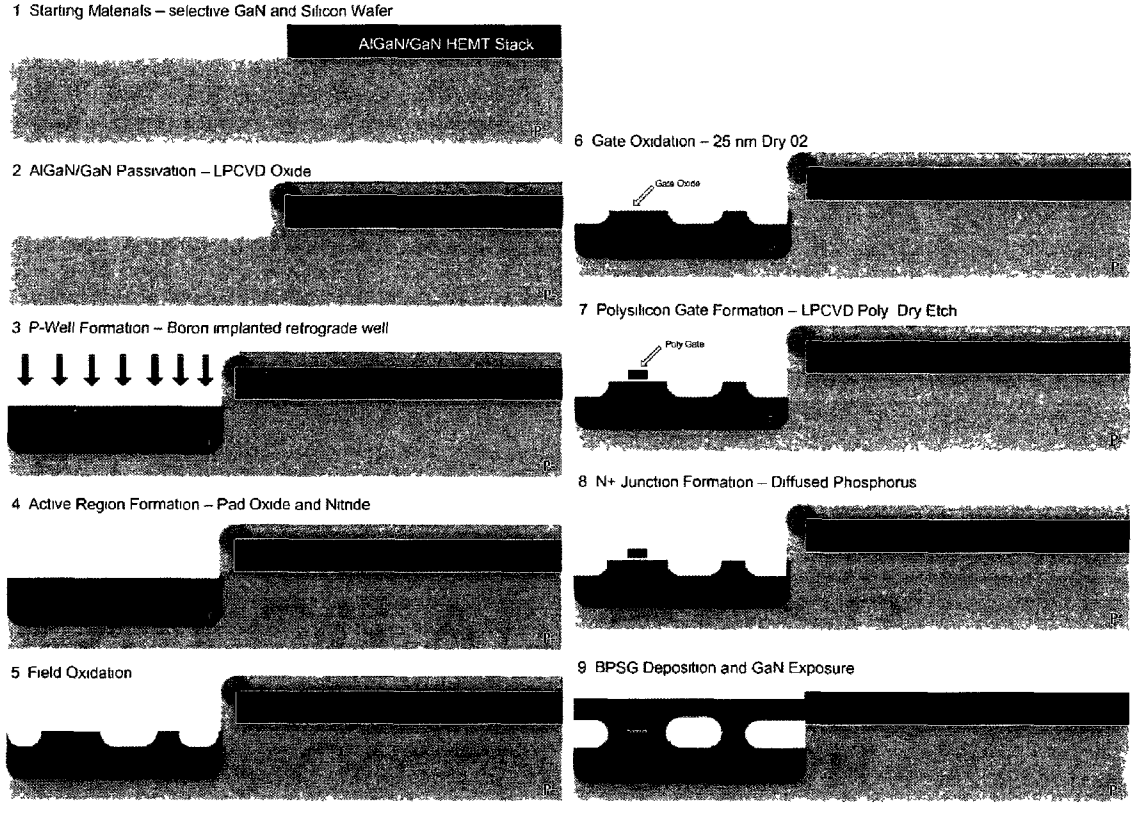
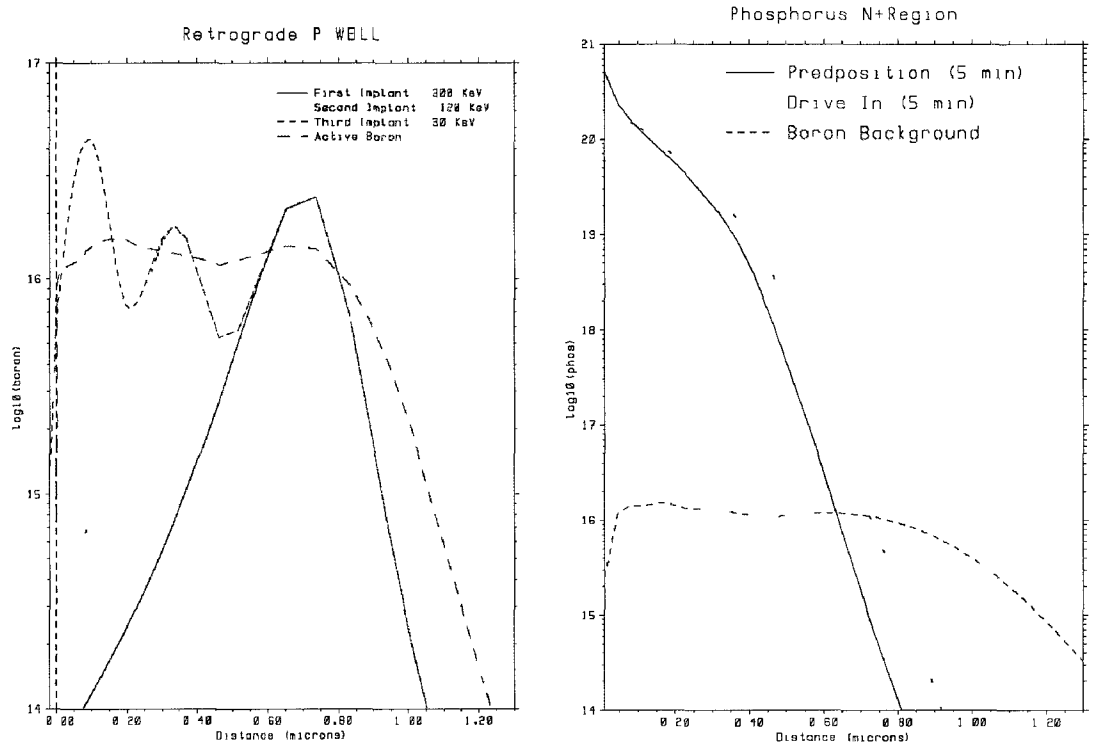


Figure 5.1: MOS process steps

The designed NMOS process began with the formation of p-wells, which were needed due to the high-resistivity substrates. In order to reduce thermal cycles, a 3-implant retrograde well was formed. This allowed for a relatively uniform doping of $1x10^{16}$ cm^{-3} and a depth of 1.3 μm without the use of a drive-in diffusion. The subsequent oxidation steps were used to activate and drive in the dopant such that no

additional thermal steps needed to be used. Figure 5.2a shows the simulated boron concentration profile for this implantation technique.



(a) Retrograde P-well Profile

(b) N+ Junction Profile

Figure 5.2: Doping profiles from Tsuprem4 simulation

The thermal cycles from the field oxidation and gate oxidation were enough to activate the boron, eliminating the need for an implant anneal. A 0.5 μm thick field oxide was chosen in order to keep the thermal budget as low as possible while still providing sufficient device isolation. An optional p-guard implant may be needed to raise the threshold voltage of the parasitic field devices in the NMOS process. A low energy boron implant of $4x10^{13}$ cm^{-2} was demonstrated in simulation to raise the parasitic threshold voltage to approximately 17.5 V to ensure device isolation.

A gate oxide thickness of 25 nm was chosen in order to give good saturation

drain current flow, set an appropriate threshold voltage (V_t), as well as minimize thermal stress by minimizing the growth time. Simulations showed that a 13 minute oxidation using a dry O_2 ambient at 1000°C would accomplish this. However, due to material decomposition, lower temperature oxidations of 950°C and 900°C were used. This will be discussed further in Section 6.3. According to Tsuprem4, the resulting threshold voltage would be 0.375 V, which is appropriate for a supply of 3-5 V. If needed, a threshold adjust implant could be easily implemented in this process as part of the retrograde well formation.

N+ junctions were formed with diffused phosphorus using a $POCl_3$ process that has been developed at Carleton University. The diffusion is typically performed for 30 minutes at a temperature of 950°C . According to simulation, this process results in a junction depth of 0.8 μm and a sheet resistance of 32 Ω/sq. However, since the tube $POCl_3$ concentration cannot be accurately specified, the Tsuprem4 simulation is, as a result, not completely accurate. The manner in which the pre-deposition was simulated was to assume a tube concentration such that the silicon is doped to solid solubility. Sheet resistances have typically been in the 10 Ω/sq range in past runs performed at slightly higher temperatures. The plot in Figure 5.2b shows the 1-D junction profile as predicted by Tsuprem4 simulation.

5.1.1 Enclosed MOS Devices

Because initial trial runs of the LOCOS process caused GaN decomposition, a simpler process was developed to yield NMOS and GaN devices on the same chip without the added thermal budget needed to isolate MOS devices.

MOS devices were fabricated and tested by completely enclosing a drain region with a gate, which is entirely enclosed by a source region. This is shown in cross-section in Figure 5.3 and in plan view in Figure 5.4. Note that the current flow goes from the source to the enclosed drain such that it does not interfere with other

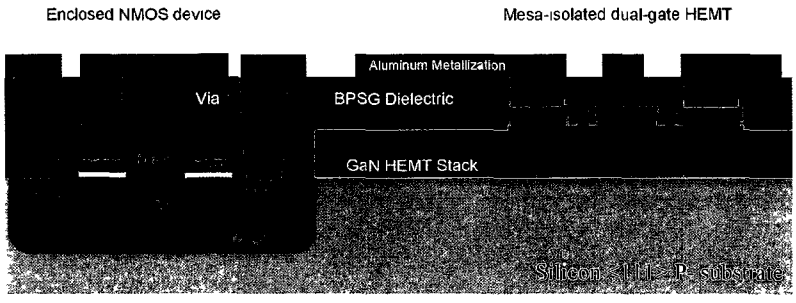


Figure 5.3: Cross-Section of enclosed nMOS device

devices.

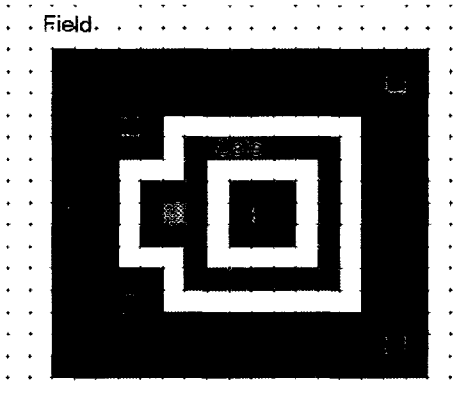


Figure 5.4: Layout of an enclosed NMOS device

Only relatively wide MOSFETs can be fabricated with this approach. This precludes the fabrication of complex circuits, but does suffice to demonstrate the co-integration concept without the added complexity and thermal stress required for the LOCOS process. The process shown in Figure 5.1 was altered such that gate oxidation simply followed the well implant. The pad oxidation, p-guard (if needed), and field oxidation steps were all eliminated. The device results are presented in Section 6.1.

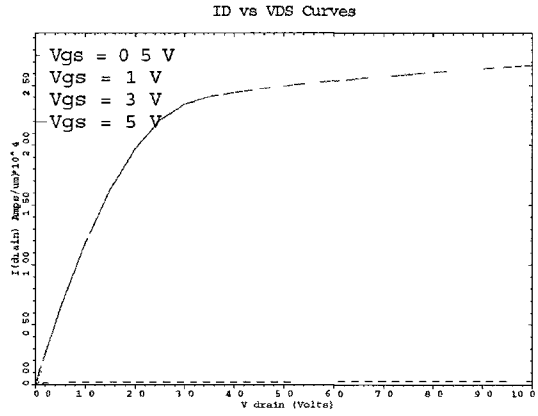
5.1.2 Electrical Characteristics

2-D Medici simulations were used to predict the NMOS characteristics. The input code for the Medici simulations can be found in Appendix B. Profiles for each portion of the device were imported into Medici from Tsuprem4 in order to give an exact representation of the device structure. The IV curves for a 1 μm wide and 2.5 μm long device are shown in Figure 5.5. It should be noted that the 2.5 μm gate length is the lithographic limitation for this process. To scale down the process further, implanted source/drain regions will be needed as short-channel effects caused by the relatively deep diffusions will interfere with device performance. Device dimensions on the order of 1 μm should be achievable with a shallow implanted arsenic junction.

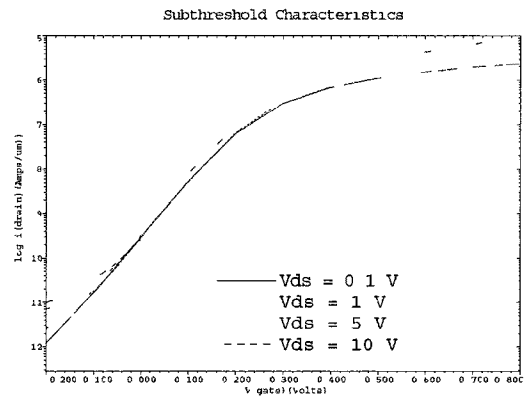
Parameter extraction revealed the device had a 0.375 V threshold voltage and a sub-threshold swing of 79.3 mV/decade. This value of sub-threshold swing is quite reasonable, and suggests that channel leakage at V_G=0 V will not be a problem. Since the sub-threshold curves for different V_{DS} almost super-imposed (Figure 5.5b), it can be concluded that drain-induced barrier lowering is not an issue. The good sub-threshold characteristics can be attributed to the long channel and thin gate oxide.

Punch-through is a short-channel effect which occurs when the gate is unable to shut off the drain current. A criterion for punch-through of 10 nA/μm drain current at V_{GS}=0 was chosen here. A simulation which varies V_{DS} as the gate voltage is kept at zero suggested that the punch-through voltage for this design is in excess of 40 V. Figure 5.5c, which shows a plot of off-state current vs. drain voltage, illustrates this result.

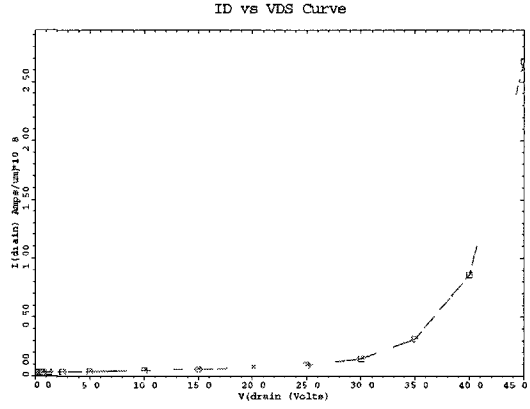
Hot carrier effects were examined by comparing the drain and substrate current, and the maximum drain voltage at the gate voltage which gives the highest avalanche generation. With the drain voltage set, the largest avalanche generation occurs at



(a) Forward Drain Current



(b) Subthreshold Characteristic



(c) Offstate Leakage(V_{GS}=0)

Figure 5.5: Medici simulations of MOS electrical characteristics for a 2.5 μm long device

a gate voltage of approximately 3 V. Simulations show that the substrate current accounts for less than 1% of the drain current, suggesting that hot carrier effects should not have been seen in these devices.

5.2 GaN Devices

The GaN HEMT process used was based on one already developed at NRC. The properties of the device are primarily dictated by the quality of the epitaxial growth

and hence, the primary engineering contribution with respect to the GaN devices was the development of the windowed growth technique presented in Chapter 4. Some alterations to the existing process were required in order to make it compatible with MOS fabrication. The primary change that was made is the metallization scheme. Gold is traditionally used for GaN device fabrication, but it can interfere with MOS circuitry due to the introduction of a mid-level trap, which can cause leaky junctions [70]. An alternative ohmic contact scheme based on aluminum was developed. Figure 5.6 outlines the GaN processing steps.

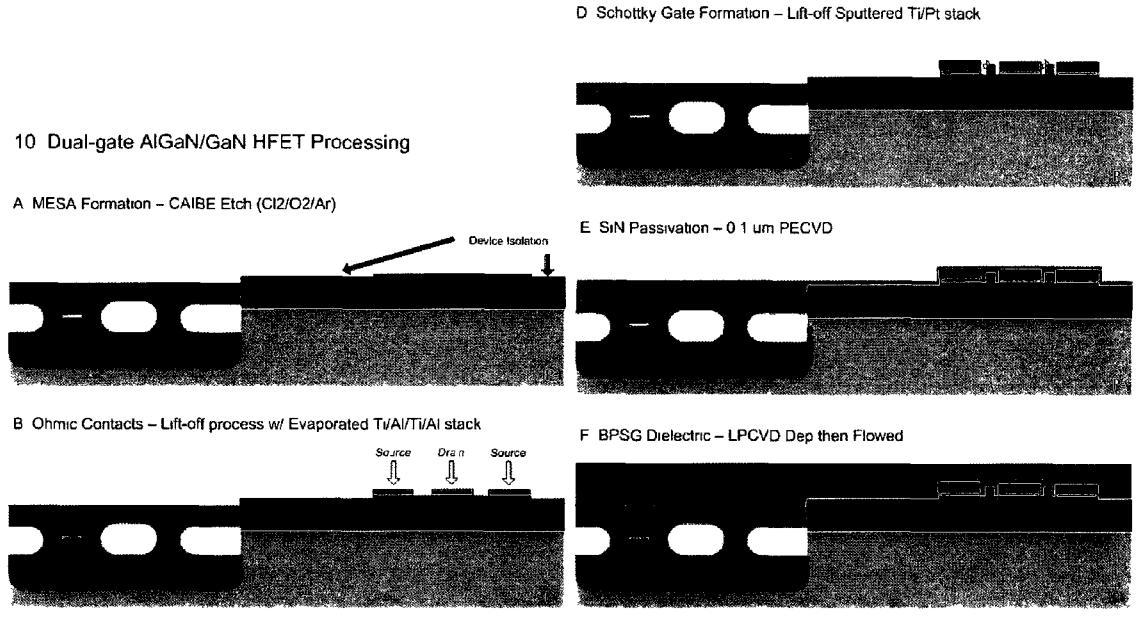


Figure 5.6: GaN processing steps

Starting with the passivated MOS circuitry shown in Figure 5.1, the first step was to etch the mesas for device isolation. A chemically-assisted ion beam etch (CAIBE) with a $Cl_2/O_2/Ar$ chemistry is used to form a slanted MESA edge, and to etch down to below the 2-DEG. Next, ohmic contacts were formed with an evaporated Ti/Al/Ti/Al stack rather than a Ti/Al/Ti/Au stack, which is traditionally used. Following the ohmic metal, a Pt-based gate metallization step takes place. The device was then

passivated with a thin PECVD nitride layer in order to mitigate surface traps which cause current collapse [9]. At this point, the wafer was ready for back-end processing and metallization.

5.3 Metallization and Passives

5.3.1 Metallization

In order to save on steps and mask costs, the metallization for both MOS and GaN devices was done concurrently. A lift-off technique based on the GaN process was used for this step as it provides a superior edge profile and eliminated the need for a metal etch step.

Figure 5.7 shows the metallization strategy used to connect the chip. By using a combined metal for both types of devices, not only is the mask cost lowered, the thermal budget is also reduced by eliminating extra RTA steps.

Again, aluminum was used in place of gold in order to make the process compatible with MOS technology. As long-term operation was not a primary objective at this point, a simple metallization scheme was desired. The metal1 and metal2 layers were simply a thin titanium layer followed by thick aluminum. The role of the titanium layer was to aid adhesion to the silicon.

5.3.2 Passive Components

Although the main goal of this work was to integrate active devices of both types, some passive components were also included for testing as they would be needed for future circuit applications. Integrated polysilicon test resistors were included for simplicity. There is also a possibility to include NiCr resistors as these were used for the GaN process. Spiral inductors were also included and designed using

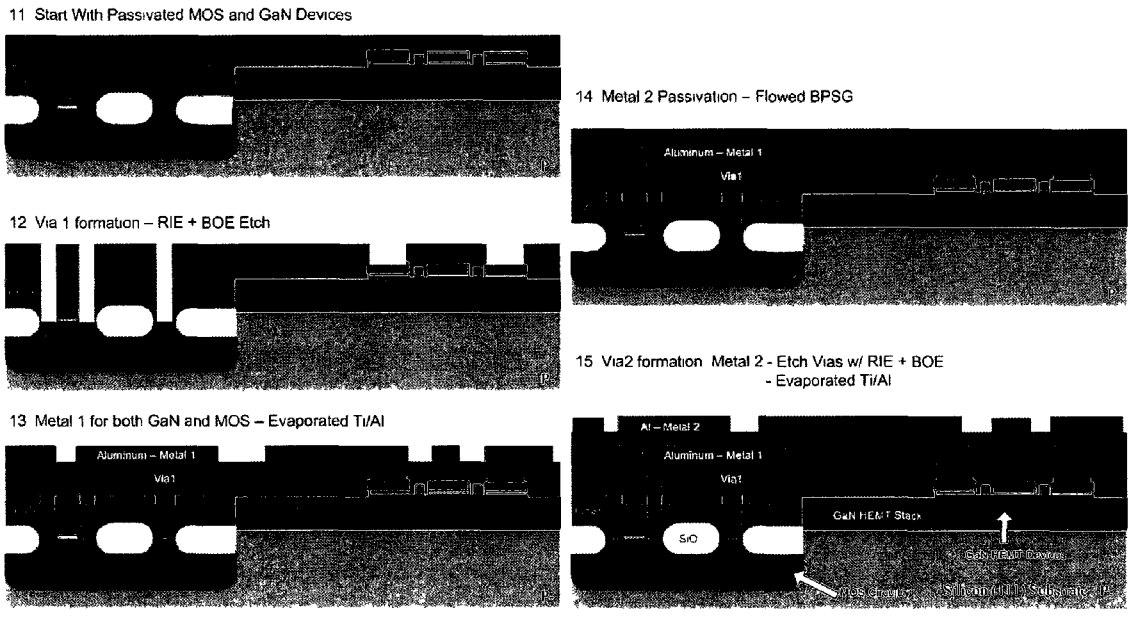


Figure 5.7: Metalization process

Sonnet [71] for operation in the GHz range, but were not tested as the samples never reached this step in the process. These were simply formed using the top metal layer of the process. Test MOScaps were also included.

5.4 Development of a Gold-Free Ohmic Contact

The formation of ohmic contacts to AlGaN/GaN heterostructures has always been a challenge due to the large band-gap of this material system. Traditional strategies to overcome the resulting large Schottky barrier height have been to use multi-layer metal stacks annealed at high temperatures, based on a low work-function metal such as titanium [72]. This is because the inter-metallic alloys formed during high-temperature anneals lower the work function of the metal, and hence reduce the potential barrier. Tunnelling through this lowered potential barrier is the primary mechanism through which current passes through the ohmic contact. It is generally

believed that nitrogen vacancies are created through the interaction of GaN with the contact metal, resulting in n-type doping. This is the physical mechanism by which low resistance ohmic contacts are formed in GaN.

Early work in ohmic contacts revolved around the use of Ti, as it has a low work function. However, the unreliability of Ti or Ti/Al bilayers due to oxidation and the low melting point of Al have necessitated more complicated multilayer metal systems, most commonly Ti/Al/Ti/Au and Ti/Al/Ni/Au [73]. The Au is employed as the top layer metal due to its low electrical resistance, its resistance to electromigration, and to improve the oxidation resistance of the Ti/Al bilayer. The barrier metal (Ti or Ni) was proposed to block diffusion of the Au into the Ti/Al layers, as well as to provide additional Ti for the formation of intermetallics such as Ti_3Al and Al_3Ti [73]. Nevertheless, Auger profiling of alloyed contacts shows that these layers are often not effective as diffusion barriers.

In order to mitigate the effects of Au contamination in MOS devices, an Au-free ohmic contact was developed for this work. Two alternatives to the schemes described above are Ti/Al/Ti/Al and Ti/Al/Ti/Ag. The use of an aluminum top layer posed concerns over oxidation, but was a good short-term solution while more reliable contacts were being developed. Silver is currently of interest for use in ohmic contacts as it has a lower work function than gold, as will silver-based inter-metallic phases, facilitating a low-resistance contact [74]. Additionally, silver has the lowest resistivity of all metals ($1.6\text{x}10^{-8}$ Ω·m vs $2.2\text{x}10^{-8}$ Ω·m for gold), making it a material of interest for improved interconnects and metallization.

Based on the work of Miller *et al.* [74], a Ti/Al/Ti/Ag ohmic contact was attempted on windowed growth material, resulting in comparable characteristics to Ti/Al/Ti/Au contacts and Ti/Al/Ti/Al contacts. These contact schemes were tested on samples of the first windowed growth wafer. Unfortunately, the results in this looked promising, but were limited in quantity due to two primary factors. Firstly,

the amount of material was limited as only one wafer was available for characterization of windowed growth material, as others were left for full processing. Secondly, cracking during the ohmic contact formation resulted in the loss of some samples, most likely due to stress. This is discussed in 5.4.2. Thus, Ti/Al/Ti/Al contacts were used in subsequent runs as not enough material was available to optimize the ohmic contact.

5.4.1 Fabrication and Characterization of Ohmic Contacts

Ohmic metal is formed using e-beam evaporation and a lift-off process developed at NRC. This is followed by a rapid thermal anneal, typically between 700°C and 950°C. These high temperatures are needed to overcome the wide bandgap, and hence large work function of the AlGaN/GaN material. The Ti/Al/Ti/Al ohmic contacts in this work were annealed between 845°C and 875°C.

Characterization of the ohmic contacts was performed using circular Corbino patterns during processing, as well as Transmission Line Method (TLM) patterns, which were measured after the first metallization step. Table 5.1 summarizes the ohmic contact properties for all samples fabricated and tested.

Sample	Contact Resistance	Sheet Resistance
464LA	2.03 Ω-mm	399 Ω/sq
484LC	8.28 Ω-mm	415 Ω/sq
487LA	4.18 Ω-mm	393 Ω/sq
487LB	6.53 Ω-mm	1836 Ω/sq
488LA	3.59 Ω-mm	425 Ω/sq
488LB	5.35 Ω-mm	348 Ω/sq

Table 5.1: Ohmic contact results as measured by TLM patterns following fabrication

It can be seen from this that the first run of the Al-based ohmic in sample 464LA gave the best results. The second iteration of processing devices resulted in inferior contacts, most likely due to three factors: the Al layer was found to be more oxidized (as observed through microscope inspection) in this case compared to the 464L batch; a thin oxide layer was left on the wafers before metal deposition on some samples; and the material quality of some of the later samples was not as good, resulting in a much worse contact as well as sheet resistance. Because of the limited availability of starting material, a full optimization of this ohmic contact scheme could not be performed.

5.4.2 Stress in Ohmic Contacts

The high temperature anneal as well as thick metal stack required to form high quality ohmic contacts to AlGaN/GaN are a major source of stress on the heterostructure during fabrication. Cracking of the GaN layers during this anneal step during ohmic contact formation is quite common, especially in growths on silicon substrates, as overcoming the thermal expansion mismatch remains a challenge. It is difficult to predict whether or not a wafer would crack as it is largely related to the quality of the growth and stress relief layers.

Figure 5.8 shows a crack in the gate periphery of a device due to the stress caused by the ohmic contact anneal.

5.5 Mask Layout

The integration strategy used in this work for topographical layout was to make use of an existing GaN mask set in conjunction with new masks that include MOS circuitry. As the NRC mask set consisted of an array of test structures, it was simple to block out one of every four units and replace it with an area for MOS fabrication.

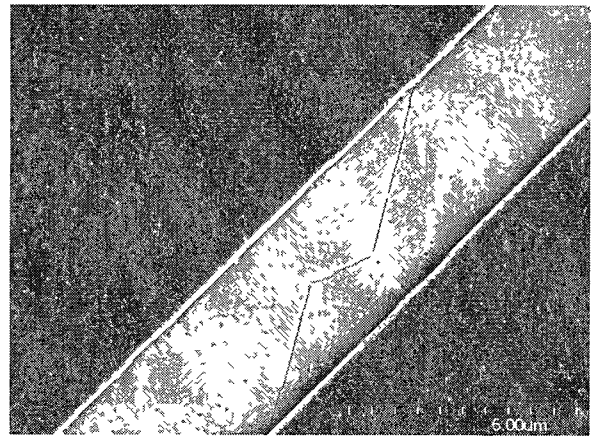


Figure 5.8: SEM micrograph of crack formation in the gate periphery of a device due to ohmic contact anneal (sample 456LB)

Two sets of NMOS masks were used for this work. The first set was based on a more ambitious MOS technology, and included test devices, several different circuits as well as passives such as poly resistors, spiral inductors, and MOScaps. The minimum geometry of the MOS devices in this case was 2.5 μm. When diffuculties were encountered in GaN HEMTs surviving the thermal budget required for full MOS processing, an enclosed MOS mask set was also produced, which only included enclosed MOS transistors and had a minimum geometry of 12.5 μm.

The advanced design had 13 mask levels, which are listed below.

GaN Isolation Covers GaN regions

Silicon Isolation Covers silicon regions

Device Well Device Well for MOS devices

Poly Polysilicon for MOS devices

Mesa (GaN) GaN Mesa

Ohmic (GaN) GaN Ohmics

Gate (GaN) GaN Gates

Contact MOS contacts to poly and device well

Via (GaN) GaN Vias to ohmic and gate metal

Metal 1 (GaN) First metal pattern for GaN

Metal 1 First metal for MOS

Via 2 Via between Metal 1 and Metal 2 for MOS and GaN

Metal 2 (GaN) Second metal for GaN and MOS, used to connect devices together

Note that the Via 1 and Metal 1 layers were all dual dark field exposures, and hence performed in the same lithography step. The Via 2 and Metal 2 masks were made to cover the entire chip and were used to connect MOS and GaN devices for circuits. Because of process issues, the project was never taken to this level. One of the mask blocks showing the MOS area and GaN devices is shown in Figure 5.9.

On the left side, the MOS devices are connected to the GaN devices using Metal 2 to form circuits. The MOS devices, circuits, test structures, and passives are in the bottom left block.

The enclosed process was used to simplify fabrication, focussing only on obtaining working devices of both types on the same chip. The mask number was reduced to 10, as listed below.

GaN Isolation Covers GaN regions

Silicon Isolation Covers Si regions

Poly Polysilicon for MOS devices

Mesa (GaN) GaN Mesa

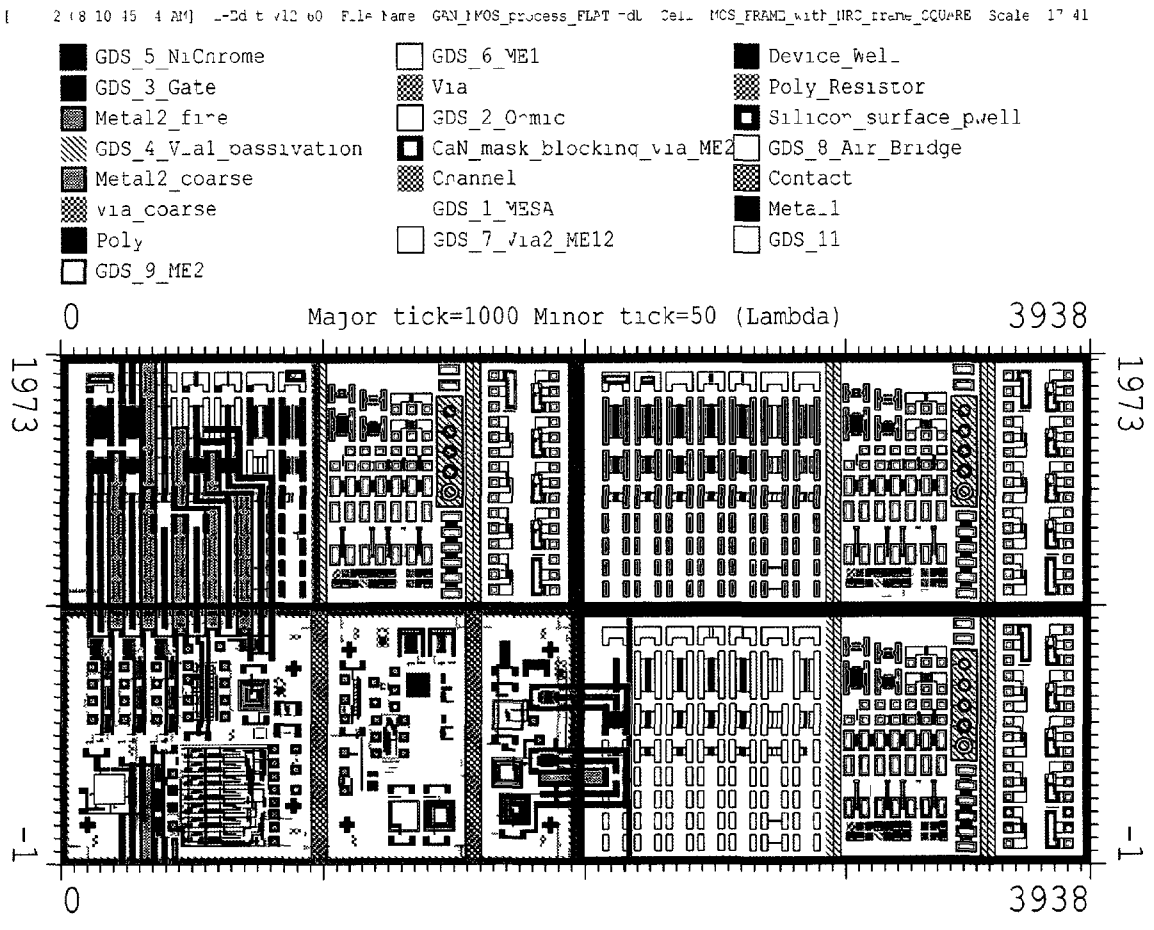


Figure 5.9: First mask layout showing MOS region (bottom left) as well as other GaN patterns

Ohmic (GaN) GaN Ohmics

Gate (GaN) GaN Gates

Contact MOS contacts to poly and device well

Via (GaN) GaN Vias to ohmic and gate metal

Metal 1 (GaN) First metal pattern for GaN

Metal 1 First metal for MOS

The layout of the enclosed MOS device frame is shown in Figure 5.10. In this case, there is no connective metal between the GaN and MOS devices. The larger scale of the devices is also shown here as the masks for the enclosed devices were run directly off of the pattern generator and not stepped down to smaller dimensions in order to reduce complexity.

The GaN mask included arrays of dual-gate test transistors with a fixed gate length of 0.8 μm. These ranged in width from 10 to 320 μm. Additionally, there were Corbino and TLM patterns on the mask for measuring sheet resistance and ohmic contact resistance. The mask also included sets of nichrome resistors, and air-bridged devices. These, however, were not used for this project.

By using a printed mylar transparency sandwiched with the glass mask, in addition to patterned passivating oxide layers, selective areas of the wafers could be processed while other areas were left protected. The BPSG layer deposited after the MOS device well and polysilicon deposition was also used as a passivation layer during MOS fabrication. Conversely, a thick 1 μm PECVD SiO_2 layer is used to cover the GaN regions during MOS fabrication. This layer is removed before GaN fabrication using partial dry etching followed by wet etching to minimize damage to the GaN surface. After MOS and GaN device fabrication, RIE is used to etch through the

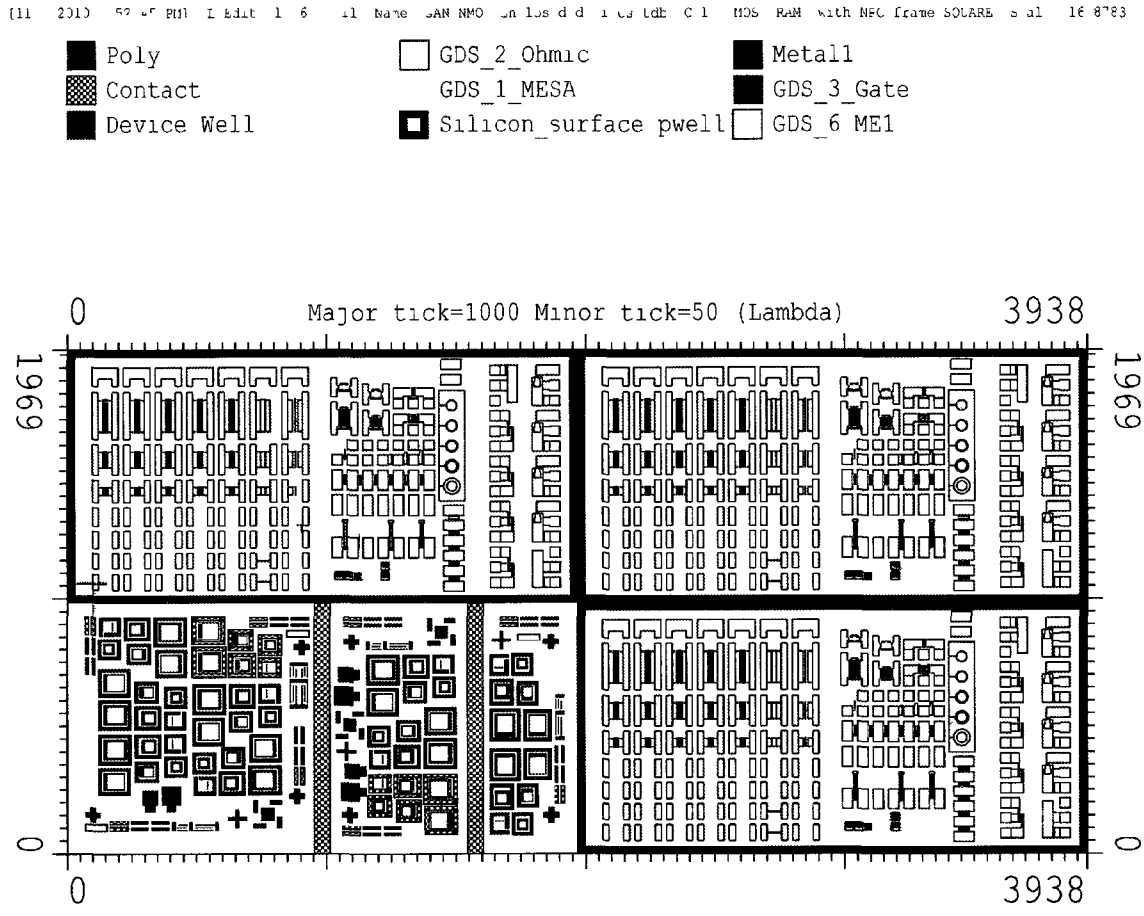


Figure 5.10: Enclosed mask layout showing MOS region (bottom left) as well as other GaN patterns

GaN passivation as well as the BPSG layer to reach either poly, silicon, or GaN metal to make contact to the metal 1 layer.

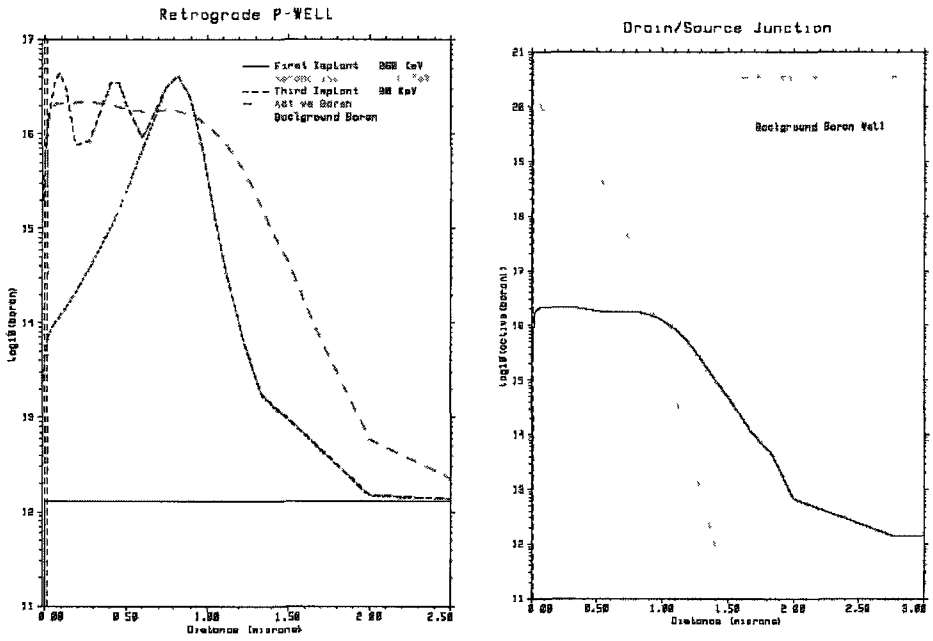
5.6 Second Iteration of MOS Design

A second iteration of the process was designed and implemented in order to mitigate some of the MOS performance issues resulting from the initial run. Although the MOS devices were functional, they had two primary issues that hampered performance: gate leakage and drain leakage. Additionally, the enclosed geometry process did not allow for isolated devices. A new isolation scheme based on a thick deposited oxide layer was proposed to resolve these problems.

Drain leakage was caused by the deeper than expected source and drain junctions punching through the implanted P-well; this is shown in Section 6.1. The source and drain junctions were diffused longer than originally simulated in order to reduce sheet resistance; however, this also resulted in a deeper junction. A TSuprem4 simulation which matches the experimental result of 17.9 Ω/sq is shown in Figure 5.11b. In this case, the depth of the n+ junction is 1.2 μm, which is close to the depth of the P-well (1.3 μm) shown in Section 5.1. The implant dose and energy of the P-well was subsequently increased in order to form a deeper well as shown in Figure 5.11a. The new well should be approximately 2 μm deep.

Table 5.2 summarizes the original and modified P-well implant scheme, which resulted in the same surface concentration as the original scheme in order to maintain the correct threshold voltage.

In order to reduce the thermal budget of the process flow, a new isolation technique based on a thick PECVD oxide was attempted, rather than using LOCOS. This scheme involved depositing a thick oxide layer, which is then subsequently wet etched to form the device well region. This isolation scheme was used in very early CMOS



(a) Deeper Retrograde P-well Profile (b) Deeper N+ Junction Profile

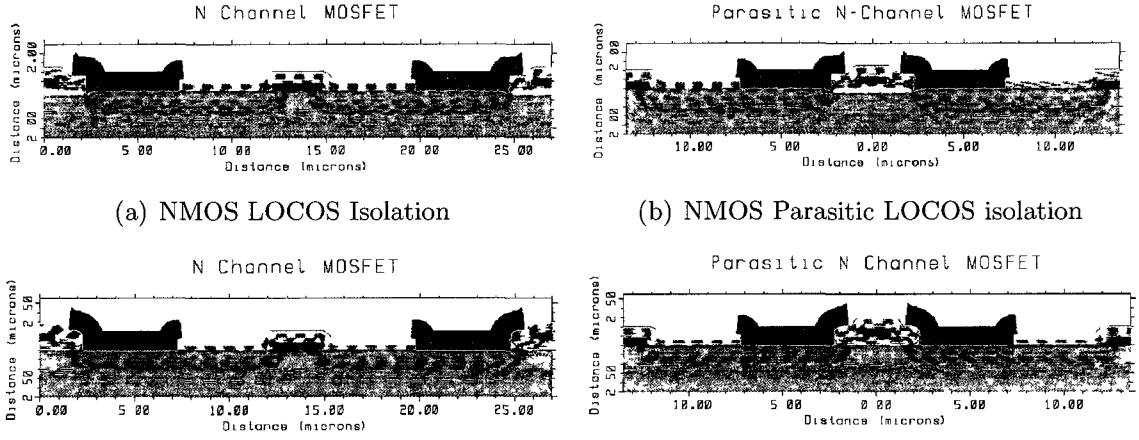
Figure 5.11: Revised doping profiles from Tsuprem4 simulation

technologies. GaN decomposition was not a threat in this case as the PECVD layer was deposited at 500°C. This process alteration allowed the 900°C based process to include isolated devices, and hence circuits, as opposed to the enclosed process. The first iteration of the MOS mask was used in this case. Figure 5.12 shows the cross-sections of both the parasitic and normal MOS devices using both the LOCOS and thick oxide isolation schemes.

Attempts to grow the thermal oxide at 950°C were also made in the new iteration in order to eliminate the gate leakage. The enclosed mask was used in this case to eliminate the thermal budget needed for LOCOS isolation. Eventually, these techniques can be combined in order to fabricate a chip with isolated devices that also have a good quality gate oxide. An in-depth discussion of the oxidations can be found in Section 6.3.

Implant Property	Original Implant	Revised Implant
Implant 1	$6x10^{11}$ $1/cm^2$ 300 kEv	$1x10^{12}$ $1/cm^2$ 360 kEv
Implant 2	$3x10^{11}$ $1/cm^2$ 120 kEv	$7x10^{11}$ $1/cm^2$ 160 kEv
Implant 3	$5x10^{11}$ $1/cm^2$ 30 kEv	$5x10^{11}$ $1/cm^2$ 30 kEv
Surface Concentration	$1x10^{16}$ $1/cm^{-3}$	$1x10^{16}$ $1/cm^{-3}$
Depth	1.3 μm	2 μm

Table 5.2: Summary of P-well retrograde well implant parameters



(a) NMOS LOCOS Isolation

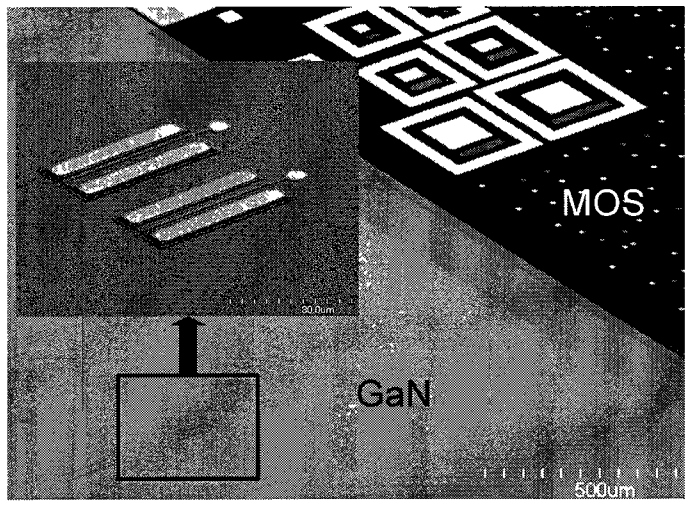
(b) NMOS Parasitic LOCOS isolation

(c) NMOS Oxide isolated

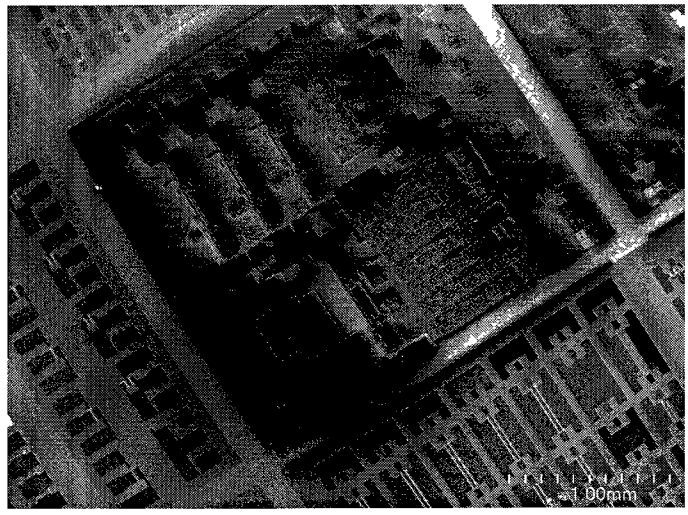
(d) NMOS Parasitic Oxide Isolation

Figure 5.12: MOS cross Sections showing both isolation techniques

Appendix C shows a full process specification for the integration process using the enclosed mask. This includes the minor changes made during the second iteration of processing. Figure 5.13 shows a SEM micrograph of the GaN devices integrated with MOS structures prior to final metallization for the enclosed mask and after completion of device isolation.



(a) Enclosed chip prior to mettalization



(b) Full chip after final fabrication

Figure 5.13: SEM images of integrated GaN HFET and MOS devices

5.7 Summary

The first iteration of a successful process was able to generate good quality GaN transistors in conjunction with enclosed MOS devices. The MOS devices were shown to have gate and drain leakage due to a poor quality oxide and deep diffused junctions. A second fabrication round was conducted, which attempted to solve the gate leakage and drain leakage issues with the MOS process, as well as produce isolated devices. The performance of both the MOS and GaN devices is presented in the following chapters.

Chapter 6

MOS Device Performance

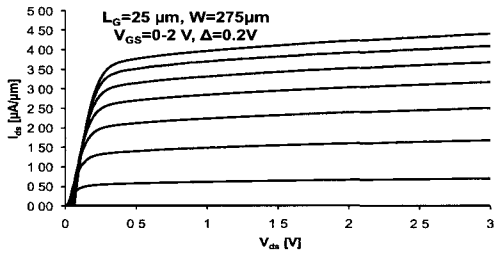
The performance of the MOS devices fabricated in the joint GaN/CMOS process is presented in this chapter. Measurements from the first set of enclosed devices were used to design a second iteration of the process, which was presented in Section 5.6. DC-IV curves as well as CV analysis were used to examine the gate oxide quality of various wafers. The results from the second iteration of the joint run are shown. Possible improvements to the process based on these results are presented in the summary.

6.1 First Run of Enclosed MOS Devices

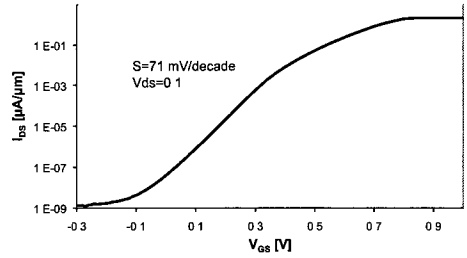
The performance of the first run of enclosed MOS devices (batch 464L) is reported here. These devices were successfully fabricated, but had two performance issues that needed to be resolved. The DC characteristics for an enclosed MOS device are shown in Figure 6.1.

A subthreshold swing of 70.4 mV/decade was measured, demonstrating strong gate control of channel charge. The drain leakage, however, was higher than expected and the gate leakage was very high. The drain leakage can be explained by the shallow P-Well implant and deeper diffused junctions. We suspected the gate leakage to be

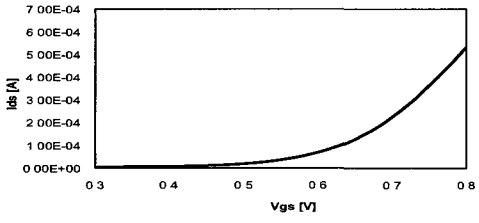
the result of the low temperature of the oxidation in combination with orientation of the silicon. However, breakdown voltage and gate leakage measurements presented in Table 6.3 show that our low temperature oxidation can yield high quality oxides. Additionally, a fabrication error was made during the pre-oxidation clean which resulted in some minor surface etching of the silicon; this could also have been a contributing factor to the high leakage current in the gate oxide.



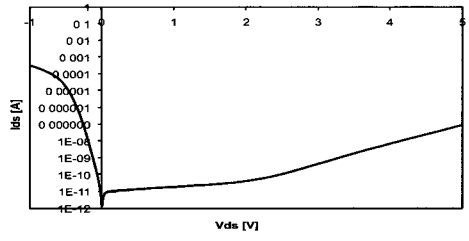
(a) Forward current: I_{DS} vs. V_{DS}



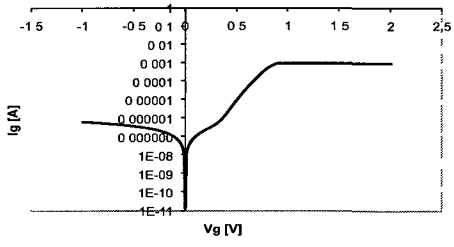
(b) Subthreshold: I_{DS} vs. V_{GS}



(c) Threshold voltage: I_{DS} vs. V_{GS}



(d) Drain leakage: I_{DS} vs. V_{DS}



(e) Gate leakage: I_{GS} vs. V_{GS}

Figure 6.1: DC characteristics of enclosed NMOS device (W=275 μm, L=25 μm) on sample 464LA

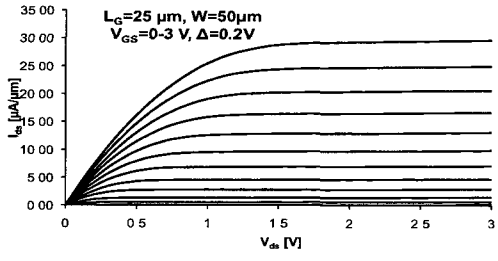
Device	Vt Calculated	Vt TSuprem4	Vt Actual
464LC	0.31	0.35	0.36
464LA	0.45	0.55	0.64

Table 6.1: Threshold voltage comparison for batch 464L

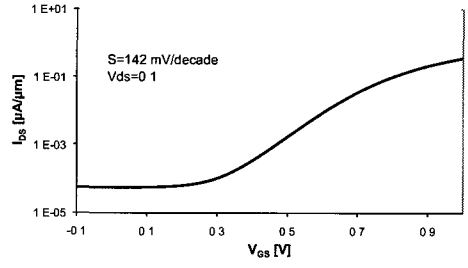
The threshold voltages of the samples probed during the initial run are summarized in Table 6.1. In the case of the 464LC run, the threshold was quite close to that predicted by Tsuprem4 simulations as well as hand calculations using standard formulas for threshold voltage [75]. Sample 464LA however, had a higher threshold voltage than 464LC, which is most likely explained by the surface concentration of the P-Well implant. Additionally, MOS capacitors were measured on test samples produced in earlier runs using CV analysis, as described in Section 6.3. The threshold voltage, which was extracted using the procedure described in Appendix D, was also found to vary from the predicted value. As the thermal budget of the process was altered to reduce the risk of GaN decomposition, the diffusion of the P-Well was also reduced, resulting in a higher concentration at the surface and hence a higher threshold voltage. This also had an impact on the drain leakage as the combination of a deep junction and a shallow P-well can lead to increased leakage. Finally, the background doping of the substrate was changed. Initially, the process was designed for high-resistivity P-type silicon substrates, with a doping of around 10^{13} atm/cm^3. However, the growth wafers were switched to intrinsic silicon after the process was designed. This variation in background doping also had an impact on the drain leakage as the n+ junctions are not guaranteed to be fully surrounded by P-type silicon due to the shallow nature of the well implant.

6.2 Second Process Iteration; Higher Temperature Oxidations, Isolated Devices

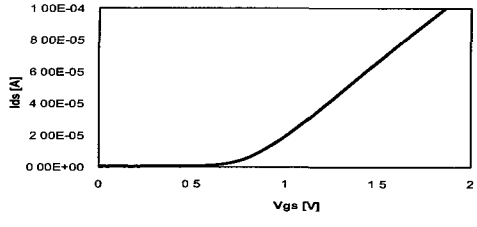
As described in Section 5.6, a second set of devices was fabricated in which higher temperature oxidations were used. Additionally, a new device isolation scheme was attempted. Fully functioning integrated samples were achieved in batches 484L, 487L and 488L. 484L and 487L were enclosed devices, in which the gate oxidation was performed at 900°C and 950°C , respectively. Batch 488L used the full MOS layout using a thick deposited oxide for field isolation. The gate oxidation was performed at 900°C. Figure 6.2 shows the DC characteristics for a 2.5 μm long test device for sample 488LA.



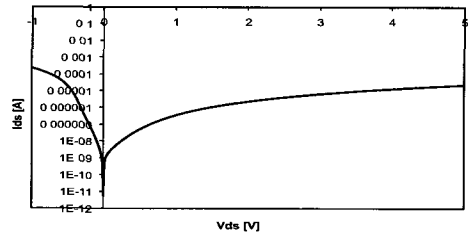
(a) Forward current: I_{DS} vs. V_{DS}



(b) Subthreshold: I_{DS} vs. V_{GS}



(c) Threshold Voltage: I_{DS} vs. V_{GS}



(d) Drain Leakage: I_{DS} vs. V_{DS}

Figure 6.2: DC characteristics of Isolated NMOS device (W=50 μm, L=2.5 μm) for sample 488LA

For sample 488LA, the gate leakage is not shown as it was lower than 0.1 pA for

Sample	Orientation	Isolation	V_T	Gate Leakage	Drain Leakage	Subthreshold Swing
464LCB	111	Enclosed	0.35 V	Yes	Yes	79 mV/dec
464LA	111	Enclosed	0.64 V	Yes	Yes	78 mV/dec
484LC	110	Enclosed	0.29 V	No	No	96 mV/dec
487LA	111	Enclosed	-0.06 V	Yes	Yes	NA
487LB	110	Enclosed	0.39 V	No	No	90 mV/dec
488LA	111	Yes	0.83 V	No	Yes	142 mV/dec
488LD	110	Yes	0.74 V	No	Yes	148 mV/dec

Table 6.2: CMOS device summary. 12.5 μm and 2.5 μm gate length data given

an area of 750 μm^2, which is below the 4155c noise floor. The gate voltage was swept to a bias of 10 V in this case. This suggests that gate leakage had been eliminated for this batch. There was still drain leakage in these devices, as well as a very poor subthreshold swing.

Table 6.2 summarizes the DC characteristics of all the successful integrated GaN/MOS samples. Only the samples with the shortest gate length are reported here. The subthreshold swing of 487LA could not be measured due to high gate leakage currents.

There is a large variation in V_t between batches, which is related to different oxide thicknesses as well as the difference in diffusion of the P-well implant, resulting in higher surface concentrations. The drain leakage issues were still not resolved for the second iteration of samples due to two factors: first, the well implant was performed through a thicker protective oxide than was desired (200 nm rather than 20 nm) and second, the source/drain junction diffusion time was increased to 30 minutes in order to lower the source/drain sheet resistance. Because of this increased time however, the junction depth also increases. A solution to this problem would be to use implanted arsenic junctions, which would result in a much shallower profile. Figure 6.3 shows a TSuprem4 simulation of the P-Well implant with a 200 nm screen oxide used rather

than a 20 nm screen oxide as desired. The lowest energy implant, which sets the threshold voltage is completely absorbed by the screen oxide. This explains the shallower P-well as well as the threshold voltage variability in the samples.

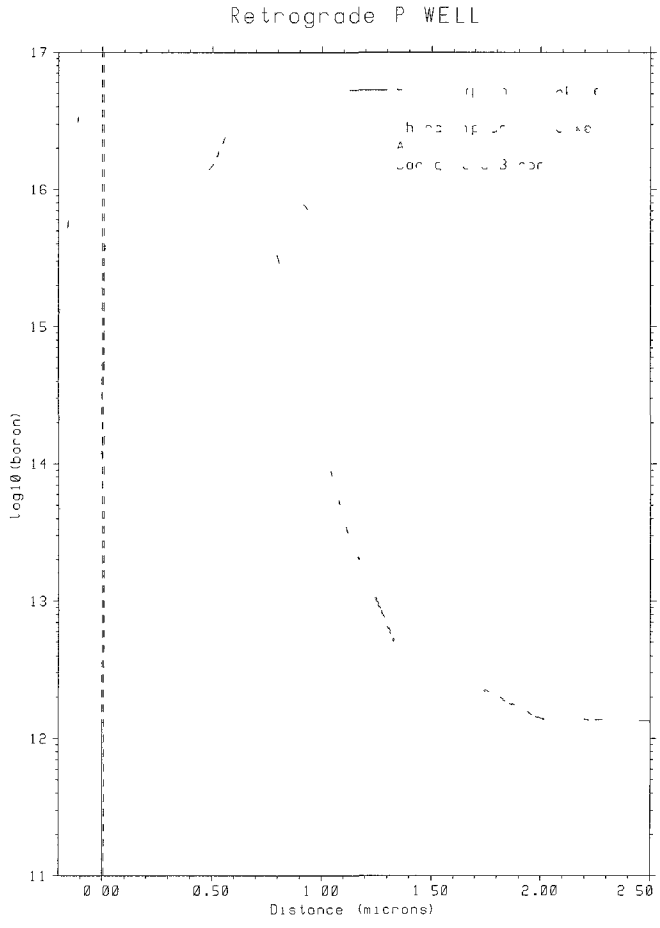


Figure 6.3: TSuprem4 simulation of P-Well implantation with 200 nm thick screen oxide used rather than 20 nm

The primary goal of the MOS process redesign was to address the leakage in the gate oxide and attempt device isolation. The gate leakage was rectified for all batches except for 487LA. The 484L and 488L batches were not expected to have a good quality oxide due to the lower oxidation temperature, however, both of these runs

were successful. Additionally, batch 487, in which the gate oxidation was performed at 950°C, showed excellent oxide properties. The gate oxidation results are summarized in Section 6.3.

6.2.1 Device Isolation in Batch 488L

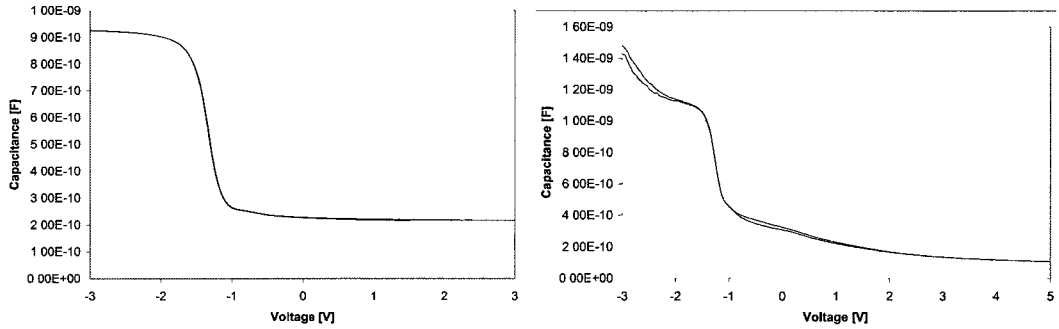
The method of using a thick deposited oxide for field isolation as described in Section 5.6 proved successful. Because test devices used to measure the parasitic field threshold voltage were left off the mask, this value could not be measured. Instead, the isolation between two adjacent wells was recorded. For a 2.5 μm separation and 5 μm separation between wells, the resistance was measured to be 291 $k\Omega$ and 454 $k\Omega$ for biases up to 5 V. This resulted in several μA of current, which must be reduced for circuits to work properly. Once again, this was related to the deep drain and source diffusion, which could be easily rectified using implanted junctions. TSuprem4 simulations predict a parasitic field threshold of 9.4 V

6.3 CV Analysis of MOS Gate Dielectics

Capacitance-Voltage analysis is used to determine the quality of gate oxide growth performed at 900°C and 950°C in a dry O_2 environment. As initial enclosed devices showed higher than average gate leakage, this tool was important to determine the minimum temperature needed for a good quality oxide, while not causing deterioration of the GaN layers via thermal decomposition.

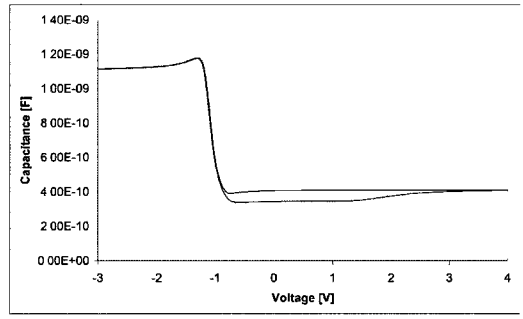
The test setup included an HP4280 C-V meter controlled by HP VEE software through a GPIB interface. A standard probe station was used to contact the devices.

Figure 6.4 shows the CV data for three oxide test wafers. These wafers are patterned with aluminum dots on top and coated with aluminum on the backside for contacts during measurement.



(a) 950°C test (458L)

(b) 900°C test (etched)(464L)



(c) 900°C test (484L)

Figure 6.4: CV curves for gate oxides on test wafers using CV dots

The first devices processed that included a 950°C gate oxidation were unsuccessful due to GaN decomposition at the elevated temperatures needed for the field oxidation. However, the MOS devices displayed zero gate leakage, which is an indication of a good quality oxide layer. The CV curve of the gate oxidation used for these devices is shown in Figure 6.4a. The flat curve in the accumulation region of the plot along with the sharp transition are indicative of a good oxide. The curve also shows no hysteresis, demonstrating a lack of mobile ion charge in the oxide.

Figure 6.4b shows the CV curve for the first working integrated MOS chip. In this case, a 900°C oxidation was used for the enclosed NMOS devices that demonstrated extremely high gate leakage. Unlike Figure 6.4a, this curve shows a sloped characteristic in accumulation, which is indicative of a leakage current in the oxide. During the processing of this sample, the silicon surface was accidentally etched directly prior to

Batch	Orientation	Oxidation Temp	Thickness	Oxidation Time	Leakage	Breakdown
464L	111	900°C	315 Å	33 min	Yes	3.9 MV/cm
484L	111	900°C	177 Å	23 min	Yes	8.4 MV/cm
484L	100	900°C	110 Å	23 min	Yes	9.6 MV/cm
485L	111	950°C	226 Å	14 min	No	9.1 MV/cm
485L	110	950°C	223 Å	14 min	No	12.4 MV/cm
487L	111	950°C	285 Å	19 min	No	7.9 MV/cm
487L	100	950°C	187 Å	19 min	No	8.7 MV/cm
488L	111	900°C	175 Å	25 min	No	12.6 MV/cm
488L	110	900°C	164 Å	25 min	No	10.7 MV/cm

Table 6.3: Oxidation thickness summary using test wafers for each batch.

gate oxidation, which resulted in some surface roughness. This is a possible explanation for the poor oxide quality. Additionally, the lower oxidation temperature and crystal orientation can also be used to explain the low quality film [76] [77].

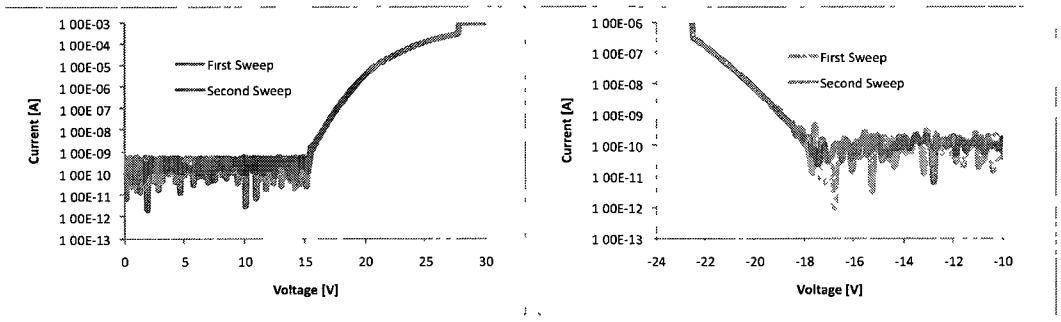
Finally, Figure 6.4c shows the CV curve for a secondary 900°C oxidation test in which the silicon was properly processed prior to oxidation. This curve shows a high quality oxide compared to that of Figure 6.4b, suggesting that the rough silicon surface used for the MOS processing may have been a major cause of the gate leakage.

It should be noted that batch 485L did not yield any successful GaN/MOS integrated devices. However, the oxides, which were grown at 950°C, were still analyzed.

6.4 Oxide Breakdown Measurements

Oxide breakdown was determined by measuring the current through the oxide using two successive voltage sweeps. A good quality oxide will reproduce the same curve as the bias is increased, whereas a poor oxide will show hysteresis. The hysteresis is caused by the presence of defects in the oxide layer that result in charge trapping, which shifts in the gate current voltage characteristic. The second sweep is continued

to a higher voltage until destructive breakdown is reached. The breakdown field is subsequently calculated by dividing this voltage by the oxide thickness. These values are summarized in Table 6.3. The second batch of samples all show excellent oxide quality, with the breakdown field reaching up to 12.6 MV/cm, which is indicative of a good quality oxide. Figure 6.5 shows the oxide test curves for two CV test structures on batches 485L and 488L.



(a) 485L 950°C test oxide (b) 488L 900°C test oxide

Figure 6.5: Oxide breakdown curves for test oxides for batch 485L and 488L (<111> oriented)

The oxides in the first run of samples (batch 464L) broke down at 3.9 MV/cm. This low breakdown was expected, as the quality of the oxide was known to be poor. Additionally, the pad oxide of only 10 nm used for the LOCOS technique employed in batch 485L had a dielectric breakdown of 9.8 MV/cm. This demonstrates that the oxide quality is still very good at lower thicknesses.

6.5 Summary

Two iterations of integrated GaN/MOS samples were successfully completed and devices tested. The first run, which only included enclosed MOS devices, demonstrated good forward current and subthreshold performance, but was plagued with high gate

leakage as well as drain leakage. The second iteration of MOS runs attempted oxidations at slightly higher temperatures, as well as a new isolation scheme based on a thick deposited oxide. An attempt to use LOCOS isolation failed once again due to GaN decomposition. The gate oxide quality of the second run of samples was excellent, even for the oxidations performed at 900°C. This suggests that the gate leakage demonstrated by the first batch of MOS samples was due to process error rather than low oxidation temperature.

The second iteration of devices still showed junction leakage issues, which were caused by a shallow P-well implantation and over-diffusion of the junctions. This can be easily rectified by using implanted junctions for future processes. The isolation scheme using a thick CVD oxide worked successfully, allowing for 2.5 μm gate length devices to be successfully fabricated. Although small leakage current was measured between adjacent wells, this technique showed promise in allowing for circuits to be implemented in the process without compromising the thermal budget.

The MOS device performance did not show variation with the orientation of the substrate. The oxide thickness for both orientations was approximately the same, as was the oxide quality. Ideally, the <110> orientation is preferred due to the increased hole mobility and relevance to state-of-the-art technology.

Three improvements to the existing process must be made. Firstly, the junction depth must be reduced in order to mitigate short-channel effects and junction leakage. Secondly, the source of the threshold voltage variation must be determined and rectified. This is most likely caused by the diffusion of the P-well being different for each run as the thermal budget is different. Finally, the device isolation scheme must be improved to eliminate all leakage currents. This is related to the deep junctions and variation in substrate doping, both factors that can be adjusted.

Chapter 7

GaN Device Performance

The performance of the GaN HEMT devices is reported in this chapter. Both field-plated and non-field-plated dual-gate HEMTs were fabricated, with gate widths ranging from 10 μm to 320 μm and a fixed gate length of 0.8 μm. A summary of the DC characteristics from all wafers that successfully completed fabrication is presented in this chapter. The breakdown voltage of the devices, gate leakage, and current collapse are also investigated. Suggestions for improvement are given in the summary.

7.1 Measurement Summary

Seven samples in total from quarters of two-inch wafers on which GaN was grown were successfully fabricated with both MOS and GaN devices; two samples (464L batch) were part of the first batch of experiments, while the remaining five were fabricated in the second iteration of the design as described in Chapter 5. The performance of HEMTs from all the successful wafers is summarized in Table 7.1.

All DC measurements were made using a standard low-frequency probe station setup that included four micro-manipulators with tungsten probes connected to an Agilent 5155c semiconductor parameter analyzer. TLM structures were used to measure sheet resistance and the specific contact resistances of the Ti/Al/Ti/Al ohmic

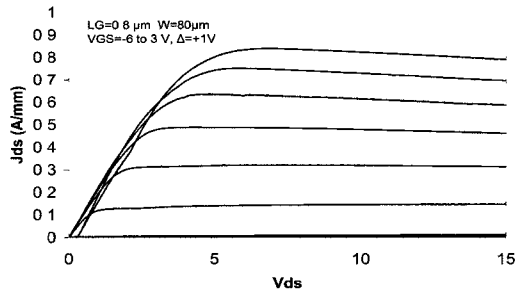
Wafer	Si Type	C-doped	Max I_{DS}	$V_{Pinchoff}$	Gate Leakage	Peak g_m	R_c
464LCB	111	Yes	0.45 A/mm	-4.7 V	$1.2\text{x}10^{-2}$ A/mm	x	x
464LA	111	No	0.81 A/mm	-3.3 V	$7.2\text{x}10^{-3}$ A/mm	181 mS/mm	$1.03\text{x}10^{-4}$ Ωcm^2
484LC	110	No	0.82 A/mm	-3.4 V	$4.4\text{x}10^{-3}$ A/mm	191 mS/mm	$1.65\text{x}10^{-3}$ Ωcm^2
484LA	111	No	0.63 A/mm	-2.3 V	$3.2\text{x}10^{-2}$ A/mm	146 mS/mm	$4.45\text{x}10^{-4}$ Ωcm^2
487LB	110	No	0.31 A/mm	-3.6 V	$3.2\text{x}10^{-2}$ A/mm	47 mS/mm	$2.32\text{x}10^{-4}$ Ωcm^2
488LA	111	No	0.72 A/mm	-2.7 V	$8.7\text{x}10^{-3}$ A/mm	165 mS/mm	$3.03\text{x}10^{-4}$ Ωcm^2
488LD	110	No	0.67 A/mm	-3.6 V	$1.58\text{x}10^{-2}$ A/mm	126 mS/mm	$8.22\text{x}10^{-3}$ Ωcm^2

Table 7.1: Summary of GaN device performance for successful runs. X denotes a value that could not be measured.

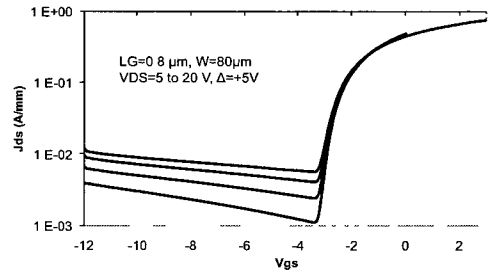
contacts. Figure 7.1 summarizes the DC performance of a typical dual-gate GaN HEMT device with a gate length of 0.8 μm and total width of 80 μm.

The device performance varied from sample to sample, with the best samples conducting over 0.8 A/mm of forward current for maximum usable gate bias of 3 V. This compares quite well to state-of-the-art devices on silicon substrates which report 1.04 A/mm forward current for 0.7 μm long devices [7], and 0.6 μm long devices on silicon-carbide that report 1.2 A/mm [21]. The currents also scaled well with device width. Figure 7.2 shows the forward current vs. device width for sample 488LD. A constant current of 0.7 A/mm is maintained. The field-plated had the same DC characteristics as the non field-plated devices.

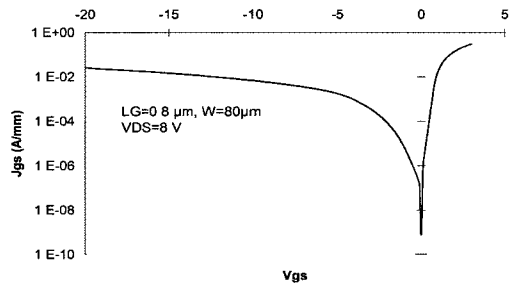
Wafers that did not have as much forward current typically had worse underlying electrical properties, such as sheet resistance and mobility. It was disappointing, however, that the ohmic contact scheme, which worked well on sample 464LA, did not work as well for the next set of samples, limiting the forward current. This is especially the case for sample 484LC, which still had the best forward current even though it was plagued with high contact resistance. A performance difference between the devices fabricated on <111> oriented and <110> oriented substrates



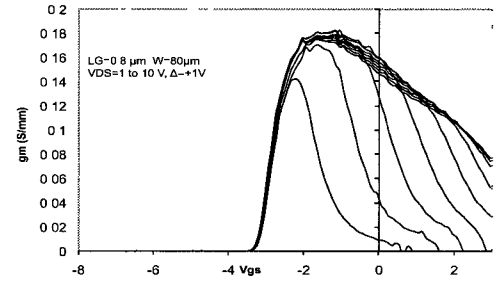
(a) Forward current: I_{DS} vs. V_{DS}



(b) Pinch Off: J_{GS} vs V_{GS}



(c) Gate Leakage: J_{GS} vs V_{GS}



(d) Transconductance: g_m vs V_{GS}

Figure 7.1: DC measurements for dual-gate AlGaN/GaN HEMT on sample 464LA

was not observed.

7.2 Gate Leakage

The amount of gate leakage in all devices fabricated is summarized in Table 7.1. The values ranged from 4.4x10^{-3} A/mm for the best wafer to 3.2x10^{-2} A/mm. These values were taken at a bias of -8 V on the gate and -10 V on the drain. It should be noted that the pinchoff and gate leakage characteristics are similar for all samples except for the C-doped wafer, 464LC. All non C-doped samples showed the same trend in gate leakage: a rising leakage current as the gate becomes highly reverse biased. However, the C-doped sample had a flat leakage curve as shown by the dashed line in Figure 7.3, which compares the gate leakage for a C-doped (464LC) vs. non C-doped (464LA) sample. This can be explained by the fact that the contribution of

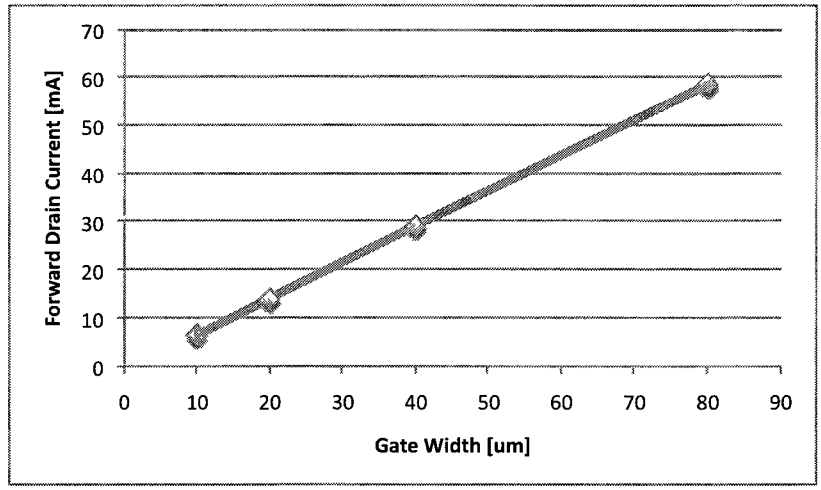
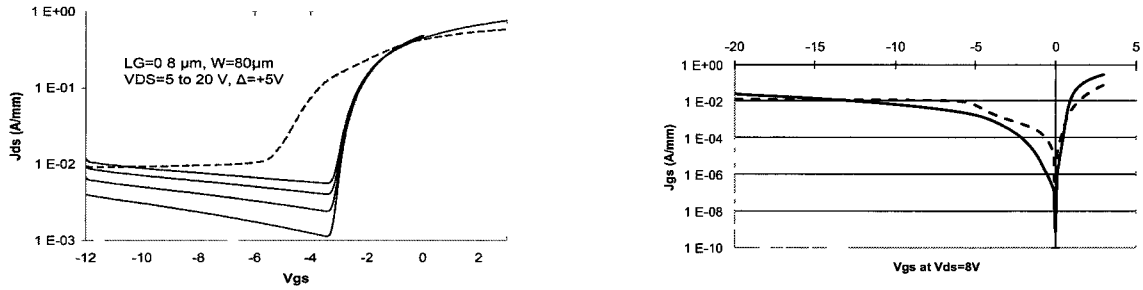


Figure 7.2: Maximum forward current vs. device width for sample 488LA

leakage current through the buffer layer is eliminated only in the case of the C-doped sample. In non C-doped samples substrate leakage increases as the gate-drain voltage is increased.



(a) Forward current: I_{DS} vs. V_{DS}

(b) Pinch-off: J_{GS} vs V_{GS}

Figure 7.3: Gate leakage comparison for C-doped 464LC sample (dashed) vs non C-doped 464LA sample

The magnitude of gate leakage for all the devices remained high. This was primarily due to the fact that the passivation layer, which was needed to eliminate current collapse, had not been optimized to mitigate gate leakage nor for growth on silicon substrates. Increasing gate leakage after passivation is a common issue for all GaN

HEMT structures, irrespective of substrate. Techniques such as aluminum oxide passivations and nitrogen plasma treatments have been used to reduce the effects of gate leakage [78].

7.3 Current Collapse

Pulsed measurements have shown that the nitride passivation layer had mitigated current collapse for all wafers. Figure 7.4 shows both the swept and pulsed DC drain characteristics. The pulsed characteristic was obtained by maintaining the gate terminal at a baseline voltage of -8V to fill surface traps. The gate was then pulsed with a 0.5 ms pulse with a period of 10 ms to the desired bias point for the measurement. The current drive remained the same for both conditions, showing that current collapse was not an issue for this device. This was the case for all the successfully fabricated wafers.

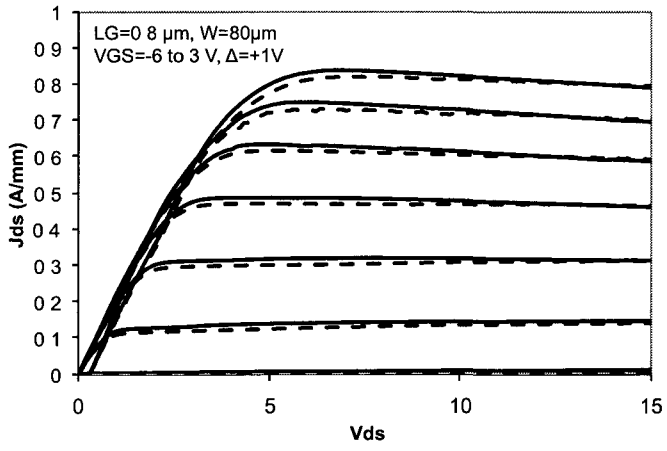


Figure 7.4: Pulsed (dashed) and non-pulsed (solid) J_{DS} vs V_{DS} curves for wafer 464LA

Table 7.2: Breakdown Voltage vs Gate-Drain Spacing

Gate-Drain Spacing	Breakdown Voltage
2.2 μm	54 V
3.2 μm	93 V
4.2 μm	140 V
5.2 μm	>200 V

7.4 Breakdown Characteristics

Breakdown measurements were performed on the best sample, 464LA. The breakdown voltage of the devices ranged from 53 V for a 2.2 μm gate-drain spacing to greater than 200 V for a 5.2 μm gate-drain spacing. It should be noted that 200 V was the measurement limit of the equipment in this case. To make this measurement, devices were pinched off with a gate voltage of -8 V while the drain voltage was increased. Breakdown was observed by monitoring the gate current, as this increased sharply at the onset of breakdown. Table 7.2 demonstrates this trend correlating the gate-drain spacing to the breakdown voltage as shown in [79]. These high breakdown voltages on non-optimized devices demonstrate the potential of HEMT integration to greatly increase the voltage-handling capability of MOS.

7.5 Summary

GaN HEMT devices ranging from 2 x 5 μm to 2 x 160 μm wide with a gate length of 0.8 μm were successfully fabricated and tested on <111> and <110> oriented silicon substrates. The GaN devices fabricated in this work showed comparable performance to state-of-the-art technology in terms of forward current, and show no signs of current collapse. However, gate leakage and a non-reproducible ohmic contact scheme are two issues that must be addressed. The breakdown characteristic also looks promising for

high-power and/or high-voltage applications. There were no major differences in the performance between the two types of substrate used.

Future work to improve the performance of the GaN devices should include field plates, as these have become standard practice to improve the breakdown characteristic and hence, allow operation at higher voltage and power levels. Additionally, the ohmic contact scheme must be revisited. Although the Ti/Al/Ti/Al scheme did provide some promising results, it was shown to be less reproducible and is not comparable performance-wise to gold-based ohmic schemes that are currently in use. Experiments should be performed to determine whether gold in the ohmic contact scheme can be kept isolated from the MOS devices. Additionally, further investigation into silver and vanadium-based contacts could be beneficial. Finally, the gate leakage of these devices must be reduced. Optimized field plates can both increase breakdown voltage and reduce gate leakage.

Chapter 8

Conclusions and Future Work

The first monolithic integration of silicon MOSFETs and GaN HEMT devices has been presented in this work. A co-integration technique that minimizes thermal budget in order to prevent GaN decomposition has been developed. This is based on a novel windowed epitaxy technique that was presented in Chapter 4, that allows for high-quality GaN layers to be grown on both <111> and <110> oriented silicon while preserving an atomically smooth silicon surface for MOS fabrication. The process flows presented in Chapter 5 yielded isolated MOS devices with good quality gate oxides alongside GaN HEMTs which show high breakdown characteristics, comparable forward current to state-of-the-art devices and no current collapse. The MOSFET and GaN HEMT device performance was summarized in Chapters 6 and 7.

8.1 Future Directions

The primary focus for the continuation of the work is to bring the performance of the MOS and GaN devices up to state-of-the art levels. For the MOS devices, the process needs to be optimized to eliminate all short-channel effects and drain leakage issues, which were mostly related to the depth of the source/drain diffusions, but not limited to these factors. The isolation scheme based on a thick deposited oxide shows promise

to be sufficient for 2.5 μm long devices, but not for current sub-micron sized technology. Good quality oxides were grown at both 900°C and 950°C which is not only important to reduce GaN decomposition, but also to minimize unwanted diffusion of source/drain junctions as the technology is scaled. Demonstrating PMOS devices on <110> oriented substrates is also a must for future research, as the increased hole mobility is the primary reason for pursuing this orientation.

The GaN devices in this work exceeded forward currents of 0.8 A/mm, which is comparable to current technology. The next steps to take in the GaN process development would be to reduce the gate leakage, which limits their application as power devices. The gate leakage can be reduced by optimizing the dielectric layer currently used to mitigate the effects of current collapse. Additionally, field plates, which have become widely used, need to be implemented and optimized to raise the breakdown voltage as well as reduce gate leakage current. Finally, the gold-free ohmic contact scheme developed for this work, which initially showed promising results, proved not to be reproducible, and hence, must be redeveloped.

With these process improvements the technology will be ready for circuit applications. Promising areas include power amplifier circuits with adaptive MOS-based circuitry, as well as GaN-based sensors that use MOSFETs for processing and readout [80]. GaN power-switching devices are also of great interest for routing and automotive applications. Having MOS readout and control circuitry alongside high-breakdown voltage GaN switches may be beneficial in this field.

8.2 Summary of Contributions

The first demonstration of the monolithic integration of silicon MOSFETs with GaN HEMT devices has been presented in this work. A new windowed-epitaxy technique was developed allowing for the growth of GaN HEMT layers alongside regions of

atomically smooth silicon. A low thermal budget and gold-free fabrication process that forms isolated MOS devices ready to be used in circuit applications alongside high performing GaN HEMTs has been developed. This was accomplished on both <111> and <110> oriented silicon substrates.

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Appendix A

Tsuprem Input File for Original nMOS Design

```
$ Simulations for NMOS/GaN integration project
$ April, 2009
$ Peter Chyurlia 100281015
$ 2D NMOS Model
$ This simulation is the ACTUAL FLOW USED AFTER FIRST ITERATION OF
FABRICATION!!
$       --> main edits are oxidation temps and times as well as diffusion
temp adn time!



$ Full non-equilibrium point defect model
$(includes transient enhanced diffusion)
method     pd.full

$ Graphics written as postscript file
option     device="c/postscript" plot.out="2D_NMOS ps"

$-------------------------------------------------------------------------
-----
$ MESH DEFINITION

$only specify half of the design and then reflect in the Y-axis
$Specify the Mesh
MESH    GRID.FAC=1.5
MESH    DY.SURF=0.002 LY.SURF=0 02  LY.ACTIV = 2.0


$-------------------------------------------------------------------------
-----
$INITIALIZE WAFER
$ Set the well background doping
$ This is the doping of the p-type wafer
$ <111> added to say that we are using 111 type silicon
$ width now changed to 13.5 since we need contacts 5 um from gate and 5 um
wide contacts

initialize Boron=1.3E12 <111> WIDTH=13.5 DX=0.05

$ Plot initial Mesh
SELECT  TITLE="NMOS MESH"
PLOT.2D SCALE GRID  Y.MAX=3 C.GRID=2


$-------------------------------------------------------------------------
```

```
--------
$WELL IMPLANT
$need a cap oxide for implant 200 Angstroms

Deposit    oxide thick=0.02

$ implant Boron to form the well
$ goal is 1e16 surface conc.
$ use singly/doubly ionized boron and a high energy such that we don't need
an anneal
$ go back to tr.boron pearson model, the chboron is giving weird behaviour
$ Can't, CHBORON is only one that goes past 100 keV, use it for this only
$ can't used triply ionized, BUT, 300 is still ok for doubly ionized!

implant    boron dose= 6E11 energy=300 tilt=7 rotation=30 impl.tab=chboron


$ Plot the as-implanted boron distribution
select     z=log10(boron) TITLE="Retrograde P-WELL"
plot.1d    top=17 bottom=14 right=1.3 color=2 line.typ=1  X.VALUE=10


$second implant for retrograde well
$ Still using chboron due to high energy implant
$ this can be singly ionized since we can go up to 180 keV

implant    boron dose=3E11 energy=120 tilt=7 rotation=30 impl.tab=chboron

$ plot the second implant
select     z=log10(boron)
plot 1d    ^ax ^cl color=3 line.typ=2 X.VALUE=10

$third implant for retrograde well
implant    boron dose=5E11 energy=30 tilt=7 rotation=30 impl.tab=tr.boron

$ Plot the as-implanted boron distribution for retrograde well
select     z=log10(boron)
plot.1d    ^ax ^cl color=4 line.typ=3 X.VALUE=10

etch oxide
$-------------------------------------------------------------------------
-------------

$ P-Gaurd PE    - this gives Vth of about 19 V, without it we get 4.9 V,
which is ok
```

```
$ DEPOSIT       PHOTORESIST THICK=1
$ ETCH PHOTORESIST LEFT P1.X=2.25

$ Field theshold adjust implant - BLOCKED BY RESIST - without P-gaurd,
VT=4.9 V
$ implant boron dose=4E13 energy=40 tilt=7 rotation=30 impl.tab=tr.boron

ETCH PHOTORESIST ALL

$-------------------------------------------------------------------------
--------------
$Field oxidation
$pad oxide
deposit oxide thick=0.02
$deposit pad nitride
deposit nitride thick=0.008

$etch nitride in outer edge to form FOX
etch Nitride  LEFT P1.X=2.25

$Field oxidation - results in 0.5 um thick field oxide
$ done at 950 actually, for a long time to give around 0.5 microns
$ performed for 1 hour and 53 minutes --> GaN exploded here
DIFFUSION  TEMP=950  TIME=113  WETO2

$ REMOVE PAD NITRIDE
ETCH NITRIDE ALL

$-------------------------------------------------------------------------
-----------------
$ Finish Plotting P-Well Concentrations
$ Check that all the boron is electrically active
select     z=log10(active(boron))
plot.1d    ^ax ^cl color=6 line.typ=5 X.VALUE=10

$Add a legend to the plot
LABEL     CM X=11  Y=23         COLOR=2 LABEL="First Implant - 300 KeV"
Line.typ=1 LEFT
LABEL     CM X=11  Y=22.5       COLOR=3 LABEL="Second Implant - 120 KeV"
Line.typ=2 LEFT
LABEL     CM X=11  Y=22         COLOR=4 LABEL="Third Implant - 30 KeV"
Line.typ=3 LEFT
LABEL     CM X=11  Y=21.5       COLOR=6 LABEL="Active Boron" Line.typ=5
LEFT

$-------------------------------------------------------------------------
```

```
--------------
$ Print junction depth information
select      z=doping
print.1d    layers

$etch away the screen oxide 200 A
etch oxide thick=0.03

$-------------------------------------------------------------------------
--------------
$GATE FORMATION

$gate oxidation
$ done at 950, not 1000, we got 311 A, not 250 so see what we get here
DIFFUSION  TEMP=950  TIME=24  DRYO2
$oxide anneal (10 mins only)
Diffusion TEMP=950 Time =10

$deposit Poly
DEPOSIT POLYSILICON THICKNESS=0.4 DIVISIONS=4

$Poly and oxide etch between 0.5 and 12.25 microns
$ this way, reflecting left will give a parasitic transistor and reflecting
right will
$ give the actual device
$ETCH POLY LEFT P1.X=12.25

ETCH POLY START X=0.75 Y=-2
ETCH CONTINUE X=0.75 Y=2
ETCH CONTINUE X=12.25 Y=2
ETCh DONE     X=12.25 Y=-2


$etch away oxide in S/D windows
ETCH OXIDE TRAP thick=0.03

$-------------------------------------------------------------------------
---------------
$source and drain formation

$phosphorus diffusion
$ done at 900 for 20 min --> got 18 ohms/sq in test wafer
$  I.CONC=1e21 is only giving 45 ohm/sq, try upping this
$  I.CONC = 1e22 is giving 33 ohm/sq try upping again
diffusion   time=20 temp=900 Impurity=Phosphorus I.CONC=1e23
$ Drive-in
```

```
diffusion     temp=900 time=5

$-------------------------------------------------------------------------
-----------------
$Back END
$BPSG deposition - very thick for this process
DEPOSIT OXIDE THICK=0.6
$Thermal steps associated with BPSG
DIFFUSION time=20 temp=900
$Long Time hydrogen annealing step - not done
$DIFFUSION time=240 temp=450
$-------------------------------------------------------------------------
-----------------
$GaN Processing Steps at this point

$Ohmic metal Anneal --> leave out, does nothing
$Diffusion temp=750 time=0.5

$-------------------------------------------------------------------------
-----------------

$open up windows for fill
ETCH OXIDE  START X=2.25 Y=-2
ETCH CONTINUE X=2.25 Y=2
ETCH CONTINUE X=7.25 Y=2
ETCh DONE       X=7.25 Y=-2

$Metallization
Deposit Aluminum THICK=1 SPACES=3
DEPOSIT PHOTORESIST THICK=1
ETCH PHOTORESIST RIGHT P1.X=7.5
ETCH PHOTORESIST LEFT P1.X=1.5
ETCH ALUMINUM TRAP ANGLE=85 THICK=1.5
ETCH PHOTORESIST ALL


$-------------------------------------------------------------------------
------------------
$REFLECT FILE
SAVEFILE OUT.FILE=NMOS_HALF.STRUCT
STRUCTURE REFLECT RIGHT
SAVEFILE OUT.FILE=2D_NMOS.MEDICI MEDICI

$-------------------------------------------------------------------------
-----------------
$Plot structure
```

```
SELECT TITLE="N-Channel MOSFET"
PLOT.2D         SCALE Y.MAX=2.5
COLOR   SILICON COLOR=5
COLOR   OXIDE   COLOR=7
COLOR   POLY    COLOR=2
COLOR   ALUMI   COLOR=1

SELECT Z=log10(BORON)
FOREACH VAL (14 to 21 step 1)
CONTOUR VALUE=VAL LINE=5 COLOR=2
END

SELECT Z=LOG10(PHOSPHORUS)
FOREACH VAL (16 to 21 step 1)
CONTOUR VALUE=VAL LINE=4 COLOR=3
END


$-------------------------------------------------------------------------
-----------
$Find Vt

$output threshold voltage
$WF is work function in ev 4.35 corresponds to doping > 1E20
ELECTRIC X=13.5 THRESHOLD NMOS V="0 2 .05" GATE.WF=4.35 GATE.ELE
$plots sheet conductance vs voltage
PLOT.1D ELECTRIC



$-------------------------------------------------------------------------
----------
$Plot Sheet resistance

electric x=10 resistan


$-------------------------------------------------------------------------
------------
$ Find parasitic Vt by reflecting other way

 LOADFILE IN.FILE=NMOS_HALF.STRUCT
 STRUCTURE REFLECT LEFT


$Plot structure
```

```
SELECT TITLE="Parasitic N-Channel MOSFET"
PLOT.2D         SCALE Y.MAX=2.5
COLOR   SILICON COLOR=5
COLOR   OXIDE   COLOR=7
COLOR   POLY    COLOR=2
COLOR   ALUMI   COLOR=1

SELECT Z=log10(BORON)
FOREACH VAL (14 to 21 step 1)
CONTOUR VALUE=VAL LINE=5 COLOR=2
END

SELECT Z=LOG10(PHOSPHORUS)
FOREACH VAL (16 to 21 step 1)
CONTOUR VALUE=VAL LINE=4 COLOR=3
END

$Etch OXIDE thick=1.1
$Find Parasitic Vt

$output threshold voltage

$output threshold voltage
$WF is work function in ev 4.35 corresponds to doping > 1E20
ELECTRIC X=0.01 THRESHOLD NMOS V="0 30 .2" GATE.WF=4.35 GATE.ELE
$plots sheet conductance vs voltage
PLOT.1D ELECTRIC
```

Appendix B

Medici Input file used to calculate MOS device properties

Files in following order:

Setup file

Subthreshold Simulation

Threshold Voltage Determination

Saturation Curves

Punchthrough

Hot Carrier effects

```
comm Peter Chyurlia 100281015 January 11, 2006
comm Setup file for medici simulations in 2D

title NMOS design

comm    Loads up my 2d TSUPREM model, including profiles
comm    xmin and xmax used to eliminate side poly
mesh    TSUPREM4 in.file=2D_NMOS.MEDICI POLY.ELEC y.max=3 ELEC.BOT x.min=2
x.max=25


comm RENAME elctrodes (Aluminum is converted to an electrode when loaded
into medici)

RENAME ELECTR OLDNAME=1 NEWNAME=source
RENAME ELECTR OLDNAME=2 NEWNAME=drain
comm ELEC.BOT renames the bottom to an electrode called substrate!
RENAME ELECTR OLDNAME=Substrate NEWNAME=sub

contact number=gate n.poly WORKFUNC=4.35


plot.2d grid boundary fill scale

comm regrid on doping, ignore region 1
comm use quad-tree mesh now


regrid QT.REGRI doping ignore=(1) log ratio=2 smooth=1

plot.2d grid boundary fill scale

contact name=gate n.poly

models conmob fldmob srfmob2

symb carriers=0
method iccg damped
solve

comment regrid on potential twice

regrid QT.REGRI potent ignore=(1) ratio=0.2 max=1 smooth=1

plot.2d grid boundary fill scale
```

```
regrid QT.REGRI potent ignore=(1) ratio=0.1 max=1 smooth=1
out.file=nmos_mesh

plot.2d  grid boundary fill scale

comm 2D concentration

plot.2d boundary fill scale
contour doping LOG MIN=-20 MAX=-14 DEL=0.5 COLOR=2 LINE=2
contour doping LOG MIN=16  MAX=21  DEL=0.5 COLOR=1 LINE=2

comm Plot1D concentration -- at y=0 it should be just under 10E15

plot.1d DOPING Y.Start=-0.0253 Y.END=0.2 X.start=5 X.end=5 POINTS Y.LOG
+       color=2
comm +  device="c/postscript" plot.out=grid.ps

comment solve for zero bias and save
symb carriers=0
solve out.file=nmos_solution
```

```
comm Peter Chyurlia 281015
comm Subtrheshold Characteristics

title Subthreshold Characteristics

comm read in the mesh
mesh in.file=nmos_mesh

comm read in the zero-bias solution
load in.file=nmos_solution

models conmob prpmob

contact name=gate n.poly WORKFUNC=4.35
symb newton carriers=2 ELECTRON
method stack=10 ICCG
comm solve for different values of VDS
LOG OUT.FILE=1.ivl
solve V(gate)=0 V(source)=0.0 V(drain)=0.1 V(sub)=0.0
+ elec=gate vstep=0.025 nstep=32
comm + elec=gate vstep=0.1 nstep=8

comm getthe mostfet parameters, which will give us the subthreshold slope

EXTRACT MOS.PARA



comm repeat this three times

mesh in.file=nmos_mesh
load in.file=nmos_solution
contact name=gate n.poly WORKFUNC=4.35
symb newton carriers=2 ELECTRON
method stack=10
LOG OUT.FILE=2.ivl
solve V(gate)=0 V(source)=0.0 V(drain)=1 V(sub)=0.0
+ elec=gate vstep=0.025 nstep=32

comm getthe mostfet parameters, which will give us the subthreshold slope

EXTRACT MOS.PARA



mesh in.file=nmos_mesh
```

```
load in.file=nmos_solution
contact name=gate n.poly WORKFUNC=4.35
symb newton carriers=2 ELECTRON
method stack=10
LOG OUT.FILE=3.ivl
solve V(gate)=0 V(source)=0.0 V(drain)=5 V(sub)=0.0
+ elec=gate vstep=0.025 nstep=32

comm getthe mostfet parameters, which will give us the subthreshold slope

EXTRACT MOS.PARA



mesh in.file=nmos_mesh
load in.file=nmos_solution
contact name=gate n.poly WORKFUNC=4.35
symb newton carriers=2 ELECTRON
method stack=10
LOG OUT.FILE=4.ivl
solve V(gate)=0 V(source)=0.0 V(drain)=10 V(sub)=0.0
+ elec=gate vstep=0.025 nstep=32

comm getthe mostfet parameters, which will give us the subthreshold slope

EXTRACT MOS.PARA


comm Plot everything

plot.1d  x.ax=V(gate) y.ax=i(drain) y.log Line.typ=1 in.file=1.ivl
+       title="Subthreshold Characteristics"
+       device="cl/postscript" plot.out=subthreshold_curves.ps
plot.1d UNCHANGE x.ax=V(gate) y.ax=i(drain) y.log Line.typ=2 in.file=2.ivl
plot.1d UNCHANGE x.ax=V(gate) y.ax=i(drain) y.log Line.typ=3 in.file=3.ivl
plot.1d UNCHANGE x.ax=V(gate) y.ax=i(drain) y.log Line.typ=4 in.file=4.ivl



comm Label all the plots
LABEL     LABEL="Vds = 0.1 V" Line.typ=1 C.Size=0.5 Start.LE LX.FINIS=10 CM
+       X=13 Y=6
LABEL     LABEL="Vds = 1 V" Line.typ=2 C.Size=0.5 START.LE LX.FINIS=10 CM
LABEL     LABEL="Vds = 5 V" Line.typ=3 C.Size=0.5 START.LE LX.FINIS=10 CM
LABEL     LABEL="Vds = 10 V" Line.typ=4 C.Size=0.5 START.LE LX.FINIS=10 CM
```

```
comm Peter Chyurlia 281015
comm Determines value of VT

title Threshold Voltage

comm read in the mesh
mesh in.file=nmos_mesh

comm read in the zero-bias solution
load in.file=nmos_solution

models conmob prpmob

contact name=gate n.poly WORKFUNC=4.35

comm solve using gummel method, default for medici
symb gummel carriers=2

LOG out.file=VT_sub0.ivl
solve V(gate)=0 V(source)=0.0 V(drain)=0.1 V(sub)=0.0
+ elec=gate vstep= 0.1 nstep=30

comm getthe mostfet parameters

EXTRACT MOS.PARA
EXTRACT RESISTAN X.POINT=5



mesh in.file=nmos_mesh
load in.file=nmos_solution
models conmob prpmob
symb gummel carriers=2
contact name=gate n.poly WORKFUNC=4.35
LOG out.file=VT_sub-1.ivl
solve V(gate)=0 V(source)=0.0 V(drain)=0.1 V(sub)=-1
+ elec=gate vstep= 0 1 nstep=30
EXTRACT MOS.PARA

mesh in.file=nmos_mesh
load in.file=nmos_solution
models conmob prpmob
symb gummel carriers=2
contact name=gate n.poly WORKFUNC=4.35
models conmob prpmob
LOG out.file=VT_sub-2.ivl
```

```
solve V(gate)=0 V(source)=0.0 V(drain)=0.1 V(sub)=-2
+ elec=gate vstep= 0.1 nstep=30
EXTRACT MOS.PARA

comm plot the output
Plot.1D         Y.AXIS=I(drain) X.Axis=V(gate) POINTS Color=2
IN.FILE=VT_sub0.ivl
+       TITLE="ID vs VGS Curve" device="c/postscript"
plot.out=IDvVG_threshold.ps
Plot.1D         Y.AXIS=I(drain) X.Axis=V(gate) POINTS Color=2
IN.FILE=VT_sub-1.ivl UNCHANGE
Plot.1D         Y.AXIS=I(drain) X.Axis=V(gate) POINTS Color=2
IN.FILE=VT_sub-2.ivl UNCHANGE



comm ------------------------------------------------------------
comm put plot into IC-CAP format

LOG ICCAP IN.FILE=VT_sub0.ivl OUT.FILE=vt_curve_VD01_VB0.set
+ DRAIN=drain GATE=Gate SOURCE=source SUBSTRAT=sub
+ OUT1=I(drain) INP1=V(gate) INP2=V(drain)
+ INP3=V(sub) INP4=V(source)

LOG ICCAP IN.FILE=VT_sub-1.ivl OUT.FILE=vt_curve_VD01_VB-1.set
+ DRAIN=drain GATE=Gate SOURCE=source SUBSTRAT=sub
+ OUT1=I(drain) INP1=V(gate) INP2=V(drain)
+ INP3=V(sub) INP4=V(source)

LOG ICCAP IN.FILE=VT_sub-2.ivl OUT.FILE=vt_curve_VD01_VB-2.set
+ DRAIN=drain GATE=Gate SOURCE=source SUBSTRAT=sub
+ OUT1=I(drain) INP1=V(gate) INP2=V(drain)
+ INP3=V(sub) INP4=V(source)
end
```

```
comm Peter Chyurlia 281015
comm Saturation IV curve Characteristics

title saturation

comm read in the mesh
mesh in.file=nmos_mesh

comm read in the zero-bias solution
load in.file=nmos_solution

models conmob prpmob

contact name=gate n.poly WORKFUNC=4.35

comm Gummels doesn't converge, so use newton's method

symb newton carriers=1 ELECTRON
method stack=10

LOG out.file=1.ivl
solve V(gate)=5 V(source)=0.0 V(drain)=0 V(sub)=0.0
 + elec=drain vstep= 0.5 nstep=20

mesh in.file=nmos_mesh
load in.file=nmos_solution
contact name=gate n.poly WORKFUNC=4.35
symb newton carriers=1 ELECTRON
method stack=10
LOG out.file=2.ivl
solve V(gate)=3 V(source)=0.0 V(drain)=0 V(sub)=0 0
 + elec=drain vstep= 0.5 nstep=20

mesh in.file=nmos_mesh
load in.file=nmos_solution
contact name=gate n.poly WORKFUNC=4.35
symb newton carriers=1 ELECTRON
method stack=10
LOG out.file=3.ivl
solve V(gate)=1 V(source)=0.0 V(drain)=0 V(sub)=0.0
+ elec=drain vstep= 0.5 nstep=20


mesh in.file=nmos_mesh
load in.file=nmos_solution
contact name=gate n.poly WORKFUNC=4.35
```

```
symb newton carriers=1 ELECTRON
method stack=10
LOG out.file=4.ivl
solve V(gate)=0.5 V(source)=0.0 V(drain)=0 V(sub)=0.0
+ elec=drain vstep= 0.5 nstep=20



comm plot everything from file

Plot.1D         Y.AXIS=I(drain) X.Axis=V(drain) Line.typ=1 UNCHANGE
IN.FILE=1.ivl
 +      TITLE="ID vs VDS Curves"
 +      device="cl/postscript" plot.out=saturation_curves.ps
Plot.1D         Y.AXIS=I(drain) X.Axis=V(drain) Line.typ=2 UNCHANGE
IN.FILE=2.ivl
Plot.1D         Y.AXIS=I(drain) X.Axis=V(drain) Line.typ=3 UNCHANGE
IN.FILE=3.ivl
Plot.1D         Y.AXIS=I(drain) X.Axis=V(drain) Line.typ=4 UNCHANGE
IN.FILE=4.ivl


comm legend

comm Label all the plots
LABEL     LABEL="Vgs = 0.5 V" Line.typ=4 C.Size=0.5 Start.LE LX.FINIS=1 CM
comm med+       X=13 Y=6
LABEL     LABEL="Vgs = 1 V" Line.typ=3 C.Size=0.5 START.LE LX.FINIS=1 CM
LABEL     LABEL="Vgs = 3 V" Line.typ=2 C.Size=0.5 START.LE LX.FINIS=1 CM
LABEL     LABEL="Vgs = 5 V" Line.typ=1 C.Size=0.5 START.LE LX.FINIS=1 CM

comm getthe mostfet parameters

EXTRACT MOS.PARA


comm
-------------------------------------------------------------------------
comm Export the ivl data into IC-CAP format for use with ADS and BSIM3
model generation

LOG ICCAP IN.FILE=1.ivl OUT.FILE=sat_curve_VG5.set
+ DRAIN=drain GATE=Gate SOURCE=source SUBSTRAT=sub
+ OUT1=I(drain) INP1=V(drain) INP2=V(Gate)
+ INP3=V(sub) INP4=V(source)
LOG ICCAP IN.FILE=2.ivl OUT.FILE=sat_curve_VG3.set
```

```
comm Peter Chyurlia 281015
comm Punthrough Simulation

title Punch-through Simulation

comm read in the mesh
mesh in.file=nmos_mesh

comm read in the zero-bias solution
load in.file=nmos_solution

models conmob prpmob

contact name=gate n.poly WORKFUNC=4.35

comm solve using newton's method
symb newton carriers=1
method stack=10

comm    no gate or source voltage, adjust VDS
comm    want less than 10 nA/um
solve V(gate)=0 V(source)=0.0 V(drain)=59 V(sub)=0.0
+ elec=drain vstep=1 nstep=10

comm getthe mostfet parameters

EXTRACT MOS.PARA

comm plot the output

Plot.1D         Y.AXIS=I(drain) X.Axis=V(drain) POINTS Color=2
+       TITLE="ID vs VDS Curve" X.MIN=60
+       device="cl/postscript" plot.out=punchthrough.ps

plot.2d boundary fill scale REGION JUNCTION title="Potential Contours,
vg=0, vd=66"

contour potential

plot.2d boundary fill scale REGION JUNCTION title="Electron concentration,
vg=0, vd=66"

contour electron logarith min.valu=15 max.valu=20 del.valu=1
```

```
end
```

```
comm Peter Chyurlia 281015
comm Hot Carrier simulation

title Hot Carrier Simulation

comm read in the mesh
mesh in.file=nmos_mesh

comm read in the zero-bias solution
load in.file=nmos_solution

contact name=gate n.poly WORKFUNC=4.35

comm peform a zero-carrier solution to bias the drain

symb carr=0
method DVLIMI=1 ICCG

comm solve for drain VDS=5
solve V(drain)=5 LOCAL

comm try to regrid to increase convergence stuff
comm regrid QT.REGRI potent ignore=(1) ratio=0.05 max=0.5 smooth=1
comm doesn't work!

comm solve using newton's method
comm symb newton carriers=1 ELECTRON
comm    newton didn't converge, gummel does
symb gummel carriers=1 ELECTRON


comm stack method increases probability of convergence, max is 20
method stack=20


comm    find point at which bulk current is maximum for a drain voltage of
5 V
comm    include the gate.cur statement to include hot carrier effects
comm    include IMPACT.I for impact Ionization method
solve   V(gate)=0 Gate.cur IMPACT.I
+ elec=gate vstep=0.5 nstep=10

comm this point should occur around VDD/2

comm plot the output
```

```
Plot.1D         Y.AXIS=I(drain) X.AXIS=V(gate) POINTS color=2 LOG
+               TITLE="Drain and Substrate Current vs Vgs, Vds=5 V"
+               device="cl/postscript" plot.out=hot_carriers.ps

Plot.1D         Y.AXIS=II X.Axis=V(gate) POINTS Color=2 LOG UNCHANGE

comm Plot.1D    Y.AXIS=I(sub) X.AXIS=V(gate) POINTS color=2


Plot.1D         Y.AXIS=HE(gate) X.Axis=V(gate) POINTS Color=2
+               TITLE="Gate Current vs Vgs"


plot.2d         boundary fill scale REGION JUNCTION title="Avanlache
Generation Rate Contours"
contour         II.GENER  NCONTOUR=15
comm            del.valu=5 fill

end
```

Appendix C

Process Sheet for Fabrication Process

C.1 Enclosed Process Flow

484L - no NRC details

LOG #	484L	PROJECT CODE
MATERIAL	GaN on Si <110> and <111>	PHONE
SAMPLE ID	A-E plus 2 test quarters (110) and (111)	DATE
DESTINATION	Jennifer/Peter	

Final ENLOSED Process, includes changes made from
464 L and 458 L 900 C ready

NO	TO BE DONE BY	PROCESS	COMPLETED date (m/d/yy) time (h mm)
1	Peter	**Thick SiO2 coating** clean HF dip/ acetone/IPA/DI rinse, blow dry, descum 3min Room 143	
2	Dan Roth	deposit 1 micron of thermal silicon dioxide OXFORD PECVD X C process for dense film	
		Passivation/P-Well Lithography	
3	Peter	Positive Lithography Exposure Level. GaN ISO (blocks GaN, opens Si) Mask· CU28006A (GaN ISO)	
4	Dan Roth	**Etch Oxide Layer** Etch in Oxford RIE etch time - **? sec**, etch down to **20 nm** of oxide **Careful removing oil backside, resist must remain intact**	
5	Peter	Send for Well Implant at KROKO	
6	Peter	ASH resist in O2 plasma (carleton) 5'+5'+5' Etch screen oxide, 45 s BOE etch Inspect	
	Rob/Rick/Carol (Carleton)	**Gate Oxidation** include two test wafers (111 and 110) for CV RCA clean Oxidation - tube temp - **900 C**, dry o2 time - 23 mins - actual time-____ oxide anneal - ONLY 10 min! target thickness - 20 nm remove test wafer for Al dot caps	

484L - no NRC details

Rob/Rick/ (Carleton)	**Polysilicon Gate Deposition**	
	include test wafer tube temperature - 625 C time - 25 min thickness - 0 4 um measured thickness - _____ um	
Peter NRC	**Gate PE**	
	Positive Lithography SPR 511A bake· 90 C, 2 min Exposure Level: Gate Mask CU 280 30 A develop MF319, 60 sec - DI rinse hard bake· 120C, 2 min inspect	
Carol/Peter (Carleton)	**Etch Gate Poly**	
	Technics Planar ETCH II power - 100 W gas - CF4/O2 pressure - 0 3 Torr time - 6 min (3' + 3' rotated) Ash Resist Plasma - 15 min total	
Carol/Peter (Carleton)	**S/D Oxide Etchback**	
	BOE etch - until Si is exposed in S/D windows time - 40 s actual time - _____ s	

484L - no NRC details

	Rob/Rick/Carol/Peter (Carleton)	**Source/Drain Diffusion** include test wafer 1 RCA Clean 2 Predeposition - POCl3 @ 20 C, tube temp - 900 C 5 min preheat 30s push 5 min warm-up 20 min dope 10 min hold 15 s pull 5min cool 3 remove PSG 1% HF etch - 2 min 30s electrical measurements - sheet resistance on test wafer sheet resistance - _____		
	Rick/Rob/Peter	**BPSG Deposition and Flow** include test wafer 1 Deposition deposit 0 1 um undoped / 0 5 um doped glass temp - 406 C target thickness - 0 6 um actual thickness - _____ um 2 FLOW temp - 900 C (phos drive-in tube) 5 min preheat N2 30 sec push to center N2 20 min anneal N2 30 sec pull N2		

484L - no NRC details

	10 min cool N2	
	GaN Recovery	
Carol/Peter (Carleton)	**GaN Recovery PE**	
	Positive Lithography Exposure Level Silicon Isolation (blocks Si, open GaN) Mask CU28005A (Silicon Iso)	
Dan Roth (NRC)	**BPSG Etch/Passivation Etch**	
	Etch in Oxford RIE press - 10 mTorr, temp 35 C O2 - 5 5, Ar - 50, C4F8 - 25 (sccm) ICP - 1500 watts, rf - 80 watts etch time - ___ **sec**, to remove 0 4 um BPSG + ~0 5 um thermal *PECVD* oxide **use oil - LEAVE at least 1000 A OXIDE ON GAN SURFACE - Etching to GaN ruins samples!**	
Peter	BOE w/surfacant etch to reveal GaN *etch rate should be around 800 A/min* time=_____	
PETER	Measure 2DEG in HALL ROOM	
	Start of GaN Processing	
Peter (carleton)	**MESA lithography** Ash Resist Plasma - 15 min total	
	Positive Lithography	

484L - no NRC details

Peter (NRC)		
	Exposure	
	Level MESA (w/ blocking transparency)	
Jennifer/Rongzhu	**CAIBE or ICP etch**	
	etch target 0 34 microns	
	etch time 8 1 min	
Peter	Removal of PR (stripping)	
	Inspect for complete resist removal - repeat descum if needed	
	Characterization	
	Dektak	
Peter	**Ohmic Contact Lithography**	
	Bilayor Lift-off Lithography	
	Exposure	
	Level Ohmic (w/ overhead transparency)	
	Ohmic Metallization	
Hue (NRC)	Descum Tecnics **30** sec at 100W	
	Pre clean	
	e-beam deposition **Ti/Al/Ti/Al** 300/800/300/800 (Å)	
	Put back in box ASAP after unload to minimize oxidation (for Ag only)	

484L - no NRC details

(NRC)	
Peter	**Ohmic metal anneal**
Peter	**Gate metal optical lithography**
	Lift-off Lithography Exposure Level Gate (w/ taped GaN ISO)
HUE	**Gate Metallization** Descum in Jupiter **60** sec at 50W Pre-clean DI rinse e-beam depostion: Pt based gate Lift-off anneal
Peter	electrical measurements
Peter	CLEAN --> ACE/IPA/DI/DESCUM
Dan Roth	**Dielectric Passivation**
	Deposit X Å of dielectric
Dan Roth	**Deposition on Samples:** Include small test piece of Si for measuring dielectric thickness with run **descum: 30 sec microwave in A116** **Pre-clean** Deposit x Å of silicon nitride under conditions for **high tensile** stress Thickness (ellipsometer) = _____Å Refractive index = _____
Peter (NRC)	**Pattern for RIE etch (Via1)** Positive Lithography Exposure (double) Level VIA1 (w/ overhead GaN ISO) expose: 12 sec at 10 mW/cm2? Level: Contact (CU 280 13B)
Rob/Rick (Carleton)	**Dielectric etch(Nitride and BPSG)** Leave 70 nm oxide in scribe channel

484L - no NRC details

		RIE etch 0 5 um BPSG Gas 15% O2 + 85% CHF3 RF POWER 350 W Pressure 150 mTorr rate~80 nm/minute time - 5 minutes, 30 sec actual time- _____		

484L - no NRC details

Carol/Peter (Carleton)	Etch to Bare Si (7800 A/min) Buffered HF etch 20 C time - 1 min actual time - _____ s	
Carol/Peter (Carleton)	ASH PR 5'+5'+5'	
Peter	**Pattern for 1ME**	
	Bilayer Lithography	
	Exposure (double) Level: 1ME (GaNFet v4)	
	Level Metal 1 (CU 280 14A)	
	resist develop	
	1ME metalization	
Hue	Descum in Jupiter **60** sec at 50W HF dip 10sec in BOE w/surfactant +DI rinse right before loading sample e-beam deposition Ti/Al	
Hue	Lift-off	
	Anneal N2 abmient	
Peter/Jennifer	Inspect Electrical testing	

Appendix D

CV calculations

This appendix give the mathematical formalism behind the CV analysis used to determine the threshold voltage of the MOS capacitors on test samples.

To determine the capacitance of the CV dot (C_{OX}), we have:

$$C_{OX} = \frac{A\epsilon_{OX}}{t_{OX}} \tag{D.1}$$

where ϵ_{OX} is the permittivity of the oxide and t_{OX} is the oxide thickness, and A is the area of the capacitor.

The CV measurement can be modelled as two capacitances in series: the oxide capacitance(C_{OX}) and semiconductor capacitance (C_S), which is variable. In the accumulation region, where the capacitance is at its maximum, the total capacitance is just C_{OX} whereas in other areas, it is the series combination of the two, given by:

$$C_G = \frac{C_{OX}C_S}{C_{OX} + C_S} \tag{D.2}$$

where C_G is the total capacitance.

The depletion layer maximum (W_t) can then be determined by extracting the value C_{min} from the CV curve, the flat region at which the capacitance is at a minimum:

$$W_t = \sqrt{\frac{4\epsilon_{Si}\phi_b)}{qN_A}} \tag{D.3}$$

where n_i is the intrinsic silicon doping , N_A is the acceptor concentration (note p-type silicon is implied here), ϵ_{Si} is the silicon permittivity and q is the electron charge. ϕ_b is given as

$$\phi_b = \frac{KT}{q} ln(\frac{N_A}{n_i}) \tag{D.4}$$

At full inversion of the layer, C_S can be expressed as:

$$C_S = \frac{A\epsilon_{Si}}{W_t} \tag{D.5}$$

Using equation D.5 in combination with D.3 and D.2, a transcendental equation can be achieved for the point at which C_G is equal to the minimum capacitance and hence the width of the depletion region is at it's maximum and we can use w_t. This equation is given as:

$$ln(\frac{N_A}{n_i}) - \frac{q}{\epsilon_{Si}}(\frac{q}{kT})(\frac{\epsilon_{Si}}{\epsilon_{OX}})^2[t_{ox}\frac{C_{OX}}{C_{min}} - 1]^2 = 0 \tag{D.6}$$

N_A is subsequently determined by solving using Newton's method.

The threshold voltage can be determined using the following standard equation for threshold voltage.

$$V_t = V_{fb} + 2\phi_b + \frac{\sqrt{2\epsilon_{Si}qN_A 2\phi_b}}{C_{OX}} \tag{D.7}$$