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Design and Analysis of CMOS Monolithic Inductor-less Voltage Controlled Oscillators

by

Maamoun Abou Seido, B. Sc.,

**A Master of Engineering thesis submitted to the
Ottawa-Carleton Institute for Electrical Engineering
Faculty of Engineering
Department of Electronics
Carleton University
Ottawa, Ontario, Canada**

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**“Design and Analysis of CMOS Monolithic
Inductor-less Voltage Controlled Oscillators”**

Submitted by

Maamoun Abou Seido, B. Sc.

in partial fulfillment of the requirements
for the degree of Master of Engineering.

Thesis Supervisor

Chair, Department of Electronics

Carleton University
September 1, 1995

Abstract

This document reports the design and implementation of high speed, low power, and low phase noise inductor-less monolithic voltage controlled oscillators. CMOS relaxation ring oscillators employing the device intrinsic parasitic capacitors are considered. A new approach in the analysis and optimization of phase noise performance in such oscillators is presented. The proposed technique is based on a frequency domain analysis that uses linearized device models for the prediction of the noise voltage present at the switching nodes of the ring oscillator, as well as on a time domain analysis for the prediction of the output period timing jitter.

Several guide lines for circuit design and layout techniques are given, for the implementation of a monolithic VCO within the available technology limitations. Three 1.2 μ m CMOS ring oscillator type VCO architectures are presented, of those, two oscillators circuits are new, optimized for improved noise performance. The measurement results indicate that the maximum operating frequency of the two new oscillators are 750 and 460 MHz. The power dissipation is 6.5 and 11.3 mW and the phase noise levels at 100 kHz offset from the carrier are -88 and -95 dBc/Hz, respectively.

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List of Symbols and Abbreviations

0 volt reference, Gnd
Supply voltage, Vdd
PMOS transistor
NMOS transistor
nnp Bipolar transistor
Resistor
Potentiometer
Inductor
Capacitor
Buffer
Diode
Varactor
Differential operational amplifier

Current source

Inverter

AC	Alternating current
BiCMOS	Bipolar CMOS
BJT	Bipolar junction transistor
CMC	Canadian Microelectronics Corporation
CMOS	Complimentary Metal Oxide Semiconductor
DC	Direct Current
ECL	Emitter-coupled logic
FM	Frequency Modulation
GaAs	Gallium arsenide
g_m	small-signal transconductance
IC	Integrated circuit
I/O	Input-output
L(f)	single-sideband phase noise spectral density
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	N-channel MOSFET device
PFD	Phase-frequency detector
PLL	Phase-locked loop
PMOS	P-channel MOSFET device
ppm	Part-per-million
Q	Quality factor
RF	Radio frequency
Si	Silicon
SPICE	A circuit simulator

T	Temperature
TRIO	Telecommunications Research Institute of Ontario
VCO	Voltage-controlled oscillator
VLSI	Very large scale integration
W/L	Width-to-length ratio of a MOSFET device

Chapter 1

Introduction

With the increasing interest in high frequency radio communication systems, there is also an increasing need for low-power monolithic circuits that can perform the functions required by front-end subsystems. The voltage controlled oscillator (VCO) is a key building block often used as part of a phase-locked loop (PLL) circuit in the design of transceivers in personal communication devices and clock and data recovery applications.

Due to their speed, low power, ease of integration, and their tunability over a wide range of frequencies [20], CMOS relaxation oscillators are increasingly being used as VCOs in applications which are phase noise sensitive.

This thesis presents a theoretical and experimental framework in analyzing the phase stability of monolithic relaxation ring oscillators. The feasibility of the design of a CMOS inductor-less oscillator that meets system specifications is also examined.

The document is organized in the following manner:

A review of the different alternatives in the design of monolithic voltage controlled high frequency (hundreds of MHz) oscillators is presented in Chapter 2. They are compared in terms of their integration technology versus their phase stability, maximum

operating frequency and power dissipation. Special emphasis is placed on the oscillators' phase stability and its impact on system performance, and on techniques for analyzing the phase stability of inductor-less oscillators.

Chapter 3 presents a frame-work for analyzing the phase instability of inductor-less oscillators. A technique for the prediction of noise induced jitter in CMOS relaxation ring oscillators is then developed. The prediction method involves modeling the oscillator's components, random noise sources, and employs frequency domain analysis using linearized models to predict the amplitude and bandwidth of the noise power density present at the circuit switching nodes. In the presence of such noise, the regenerative switching mechanism of relaxation oscillators is analyzed in the time domain to allow for the prediction of the output waveform period jitter.

Chapter 4 presents the design and implementation of an inductor-less CMOS VCO, with guidelines on the techniques to be employed to meet the design requirements within the limitations of the available technology. Three VCO circuit configurations are presented, distinguished by the employed optimization criteria and their post-layout simulation results.

The experimental setups and characteristic performance of the fabricated VCOs are reported in Chapter 5. These include the measured phase noise results, and an overview of the phase noise measurement technique and test procedure.

The final chapter provides a summary of the thesis and suggests recommendations for future work.

Chapter 2

The Design of Monolithic Voltage Controlled Oscillators

2.1 Introduction

Whether serving as a frequency synthesizer in wireless transceivers[23][24][25], or as part of a clock recovery circuit in high speed data communication systems [27][28][29], a monolithic voltage controlled oscillator can be an integral part in the implementation of today's fully integrated on-chip phase locked loops (PLLs). A block diagram of a conventional PLL is shown in Figure 2-1.

Figure 2-1: Conventional phase-locked loop for indirect frequency synthesis

A PLL can be employed as an oscillator whose frequency is locked onto a fixed reference frequency component such as a stable crystal oscillator. This is achieved by means of a feedback control loop. The phase frequency detector (PFD) compares the phase

of the synthesized frequency with that of the reference frequency resulting in an output voltage v_d with an average V_{cont} proportional to the phase difference. The loop filter serves to limit the PLL bandwidth and reduce the phase error.

In this chapter, different alternatives in the design of monolithic voltage controlled high frequency (hundreds of MHz) oscillators will be presented. They will then be compared in terms of their integration technology versus their phase stability, maximum operating frequency and power dissipation. Special emphasis will be placed on the oscillators' phase stability and its impact on system performance. In the last section of this chapter several techniques for analyzing phase stability of inductor-less oscillators will be reviewed.

2.2 Monolithic High Frequency Oscillators

Different types of voltage controlled oscillators (VCOs) are in common use [30], including crystal oscillators, resonator (LC, coaxial, or cavity) oscillators, active-RC oscillators, RC multivibrators and YIG-tuned Gunn Oscillators. There are two distinct approaches for the implementation of a fully integrated oscillator. The first approach utilizes some form of resonance and employs a positive-feedback loop consisting of an amplifier and a frequency-selective network. The circuit oscillates at the frequency in which the total phase shift in the feedback loop is zero and the magnitude of the loop gain is greater or equal to one. Such circuits can be implemented as an active-RC oscillator or as a resonant LC oscillator. Since the maximum operating frequency of active-RC oscillators is governed by the frequency response and the slew rate limitation of the op-amps, they are considered [42] not suitable for high frequency (hundreds of MHz) VCO implementations. LC oscillators can operate at higher frequencies with a great potential for monolithic implementation due to the possible realization of on-chip spiral inductors [1] [2].

The second approach to the implementation of monolithic frequency generators is based on the employment of a switching mechanism as in relaxation oscillators. These circuits operate by alternately charging and discharging an energy storage element (usually a capacitor) between two values of threshold voltages, hence providing the required

switching characteristics.

For an oscillator circuit to satisfy the condition of oscillation [31], the following components are necessary: an amplifying device, a regenerative feedback, some circuit non-linearity to define an amplitude, and some energy storage system to define the waveform shape. In the following subsections, an overview of VCOs which satisfy the condition of oscillation and have the potential for monolithic implementation will be presented. Examples from recent publications will be provided.

2.2.1 Resonant LC oscillators

The resonant LC circuit of Figure 2-2(a) is a commonly used type of oscillatory circuit. The circuit is frequency selective. Resonance, which can be defined as the state in which the current and the voltage in the reactive circuit are in phase with one another, occurs at frequency f_0 , which is defined as

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \quad (2.1)$$

In a practical model, the inductance has some resistance which can be represented as a parallel R_p as shown in Figure 2-2(b). This is not an actual resistance but a model of

Figure 2-2: a. The resonant LC circuit, b. Practical resonant LC circuit.

effective resistance due to losses in the inductor. The presence of resistance means that some energy stored in the reactive element is dissipated as heat in R_p . A quality factor, Q ,

is defined for resonant circuits as

$$Q = \frac{\text{energy stored in system}}{\text{energy dissipated per cycle}} = \frac{R_p}{2\pi f_o L} \quad (2.2)$$

where, f_o is the resonant frequency of the LC oscillator.

2.2.1.1 Varactor voltage controlled LC resonant oscillators

Figure 2-3 illustrates the principle of a voltage controlled resonator [19]. The schematic diagram shows the components needed to satisfy the condition of oscillation. The frequency f_o is controlled by varying the capacitance C electronically using a varactor diode as part of the LC tank capacitor. A varactor is a reverse biased diode whose junction capacitance C_T is a function of the reverse bias voltage v_R . The total tank capacitance ($C = \frac{C_S C_T}{C_S + C_T}$) varies by varying the control voltage v_C applied to the varactor's reverse bias voltage v_R , which in turn causes controllable variation in the oscillator's resonant frequency.

Figure 2-3: Voltage controlled LC resonant oscillator.

2.2.1.2 Examples of monolithic LC voltage controlled oscillators

As apposed to fully integrated oscillators, semi-integrated resonant LC frequency sources often employ off-chip LC tank and varactor circuits. Such external components serve as high Q LC resonators and linear frequency control characteristic varactors. Several approaches show promise for the realization of fully integrated voltage controlled LC resonators. In this subsection two examples of such implementations will be presented.

Nguyen and Meyer [3] demonstrated the use of on-chip inductors to implement the VCO. The technique involves using aluminum spiral inductors in standard bipolar technology. To overcome the difficulties of integrating a high quality on-chip varactor, the oscillator is implemented using two LC-tuned circuits with two different resonant frequencies (see Figure 2-4) in a classical Colpitts [41] configuration. The frequency is varied continuously by switching between the two feedback loops. The oscillator's die area excluding the I/O pads is $315\mu\text{m} \times 670\mu\text{m}$. It has a 200-MHz tuning range at 1.8 GHz center frequency, with quiescent power dissipation of 70mW reported. Due to the limited tank Q (about 5), the achievable phase noise at 100kHz offset from the carrier was reported to be -88dBc/Hz.

Figure 2-4: Simplified schematic of an LC VCO in a standard silicon bipolar technology

Yamauchi [4] developed a monolithic AlGaAs/GaAs HBT VCO with a tuned on-chip LC using a variable capacitance diode (varactor). The VCO schematic, shown in Figure 2-5, consists of an HBT, a varactor, inductors, a coplanar wave guide, a resistor, and capacitors. The chip size is 1.2X1.8mm, and the oscillator has a tuning range of 600 MHz and operates at 15 GHz. The power dissipation is reported to be around 75 mW, and the measured phase noise of -85 dBc/Hz at 100 kHz offset frequency.

Figure 2-5: Schematic diagram of an LC VCO in an ALGaAs/GaAs HBT technology

Due to limited Q availability when using on-chip inductors, the phase stability of monolithic resonant LC oscillators may not reach the values required by some applications. Other high quality implementations include the use of bond wire inductance [6], and the use of a plate-up gold inductor over thick oxide [7]. It is important, however, to notice that it is still difficult to implement a low resistance, wide-range varactor tuning capacitance using standard IC technology [24].

2.2.2 Relaxation oscillators

A general block diagram illustrating the principles of operation in a relaxation oscillator (or astable multivibrator) [42] is shown in Figure 2-6. The oscillator contains an ideal comparator circuit with hysteresis and an inverting integrator in a closed loop feedback configuration. The comparator switches between its two possible output states $L+$ and $L-$ when the integrator output reaches the comparator threshold voltage levels V_{TH} and V_{TL} , respectively. Ideally, the comparator should produce a square waveform causing the integrator to produce a triangular waveform with a rising edge slope of I_{L-}/RC and a falling edge slope of $-I_{L+}/RC$.

Figure 2-6: Simplified block diagram for an astable multivibrator oscillator

From Figure 2-6 the period of oscillation T can be seen to be:

$$T = T_1 + T_2 \quad (2.3)$$

during the interval T_1

$$\frac{V_{TH} - V_{TL}}{T_1} = \frac{L_+}{RC} \quad (2.4)$$

Hence

$$T_1 = CR \frac{V_{TH} - V_{TL}}{L_+} \quad (2.5)$$

Similarly,

$$T_2 = CR \frac{V_{TH} - V_{TL}}{-L_-} \quad (2.6)$$

The expression of the period of oscillation indicates that unlike resonant LC oscillators,

the frequency of relaxation oscillators is not a function of frequency-selective elements (LC) but of the parameters and characteristics of the elements used in its implementation.

2.2.2.1 Voltage controlled relaxation oscillators

The analysis presented in the previous subsection indicates that the frequency of relaxation oscillators is established by the time needed for the capacitor voltage to run down from an initial condition, set after switching, to the trigger point, set by the threshold voltage of the comparator device. Hence, the frequency control of such oscillators can be achieved by charging the capacitor with a controllable current. Several implementations involving voltage controlled current sources and voltage controlled resistors [43] can be used in the design of a linear transfer characteristics voltage controlled relaxation oscillator.

Designed using a ring composed of an odd number of inverting delay cells, a ring oscillator is a commonly used configuration of monolithic relaxation oscillators. It operates by alternatively charging and discharging the timing capacitors of the cell's intrinsic output capacitance. The period of oscillation in such circuits equals the total delay within the feedback loop. Frequency control is achieved by varying the delay of the controlled delay cells.

2.2.2.2 Examples of monolithic voltage controlled relaxation oscillators

Relaxation astable multivibrator and ring oscillators are commonly used as monolithic integrated-circuit VCOs. In this subsection, several circuit structures will be presented with implementation examples from recent publications.

Figure 2-7 shows a traditional emitter coupled bipolar multivibrator oscillator [56] (a similar structure is employed in CMOS oscillators). The multivibrator charges and discharges a single floating timing capacitor C_T . The maximum frequency is dependent among others on the value of the timing capacitor. As the value of that capacitor decreases, the oscillation frequency increases, with an additional decay in the oscillator signal amplitude, imposing a further limitation on the attainable maximum oscillating frequency.

Table 2-1 lists examples of monolithic implementations of emitter coupled multivibrator oscillators [46] [48] [49] [51], as well as other configurations of multivibrator oscillators in which the floating capacitor has been replaced with grounded capacitors to increase the amplitude of the output voltage [54] [56].

Figure 2-7: Emitter coupled bipolar multivibrator oscillator

A block diagram of a conventional ring oscillator composed of a feedback ring of three inverting controlled delay cells is shown in Figure 2-8a. The circuit intrinsic grounded parasitic capacitors are utilized as the relaxation oscillator charging and discharging capacitors, increasing the maximum attainable oscillating frequency. The period of oscillation is proportional to the sum of the cells' propagation delays. In a single loop ring oscillator, an odd number of inverting delay cells must be employed. Furthermore, a minimum of three stages should be used to ensure reliable oscillation. This would make the total phase shift around the loop sufficient to allow complete switching in each stage. Examples of current high frequency (hundreds of MHz) monolithic implementations of ring oscillators are listed in Table 2-1. The differential ring oscillator structure of Figure 2-8b reduces the sensitivity to power supply fluctuations, and special configurations [52] can

be further employed to provide quadrature frequency outputs. Examples of monolithic implementations utilizing such structures are also listed in Table 2-1.

Figure 2-8: a. Relaxation ring oscillators, b. Differential ring oscillator

A summary of current monolithic VCO implementations has been reported [44] [45]. Table 2-1 presents an update on current research work on monolithic relaxation VCOs. They are compared in terms of the implementation technology and oscillator circuit structure versus the reported operating frequency, power dissipation, and phase stability.

Table 2-1: Summary of monolithic relaxation VCO implementations to date

Technology	Oscillator circuit structure	max. operating frequency	Power dissipation	Phase stability	Reported by
Silicon Bipolar $f_T=9\text{GHz}$	Emitter coupled multivibrator	800MHz	-	-110dBc/Hz at 1MHz offset from 400MHz carrier	Dobos and Jenson [46]'94
Silicon Bipolar $f_T=3\text{GHz}$	Emitter coupled multivibrator	500MHz	-	-121dBc/Hz at 1MHz offset from 200MHz carrier	Verhoeven [48]'92
Silicon Bipolar $0.8\mu\text{m}$	Emitter coupled multivibrator	7.4MHz	70mW	-	Soyuer and Warnock [49]'92
Silicon Bipolar $f_T=3\text{GHz}$	Differential ring	180MHz	-	-	Sun [47]'91
BiCMOS $1\mu\text{m}$, $f_T=20\text{GHz}$	Differential ring	6GHz	-	-	Razavi and Sung [50]'94
BiCMOS $f_T=9\text{GHz}$	Emitter coupled multivibrator	90MHz	-	-	Kurita et al. [51]'91
AlGaAs/GaAs (HBT)	Differential ring	6GHz	-	-	Buchwald et al. [52]'92
NMOS $1.0\mu\text{m}$	Differential ring	1.1GHz	-	-	Enam and Abidi [53]'92
NMOS $0.75\mu\text{m}$	Multivibrator	1.4GHz	50mW	-	Banu [54]'88
CMOS $1.2\mu\text{m}$	ring	920MHz	7.4mW	-83dBc/Hz at 100kHz offset from 900MHz carrier	Thamsirianunt and Kwasniewski [55]'95
CMOS $1.2\mu\text{m}$	Multivibrator	80MHz	20mW	timing jitter of 160ppm	Flynn and Lidholm [56]'92
CMOS $1.0\mu\text{m}$	ring	320MHz	-	-	Enam and Abidi [57]'90

2.3 Oscillator Noise

Due to internal noise sources within the frequency source, all practical oscillators have undesirable phase or frequency noise modulation imposed on an otherwise ideal carrier. The oscillator's frequency stability is defined [32] by its long-term and short-term stability. As the term implies, long-term frequency stability describes frequency variations over long time periods. Usually referred to as frequency drift, it can be eliminated if the oscillator is locked in a PLL configuration with a PLL bandwidth larger than the possible frequency drift. Short term stability refers to frequency variations over short time periods, which cause a degradation in the frequency source performance even in locked oscillator configurations.

There are two types of short-term frequency variations. The first type is the deterministic or systematic signal, commonly called spurious. This type can be related to known phenomena in the frequency sources. The second type consists of the random frequency variations, commonly called phase noise since it also refers to the short term instabilities of phase jitter. The source of such random noise can be attributed to thermal noise, shot noise and flicker noise, in the passive and active components of a frequency source.

2.3.1 Quantifying phase noise

In the frequency domain the oscillator's phase noise is quantified by its output signal spectral purity. Ideally, the oscillator produces a single frequency f_0 . The output signal power spectral density consists of a line with zero width as shown in Figure 2-9a. In practical oscillators, the frequency is modulated by a random noise source originating from the oscillator itself. Hence, the output signal power spectral density has a bandwidth

(Figure 2-9b) which is inversely proportional to Q (the oscillator's quality factor).

Figure 2-9: Oscillator's spectral purity

The oscillator's phase noise is practically determined by measurement, due to the random nature of the noise sources inducing the phase instabilities and its theoretical prediction is often too complex. It is usually represented by a spectral density distribution plot, with different units being used to quantify the spectral density of phase fluctuations. The most commonly used noise measure is the single sideband phase noise relative to the total signal power - $L(f)$ - in dBc/Hz. Techniques to measure frequency sources' phase noise will be presented in Section 5.3.

In the time domain the oscillator's phase noise is quantified by random fluctuations in the period of their output waveforms, usually termed the timing jitter. This can be defined in terms of the mean μ_T and standard deviation σ_T of the oscillation period, as follows

$$Jitter = \frac{\sigma_T}{\mu_T} \quad (2.7)$$

Jitter is the commonly used term in the design requirement of digital communication systems. Figure 2-10 shows the effect of noise in time domain on the output waveform of a square wave oscillator. Techniques to measure the timing jitter of frequency sources are presented in [40] and [34].

Figure 2-10: Output waveform of a square wave oscillator showing the effect of noise

It should be noted that mathematical formulae [34] can be utilized to calculate the timing jitter for an oscillator from the measured spectral density of phase fluctuations and vice versa.

2.3.2 Phase noise impact on system performance

Phase noise is an important parameter in the design of receiving and transmitting systems, and is often the limiting factor determining the performance in an application. In the following subsections, two basic examples of phase noise impairment in analog and digital communication systems will be demonstrated.

2.3.2.1 Phase noise impairment in analog communication systems

Phase noise requirements vary dramatically depending on the modulation waveform being used (e.g., FSK, MPSK) and the communication system concerned. A number of different modulation types and several examples of the impact of phase noise on system performance were demonstrated in [36]. One example of phase noise impairment in analog communication systems present in a multi-signal environment in the reciprocal mixing due to high local oscillator (LO) phase noise sidebands. This can lead to out-of-band signals being translated into the IF. That type of performance degradation in a receiver front end is shown in Figure 2-11, where the local oscillator phase noise sidebands in the receiver are shown directly transferred to the signals at the IF port due to the mixing process. The presence of strong adjacent signals mixing with the LO phase noise sidebands results in a

corresponding reduction in the receiver's sensitivity.

Figure 2-11: Local oscillator phase noise affects receiver selectivity in a multi-signal environment

2.3.2.2 Phase noise impairment in digital communication systems

In high speed data communications, phase noise is expressed in terms of clock jitter, it affects the clock recovery process in bit synchronizers [38]. This type of performance degradation can be analyzed while predicting the effective decoding window in the presence of timing jitter [37]. In the generic data acquisition system of Figure 2-12, clock jitter added to the expected data jitter reduced the effective decoding window, which imposes constraints on the maximum operating frequency of the system and causes degradation in the expected bit error rate (BER). Techniques to measure jitter tolerance in digital communication systems are presented in [39].

Figure 2-12: The effective decoding window in the presence of jitter

2.4 Analysis of Phase Noise in Inductor-less Oscillators

Resonant LC oscillators are widely used in high frequency receivers. Since the 1920s several text books [8][9] and a number of papers [10][11] were published in which theories were developed for the prediction of phase noise performance. Noise in these circuits is filtered into a narrow bandwidth by Q of the oscillator. This allows a relatively simple technique for noise performance optimization, where the phase noise is inversely proportional to Q . This section reports different approaches introduced within the last few years in analyzing, modeling, and simulating the phase noise of inductor-less oscillators, with special emphasis on the techniques that can be applied to CMOS voltage controlled oscillators.

Abidi and Meyer [13] analyzed timing jitter in relaxation (multivibrator) oscillators that have either a floating or a grounded timing capacitor. The problem was stated and analyzed in time domain. The analysis showed that the standard deviation in the oscillation period σ can be calculated as

$$\sigma(\delta T) = \alpha \left\{ \sum_i \frac{V_{ni}^2}{S_i^2} \right\}^{1/2} \quad (2.8)$$

where S : is the slope of node capacitor voltage waveform,

V_n : is the node rms voltage noise,

α : is a circuit dependent constant that varies with the relative slope of the voltage, ramp to the rms slope of the noise, and

i : denotes the i^{th} transition (two transitions per node).

As an application of that theory, the timing jitter of a relaxation oscillator was predicted and measured for a fixed injected rms noise. For the more important application, which is the determination of the jitter due to the inherent noise sources in the oscillator circuit, conventional noise analysis techniques using SPICE [17] were utilized to calculate the inherent rms voltage noise to allow for the prediction of the timing jitter.

Weigandt, Kim and Gray [14] investigated the timing jitter in CMOS ring oscillators composed of source-coupled differential delay cells (Figure 2-13). They derived a relationship between the ring oscillator delay elements design parameters and the noise induced timing jitter.

Figure 2-13: Ring oscillator composed of source-coupled differential delay cells

The traditional noise analysis techniques [21] were applied and the output voltage noise was determined by integrating the noise spectral density over the bandwidth of the low pass filter formed by the linearized model of the load resistor of the inverting stage and the gate capacitor of the next stage. An effort was made to study the effect of time varying noise sources and the inter-stage interaction. The analysis results were compared with

with simulation results from SPICE Monte-Carlo transient noise analysis. The timing jitter modelling technique showed that the ring oscillator jitter is inversely proportional to the square root of the total capacitance at the output of each inverter, and inversely proportional to the gate-source bias voltage above threshold of the source-coupled devices. This implies an inverse relationship between jitter and power dissipation.

Razavi [16] analyzed the phase noise in a fully differential three stage ring voltage controlled oscillators by modeling the signal path in the VCO with a linearized (single-ended) circuit as shown in Figure 2-14, where R and C represent the output resistance and the load capacitance of each stage respectively, and $G_m R$ is the gain required for steady oscillations.

Figure 2-14: Single-ended linearized model of the signal path in a differential VCO

The oscillator was considered as a linear feedback system having a transfer function describing the noise shaping in the oscillator. An equation was derived describing the phase noise components due to an injected noise source I_n , at offset frequency $\Delta\omega$ from the center frequency ω_o as

$$\left| \frac{V_1}{I_{n1}} [j(\omega_o + \Delta\omega)] \right|^2 = \frac{R^2}{27} \left(\frac{\omega_o}{\Delta\omega} \right)^2 \quad (2.9)$$

The technique was verified by comparing the theoretically predicted phase noise with simulation results. Phase noise was simulated by injecting a sinusoidal noise current into different nodes in the circuit and calculating the Fast Fourier transform of the transient analysis simulation output waveforms.

McNeil [15] described a theoretical framework for analyzing and predicting jitter in ring oscillators. A statistical analysis in the time domain was adopted, taking into consideration each stage and adding a uniform amount of phase on a varying amount of time. The analysis predicted the variance of the period to be

$$\sigma^2 = \left(\frac{K_o}{f_o} \right)^2 \frac{e_n^2 T_o}{2} \quad (2.10)$$

where e_n : is the spectral density of a VCO ideal white noise input,

K_o : is the VCO frequency control constant (in Hz/V),

f_o : is the VCO center frequency, and

T_o : is the nominal (average) period of oscillation.

This methodology of analyzing jitter was verified through simulations where traditional noise analysis techniques [21] were used to predict e_n of the oscillator. Furthermore the simulation results were compared with experimental measurement on a fabricated oscillator circuit.

2.5 Summary

This chapter has presented the different alternatives present today in the design of monolithic voltage controlled high frequency (hundreds of MHz) oscillators. The alternatives were compared in terms of their circuit configuration and implementation technology versus their phase stability, maximum operating frequency, and power dissipation. Relaxation oscillators have higher potential in a monolithic implementation on silicon than LC resonant oscillators. CMOS relaxation ring oscillators, employing the device intrinsic parasitic timing capacitors, were bound to be the most suitable and widely used on-chip sub-circuits for high frequency large scale monolithic implementation, but the phase stability of such oscillators is of great concern.

The level of the oscillators' phase noise is a primary design parameter due to its impact on analog and digital communication systems performance. It is quantified in terms of the oscillators' spectral purity or timing jitter.

Several techniques for analyzing, modeling, and simulating the phase stability of inductor-less oscillators were reviewed. The presented methods employ conventional noise analysis techniques to model random noise sources. Phase noise prediction is carried out in the time domain relying on transient analysis simulations, or in frequency domain relying on a linearized model analysis. A further quantitative analysis and prediction of inductor-less oscillators' timing jitter or phase noise needs to be carried out.

Chapter 3

Jitter in CMOS Ring Oscillators

3.1 Introduction

In Chapter 2, two different approaches were illustrated for the implementation of a monolithic frequency generator. The first approach relies on a positive-feedback loop that consists of an amplifier and an integrated LC frequency-selective network, these frequency sources are known as linear oscillators. In spite of the name, some form of non-linearity has to be employed to provide control of the amplitude of the output sine wave. The first step in the design and analysis of that type of oscillators is a linear one, and frequency domain methods of feedback circuit analysis can be readily employed [8].

The second approach in the design of fully integrated oscillators employs astable multivibrator circuit building blocks, commonly called non-linear oscillators. Operating principles and examples of this type of oscillator were previously presented in Chapter 2. Due to the non-linear fashion in which these oscillators operate, no systematic studies are available in the literature on how the periodic output waveforms are being randomly modulated by the noise sources in the components of the oscillator.

In this chapter a frame-work for analyzing phase instability in inductor-less oscillator circuits is presented. The goal of the presented analysis is to predict the output period timing jitter error in a CMOS relaxation oscillator composed of a ring of an odd number of inverting amplifiers, either in a simple structure similar to that shown in Figure 3-1a or in a more complex differential structure as shown in Figure 3-1b. The prediction method

employs conventional techniques for modeling the oscillator's components' random noise sources. It relies on frequency domain analysis using small signal linearized models to predict the amplitude and bandwidth of the noise power density present at each switching node. In the presence of such noise, the regenerative switching mechanism of relaxation oscillators was analyzed in the time domain yielding a prediction of the output waveform period jitter.

Figure 3-1: Examples of CMOS ring oscillator configurations

In section II of this chapter, an overview of random noise sources within a MOSFET device is presented, while section III provides a linear analysis in the frequency domain to model the filtering mechanism limiting the amplitude and the bandwidth of the noise power density at the switching nodes of the oscillator. Time domain analysis of the regenerative switching in the CMOS ring oscillator is illustrated in section IV, in order to predict the amount of induced timing jitter in the presence of noise.

3.2 Noise Sources in MOSFET Devices

Other than the substrate and power supply pick up noise, random noise sources associated with CMOS relaxation ring oscillators are associated primarily the MOSFET

device. Noise in such devices have been analyzed in several text books on analog circuit design ([12]and [21]). An overview of MOSFET's random noise sources will be summarized in this section.

There are two main noise sources in a MOS device: thermal noise which is associated with carriers in the channel, and flicker noise associated with the trapping and release of electrons in the Si-SiO₂ interface region. As these noise sources contribute to the total drain current they can be modeled, as shown in Figure 3-2.

Figure 3-2: a. Channel current noise source in the output, b. Input referred voltage noise source

The thermal noise is a white noise characterized by its spectral density S_{IW} :

$$S_{IW} = \begin{cases} \frac{4kT}{R_{REF}} & \text{ohmic region} \\ \frac{4kTg_m}{3} & \text{saturation region} \end{cases} \quad (3.1)$$

where T : is temperature in degrees Kelvin,

k : is Boltzman's constant,

R_{FET} is the equivalent FET resistance, and

g_m : is the small signal trans-conductance at the operating point.

The flicker noise current in both the ohmic and saturation regions is characterized by the spectral density S_{IF} :

$$S_{IF} = \frac{K_f I_{DQ}}{C_{ox} L^2 f} \quad (3.2)$$

where K_f : is the flicker noise coefficient,

I_{DQ} : is the quiescent current,

f : is the offset frequency from the device operating frequency,

C_{ox} : is the capacitance density of the gate-channel capacitor, and

L : is the device effective channel length.

The total noise power $S_{IN} = S_{IW} + S_{IF}$ and hence the rms current noise source I_N of Figure 3-2a can be defined as the square root of the total noise power S_{IN} integrated over the frequency range of interest. Similarly, the input referred voltage noise source of Figure 3-2b can be modeled using an equivalent MOSFET small signal model, so that the total input referred noise power (S_{VN}) is S_{IN} / g_m^2 , and the input referred rms voltage noise source (V_N) is I_N / g_m .

Looking at the expressions for the flicker and thermal noise power, it is evident that at high offset frequencies from the device operating frequency, the thermal noise is the dominant noise source. The frequency at which the spectral density of the flicker noise crosses that of the thermal noise can be predicted by solving for $S_{IW} = S_{IF}$, and assuming the device is operating at saturation, then:

$$f = \frac{3}{16} \frac{K_f}{kT} \left(\frac{V_{GS} - V_T}{L^2} \right) \quad (3.3)$$

Hence, for smaller device geometries it would not be possible to ignore the flicker noise models when predicting noise performance of oscillator circuits.

Other noise sources might be modeled in a MOS device, such as the device drain and source resistances. The spectral densities of these sources can be modeled as

$$\begin{aligned} S_{IR_D} &= \frac{4kT}{R_D} \\ S_{IR_S} &= \frac{4kT}{R_S} \end{aligned} \quad (3.4)$$

where R_D and R_S are the drain and source parasitic resistances respectively. The device gate resistance might contribute to the noise sources in the MOS device. But, it is quite difficult to model such sources, since the available extraction techniques cannot yield accurate extraction parameters for the source, drain and gate resistors, and in general it is of more importance to consider these models at high operating frequencies.

3.3 Analysis in Frequency Domain for the Prediction Noise Power Spectral Density

In this section, analysis in the frequency domain is employed to predict the amplitude and the bandwidth of the noise power spectral density at the switching nodes in a CMOS ring oscillator circuit. Thermal random noise sources within the device are white; they have a spectral density that is essentially flat for all frequencies. In practice there is always some filtering mechanism limiting the bandwidth and therefore the power of that noise.

Approaches aiming at calculating the bandwidth of non-linear oscillators are problematical. Conventional techniques rely on the utilization of small signal analysis models [13] [15]. However, this requires a steady bias point not readily available, since the oscillating devices under consideration experience large voltage excursions.

In the next subsection, an attempt is made to derive a small signal model for MOSFET devices employed in a CMOS ring oscillator circuit configuration. The analysis is followed by an illustrative application example to model the noise power density at the switching nodes of a CMOS inverter chain ring oscillator.

3.3.1 Small signal AC analysis model for the MOS device:

Previous work on the analysis of noise performance in ring oscillators using linear models [14] [16] has lagged, since the ring circuit does not fit well into either of these linear models. In fact, there are many energy storage elements within a multistage ring oscillator circuit, and they cannot be modeled only by the gate capacitance of each stage.

In an attempt to provide a technique that describes the filtering mechanism between

different nodes within the circuit, effort was directed to providing a proper small signal analysis model for each MOSFET device within the oscillator circuit. This allows for the prediction of noise power amplitude and bandwidth at each critical node within the circuit by employing linear circuit analysis techniques. While the models can be complex for hand calculation, the analysis can be done using linear circuit simulators such as HSPICE [17].

A small signal AC analysis model of a MOS device can be derived at each biasing point. In a CMOS oscillator with large voltage swings, the actual biasing conditions can be predicted by examining its behavior in the time domain. Each individual MOS device is assumed to experience a steady biasing condition in the middle of its switching point. Through transient analysis simulations this biasing point can be derived. Figure 3-3 shows the adopted small signal AC analysis model for the MOS device.

Figure 3-3: Adopted small signal AC analysis model for the MOS device

The parameters g_m and g_{ds} , for each of the small signal AC analysis models for the oscillator circuits' MOS devices, were extracted by first running SPICE transient analysis on the circuit under consideration to obtain an assumed biasing condition for each device, which was approximated as the middle of the transient dynamic range at the ports of each device. Then SPICE AC analysis was run using these predicted biasing points as the initial conditions of simulation, thus utilizing SPICE numerical capabilities in calculating the parameters for the small signal AC analysis model. The capacitances C_{gs} and C_{gd} were each approximated linearly, as 2/3 of the total gate capacitance, and the capacitance C_{sb} was extracted as the difference between the total source capacitance and the C_{gs} capacitance, whereas the capacitance C_{db} was extracted as the difference between the total drain capacitance and the C_{gd} capacitance.

In the following subsection, linear circuit analysis using the derived small signal analysis model will be illustrated, applying the modeling technique to a CMOS inverter chain ring oscillator.

3.3.2 Simulated noise power density of the CMOS ring oscillator

The analysis in frequency domain using the adopted AC small signal modeling technique was applied to CMOS ring oscillator circuits composed of a loop of three inverting delay elements. Shown in Figure 3-4 is a transistor level schematic of a CMOS ring oscillator structure composed of three identical stages of inverting amplifiers. This is a hypothetical design for a CMOS voltage controlled oscillator circuit, since the loop is not loaded with an output buffer stage and it does not have a frequency control mechanism.

Figure 3-4: CMOS oscillator circuit composed of three stages of identical inverting amplifiers

Two oscillator circuits were simulated, both had the same structure as that of Figure 3-4. SPICE level 3 model for a CMOS $1.2\mu\text{m}$ (CMOS4S) process parameter was employed. The first oscillator (referred to as osc1) has identical stages with device sizes of minimum width ($2\mu\text{m}$) for the utilized NMOS and PMOS devices. The other oscillator circuit (referred to as osc2) has the same circuit structure as of osc1, but a three times larger devices' width. It is of interest to note that the osc2 circuit is expected to occupy three times more silicon area, and to dissipate three times more power than osc1. The device sizing of the considered circuits was selected to determine through simulations the relationship between the design parameters of the inverter cells used in the ring-oscillator and the resulting noise power density at the switching nodes.

In an attempt to model the noise power at the critical nodes in the circuit, each of the active components in the considered oscillators was replaced with a linear sub-circuit of the corresponding small signal AC analysis model. At each node, one noise current source replaced all the injected noise current sources at that node, with the rms current corresponding to the sum of the injected noise power at that node. As an example, Figure 3-5 a, b and c shows the noise power spectral density at one of the critical nodes of osc1 due to an injected equivalent noise current source at different nodes in the ring. The total noise power spectral density at the switching nodes was predicted using superposition analysis. Figure 3-5.d shows the total noise power spectral density at one of the critical nodes of osc1.

a. Noise power spectral density at node 1 for an injected noise current at node 1

b. Noise power spectral density at node 1 for an injected noise current at node 2

c. Noise power spectral density at node 1 for an injected noise current at node 3

d. Total noise power spectral density at node 1 using superposition analysis

Figure 3-5: Noise power spectral density at a critical node of osc1

Since the oscillator circuits under consideration have identical stages, the power spectral density at each of the switching nodes was identical. Figure 3-6 shows the power spectral density at a switching node for the two considered circuits.

Figure 3-6: Noise Power spectral density at a switching node for oscillator circuits 1 and 2

The small signal AC analysis simulation on the considered oscillator circuits showed that the band pass noise filtering function had a center frequency matching the oscillator's operating frequency in the transient analysis of the actual transistor level simulations. Figure 3-6 assists in making such a comparison. The transient simulations predicted oscillator's operating frequency and the AC small signal analysis power spectral density center frequency had a 3% difference, which provided an indication of the accuracy of the adopted linear model in approximating the noise filtering functions between different nodes in the circuit.

An important parameter for the prediction of the noise-induced timing jitter (whose analysis is presented in the next subsection) is the root-mean-square (rms) noise at the

switching nodes in the circuit. The mean-square noise can be calculated by integrating the noise power spectral density curve. It can be approximated knowing the bandwidth and the center frequency power of the noise power spectral density, [19] defined as the mean square noise $\overline{V_n^2}$ for a bandpass filter with noise bandwidth BW , and the center frequency noise power N_o as

$$\overline{V_n^2} = N_o \times BW \quad (3.5)$$

The rms noise voltage is defined as the square root of $\overline{V_n^2}$. Table 3-1 summarizes some extracted parameters from the noise power spectral density curves of osc1 and osc2 circuits.

Table 3-1: Small signal AC analysis simulations' extracted results for oscillator circuits 1 and 2

	osc1	osc2
Device width	2 μm	6 μm
Device length	1.2 μm	1.2 μm
Parasitic capacitor at switching nodes	6.08 fF	18.35 fF
Expected dissipated power	1.23 mW	3.65 mW
Noise power spectral density center frequency	1368 MHz	1362 MHz
Noise power at center frequency	144.4e-18 V ² /Hz	48.12e-18 V ² /Hz
Noise Bandwidth	1662 MHz	1657 MHz
Mean-square noise	240.0 nV ²	79.7 nV ²
rms noise	489.9 μV	282.3 μV

It can be seen that for ring oscillator circuits of similar structure, the dominant factors

affecting the mean square noise were the circuit design parameters. The noise power appears to be inversely proportional to the parasitic capacitor at the switching node. However, this may not hold true for circuits of different structures. Hence, analog design techniques adopted to minimize noise power in the design of op-amps and analog filters can be employed for the partial optimization of phase noise performance in the design of CMOS ring oscillators.

The analysis in frequency domain for the prediction of the switching nodes noise for a multi stage ring oscillator, reveals that

- the mean-square noise at the switching nodes is inversely proportional to the oscillator circuit device width, implying an inverse relationship between the mean-square noise and the power dissipation, and
- the noise at the circuit switching nodes is minimized for circuit structures which allow maximum filtering of the active device random noise sources.

3.4 Time Domain Analysis for the Prediction of Noise-Induced Jitter

In this section, the effect of noise at the switching nodes on the output waveform jitter is analyzed. The objective is to predict the amount of noise-induced timing jitter in a multi-stage ring oscillator configuration. The regenerative feedback switching mechanism of ring oscillators is analyzed in time domain in order to predict the effect of each stage on the total jitter of the output waveform. The analysis will be applied to the CMOS ring oscillator circuits introduced earlier in this chapter, to illustrate how transient analysis simulation can assist in the optimization of inductor-less oscillators' noise performance.

3.4.1 Regenerative switching of feedback ring oscillators

The period of a ring oscillator output waveform is determined by the delay of each stage and the number of stages employed. In the presence of noise, the period in each cycle of oscillation is combined with a random timing error. The objective of this analysis is to determine the noise power present at the switching nodes in the circuit, and its contribution

to the timing jitter at the output period.

A simplified model of a three stage CMOS ring oscillator is shown in Figure 3-7a. C_{Li} corresponds to the total input capacitance of the i^{th} stage, and it is assumed that it is the only energy storage element defining the shape of the output voltage waveform at the switching node. It is also assumed that each inverting stage has typical input voltage versus output voltage characteristics with hysteresis, similar to that shown in Figure 3-7b, in which the output switches to one of its possible states L^+ and L^- when the input reaches the threshold voltage levels V_{TH} and V_{TL} , respectively.

Figure 3-7: Time domain analysis of regenerative switching for a CMOS ring oscillator

The output waveform at the switching nodes of a three stage CMOS ring oscillator are shown in Figure 3-7c. Each inverter stage in the ring contributes a nominal time delay to the total period of oscillation. The delays contributed by the i^{th} stage τ_{ri} and τ_{fi} are measured from the time the output begins switching to the time it reaches the threshold voltage of the input to the next stages V_{TL} and V_{TH} , respectively. Hence the period of oscillation T for a three stage ring oscillator is given as

$$T = \tau_{r1} + \tau_{f1} + \tau_{r2} + \tau_{f2} + \tau_{r3} + \tau_{f3} \quad (3.6)$$

Any error of the time of crossing at the threshold voltage is a timing error passed to other stages in the ring and contributes to the total output jitter. Figure 3-7d shows that an error voltage $V_n(t_x)$, at the nominal time of threshold crossing, shifts the actual delay time by an amount $\Delta\tau$ proportional to the voltage error divided by the slope of the output waveform. The fluctuations at times $t_1, t_2, \dots, \text{and } t_6$ all contribute to total error in the oscillation cycle output period δT . Thus,

$$\delta T = \frac{V_{n1}(t_1)}{S_{r1}} + \frac{V_{n1}(t_4)}{S_{f1}} + \frac{V_{n2}(t_2)}{S_{r2}} + \frac{V_{n2}(t_5)}{S_{f2}} + \frac{V_{n3}(t_3)}{S_{r1}} + \frac{V_{n3}(t_6)}{S_{f1}} \quad (3.7)$$

where $V_{ni}(t)$: the noise error voltage at the output of the i^{th} stage on the time instant t , due to the contributions of all noise sources within the circuit,

S_{ri} : the rising edge slope of the output waveform at the i^{th} stage, and

S_{fi} : the falling edge slope of the output waveform at the i^{th} stage.

Abidi and Meyer [13] showed that the noise induced jitter σ_T in the relaxation oscillator is the standard deviation of the random variable δT , and can be calculated as

$$\sigma_T = \alpha \sqrt{\text{mean value of} \left(\frac{V_{n1}^2(t_1)}{S_{r1}^2} + \frac{V_{n1}^2(t_4)}{S_{f1}^2} + \frac{V_{n2}^2(t_2)}{S_{r2}^2} + \frac{V_{n2}^2(t_5)}{S_{f2}^2} + \frac{V_{n3}^2(t_3)}{S_{r1}^2} + \frac{V_{n3}^2(t_6)}{S_{f1}^2} \right)} \quad (3.8)$$

where α is a proportionality constant [13] that varies with the relative slope of the load

capacitor charging current waveform to the rms slope of the noise. $V_{n1}(t_1)$ and $V_{n1}(t_4)$ are statistically independent values of the noise voltage $V_{n1}(t)$. A similar argument is made for $V_{n2}(t)$ and $V_{n3}(t)$, the noise voltage at nodes 2 and 3, respectively. Hence, period jitter can be calculated as

$$\sigma_T = \alpha \left(V_{n1}(rms) \left(\frac{1}{S_{r1}^2} + \frac{1}{S_{f1}^2} \right)^{1/2} + V_{n2}(rms) \left(\frac{1}{S_{r2}^2} + \frac{1}{S_{f2}^2} \right)^{1/2} + V_{n3}(rms) \left(\frac{1}{S_{r3}^2} + \frac{1}{S_{f3}^2} \right)^{1/2} \right) \quad (3.9)$$

where $V_{ni}(rms)$ is the rms noise voltage at the output of the i^{th} stage. A normalized timing jitter can be defined in terms of the mean μ_T and the standard deviation σ_T of the period of oscillation as

$$Jitter = \frac{\sigma_T}{\mu_T} \quad (3.10)$$

which is usually expressed in parts per million.

In any ring oscillator structure, the per stage jitter contributed during the i^{th} stage output waveform rising edge can be predicted as

$$\sigma_{\tau_{ri}} = \alpha \frac{V_{ni}(rms)}{S_{ri}} \quad (3.11)$$

Similarly, the per stage jitter contributed during the i^{th} stage output waveform falling edge can be predicted as

$$\sigma_{\tau_{fi}} = \alpha \frac{V_{ni}(rms)}{S_{fi}} \quad (3.12)$$

In the following subsection, the analysis will be further illustrated by applying the jitter prediction technique on a CMOS inverter chain ring oscillator.

3.4.2 Simulated per-stage timing jitter of CMOS ring oscillators

The timing jitter prediction technique is further illustrated by applying the analysis on the CMOS ring oscillator circuits *osc1* and *osc2* of Figure 3-4. These circuits were previously analyzed in frequency domain using small signal AC analysis models to predict the rms noise at the circuits' switching nodes. Transient simulations using HSPICE [17] were done on the two considered oscillator circuits, to predict the period of oscillation and the output waveforms slopes. Table 3-2 summarizes the simulation extracted parameters, the predicted per stage jitter contribution and the output period jitter.

Table 3-2: Transient simulation extracted results of oscillator circuit 1 and 2

	osc1	osc2
Power dissipation	1.23 mW	3.65 mW
Frequency (f)	1326 MHz	1312 MHz
Oscillation period (T)	753.7 psec	762.0 psec
Output waveform rising slope(S_r)	1.87e+10 V/sec	1.84e+10 V/sec
Output waveform falling slope (S_f)	2.75e+10 V/sec	2.68e+10 V/sec
rms noise (V_{ni})	489.9 μ V	282.3 μ V
Per stage jitter contribution during rising edge (σ_{tri})	26.2 α fsec	15.3 α fsec
Per stage jitter contribution during falling edge (σ_{tfi})	17.8 α fsec	10.5 α fsec
Output jitter = σ_T/μ_T	72.8 α ppm	42.3 α ppm

Examining the predicted per stage jitter contribution during the rising and falling edges of the output waveform, it is evident that for the same amount of predicted rms noise voltage the jitter contribution is expected to be higher during the rising edge, due to the weak PMOS device driving capability. Comparing the simulation extracted parameter of the two oscillator circuits 1 and 2, it is clear that the absolute device sizing and power

dissipation are not the only factors effecting the amount of noise induced timing jitter.

In ring oscillators having similar amounts of rms noise at the switching nodes, the noise-induced timing jitter is inversely proportional to the slopes of the switching nodes' output waveforms. The slope of the output waveform is dependent in a complex way on both the output waveform's peak to peak voltage swing and on the oscillating frequency. Hence, the analysis in the time domain for jitter prediction in ring oscillators can lead to the following conclusions:

- output period jitter is minimized by maximizing the waveform slopes at the switching nodes within the circuit;
- jitter is minimized by maximizing the switching nodes voltage waveform amplitudes; and
- a high frequency ring oscillator has less time jitter than a low frequency unit employing the same circuit except for timing capacitors. Therefore, to obtain improved phase jitter, it is useful to operate the oscillator at a frequency Nf_0 , where f_0 is the desired frequency and divide the output by N .

3.5 Summary

Timing jitter in CMOS ring oscillators was investigated using a frame-work composed of an analysis in frequency domain using linearized device modeling, followed by an analysis in time domain to predict the amount of noise induced jitter through the regenerative switching mechanism of ring oscillators.

The analysis assists in the selection of an optimized oscillator circuit structure, and in providing the design of an oscillator with optimum phase noise performance. Even though the technique provided a realistic comparative prediction of noise induced jitter, the simulated results may be an order of magnitude lower than the anticipated measured values. This can be attributed to several factors such as the employed models of MOSFET devices' random noise sources, or to the weak assumption that the feedback oscillator is a memory-less system in which jitter induced per oscillation cycle does not effect the jitter error of the future cycles.

Chapter 4

The Design and Implementation of a Monolithic CMOS Inductor-less Oscillator

4.1 Introduction

The design of a CMOS on-chip relaxation ring oscillator, which employs the circuit intrinsic parasitic capacitances, provides a low cost, high speed, low power and easy to integrate alternative of voltage controlled oscillators (VCOs). This chapter will review different VCO performance characterization considerations. The design and implementation of an inductor-less CMOS VCO circuits with the optimum characteristics achieved within the technology limitations will be presented.

In the next section various VCO design issues will be addressed, with guidelines on techniques to be employed to meet these requirements within the limitations of the available technology. In the last section of this chapter the implemented VCO circuit configurations will be introduced, characterized by the optimization criteria introduced in chapter 3, their post-layout simulation results are also presented.

The presented circuit post layout simulations were performed using the typical process parameter of Nortel 1.2 μ m CMOS (CMOS4S), whose process parameters are given in Appendix A. The circuit layout and the corresponding device sizes are presented in

Appendix B.

4.2 VCO Design Considerations

The design requirements of a practical VCO implementation can be summarized by the following basic features:

- output frequency with minimal phase instability;
- linear frequency control characteristics within the intended range of operating frequency;
- design insensitive to power supply fluctuations and noise of adjacent on chip circuitry;
- design insensitive to power supply, temperature and process parameters variations, and
- possible testability, with the ability to preserve the signal integrity at an output pad.

In this section each of these features will be discussed, along with several illustrated implementation alternatives and guidelines leading to an optimum VCO design within the limitations of the available technology.

4.2.1 Phase stability

The analysis of timing jitter in CMOS ring oscillators was presented in Chapter 3 provides a technique for predicting an approximate comparative measure of the timing jitter in such oscillators. This technique can assist in the selection of an optimized VCO structure, and in sizing the MOS devices within the limitations of the provided silicon area and the expected power dissipation.

In the frequency domain, the analysis of ways to reduce the noise power density at the switching nodes of a CMOS inductor-less relaxation oscillator lead to the following conclusions:

- circuit structures which allow the maximum filtering of random noise sources should be utilized, and
- maximum device widths should be employed up to the limit imposed by allowed

power dissipation.

In time domain, the induced timing jitter was predicted for a selected monolithic inductor-less oscillator circuit structure, for a given silicon area and power dissipation. The analysis suggested that the induced jitter can be minimized by employing the following optimization criteria:

- maximization of the waveform (rising and falling edge) slopes for each switching node within the feedback loop,
- maximization of the switching nodes voltage waveform amplitudes, and
- if possible, operating the oscillator at higher frequency Nf_o , when f_o is the desired frequency and dividing the output by N .

4.2.2 Frequency control characteristics

Of the many requirements concerning the frequency control of a VCO, some of the more important include:

- linearity of the frequency versus control voltage,
- large tuning range,
- large gain factor, and
- capability of accepting wide band modulation.

Since some of these requirements are in conflict with one another, a compromise dependent on the intended application is needed. Theoretically, the VCO output frequency f_{out} is linearly related to the control voltage (V_{cont}) by the following relationship

$$f_{out} = f_o + K_o V_{cont} \quad (4.13)$$

where: K_o is the VCO gain factor in Hz/V, and

f_o is the minimum operating frequency of the VCO.

Any non-linearity in the transfer characteristics of the VCO over the intended range of operating frequency should be avoided, since it affects the closed loop performance of the PLL. Therefore, an effort should be made to maintain a constant slope K_o for the VCO

transfer characteristics. Ideally, the VCO gain factor K_0 should also be independent of temperature, power supply and process parameters variations. This issue will be dealt with in the next subsection.

In relaxation ring oscillators the frequency is determined by the gate delays. For a basic ring structure of n inverting amplifiers the oscillating frequency would be described as:

$$f = \frac{1}{n \sum_{i=1}^n (t_{di} + t_{ci})} \quad (4.14)$$

where t_{ci} and t_{di} are the charging and discharging propagation delays of the i^{th} cell.

Hence, the frequency control mechanism can be achieved through the use of voltage controlled resistors (VCR) controlling the charging or discharging current path for each individual gate within the ring, as shown in Figure 4-1b.

Figure 4-1: a. Inverting amplifier cell, b. Conventional controlled delay cell

For linear VCO characteristics, it is important to employ a linear VCR. In a CMOS implementation, the voltage applied to $R_{control}$ varies the trans-conductance of a MOSFET device. A single NMOS device can provide a working but crude VCR. [22] demonstrates a more sophisticated structure for a VCR shown in Figure 4-2c. It achieves higher and linearized dynamic range of frequency control if device sizes are optimized through

transient analysis simulations for best performance over the intended range of operating frequency. Figure 4-3 illustrates the V-I simulated transfer characteristics of MOS voltage controlled resistors, simulations which were accomplished using the typical process parameter of Nortel 1.2 μ m CMOS (CMOS4S) using transistors of minimum device width (2 μ m).

Figure 4-2: Voltage-controlled resistor (VCR)

Figure 4-3: V-I transfer characteristics of MOS voltage controlled resistors

Employing either one of the MOSFET voltage control resistor configurations on a basic controlled delay cell similar to that of Figure 4-1b reduces the minimum operating frequency f_0 of the VCO to zero. This is usually undesired, since it reduces the control ratio K_0 of the VCO characteristics, and hence slows the acquisition of the phase locked loop. The basic controlled delay cell can then be modified to that shown in Figure 4-4, where parallel NMOS devices are used to provide the discharging path for the switching

capacitors. Hence sizing M2 defines the minimum operation frequency f_0 , while sizing M3 defines the maximum operating frequency of the VCO, and hence M3 defines the control ratio K_0 .

Figure 4-4: Controlled delay cell over a limited range of frequency

4.2.3 Sensitivity to power supply fluctuations and noise of adjacent on-chip circuitry

Ring oscillators are quite sensitive to power supply fluctuations, such as current spikes and ground bounce of common on-chip Vdd and gnd rails, as well as noise induced from adjacent on-chip circuitry. Several layout optimization techniques must be considered to reduce the VCO sensitivity to such noise sources:

- usage of separate power supply pads for the VCO circuit reduces the sensitivity of the oscillator to changes in supply voltage levels of the common on-chip power rails,
- on-chip decoupling capacitors between Vdd and gnd lines filter the power supply high frequency noise, and
- to isolate the VCO circuit from the substrate noise of adjacent circuitry, more substrate contacts are placed within the N and P wells, and double guard rings of n+ and p+ are connected to a stable Vdd and gnd rails are placed around each well

of the VCO cell as shown in Figure 4-5.

Figure 4-5: Guard rings around the VCO cell to reduce substrate noise of adjacent circuitry

4.2.4 Sensitivity to integration, temperature and power supply variation

Process parameter variations between best case and worst case parameters can lead to changes in the center operating frequency of the VCO. Other variations in the center operating frequency can occur due to changes in the nominal operating temperature on the chip, or to variation in the supplied voltage. Figure 4-6 illustrates the effect of such variations on the transfer characteristics curve of a VCO.

Figure 4-6: The effect of temperature, process parameters and power supply variation on the center operating frequency of a VCO

The basic technique adopted to overcome this problem is to design the VCO that can be controlled over a wide range; taking into consideration that the VCO intended center frequency can be reached under worst case and best case conditions. This technique increases the VCO gain control ratio K_o , which might affect the stability of the PLL and would increase the recovery time of the PLL. For temperature and power supply variations, another technique can be adopted to eliminate their effect on the center frequency of which the device operates, this can be achieved through the use of voltage controlled resistors (VCR) controlling the charging current path for each individual gate within the ring, as shown in Figure 4-7. The reference control voltage V_{REF} is obtained using a bandgap circuit producing a regulated voltage that eliminates the circuit sensitivity to temperature and power supply variation. Such a circuit is difficult to design in a fully CMOS process, but it is easily achievable in a BiCMOS process. Reference [26] describes a bandgap circuit that controls a PMOS voltage controlled resistor with a reference voltage of 0.5V.

Figure 4-7: Controlled delay cell insensitive to temperature and power supply variations

4.2.5 Testability of the VCO

Inductor-less integrated oscillators are designed to provide an on-chip stable frequency generator, whose output should be capable of driving other on-chip circuitry. However, it is important to be able to probe the oscillator's output and characterize its behavior. In a typical $1.2\mu\text{m}$ CMOS process, a bonding pad can have a capacitance of 0.5pF , and the pin capacitance varies in the range of a few pF and is dependent on the packaging technology.

Since standard digital output buffers are incapable of driving the signal at very high frequencies (hundreds of MHz), in a fully CMOS process only the following two testing techniques can be utilized. The first uses a custom designed multistage output buffer to drive the expected output pad and pin model. However, the number of stages that can be used is limited, since it is basically dependent on the number of stages in which the oscillating waveform might die out at different process parameter conditions. The maximum number of buffer stages can be identified using the best NMOS and the worst PMOS (or vice versa) process parameter variations.

Figure 4-8: CMOS multi-stage output buffer to drive the VCO high frequency output

The second technique for probing high frequency outputs employs frequency dividers to scale down the output frequency by a factor of N , which makes it possible to buffer the signal using a digital output driver. It should be noted that the latter technique reduces the measured output phase noise power by a factor of $20\log(N)$ dBc/Hz, and the use of dividers adds some unexpected jitter to the output signal.

Figure 4-9: Frequency divider scales down the VCO high frequency output

In a BiCMOS process it is possible to use the high speed capability of the bipolar device to drive the VCO output. As shown in Figure 4-10, a single bipolar device in an emitter follower configuration can be employed to buffer the oscillating waveform to the bonding pad. However, care must be taken in the design of the off-chip probing and biasing circuitry of the transistor Q_1 , to avoid overloading the on-chip CMOS buffer if a large current is drained from the emitter follower device.

Figure 4-10: Emitter follower bipolar transistor to drive a high frequency output signal

Another alternative can be adopted to probe the output signal in a BiCMOS process without the danger of overloading the on-chip CMOS buffer. As shown in Figure 4-11, this can be achieved through the utilization of a CMOS to ECL interface stage between the CMOS buffer and the emitter follower device. In the circuit of Figure 4-11, M1 should be sized to match the performance of Q2, and an off-chip reference voltage should be used to insure the matching performance between the NMOS and bipolar differential devices.

Figure 4-11: CMOS to ECL interface circuit between the CMOS buffer and the emitter follower

4.3 VCO Implementations

In this section, the design of an all CMOS high frequency voltage controlled oscillator will be introduced. The considered circuit configurations are presented with an illustration of the adopted device sizing optimization criteria. The implemented oscillators were characterize by performing various post layout simulations.

4.3.1 Circuits considered

Three inductor-less CMOS VCO circuits are considered, all employing the circuits' intrinsic parasitic capacitance as the relaxation oscillator switching device, and implemented using the Nortel 1.2 μ m CMOS process (CMOS4S).

4.3.1.1 Reference VCO

This VCO is a duplicate of previously reported work [45] of a relaxation based three stage ring oscillator (schematic diagram shown in Figure 4-12). The frequency control voltage is applied at the gate of an NMOS device controlling the delay of the pull-down path at one of the ring stages. The circuit represents the least number of components required for the implementation of a functional CMOS relaxation voltage controlled oscillator. This test circuit is used as a design reference to provide a compatible setup to study the performance of the other newly developed VCOs. The reference VCO circuit will be referred to as VCO1.

Figure 4-12: Reference VCO circuit schematic diagram

4.3.1.2 Single loop optimized VCO

The single loop optimized VCO circuit schematic diagram is shown in Figure 4-13. The circuit is a ring of three inverting controlled delay cells. Parallel pull down paths are employed to provide a frequency control over a limited range of operating frequency. Linear frequency control characteristics were achieved using a linearized current controlled devices in the pull down path of each stage in the ring structure. The single loop optimized VCO circuit will be referred to as VCO2.

Compared to VCO1, the design is expected to have good phase noise performance (the adopted optimization criteria employed in device sizing will be presented in Section 4.3.2). Also, it has a linear frequency versus control voltage transfer characteristics over a limited range of operating frequency.

Figure 4-13: Single loop optimized VCO circuit schematic diagram

4.3.1.3 Differential optimized VCO

While differential ring oscillator structures reduce the effect of power supply high frequency noise, this improvement is achieved at the price of decreased maximum oscillating frequency due to increased node capacitance. Figure 4-14 shows a simplified schematic diagram of the newly developed differential VCO, composed of two three-stage ring oscillators cross coupled using NMOS devices. One stage is a controlled delay cell that utilizes a MOSFET voltage controlled resistor for linear frequency control characteristics over a limited range of operating frequencies. Two identical but 180° out of phase outputs can be available: a dummy output buffer was employed to insure symmetry between the two rings. The differential optimized VCO circuit will be referred to as VCO3.

Figure 4-14: Differential optimized VCO simplified schematic diagram

4.3.2 Device sizing

VCO1 is a duplicate of a previously designed voltage controlled oscillator, with maximum speed as its main optimization criteria. VCO2 and VCO3 are optimized in the time domain for:

- maximum speed,
- maximum node voltage amplitudes and slopes for an optimum phase noise performance for selected VCO circuit structure, and
- linear frequency controllability.

The technique adopted for the design of linear frequency controllability over a limited

range of operating frequencies was previously demonstrated in Section 4.2.2. The following subsection illustrates the means employed in sizing the devices towards the fulfillment of the optimization criteria.

4.3.2.1 The frequency of CMOS ring oscillator versus device sizing

The frequency of CMOS ring oscillators depends in a complex way on the size of all devices used, since the size of each device controls both its current capability and its capacitance. The period of oscillation (T) in a ring oscillator of n stages is proportional to the sum of the capacitors' charging and discharging propagation delays (t_{ci} and t_{di} , respectively):

$$T = \sum_i^n (t_{ci} + t_{di}) \quad (4.15)$$

In the following analysis the propagation delay of an inverter stage i loaded by the $i+1$ stage will be calculated. As shown in Figure 4-15 the device sizes of the driving and loading stages are denoted by the symbols i and $i+1$, respectively.

Figure 4-15: An inverter stage i loaded by the $i+1$ stage in a CMOS ring oscillator configuration

Ignoring the diffusion capacitances of the driving stage, the output load capacitance is given by

$$C_L = C_{ox} (W_{ni+1} L_{ni+1} + W_{pi+1} L_{pi+1}) \quad (4.16)$$

where, C_{ox} : is the capacitance per unit area of the device gate to channel capacitor, and
 W and L : are the device channel width and length, respectively.

To simplify the analysis it will be assumed that the current in a CMOS inverter flows only during the transition, and the current during a charging transition is approximated to be a ramp of duration equal to the charging propagation delay (t_{ci}) and a peak value equal to the saturation current. Similar assumptions are made for the current during the discharging delay (t_{di}). It will be also assumed that the input signal experiences fast transition. The voltage v_C across a capacitance C charged by the current i_C is given by

$$v_C = \frac{1}{C} \int_0^t i_C dt \quad (4.17)$$

Thus, for an inverter stage load capacitance C_L charged to V_{dd}

$$C_L V_{dd} = \frac{1}{4} C_{ox} \mu_p \left(\frac{W_{pi}}{L_{pi}} \right) (V_{dd} - |V_{thp}|)^2 t_{ci} \quad (4.18)$$

where, μ_p : is the mobility of holes, and

V_{thp} : is the threshold voltage of the PMOS device.

Hence, from equations (4.16) and (4.18) the charging propagation delay t_{ci} is given by

$$t_{ci} = \frac{(W_{ni+1} L_{ni+1} + W_{pi+1} L_{pi+1}) V_{dd}}{\frac{1}{4} \mu_p \left(\frac{W_{pi}}{L_{pi}} \right) (V_{dd} - |V_{thp}|)^2} \quad (4.19)$$

Similarly, the discharging propagation delay t_{di} is given by

$$t_{di} = \frac{(W_{ni+1} L_{ni+1} + W_{pi+1} L_{pi+1}) V_{dd}}{\frac{1}{4} \mu_n \left(\frac{W_{ni}}{L_{ni}} \right) (V_{dd} - V_{thn})^2} \quad (4.20)$$

where, μ_n : is the mobility of electrons, and

V_{thn} : is the threshold voltage of the NMOS device.

In the analysis of speed optimization by device sizing it is assumed that each device uses its smallest gate length (given by the process technology), whereas its gate width is optimized for speed. The width might affect different delays both through its effect on driving force and self-loading and its effect on loading the previous stage. Thus, improvement in speed can be obtained by trying different device sizes in a circuit simulator like SPICE.

4.3.2.2 Node voltage amplitude and slope versus device sizing

The waveform shape at the output of any stage is a ring oscillator dependent on both the driving capability and the loading of that stage, and also the transition delay at its input. Therefore, the optimization objectives of maximum amplitude and the rising and falling edge slopes of the node voltages are dependent on the sizes of all devices used. A ring oscillator structure having equal voltage amplitudes and slopes at each switching node is a solution to the optimization objective.

A timing simulator (SPICE) was used to equalize the rising and falling edge slopes, and the iterative simulations were started using a ratio of NMOS and PMOS device widths at which $t_{di}=t_{ci}$ in equations (4.19) and (4.20). This also result in an output waveform with a 50% duty cycle.

The switching nodes' waveform amplitudes and slopes were equated through the equalization of the propagation delays of each stage. In the three stage ring oscillator of Figure 4-16, this was achieved by employing a scaling ratio S in sizing the device width each stage. For an output stage of size equal to the smallest stage in the ring, the ratio S was mathematically calculated to be 1.26. This ratio was used to choose a starting value for sizing the devices in an iterative transient analysis simulation using HSPICE [17].

Figure 4-16: A three stage ring oscillator model with an equal per stage propagation delay

The optimization resulted in nearly rail-to-rail equal slopes switching nodes' output waveforms. Figure 4-17 shows the simulated output waveforms for the optimized oscillators (VCO2 and VCO3) compared to the reference oscillator (VCO1). The circuits' layout and corresponding device sizes are presented in Appendix B.

a. VCO1

b. VCO2

Figure 4-17: VCOs' switching nodes simulated output waveforms

4.3.3 Post layout simulation results

To further characterize the considered VCO circuits various post layout simulations were performed. The oscillators' output frequency versus control voltage transfer characteristics are shown in Figure 4-18. VCO2 operates between 600 and 720 MHz with an average tuning constant (K_o) of 29 MHz/V, and VCO3 operates in the frequency range of 435 and 490 MHz, with an average tuning constant of 14 MHz/V. While VCO1 has a wider tuning range between 310 and 735 MHz, its tuning constant varies drastically as its single NMOS tuning device switches between the linear region and the saturation mode of operation.

Figure 4-19 shows the simulated power dissipation versus the operating frequency for the three VCOs. The reported power dissipation results include that of the VCO circuit and its first stage inverting amplifier output buffer.

Simulation results of the VCOs' maximum operating frequency as a function of power supply and temperature variations are reported in Figure 4-20 and Figure 4-21 respectively.

Figure 4-18: VCOs' transfer characteristics

Figure 4-19: VCOs' power dissipation versus the oscillating frequency

Figure 4-20: VCOs' sensitivity to power supply variations at their maximum operating frequency

Figure 4-21: VCOs' sensitivity to temperature variations at their maximum operating frequency

4.4 Summary

Various voltage controlled oscillator design issues have been discussed, with guidelines on techniques to be employed to meet the requirements for the implementation of an inductor-less CMOS VCO, within the limitations of the available technology.

It was demonstrated that the implementation of CMOS monolithic relaxation ring oscillators, which employ the circuitry intrinsic parasitic capacitors, provide a low cost, high speed, low power and easy to integrate design alternative. The design of three VCO circuit configurations in a 1.2 μ m CMOS process was introduced, characterized by the adopted optimization criteria and their post-layout simulation results. Table 4-1 provides a summary of the implemented VCOs' characteristics.

Table 4-1: Summary of the implemented VCOs' characteristics

	VCO1 [45]	VCO2	VCO3
circuit structure	ring	ring	differential ring
optimization criteria	•high speed	•high speed •linear frequency control •max. node voltage swings and slopes	•high speed •linear frequency control •max. node voltage swings and slopes
range of operating frequency [MHz]	310-735	600-720	435-490
VCO gain factor [MHz/V]	106	29	14
power dissipation at max. osc. frequency [mW]	5.8	6.1	11.8

5

Measurement Results of the Integrated VCOs'

5.1 Introduction

In this chapter, measurement results of the implemented integrated voltage controlled oscillator circuits will be presented. Different versions of the optimized VCOs and the reference VCO were included in two IC submission, both were fabricated at Nortel in a 1.2 μ m double-polysilicon double-metal N-well CMOS process (CMOS4S) through the Canadian Microelectronics Corporation (CMC). The objective of the first submission (it will be referred to as CUOS2) was to verify the optimization methodology and design guidelines introduced in Chapters 3 and 4, by comparing the measured performance of the optimized VCOs with that of the reference VCO. The other integrated circuit (it will be referred to as CUOS3) was fabricated to further investigate the performance of the optimized VCOs as well as the effect of the selection of the absolute device sizes and the employment of special layout considerations to reduce noise from adjacent on-chip circuitry.

To evaluate the performance of the VCO the following measurement results were performed and are presented:

- spectrum analyzer power spectral output,
- oscilloscope traces for the oscillator output waveform,

- voltage to frequency transfer characteristic,
- power dissipation as a function of the oscillation frequency,
- sensitivity to power supply variation, and
- FM single sided band phase noise measurement.

To provide a comparative study and reliable measurement results, the experimental setups, utilized equipment and test procedure should be reported. Three [32] phase noise measurement techniques that can be utilized, and an overview of there techniques with special emphasis on the employed technique will be presented.

In Section 2 of this chapter the experimental setups and characteristic performance of the VCOs will be presented. The utilized phase noise measurement technique, the test procedure and the FM single sided band phase noise measurement results will be presented in Section 3. The effect of the selection of the VCOs' absolute device sizes is demonstrated in section 4, while section 5 demonstrates the effect of the utilization of special layout considerations in the reduction of noise induced from adjacent on-chip circuitry. The measurement results will be summarized and tabulated in the last section of this chapter.

5.2 Performance evaluation of the VCOs

In this section, different measurement results that characterize the performance of the VCOs are presented, such as the VCO spectral output and waveform, transfer characteristic, power dissipation and sensitivity to power supply variations. The measurement were performed on the free running VCO, and it is commonly referred to as the open loop performance characterization of the oscillator. It is important to indicate that the same type of measurement result might vary due to some variations in the measurement equipment used and the measurement setup employed; hence a detailed description of the utilized equipment and test setup will be presented in the first subsection.

All measurements were performed on bonded ICs with a standard ceramic 68-pin PGA package. A total of 10 packaged ICs of each submission were received. The measurements reported in this document were performed on one of those 10 packaged ICs, that IC was randomly selected. While all the other nine received ICs had the same performance with slight variation in the VCO center operating frequency of up to 3% the

center frequency for the reported one, but up to 6% variation was noticed in the performance of the same VCO designed in two different submissions.

5.2.1 The VCO test setup

The test bed shown in Figure 5-1 was designed to test the open loop performance of each VCO circuit. It was constructed using a general purpose prototyping board, and one LM7805 three terminal voltage regulator sourced from an 8 Volt DC external power supply was utilized to provide a 5 Volt DC. The 5 Volt power supply was used for both the VCO circuitry and to the on-chip output buffer. A 10K ohm potentiometer connected across the 5V regulated power supply was employed to provide the required VCO DC control voltage ranging from 1 to 5Volt. Decoupling capacitors of 0.1 μ F connected directly across the VCOs' power supply and control voltage package pins to filter the power supply high frequency noise. Separate power supply pins for the VCOs allowed for power dissipation measurement for the VCO circuitry excluding power dissipated in the output buffers. Since the on-chip multi-stage CMOS output buffer cannot provide buffering for a low impedance load (50ohm), a high-frequency high-input-impedance probe was utilized to buffer the signal to the spectrum analyzer and to the oscilloscope. A 2.7 nF capacitance at the VCO's output was used to provide AC coupling for the high-input-impedance probe.

5.2.2 VCO waveform and power spectral output

Figure 5-2 shows the oscilloscope traces for the VCOs' output waveforms, with the captured traces showing VCO1 oscillating at 750MHz with a peak to peak voltage of 500mV, VCO2 oscillating at 720MHz with a peak to peak output voltage of 1000mV, and

VCO3 oscillating at 460MHz with a peak to peak voltage of 1050mV. The measured outputs had a sinusoidal waveform shape.

Figure 5-3 shows the power spectral density of the VCOs' output. A 500kHz frequency span¹ was used for each trace with a resolution bandwidth² of 1kHz. The center frequency of each reported VCO trace is indicated on the bottom left corner of each graph. Such spectra at a small frequency span can be utilized to give a measure of the phase noise performance for each VCO. The technique employed will be discussed in Section 5.3.1.1. Looking at the bandwidth of the output traces, it can be seen that the optimized VCOs 2 and 3 have better noise performance than that of the reference VCO1.

The spectral purity of the VCOs' output was measured on the spectrum analyzer using a wider frequency span. Even though the oscilloscope output waveforms seem to have a sinusoidal shape, the spectral outputs (graphs not shown) have some even harmonics which were at least 20dBm lower than the carrier power. It should be noted that this is not a good measure of the VCOs' spectral purity, since it is obtained from the buffered output, knowing that an on-chip multistage CMOS buffer was utilized to drive the output pad and that the package pin circuitry reduces the validity of this measurement.

1. spectrum analyzer term: power spectrum frequency range

2. spectrum analyzer term: averaging bandwidth in the power spectrum calculation

a. VCO1 output waveform at
720MHz

(x-axis 500 ps/div)

(y-axis 100 mV/div)

b. VCO2 output waveform at
720MHz

(x-axis 500 ps/div)

(y-axis 200 mV/div)

c. VCO3 output waveform at
460MHz

(x-axis 500 ps/div)

(y-axis 200 mV/div)

Figure 5-2: Oscilloscope traces for the VCOs' output waveforms

a. Power spectral output of VCO1

b. Power spectral output of VCO2

c. Power spectral output of VCO3

Figure 5-3: Spectrum analyzer power spectra for the VCOs' outputs

5.2.3 VCO transfer characteristics

The voltage to frequency transfer characteristics for the three VCOs are shown in Figure 5-4. The measurement was performed using the same setup of Figure 5-1 by gradually varying the control voltage from 1V to 5V between the minimum and maximum operating frequencies. Simulation results are drawn on the same graph to show the effect of process parameter variations on the center operating frequency of the VCO. In Figure 5-5 the measured transfer characteristics of the three VCOs were superimposed on one another to provide a comparative view on the linearity of the transfer characteristics of VCO2 and VCO3 compared to those of VCO1. Table 5-1 shows tabulated results of the VCOs' range of operating frequency and the average VCO gain (K_0).

a. Measured and simulated transfer characteristics of VCO1

b. Measured and simulated transfer characteristics of VCO2

c. Measured and simulated transfer characteristics of VCO3

—— Measured
..... Simulated

Figure 5-4: VCO voltage to frequency transfer characteristics

Figure 5-5: Superimposed transfer characteristics of the three VCOs

Table 5-1: Measured VCOs' range of operating frequency and the average VCO gain

	VCO1	VCO2	VCO3
Range of operating frequency [MHz]	290 - 755	625 - 750	420 - 465
VCO average gain K_o [MHz/V]	116	31	11

5.2.4 VCO power dissipation

The low power dissipated in the monolithic minimum device sizes CMOS relaxation ring voltage controlled oscillator is one of its most attractive features: less than half that dissipated in other comparable performance VCOs presented in Chapter 2.

Figure 5-6 shows the power dissipation measurement for the three VCOs; the reported power includes that of the VCO and its first stage inverting amplifier output buffer. Separate power supply pads for the VCO circuitry and the multistage buffer were utilized in the design of VCO2 and VCO3 which allowed measurement of the power dissipated in the VCO circuitry itself. However, to measure the power dissipated by VCO1, its buffer simulated power dissipation results were utilized to predict the exact power dissipated by

the oscillator circuitry.

Figure 5-6: VCOs' power dissipation versus the oscillating frequency

The average power dissipated in CMOS circuits is dependent on the dynamic switching characteristic of the devices and can be approximated [35] as:

$$P_{average} = fV^2C \quad (5.21)$$

where f : is the switching frequency,
 V : is the peak to peak switching voltage, and
 C : is the load switching capacitance (device parasitic capacitances).

Examining the graphs for VCO2 and VCO3 in Figure 5-6 indicates that the average dissipated power is linearly dependent on frequency since it was optimized for maximum and equal switching voltage amplitudes at the critical nodes in the circuit at different operating frequencies. This is not the case for VCO1, which experiences reduced voltage amplitudes at high operating frequencies, and hence, reduced power dissipation at these frequencies.

5.2.5 VCO sensitivity to power supply variations

It is useful to study the variation in the VCO operating frequencies due to changes in power supply voltage. This is of extreme importance in battery operated circuits since it experiences a decrease in the supply voltage over the life time of the battery.

As shown in Figure 5-7, the VCOs' sensitivity to power supply variations curves at their maximum operating frequency. The measurements were made using the same test setup shown in Figure 5-1, but employing an external variable DC power supply to power the VCOs, and applying a control voltage equal to the applied power supply voltage to examine the oscillator's maximum operating frequency. By inspection, the graphs indicate that the maximum operating frequency of the oscillators is sensitive to variations in power supply, hence some measures (discussed in Section 4.2.4) must be adopted to guarantee that the VCO can be locked within a certain range of operating frequencies.

It is important to indicate that the measured curves match simulation results with slight variations due to process integration parameters. These results also provide a clear indication of the maximum operating frequency potential if such a device were to operate at a lower power supply voltage (i.e., 3.3V).

Figure 5-7: VCOs' sensitivity to power supply variations at their maximum operating frequency

5.3 VCO Phase Noise Measurement

In this section, the phase noise measurement of each free running VCO will be reported, providing a measure of the phase stability of the optimized oscillators VCO2 and VCO3 compared to that of the reference oscillator VCO1. To provide comparable measurement results, the adopted phase noise measurement technique will be presented in the first subsection, while the test setup will be demonstrated in the next subsection.

5.3.1 Phase noise measurement techniques

In the following subsections, three phase noise measurement techniques [32] will be described: the direct spectrum analyzer method, the frequency discriminator method and the phase detector method. The basic measurement setup, the equipment utilized, and the advantages and disadvantages of each will be presented. The measurement results reported were obtained using the HP3048 phase noise measurement setup which is based on the phase detector method.

5.3.1.1 The direct spectrum analyzer method

Figure 5-8: Direct spectrum phase noise measurement technique

The simplest measurement technique is shown in Figure 5-8, in which the frequency source is directly connected to a spectrum analyzer tuned to the source frequency, hence measuring the power spectral density of the oscillator output. The single-sideband signal to carrier ratio measured phase noise $L(f)$ in dBc/Hz at any offset frequency f can be calculated as:

$$L(f) = P_N(f) - P_C \quad (5.22)$$

where $P_N(f)$: is the measured average noise power in a 1-hertz bandwidth in dBm at an offset frequency f , and

P_C : is the measured carrier power in dBm.

Since it is impractical to make measurements in a 1-hertz bandwidth using the direct spectrum technique, typically, the average noise power bandwidth is corrected by a normalization factor. In addition, another correction is needed when measuring random noise using a spectrum analyzer since its detection circuitry is calibrated for accuracy in measuring discrete signals (sinusoids). Hence, using the direct spectrum technique, the phase noise $L(f)$ in dBc/Hz at any offset frequency f can be calculated as:

$$L(f) = P_M(f) - P_C - BW \text{ Normalization} + SA \text{ Effect} \quad (5.23)$$

where $P_M(f)$: is the measured average noise power for a given resolution bandwidth in dBm at an offset frequency f ,

P_C : is the measured carrier power in dBm,

BW Normalization: is the correction factor to calculate the measured noise power of a 1 Hz rectangular bandwidth = $10 \log(1.2 \times \text{resolution BW})$ dB for an HP8591 spectrum analyzer [33], and

SA Effects: is the spectrum analyzer effects correction factor = 2.5 dB for an HP8591 spectrum analyzer [33].

While the direct spectrum measurement technique [32] is simple to use and can be utilized for a broadband frequency range, it can not measure high purity frequency sources, nor can it measure noisy sources that have high level of amplitude modulation or large frequency drift.

5.3.1.2 The frequency discriminator method

Figure 5-9: The frequency discriminator phase noise measurement technique

In this method (shown in Figure 5-8), the frequency fluctuations of the source are translated to baseband voltage fluctuations by the frequency discriminator which can be measured by a baseband analyzer.

There are various implementations of frequency discriminators, one of which is the delay line/phase detector implementation which is employed in the HP3048A phase noise measurement system [34]. In that implementation of frequency discriminators, the signal from the tested frequency source is split into two channels, the signal of one path being delayed relative to the signal in the other path. This unequal delay converts the frequency fluctuations of the signal into phase fluctuations; the phase detector then converts phase

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fluctuations to voltage fluctuations, which are read by the spectrum analyzer and are related to the phase noise of the source. Phase noise measurement using that method requires a procedure for set up and calibration and for data conversion and correction which is automated in the HP3048A phase noise measurement system [34].

Figure 5-10: Delay line/phase detector implementation for the frequency discriminator phase noise measurement technique

The frequency discriminator technique has been reported [32] as suitable for measuring free running sources with high level phase noise. Though it has a low broadband noise floor, it is difficult to implement due to loss in the delay line which makes it limited in the maximum range of offset frequencies. It also has poor close-in sensitivity (sensitivity at small offset frequencies).

5.3.1.3 The phase detector method

Figure 5-11: The phase detector phase noise measurement technique

The phase detector technique is the most sensitive and broadband method. This technique (shown in Figure 5-8) converts the phase difference between the device under test frequency source and the reference frequency source into voltage, using the phase detector, that voltage can then be measured by the baseband spectrum analyzer.

This phase noise measurement technique is also implemented in the HP3048A system [34]. A typical block diagram is shown in Figure 5-12. Where two sources at the same frequency and in phase quadrature are input to the double-balanced mixer used as a phase detector, the output of the mixer will be the sum and the difference frequencies. The sum is filtered by the low-pass filter (LPF) to prevent it from overloading the LNA or the baseband analyzer. Any phase fluctuation that is not common to both signals will be represented by a phase term in the difference frequency signal. The LNA improves the sensitivity and the noise figure of the spectrum analyzer. Analog spectrum analyzers are used for high offset frequency measurements and digital spectrum analyzers are useful for close-in offsets but limited in the maximum range of offset frequency. Hence, a combination of both is needed for a wide offset frequency range.

It is important that the phase detector input sources stay in quadrature (90° phase relationship), since it is the condition at which the system is operating near the “zero” crossing of the phase detector. The sources are held in a 90° phase relationship by the use of a second order phase locked loop (PLL) in a feedback path to one of the oscillators. If the system was employed in the phase noise measurement of free running oscillators, the utilization of PLL to maintain lock at the phase detector for a drifting frequency source does not contradict the fact that it is an open loop measurement. Since, however a correction factor is needed while measuring phase noise at offset frequencies less than the PLL bandwidth, care should be taken to use a PLL bandwidth less than that of any offset frequency of interest to increase the validity of the measured performance.

Figure 5-12: Typical block diagram of an HP3048A, phase detector phase noise measurement system

5.3.2 Phase noise measurement setup

The phase detector phase noise measurement technique was utilized to characterize the frequency stability of the designed VCOs. The test setup and the required equipment are shown in Figure 5-13; the HP3048A [34] system provided an automated calibration and data conversion and correction. The high input impedance probe was used to prevent overloading the on-chip output buffer, and to preserve signal integrity at the input of the phase detector. A $0.1\mu\text{F}$ decoupling capacitance was utilized to filter the power supply high frequency noise, and a 2.7nF coupling capacitance was used to prevent the overloading of the high impedance probe by the output signal D.C. offset.

As indicated in the analysis of Section 5.3.1.3, the two frequency sources must maintain a 90° phase relationship by the use of a PLL in a feedback path to one of the oscillators, which must be a tunable voltage controlled oscillator. In the utilized setup, the VCO under test is the one locked in quadrature phase difference to that of the reference VCO, because of its wide tuning range. In the next section the resulting PLL bandwidth will be reported for each tested VCO, since the measurement results are only reliable for offset frequencies larger than that of the PLL bandwidth.

Figure 5-13: Test setup for the VCOs' phase noise measurement

5.3.3 Phase noise measurement results

The phase instability of VCO1, VCO2 and VCO3 is measured by their residual FM single-sideband (SSB) phase noise performance shown in Figure 5-14, graphs a, b and c respectively. The graphs indicate the VCO's phase noise level in dBc/Hz at different offset frequencies.

As indicated in previous subsections, the results are more reliable as an open loop (free running) oscillator measurement for offset frequencies higher than the PLL bandwidth of each measurement setup. The setup PLL bandwidth is a function of the tuning range of each oscillator, the measurement system operation manual [34] contains graphs that assist in the determination of that parameter. The PLL bandwidth was 25 kHz for VCO1 setup, 9 kHz for VCO2 setup, and less than 1 kHz for VCO3 setup. The measured phase noise data at offset frequencies lower than the PLL bandwidth were corrected by the measurement system.

To provide comparable results, the reference oscillator VCO1 and the optimized oscillator VCO2 were tested at the same operating frequency of 720 MHz. The measurement graphs indicate that VCO2 had a 4 dBc/Hz better performance at different offset frequencies. The differential optimized oscillator VCO3 had a lower range of operating frequencies; when tested at 460 MHz, the phase noise measurements were lower than that of VCO2 by 7 dBc/Hz at different offset frequencies. The phase noise at 100 kHz offset from carrier shows that VCO1 had the worst noise level of -84 dBc/Hz, followed by VCO2 at -88 dBc/Hz, while VCO3 had the best noise level at -95 dBc/Hz.

1. Measurement results of VCO1

1. Measurement results of VCO2

1. Measurement results of VCO3

Figure S-14: Measure of single sideband phase noise performance of VCO1, VCO2 and VCO3

5.4 Phase Stability Versus the Selection of Absolute Device Sizes

The frequency domain analysis of Chapter 3 demonstrated that the noise filtering mechanism in the relaxation ring oscillator linear model is linearly dependent on the absolute device sizes of the oscillator circuitry. To measure the effect of selecting the device sizes for any relaxation ring oscillator circuit structure, two new VCOs having exactly the same circuit and device ratios as that of VCO2 were designed on a CUOS3 chip. The first was designed with its smallest NMOS device having the process minimum device size, and the other having its device size three times as that of the first VCO, i.e., one circuit dissipated three times the power and employed three times the silicon area of the other.

The new VCOs were characterized using the test setup as that of Figure 5-1. Both had nearly the same transfer characteristics as that of VCO2, with the power dissipation at the maximum operating frequency for the small device sizes VCO being 6.5 mW, and 19 mW for the other oscillator. The oscillators' phase stability was measured using the test setup of Figure 5-13. The SSB phase noise measurement is shown in Figure 5-15. To provide comparable results, the measurement was performed at the same operating frequency of 689MHz, and the setup PLL bandwidth was 27kHz for both VCOs. It should be noted that the noise floor of the phase noise measurement was different between the two VCOs due to differences in the carrier frequencies' output power levels, which was about 1 dBm for the minimum device sizes VCO and about -3 dBm for the other VCO.

Tripling the absolute device sizes of the oscillator yielded an improvement of phase noise level of about 3 dBc/Hz at different offset frequencies, except for offset frequencies in range of the oscillator's noise floor. It should be noted that this does not correspond to a linear relationship between the noise performance of such oscillators and their absolute device sizes, nor between the noise performance of the VCO and its power dissipation.

a. Phase noise measurement of VCO2 with minimum device sizes

b. Phase noise measurement of VCO2 with three times the minimum device sizes

Figure 5-15: SSB phase noise measurement showing the effect of absolute device sizing on the oscillators' phase stability

5.5 The Effect of Utilizing Special Layout Considerations

Special layout considerations were reported in Chapter 4 to reduce the monolithic oscillator sensitivity to high frequency power supply fluctuations and the noise of adjacent on-chip circuitry.

To test the effect these special layout considerations had on the performance of the

designed VCOs, a test setup was built to induce high frequency noise to the on board regulated power supply, also an effort was directed to induce substrate noise from adjacent on-chip circuitry. The measurements were performed on VCO2 circuit in CUOS2 submission. The following setup conditions were employed:

- Power supply noise was induced by operating other oscillating circuitry (CUOS3 chip) from the same power supply powering VCO2 circuit.
- Substrate noise was induced by powering the other on-chip oscillators (VCO1 and VCO3), which operate at frequencies close to and far from the center frequency of the tested VCO, taking into consideration not powering the output buffers of these other oscillators to prevent any frequency inter-modulation from the chip package output pins.

The power spectral output of VCO2 in this noise induced test setup indicates that there is no change in the center operating frequency, nor in the harmonic content of that VCO's output waveform. In addition, the measurements done to test the phase stability of VCO2 under these conditions were no different than those done under regular operating conditions

5.6 Summary of Measurement Results

Three different VCO circuits designed in two CMOS chips were measured and reported. The VCOs were evaluated in terms of their transfer characteristics, power dissipation, sensitivity to power supply variation and their phase noise performance. A summary of the key parameters of the measurement results is presented in Table 5-2.

Table 5-2: Summary of measurement results

	VCO1	VCO2	VCO3
range of operating frequency [MHz]	290 - 755	625 - 750	420 - 465
power dissipated at the max. operating frequency [mW]	6.3	6.5	11.3
phase noise at 100kHz offset frequency [dBc/Hz]	-84 operating at 720MHz	-88 operating at 720MHz	-95 operating at 460MHz

The effect of the time domain optimization on improving the phase stability of relaxation ring oscillators was evident when comparing the phase performance of VCO1 and VCO2. The effect of employing a complex differential circuit structure on the oscillator's phase stability was clear on the phase noise performance of VCO3 compared to that of the simple ring circuitry of VCO1 and VCO2, with penalty paid in increased power dissipation and employed silicon area and reduced maximum operating frequency.

The transfer characteristics of the optimized oscillators VCO2 and VCO3 indicate that the utilization of the specially designed MOSFET linear voltage controlled resistor improved the VCO transfer characteristics over a limited range of operating frequencies.

Measurements done on designed VCOs having the same circuitry with different absolute device sizes indicate that increasing the device sizes yields an improved phase noise performance though this does not correspond to a linear relationship between the noise performance of a relaxation ring oscillator and its absolute device sizes, nor between the noise performance of the VCO and its power dissipation.

Chapter 6

Conclusion

This thesis presented design alternatives for a monolithic voltage controlled oscillator (VCO). Literature research showed that CMOS relaxation ring oscillators, employing device intrinsic parasitic timing capacitors, were the most suitable and widely used on-chip sub-circuits for high frequency range (hundreds of MHz) and low power oscillator implementation.

A thorough review of the previous work on the analysis of phase noise in relaxation oscillators indicated that a new approach was needed to provide a systematic design methodology for the implementation of low noise relaxation ring oscillators. The new proposed optimization technique was derived from two directions. The first was based on frequency domain analysis using linearized models for the prediction of rms noise voltage present at the switching nodes of a ring oscillator. Part of the research in this thesis focused on the development of suitable linear models for the oscillator circuit MOS device. The second direction was based on an analysis in the time domain to develop an understanding of regenerative switching in ring oscillators. This allowed for the prediction of the output period jitter in the presence of noise. The analysis provided guidelines in the selection of a VCO structure and in sizing the MOS devices for an optimal noise performance. It is important to indicate that some of the frequency and time domain guidelines contradict one another and a compromise is usually needed.

In the text, various voltage controlled oscillator design issues were discussed, including:

- the oscillator phase stability,
- frequency control characteristics,
- sensitivity to power supply fluctuations and noise of adjacent on chip circuitry,
- sensitivity to power supply, temperature and process parameters variations, and
- the ability to preserve the signal integrity at the chip output pad.

Guidelines on circuit design and layout techniques were formulated that help meet these requirements within the limitations of the available technology.

Three different VCO circuits implemented in CMOS 1.2 μ m technology were presented. The structures included a previously reported [20] simple ring oscillator configuration and two new ones whose design provides improved noise performance and linear frequency control characteristics. The VCOs' performance was measured and evaluated in terms of their transfer characteristics, power dissipation, sensitivity to power supply variation, and phase noise levels. The maximum operating frequencies of the two new oscillators are 750 and 460 MHz. The phase noise measured at 100 kHz offset from the carrier equals -88 and -95 dBc/Hz, respectively. These results, combined with the power dissipation of 6.5 and 11.3 mW, indicate that the newly designed oscillators are better in performance than any previously reported VCO design in a comparable technology.

The work described in this thesis can be pursued further in a number of areas:

The proposed timing jitter prediction technique involves routine mathematical manipulations of a large number of extracted simulation parameters, and therefore, cannot be applied on complex circuits with multi-feedback loops and a large number of devices. A simulation program utilizing SPICE analysis tools can be developed to allow for the prediction of jitter for any relaxation type ring oscillator.

Although the optimization techniques applied to ring oscillators for frequency synthesis applications the same optimization methodology can be used in the design of controlled delay elements in the implementation of a digital sampler for data recovery applications, since the sampler has to be designed using cells of minimal delay and lowest possible jitter which is the same design requirement for a multi-stage ring oscillator.

The results demonstrated in this thesis indicate that by using submicron CMOS technology, good quality low noise oscillators (previously achievable only by LC tank bipolar circuits), that reach gigaHertz frequency range, can be built. That implementation could be integrated in a monolithic CMOS frequency synthesizer, towards the design of a low power and low cost radio front end for personal communications devices.

The accuracy of SPICE small signal analysis models for high frequency simulations needs to be examined. Furthermore, the utilization of a harmonic balance simulator in characterizing the performance of relaxation ring oscillators deserves further investigation.

Appendix A

CMOS4S Process Parameters

This section contains information regarding the mask layers, simulation and electrical parameters for Northern Telecom Electronics CMOS4s, a 1.2 micron, double-ploysilicon, double-metal, N-well process. The material that appears in this section is extracted from report IC90-01, "Design Rules and Process parameters for the Northern Telecom CMOS4S process," provided by the Canadian Microelectronics Corporation.

A.1 CMOS4S mask layers

Table A-1: CMOS4S mask layers

Mask Level	Name	Function
05	N-Well	Defines n-wells.
10	Device Well	Defines active regions. All other regions will be covered by field oxide.
15	P-Guard Exclusion	Implant mask to increase p-substrate surface doping under field oxide. Exclusion mask to be drawn around n-well.
20	Polysilicon	Defines polysilicon lines and transistor gates.
27	Capacitor Polysilicon	Defines top poly plates to form poly-to-poly capacitors (optional).
30	N+ Doping Exclusion	Defines areas not to be doped n+. Substrate doping will occur only in device wells.
35	P+ Doping	Defines areas to be doped p+. Substrate doping will occur only in device wells.
40	Contact Window	Defines contact areas from metal 1 to polysilicon or diffusion.
50	Metal 1	Defines first level metal lines.
60	Via 1	Defines contact areas from metal 2 to metal 1.
70	Metal 2	Defines second level metal lines.
95	Passivation Windows	Defines openings in passivation layer for bonding pads.

Figure A-1: CMOS4S layer legend

A.2 SPICE level 3 Parameters

- Nominal conditions.
- All resistances (RS and RD) are for 20 micron wide devices.

Table A-2: CMOS4S SPICE level 3 parameters

Parameter	NMOS	PMOS	Units
Level	3	3	-
UO	566.3	200.8	cm ² /Vs
VTO	0.7572	-0.8307	V
NFS	5.76E+11	5.864E11	1/cm ²
TPG	1.000	1.000	-
TOX	2.502E-08	2.502E-08	m
NSUB	1.400E+16	2.011E+16	1/cm ³
VMAX	1.651E+05	2.823E+05	m/s
RS	26.77	58.90	ohm
RD	26.77	58.90	ohm
XJ	1.165E-07	1.742E-07	m
LD	1.157E-07	1.364E-07	m
DELTA	0.3551	0.4598	-
THETA	6.574E-02	0.1376	1/V
ETA	9.814E-02	6.729E-02	-
KAPPA	2.000E-17	7.487	-
PB	0.800	0.800	V
IS	1.000E-16	1.000E-16	A
JS	1.000E-04	1.000E-04	A/m ²
CJ	2.900E-04	4.100E-04	F/m ²

Table A-2: CMOS4S SPICE level 3 parameters

Parameter	NMOS	PMOS	Units
MJ	0.486	0.540	-
CJSW	3.300E-10	3.400E-10	F/m
MJSW	0.330	0.300	-
CGSO	1.973E-10	3.284E-10	F/m
CGDO	1.973E-10	3.284E-10	F/m
FC	0.500	0.500	-

A.3 Other Electrical Parameters

Table A-3: CMOS4S electrical parameters - resistance

Resistance	ohms/sq.
N+ Diffusion	45
P+ Diffusion	100
N+ Poly	30
P+ Poly	30
N- well	1.8K (geometry and voltage dependent)
Metal 1	0.050
Metal 2	0.025
Metal 1- Diffusion Contacts	20 ohms (1.2 X 1.2 microns)
Metal 1 - Poly contacts	10 ohms (1.2 X 1.2 microns)
Metal 1 - Metal 2 Via	0.120 ohms (1.6 X 1.6 microns)

Table A-4: CMOS4S electrical parameters - capacitance

Capacitance	Area Component (pF/ μm^2)	Edge Component (pF/ μm)
Metal 1 - Field	2.9E-05	5.00E-05
Metal 2 - Poly	6.0E-05	-
Metal 1 - Diffusion	5.5E-05	-
Poly - Field	6.4E-05	2.20E-05
Metal 2 - Field	1.6E-05	4.63E-05
Metal 2 - Poly	2.5E-05	-
Metal 2 - Metal 1	2.0E-05	-
Metal 1 - Field	5.2E-05	-
Capacitor Poly to Poly	7.76E-04	1.06E-04

Appendix B

Physical Design: Circuit layout and device sizes

This section contains detailed information regarding the implemented VCO circuit layout and device sizes. The layout of the VCO's chips, CUOS2 and CUOS3, are also included.

Dimensions of the layout are as specified in Design Scale Microns (DSM), though the design is scaled down by a factor of 80% in actual implementation. The device sizes shown on the circuit schematic diagrams correspond to the device width in microns, with all devices employed in the design having the minimum device length of 1.2 μ m.

Figure B-1: The layout of VCO1, reference oscillator

Figure B-2: VCO1 device sizes

Figure B-3: The layout of VCO2, optimized oscillator

Figure B-4: VCO2 device sizes

Figure B-5: The layout of VCO3, differential optimized oscillator

Figure B-6: VCO3 device sizes

Figure B-7: Layout of the CUOS2 chip

Figure B-8: Layout of the CUOS3 chip

References

- [1] J.R. Long, M.A. Copeland et al., "A low voltage silicon bipolar RF front-end for PCN receiver applications," Digest of Technical Papers, ISSC, San Francisco, CA, 1995.
- [2] N. M. Nguyen, R. G. Meyer, "Si IC-Compatible Inductors and LC Passive Filters," IEEE Journal of Solid-State Circuits, Aug. 1990.
- [3] N. M. Nguyen, R. G. Meyer, "A 1.8-GHz Monolithic LC Voltage-Controlled Oscillator," IEEE Journal of Solid-State Circuits, vol. 27, No. 3, March 1992.
- [4] Y. Yamauchi et al., "A 15-GHz Monolithic Low-Phase-Noise VCO Using AlGaAs/GaAs HBT," IEEE Journal of Solid-State Circuits, vol. 27, No. 10, Oct. 1992.
- [5] Nan-Lei and Wu-Jing Ho, "X-Band HBT VCO with High-Efficiency CB Buffer Amplifier," IEEE Journal of Solid-State Circuits, vol. 27, No. 10, Oct. 1992.
- [6] M. Steyaert, J. Craninckx, "A 1.1 GHz Oscillator Using Bondwire Inductance," Electronics Letters, Feb. 3, 1994.
- [7] K. Negus, et al., "A Highly Integrated Transmitter IC with Monolithic Narrowband Tuning for Digital Cellular Handsets," Digest of Technical Papers, 1993 International Solid-State Circuits Conf., San Francisco, CA, Feb. 1994.
- [8] George D. Vendelin, "Microwave Circuit Design Using Linear and Nonlinear Techniques," Wiley, New York, 1990.
- [9] Benjamin Parzen, "Design of Crystal and Other Harmonic Oscillators," Wiley, Toronto, 1983.
- [10] J. Rutman, "Characterization of Phase and Frequency Instabilities in Precision Frequency Sources: Fifteen years of progress," Proc. IEEE, vol. 66, pp. 1048-1075, Sept. 1978.
- [11] P. Grivet and A. Blaquiere, "Nonlinear Effects of Noise in Electronic Precision Clocks," Proc. IEEE, vol. 51, pp. 1606-1614, Nov. 1963.

- [12] R.L. Geiger, P.E. Allen, N.R. Strader, "VLSI Design Techniques for Analog and Digital Circuits," McGraw-Hill, NY, 1990.
- [13] A. A. Abidi, T.G. Meyer, "Noise in Relaxation Oscillators," IEEE J. Solid-State Circuits, vol. SC-18, pp. 794-802, Dec. 1983.
- [14] T. C. Weignandt, B. Kim, P. R. Gray, "Analysis of Timing Jitter in CMOS Ring Oscillators," Proceedings of the ISCAS, 1994.
- [15] J. McNeil, "Jitter in Ring Oscillators," Proceedings of the ISCAS, 1994.
- [16] B. Razavi, "Analysis Modeling, and Simulation of Phase Noise in Monolithic Voltage-Controlled Oscillators," IEEE Custom Integrated Circuits Conf. Proceedings, 1995.
- [17] HSPICE User's Manual, Meta-Software Inc.
- [18] Macallan Consulting, User's manual, "Nodal Circuit Design Software," CA, 1992.
- [19] D.H. Wolaver, "Phase-Locked Loop Circuit Design," Prentice Hall, NJ, 1991.
- [20] M. Thamsirianunt and T.A. Kwasniewski, "A 1.2 μ m CMOS Implementation a Low-Power 900-MHz Mobile Radio Frequency Synthesizer," IEEE Custom ICs Conf. Proceeding, 1994.
- [21] P.R. Gray and R.G. Meyer, "Analysis and Design of Analog Integrated Circuits", John Wiley & Sons, NY, 1984.
- [22] I.A. Young, J.K. Greason, K.L. Wong, "A PLL clock generator with 5 to 110 MHz of lock range for microprocessors," IEEE J. Solid State Circuits, vol. 27, pp. 1599-1606, Nov. 1992.
- [23] T. Kwasniewski, M. Abou-Seido, A.J. Bergsma, "Towards an all CMOS Digital Radio," Calgary Wireless Conf. Proceedings, 1995.
- [24] P. Gray and R. Meyer, "Future Direction in Silicon ICs for RF Personal Communications," IEEE Custom Integrated Circuits Conf. Proceedings, 1995.
- [25] J. Min, A. Rofougaran, H. Samueli and A. A. Abidi, "An All-CMOS Architecture for a Low-Power Frequency-Hopped 900 MHz Spread Spectrum Transceiver," IEEE Custom Integrated Circuits Conf. Proceedings, 1994.
- [26] K.M. Ware, H. Lee, C.G. Sodini, "A 200 MHz CMOS Phase-Locked Loop With a Dual Phase Detector," IEEE J. Solid State Circuits, vol. 24, pp. 1560-1568, Dec. 1989.

- [27] Deog-Kyoon Jeong, Gaetano Borriello, David A. Hodges, and Randy H. Katz, "Design of PLL-Based Clock Generation Circuits," *IEEE Journal of Solid-State Circuits*, April 1987.
- [28] M. Banu and A.E. Dunlop, "Clock Recovery Circuits with Instantaneous Locking," *Electronics Letters*, Vol. 28, No 23, Nov. 1992.
- [29] Benny Lai and Richard C. Walker, "A Monolithic 622Mb/s Clock Extraction Data Retiming Circuit," *IEEE International Solid-State Circuits Conf. Proceedings*, 1991.
- [30] F. M. Gardner, "Phaselock Techniques", John Wiley & Sons, NY, 1979.
- [31] R. E. Sentz and R. A. Bartkowiak, "Feedback Amplifiers and Oscillators", Holt Rinehart and Winston Inc., NY, 1968.
- [32] Hewlett-Packard, Seminar notes, "RF & Phase Noise Measurement Seminar", 1988.
- [33] Hewlett Packard, User's Manual, "HP 8590 Series Spectrum Analyzer", 1990.
- [34] Hewlett-Packard, User's Manual, "HP 3048A Phase Noise Measurement System", 1989.
- [35] Neil H.E. Weste, Kamran Eshraghian, "Principles of CMOS VLSI design", second edition, Adison Wesley, USA, 1992
- [36] James A. Crawford, " Frequency Synthesizer Design Handbook", Artech House, Boston, 1994.
- [37] B. Kim, D. Helman and P. Gray, "A 30-MHz Hybrid Analog/Digital Clock Recovery Circuit in 2- μ m CMOS", *IEEE J. Solid State Circuits*, vol. 25, pp. 1385-1394, Dec. 1990.
- [38] AT&T Microelectronics, Technical Note, "Understanding Timing Recovery and Jitter in Digital Transmission Systems," May 1993.
- [39] Hewlett-Packard, Application Note 360, "Jitter Tolerance Testing using External Phase or Frequency Modulated Sources and Bit Error Rate Test Sets".
- [40] Dan H. Wolaver, "Measurement of Jitter with a Spectrum Analyzer", *Microwave Logic*, Jan. 1994.
- [41] J. Millman and A. Grabel, "Microelectornics," McGraw-Hill, NY, 1988.
- [42] Adel S. Sedra, Kenneth C. Smith, "Microelectornics Circuits," Holt, Rinehart and Winston, NY, 1987.

- [43] Y. Tsividis, M. Banu and J. Khoury, "Continuous-Time MOSFET-C Filters in VLSI," IEEE Transactions of Circuits and Systems, vol. CAS-33, No. 2, Feb. 1986.
- [44] Matthew K. Maguire, "The Design of a High-Frequency Voltage-Controlled Oscillator in BiCMOS Using On-Chip Inductors," M. Eng. Thesis, Carleton University, Ottawa, Canada, 1995.
- [45] Manop Thamsirianunt, "The Design & Implementation of CMOS Components for Gigahertz Frequency Synthesizer," M. Eng. Thesis, Carleton University, Ottawa, Canada, 1993.
- [46] Laszlo Dobos and Brent Jensen, "A Versatile Monolithic 800kHz to 800MHz Phase-Startable Oscillator," IEEE Custom Integrated Circuits Conf. Proceedings, 1994.
- [47] Sam Yinshang Sun, "A High Speed High Jitter Tolerant Clock and Data Recovery Circuit Using Crystal Based Dual PLL," IEEE Bipolar and Technology Meeting, 1991.
- [48] C. J. M. Verhoeven, "A High-Frequency Electronically Tunable Quadrature Oscillator," IEEE J. Solid State Circuits, vol. 27, No. 7, pp. 1097-1100, July 1992.
- [49] M. Soyuer and J. D. Warnock, "Multigigahertz Voltage-Controlled Oscillators in Advanced Silicon Bipolar Technology," IEEE J. Solid State Circuits, vol. 27, No. 4, pp. 668-670, April 1992.
- [50] B. Razavi and J. J. Sung, "A 6 GHz 60mW BiCMOS Phase-Locked Loop," IEEE J. Solid State Circuits, vol. 29, no. 12, pp. 1560-1565, Dec. 1994,
- [51] K. Kurita, T. Hotta, T. Nakano and N. Kitamura, "PLL-Based BiCMOS On-Chip Clock Generator for Very High-Speed Microprocessors", IEEE J. Solid State Circuits, vol. 26, No. 4, pp. 585-589, April 1991.
- [52] A. W. Buchwald et al., "A 6GHz Integrated Phase-Locked Loop Using AlGaAs/GaAs Hetrojunction Bipolar Transistors," IEEE J. Solid State Circuits, vol. 27, No. 12, pp. 1752-1762, Dec. 1992.
- [53] S. K. Enam and A. Abidi, "NMOS IC's for Clock and Data Regeneration in Gigabit-per-Second Optical-Fiber Receivers," IEEE J. Solid State Circuits, vol. 27, No. 12, pp. 1763-1774, Dec. 1992.

- [54] Mihai Banu, "MOS Oscillator with Multi-Decade Tuning Range and Gigahertz Maximum Speed," *IEEE J. Solid State Circuits*, vol. 23, No. 6, pp. 1386-1393, Dec. 1988.
- [55] M. Thamsirianunt and T.A. Kwasniewski, "CMOS VCOs for PLL Frequency Synthesis in GHz Digital Mobile Radio Communications," *IEEE Custom Integrated Circuits Conf. Proceedings*, 1995.
- [56] M. P. Flynn and S. U. Lidholm, "A 1.2mm CMOS Current-Controlled Oscillator," *IEEE J. Solid State Circuits*, vol. 27, No. 7, pp. 982-987, July 1992.
- [57] S. K. Enam and A. Abidi, "A 300-MHz CMOS Voltage Controlled Ring Oscillator," *IEEE J. Solid State Circuits*, vol. 25, No. 1, pp. 312-315, Feb. 1990.

Bibliography

- 1 T. Kwasniewski, M. Abou-Seido, A. Bouchet, F. Gaussorgues, J. Zimmerman, "Inductor-less Oscillator Design for Personal Communication Devices - A 1.2 μ m CMOS Process Case Study," IEEE Custom Integrated Circuits Conference, 1995.
- 2 J. A. Crawford, "Frequency Synthesizer Design Handbook," Artech House, Boston, USA, 1994.
- 3 B. Nauta, "Analog CMOS Filters for Very High Frequencies," Kluwer Academic Publisher, Massachusetts, USA, 1993.
- 4 W. H. Hayt, J. E. Kemmerly, "Engineering Circuit Analysis," fourth edition, McGraw-Hill, NY, 1986.
- 5 A. R. Alvarez, "BiCMOS Technology and Applications," Kluwer Academic Publisher, MA, USA, 1989.
- 6 G.F. Franklin, J. D. Powell, A. Emami-Naeini, "Feedback Control of Dynamic Systems," Addison Wesley, USA, 1986.
- 7 J. Shyu, G. C. Temes, F. Krummenacher, "Random Error Effects in Matched MOS Capacitors and Current Sources," IEEE Journal of Solid-State Circuits, vol. SC-19, No. 6, Dec. 1984.
- 8 Aurelie Bouchet, Fabien Gaussorgues, "Design and Design Methodology of CMOS Ring Oscillators," Carleton University research report, 1994.
- 9 M. Banu, "Design of High-Speed, Wide-Band MOS Oscillators for Monolithic Phase-Locked Loop Applications," Proceedings of the ISCAS, 1988.
- 10 M. P. Flynn, S. U. Lidholm, "A 1.2- μ m CMOS Current-Controlled Oscillator," IEEE Journal of Solid-State Circuits, vol. 27, No. 7, pp. 982-987, July 1992.
- 11 J. McNeil, "A 150 mW, 155 MHz Phase Locked Loop with Low Jitter VCO," Proceedings of the International Symposium for Circuits and Systems, 1994.

- 12 T. S. Cheung, H. Wong, Y.C. Cheng, "250 MHz Relaxation Oscillator with Enhanced Linear Voltage-Frequency Characteristic and Temperature Stability," *Electronics Letters*, vol. 28, No. 20, Sept. 24, 1992.
- 13 M. H. Wakayama, A. A. Abidi, "A 30-MHz Low-Jitter High-Linearity CMOS Voltage-Controlled Oscillator," *IEEE Journal of Solid-State Circuits*, vol. sc-22, No. 6, pp. 1074-181, Dec. 1987.

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