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Full Name of Author — Nom complet de l'auteur

James Douglas Kendall

Date of Birth — Date de naissance

April 15, 1959

Country of Birth — Lieu de naissance

U.S.A.

Permanent Address — Résidence fixe

2201 Riverside Dr. Apt. 515
Ottawa, Ontario
K1H 8K9

Title of Thesis — Titre de la thèse

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Name of Supervisor — Nom du directeur de thèse

Dr. A.R. Boothroyd

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James D. Kendall

A PUNCHTHROUGH CURRENT MODEL FOR
SHORT-CHANNEL MOSFETs

by

© James D. Kendall B. Eng.

A thesis submitted to the Faculty of Graduate
Studies and Research in partial fulfillment
of the requirements for the degree of

Master of Engineering

Department of Electronics
Faculty of Engineering
Carleton University
Ottawa, Canada
August 1983

The undersigned recommend to the Faculty of Graduate Studies and Research
the acceptance of the thesis:

"A Punchthrough Current Model For Short-Channel MOSFETs"

submitted by James D. Kendall in partial fulfillment of the requirements
for the degree of Master of Engineering.

Prof. A.R. Boothroyd
Thesis Supervisor

Prof. A.R. Boothroyd
Chairman
Department of Electronics

August, 1983

ABSTRACT

In this thesis, a model is presented which may be used to simulate punchthrough current in uniform and non-uniform substrate short-channel MOSFETs. This model is used to create a simulator which is both accurate enough and fast enough to be used for the computer-aided design of MOSFET circuits. In fact, this simulator is approximately 50,000 times faster than the best existing simulator. The model is derived by first solving Poisson's equation and the current continuity equation for a one-dimensional punchthrough geometry. This solution is then applied to the two-dimensional MOSFET geometry with the aid of a scale factor and a fitting parameter. Finally, measured and simulated results are compared, and it is pointed out how the model may be used in device development.

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LIST OF SYMBOLS

a	quadratic equation solution parameter
b	quadratic equation solution parameter
c	quadratic equation solution parameter
C_B	bulk doping concentration
C_I	maximum bulk implant doping concentration
C_S	maximum surface implant doping concentration
E	electric field
E_{Fn}	quasi-Fermi level for electrons
E_{max}	maximum electric field
I_D	drain current
I_{PT}	punchthrough current
J_n	electron current density
J_{PT}	punchthrough current density
k	Boltzmann's constant
l	lateral strip length
l'	lateral strip length for which the potential minimum is zero
l_s	lateral strip length at depth s
L_c	channel length
L_{cmea}	measured channel length
L_{csim}	simulated channel length
L_g	gate length
M	variable which is proportional to the substrate doping
n	electron density
n_i	intrinsic carrier density
N	number of points in the finite difference analysis
N_B	bulk doping concentration

N_C	density of carriers in the punchthrough current
N_S	doping concentration at the surface of the source and drain
N_T	space charge number density
q	electron charge
r	radius in a polar coordinate system
r_j	radius of curvature of the drain and source underdiffusions
R_d	radius of the drain underdiffusion depletion region edge
R_{dmax}	maximum value of R_d allowed by the model
R_{ds}	value of R_d when $s = r_j$
R_s	radius of the source underdiffusion depletion region edge
s	depth of the depletion region intersection point
$SD(x)$	substrate doping as a function of depth
T	temperature
u	substitutional variable
v	velocity
v_s	scatter-limited velocity
V_a	applied voltage
V_{BS}	substrate bias
V_{DS}	drain voltage
V_{DSS}	drain voltage when $s = r_j$
V_{GS}	gate voltage
W	gate width
x	depth into the silicon
x_M	mean of the bulk implant distribution
y	lateral distance from point 0
y_M	position of the potential minimum
α	straggle parameter for the surface implant
β	straggle parameter for the bulk implant

- ΔZ boundary condition matching parameter
- ΔZ_s value of ΔZ for $s = r_j$
- Δx lateral strip width
- ϵ dielectric constant of silicon times the permittivity of free space
- ϕ electric potential
- ϕ_B built-in potential of a pn junction
- ϕ_{BL} potential barrier lowering

CHAPTER 1

INTRODUCTION

The maximum drain to source voltage that can be applied to a MOSFET, and still have it operate as a transistor, is limited by one of two mechanisms. For conventional long-channel devices, the drain voltage is limited by avalanche breakdown. This current flow mechanism involves high electric fields near the drain that cause carrier generation by impact ionization and produce a current that flows from the drain into the neutral substrate. In the future, the short-channel devices that will be required for very large-scale integration are likely to be limited by a second current conduction mechanism called "punchthrough". In this mechanism, the drain and source depletion regions meet in the bulk underneath the channel. See Figure 1.1 for an illustration of the depletion layer configuration for this situation. The electric field due to the drain lowers the potential barrier near the source, and this causes current injection from the source into the depleted region. The injected current is then swept by high electric fields to the drain.

The I_D vs V_{DS} characteristics for an n-channel MOSFET, for which punchthrough occurs, can be seen in Figure 1.2. Punchthrough begins to occur when the $V_{GS} = 0$ characteristic starts to bend upward from the V_{DS} axis. This phenomenon is of fundamental importance since it means that for a drain voltage above 1 V, this device cannot be turned off by applying a zero or negative gate voltage. For drain voltages in this range the MOSFET will no longer act as a switching element. Thus the maximum drain voltage

Figure 1.1 The Depletion Layer Configuration in Punchthrough

Figure 1.2 MOSFET Characteristics in Punchthrough for $v_{GS} = 0$ to 5V

is limited for a digital circuit which uses these devices. This can be a very severe design restriction.

This leads us to the purpose of this thesis which is to develop a mathematical model for punchthrough current in short-channel MOSFETs. The model is intended to be used in computer-aided circuit design so that the designer will know what the magnitude of the punchthrough current is for a given device and set of voltage conditions. This application makes two basic demands on the computer simulation. The first is that the simulation must be fast because a circuit designer may require the evaluation of hundreds of bias points for tens or hundreds of transistors, with a turnaround time of several minutes. Therefore the simulation must be able to calculate the punchthrough current for a given set of bias conditions in a fraction of a CPU second. This requires a simple simulation with a minimum of calculations. The second demand is that the simulation must give reliable results over a wide range of bias conditions and device parameters. The relevant device parameters which may be varied are: channel length, substrate doping, which may be uniform or non-uniform, and drain and source junction depth and profile. The simulation must also operate for n and p-channel devices.

These demands are not of a trivial nature because punchthrough is a two-dimensional, high level phenomenon, which does not easily lend itself to the type of simple analysis required for computer-aided design simulations. A complete solution of the problem requires a simultaneous solution of Poisson's equation and the current continuity equation in two dimensions, for the complicated geometry and boundary conditions of the MOSFET. This cannot be done analytically, but it can be done approximately by two-dimensional, finite difference analysis.

The two-dimensional, finite difference simulations [1-7] fall into two categories: those that solve only Poisson's equation, and those that simultaneously solve Poisson's equation and the current continuity equation. The former type [1,2,7] do not take into account the dependence of the electric potential on the mobile charge distribution, and are restricted to the simulation of low levels of current flow. But simple calculations show that in punchthrough the current commonly has high enough carrier densities for the mobile charge to have a major effect on the potential. Thus such simulations are not useful for application in the present work. Another objection to using these simulations is that they require several minutes of mainframe CPU time per bias point, which is too long for computer-aided design use.

The second type of two-dimensional simulation [3-6] takes into account the coupling between potential and current. This involves additional calculations, which means that the second type of simulation requires even more CPU time than did the first type of simulation. Thus these simulations are also unsuitable for the present work.

Given this situation, a simpler, more approximate analytic approach must be sought. The only published work along these lines is by G.W. Taylor [8]. He presents a punchthrough current model which uses the conventional channel current equations with the threshold voltage and saturation voltage modified. This model is not useful for computer-aided design for reasons that will be discussed in Chapter 2.

A punchthrough simulation for use in computer-aided design must be fast, and it must be versatile enough to deal with a wide range of bias conditions and device parameters. None of the existing punchthrough models satisfy both of these requirements. The first step in deriving an acceptable model is to clearly define what is meant by "punchthrough current" so

that one knows what to simulate. The next step is to gain physical intuition about the phenomenon by reviewing the published literature on the subject, and observing how devices actually behave. These preliminaries are dealt with in Chapter 2 of this thesis.

With the physical intuition garnered from the literature and from device measurements, a punchthrough current model suitable for computer-aided design is derived in Chapter 3. This model is flexible enough to simulate a variety of devices under all relevant bias conditions. The simplifications used in its derivation are also explained and justified in this chapter.

In Chapter 4 the computer implementations of the model, for the simulation of uniform and non-uniform substrate devices, are presented. The algorithms employed in these programs are described in detail. The usefulness of the programs is verified by the comparison of measured and simulated results in Chapter 5. It is also shown that they may be used as a first-order approximation for device development. The thesis closes with Chapter 6 which presents a summary and outlines areas for further research.

CHAPTER 2

THE PHYSICAL NATURE OF PUNCHTHROUGH CURRENT

2.1 A Rigorous Definition of the Punchthrough Current Mechanism

A number of models exist which are able to simulate punchthrough currents in some restricted regime. Even though none of them is satisfactory for use in computer-aided design, their examination yields physical insights which can be used to construct a model which is satisfactory for this purpose. But before one undergoes such an examination, it is advantageous to define the MOSFET punchthrough current mechanism. This is necessary because a clearly stated, unambiguous definition of this mechanism has not been presented in the literature.

In order to construct a definition of the punchthrough current mechanism, let us begin by referring to Figure 2.1.1. This figure shows the geometry of an n-channel MOSFET operating in punchthrough. It can be imagined that this state was established by having the source and substrate grounded with an arbitrary voltage on the gate, and then the voltage on the drain was increased from zero. This caused the depletion region of the reverse biased drain-substrate junction to be extended until it touched and then overlapped the source depletion region.

Let us define the substrate to be at zero potential and assume zero substrate bias. Then the source region will be at the built-in potential ϕ_B and the drain will be at a potential $\phi_B + V_{DS}$. If the drain and source depletion regions overlap as shown in Figure 2.1.1, then there is insufficient depleted material to allow the potential distribution to go to zero

Figure 2.1.1 The MOSFET Punchthrough Geometry

at any point in the overlapped region. Thus it is clear that the potential minimum on a horizontal line from the drain to the source in this region will be greater than zero. In fact, since this will be true for any horizontal line between the source and the drain in the overlapped depletion region, there will be a potential minimum locus extending from the bottom of the inversion layer down to the point which we shall call the "depletion region intersection point". (See Figure 2.1.1.) This is the point at which the drain and source depletion region edges intersect. The depletion region intersection point is the potential minimum on a horizontal line which passes through it. This is because the potential at this point is zero since it lies on the edge of the drain and source depletion regions, and the potential at every other point on the horizontal line must be higher. The depletion region intersection point is an important point because it fixes the position of one end of the potential minimum locus.

If a potential minimum near the source is greater than zero, then the potential barrier has been lowered. In punchthrough, barrier lowering occurs at all points along the potential minimum locus. This implies that current is injected across the potential minimum locus from the bottom of the inversion layer down to the depletion region intersection point.

The potential maximum on the potential minimum locus is called a "saddle point" because of its appearance on a plot of potential in two dimensions. Since the injected current density is exponentially dependent upon the barrier lowering, the greatest injection will occur at the saddle point.

The potential maximum on the potential minimum locus may appear at the surface or in the bulk, depending upon the operating conditions and structure of the device. Troutman [9] calls these two conditions surface punchthrough and bulk punchthrough, respectively. This terminology would imply

that different physical mechanisms are operating in the two cases, but one can see from the preceding explanation that it is the same physical mechanism. Thus it seems more reasonable to speak of punchthrough as one unified phenomenon and refer to it only by that name. Hence, Troutman's terminology will not be used in this thesis.

In the analysis of the current flow in any device, the currents are divided into two classes. A current whose carrier density is significantly less than the doping level of the neighbouring material is referred to as being a "low level current". If the carrier density is approximately equal to or greater than the doping level, then the current is referred to as a "high level current". The major difference between the two regimes is that for low level currents the space charge is mainly determined by the ionized dopant density. Thus one can, to a good approximation, neglect the coupling between Poisson's equation and the current continuity equation when solving for the electric potential. For high level conditions the space charge in the region of the current flow is mainly due to the current, so the coupling between Poisson's equation and the current continuity equation must be accounted for when solving for the electric potential.

It is important to know whether punchthrough current is at low level or high level if one is trying to model this phenomenon. When barrier lowering has just begun, the punchthrough current increases from a value of zero. Thus the punchthrough current must be low level up to a certain value of barrier lowering. The question that arises is: Do devices of interest commonly have enough barrier lowering to produce high level punchthrough? This question can be answered by examining the drain characteristics of a particular device.

The device, whose characteristics are shown in Figure 2.1.2, is a p-channel MOSFET with a uniform substrate doping of 10^{15} cm^{-3} . Its source

Figure 2.1.2 Characteristics for a P-channel MOSFET in Punchthrough for $V_{GS}=0$ to $-5V$

and drain junction depths are $.63 \mu\text{m}$, its channel length is $1.5 \mu\text{m}$, and it is $50 \mu\text{m}$ wide. The $V_{GS} = 0$ characteristic shows that the device begins to punchthrough at approximately $V_{DS} = -1 \text{ V}$. The drain current at $V_{DS} = -10 \text{ V}$ is -2.35 mA . If it is assumed that this current flows uniformly from the surface down to the junction depth at scatter limited velocity, then an estimate can be obtained of the charge density in the current. These assumptions tend to reduce the high level effects because non-uniformities in the current flow and lower carrier velocities will produce higher carrier densities. The figures given above yield a current density of $7.46 \times 10^3 \text{ A/cm}^2$, and assuming that the carriers move at the hole scatter limited velocity of $6 \times 10^6 \text{ cm/s}$, the carrier density in the current is $7.76 \times 10^{15} \text{ cm}^{-3}$. This is approximately a factor of eight greater than the substrate doping and, in reality, higher carrier concentrations would surely be observed. This calculation demonstrates that for a typical device with typical applied voltages, the punchthrough current is at high level. In fact, it is to be expected that this would be the case over most of the $V_{GS} = 0$ drain characteristic shown for the device cited. It must be concluded that punchthrough is basically a high level phenomenon and any punchthrough model must take this into account.

In view of the preceding discussion, the punchthrough mechanism can be defined as follows:

In a short channel MOSFET, the drain and source depletion regions meet and overlap in the bulk region underneath the channel. The potential minima near the source are raised due to the influence of the drain potential, and this causes carrier injection into the depleted region from the source. There is a potential minimum locus created that extends from the bottom of the inversion layer down to the depletion region intersection point. Injection occurs across the entire length

of this locus. The greatest injection occurs at the maximum on the potential minimum locus which is called the saddle point. This point may occur at the surface or in the bulk, depending upon the conditions. Once the carriers have been injected across the potential minimum locus, they are swept to the drain by the high fields that are present in the depletion region. The current flow is at low level if the density of the carriers is much less than that of the substrate doping, and at high level if the density is approximately equal to or higher. Most of the currents of interest for computer-aided design are high level.

Now that this definition has been established, we will use it to examine the punchthrough models that have been published in the literature. This definition will also be used in Chapter 3 as a basis for the development of a punchthrough model for computer-aided design.

2.2 Elementary Models

There are a number of published models that simulate punchthrough current. Although none of these models is adequate for computer-aided design use, a study of them provides some insights that will be useful in constructing a satisfactory model.

The simplest of these models is a conceptual model described by Troutman [9]. This is intended to be used in conjunction with a two-dimensional, finite difference simulation to provide conceptual guidance. The model abstracts the MOSFET geometry so that the drain and source become a dipole, the gate remains a fixed conducting plane, and the substrate becomes a movable conducting plane, as can be seen in Figure 2.2.1. This model is intended to provide a qualitative understanding of the electric field line

Figure 2.2.1 Troutman's [9] Conceptual Punchthrough Model

configuration in a MOSFET which is undergoing punchthrough. It is useful in that it provides an idea of how the drain to source coupling occurs. It does not, however, give any quantitative information about the potential minima that are responsible for carrier injection. Its value for proving that there is drain to source coupling is also questionable because, as was explained in Section 2.1, as soon as the drain and source depletion regions overlap, it is obvious that drain to source coupling occurs.

The most accurate part of the model is the induction of image charges on the gate, because it is clear from electrostatic principles that this must occur. Troutman states that when the gate is closer to the dipole, more field lines will be coupled to it, and fewer field lines will be coupled from the drain to the source. Thus the potential minima will generally be lower, and less injection will occur. This is a valuable insight into the solution of Poisson's equation and the current continuity equation for this complex geometry. Unfortunately, this is not a universal principle because Troutman later states that in some circumstances a decrease in gate oxide thickness decreases drain current, while in other cases it increases the drain current. This is explained as being due to the fact that a decrease in oxide thickness raises the surface potential for a given gate voltage, and this increases the channel current. This effect is sometimes more important than the reduction of drain to source coupling. Thus the gate coupling part of Troutman's conceptual model is only applicable in some instances.

The "movable" conducting plane that represents the substrate in Troutman's conceptual model seems much less defensible than the conducting plane representing the gate. The source and drain do not produce image charges in the substrate and the substrate does not look like a conducting plane. Troutman says that increasing the substrate doping is tantamount to moving

the conducting plane closer to the dipole. When the substrate doping is increased, the widths of the depletion regions decrease, which decreases the overlap region, and hence the injected current. This is not at all similar to moving a conducting plane closer to the source and drain. The movable conducting plane which represents the substrate appears to be the weakest part of Troutman's conceptual model. It is concluded that this approach is of questionable value even for the development of insights, and provides little basis for qualitative modelling.

The only analytic punchthrough model that has been published to date was proposed by Taylor [8]. The model employs the conventional channel current equations, but the threshold voltage and saturation voltage are modified to allow the model to be used under punchthrough conditions. Reasonable agreement was obtained between measured and simulated results for low level punchthrough.

The basic problem with this approach is that the channel current equations are not representative of punchthrough, hence the model is non-physical. This means that the approach is essentially empirical, and fitting parameters have to be used to fit the model to each new device which is considered. Other problems are that the model cannot simulate high level punchthrough current, and it is restricted to uniform substrate devices. A punchthrough model for computer-aided design should be physically based with a minimum of fitting parameters, and should simulate high level punchthrough currents for both uniform and non-uniform substrate devices. Since Taylor's model does not meet these specifications, it is not useful for computer-aided design and is not considered further.

2.3 Models That Solve Only Poisson's Equation

The two models that have been considered so far are too simplistic to be of significant value. Punchthrough is a complicated phenomenon which can only be modelled completely by a simultaneous solution of Poisson's equation and the current continuity equation for the complicated MOSFET geometry. This problem does not have an analytic solution, but it can be solved by a two-dimensional analysis of the finite difference or finite element type. Finite difference analysis involves the solution of the desired partial differential equations in finite difference form at a fixed number of points on a grid, which may be uniform or non-uniform. Finite element analysis involves approximating the potential, carrier concentration and other distributions, as a series of polynomials whose coefficients must be solved for. Only the finite difference method will be considered here because all the published numerical punchthrough models use this type of analysis.

The finite difference approaches divide into two categories: those that solve only Poisson's equation, and those that solve Poisson's equation and the current continuity equation. The first type of simulation cannot treat high level punchthrough current accurately, thus it is not directly useful as the basis of a punchthrough model for computer-aided design. But it can provide insight into low level punchthrough, and in this respect it is useful. The second type of simulation is essential for the analysis of device behaviour in high level punchthrough. Such simulations will be considered in Section 2.4.

Under low level punchthrough conditions, the minority carrier concentration in the source and drain depletion regions, which is responsible for the punchthrough current, can be neglected in the solution of Poisson's

equation. The potential solution is dependent only on the device geometry, substrate doping distribution and applied voltages. The minority carrier density distribution can be deduced from this potential distribution, and then the current flow can be calculated. Simulators which involve the solution of only Poisson's equation are TWIST [1], GEMINI [2], and WATMOS [7].

Liu, Hoefflinger and Pederson, the authors of TWIST, point out that the convergence of a finite difference analysis is largely dependent upon the initial conditions supplied. Thus TWIST begins by breaking the two-dimensional transistor geometry into a number of regions for which analytic approximations to the electric potential are generated. This approximate solution is supplied to the finite difference analyser which then generates the two-dimensional potential distribution.

By the use of an appropriate equation, the potential distribution can be used to calculate the punchthrough current. This relation takes the form of a diffusion equation because the lateral component of the electric field is zero along the potential minimum locus, hence the lateral current flows only by diffusion in this region. Under low level conditions, the quasi-Fermi level for the minority carriers is relatively constant near the potential minimum locus, thus the carrier concentration, and hence the lateral current density, can be calculated directly from the potential. Using these two ideas, the total current can be obtained by integrating over the lateral diffusion current density along the potential minimum locus. Hence the punchthrough current [1] is given by:

$$I_{DS} = \frac{qDn_i^2 W}{N_{sub} W_B} \int \exp \left\{ q \left[\phi_B(y) - \phi_{SRC} \right] / kT \right\} dy \quad (2.3.1)$$

where W_B is the "base width", W is the gate width, $\phi_B(y)$ is the barrier lowering at any depth y , D is the carrier diffusivity, and ϕ_{SRC} is the source bias, given that the substrate is used as a potential reference. This term would be called the substrate bias if the source was used as a reference. This equation is consistent with the definition of the punch-through mechanism put forward in Section 2.1.

One remarkable thing about this equation is the use of a "base width" in a device geometry that has no neutral base. The need for this stems from the fact that a concentration gradient is required for use in the diffusion current expression. In the neutral base of a bipolar transistor, the concentration gradient is given by the excess minority carrier concentration on the emitter side of the base, divided by the base width. For a MOSFET in punchthrough, the region near the saddle point has very low fields and is similar to the neutral base of a bipolar device. If the width of the low field region is taken to be the base width, then the carrier concentration gradient along the potential minimum locus can be obtained. The base width is defined to be the distance on either side of the saddle point that must be travelled to have the potential change by one or two kT/q . Its value is only weakly dependent on the number of kT/q used in the definition since the potential varies rapidly near the saddle point.

TWIST is limited to studying low level punchthrough currents since it does not solve the current continuity equation. Its accuracy is also limited because of the use of a loosely defined base width. Nonetheless, TWIST does make a major contribution to our understanding of punchthrough current because it illustrates the form of the punchthrough current equation. It shows that the punchthrough current must depend exponentially on the barrier lowering, and the pre-exponential factors take the same form as in any other injection current expression. Furthermore, to obtain the

total punchthrough current, the current density must be integrated from the surface down into the bulk. We shall see that these ideas are basic to constructing a punchthrough current model for computer-aided design.

GEMINI is very similar to TWIST in that it only solves Poisson's equation, and calculates the punchthrough current in a similar way. It differs in that the equation used to calculate punchthrough current is more sophisticated, because the integration has been performed analytically and a term involving V_{DS} has been added to ensure that I_{DS} is zero when V_{DS} is zero. This equation is:

$$I_{DS} = -qD_n W \frac{Z^*}{L^*} \frac{n_i^2}{N_B} \exp \left[\frac{q(\psi^* - V_S)}{kT} \right] \left[1 - \exp \left(\frac{-q V_{DS}}{kT} \right) \right] \quad (2.3.2)$$

where Z^* and L^* are the effective width and length, respectively, of the injection near the saddle point, ψ^* is the barrier lowering at the saddle point, and V_S is the source bias using the substrate as a reference.

This equation is applied in a polar coordinate system where the r axis points in the direction of the current injection at the saddle point, the θ axis is orthogonal to the r axis, and the saddle point is the origin. (See Figure 2.3.1.) L^* is defined as being the distance from where the potential is $\psi^* + (\pi/4) kT/q$ on either side of the saddle point on the r axis. Z^* is defined as being the distance from where the potential is $\psi^* - (\pi/4) kT/q$ on either side of the saddle point on the θ axis. If the maximum on the potential minimum locus appears at the surface, then

$$Z^* = \frac{kT}{q} / |E_S| \quad (2.3.3)$$

where E_S is the vertical component of the electric field at this point.

Figure 2.3.1 The Coordinate System Used by GEMINI's [2]
Punchthrough Current Equation

Equation (2.3.2) can be derived [2] from the carrier current equations if one assumes low level conditions, Boltzmann statistics, and that the quasi-Fermi level of the minority carriers is essentially constant from the source to the saddle point. The derivation involves an integration of the current density along the potential minimum locus, hence equation (2.3.2) is consistent with the definition of punchthrough current given previously. The full derivation shows that the ratio Z^*/L^* is actually a two-dimensional integral in r, θ space. The definitions for Z^* and L^* given previously can be derived from this integral.

Greenfield and Dutton, the authors of GEMINI, found that the punchthrough current given by equation (2.3.2) under low level conditions, was in good agreement with the results of simulations using CADDET [3-5], which is a program that solves both Poisson's equation and the current continuity equation. It also provided reasonable agreement between measured and simulated results for drain currents of less than 10^{-5} A for a device of 10 μm width. Currents in this range for a device of this size are clearly low level. Thus equation (2.3.2) is an improvement over equation (2.3.1) because it can be used to simulate punchthrough currents accurately. This improvement is presumably due to the replacement of the empirical parameter W_B with the rigorously derived value L^* .

GEMINI serves to confirm that punchthrough current depends exponentially on the barrier lowering, and that the pre-exponential factors resemble those of any other injection equation. But it still cannot simulate high level punchthrough current, and thus it is not directly applicable for the purpose of modelling punchthrough for computer-aided design.

Husain and Chamberlain [7] developed a simulation called WATMOS which is similar to TWIST and GEMINI in that it only solves Poisson's equation. Its major difference is that it produces a solution in three dimensions

rather than two. This allows one to study the effect of channel width on punchthrough current.

The two-dimensional potential distributions produced by WATMOS for devices in punchthrough closely resemble those produced by TWIST and GEMINI. They show saddle points in the bulk through which the majority of the injection occurs. No details are given as to how punchthrough currents are calculated in WATMOS. In any case, the only new information produced by WATMOS is that as the channel becomes more narrow, the punchthrough current is reduced. This is because a narrow channel tends to reduce the barrier lowering near the edges of the device.

2.4 Models That Solve Both Poisson's Equation and the Current Continuity Equation

WATMOS, TWIST and GEMINI all have the same basic limitation; they cannot simulate high level punchthrough current. In order to do this, a simulator that solves both Poisson's equation and the current continuity equation must be used. Such a model was first created by Toyobe et al. [3] and it is called CADDET. MINIMOS is a similar, but more sophisticated, simulator developed subsequently by Selberherr et al. [6].

Very few details about the nature of the approach used by CADDET have been published. This is presumably because it is considered to be proprietary information by Hitachi Ltd. where CADDET was developed. All that is known about the approach is that it normalizes Poisson's equation using Gummel's algorithm [10], which is then solved using Stone's method [11]. The current continuity equation is solved using the stream function [12] and the line iteration method.

Barnes, Shimohigashi and Dutton [5] used CADDET to do an extensive study of punchthrough current. They observed the same form of potential distribution, with a saddle point through which most of the injection occurs, as was seen with the other two-dimensional simulations. It was found that the position of this saddle point moved closer to the source with higher drain voltages, and it moved closer to the gate with higher substrate biases. The authors observed that the amount of barrier lowering at the saddle point depended linearly on V_{DS} for low drain voltages, and only weakly on V_{DS} for higher values. They approximated the barrier lowering at the saddle point by the empirical expression

$$\Delta V_{bi} = \alpha \ln (V_{DS} / V_{DS0}) \quad (2.4.1)$$

where ΔV_{bi} is the barrier lowering, α is a fitting parameter, and V_{DS0} is the intercept of the ΔV_{bi} vs $\ln V_{DS}$ plot on the V_{DS} axis.

Barnes et al. were able to use CADDET to obtain agreement between measured and simulated drain current characteristics in the punchthrough regime. They observed that in punchthrough the drain current depended on V_{DS} as:

$$I_{DS} \propto \left(\frac{V_{DS}}{V_{DS0}} \right)^{\gamma} \quad (2.4.2)$$

where γ is a fitting parameter. It was found that the drain current was suppressed by both substrate bias and by negative gate bias. An increased substrate bias increases the height of the potential barrier that must be surmounted for injection to occur. According to the authors, a negative gate bias suppressed punchthrough by changing the potential distribution near the source, but no more details were given. They arbitrarily defined

the punchthrough voltage as the drain voltage necessary to produce 1 μ A of punchthrough current. The following equation was then formulated which approximates the dependence of the punchthrough voltage on the substrate bias.

$$V_{PT} = V_{PT}(0) + K \left(\sqrt{V_{SB} + V_{bi}} - \sqrt{V_{bi}} \right) \quad (2.4.3)$$

where $V_{PT}(0)$ is the punchthrough voltage at zero substrate bias, K is a fitting parameter, and V_{bi} is the built-in voltage for the source-substrate junction.

Barnes et al. used CADDET to show three ways in which the punchthrough voltage could be increased. All of these methods were aimed at increasing substrate doping between the drain and the source below the channel. The most straightforward solution is to simply increase the substrate doping, but this will affect the threshold voltage and its substrate bias sensitivity. Another approach is to increase the range parameter of the threshold voltage implant so that the dopant is distributed more deeply. Still another solution is to use two ion implantations [13]. The first implant is a surface implant which is used for threshold voltage adjustment. The second implant is a deeper implant which is used to raise the punchthrough voltage.

The highest carrier concentration that Barnes et al. encountered in their simulations was in the range of 10^{13} - 10^{14} cm^{-3} . The substrate doping level for the devices they simulated was in the range of 10^{15} - 10^{17} cm^{-3} . Thus their simulations were all at low level. From this they concluded that the punchthrough current in their devices was at low level and barrier limited, not high level and space charge limited. By this they mean that under low level conditions the punchthrough current is governed by the bar-

rier lowering that comes from the solution of Poisson's equation, and it is only weakly dependent on the space charge of the current. Space charge limited means that the degree of barrier lowering, and hence the current, is limited by the space charge of that same current.

Barnes et al.'s conclusion that the punchthrough current in their devices is all low level is strange considering that we have already seen that a typical device has high level punchthrough currents with reasonably low drain voltages. If CADDET will solve simultaneously Poisson's equation and the current continuity equation, why did they not simulate high level punchthrough? This may have been a decision by the authors or it may be that the numerical model of CADDET will not converge for the extreme conditions of high level punchthrough.

The results obtained using CADDET are clearly the most useful to date. They produce a better idea of the physical nature of punchthrough than the results of any of the other simulations we have considered. But these results cannot be treated as a definitive answer for the purpose of constructing a simulation for computer-aided design. This is because the equations that Barnes et al. have presented are empirical, and would be difficult to use for computer-aided design owing to the employment of fitting parameters. Furthermore, all their simulations are restricted to low level punchthrough current, whereas high level punchthrough current must also be considered for a computer-aided design simulation. It must be realized that conditions may be considerably different for high level punchthrough, and it is unlikely that the results presented by Barnes et al. would then be valid. Since CADDET was not available to this author, it was not possible to investigate whether it would operate under high level con-

ditions. All such simulations were done using MINIMOS [6] which was available*.

Several versions of MINIMOS have been made available to independent users by the Technical University of Vienna where it was developed. The one used in this work is called MINIMOS Version 2.1, but it shall hereafter be referred to as simply MINIMOS. This version is the most sophisticated of those presently available.

MINIMOS is a two-dimensional MOSFET simulator that solves both Poisson's equation and the current continuity equation. It requires the input of bias conditions and a description of the device to be simulated in the form of oxide thickness; gate length, width and material; and doping levels. The two-dimensional doping profile can be generated in three ways. One way is to describe the diffusion and implantation steps to MINIMOS and it will generate a doping profile automatically. A second way is to supply MINIMOS with the one-dimensional profile from the process simulation program SUPREM [14], and MINIMOS will generate a two-dimensional profile from this. The third way is the same as the second except that the one-dimensional profile is defined point-by-point by the user.

MINIMOS has a number of sophisticated features. It has an elaborate mobility model which accounts for the mobility's dependence on temperature, electric field, spatial position, ionized dopant concentration, and carrier concentration. This model can be compared to CADDET's model which uses a constant value for hole and electron mobilities [5]. MINIMOS also automatically generates a non-uniform two-dimensional grid. The grid spacings depend upon device geometry, bias values and the doping profile.

MINIMOS will calculate ionization integrals, and thus it can be used to simulate avalanche currents. On the other hand, CADDET simply calcu-

* Courtesy of Northern Telecom Electronics Ltd., Corkstown Labs, Ottawa.

lates whether the gain of the avalanche process is greater than one, in which case the program stops [5].

In the paper in which Selberherr et al. introduced MINIMOS [6], they simulated punchthrough current in three different devices. The first had a uniform substrate, the second had a surface implant, and the third had both surface and bulk implants. MINIMOS showed that the punchthrough current flows predominantly at the surface for the uniform substrate device, the current is forced down into the bulk by the surface implant, and it is forced back to the surface by the bulk implant. MINIMOS also shows that the punchthrough current is greatly reduced by the two implants. These examples illustrate that MINIMOS is capable of simulating punchthrough current.

It would seem that MINIMOS has no real limitations because it simulates all the major mechanisms that occur in a MOSFET. Unfortunately, in this author's experience, when MINIMOS is used to simulate punchthrough current in short-channel devices, simulated and measured results are not likely to agree. The simulated drain currents have been found to be between one and nine orders of magnitude too small.

This observation is in distinct contrast to the good agreement between measured and simulated results obtained for longer channel devices, which can be obtained by appropriately choosing the device parameters and avalanche model coefficients. It would appear that agreement could also be secured for short-channel devices operating in punchthrough if these quantities could be set to the proper values.

For short-channel MOSFETs in high level punchthrough, the solution of Poisson's equation is highly dependent upon device parameters and the amount of ionization charge present, which can be significant if the device is in weak avalanche. The barrier lowering is given by the solution of

Poisson's equation, and the punchthrough current depends exponentially on the barrier lowering. Thus it is expected that the simulated drain current is strongly dependent upon the device parameters and avalanche model coefficients. The imperfect knowledge of these quantities is probably the cause of the disagreement between measured and simulated results.

However, for the purpose of this thesis it is not necessary to obtain agreement between measurements and the results of MINIMOS simulations. All that is required is to derive a few basic physical principles from these simulations, which can be used to derive a physical model. To achieve this, several devices that are presumed to be similar to those whose measured results are presented later in the thesis, were simulated in punch-through using MINIMOS.

It was found that this was not a simple task because convergence problems were encountered. The majority of the simulations that were tried did not converge either because the cycle limit was reached or because the model found that the device was in breakdown. Given these convergence problems, it was felt to be necessary to check the validity of the output by hand calculations when convergence was finally obtained. These calculations were used to check Gauss' Law, current continuity, and the agreement between the potential, quasi-Fermi level and carrier concentration. The mobility model was also checked to see if scatter-limited velocities were achieved. The errors detected by these checks could all be accounted for by round-off error. Thus if MINIMOS converges, the solution it produces is physically real and can be used to derive physical principles. This is what will be done with the results of the following simulations.

In order to understand these simulations, a few words of explanation must first be provided about the graphics used to display the results. MINIMOS outputs files which contain the two-dimensional variation of vari-

ables such as potential, electric field, and carrier concentration. These files can be displayed as a three-dimensional picture, where the x axis is the depth into the silicon, the y axis is the lateral dimension between the source and the drain running along the silicon surface, and the z axis is the variable of interest. The origin of this coordinate system lies on the silicon surface and is in line with the edge of the gate nearest the source. The only additional information needed to understand these plots is that the source is on the left and the drain is on the right.

The first device that was simulated was p-channel with a uniform substrate doping of 10^{15} cm^{-3} . It had drain and source junction depths of .63 μm , a gate length of 2.78 μm , a channel length of 1.66 μm , and an oxide thickness of 85 nm. The gate, source and substrate were grounded, and -15 V was applied to the drain.

The MINIMOS simulation of this device gave the potential distribution of Figure 2.4.1. A close-up of the channel potential, in Figure 2.4.2, reveals the existence of a saddle point approximately .1 μm in the y direction from the source, and .42 μm below the silicon surface. Analysis of the numerical data shows that the carrier concentration at the saddle point is $2.5 \times 10^{14} \text{ cm}^{-3}$, which means that the punchthrough current is at low level. The numerical data also reveals that the holes need travel only .8 μm beyond the saddle point before the fields become strong enough to accelerate them to scatter-limited velocity.

The current flow mechanism can be studied by looking at the plot of carrier concentration in Figure 2.4.3. A close-up of the carrier concentration in the channel region (see Figure 2.4.4) reveals that the current is injected in the bulk around the saddle point, and it then proceeds towards the drain in a mainly lateral direction. Some current spreading into the bulk is observed as the holes approach the drain.

FIGURE 2.4.1 POTENTIAL DISTRIBUTION FOR 1.66 μ m P-CHANNEL DEVICE

FIGURE 2.4.2 CLOSE-UP OF CHANNEL POTENTIAL FOR 1.66 μ m P-CHANNEL DEVICE

FIGURE 2.4.3 CARRIER CONCENTRATION FOR 1.60UM P-CHANNEL DEVICE

FIGURE 2.4.4 CLOSE-UP OF CARRIER CONC. FOR 1.60UM P-CHANNEL DEVICE

It is instructive to compare this simulation to a simulation of a similar p-channel device in high level punchthrough. The high level conditions were facilitated by merely shortening the gate length to $2.18 \mu\text{m}$, which produces a channel length of $1.06 \mu\text{m}$. All other parameters and bias conditions were maintained at their previous values.

This change caused the drain current to rise by two orders of magnitude. The saddle point was still in the bulk, as can be seen in Figure 2.4.5, and it was less than $.1 \mu\text{m}$ from the source. The carrier concentration at the saddle point rose to $3.69 \times 10^{15} \text{ cm}^{-3}$, which means that the current is at high level. The distance needed to accelerate the injected holes to scatter-limited velocity was shortened to $.3 \mu\text{m}$, due to the higher fields. The current flow can be seen in a plot of carrier concentration in Figure 2.4.6. This graph strongly resembles Figure 2.4.4, and it shows a predominantly lateral current with some current spreading into the bulk as the holes near the drain.

An n-channel device was also simulated whose parameters were chosen so that it would operate in high level punchthrough. This device had source and drain junction depths of $1.09 \mu\text{m}$, a gate length of $2.5 \mu\text{m}$, a channel length of $.6 \mu\text{m}$, a gate oxide thickness of 85 nm , and a substrate doping of $1.05 \times 10^{16} \text{ cm}^{-3}$. The gate, source and substrate were grounded, and 10 V was applied to the drain.

The MINIMOS simulation of this device produced a potential distribution which had a maximum on the potential minimum locus at the silicon surface. This can be seen in the close-up of the channel potential presented in Figure 2.4.7. One could call this a "half saddle point", but for simplicity let us call this a "surface saddle point". It should be noted that all MINIMOS simulations of similar n-channel devices produced surface

FIGURE 2-4-5 CLOSE UP OF CHANNEL POTENTIAL FOR 1.03UM P CHANNEL DEVICE

FIGURE 2-4-6 CLOSE UP OF CHANNEL PLOT FOR 1.03UM P CHANNEL DEVICE

FIGURE 2.4.7 CLOSE-UP OF CHANNEL POTENTIAL FOR μM N-CHANNEL DEVICE

FIGURE 2.4.8 CLOSE-UP OF CARRIER CONC. FOR μM N-CHANNEL DEVICE

saddle points. Another interesting observation is that this saddle point actually appeared inside the n-type region of the source.

The numerical data given by the simulation showed that the carrier concentration at the saddle point was $3.39 \times 10^{16} \text{ cm}^{-3}$, which means that the punchthrough current was at high level. These data also showed that the injected electrons reached scatter-limited velocity after they had travelled only $.3 \text{ } \mu\text{m}$ from the saddle point. The current flow can be understood by observing the carrier concentration in Figure 2.4.8. This shows that the carrier injection occurs mainly at the surface near the saddle point. The current then flows in a predominantly lateral direction with some spreading towards the bulk as the electrons near the drain. This is the same current-spreading phenomenon that was observed for the p-channel devices.

From these simulations, the following conclusions can be drawn: The saddle point appears at the surface for the n-channel devices and in the bulk for the p-channel devices, and is always very close to the source. According to Fu [21], this is due to the different flatband voltages of the n and p-channel devices. A second conclusion is that the punchthrough current in any device can be made to be at high level. These current flows are predominantly lateral except for some current spreading towards the bulk as the carriers approach the drain. Another conclusion is that the injected carriers are quickly accelerated to scatter-limited velocity. We will find that these observations will be very important in the development of a punchthrough model for computer-aided design.

2.5 Observations on the Punchthrough Characteristics of Fabricated Devices

There are two more observations which should be made before attempting to construct a punchthrough model for computer-aided design. These are made most easily by reference to measured device characteristics rather than two-dimensional simulations.

Figure 2.5.1 shows the device characteristics of an n-channel MOSFET which has source and drain junction depths of $1.1\text{ }\mu\text{m}$, a gate length of $2\text{ }\mu\text{m}$, a channel length of $.75\text{ }\mu\text{m}$, a gate oxide thickness of 85 nm , and a substrate doping of 10^{15} cm^{-3} . The characteristics exhibit a well-defined triode region and a steeply sloped saturation region. The steep slope is due to the fact that punchthrough current is being added to the channel current in this region, and the length of the channel inversion layer becomes shorter with increasing drain voltage. In the third region, where the drain current rises rapidly, punchthrough current is dominant. This will be referred to as the "punchthrough regime" of operation.

The key observation to make here is that in the punchthrough regime the drain current is only a weak function of the gate voltage. For these characteristics the gate voltage is varied between 0 and 5 V, but the drain current in the punchthrough regime changes by only a few percent. This can be physically justified by noting that once the gate voltage has created an inversion layer, which is a thin surface layer of very dense charge, then the bulk is screened from the effect of the gate. Furthermore, in high level punchthrough, the carriers injected near the surface screen the deeper bulk from the effect of the gate. Thus the gate has very little effect on the potential in the bulk, and hence on the punchthrough current.

Figure 2.5.1 The Effect of Gate Voltage on Punchthrough Characteristics

Therefore, to a reasonably good approximation, the dependence of punch-through current on the gate voltage can be neglected.

Our next observation relates to the influence of substrate bias on the drain current in the punchthrough regime. Figure 2.5.2 shows a plot of I_D vs V_{BS} for $V_{GS} = 0$ and $V_{DS} = 16$ V, for a p-channel device which has drain and source junction depths of $.63 \mu\text{m}$, a gate length of $2 \mu\text{m}$, a channel length of $.8 \mu\text{m}$, and an oxide thickness of 85 nm . It has a bulk doping of 10^{15} cm^{-3} , and its surface is doped lightly p-type by a threshold adjustment implant. The surface doping concentration is $3 \times 10^{15} \text{ cm}^{-3}$ p-type, and the junction depth of the implant is $.3 \mu\text{m}$. It can be seen from Figure 2.5.2 that in punchthrough the drain current is only weakly a function of substrate bias. Similar measurements were made on n-channel devices with the same parameters as the device whose drain characteristics are shown in Figure 2.5.1 except that the channel lengths were longer. For these transistors, it was found that there was no measurable change of drain current with substrate biases up to -4 V.

The above observation is in direct contradiction to the statements of many authors [1,2,5,8,9], who say that a larger substrate bias increases the potential barrier for injection near the source, and this significantly reduces the punchthrough current. However, the results reported by these authors were for low level punchthrough currents. In this case, the effect of a substrate bias is to increase the width of the depletion region and change the boundary condition at the depletion region edge. Clearly, if the space charge of the current is negligible, this change of boundary condition will have a large effect on the solution of Poisson's equation, and hence on the punchthrough current. But if the punchthrough current is at high level and a substrate bias is applied, then the space charge of the current will shield the silicon above it from the effect of this change in

FIGURE 2.5.2

ID vs VBS FOR A DEVICE IN PUNCHTHROUGH

the boundary condition. The substrate bias will therefore have only a small effect on the punchthrough current as noted in the present work.

We have observed that high level punchthrough current is a weak function of gate voltage and substrate bias. This means that in high level punchthrough a MOSFET can be treated as a two-terminal device, with the drain and source as the only terminals of consequence. This conclusion may be used to greatly simplify the construction of a punchthrough model for computer-aided design.

CHAPTER 3

A PUNCHTHROUGH MODEL FOR COMPUTER-AIDED DESIGN

3.1 A General Description of the Punchthrough Model and Its Approximations

From the definition of the punchthrough mechanism and our analysis of the finite difference simulations, the essential procedure for the calculation of punchthrough current has been established. Poisson's equation and the current continuity equation must be solved simultaneously for the MOSFET geometry and boundary conditions. From this solution the potential and the punchthrough current density along the potential minimum locus can be obtained. Then the integration of the current density yields the total punchthrough current of the device.

The relevant punchthrough simulations that have been examined hitherto have solved Poisson's equation using two-dimensional finite difference analysis. This approach is not useful for a punchthrough model for computer-aided design because it requires four or five orders of magnitude more CPU time than is practical. The question that must now be answered is: What other approaches can be used?

An analytic solution of Poisson's equation and the current continuity equation for the two-dimensional MOSFET geometry and boundary conditions does not of course exist. However, it will be seen that an analytic solution does exist for a one-dimensional punchthrough geometry. Perhaps this solution can be utilized to help solve this problem.

It may also be possible to use some numerical techniques in the model. Although two-dimensional finite difference analysis has already been elimi-

nated, possibly one-dimensional finite difference analysis could be used, provided that the number of intervals is not too large. Another numerical technique that might be helpful is numerical integration.

It was shown in Section 2.5 that high level punchthrough current depends only weakly on the gate voltage and the substrate bias. This means that a MOSFET operating in high level punchthrough can be thought of as a two-terminal device, with the only relevant terminals being the drain and the source. Thus an approximate analysis of the MOSFET in punchthrough can omit the effect of the gate and substrate voltages. The effect of the gate can be eliminated by proceeding as though it did not exist and only analyzing the region below the silicon surface. Thus there will be no boundary conditions at this surface. The effect of the substrate bias can be ignored by setting it to some arbitrary value. Since the punchthrough current is only weakly dependent on the substrate bias this value is not critical, so let us choose it to be zero.

Another simplification can be made by recalling the MINIMOS simulations presented previously (see Figures 2.4.4, 2.4.6 and 2.4.8) which show that the punchthrough current flows in a predominantly lateral direction, with some spreading towards the bulk as the carriers approach the drain. This situation can be approximated by considering the punchthrough current to be entirely lateral. To make use of this approximation, the depletion region between the source and the drain, from the silicon surface down to the depletion region intersection point, must be divided into a large number of strips parallel to the surface. These lateral strips are of length l which is a function of depth x , as depicted in Figure 3.1.1. If these strips are thin enough, then the punchthrough current density and barrier lowering across their width will be essentially constant. Furthermore, because the current flow is assumed to be lateral, the electric field lines

Figure 3.1.1 The Lateral Strips

Figure 3.1.2 The One-Dimensional Punchthrough Geometry

must be lateral also. Hence they are parallel to, and do not cross the strip boundaries. Thus each individual strip resembles a one-dimensional punchthrough device whose geometry is shown in Figure 3.1.2.

An approximate, simultaneous solution of Poisson's equation and the current continuity equation is derived for this one-dimensional structure in Section 3.3. This solution provides the barrier lowering and punchthrough current density as a function of the applied voltage and device structure. In principle, this solution can be applied to each lateral strip to yield the barrier lowering and punchthrough current density along the entire potential minimum locus. But first, two issues must be dealt with that are consequences of the approximations which have just been made.

The first issue is that the boundary condition at the depletion region intersection point is not satisfied by blindly applying the one-dimensional solution to each lateral strip. If the neutral substrate is defined to be at zero potential, then the boundary condition at the depletion region intersection point is that the potential is zero there also. In Section 2.1 it was explained that the depletion region intersection point is the potential minimum on the lateral line which passes through it. Thus the boundary condition can be satisfied by adjusting the length of the lateral strip which passes through this point so that the barrier lowering, or in other words the potential minimum for this strip, is zero. This is done by calculating a length Δl which is added to the geometric length of all the lateral strips, including the one that passes through the depletion region intersection point. It must be added to all the strip lengths so as not to distort the drain and source underdiffusion curvature, and thus the basic device geometry is preserved. An analytic equation which can be used to calculate Δl is derived in Section 3.5.

The second issue that must be dealt with is charge balance in the volume under consideration. By using the one-dimensional approximation, it is tacitly assumed that the electric field lines originating from the charges in the volume that is divided into lateral strips, all terminate on charges in the source or drain regions. Clearly, this is not so because some of them terminate on charges on the gate, or on charges generated by impact ionization. The latter phenomenon can be quite important because weak avalanche breakdown usually accompanies punchthrough. Furthermore, the electric field distribution is affected by the field lines originating from the depletion region which was not included in the lateral strips. These effects all contribute to changing the amount of charge which should be considered in the one-dimensional solution. This problem can be remedied by using the channel length as a fitting parameter to change the amount of charge in the volume under consideration. It is used by selecting a non-physical value which will cause the measured and simulated characteristics to match at a single point. This allows the charge in the volume under consideration to be adjusted to approximately the correct value. This procedure is quite different from the calculation of Δl because the channel length is used to define the MOSFET geometry, and hence remains fixed throughout the simulation. By comparison, Δl is allowed to change as the drain voltage is varied, so as to continue to satisfy the potential boundary condition at the depletion region intersection point.

It should be noted that this sort of charge balance adjustment can be used to obtain better agreement for a number of different models. Although the authors did not publish the fact, it has been found by the modelling group at Northern Telecom Electronics that charge balance adjustment is useful both with El-Mansy and Boothroyd's [19] saturation region model and

with Ratnakumar and Meindl's [20] threshold voltage model. Thus the use of this technique is not without precedent.

The stage has now been reached where an outline of the MOSFET punch-through model can be given. First, a channel length is chosen and the size of the depletion region is determined. It is then divided into lateral strips parallel to the surface. Next, a length Δz is calculated and added to all the geometric strip lengths, which permits the potential boundary condition at the depletion region intersection point to be satisfied. The one-dimensional solution of Poisson's equation and the current continuity equation is then applied to each of the lateral strips, and the barrier lowering and punchthrough current density are calculated. Finally, the current density is integrated to find the punchthrough current of the device. This procedure may have to be used several times with several non-physical channel lengths to obtain good agreement between measured and simulated results. Once the proper channel length is chosen, charge balance is approximately satisfied.

An advantage of this analysis is that, by virtue of the lateral strip approximation, it can be used to simulate punchthrough current in non-uniform substrate MOSFETs. This may be done using the doping at the depth of each lateral strip as the effective substrate doping for that strip. Thus the doping is allowed to change from one lateral strip to another, but the method of analysis remains essentially the same.

With these ideas and approximations, we are now ready to construct a punchthrough current model for computer-aided design. The tasks that remain to do this are to derive an expression for the punchthrough current density, solve Poisson's equation and the current continuity equation for a one-dimensional punchthrough geometry, find an efficient way to calculate the cylindrical depletion layer widths, and then apply these equations to

the MOSFET geometry. These aspects of the modelling process are addressed in the remainder of this chapter.

3.2 A Derivation of the Punchthrough Current Density Equation

In order to calculate punchthrough current, an expression must be derived for the punchthrough current density as a function of the barrier lowering along the potential minimum locus. This derivation begins by noting that any electron current is given by:

$$\underline{J_n} = -qn\underline{v} \quad (3.2.1)$$

where $\underline{v}$ is the equivalent electron velocity due to both drift and diffusion. If the current is assumed to be entirely lateral, then according to the coordinate system defined in Figure 3.1.1, the injected electron current density in an n-channel MOSFET is negative. Thus the punchthrough current density is given by:

$$J_{PT} = -J_n = qnv \quad (3.2.2)$$

The electron density n is given by:

$$n(\phi, E_{Fn}) = n_i e^{(E_{Fn} - E_i(\phi))/kT} \quad (3.2.3)$$

where ϕ is the potential, E_{Fn} is the quasi-Fermi energy level, E_i is the mid-band energy level, and n_i is the intrinsic carrier density. The expression for the mid-band energy level as a function of potential is:

$$E_1(\phi) = E_{10} - q\phi \quad (3.2.4)$$

where E_{10} is the equilibrium mid-band energy level. Substitution of equation (3.2.4) into equation (3.2.3) yields:

$$n = n_1 e^{(E_{Fn} - E_{10})/kT} e^{q\phi/kT} \quad (3.2.5)$$

The analysis can now be greatly simplified if the quasi-Fermi energy level is approximated to be constant from the edge of the neutral region of the source to the potential minimum locus. Although the grid used by MINIMOS is too coarse to give accurate values, the results of simulations indicate that the variation of the quasi-Fermi energy level in this region is less than .1 or .2 kT, even in high level punchthrough. Thus it is reasonable to approximate this value as a constant. Using this assumption, the first two terms of equation (3.2.5) are equal to the equilibrium electron concentration in the neutral substrate. Thus:

$$n = \frac{n_1^2}{N_B} e^{q\phi/kT} \quad (3.2.6)$$

Since the potential along the potential minimum locus is the barrier lowering ϕ_{BL} , then the electron concentration along this locus is:

$$n = \frac{n_1^2}{N_B} e^{q\phi_{BL}/kT} \quad (3.2.7)$$

Another observation that was made of the MINIMOS simulations was that the carriers were accelerated to the scatter-limited velocity v_g shortly

after injection. An approximation to this situation is to assume that the carriers move at the scatter-limited velocity as soon as they are injected. Thus the velocity in equation (3.2.2) can be set equal to v_s . Using this approximation and substituting equation (3.2.7) for n , equation (3.2.2) becomes:

$$J_{PT} = \frac{qn_s^2 v_s}{N_B} e^{q\phi_{BL} / kT} \quad (3.2.8)$$

This is the expression for the punchthrough current density which we seek.

It is to be expected that the punchthrough current density would go to zero for zero barrier lowering. Thus equation (3.2.8) should be more properly written as:

$$J_{PT} = \frac{qn_s^2 v_s}{N_B} \left(e^{q\phi_{BL} / kT} - 1 \right) \quad (3.2.9)$$

However, we are only interested in cases where the barrier lowering causes the exponential term to be much larger than 1. Therefore equation (3.2.8) will suffice for our purposes. Note that equation (3.2.9) is also applicable to holes if the hole scatter-limited velocity is used.

Equation (3.2.9) is very similar to the current injection expressions used by TWIST and GEMINI, and this gives one faith in its validity. It is virtually identical to an expression used by Boothroyd [15] in an unpublished report concerning punchthrough current simulation. He used the same expression, but did not derive it as rigorously as has been done here.

3.3 A Simultaneous Solution of Poisson's Equation and the Current Continuity Equation for a One-Dimensional Punchthrough Geometry

It is impossible to solve analytically Poisson's equation and the current continuity equation for the two-dimensional geometry of a MOSFET operating in punchthrough. But it is possible to solve these equations for a one-dimensional punchthrough geometry such as would exist for a large area bipolar transistor with a heavily doped emitter and collector. This geometry was presented in Figure 3.1.2. Note that the regions in this figure are labelled Source, Substrate and Drain. This labelling is merely to establish the polarity of the applied voltage and for future reference when this model is applied to the MOSFET geometry. The method used to obtain a solution is to first solve Poisson's equation with the mobile charge neglected. Then the effect of the mobile charge is accounted for by assuming that it is uniformly distributed in the substrate, and the charge density is increased accordingly.

The first part of this solution begins by defining the substrate to be at zero potential. Then the source is at the built-in potential ϕ_B and the drain is at potential $\phi_B + V_{DS}$. The built-in potential ϕ_B is given by:

$$\phi_B = \frac{kT}{q} \ln \left(\frac{N_S N_B}{n_i^2} \right) \quad (3.3.1)$$

where N_S is the doping concentration of the source and drain, and N_B is the substrate doping. Note that all regions are assumed to be uniformly doped. The drain and source potentials give us the following boundary conditions:

$$\phi(0) = \phi_B \quad (3.3.2)$$

$$\phi(L) = \phi_B + V_{DS} \quad (3.3.3)$$

Let us assume that a large enough drain to source voltage has been applied to cause the drain and source depletion regions to meet. Thus the substrate is entirely depleted, and Poisson's equation in the substrate can be written as:

$$\frac{d^2 \phi}{dy^2} = \frac{qN_B}{\epsilon} = M \quad (3.3.4)$$

where ϵ is the product of the dielectric constant of silicon and the permittivity of free space, and M is a constant.

Using the boundary conditions given by equations (3.3.2) and (3.3.3), the solution of Poisson's equation is:

$$\phi(y) = \frac{M}{2} (y^2 - ly) + V_{DS} \frac{y}{l} + \phi_B \quad (3.3.5)$$

where l is the distance between the drain and source metallurgical junctions. This expression is sketched in Figure 3.3.1. Note that the potential minimum is marked as the barrier lowering ϕ_{BL} since the two are identical. This potential will cause current to be injected from the source with a current density given by equation (3.2.8).

The position of the potential minimum can be found by setting the first derivative of the potential equal to zero. Thus:

$$\frac{d\phi}{dy} = 0 = \frac{M}{2} (2y - l) + \frac{V_{DS}}{l} \quad (3.3.6)$$

yields that the position y_M is given by:

Figure 3.3.1 The Potential Distribution in a One-Dimensional Punchthrough Device

$$y_M = \frac{L}{2} - \frac{V_{DS}}{L M} \quad (3.3.7)$$

The effect of the mobile charge may now be included by using the following equation for the punchthrough current density which was given in Section 3.2:

$$J_{PT} = qnv \quad (3.3.8)$$

If it is assumed that the current density across the cross-section of the one-dimensional punchthrough device is uniform, and that all the carriers move at the scatter-limited velocity v_s , then the number density of the carriers in the current N_C is given by:

$$N_C = \frac{J_{PT}}{qv_s} \quad (3.3.9)$$

Thus the total number density of negative charges in the substrate N_T is given by the sum of the negative charges due to the substrate doping and those due to the current. Hence:

$$N_T = N_B + N_C = N_B + \frac{J_{PT}}{qv_s} \quad (3.3.10)$$

Substituting for J_{PT} using equation (3.2.8), N_T can be written as:

$$N_T = N_B + \frac{n_i^2}{N_B} \exp\left(\frac{q \phi_{BL}}{kT}\right) \quad (3.3.11)$$

Let us now replace M with qN_T/ϵ in equations (3.3.5) and (3.3.7), which assumes that the carriers in the current are uniformly distributed throughout the substrate. This yields:

$$\phi(y) = \frac{qN_T}{2\epsilon} (y^2 - ly) + V_{DS} \frac{y}{l} + \phi_B \quad (3.3.12)$$

$$y_M = \frac{l}{2} - \frac{V_{DS}\epsilon}{lqN_T} \quad (3.3.13)$$

The barrier lowering, which is equal to $\phi(y_M)$, can now be obtained by substituting y_M for y in equation (3.3.12) which reduces to:

$$\phi_{BL} = \frac{V_{DS}}{2} + \phi_B - \frac{V_{DS}^2\epsilon}{2l^2qN_T} - \frac{l^2qN_T}{8\epsilon} \quad (3.3.14)$$

Equation (3.3.14) expresses the coupling between Poisson's equation and the current continuity equation, by virtue of the fact that N_T depends upon the barrier lowering ϕ_{BL} . In principle, this transcendental equation can be solved for the barrier lowering at any arbitrary current density. In practice, N_T has an exponential dependence on ϕ_{BL} that can be observed in equation (3.3.11), which gives equation (3.3.14) unstable properties when it is used in an iterative solution.

This problem can be remedied by rearranging equation (3.3.14) to give the following equation which is quadratic in N_T .

$$N_T^2 + \frac{8\epsilon}{l^2q} \left(\phi_{BL} - \phi_B - \frac{V_{DS}}{2} \right) N_T + \left(\frac{2V_{DS}\epsilon}{ql^2} \right)^2 = 0 \quad (3.3.15)$$

The roots of equation (3.3.15) are:

$$N_T = \frac{4\epsilon}{q\ell} \left\{ \frac{V_{DS}}{2} + \phi_B - \phi_{BL} \pm \left[V_{DS} (\phi_B - \phi_{BL}) + (\phi_B - \phi_{BL})^2 \right]^{\frac{1}{2}} \right\} \quad (3.3.16)$$

To choose the correct root, let us do a binomial expansion of the square root term for the condition:

$$V_{DS} \ll (\phi_B - \phi_{BL}) \quad (3.3.17)$$

This yields:

$$N_T = \frac{4\epsilon}{q\ell} (\phi_B - \phi_{BL}) \left\{ 1 + \frac{V_{DS}}{2 (\phi_B - \phi_{BL})} \pm \left[1 + \frac{V_{DS}}{2 (\phi_B - \phi_{BL})} \right] \right\} \quad (3.3.18)$$

If the negative root is chosen, then N_T is equal to zero. Since N_T cannot be less than the substrate doping N_B , this is clearly a spurious root.

Thus N_T is given by:

$$N_T = \frac{4\epsilon}{q\ell} \left\{ \frac{V_{DS}}{2} + \phi_B - \phi_{BL} + \left[V_{DS} (\phi_B - \phi_{BL}) + (\phi_B - \phi_{BL})^2 \right]^{\frac{1}{2}} \right\} \quad (3.3.19)$$

To make use of this solution, equation (3.3.11) must be rearranged to give:

$$\phi_{BL} = \frac{kT}{q} \ln \left[\frac{N_B}{n_1^2} (N_T - N_B) \right] \quad (3.3.20)$$

Then substituting equation (3.3.19) for N_T yields:

$$\phi_{BL} = \frac{kT}{q} \ln \left[\frac{N_B}{n_i} \left(\frac{4\epsilon}{ql^2} \left\{ V_{DS} / 2 + \phi_B - \phi_{BL} + \left[V_{DS} (\phi_B - \phi_{BL}) + (\phi_B - \phi_{BL})^2 \right]^{1/2} \right\} - N_B \right) \right] \quad (3.3.21)$$

This equation can be used iteratively to find the barrier lowering under virtually any high-level conditions. If the initial value is chosen to be .4 V, then it will converge to an accuracy of 1 part in 10^5 in 4 to 8 iterations for carrier concentrations that are as low as 5 to 10% of the substrate doping. For lower carrier concentrations, N_T will become less than N_B in the course of the iterative solution, and the logarithm will become a complex number. If this condition is encountered, then the low-level equations (3.3.5) and (3.3.7) can be applied to obtain the barrier lowering. This is most easily done by substituting equation (3.3.7) into equation (3.3.5) to obtain the following expression, which may be used to calculate the low-level barrier lowering.

$$\phi_{BL} = \frac{V_{DS}}{2} + \phi_B - \frac{V_{DS}^2 \epsilon}{2l^2 q N_B} - \frac{l^2 q N_B}{8\epsilon} \quad (3.3.22)$$

Very close to the transition from high to low level conditions, numerical oscillations are sometimes observed if equation (3.3.21) is used. This problem can be eliminated by employing a longer word length for the numbers used in the calculation, or by reducing the required accuracy.

A method has now been established whereby the barrier lowering can be calculated for a one-dimensional punchthrough device for both high and low level currents. Once it is found, the barrier lowering can be used in equation (3.2.8) to obtain the punchthrough current density. This consti-

gives an approximate, simultaneous solution of Poisson's equation and the current continuity equation for a one-dimensional punchthrough geometry. The task that remains is to apply this one-dimensional solution to the complex two-dimensional geometry of the MOSFET.

3.4 An Efficient Method for Calculating Cylindrical Depletion Layer Widths

As has been mentioned previously, it is important to know where the depletion region intersection point is in order to calculate punchthrough current. The position of this point can only be calculated if it is known where the edge of the drain and source depletion regions are. If the drain and source underdiffusions are modelled as quarter circular cylinders, then the depletion widths needed to calculate the position of the depletion region intersection point may be calculated from cylindrical geometry.

The cylindrical geometry of the source is presented in cross-section in Figure 3.4.1. The radius of the underdiffusion is r_j and the radius of the depletion region is R_s . The vector marked r defines a polar coordinate system with point 0 as the origin.

Given this geometry, several approximations must be made before calculating the depletion layer width. First, since the source is generally about four orders of magnitude more heavily doped than the substrate, the depletion region width in the source can be ignored and the one-sided junction approximation can be used. This approximation models the depletion region as being entirely on the more lightly doped side of the junction.

Another simplification that may be made is to treat both the source and the substrate as being uniformly doped. The substrate is taken to be at the bulk doping concentration which is reasonably accurate except near

Figure 3.4.1 The Source Depletion Layer Geometry

the metallurgical junction. The source is taken to be at the surface concentration. This is not an accurate model of the true doping concentration, but it does not affect the depletion layer width since the one-sided junction approximation is being used, and it yields the correct built-in potential. Thus this approximation is acceptable.

Using the above simplifications and defining the substrate to be at zero potential, the following boundary condition is obtained:

$$\phi(R_s) = 0 \quad (3.4.1)$$

Let us apply an arbitrary voltage from the source to the substrate V_a , then the boundary condition at r_j is:

$$\phi(r_j) = \phi_B + V_a \quad (3.4.2)$$

Because there is assumed to be no voltage variation in the source or in the neutral substrate, the other boundary conditions are that the electric field is zero at R_s :

$$E(R_s) = 0 \quad (3.4.3)$$

and the electric field at r_j is a maximum:

$$E(r_j) = E_{\max} \quad (3.4.4)$$

Using the one-sided junction approximation and assuming that the substrate is uniformly doped, Poisson's equation for the depletion region in cylindrical coordinates is:

$$\frac{1}{r} \frac{d}{dr} \left(r \frac{d\phi}{dr} \right) = \frac{qN_B}{\epsilon} = M \quad (3.4.5)$$

This can be integrated as follows:

$$\int_{-r_j E_{\max}}^{-r E(r)} d \left(r \frac{d\phi}{dr} \right) = \int_{r_j}^r M r \, dr \quad (3.4.6)$$

and yields:

$$-r E(r) + r_j E_{\max} = \frac{M}{2} (r^2 - r_j^2) \quad (3.4.7)$$

Solving for $E_{\max}$ and applying the boundary condition that $E(R_s) = 0$, it is found that:

$$E_{\max} = \frac{M}{2r_j} (R_s^2 - r_j^2) \quad (3.4.8)$$

Substituting this expression into equation (3.4.7) for $E_{\max}$ and noting that:

$$E(r) = -\frac{d\phi}{dr} \quad (3.4.9)$$

a second integral can be constructed:

$$\int_{\phi_B + V_a}^{\phi(r)} d\phi = \frac{M}{2} \int_{r_j}^r \left(r - \frac{R_s^2}{r} \right) dr \quad (3.4.10)$$

This integral gives the following expression for the potential in the depletion region:

$$\phi(r) = \phi_B + V_a + \frac{M}{2} \left[\frac{r^2 - r_j^2}{2} - R_s^2 \ln \left(\frac{r}{r_j} \right) \right] \quad (3.4.11)$$

The one boundary condition that has not been used in this derivation is that $\phi(R_s) = 0$. This boundary condition can now be applied to find an equation for R_s since it is not otherwise determined. Thus:

$$\phi(R_s) = 0 = \phi_B + V_a + \frac{M}{2} \left[\frac{R_s^2 - r_j^2}{2} - R_s^2 \ln \left(\frac{R_s}{r_j} \right) \right] \quad (3.4.12)$$

This expression can be rearranged to give the following transcendental equation:

$$R_s = \left[\frac{\frac{R_s^2 - r_j^2}{2} + \frac{2}{M} (\phi_B + V_a)}{\ln \left(\frac{R_s}{r_j} \right)} \right]^{\frac{1}{2}} \quad (3.4.13)$$

Equation (3.4.13) can be solved iteratively, and it is found that there are two roots for R_s . One is larger than r_j and one is smaller. The larger one is of course the physical root. The larger root can be obtained by choosing an initial value greater than r_j . The smaller root is obtained for a starting value less than r_j , and the equation diverges if R_s is set equal to r_j .

It has been found that convergence is in general fastest for a starting value of $r_j + 10^{-5}$ cm. This allows convergence to the proper root in 6 iterations with an accuracy of 1 part in 10^6 .

Equation (3.4.13) may also be applied to the drain by using V_{DS} as the applied voltage V_a . Thus this equation can be used to calculate drain and

source depletion layer widths, and it is used for this purpose in the punchthrough current model developed in the next section.

3.5 Applying the One-Dimensional Solution to MOSFET Geometry

Thus far, the general nature of the MOSFET punchthrough current model has been outlined, and some of the key expressions necessary to implement this model have been derived. These expressions include: the punchthrough current density equation, an approximate, simultaneous solution of Poisson's equation and the current continuity equation for a one-dimensional punchthrough geometry, and an equation to calculate drain and source depletion layer widths. What remains to be done is to apply the one-dimensional solution to the two-dimensional MOSFET geometry.

The way in which this may be done was described in Section 3.1. The depletion region from the surface down to the depletion region intersection point must be divided into thin strips parallel to the surface. Provided that the current is approximated to be completely lateral, and the strips are thin enough, the one-dimensional solution of Poisson's equation and the current continuity equation can be applied to each strip. After satisfying two additional conditions, the punchthrough current density can be calculated for each strip and integrated to yield the punchthrough current of the device. These additional conditions are that a length Δl must be calculated and added to each strip length to satisfy the potential boundary condition at the depletion region intersection point, and the channel length must be used as a fitting parameter to maintain charge balance in the volume of interest. The latter requirement needs no additional equations but the former does, and a suitable equation for the calculation of Δl is derived in this section. Another geometric consideration which requires

attention is the condition that exists when the depletion region intersection point drops below the drain and source junction depths. Equations to deal with this situation are also derived in this section.

The idealized MOSFET geometry used by the punchthrough current model is presented in Figure 3.5.1. A Cartesian coordinate system has been defined for this geometry with point 0 as the origin. As before, the underdiffusions and their depletion regions are modelled as quarter circular cylinders. The radius of the drain and source underdiffusions is r_j , and the radii of the source and drain depletion regions are R_s and R_d , respectively. The quantity l is the length of a lateral strip for a given x . The depth of the depletion region intersection point, which is labelled with a capital S, is called s and is indicated on the x axis. The channel length is denoted as L_c and the gate length is L_g . Note that this gate length may not be the true geometric gate length if a radius of curvature is used for r_j rather than the underdiffusion distance, because L_g is defined as:

$$L_g = L_c + 2 r_j \quad (3.5.1)$$

The radius of curvature is used for r_j so that the circular boundary of the idealized junction can be fit as closely as possible to the real junction contour. Note that in general the radius of curvature is significantly larger than the underdiffusion length.

An equation for the lateral strip length can be derived by using Pythagoras' Theorem. This yields:

$$l = L_g - 2 \left(r_j^2 - x^2 \right)^{\frac{1}{2}} \quad (3.5.2)$$

Figure 3.5.1 The MOSFET Punchthrough Geometry and Geometric Parameters

Another expression that is required is s in terms of known quantities. This can be obtained by extending the depletion region quarter circles into full circles, as is shown in Figure 3.5.2. The source depletion region circle C_1 has the equation:

$$C_1: x^2 + y^2 = R_s^2 \quad (3.5.3)$$

The drain depletion region circle C_2 has the equation:

$$C_2: x^2 + (y - L_g)^2 = R_d^2 \quad (3.5.4)$$

Point S is one of the two intersection points of the circles, so to find its x coordinate solve equations (3.5.3) and (3.5.4) for y . Choose the positive root for C_1 and the negative root for C_2 to obtain the correct semicircles. Thus:

$$C_1: y = + \left(R_s^2 - x^2 \right)^{\frac{1}{2}} \quad (3.5.5)$$

$$C_2: y = L_g - \left(R_d^2 - x^2 \right)^{\frac{1}{2}} \quad (3.5.6)$$

Now equate these two expressions, set x equal to s , and solve for s . Choosing the positive root because it is physically real, the following equation for s is obtained:

$$s = \left[R_d^2 - \left(\frac{L_g^2 + R_d^2 - R_s^2}{2 L_g} \right)^2 \right]^{\frac{1}{2}} \quad (3.5.7)$$

Figure 3.5.2 The Depletion Region Edges Extended to Full Circles

An equation must now be derived to find Δl , which is used to satisfy the potential boundary condition at the depletion region intersection point. To calculate Δl , the junction-to-junction length of the one-dimensional punchthrough geometry which will produce a potential minimum of zero must be calculated. Let us call this length l' . If the lateral strip passing through the depletion region intersection point is adjusted so that it equals l' , then the potential minimum along this strip becomes zero. Thus the boundary condition at the depletion region intersection point is satisfied.

To derive l' , we recall that the solution of Poisson's equation for the one-dimensional punchthrough geometry was given by equation (3.3.5), and the position of the potential minimum was given by equation (3.3.7).

$$\phi(y) = \frac{M}{2} (y^2 - ly) + V_{DS} \frac{y}{l} + \phi_B \quad (3.3.5)$$

$$y_M = \frac{l}{2} - \frac{V_{DS}}{lM} \quad (3.3.7)$$

Note that the low-level equations may be used in this derivation because no current flows through the depletion region intersection point. Substituting y_M for y in equation (3.3.5) to find the potential minimum $\phi(y_M)$, and then equating the equation to zero, gives:

$$\phi(y_M) = 0 = \frac{M}{8} l^2 - \left(\frac{V_{DS}}{2} + \phi_B \right) + \frac{V_{DS}^2}{2l^2 M} \quad (3.5.8)$$

Using the following substitutions:

$$u = l^2 \quad (3.5.9)$$

$$a = \frac{M}{8} \quad (3.5.10)$$

$$b = \frac{V_{DS}}{2} + \phi_B \quad (3.5.11)$$

$$c = \frac{V_{DS}^2}{2M} \quad (3.5.12)$$

a quadratic equation in u , which is also quartic in l , is obtained.

$$0 = au^2 - bu + c \quad (3.5.13)$$

Since l' is a length it must be positive and real. Thus three of the four roots of the quartic equation can be discarded, which yields the following expression for l' :

$$l' = \left[\frac{b + \sqrt{b^2 - 4ac}}{2a} \right]^{\frac{1}{2}} \quad (3.5.14)$$

By looking at the expressions for l' , a , b and c , it can be seen that l' does not depend on the MOSFET geometry at all. It is simply the distance two n^+ regions must be separated in order that a potential minimum of zero can be obtained in the common depletion region, for a given set of doping levels and bias conditions.

After l' has been calculated, Δl may be found by determining the geometric lateral strip length l_s at depth s (see Figure 3.5.1), where l_s is given by:

$$l_s = L_g - 2 \left(r_j^2 - s^2 \right)^{\frac{1}{2}} \quad (3.5.15)$$

and then:

$$\Delta l = l' - l_g \quad (3.5.16)$$

Once Δl is found by this method it can be added to all the geometric lateral strip lengths to satisfy the potential boundary condition at the depletion region intersection point. Thus using equation (3.5.2) for the geometric strip length, it is found that the modified strip length is given by:

$$l = l_g - 2 \left(r_j^2 - x^2 \right)^{\frac{1}{2}} + \Delta l \quad (3.5.17)$$

It should be noted that although Δl has been treated previously as though it was a positive quantity, it can in fact be negative for very short-channel devices, if large drain voltages are applied. Under extreme conditions, this can produce negative channel lengths. Since a punch-through current cannot be calculated for a negative channel length, this phenomenon is used by the model to place an upper limit on the drain voltage which can be simulated.

As previously mentioned, another geometric consideration that must be dealt with is the condition that exists when the depletion region intersection point drops below the drain and source junction depths. This condition is illustrated in Figure 3.5.3. The first problem encountered when extending the model into this regime is that of dividing the depletion region between the junction depth and the depletion region intersection point into strips. Rather than become embroiled in the complexities of dividing this region into curved or angular strips (see Figure 3.5.3), it has been found to be sufficient to simply neglect any current flowing below

Figure 3.5.3 The MOSFET Geometry for the Condition $s > r_j$

the junction depth. This is a reasonably good approximation because the barrier lowering and current density in this region are much less than in those regions above the junction depth.

The only difficulty introduced by this approximation is that ΔL can no longer be calculated, since the depletion region intersection point is omitted from the analysis. This problem is dealt with by assuming that the value of ΔL calculated when s equals r_j , which is referred to as ΔL_s , is also the value of ΔL required when s is greater than r_j . Provided that ΔL does not vary too rapidly, this is a reasonably good assumption. The use of ΔL_s in place of ΔL , when the depletion region intersection point is below the junction depth, allows the model to be extended into this regime.

The analysis to determine ΔL_s begins by finding the values of R_s and V_{DS} that will cause s and r_j to be equal. These values will be referred to as R_{ds} and V_{DSS} , respectively. An equation for R_{ds} is derived by setting s equal to r_j in equation (3.5.7) and using the substitution:

$$u = R_{ds}^2 \quad (3.5.18)$$

This yields:

$$0 = u^2 - 2(L_g^2 + R_s^2)u + 4L_g^2 r_j^2 + L_g^2 R_s^2 \quad (3.5.19)$$

which is solved for u , and then the positive root of u is taken to obtain R_{ds} . This still leaves two possible roots since equation (3.5.19) is quadratic in R_{ds} . The proper root is found by numerical substitution which yields:

$$R_{ds} = \left[L_g^2 + R_s^2 - 2L_g \left(R_s^2 - r_j^2 \right)^{1/2} \right]^{1/2} \quad (3.5.20)$$

The value of V_{DSS} is calculated by setting equation (3.4.11) equal to zero, solving for V_{DSS} , and replacing R_d with R_{ds} . This gives:

$$V_{DSS} = \frac{M}{2} \left[R_s^2 \ln \left(\frac{R_{ds}}{r_j} \right) + \frac{r_j^2 - R_{ds}^2}{2} \right] - \phi_B \quad (3.5.21)$$

Now that V_{DSS} is found, the value of Δl_s is determined by setting V_{DS} equal to V_{DSS} in the calculation of l' , and then using the following equation:

$$\Delta l_s = l' - L_g \quad (3.5.22)$$

The gate length L_g is used because it is the geometric strip length at the junction depth.

A second problem that is encountered in this regime occurs when the drain depletion region gets so large that its edge intersects the source depletion region where it is flat (see Figure 3.5.4). This violates the conditions under which equation (3.5.7) was derived, and causes s to become complex. The problem can be avoided by calculating R_{dmax} , which is the largest value of R_d for which equation (3.5.7) is valid. It is given by:

$$R_{dmax} = \left(R_s^2 + L_g^2 \right)^{\frac{1}{2}} \quad (3.5.23)$$

If R_d is found to be larger than R_{dmax} , then equation (3.5.7) is not used to calculate s . It is simply set equal to R_g , which initiates the use of Δl_s later in the algorithm. Thus the use of R_{dmax} avoids computational difficulties.

The stage has now been reached at which the complete punchthrough current model can be described. Given the doping levels, drain voltage,

Figure 3.5.4 The Geometry Used for the Calculation of R_{dmax}

and a value for r_j , equation (3.4.13) is used to calculate R_g and R_d . A check is then done to see if punchthrough has occurred. The condition for punchthrough is that $R_g + R_d$ is greater than L_g . If this is so, then the simulation continues. If it is not, then the punchthrough current is zero and the simulation is finished. Another check must then be done to see if R_d is greater than R_{dmax} . If it is, then the calculation of s is skipped and s is set equal to R_g . If it is not, then equation (3.5.7) is used to calculate s .

Once s has been found, it is used to determine the number of points in the finite difference analysis using one of the following equations:

$$N = \text{truncation } (s/\Delta x) + 1 \quad (3.5.24)$$

$$N = \text{truncation } (r_j / \Delta x) + 1 \quad (3.5.25)$$

where N is the number of points at which the barrier lowering and punchthrough current density must be calculated for $N-1$ lateral strips. Equation (3.5.24) is used if s is less than r_j , and equation (3.5.25) is used if s is greater than or equal to r_j . The parameter Δx used in these two equations is the strip width. It must be chosen to be small enough so as to provide for a large enough number of strips. A value such as $.01 \mu m$ is appropriate. These two equations allow the analysis to be limited to the region above the junction depth.

The value of x is now stepped from 0 to $(N-1) \Delta x$ in steps of Δx , and used to calculate the lateral strip length l at each value of x using equation (3.5.17). The value of Δl is calculated and used in this equation if s is less than r_j , and Δl_g is used in place of Δl if s is greater than or equal to r_j . Once l has been obtained, it is used in equation (3.3.21) to

find the barrier lowering ϕ_{BL} , and the punchthrough current density J_{PT} is calculated from this value. The current density is then numerically integrated using Simpson's Rule to obtain the punchthrough current of the device. Thus:

$$I_{PT} = \frac{W \Delta x}{3} \sum_1 \left(J_{PT}^{i-1} + 4 J_{PT}^i + J_{PT}^{i+1} \right) \quad (3.5.26)$$

for $i = 2, 4, 6 \dots N-1$ (or $N-2$ if $N-1$ is odd)

where W is the width of the gate.

As was mentioned in Section 3.1, this model can also be used to simulate punchthrough current for non-uniform substrate MOSFETs. This is made possible by the lateral strip approximation, because a non-uniformly doped substrate generally has lateral symmetry. Thus the substrate doping distribution can be approximated by setting the doping level in each strip to the doping level at that depth. The analysis for each strip proceeds as though the entire substrate was doped at the same level as the strip in question.

In order to know how many strips there are, the value of s must be determined, but this is impossible for a non-uniform substrate because equation (3.5.7) is no longer valid. The solution to this problem is to use the bulk doping level, which is the uniform doping level in the substrate, in the calculation of s . This will yield a maximum value of s provided that this is the lowest doping level in the substrate. This value of s can be used to find the maximum number of strips that is possible. Individual punchthrough checks can then be conducted for each strip to decide whether or not to include them in the analysis.

For punchthrough to occur in a given strip, the following condition must be satisfied:

$$\left[\left(R_s^2 - x^2 \right)^{\frac{1}{2}} + \left(R_d^2 - x^2 \right)^{\frac{1}{2}} \right] > L_g \quad (3.5.27)$$

Note that the values of R_s and R_d used in this equation are calculated using the effective substrate doping for the strip in question. Thus they are the values for a uniform substrate doped at this level. This is not strictly correct, because for the depletion layer calculations in a non-uniformly doped substrate, it is really only valid to assume uniform doping along a single strip. But it is necessary since equation (3.4.13), which calculates R_s and R_d , assumes a uniformly doped substrate. This is believed to be a reasonable approximation to the true situation which is not susceptible to rigorous analysis.

If the punchthrough condition is satisfied, then the calculations proceed as though this strip was part of a uniformly doped substrate whose doping level is the same as that of the strip. Thus all the quantities which are used in the uniform substrate simulation such as: s , R_{dmax} , Δl , Δl_g , l , ϕ_{BL} and J_{PT} must be calculated for this strip using its doping level. Note that since these parameters must be recalculated for the doping level of every strip, a non-uniform substrate simulation requires more computation than does a uniform substrate simulation. Once the current density has been found for all of the lateral strips, it is integrated using equation (3.5.26) to yield the punchthrough current of the device.

The outlines presented in this section of the punchthrough current models for uniform and non-uniform substrate MOSFETs are useful for understanding. They also serve as an introduction to the implementation of the model as computer algorithms, which are described in the next chapter.

CHAPTER 4

ALGORITHMS FOR THE SIMULATION OF PUNCHTHROUGH CURRENT
IN UNIFORM AND NON-UNIFORM SUBSTRATE MOSFETS4.1 Uniform Substrate Algorithm

This chapter presents the computer implementation of the punchthrough current model. The simulation for a uniform substrate MOSFET is carried out by the FORTRAN program UNISUB, the listing of which is presented in Appendix A.

UNISUB's inputs are the device geometry parameters, the doping densities, and some physical constants. Its outputs are two files: the first lists the punchthrough current as a function of drain voltage; the second gives the barrier lowering, punchthrough current density, lateral strip length, space charge number density, and a parameter which specifies whether conditions are high or low level, for each x value used in the simulation. Examples of these two outputs can be seen in Appendices C and D, respectively.

UNISUB begins by establishing the device parameters and physical constants using DATA statements. This is followed by some interactive code that allows the user to specify the channel length, select whether or not to have the second data file, and choose an n or p-channel simulation. The only differences between the n and p-channel simulations are the value of the scatter-limited velocity, and the sign of the voltages and currents in the output. The scatter-limited velocity values are specified in line 6 and they are 1×10^7 cm/s for electrons and 6×10^6 cm/s for holes.

The calculations begin with the determination of the thermal voltage V_T , the gate length L_g , the built-in potential ϕ_B , and the constant M . Next, the strip width Δx is fixed at 10^{-6} cm, and the value of the source depletion region radius R_s is calculated using the subroutine RGEN, which is found at the bottom of the listing. This subroutine solves equation (3.4.13) iteratively, and can be used to calculate both R_s and R_d . Note that it is written in double precision to ensure that the iterative solution converges and does not oscillate.

In the next section, entitled "Calculate DLS", the value of ΔL_s is found using the equations for R_{ds} , V_{DSS} , a , b , c , L' and ΔL_s . Notice that ΔL_s is calculated before the loop in which V_{DS} is chosen is entered, because V_{DS} is not necessary for this calculation and this is computationally more efficient.

Next, the value of V_{DS} is chosen, and it is used to calculate R_d by calling the subroutine RGEN. In the section entitled "Excessively High V_{DS} Check", R_{dmax} is calculated and compared to R_d . If R_d is larger, then s is set equal to R_s and the calculation of s using equation (3.5.7) is skipped.

In the next section, a check is made to see if punchthrough has occurred. This is done by comparing $R_s + R_d$ to L_g . If $R_s + R_d$ is smaller, then the depletion regions have not overlapped and punchthrough has not occurred. Then I_{PT} is set equal to zero and the program moves onto the next voltage to be considered. If $R_s + R_d$ is larger than L_g , then punchthrough has occurred and s is calculated. A second check is then performed to see if s is greater than $2 \Delta x$. This must be done because at least three points are required for a Simpson's Rule numerical integration. If this condition is met, then the number of points for the finite difference analysis is calculated from either equation (3.5.24) or equation (3.5.25). The

former equation is used if s is less than r_j , and the latter is used if s is greater than or equal to r_j . If this condition is not met, then I_{PT} is set equal to zero and the program seeks the next value of V_{DS} .

At this point in the simulation all the physical constants and geometric parameters have been calculated, and the grid for the lateral strip finite difference analysis has been defined by N and Δx . Thus we are now ready to calculate the barrier lowering for each lateral strip. This process is begun by calculating the value of $\Delta \ell$ for the drain voltage being considered. It is calculated using the equations for b , c , ℓ' , ℓ_s and $\Delta \ell$. Note that a does not need to be found since it was determined in the calculation of $\Delta \ell_s$ and it is a constant. Once this has been done, an x value is chosen and the lateral strip length ℓ is calculated.

A check is now initiated to discover if ℓ is negative. If it is, then error messages are output and the simulation halts because the V_{DS} limit of the model has been exceeded. If it is not, then the simulation continues and a loop is entered which calculates the barrier lowering ϕ_{BL} . Using an initial value of .4 V for the barrier lowering, the space charge number density N_T is calculated using equation (3.3.19). A new value of barrier lowering is then calculated from N_T using equation (3.3.20). The loop causes these two equations to be used iteratively until the barrier lowering is found to an accuracy of 1 part in 10^5 . If at any time in the iteration N_T is found to be greater than the source doping N_S , then the conditions are too high level to be simulated. This causes an error message to be output and the program halts. At the other extreme, if N_T is found to be less than the substrate doping N_B , then the conditions are too low level to be simulated by equation (3.3.20). An exit must then be made from the loop or else the use of a value of N_T less than N_B in equation (3.3.20) will cause the equation to diverge. When this exit is made, the low-level

expression, which is equation (3.3.22), is used to find the barrier lowering. This calculation does not require any iteration.

Once the barrier lowering has been determined, it is used in equation (3.2.8) to calculate the punchthrough current density J_{PT} . This value is then stored in an array for future use. After the appropriate signs have been chosen, the values of x , ϕ_{BL} , J_{PT} , l , N_T , and a parameter which is 1 if the current is high level, and 2 if it is low level, are output to a data file. This file may be examined to obtain physical understanding of the punchthrough current mechanism.

The current density array is now integrated using Simpson's Rule which is given in equation (3.5.26). This yields the punchthrough current for the drain voltage in question, and these two values are output to a file that records the punchthrough current characteristic. The program then loops back and chooses the next value of V_{DS} for which the punchthrough current is to be calculated until there are no values left. This completes the description of the program UNISUB which simulates punchthrough current in uniform substrate short-channel MOSFETs.

4.2 Non-Uniform Substrate Algorithm

The simulation of punchthrough current in non-uniform substrate MOSFETs, is implemented in the program NONUNI whose listing is presented in Appendix B. It is very similar to UNISUB except that the doping level is allowed to change from one lateral strip to another.

The fundamental aspects of the non-uniform substrate algorithm are that the maximum number of lateral strips is calculated by assuming that the substrate is uniformly doped at the bulk doping level, and then a separate analysis is applied to each lateral strip with the provision that the

doping level may change from one strip to another. There are three major changes which must be made to the uniform substrate program UNISUB to implement this algorithm: first, two punchthrough checks must be used for greater computational efficiency; second, a method of selecting and checking the doping of the lateral strips must be devised; and third, the order of calculations must be changed because the effective substrate doping for each strip is not immediately available.

The first change involves using a check similar to the one in UNISUB to see if any lateral strip could be in punchthrough. If the answer is affirmative, then a second check tests the punchthrough condition for each lateral strip. This is necessary because if punchthrough has not occurred, it is better to detect this with one check rather than many. The first test is done by setting the substrate doping to the bulk doping level, calculating R_s and R_d , and then seeing if $R_s + R_d$ is greater than L_g . If this is true, then punchthrough has occurred, and if it is not, then punchthrough has not occurred. The rationale behind this is that it checks to see if punchthrough has taken place at the surface for the lowest doping level in the substrate. If punchthrough has not happened for this condition, which most strongly favours the phenomenon, then it has not happened at all.

This check is performed by the section of code in NONUNI, entitled "Uniform Substrate Punchthrough Check". The values of R_s and R_d calculated here are used in the next section to determine the number of strips for the finite difference analysis, since the second calculation also requires that the bulk doping level be used. It involves finding R_{dmax} , and comparing R_d to this value sets s equal to R_s or allows it to be found from equation (3.5.7). The value of s is then compared to r , and, depending upon which one is larger, the number of points in the finite difference analysis N is

obtained from either equation (3.5.24) or equation (3.5.25). (See Section 3.5 for a more detailed analysis of these calculations.)

After this number is determined, a lateral strip at depth x is chosen, and the effective substrate doping for this strip is found from the substrate doping function $SD(x)$. The substrate doping function can take any analytic form that approximates the substrate doping in question. An example of this function is presented in line 7 of NONUNI for a substrate with surface and bulk implants. This line is duplicated in equation (4.2.1):

$$SD(x) = C_s \exp(-x^2/\alpha^2) + C_I \exp\left[-(x - x_M)^2/\beta^2\right] + C_B \quad (4.2.1)$$

where C_s is the surface concentration, C_I is the maximum concentration in the bulk implant, C_B is the bulk concentration, x_M is the depth of the maximum of the bulk implant, and α and β are straggle parameters.

Once the effective substrate doping is obtained, it must be checked to make sure that it is within reasonable limits. In NONUNI, this is done by first checking that the doping level is no greater than an order of magnitude below the source doping. If it is, then the punchthrough current density for the strip in question is set to zero. Otherwise, a check is performed to test whether the substrate doping is less than an order of magnitude below the bulk doping. If this condition is true, then the punchthrough current density is set to zero. If it is not true, then the substrate doping is assumed to be in an acceptable range and the algorithm continues. Note that this check includes the case where the substrate doping has changed type due to an implant, because in NONUNI this is indicated by a negative doping level. The punchthrough current density is set

to zero for this situation because only buried channel current flows in this region. Thus it should not be included in a punchthrough simulation.

After these two checks are completed, the substrate doping is used to calculate new values for R_s , R_d , s , ϕ_B , M , R_{dmax} and ΔL . The rest of the program is identical to that of UNISUB with the exception that the variables just mentioned must be recalculated for each lateral strip. This is necessitated by the fact that they all depend upon the substrate doping, which is allowed to change from one lateral strip to another. The recalculation of these parameters for each strip makes this simulation more lengthy than that for a uniform substrate, but this is unavoidable if punchthrough current is to be simulated for non-uniform substrate devices.

Although the algorithms described in this chapter are fairly complicated, it will be seen that they are both fast enough and accurate enough for computer-aided design. This stems from the fact that they are based upon simple equations which are analytic or can be solved in a few iterations. The suitability of these algorithms is demonstrated in the next chapter.

CHAPTER 5 -

VERIFICATION OF THE PUNCHTHROUGH MODEL

5.1 Comparison of Measured and Simulated Results

The accuracy of the punchthrough current model used by the programs UNISUB and NONUNI was tested by comparing measured and simulated characteristics for three types of devices. The first two were uniform and non-uniform substrate p-channel MOSFETs. The third were uniform substrate n-channel MOSFETs. The relevant device parameters of these transistors are listed in Table 5.1.1.

TABLE 5.1.1 Device Parameters

CHANNEL	SUBSTRATE	N_S (cm^{-3})	N_B (cm^{-3})	r_j (μm)	W (μm)
p	Uniform	$5 \times 10^{19} \pm 10^{19}$	$1 \times 10^{15} \pm 10^{14}$	$.68 \pm .05$	50 ± 1
p	Non-uniform	5×10^{19}	1×10^{15}	.68	50
n	Uniform	1.5×10^{20}	$1.05 \times 10^{16} \pm 10^{15}$	1.03	50

The doping level of the source and drain N_S is actually the surface concentration. It was obtained from four-point probe measurements taken from appropriate source and drain diffusion test samples. It was assumed that these diffusions had a Gaussian distribution, thus Irvin's [16] curves could be used to obtain the surface concentration. The substrate doping for the p-channel devices was also obtained by four-point probe measurements. For the n-channel devices, it was found from SUPREM [14] simula-

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tions. The parameter r_j , as was noted in Section 3.5, is not the underdiffusion length, but the radius of curvature of the underdiffusions. This was obtained by fitting a radius of curvature to scanning electron micrographs of the underdiffusion [17]. The width of the transistors W was taken from the mask size.

The channel lengths for the devices considered in this section are listed in Table 5.1.2. The measured channel lengths are denoted as L_{cmea} , and were determined by optically measuring the gate length and then subtracting a known underdiffusion from both sides of the gate. The symbol L_{csim} denotes the channel length used in the punchthrough current simulation. It differs from the measured channel length because it has been used as a fitting parameter to obtain charge balance.

TABLE 5.1.2 Measured and Simulated Channel Lengths

DEVICE #	CHANNEL	L_{cmea} (μm)	L_{csim} (μm)
1	n	.75 $\pm$.1	.72
2	n	1.05	.90
3	p	1.6	1.95
4	p	1.35	2.0

It is seen from Table 5.1.1 that the uniform and non-uniform p-channel devices are very similar. In fact, they are the same structure except that the non-uniform device has a surface implant that makes the surface p-type. An analytic expression to describe the substrate doping concentration as a function of x was derived using SUPREM simulations which were then matched to threshold voltage measurements [18]. This method yielded the following expression:

$$SD(x) = 10^{15} - 4.3 \times 10^{15} \exp \left[-(x/.26)^2 \right] \quad (5.1.1)$$

where x is in microns and $SD(x)$ has dimensions of cm^{-3} . This expression is in the form necessary for use in the program NONUNI.

In order to check the accuracy of the model, a study was conducted using 10 devices of each of the three types. The uniform substrate devices were simulated using the program UNISUB and the non-uniform substrate devices were simulated using NONUNI. The simulated characteristics were fit to the measured characteristics at a single point using the channel length as a fitting parameter. As has been mentioned previously, this is done to obtain charge balance in the volume of interest. The measured and simulated results were then compared.

Some typical measured and simulated characteristics are presented in Figures 5.1.1 to 5.1.4. These are all I_D vs V_{DS} characteristics for $V_{GS} = 0$ and $V_{BS} = 0$. This characteristic was chosen so that a minimum of channel current would be measured. The only appreciable channel current appears for device #1 in Figure 5.1.1. Thus for this device, the measured characteristic is the sum of the channel and punchthrough currents. Since the simulated characteristic includes only punchthrough current, agreement should only be expected in the punchthrough regime where the punchthrough current is much greater than the channel current.

Another component of the drain current that could present problems is that due to avalanche ionization which, when present, flows as substrate current. This poses a problem for punchthrough measurements because punchthrough and avalanche can occur simultaneously. Thus it is not certain which is being measured until the drain and substrate currents are determined and compared. These currents were measured as a function of drain voltage for devices #1-4, and are presented in Figures 5.1.5 to 5.1.8.

FIGURE 5.1.1 ID vs VDS FOR DEVICE #1

FIGURE 5.1.2 ID vs VDS FOR DEVICE #2

FIGURE 5.1.3 ID vs VDS FOR DEVICE #3

FIGURE 5.1.4 ID vs VDS FOR DEVICE #4

FIGURE 5.1.5 ID and Isub vs VDS
DEVICE#1 Vgs=0 Vbs=0

FIGURE 5.1.6 ID and Isub vs VDS
DEVICE#2 Vgs=0 Vbs=0

FIGURE 5.1.7 ID and Isub vs VDS
DEVICE#3 Vgs=0 Vbs=0

FIGURE 5.1.8 ID and Isub vs VDS
DEVICE#4 Vgs=0 Vbs=0

In Figure 5.1.5 it is seen that when the steeply sloped regime begins, for device #1 at a drain voltage of 7 V (see Figure 5.1.1), the substrate current is two orders of magnitude less than the drain current. Thus the current throughout most or all of the steeply sloped regime is predominantly punchthrough current. Clearly, at some high value of drain voltage, the substrate current will become dominant, but considering the good agreement between measured and simulated results for this device, this value is thought to be higher than 10 V. Its exact value could not be determined due to the current limits of the apparatus used for the drain and substrate current measurements. The substrate current measurements for the other three devices (see Figures 5.1.6 to 5.1.8) are reasonably straightforward, because throughout the punchthrough regime, the substrate current is at least an order of magnitude below the drain current. Thus for all four devices, the drain current in the region of interest is due almost exclusively to punchthrough, and hence the comparison of measured and simulated characteristics in this region is valid.

The agreement between measured and simulated results displayed in Figures 5.1.1 to 5.1.4 is reasonably good, and is considered sufficient for the model to be used in computer-aided design. The accuracy is very satisfactory considering the number of approximations used in the model, and the extremely high-level nature of the punchthrough regime. The model indicates that the space charge in the punchthrough current for these simulations can be as much as 20 times the substrate doping. It also shows that virtually all of the punchthrough characteristic is due to high-level current.

It is interesting to note that the agreement is better for device #1 than for any of the other devices. The reason is that the visible punchthrough regime is delayed until a drain voltage of 7 V because of the pres-

ence of channel current. Thus when punchthrough current is finally seen, the carriers move at scatter-limited velocity for nearly their entire transit from the source to the drain because of the high electric fields present. Hence the approximation which set the carrier velocity to its scatter-limited value in the punchthrough current density equation is a reasonably good one. The carriers in the other three devices move at velocities less than the scatter-limited velocity for a greater fraction of their source to drain transit. This is due to the lower fields caused by the larger size of these devices, and the lower drain voltages in the punchthrough regime. Thus the scatter-limited velocity approximation is not as valid for these devices, and this is the major cause of the poorer agreement between measured and simulated results. Clearly, the use of a carrier velocity which depends upon the device parameters and applied voltages would improve the agreement, but this is considered to be beyond the scope of this work.

The fact that the agreement for devices #1, 2 and 3 is approximately the same raises another interesting point. This model is incapable of simulating a bulk saddle point because as one moves away from the surface there is a monotonic increase in the strip length, which produces a monotonic decrease in the barrier lowering. This is the result of using a one-dimensional solution to solve a two-dimensional problem. Yet it is known from MINIMOS simulations that device #2 has a surface saddle point, while devices #3 and 4 have bulk saddle points. It appears that the accuracy of the model does not greatly depend on whether the device has a surface or bulk saddle point. Thus its inability to simulate bulk saddle points does not appear to be a severe handicap.

Besides accuracy, the other important criterion for computer-aided design is the speed of the simulation. This was measured, and it was found

that for a device operating in high-level punchthrough, the average CPU time requirements per bias point on an IBM 4341 computer are 10 ms for a uniform substrate device and 46 ms for a non-uniform substrate device. When punchthrough does not occur, the CPU time requirements are .60 ms for a uniform substrate device and .82 ms for a non-uniform substrate device. These speeds are considered acceptable for computer-aided design use. An interesting comparison can be made by noting that MINIMOS requires approximately 500 CPU seconds to calculate a bias point for a uniform substrate MOSFET in high-level punchthrough. Thus using UNISUB reduces computation time by a factor of approximately 50,000.

There are two more observations which can be made to reveal more physical insights into the punchthrough model. The first is to notice the difference between the simulated punchthrough characteristics of the n-channel devices in Figures 5.1.1 and 5.1.2, and the p-channel devices in Figures 5.1.3 and 5.1.4. The difference is that the p-channel characteristics are nearly straight lines, while the n-channel characteristics are curves. This is due to the fact that the p-channel devices have a much lower substrate doping, which means that the punchthrough currents are mostly limited by the space charge of the current itself. The n-channel characteristics are more curved because the substrate doping plays more of a role in determining the current and, at least for lower drain voltages, the current is less space charge limited.

A second observation can be made by examining the full IV characteristics for devices #1 and 2 which can be seen in Figures 5.1.9 and 5.1.10, and recalling the measured and simulated $V_{GS} = 0$ characteristics for these devices from Figures 5.1.1 and 5.1.2. The measured and simulated characteristics for device #2 diverge sharply after the drain voltage reaches

Figure 5.1.9 IV Characteristics for Device #1

Figure 5.1.10 IV Characteristics for Device #2

9 V, while for device #1 the measured and simulated characteristics do not agree until a drain voltage of 7 V is attained. Thus the model predicts that breakdown in device #1 is due to punchthrough, and in device #2 it is due to avalanche. This prediction agrees with the substrate current measurements presented in Figures 5.1.5 and 5.1.6. Therefore the punchthrough model may be used to identify the predominant current mechanism in breakdown.

These two observations show that the punchthrough model which has been developed in this thesis has captured a large part of the physical reality of the punchthrough mechanism. It may therefore be used for the physical interpretation of measured results. This is significant because it is the first punchthrough model based on analytic equations which can make such a claim.

5.2 Use of the Model in Device Design

The punchthrough model that is derived in this work is physically based, and thus it may be used in the development of new devices. An especially useful application is to simulate short-channel MOSFETs with non-uniform substrates. Devices of this type will need to be developed for use in VLSI circuitry.

This is done by first fabricating the uniform substrate device and simulating its punchthrough characteristic with the program UNISUB. The measured and simulated results are then matched by using the channel length as a fitting parameter to obtain charge balance. The channel length determined by this process is used to simulate non-uniform substrate devices with the program NONUNI and, as long as the non-uniformities do not deviate too widely from the previous uniform substrate doping, it is reasonable to

expect that charge balance will be maintained. Once a non-uniform structure with the desired properties is identified, it may be simulated in more detail using a program such as MINIMOS.

An example of such an investigation is illustrated by studying Wang's [13] suggestion of a double boron implant process for n-channel MOSFETs. He uses a surface implant to adjust the threshold voltage and a bulk implant to reduce punchthrough by raising the substrate doping in this region.

This idea was studied by taking a .75 μm channel length n-channel MOSFET, which has the same parameters as device #1, and then adding surface and bulk implants to this structure. The device was simulated with a uniform substrate, a surface implant, and surface and bulk implants. The substrate doping function is given for the surface implant structure in equation (5.2.1), and for the double implant structure in equation (5.2.2).

$$SD(x) = 10^{17} \exp(-x^2/.01) + 1.05 \times 10^{16} \quad (5.2.1)$$

$$SD(x) = 10^{17} \exp(-x^2/.01) + 10^{17} \exp\left[-(x-.5)^2/.01\right] + 1.05 \times 10^{16} \quad (5.2.2)$$

where x is in microns and $SD(x)$ is in cm^{-3} .

The results of the simulation are seen in Figure 5.2.1. The effect of the increased substrate doping for both a single and a double implant is to decrease the punchthrough current. The net effect of the double implant is to increase the voltage at which punchthrough current appears from 2 V to 3 V. It is interesting to note that a .75 μm device that could operate with a drain voltage of 3 V is a feasible device for VLSI circuitry. It is clear from this example that the simulation NONUNI can be used as a first-order approximation for device development.

FIGURE 5.2.1

ID vs VDS FOR NON-UNIFORM SUBSTRATE DEVICES

CHAPTER 6

CONCLUSION

6.1 Summary

The investigation of punchthrough current was begun by defining the punchthrough current mechanism. This facilitated a better physical understanding of punchthrough, and it provided the basis for a study of the existing punchthrough models. A survey of these models showed that none of them is adequate for use in computer-aided design. The models either use too many simplifications to be accurate, or require too much computer time, or have both of these difficulties.

The derivation of a punchthrough current model that is suitable for computer-aided design was begun by deriving a punchthrough current density equation for a one-dimensional punchthrough geometry. Then Poisson's equation and the current continuity equation were simultaneously solved for the same one-dimensional geometry under conditions of both high and low level punchthrough. This solution was used for the MOSFET geometry by dividing the depletion region between the surface and the depletion region intersection point into thin strips parallel to the surface. The one-dimensional solution may then be applied to each of these strips to obtain the barrier lowering and punchthrough current density along the potential minimum locus, provided that two conditions are satisfied: first, an analytically calculated length Δz must be added to each of the lateral strips to satisfy the potential boundary condition at the depletion region intersection point; and second, the channel length must be used as a fitting parameter

to match the measured and simulated characteristics at one point in order to maintain charge balance. The current density along the potential minimum locus can then be integrated to yield the punchthrough current of the device.

The simulated characteristics produced by this model were compared to measured characteristics for uniform substrate n-channel devices, and both uniform and non-uniform substrate p-channel devices. The agreement between measured and simulated results was reasonably good, and is considered sufficient to allow the model to be used in computer-aided circuit design. The CPU time requirements per bias point were measured for the model, and it was determined that it requires 10 ms for a uniform substrate device and 46 ms for a non-uniform substrate device. This is approximately 50,000 times faster than a MINIMOS simulation.

It was found that the model captures enough of the physical reality of the punchthrough current mechanism for it to be used for the physical interpretation of device characteristics. Since it is physically based, the model may also be used as a first-order approximation for short-channel device development.

From the summary presented here, it is concluded that a model has been created which can simulate punchthrough current for both uniform and non-uniform substrate MOSFETs. It provides reasonable accuracy of simulation and has low CPU time requirements. Thus it is suitable for use in the computer-aided design of MOSFET circuits.

6.2 Future Research

As in any field of scientific endeavour, the research that has answered the questions that motivated this thesis has itself spawned more un-

answered questions. Most of these questions are related to the approximate, simultaneous solution of Poisson's equation and the current continuity equation for the two-dimensional MOSFET geometry. The first question that should be raised about this solution is: How accurate is it? This could be answered by comparing the solution to a MINIMOS output. Great care would have to be taken to ensure that both solutions were for the same device geometry and device parameters because, as was discussed in Section 2.4, the solution is very sensitive to these quantities.

The one thing that is known for certain about the accuracy of the approximate solution is that, as mentioned in Section 5.1, it cannot simulate bulk saddle points, even though it is known from MINIMOS simulations that these occur. Thus the model's potential solution can be very inaccurate. This raises the question that, if this is so, how can it simulate the characteristic with reasonable accuracy? The comparison of the real and approximate solutions might also yield the answer to this problem.

Another question in the same vein is: What causes the saddle point to be at the surface or in the bulk? It is known from MINIMOS simulations that the value of the flatband voltage affects the position of the saddle point [21]. But what effect do the other device parameters and bias conditions have? Again, MINIMOS simulations could provide some answers to this problem.

The approximate solution of Poisson's equation and the current continuity equation also raises a series of questions to do with charge balance. For instance, what is the significance of the value of the effective channel length, and are there other methods of fitting the measured and simulated results such as using the substrate doping? If the physical meaning of the effective channel length could be understood, then it might be possible to predict its value, which would eliminate the need for the model to use a

fitting parameter. This would also answer the question of whether it is justifiable to use the same effective channel length in both uniform and non-uniform substrate simulations, as was discussed in Section 5.2.

There are more questions that are associated with the non-uniform substrate simulation. These have to do with the approximation that sets the substrate doping to the doping level of the lateral strip in question. Since the values of R_s , R_d and ΔL are all dependent upon the substrate doping, it would be interesting to discover how accurate the depletion layer widths and barrier lowering produced by this approximation are. This could be done by comparing the values produced by the model and those generated by a MINIMOS simulation.

In Section 5.1 a question was raised about the use of the scatter-limited velocity in the punchthrough current density equation. It was suggested that an effective velocity which depends on device parameters and bias conditions might produce better agreement between measured and simulated results. It might also be possible to use a polynomial or exponential function for the velocity where the coefficients could be used as fitting parameters. This too is an area for additional study.

It is hoped that further research will yield the solutions to all these unanswered questions.

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APPENDIX A

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FILE: UNISUB FORTRAN A BELL-NORTHERN RESEAPCH

```

        DIMENSION JPT(300)
        DOUBLE PRECISION RDBL
        REAL NS,NB,NI,LG,LE,L,M,IPT,LP,LS,NT,NTT,JPT,K
        DATA NS,NB,NI,FJ,W/5.E19,1.E15,1.5E10,.68E-4,5.E-3/
        DATA K,T,Q,W/1.380622E-23,300.,1.6021917E-19,1.0359414E-12/
        DATA VSE,VSH/1.E7,6.E6/
        WRITE(6,600)
600    FORMAT ( , ' IS THE DEVICE N OF P-CHANNEL?')
        WRITE(6,610)
610    FORMAT ( , ' TYPE 1 FOR N-CHANNEL AND 2 FOR P-CHANNEL')
        READ(6,*) IPN
        IF (IPN.EQ.1.OR.IPN.EQ.2) GO TO 210
        WRITE(6,625)
625    FORMAT ( , ' INPUT ERROR')
        GO TO 300
        IF (IPN.EQ.2) GO TO 220
        WRITE(1,630)
        WRITE(2,630)
630    FORMAT ( , ' N-CHANNEL DEVICE')
        GO TO 230
        IF (IPN.EQ.1) SIGN=1.0
        IF (IPN.EQ.2) SIGN=-1.0
        IF (IPN.EQ.1) VS=VSE
        IF (IPN.EQ.2) VS=VSH
        WRITE(6,620)
620    FORMAT ( , ' INPUT THE CHANNEL LENGTH IN CENTIMETERS')
        READ(6,*) LE
        WRITE(1,650) LE
        WRITE(2,650) LE
650    FORMAT ( , ' CHANNEL LENGTH=',E8.3)
        WRITE(6,667)
667    FORMAT ( , ' TYPE 1 FOR A DATA RECORD AND 2 FOR NO DATA RECORD')
        READ(6,*) IWET
        VT=K*T/Q
        DX=1.E-6
        LG=LE+2.*RJ
        PB=VT*ALOG (NB*NS/NI**2)
        M=Q*NB/E
        VDS=-.5
        CALL FGGEN (RDBL,FJ,M,PB,0.0)
        PS=SNGL(RDBL)

C
C CALCULATE DLS
C
        RDS=SQRT (LG**2+PS**2-2.*LG*SQRT (RS**2-FJ**2))
        VDSS=M/2.*(RDS**2*ALOG (EDS/FJ) + (FJ**2-RDS**2)/2.)-PB
        A=M/R.
        B=VDSS/2.+PB
        C=VDSS**2/(2.*M)
        LP=SQRT ((B+SQRT (B**2-4.*A*C))/(2.*A))
        DLS=LP-LG
        WRITE(1,460) DLS
    
```

FILE: UNISUB PORTPAN A BELL-NORTHERN RESEARCH

460 FORMAT (, ' DL AT S=PJ IS ', E10.4)

WRITE(2,485)

485 FORMAT (, 2X, 'VDS', 7X, 'IPT')

C

C LOOP

C

DO 5 I=1,51

VDS=VDS+.5

CALL PGGEN (RDBL,RJ,M,PB,VDS)

RD=SMGL(RDBL)

C

C EXCESSIVELY HIGH VDS CHECK

C

RDMAX=SQRT(FS**2+LG**2)

IF (PD.LT.RDMAX) GO TO 95

S=ES

GO TO 110

C

C PUNCHTHROUGH CHECK

C

95 TEST=RS+RD

IF (TEST.GT.LG) GO TO 100

IPT=0.0

GO TO 200

100

S=SQRT(RD**2-((LG**2+RD**2-FS**2)/(2.*LG))**2)

DX2=2.*DX

IF (S.GE.DX2) GO TO 110

IPT=0.0

GO TO 200

C

C FIND THE NUMBER OF POINTS FOR FINITE DIFFERENCE ANALYSIS

C

110 IF (S.LE.RJ) D=S

IF (S.GT.RJ) D=RJ

NM1=AIN(T(D/DX)

N=NM1+1

C

C CALCULATE THE POTENTIAL MINIMA

C

WRITE(1,490) VDS,S

490

FORMAT (, ' VDS=', F4.1, 2X, 'S=', E10.4)

WRITE(1,500)

500

FORMAT (, 5X, 'X', 7X, 'PBL', 7X, 'JPT', 10X, 'L', 10X, 'NT', 6X, 'MODEL')

IF (S.GE.RJ) GO TO 120

B=VDS/2.*PB

C=VDS**2/(2.*M)

LP=SQRT((B+SQRT(B**2-4.*A*C))/2.*A)

LS=LG-2.*SQRT(RJ**2-S**2)

DL=LP-LS

GO TO 130

120

DL=DLS

130

X=-DX

DO 10 J=1,N

X=X+DX

L=LG-2.*SQRT(RJ**2-X**2)+DL

FILE: UNISUB FORTAN A BELL-NORTHERN RESEARCH

```

      IF (L.GT.0.0) GO TO 150
140  * WRITE(1,520)
      WRITE(2,520)
      WRITE(6,520)
520  FORMAT ( ' VOLTAGE LIMIT OF PUNCTHROUGH MODEL EXCEEDED' )
      GO TO 300
150  PBL=.4
      PBLT=.4
      DO 12 I1=1,20
      NT=.4.*E/Q/L**2*(VDS/2.+PB-PBL+SQRT(VDS*(PB-PBL)+(PB-PBL)**2))
      IF (NT.LE.NB) GO TO 170
      IF (NT.GE.NS) GO TO 140
      PBL=VT*ALOG(NB/NI**2*(NT-NB))
      FF=ABS(4*(PBL-PBLT)/PBLT)
      IF (FF.LE.1.E-5) GO TO 160
12   PBLT=PBL
160  MODL=1
      JPT(J)=Q*NI**2*VS/NB*EXP(PBL/VT)
      GO TO 180
170  MODL=2
      PBL=VDS/2.+PB-VDS**2*E/(2.*Q*L**2*NB)-L**2*Q*NB/(8.*E)
      JPT(J)=Q*NI**2*VS/NB*EXP(PBL/VT)
180  IF (IWPT.EQ.2) GO TO 10
      IF (NT.LT.NB) NT=NB
      PBL=SIGN*PBL
      JPT(J)=SIGN*JPT(J)
      WRITE(1,510) X,PBL,JPT(J),L,NT,MODL
510  FORMAT ( ,1X,E8.3,2X,F6.4,2X,E10.4,2X,E10.4,2X,E10.4,4X,I1)
10   CONTINUE
C
C SIMPSON'S RULE NUMERICAL INTEGRATION
C
190  IPT=0.0
      DO 15 J=2,NM1,2
15   IPT=IPT+DX/3.*W*(JPT(J-1)+4.*JPT(J)+JPT(J+1))
200  VDST=SIGN*VDS
      IPT=SIGN*IPT
      WRITE(2,520) VDST,IPT
530  FORMAT ( ,1X,F5.1,2X,E10.4)
5    CONTINUE
C
C END LOOP
C
300  STOP
      END
C
C SUBROUTINE TO GENERATE IS AND RD
C
      SUBROUTINE FGGEN (F,IJ,M,PB,VA)
      DOUBLE PRECISION R,FJ,I,PB,VA,FT,FF
      R=FJ+1.0E-5
      RT=R
      DO 10 I=1,30
      P=DSQRT(((R**2-FJ**2)/2.+2./M*(PB+VA))/DLOG(R/FJ))
      FF=DABS((F-FT)/FT)

```

FILE: UNISUB PORTPAN A BELL-NORTHERN RESEARCH

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10 IF (FR.LE.1.E-6) GO TO 100
100 RT=R
 RETURN
 END

APPENDIX B

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FILE: NONUNI FORTRAN A BELL-NORTHERN RESEARCH

```

      DIMENSION JPT(300)
      DOUBLE PRECISION RDBL
      REAL NS,NB,NI, LG,LE,L,LP,LS,M,JPT,IPT,NT,NTT,K
      DATA NS,NB,NI,VSE,VSH/1.5E20,1.03E-4,5.E-3,1.5E10,1.E7,6.E6/
      DATA K,T,Q,E/1.380622E-23,300.,1.6021917E-19,1.0359414E-12/
      DATA CS,AL,CI,XM,BE,CB/1.E17,.1E-4,1.E17,.5E-4,.1E-4,1.05E16/
      SD(X)=CS*EXP(-X**2/AL**2)+CI*EXP(-(X-XM)**2/BE**2)+CB
C
C NOTE THAT CB MUST BE POSITIVE FOR BOTH N- AND P-CHANNEL DEVICES.
C A CHANGE IN DOPING TYPE IS INDICATED BY A NEGATIVE DOPING
C CONCENTRATION.
C
      WRITE(6,500)
500  FORMAT ( , ' IS THE DEVICE N OF P-CHANNEL?')
      WRITE(6,510)
510  FORMAT ( , ' TYPE 1 FOR N-CHANNEL AND 2 FOR P-CHANNEL')
      READ(6,*) IPN
      IF (IPN.EQ.1.OF.IPN.EQ.2) GO TO 90
      WRITE(6,525)
525  FORMAT ( , ' INPUT EKEOF')
      GO TO 300
90   IF (IPN.EQ.2) GO TO 100
      WRITE(1,530)
      WRITE(2,530)
530  FORMAT ( , ' N-CHANNEL DEVICE')
      GO TO 110
100  WRITE(1,540)
      WRITE(2,540)
540  FORMAT ( , ' P-CHANNEL DEVICE')
110  IF (IPN.EQ.1) VS=VSE
      IF (IPN.EQ.2) VS=VSH
      IF (IPN.EQ.1) SIGN=1.0
      IF (IPN.EQ.2) SIGN=-1.0
      WRITE(6,520)
520  FORMAT ( , ' INPUT THE CHANNEL LENGTH IN CENTIMETERS')
      READ(6,*) LE
      WRITE(1,550) LE
      WRITE(2,550) LE
550  FORMAT ( , ' CHANNEL LENGTH=',E8.3)
      WRITE(6,567)
567  FORMAT ( , ' TYPE 1 FOR A DATA RECORD AND 2 FOR NO DATA RECORD')
      READ(6,*) IWST
      VT=K*T/Q
      DX=1.E-6
      LG=LE+2.*FJ
      WRITE(2,570)
570  FORMAT ( , 2X, 'VDS', 7X, 'IPT')
      VDS=-.5
C
C LOOP
C
      DO 5 I=1,27
      VDS=VDS+.5
C
C UNIFORM SUBSTRATE PUNCHTHROUGH CHECK

```

FILE: NONUNI FORTFAN A BELL-NORTHFEN RESEARCH

C

```

M=Q*CB/E
PB=VT*ALOG(NS*CB/NI**2)
CALL RGGEN (FDBL,RJ,M,PB,0.0)
RS=SNGL(FDBL)
CALL RGGEN (FDBL,RJ,M,PB,VDS)
RD=SNGL(RDBL)
TEST=RS+RD
IF (TEST.GT.LG) GO TO 80
IPT=0.0
GO TO 290

```

C

C FIND THE NUMBER OF POINTS FOR FINITE DIFFERENCE ANALYSIS

C

```

80  RDMAX=SQRT(PS**2+LG**2)
    IF (FD.GE.RDMAX) S=FS
    IF (RD.LT.RDMAX) S=SQRT(RD**2-((LG**2+RD**2-PS**2)/(2.*LG))**2)
    IF (S.LE.FJ) D=S
    IF (S.GT.FJ) D=FJ
    NM1=AIN(T(D/DX))
    N=NM1+1
    WRITE(1,590) VDS
590  FORMAT ( , ' VDS=',F4.1)
    WRITE(1,600)
600  FORMAT ( ,5X,'X',7X,'PBL',7X,'JPT',10X,'L',10X,'NT',6X,'MODEL')
    X=-DX
    DO 10 J=1,N
    X=X+DX

```

C

C FIND THE SUBSTRATE DOPING AT DEPTH X AND MAKE SURE THAT IT
C IS WITHIN REASONABLE LIMITS

C

```

NB=SD(X)
TEST1=NS/10.0
IF (NB.LT.TEST1) GO TO 130
WRITE(6,580)
580  FORMAT ( , ' SUBSTRATE DOPING TOO HIGH FOR MODEL')
PBL=0.0
JPT(J)=0.0
L=0.0
MODL=0
GO TO 280
130  TEST2=CB/10.0
    IF (NB.GT.TEST2) GO TO 135
    PBL=0.0
    JPT(J)=0.0
    L=0.0
    MODL=0
    GO TO 280
135  PB=VT*ALOG(NB*NS/NI**2)
    M=Q*NB/E

```

C

C CALCULATE FS AND FD

C

```

CALL RGGEN (FDBL,RJ,M,PB,0.0)

```

FILE: NONUNI-~~PORT~~TRAN A BELL-NORTHERN RESEARCH

```

      RS=SNGL(RDBL)
      CALL RGGEN (FDBL,RJ,M,PB,VDS)
      RD=SNGL(RDBL)

C
C EXCESSIVELY HIGH VDS CHECK
C
      RDMAX=SQRT (PS**2+LG**2)
      IF (PD.LT.PDMAX) GO TO 140
      S=RS
      GO TO 160

C
C PUNCHTHROUGH CHECK
C
140   TEST=SQRT (PS**2-X**2) +SQRT (PD**2-X**2)
      IF (TEST.GT.LG) GO TO 150
      PBL=0.0
      JPT(J)=0.0
      L=0.0
      MODL=0
      GO TO 280
150   S=SQRT (RD**2-((LG**2+PD**2-RS**2)/(2.*LG))**2)
C
C CALCULATE THE LENGTH CORRECTION TERM
C
160   IF (S.LT.FJ) GO TO 170
      RDS=SQRT (LG**2+RS**2-2.*LG*SQRT (PS**2-FJ**2))
      VDSS=M/2.*(RDS**2*ALOG (RDS/FJ) + (RJ**2-RDS**2)/2.)-PB
      A=M/8.
      B=VDSS/2.+PB
      C=VDSS**2/(2.*M)
      LP=SQRT ((B+SQRT (B**2-4.*A*C))/(2.*A))
      DL=LP-LG
      GO TO 180
170   A=M/8.
      B=VDS/2.+PB
      C=VDS**2/(2.*M)
      LP=SQRT ((B+SQRT (B**2-4.*A*C))/(2.*A))
      LS=LG-2.*SQRT (FJ**2-S**2)
      DL=LP-LS
180   L=LG-2.*SQRT (FJ**2-X**2)+DL
      IF (L.GT.0.0) GO TO 200
190   WRITE(1,610)
      WRITE(2,610)
      WRITE(6,610)
610   FORMAT (,' VOLTAGE LIMIT OF PUNCHTHROUGH MODEL EXCEEDED')
      GO TO 300

C
C CALCULATE THE POTENTIAL MINIMUM AND CURRENT DENSITY
C
200   PBL=.4
      PBLT=.4
      DO 15 I1=1,20
      NT=4.*E/Q/L**2*(VDS/2.+PB-PBL+SQRT (VDS*(PB-PBL)+(PB-PBL)**2))
      IF (NT.LE.NB) GO TO 220
      IF (NT.GE.NS) GO TO 190

```

FILE: NONUNI POETAN A BELL-NORTHERN RESEARCH

```

PBL=VT*ALOG(NB/NI**2*(NT-NB))
PF=ABS((PBL-PBLT)/PBLT)
IF (PR.LE.1.E-5) GO TO 210
15  PBLT=PBL
210  MODL=1
      JPT(J)=Q*NI**2*VS/NB*EXP(PBL/VT)
      GO TO 280
220  MODL=2
      PBL=VDS/2.+PB-VDS**2*E/(2.*Q*L**2*NB)-L**2*Q*NB/(8.*E)
      JPT(J)=Q*NI**2*VS/NB*EXP(PBL/VT)
280  IF (IWRT.EQ.2) GO TO 10
      IF (NT.LT.CB) NT=CB
      PBL=SIGN*PBL
      JPT(J)=SIGN*JPT(J)
      WRITE(1,620) X,PBL,JPT(J),L,NT,MODL
620  FORMAT ( ,1X,E8.3,2X,F6.4,2X,E10.4,2X,E10.4,2X,E10.4,4X,I1)
10   CONTINUE
C
C SIMPSON'S RULE NUMERICAL INTEGRATION
C
285  IPT=0.0
      DO 20 J=2,NM1,2
20   LPT=IPT+DX/3.*((JPT(J-1)+4.*JPT(J)+JPT(J+1)))
290  VDST=SIGN*VDS
      IPT=SIGN*IPT
      WRITE(2,630) VDST,IPT
630  FORMAT ( ,1X,F5.1,2X,E10.4)
5    CONTINUE
C
C END LOOP
C
300  STOP
      END
C
C SUBROUTINE TO GENERATE FS AND FD
C
SUBROUTINE PGGEN (R,RJ,M,PB,VA)
DOUBLE PRECISION R,RJ,M,PB,VA,FT,FF
R=RJ+1.0E-5
RT=P
DO 10 I=1,30
R=DSQRT(((P**2-RJ**2)/2.+2./M*(PB+VA))/DLOG(R/RJ))
FF=DABS((F-RT)/RT)
IF (FF.LE.1.E-6) GO TO 100
10   RT=R
100  RETURN
      END

```

APPENDIX C

PAGE 112

FILE: UNISUB DATA A BELL-NORTHERN RESEAPCH

N-CHANNEL DEVICE
CHANNEL LENGTH=720E-04

VDS IPT

0.0	0.0
0.5	0.1704E-14
1.0	0.6092E-10
1.5	0.4255E-06
2.0	0.1599E-03
2.5	0.5343E-03
3.0	0.1161E-02
3.5	0.2016E-02
4.0	0.3084E-02
4.5	0.4394E-02
5.0	0.5964E-02
5.5	0.7879E-02
6.0	0.1023E-01
6.5	0.1311E-01
7.0	0.1676E-01
7.5	0.2147E-01
8.0	0.2775E-01
8.5	0.3650E-01
9.0	0.4948E-01
9.5	0.7051E-01
10.0	0.1097E+00
10.5	0.2039E+00
11.0	0.6276E+00

VOLTAGE LIMIT OF PUNCHTHROUGH MODEL EXCEEDED

APPENDIX D

PAGE 113

FILE: UNISUB DATA A BELL-NORTHERN RESEARCH

N-CHANNEL DEVICE

CHANNEL LENGTH=.720E-04

DL AT S=PJ IS -.1153E-03

VDS= 2.0 S=0.4830E-04

X	PBL	JPT	L	NT	MODEL
.0	0.6305	0.1344E+04	0.7024E-04	0.1134E+17	1
.100E-05	0.6305	0.1341E+04	0.7025E-04	0.1134E+17	1
.200E-05	0.6303	0.1330E+04	0.7028E-04	0.1133E+17	1
.300E-05	0.6299	0.1312E+04	0.7033E-04	0.1132E+17	1
.400E-05	0.6294	0.1297E+04	0.7039E-04	0.1130E+17	1
.500E-05	0.6288	0.1256E+04	0.7048E-04	0.1128E+17	1
.600E-05	0.6280	0.1218E+04	0.7059E-04	0.1126E+17	1
.700E-05	0.6270	0.1174E+04	0.7072E-04	0.1123E+17	1
.800E-05	0.6259	0.1123E+04	0.7086E-04	0.1120E+17	1
.900E-05	0.6246	0.1067E+04	0.7103E-04	0.1117E+17	1
.100E-04	0.6230	0.1006E+04	0.7121E-04	0.1113E+17	1
.110E-04	0.6213	0.9399E+03	0.7142E-04	0.1109E+17	1
.120E-04	0.6613	0.4428E+04	0.7164E-04	0.1050E+17	2
.130E-04	0.6559	0.3580E+04	0.7189E-04	0.1050E+17	2
.140E-04	0.6499	0.2840E+04	0.7215E-04	0.1050E+17	2
.150E-04	0.6434	0.2209E+04	0.7244E-04	0.1050E+17	2
.160E-04	0.6364	0.1694E+04	0.7274E-04	0.1050E+17	2
.170E-04	0.6288	0.1258E+04	0.7306E-04	0.1050E+17	2
.180E-04	0.6207	0.9200E+03	0.7341E-04	0.1050E+17	-2
.190E-04	0.6121	0.6583E+03	0.7377E-04	0.1050E+17	2
.200E-04	0.6029	0.4606E+03	0.7416E-04	0.1050E+17	2
.210E-04	0.5930	0.3149E+03	0.7457E-04	0.1050E+17	2
.220E-04	0.5826	0.2102E+03	0.7499E-04	0.1050E+17	2
.230E-04	0.5715	0.1369E+03	0.7544E-04	0.1050E+17	2
.240E-04	0.5598	0.8698E+02	0.7591E-04	0.1050E+17	2
.250E-04	0.5473	0.5381E+02	0.7640E-04	0.1050E+17	2
.260E-04	0.5342	0.3241E+02	0.7691E-04	0.1050E+17	2
.270E-04	0.5204	0.1998E+02	0.7744E-04	0.1050E+17	2
.280E-04	0.5058	0.1080E+02	0.7800E-04	0.1050E+17	2
.290E-04	0.4905	0.5965E+01	0.7857E-04	0.1050E+17	2
.300E-04	0.4743	0.3195E+01	0.7917E-04	0.1050E+17	2
.310E-04	0.4574	0.1657E+01	0.7979E-04	0.1050E+17	2
.320E-04	0.4396	0.8319E+00	0.8043E-04	0.1050E+17	2
.330E-04	0.4209	0.4036E+00	0.8110E-04	0.1050E+17	2
.340E-04	0.4012	0.1890E+00	0.8179E-04	0.1050E+17	2
.350E-04	0.3807	0.8537E-01	0.8250E-04	0.1050E+17	2
.360E-04	0.3592	0.3713E-01	0.8323E-04	0.1050E+17	2
.370E-04	0.3366	0.1553E-01	0.8399E-04	0.1050E+17	2
.380E-04	0.3131	0.6238E-02	0.8477E-04	0.1050E+17	2
.390E-04	0.2884	0.2404E-02	0.8558E-04	0.1050E+17	2
.400E-04	0.2626	0.8967E-03	0.8641E-04	0.1050E+17	2
.410E-04	0.2357	0.3128E-03	0.8726E-04	0.1050E+17	2
.420E-04	0.2076	0.1053E-03	0.8814E-04	0.1050E+17	2
.430E-04	0.1782	0.3381E-04	0.8905E-04	0.1050E+17	2
.440E-04	0.1475	0.1033E-04	0.8998E-04	0.1050E+17	2
.450E-04	0.1155	0.2995E-05	0.9094E-04	0.1050E+17	2
.460E-04	0.0821	0.8232E-06	0.9192E-04	0.1050E+17	2
.470E-04	0.0410	0.2141E-06	0.9294E-04	0.1050E+17	2
.480E-04	0.0110	0.5258E-07	0.9399E-04	0.1050E+17	2
VDS= 6.0	S=0.7484E-04				

FILE: UNISUB DATA? A BELL-NORTHERN RESEARCH

X	PBI	JPT	L	NT	MODEL
.0	0.7259	0.5376E+05	0.5071E-04	0.4405E+17	1
.100E-05	0.7259	0.5373E+05	0.5072E-04	0.4404E+17	1
.200E-05	0.7258	0.5366E+05	0.5074E-04	0.4399E+17	1
.300E-05	0.7258	0.5352E+05	0.5079E-04	0.4391E+17	1
.400E-05	0.7257	0.5334E+05	0.5086E-04	0.4379E+17	1
.500E-05	0.7256	0.5311E+05	0.5095E-04	0.4365E+17	1
.600E-05	0.7254	0.5282E+05	0.5106E-04	0.4347E+17	1
.700E-05	0.7253	0.5249E+05	0.5118E-04	0.4326E+17	1
.800E-05	0.7251	0.5211E+05	0.5133E-04	0.4302E+17	1
.900E-05	0.7249	0.5164E+05	0.5149E-04	0.4275E+17	1
.100E-04	0.7246	0.5120E+05	0.5168E-04	0.4246E+17	1
.110E-04	0.7244	0.5068E+05	0.5188E-04	0.4213E+17	1
.120E-04	0.7241	0.5012E+05	0.5211E-04	0.4178E+17	1
.130E-04	0.7238	0.4951E+05	0.5235E-04	0.4140E+17	1
.140E-04	0.7234	0.4886E+05	0.5262E-04	0.4100E+17	1
.150E-04	0.7231	0.4818E+05	0.5290E-04	0.4057E+17	1
.160E-04	0.7227	0.4746E+05	0.5321E-04	0.4012E+17	1
.170E-04	0.7223	0.4670E+05	0.5353E-04	0.3965E+17	1
.180E-04	0.7218	0.4592E+05	0.5388E-04	0.3916E+17	1
.190E-04	0.7213	0.4510E+05	0.5424E-04	0.3865E+17	1
.200E-04	0.7209	0.4425E+05	0.5463E-04	0.3812E+17	1
.210E-04	0.7203	0.4338E+05	0.5503E-04	0.3758E+17	1
.220E-04	0.7198	0.4249E+05	0.5546E-04	0.3702E+17	1
.230E-04	0.7192	0.4157E+05	0.5591E-04	0.3644E+17	1
.240E-04	0.7186	0.4063E+05	0.5638E-04	0.3586E+17	1
.250E-04	0.7180	0.3967E+05	0.5687E-04	0.3526E+17	1
.260E-04	0.7174	0.3870E+05	0.5738E-04	0.3466E+17	1
.270E-04	0.7167	0.3772E+05	0.5791E-04	0.3404E+17	1
.280E-04	0.7160	0.3672E+05	0.5846E-04	0.3342E+17	1
.290E-04	0.7153	0.3571E+05	0.5904E-04	0.3279E+17	1
.300E-04	0.7146	0.3469E+05	0.5964E-04	0.3216E+17	1
.310E-04	0.7138	0.3367E+05	0.6026E-04	0.3152E+17	1
.320E-04	0.7130	0.3265E+05	0.6090E-04	0.3088E+17	1
.330E-04	0.7122	0.3162E+05	0.6156E-04	0.3023E+17	1
.340E-04	0.7113	0.3059E+05	0.6225E-04	0.2959E+17	1
.350E-04	0.7104	0.2956E+05	0.6296E-04	0.2895E+17	1
.360E-04	0.7095	0.2853E+05	0.6370E-04	0.2831E+17	1
.370E-04	0.7086	0.2750E+05	0.6446E-04	0.2767E+17	1
.380E-04	0.7076	0.2648E+05	0.6524E-04	0.2703E+17	1
.390E-04	0.7066	0.2547E+05	0.6604E-04	0.2639E+17	1
.400E-04	0.7055	0.2446E+05	0.6687E-04	0.2576E+17	1
.410E-04	0.7044	0.2346E+05	0.6773E-04	0.2514E+17	1
.420E-04	0.7033	0.2246E+05	0.6861E-04	0.2452E+17	1
.430E-04	0.7022	0.2146E+05	0.6952E-04	0.2391E+17	1
.440E-04	0.7010	0.2051E+05	0.7045E-04	0.2330E+17	1
.450E-04	0.6997	0.1955E+05	0.7141E-04	0.2271E+17	1
.460E-04	0.6985	0.1861E+05	0.7239E-04	0.2211E+17	1
.470E-04	0.6971	0.1768E+05	0.7340E-04	0.2153E+17	1
.480E-04	0.6958	0.1676E+05	0.7444E-04	0.2096E+17	1
.490E-04	0.6943	0.1585E+05	0.7551E-04	0.2039E+17	1
.500E-04	0.6928	0.1496E+05	0.7661E-04	0.1984E+17	1
.510E-04	0.6913	0.1409E+05	0.7773E-04	0.1929E+17	1
.520E-04	0.6896	0.1323E+05	0.7889E-04	0.1876E+17	1
.530E-04	0.6879	0.1238E+05	0.8007E-04	0.1823E+17	1

FILE: UNISUB DATA? A BELL-NORTHERN RESEARCH

.540E-04	0.6861	0.1156E+05	0.8129E-04	0.1771E+17	1
.550E-04	0.6843	0.1075E+05	0.8253E-04	0.1721E+17	1
.560E-04	0.6823	0.9352E+04	0.8381E-04	0.1671E+17	1
.570E-04	0.6802	0.9175E+04	0.8512E-04	0.1623E+17	1
.580E-04	0.6780	0.8416E+04	0.8647E-04	0.1575E+17	1
.590E-04	0.6756	0.7675E+04	0.8785E-04	0.1529E+17	1
.600E-04	0.6730	0.6951E+04	0.8927E-04	0.1484E+17	1
.610E-04	0.6702	0.6245E+04	0.9072E-04	0.1440E+17	1
.620E-04	0.6672	0.5557E+04	0.9221E-04	0.1397E+17	1
.630E-04	0.6639	0.4889E+04	0.9373E-04	0.1355E+17	1
.640E-04	0.6602	0.4239E+04	0.9530E-04	0.1315E+17	1
.650E-04	0.6561	0.3610E+04	0.9691E-04	0.1275E+17	1
.660E-04	0.6513	0.3002E+04	0.9855E-04	0.1237E+17	1
.670E-04	0.6457	0.2418E+04	0.1002E-03	0.1201E+17	1
.680E-04	0.6393	0.1861E+04	0.1020E-03	0.1166E+17	1
.690E-04	0.6304	0.1336E+04	0.1038E-03	0.1133E+17	1
.700E-04	0.6188	0.8553E+03	0.1056E-03	0.1103E+17	1
.710E-04	0.6390	0.1869E+04	0.1075E-03	0.1050E+17	2
.720E-04	0.5877	0.2562E+03	0.1094E-03	0.1050E+17	2
.730E-04	0.5315	0.2919E+02	0.1114E-03	0.1050E+17	2
.740E-04	0.4704	0.2741E+01	0.1134E-03	0.1050E+17	2
.750E-04	0.4040	0.2103E+00	0.1155E-03	0.1050E+17	2
.760E-04	0.3321	0.1305E-01	0.1177E-03	0.1050E+17	2
.770E-04	0.2545	0.6479E-02	0.1199E-03	0.1050E+17	2
.780E-04	0.1708	0.2545E-04	0.1222E-03	0.1050E+17	2
.790E-04	0.0807	0.7802E-06	0.1245E-03	0.1050E+17	2
VDS=10.0	S=0.9589F-04				
X	PBL	JPT	L	NT	MODEL
.0	0.7918	0.6889E+06	0.1937E-04	0.4405E+18	1
.100E-05	0.7918	0.6882E+06	0.1938E-04	0.4401E+18	1
.200E-05	0.7917	0.6862E+06	0.1941E-04	0.4388E+18	1
.300E-05	0.7916	0.6827E+06	0.1946E-04	0.4366E+18	1
.400E-05	0.7914	0.6780E+06	0.1953E-04	0.4337E+18	1
.500E-05	0.7912	0.6719E+06	0.1961E-04	0.4299E+18	1
.600E-05	0.7909	0.6646E+06	0.1972E-04	0.4253E+18	1
.700E-05	0.7906	0.6561E+06	0.1985E-04	0.4200E+18	1
.800E-05	0.7902	0.6465E+06	0.1999E-04	0.4141E+18	1
.900E-05	0.7893	0.6359E+06	0.2016E-04	0.4074E+18	1
.100E-04	0.7892	0.6243E+06	0.2034E-04	0.4002E+18	1
.110E-04	0.7888	0.6119E+06	0.2055E-04	0.3924E+18	1
.120E-04	0.7882	0.5986E+06	0.2077E-04	0.3841E+18	1
.130E-04	0.7876	0.5847E+06	0.2102E-04	0.3754E+18	1
.140E-04	0.7869	0.5701E+06	0.2128E-04	0.3663E+18	1
.150E-04	0.7862	0.5551E+06	0.2157E-04	0.3569E+18	1
.160E-04	0.7855	0.5396E+06	0.2187E-04	0.3473E+18	1
.170E-04	0.7847	0.5237E+06	0.2220E-04	0.3374E+18	1
.180E-04	0.7839	0.5077E+06	0.2254E-04	0.3274E+18	1
.190E-04	0.7831	0.4914E+06	0.2291E-04	0.3172E+18	1
.200E-04	0.7822	0.4751E+06	0.2329E-04	0.3070E+18	1
.210E-04	0.7813	0.4587E+06	0.2370E-04	0.2968E+18	1
.220E-04	0.7804	0.4423E+06	0.2412E-04	0.2866E+18	1
.230E-04	0.7794	0.4261E+06	0.2457E-04	0.2764E+18	1
.240E-04	0.7784	0.4100E+06	0.2504E-04	0.2664E+18	1
.250E-04	0.7774	0.3941E+06	0.2553E-04	0.2565E+18	1
.260E-04	0.7763	0.3784E+06	0.2604E-04	0.2467E+18	1

FILE: UNISUB DATA A BELL-NORTHERN RESEARCH

.270E-04	0.7753	0.3631E+06	0.2657E-04	0.2371E+18	1
.280E-04	0.7742	0.3480E+06	0.2713E-04	0.2277E+18	1
.290E-04	0.7731	0.3333E+06	0.2770E-04	0.2185E+18	1
.300E-04	0.7719	0.3190E+06	0.2830E-04	0.2096E+18	1
.310E-04	0.7708	0.3050E+06	0.2892E-04	0.2009E+18	1
.320E-04	0.7696	0.2914E+06	0.2956E-04	0.1924E+18	1
.330E-04	0.7684	0.2783E+06	0.3023E-04	0.1842E+18	1
.340E-04	0.7672	0.2656E+06	0.3092E-04	0.1763E+18	1
.350E-04	0.7660	0.2533E+06	0.3163E-04	0.1686E+18	1
.360E-04	0.7647	0.2414E+06	0.3236E-04	0.1612E+18	1
.370E-04	0.7635	0.2299E+06	0.3312E-04	0.1540E+18	1
.380E-04	0.7622	0.2189E+06	0.3390E-04	0.1471E+18	1
.390E-04	0.7609	0.2083E+06	0.3471E-04	0.1405E+18	1
.400E-04	0.7596	0.1981E+06	0.3554E-04	0.1341E+18	1
.410E-04	0.7583	0.1883E+06	0.3639E-04	0.1280E+18	1
.420E-04	0.7570	0.1789E+06	0.3727E-04	0.1222E+18	1
.430E-04	0.7556	0.1699E+06	0.3818E-04	0.1166E+18	1
.440E-04	0.7543	0.1613E+06	0.3911E-04	0.1112E+18	1
.450E-04	0.7529	0.1530E+06	0.4007E-04	0.1060E+18	1
.460E-04	0.7516	0.1452E+06	0.4106E-04	0.1011E+18	1
.470E-04	0.7502	0.1376E+06	0.4207E-04	0.9639E+17	1
.480E-04	0.7488	0.1304E+06	0.4311E-04	0.9189E+17	1
.490E-04	0.7474	0.1235E+06	0.4417E-04	0.8759E+17	1
.500E-04	0.7460	0.1169E+06	0.4527E-04	0.8348E+17	1
.510E-04	0.7445	0.1106E+06	0.4640E-04	0.7956E+17	1
.520E-04	0.7431	0.1047E+06	0.4755E-04	0.7582E+17	1
.530E-04	0.7417	0.9894E+05	0.4874E-04	0.7225E+17	1
.540E-04	0.7402	0.9348E+05	0.4995E-04	0.6885E+17	1
.550E-04	0.7387	0.8828E+05	0.5120E-04	0.6560E+17	1
.560E-04	0.7372	0.8332E+05	0.5248E-04	0.6251E+17	1
.570E-04	0.7357	0.7860E+05	0.5379E-04	0.5955E+17	1
.580E-04	0.7342	0.7409E+05	0.5514E-04	0.5674E+17	1
.590E-04	0.7326	0.6980E+05	0.5652E-04	0.5406E+17	1
.600E-04	0.7311	0.6570E+05	0.5793E-04	0.5151E+17	1
.610E-04	0.7295	0.6180E+05	0.5938E-04	0.4907E+17	1
.620E-04	0.7279	0.5808E+05	0.6087E-04	0.4675E+17	1
.630E-04	0.7263	0.5454E+05	0.6240E-04	0.4454E+17	1
.640E-04	0.7246	0.5117E+05	0.6396E-04	0.4244E+17	1
.650E-04	0.7229	0.4795E+05	0.6557E-04	0.4043E+17	1
.660E-04	0.7212	0.4488E+05	0.6722E-04	0.3851E+17	1
.670E-04	0.7195	0.4196E+05	0.6891E-04	0.3669E+17	1
.680E-04	0.7177	0.3917E+05	0.7064E-04	0.3495E+17	1
.690E-04	0.7159	0.3651E+05	0.7243E-04	0.3329E+17	1
.700E-04	0.7140	0.3398E+05	0.7425E-04	0.3171E+17	1
.710E-04	0.7121	0.3157E+05	0.7613E-04	0.3020E+17	1
.720E-04	0.7102	0.2926E+05	0.7806E-04	0.2876E+17	1
.730E-04	0.7081	0.2707E+05	0.8004E-04	0.2739E+17	1
.740E-04	0.7061	0.2497E+05	0.8208E-04	0.2609E+17	1
.750E-04	0.7039	0.2297E+05	0.8417E-04	0.2484E+17	1
.760E-04	0.7017	0.2106E+05	0.8633E-04	0.2365E+17	1
.770E-04	0.6993	0.1924E+05	0.8855E-04	0.2251E+17	1
.780E-04	0.6969	0.1750E+05	0.9083E-04	0.2142E+17	1
.790E-04	0.6943	0.1584E+05	0.9319E-04	0.2039E+17	1
.800E-04	0.6916	0.1426E+05	0.9562E-04	0.1940E+17	1
.810E-04	0.6887	0.1274E+05	0.9812E-04	0.1845E+17	1

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.820E-04	0.6856	0.1130E+05	0.1007E-03	0.1755E+17	1
.830E-04	0.6822	0.9917E+04	0.1034E-03	0.1669E+17	1
.840E-04	0.6785	0.8597E+04	0.1062E-03	0.1587E+17	1
.850E-04	0.6744	0.7336E+04	0.1090E-03	0.1508E+17	1
.860E-04	0.6698	0.6132E+04	0.1120E-03	0.1433E+17	1
.870E-04	0.6644	0.4984E+04	0.1151E-03	0.1361E+17	1
.880E-04	0.6580	0.3890E+04	0.1183E-03	0.1293E+17	1
.890E-04	0.6500	0.2854E+04	0.1217E-03	0.1228E+17	1
.900E-04	0.6392	0.1880E+04	0.1252E-03	0.1167E+17	1
.910E-04	0.6225	0.9905E+03	0.1289E-03	0.1112E+17	1
.920E-04	0.6190	0.8620E+03	0.1327E-03	0.1050E+17	2
.930E-04	0.4983	0.8079E+01	0.1368E-03	0.1050E+17	2
.940E-04	0.3534	0.2965E-01	0.1412E-03	0.1050E+17	2
.950E-04	0.1809	0.3752E-04	0.1458E-03	0.1050E+17	2

END

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FIN