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**Design of a CMOS Decision Feedback
Equalizer for High Speed Backplane Transceiver**

By

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Bachelor of Science

A thesis submitted to the Faculty of Graduate Studies and Research

in partial fulfillment of the requirements for the degree of

Master of Applied Science

Department of Electronics

Carleton University

Ottawa, Ontario, Canada

May 2005

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The information used in this thesis comes in part from the research program of Dr. Tad Kwasniewski and his associates in the VLSI in Communications group. The research results appearing in this thesis represent an integral part of the ongoing research program. All research results in this thesis including tables, graphs and figures but excluding the narrative portions of the thesis are effectively incorporated into the research program and can be used by Dr. Kwasniewski and his associates for educational and research purposes, including publication in open literature with appropriate credits. The matters of intellectual property may be pursued cooperatively with Carleton University and Dr. Kwasniewski, where and when appropriate.

Abstract

Increases in backplane data transfer rates are accompanied by worsening signal integrity problems, principally ones of channel attenuation, reflection and crosstalk. The collective effect of these appears as inter symbol interference (ISI), a major factor limiting transmission distance and speed.

Both linear and nonlinear equalizers use knowledge of a data stream's history to eliminate ISI effects, but the nonlinear ones are able to enhance the desired signal while not amplifying noise. Decision Feedback Equalization (DFE), a kind of nonlinear device, is one of the most effective means of dealing with the ISI problem.

A new half-rate pipelined multi-tap CMOS DFE structure is proposed in the present work. Starting from an initial circuit concept, a MATLAB behavioral model having fixed post-tap coefficients is constructed. The model is used to verify the design's functionality and to determine parameters needed for a transistor-level design.

The proposed DFE is composed of two pipelined signal paths with cross-coupled feedback in which linear equalizing amplifier circuits and phase detecting circuits are used to process the even- and odd-indexed bits of the data stream. The outputs of the two branches are then reintegrated to recover a data stream at the original rate. Since each branch only has to work at one-half of the incoming data rate, the new DFE is called a half-rate DFE, or HRDFE.

The design was verified by HSPICE simulation, with TSMC 0.18 μ m CMOS process parameters being assumed. The results of a post-layout simulation involving a 34 inch FR4 backplane demonstrate eye opening increases and acceptable BER at data rates at least as high as 8 gigabits per second. Only 12.2 milliWatts is consumed from a 1.8 Volt power supply.

Acknowledgements

This thesis would not have been possible without the encouragement, support and contributions of many people. In particular, I would like to express my deep gratitude and appreciation to my supervisor Prof. Tad Kwasniewski not only for providing an interesting topic, but also for the motivations when I needed them most, and many hours of inspiring discussions. Without professor's guidance and helpful suggestions, working on this thesis would have been much more difficult.

Colleagues, especially Miao Li, contributed many valuable ideas, comments and suggestions which are always welcome and appreciated; Their constructive criticism and helpful ideas were refreshing.

I would also like to express my gratitude to the students, professors and staff at the department of electronics for making my work such an enjoyable and stimulating experience.

I leave a special note to my mother and my sister, thank you for your unconditional love and trust. Without you, I would have not become what I am now. I believe your patience finally paid off.

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List of Abbreviations

AC	Alternating Current
ADC	Analog to Digital Conversion
ANSI	American National Standards Institute
ASIC	Application Specific Integrated Circuit
BER	Bit Error Rate
CDAC	Coefficient Digital to Analog Conversion
CDR	Clock Data Recovery
CMC	Canadian Microelectronics Corporation
CML	Current Mode Logic
CMOS	Complementary Metal Oxide Semiconductor
CMOSP18	0.18um CMOS Process provided by TSMC
DAC	Digital to Analog Conversion
DC	Direct Current
DEF	Design Exchange Format
DETFE	Dual Edge Triggered Flip Flop
DFE	Decision Feedback Equalizer
DFF	D-latch Flip Flop
DFT	Design For Testability
DRC	Design Rule Check
FBF	FeedBack Filter
FF	Flip Flop
FFF	FeedForward Filter
FIR	Finite Impulse Response
FR-4	Flame retardant version of the old G10 epoxy laminate with glass fibre reinforcement
FTF	Fast Transversal Filters
HDL	Hardware Description Language
HDSL	High Rate Digital Subscriber Lines
HSBI	High Speed Backplane Initiative
ISDN	Integrated Services Digital Network
ISI	Intersymbol Interference
LMS	Least Mean Square

LVS	Layout Versus Schematic
MMSE	Minimum Mean Squared Error
MSB	Most Significant Bit
MSE	Mean Square Error
MUX	Multiplexer
NEXT	Near-End Crosstalk
NRZ	Non Return to Zero
PAM	Pulse Amplitude Modulation
PCB	Printed Circuit Board
PDP	Physical Design Planner - a Cadence tool for digital layout
PRBS	Pseudo Random Binary Sequence
RLS	Recursive Least Square
RTL	Register Transfer Level
SD-LMS	Sign Data Least Mean Square
SE-LMS	Sign Error Least Mean Square
SERDES	Serializer/Deserializer
SNR	Signal to Noise Ratio
SS-LMS	Sign-Sign Least Mean Square
TF	Transversal Filter
T_{CQ}	Delay of DFF from clock to output Q
T_{mux}	Delay of Multiplexer
T_S	Delay of equalizer
TSMC	Taiwan Semiconductor Manufacturing Company
UTP	Unshielded Twisted Pair
VLSI	Very Large Scale Integration
XOR	Exclusive OR Gate
ZF	Zero Forcing

List of Symbols



0-Volt reference, Gnd



Supply voltage, Vdd



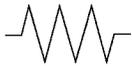
n-MOSFET transistor



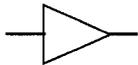
p-MOSFET transistor



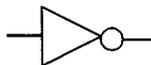
Capacitor



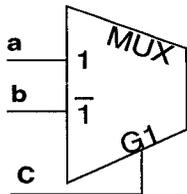
Resistor



Buffer



Inverter



2:1 Multiplexer

1.1 Research Motivation

Designers must devise methods to improve upon the present 3.125Gbit/s methods in their efforts to meet the demands presented by a trend toward higher transmission speeds. They must now deal with the requirements of 10Gbit/s rates, involving for example 25 – 30ps chip edge rates and correspondingly tighter constraints.

There are two approaches that can be taken. The replacement of entire systems is the most obvious one, but one which involves a great deal of time and expense. The other is to improve the performance of existing hardware. The latter is clearly the course of choice for manufacturers. In particular, speed-improvement efforts should be focused on the modules that communicate with one another over the backplane.

Larger systems are typically implemented as a set of functional blocks, modules, connected to one-another over a backplane and which communicate over standard interfaces. The physical form of the backplane may range from copper traces on a glass/epoxy substrate through to optical cables. The system of interest in this work consists of a number of transmitting and receiving elements linked together on a backplane. The most basic system, one which consists of two devices communicating with each other, is shown in Figure 1.1.

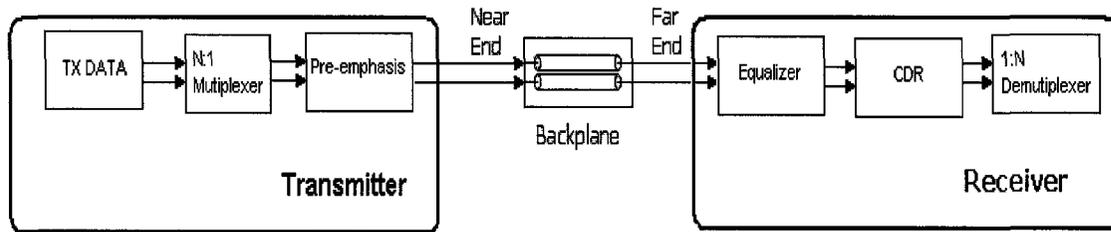


Figure 1.1: Simplified transceiver block diagram

For economic and other reasons, it is preferable to direct one's performance-improvement efforts at the system modules, and not at the backplane itself. This will involve the development of equalizers for compensating the speed-reducing characteristics of the backplane. A new half-rate Decision Feedback Equalizer (HRDFE) for doing this was the result of the research described in this thesis report.

One of the most important issues that must be addressed is that of inter-symbol interference (ISI). It would seem that the designers of the copper-based FR-4 backplanes used in today's communication systems gave this little consideration, especially not to the ISI effects which are important at speeds above 5 Gb/s and cause worsening crosstalk and reflections with increasing transmission rates, to the point that reliable data extraction is ultimately rendered impossible. In this work, the ISI problem is re-examined with the goal of finding a new and less costly means of dealing with it.

The system design of conventional transceivers has been extensively discussed in the literature [1-6].

One method of dealing with the ISI problem involves the insertion of an equalizer on the receiver side, it can be either analog or digital, and in either case the equalizers work with clock and data recovery circuit.

Analog equalizers are often used at rates greater than 3.125 Gb/s. The advantages of the analog approach include ease of implementation, low power consumption and more economical use of silicon area [7]. Signal compensation is the simplest way to higher transmission speeds, however, when an analog equalizer amplifies the signal it also amplifies the noise and crosstalk. These will decrease the BER seriously.

If it has been decided to use a digital equalizer, the input signal must first be converted to a digital format. The impulse response will have been corrected by a fixed equalizer before timing recovery is attempted [8-9]. At high speeds, the low-pass effects of backplane conductor capacitances and inductances lead to phase and amplitude distortions of the digital signals being conveyed, a process that must be compensated before the signal is sent to the digital circuits.

A class of baud-rate sampling and timing-recovery techniques has been proposed by Mueller and Muller [10]. Their method has two principal parts:

1. Selection of the timing phase control function suited to the impulse response.
2. Timing function estimation based on the arriving signal samples and detected data.

But in practise, the method of Mueller and Muller is beset by difficulties in estimating the timing function itself and its derivative.

Therefore, Jennings and Clarke [11] proposed an alternative method for performing these tasks, but one which requires a precise and stable master clock, something which is not always available.

The necessity of selecting an optimal timing phase can be relaxed by using a linear fractional spaced equalizer, as described in [12]. However, a fractional spaced equalizer requires two or more samples per baud period which limits the maximum achievable data rate. One method of overcoming this problem would be to use a baud rate or even half baud rate timing recovery receiver, which can be achieved by using Decision Feedback

Equalizer (DFE). In this research, we make use of DFE without employing feedforward filter (FFF), because at transmission speeds of interest and for the channel under study, only few equalizer precursor taps are necessary, and the number of taps is insensitive to the trace length and to the number of bridged-taps. Also the DFE-without-FFF has a major advantage, hardware simplicity.

1.2 Thesis Objective

The goal of this thesis is to continue with the work DFE-without-FFF described, and to develop a half-rate pipelined DFE circuit design which is capable of eliminating ISI problems at high speeds while consuming little power.

The design challenges which appear in high speed work will be analyzed in terms of equalization principles. The performance of a number of equalizer structures will be compared and evaluated. Limitations imposed by the transmission medium will be studied.

The design of a new DFE, one capable of dealing with the ISI problems outlined in section 1.1, will be developed, and then a MATLAB behavioral model of the device will be developed and used to verify its functionality before the actual hardware is built.

Pre-layout and post-layout simulation of a specific TSMC CMOS 0.18 μm technology implementation operating at backplane speeds of up to 8Gb/s will be carried out, and a BER estimation made.

1.3 Thesis Outline

The thesis follows the design flow chart of the IC circuits in Figure 1.2 [28].

Industry background is reviewed at the beginning of Chapter 2. Challenges of high-speed backplane design are discussed. Analysis of the problems that the high-speed

designer is confronted with and their solutions is done, as is an examination of transmission-medium limitations and linear equalizer and decision feed back equalizer design issues.

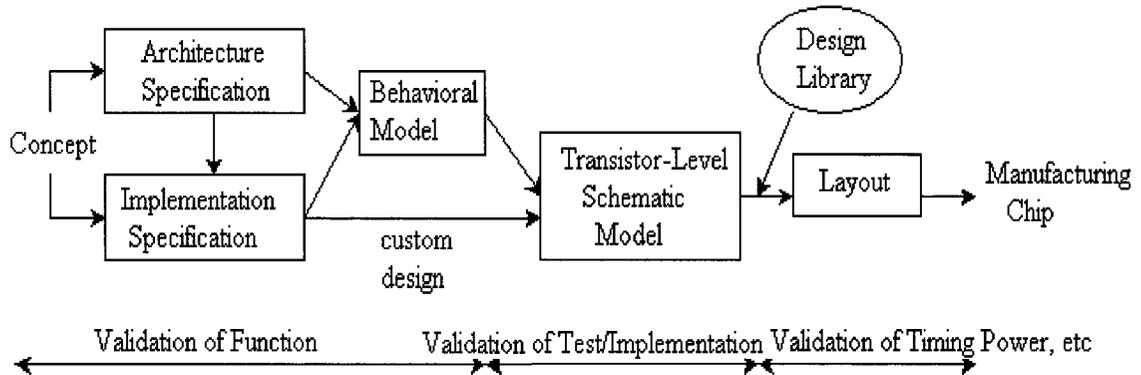


Figure 1.2: Design flow chart

Chapter 3 begins with the design of the DFE to be used in high speed backplane and transceiver applications; a MATLAB behavioral model of the DFE is constructed to prove architectural feasibility and to verify functionality. This results in a behavioral model for the proposed HRDFE. A complete MATLAB pipelined 3-tap HRDFE simulation model will then be described in detail and used to prove the functionality of the pipelined architecture. MATLAB simulation results and initial hardware implementation parameters are also presented.

There follows, in Chapter 4, a description of the implementation in $0.18\ \mu\text{m}$ CMOS of the DFE circuit, and of its simulation. Discussed are the transistor-level HRDFE structure with 3X sampling circuits and the post-layout simulation used to verify the high-speed performance of the HRDFE design.

A summary of the thesis, of conclusions drawn and suggestions for future work, makes up the remainder of the thesis.

2.1 Introduction

This Chapter presents an overview of the design issues to be considered in high-speed backplane design. Equalizers will be examined, and the performances of a number of structures will be compared. The following subjects will be investigated:

- High-speed serial transmission problems and the methods used in their solutions,
- Physical restrictions imposed by channel media,
- Linear and decision feedback equalizer principles.

2.2 Backplane design challenges

Backplane transmission plays a major role in determining the overall speed of modern digital and communication systems. The design of backplane structures for use at low data rates is straightforward, but at higher data rates such as 10Gb/s problems such as crosstalk, reflections and high frequency dependent attenuation have a serious effects on signal integrity.

The solution to the above problems is complicated and has to be economic. One approach is upgrading the current system, and the other is to replace it with a totally new

design. The former is usually much more attractive economically. Existing hardware has a capability of 3.125 Gb/s or less and extending this speed, to 10Gb/s, involves problems that today's designers probably were not anticipating. The three most important are:

Frequency dependent Attenuation

Signal frequency dependant attenuation, becomes more severe as the data rate increases; the channel attenuates the high frequency contents of the signal more than the low frequency content which results in ISI. The high frequency components of the transmitted signal will be attenuated so much in the channel that sharp edges of signals will vanish, tails will be generated and become longer as the channel gets longer. Other effects include worsening signal-to-noise ratio accompanied by the reduction in signal power.

Reflections

Signal reflections take place at data-path impedance discontinuities, the sources of reflection in a typical backplane are: the connectors, vias in printed-circuit cards, pins and stubs. The obvious methods of dealing with such reflection sources are using higher-performance connectors and back-drilling manufacturing techniques. But these solution are expensive so that are not considered as upgrades to existing backplanes.

Crosstalk

Crosstalk occurs between signal paths as a result of capacitive and inductive coupling between them. These coupling effects worsen with increasing frequency and must be guarded-against especially in places where data paths are physically near to one another, in places like connectors and in the integrated circuits themselves. Crosstalk is also an undesirable side-effect of transmitter pre-emphasis, a standard backplane signal-condi-

tioning method. Crosstalk can be reduced by using connector with higher performance and increasing the distance between signal paths. These solutions are expensive and increase the physical dimension of the PCB both of which are not desirable in today's industry.

The three problems noted above can be dealt with using an appropriately-designed equalizer, the design of which will take up the remainder of this thesis report.

There are a number of techniques that can be creatively implemented at both transmitting and receiving nodes to ensure reliable performance. One of these is combined transmitter pre-emphasis and receiver equalization, which selectively amplifies the higher frequency components that are more seriously attenuated than lower-frequency components in lossy channels. These lower-frequency components of the signal may also be de-emphasized at the same time. The intent is to compensate for the link losses as much as possible.

It is important to make an equalizer adaptable so that the same device can be made to work in a variety of backplane environments. This has not been included in the present work, but it is one of the issues to be explored in future research along these lines. Such programmability will allow an equalizer to adapt automatically to changes in its backplane environment [13-14].

Increasing the receiver input sensitivity can be greatly helpful for better equalizer performance at 10Gbit/s. Theoretically, a device operating at 3.125Gb/s requires a minimum of 200 mV differentially at the receiver input, but in general 300 - 400 mV is needed to ensure a very low BER for practical purposes. Finding methods to increase the receiver's input sensitivity will help to reach a lower BER. But this must not be carried too far, as increased receiver sensitivity will result in noise amplification to a level where the BER is increased. High sensitivity must therefore be accompanied by high jitter immunity, and special noise-cancellation and jitter rejection methods [14].

Beside equalization techniques, technologies are also chosen to improve the backplane transmission performance, Pulse Amplitude Modulation (PAM)₄, Duobinary systems instead of PAM₂ binary system have been studied [15-16]. These M-ary PAM technologies use the concept that reduces the symbol rate by $2/M$ compared to the PAM₂ system. This symbol rate reduction relaxes the requirement for the channel bandwidth by a factor of $M/2$ and allows the on-chip clock frequency to be reduced to $2/M$ of the original at the expense of noise sensitivity.

In high speed backplane data communications, the use of DFE aligning with Clock Data Recovery (CDR) a receiver is very important [27, 29]. The inclusion of such a capability places demands on the designer to pay close attention to issues from the device level, careful differential-pair length matching to maintain eye integrity, to the distribution of skew effects over system components [14].

Manufacturing tolerances and board layout considerations must be assessed early in the design cycle. Connector and via effects must also be taken into account. By applying the very latest design and manufacturing techniques, backplane and interconnection technology is reaching performance and data rate speeds thought impossible just several years ago.

2.2.1 Transceiver Description

In the situation here considered, data may be sent over buses, where a number of transmitters and receivers (transceivers) share the same backplane resource, or else between pairs of transceivers connected by point-to-point links. High bandwidths are more easily attained with the latter arrangement. In both of these cases, the problems discussed in this thesis are embodied in the simple transmitter/channel/receiver connection of Figure 2.1.

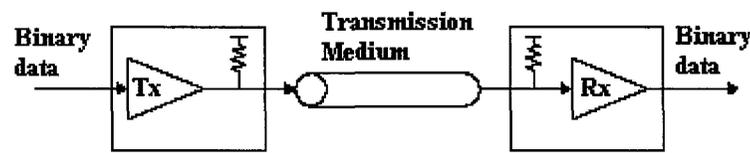


Figure 2.1: Structure of transceiver

Backplane signals are sent in analog format. The transmitter converts its digital output data to an analog waveform which is then placed onto the physical channel. The usual transmission-line terminations ensure that all energy incident on them is absorbed so that there will be no reflections. The source terminations are built to make the system more tolerant to crosstalk.

At the receiving end, the analog waveform is amplified and then restored to the original digital form by sampling. A timing-recovery circuit is used to properly place the sampling strobe.

2.2.2 The Transmission Medium

The transmitter and the receiver of Figure 2.1 are connected by a physical channel implemented in some ‘transmission medium’, the most common of which are PCB traces or coaxial cables. A real channel can be thought of as a series of paths joined by vias and connectors, at which there may occur impedance discontinuities.

The signal travel time along the channel is greater than the expected transition time of the transmitter because of the line’s distributed capacitance and inductance, and thus, the load seen by the source during a signal-level transition is that presented by the channel itself, not by the receiver. The channel serves to electrically isolate the transmitter from the receiver. By the same token, the impedance seen by the receiver during a transition time is that of the channel, not that of the transmitter. The channel behaves as a transmission line, and typical transmission line effects, such as reflection, overshoot, undershoot

and crosstalk must be considered in the course of design, and their modeling must be an admixture of electromagnetic and circuit theory [17].

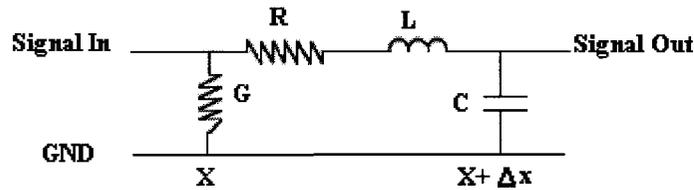


Figure 2.2: Distributed transmission line model

An ideal transmission line is a lossless line, one having zero resistance per unit length, but this is not true of a real transmission line. To model a practical transmission line, one begins by assuming that it is made up of an infinite sequence of the elemental components [18] described in Figure 2.2. Here, R is the line's resistance per unit length and G the conductivity per unit length due to nonidealities of the transmission line dielectric.

A nonzero R leads to both attenuation and distortion of the signals propagating along the line. The distortion arises from signal dispersion, where in the propagation velocity of a sinusoid (Fourier harmonic) becomes a function of the frequency. Attenuation effects in a transmission line are Ohmic in origin and primarily due to non-zero values of R and G . A mathematical analysis of the elemental segment of length dx in Figure 2.2 is used to derive a complex attenuation coefficient for an elemental transmission-line segment:

$$\gamma = \sqrt{(R + j\omega L) \times (G + j\omega C)} \quad (2.1)$$

which is a relation between attenuation, phase shift and frequency at some position x on the line. This coefficient appears in the formula for the (complex) transfer function of that channel segment [17].

$$H(\omega) = e^{-x\gamma} \quad (2.2)$$

The complex character of H means that each Fourier harmonic will be weighted by a distance-dependant attenuation factor.

These formulas were derived under the assumption that L , C , R and G are frequency-independent, an assumption that is not valid at the higher frequencies of interest in this work. One reason for their becoming frequency dependent is the so-called 'skin effect' [17-18].

2.2.3 Frequency-Dependent Attenuation

2.2.3.1 Skin Effect Loss

The skin effect is the name given to the tendency of alternating current to flow near the surface of a conductor, thereby restricting the current to a small conducting part of the total cross-sectional conductor area. The effect becomes more pronounced as the frequency increases, and causes a conducting path's resistance to become an increasing function of frequency.

The skin effect is due ultimately to the Lorentz force on the electron, and this can be translated into terms of conductor self-inductance. What happens is that as the signal frequency is increased, the moving charge carriers, i.e. electrons, are forced nearer and nearer to the surface of the conductor causing its inductive reactance to increase [17]. Resistance, and thus Ohmic loss, also increases because of the lessening of the effective cross-sectional area of the conductor. An analysis of the situation predicts that current density decays exponentially with distance of penetration into the conductor's cross-section. 'Skin depth' is defined as the average depth of such penetration [17](See pgs 49 & 85).

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}} \quad (2.3)$$

Here ω = radian frequency, ρ = volume resistivity, and μ = magnetic permeability. Equation (2.3) can be used with some elementary geometry to provide a formula for resistance as a function of frequency, one which for very high frequencies predicts that a conductor's resistance will be proportional to the square root of the frequency. Further analysis (involving the Biot-Savart law) shows that the magnetic field inside a conductor is reduced due to the skin effect, and so thus so is the conductor's inductance. The inductance tends to a very small limiting (constant) value at very high frequencies.

2.2.3.2 Dielectric Loss

Because of non-zero electron mass, the electric polarization in a dielectric develops a phase lag as frequency increases. This is equivalent to saying that the dielectric constant becomes complex, which causes the usual complex solution of the wave equation to be prefaced by a real exponential decay (attenuation) term, which in turn can be thought of as being due to Ohmic conductivity in an otherwise ideal dielectric. The energy loss due to this effect can reach significant proportions at high frequencies.

Ideally, there exists a phase difference of $\pi/2$ between the voltage and the current waveforms in a transmission line. The dielectric loss mechanism described previously causes a deviation from this ideality, one which can be quantified in terms of a frequency-dependent 'loss tangent' for a particular coaxial cable or PCB substrate dielectric. Dielectric loss is substantial in common PCB epoxy/glass materials, and is somewhat less in the case of polyethylene. Energy loss due to dielectric imperfections shows an approximately linear dependence on frequency [18].

2.3 Linear Equalization Techniques

When the data transmission speed is higher than the bandwidth of the channel, a binary transition may require more time than is available in a symbol interval which is

defined as a one-bit period. It will spread into adjacent symbols and cause ISI, Figure 2.3 shows an example of pulse response of data transverses of a 34" FR-4 channel at 8Gb/s. Physically, this FR-4 channel includes 30-inch PCB traces, two connectors and two 2" daughter boards.

The ISI problem is a result of rectangular pulses having infinite bandwidth while the channels expected to carry them do not.

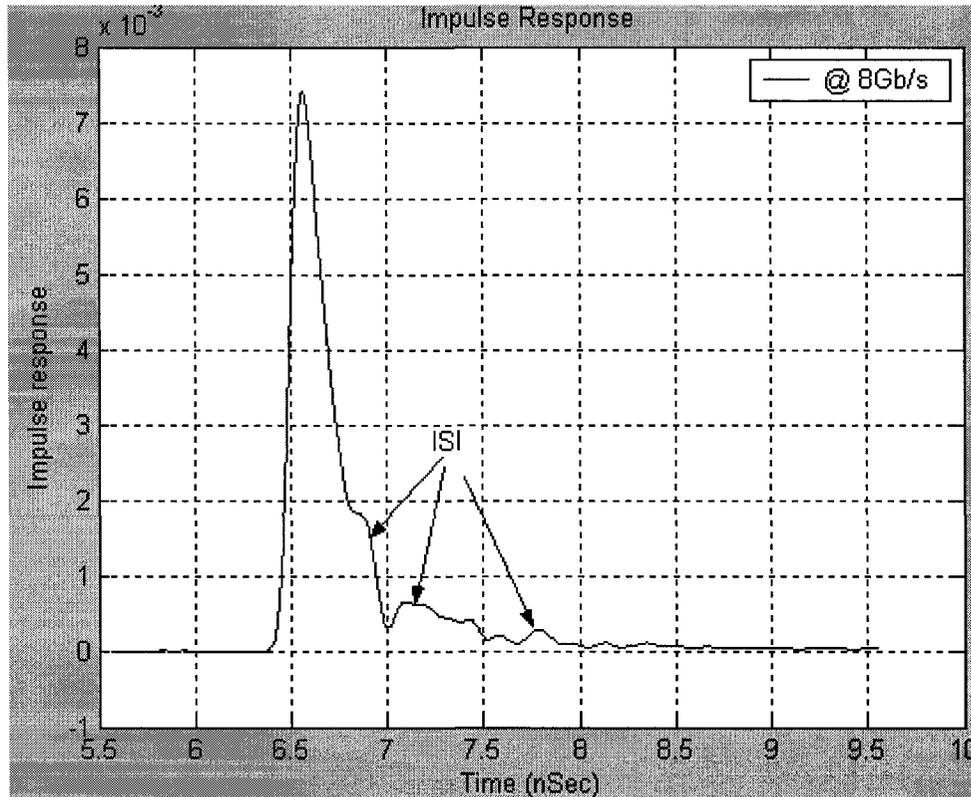


Figure 2.3: Impulse response after a FR-4 channel

The most promising approach is to compensate the distortions, including amplitude and phase distortion, and signal reflections, that occur after the signal leaves the transmitter [9, 19-21]. Consider that the overall (equivalent) transfer function of a signal link as shown in Figure 2.1, the equation of the transfer function is written as:

$$H(z) = H_{pulse-shaper}(z) \times H_{DAC}(z) \times H_{channel}(z) \times H_{Rx-filter}(z)$$

where the various terms refer to transmit pulse-shaping, the D/A converter with possible $x/\sin x$ correction, the channel itself and receiver filtering, and z is the discrete z -plane variable.

It is the function of the receive equalizer to adjust $H(z)$ in such a way that ISI is eliminated – it can be shown [9] that the ISI distortion will be zero when the compensated transfer function is spectrally flat in both magnitude and phase. Figure 2.4 shows the magnitude of a compensated transfer function.

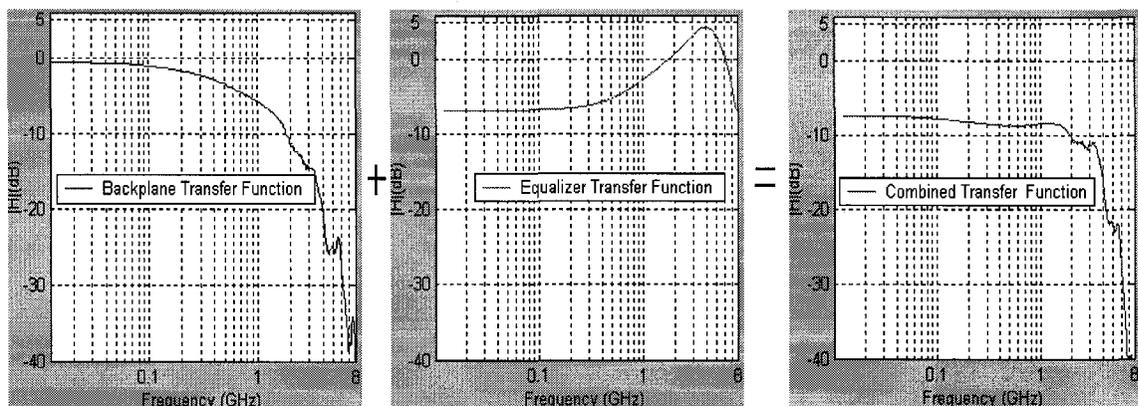


Figure 2.4: Transfer function of backplane, equalizer and combined one after a 34"FR-4 channel

A symbol arriving at the receiver may be written

$$x_0 = y_0 + \sum_{j=-\infty}^{\infty} y_j \cdot c_j \quad (2.4)$$

where the signal actually sent is y_0 and the distorted version arriving at the receiving end is x_0 , with the distortions occurring along the data path y_j being embodied in the multipliers c_j . The summation expresses the ISI effects caused by transmitted symbols lying at intervals $\pm 1, \pm 2$, etc on either side of the desired one. Note that the method being developed will have a built-in time-lag since a decision about y_0 involves symbols which have not yet arrived. The summation is theoretically an infinite one, but in practise only a few terms on either side of $j=0$ will be important.

A rearrangement of this equation to

$$y_0 = x_0 - \sum_{j=-\infty}^{\infty} \hat{y}_j \cdot c_j$$

shows that the desired signal y_0 is the received (distorted) one x_0 from which a sum of compensation terms has been subtracted, \hat{y}_j is the sampled desired signal at time j . If the multipliers c_j were to be properly characterized and incorporated into the equalizer, ISI effects would be eliminated, which is the ultimate goal of the work.

The summation form suggests that the equalizer be implemented using a transversal filter (tapped delay line – see Fig. 2.5) idea. By way of example, if the desired symbol were to be affected by five symbols on either side of it, ideal equalization from an ISI-only perspective would involve summing these samples to get

$$y_0 = x_0 - \sum_{j=1}^M \hat{y}_j \cdot c_j \quad (2.5)$$

Some of the methods used for computing the K_j are

- 1) The *Zero-Forcing* (ZF) algorithm aims to eliminate inter symbol interference (ISI) at decision time instants (i.e. at the center of the bit/symbol interval) [22].
- 2) The *Least-Mean-Square* (LMS) algorithm will be investigated in greater detail later [22].
- 3) The *Recursive Least-Square* (RLS) algorithm offers faster convergence, but is computationally more complex than LMS, as a matrix inversion is required [22].

There are two basic methods of implementing the equalization process described in the previous equations: the linear (FIR) equalizer and the decision feedback equalizer [23, 24]. In each case, any of the three algorithms mentioned previously may be used to compute the coefficients c_j .

2.3.1 The Linear Equalizer

The linear equalizer will first be examined, with attention paid to its architecture. It will turn out that a linear equalizer, whose ISI performance is not totally eliminated but reduced to ‘acceptable’ levels, can provide better overall error statistics than a theoretically optimal one. The general idea of a linear digital equalizer is in Figure 2.5.

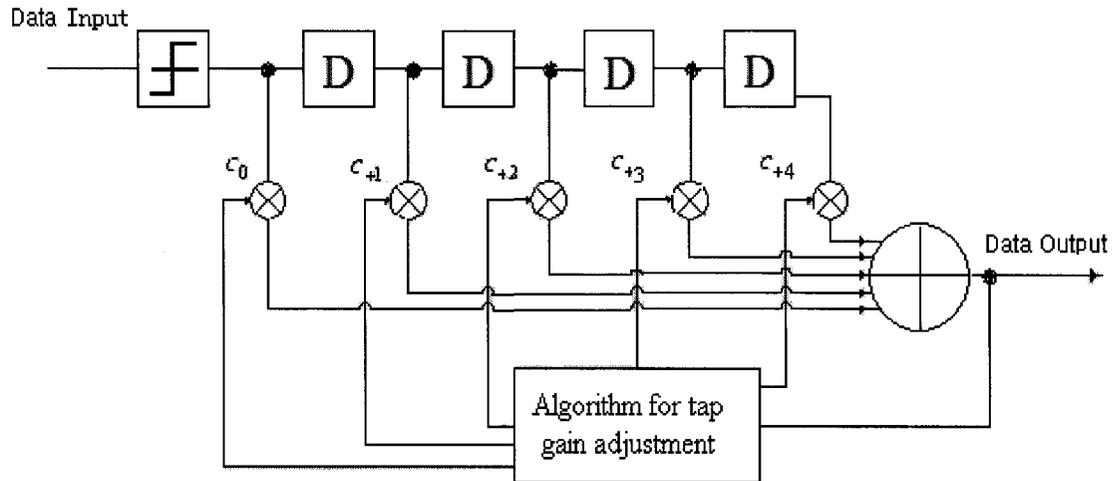


Figure 2.5: Linear equalizer structure

This schematic illustrates the FIR filter approach to applying (2.4) to a distorted data stream – in practise, this is the architecture of choice. The coefficients c_k are produced by one of the algorithms mentioned earlier. The complex issues of filter length and design trade-offs will be treated in Chapter 3 and 4.

There are two basic approaches to linear equalization. One is designed to have a transfer function that is the reciprocal of the equivalent transfer function for all z . This zero-forcing (ZF) technique immediately satisfies the condition for zero ISI, namely that the channel transfer function be spectrally flat. Calling the ZF equalizer transfer function $L_{ZF}(z)$, we have

$$L_{ZF}(z) = 1/H(z) \quad (2.6)$$

The effective channel transfer function seen by the receiver will be spectrally flat since $L_{ZF}(z)H(z) = 1$, and so any ISI effects should vanish. But this last equation also shows that spectral nulls when $H(z)$ approaching zero will lead to problems, for the gain of the equalizer will become very high and incident noise will be amplified excessively.

In other words, optimally complete ISI elimination will in general be accompanied by a worsened noise situation, and this noise will itself be the cause of an increased BER. One is then led to consider a compromise, where ISI effects are reduced, not completely eliminated, and the noise increase is held to tolerable levels. It may then be that the overall BER due to both ISI and noise, is less than in the case where ISI is removed completely.

When the smallest Mean Square Error (MSE) at the equalizer output is striven for, instead of a complete eradication of ISI being sought, the MSE linear equalizer results [22].

The determination of the equalizer characteristics concurrent with a minimal error probability is not so easily done, in general. But one reasonable approach, which will serve as an example, is to minimize the probability of error due to the combined effects of additive white Gaussian noise (AWGN) and ISI at the decision device input. If this is done, the Zero-Forcing linear equalizer transfer function $L_{ZF}(z)$ is modified to

$$L_{MSE}(z) = \frac{1}{H(z) + (N_o/P_s)} \quad (2.7)$$

where the channel noise is white, it has a two-sided noise power density of $N_o/2$, and P_s is the average transmitted power. The second term in the denominator is basically an SNR term. Its presence causes a departure from the characteristics necessary to guarantee complete ISI removal, but also reduces equalizer gain excursions with the attendant possibility of lessened noise – the BER of L_{MSE} is potentially less than that of L_{ZF} [22].

FIR-based linear equalization performance is not very good when the frequency response of the frequency selective channel contains deep fades which normally happen at high frequency. So we need to find a better performance equalizer for high-speed data communications, and the decision feedback equalizer is one of the choice.

2.4 Decision-Feedback Equalizer

The general decision-feedback equalizer is a nonlinear device containing a forward filter and a feedback filter. The forward filter is similar in structure to the linear equalizer of the previous section, while the feedback filter is made up of a tapped delay line whose inputs are the decisions made on the equalized signal [23-26]. The purpose of the DFE is to minimize both intersymbol interference and noise amplification [23].

2.4.1 Introduction

A block diagram of the DFE is shown in Figure 2.6, with more detail being displayed in the following Figure 2.7 [24].

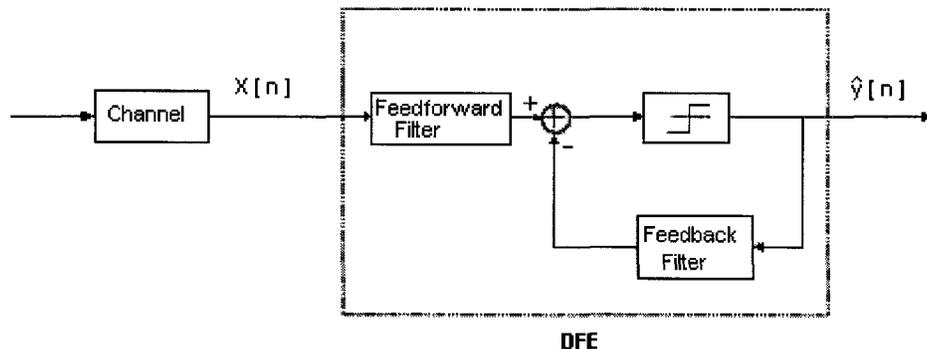


Figure 2.6: Decision feedback equalizer in block diagram

In each symbol period, one input sample is applied to the forward filter, and one decision, or training, sample to the feedback filter. The equalizer then outputs a weighted

sum of the delayed values at the filter outputs, and updates the weights in preparation for the next symbol.

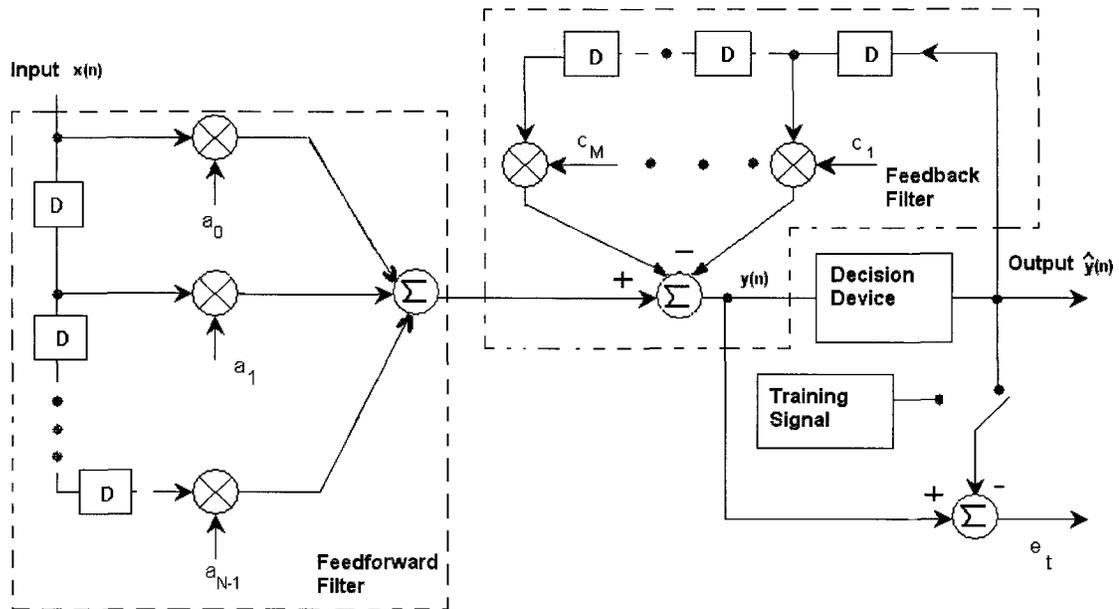


Figure 2.7: Decision feedback equalizer

Proper characterization of the distortion is essential to the effective removal of ISI. In the interest of making correct decisions, a decision is chosen which minimizes the probability of making an error.

Two main issues are of concern in this process. First, the feedback decision has to be correct, as the assumptions that go into the analysis of a DFE are most accurate at low-error-rates. Furthermore, because the DFE is a feedback loop where the results of previous decisions are used to make new ones, incorrect results might lead to instability in the decision process and error propagation.

The second point is related to the use of the symbols in the future of the desired pulse, since the feedback part of the equalizer only considers previously detected pulses.

Although the forward filter is structurally similar to the linear equalizer, it turns out that the ZF problem of nulls is not an issue when a linear equalizer is implemented in a DFE, because the linear equalizer in this case is only concerned with eliminating the pre-

cursor ISI. However, a ZF forward filter is still outperformed in the MSE sense by a DFE, which has a forward filter designed around the MSE criteria.

Of importance is the DFE's relationship to optimal reception. One problem with the equalization idea is that the optimal fundamental receiver structure is well known for an FR-4 channel, so that an equalizer which removes ISI without enhancing noise can be designed. This is because the spectral null problem no longer exists and because correct decisions result in noise-free feedback. Fortunately, it turns out that in a DFE approach, the forward filter output is compatible with the well-known optimal receiver structures. This is because the forward filtering is designed to minimize MSE.

In Figure 2.7 it is apparent that a general DFE is made up of two filters – forward and feedback. The taps of both filters are separated by delays of one symbol interval D . ISI-contaminated data from the channel is applied to the forward filter's input. The feedback filter has as its input the sequence of decisions on previously detected symbols. Functionally, the feedback filter is used to remove from the present estimate that part of the inter-symbol interference caused by the k previously detected symbols [24].

The equation for this filter is

$$c_m(k+1) = c_m(k) + e_k \hat{y}_{k-m} \quad (2.8)$$

Here $c_m(k)$ is the m^{th} total feedback coefficient, k is the current time index and \hat{y} is the k^{th} (current) decision symbol, $e_k = y_k - \hat{y}_k$ is the k^{th} error signal.

2.4.2 Adaptive Equalizer with LMS Algorithm

In the minimization of the MSE, it is found that the optimum equalizer coefficients are determined by solving a set of linear equations, something that is very difficult to do with real-time hardware. But an iterative procedure that avoids the direct matrix inversion can be used to compute the optimal coefficients c_i . The simplest iterative procedure is the method of steepest descent, in which one begins by arbitrarily choosing an initial coeffi-

cient vector C_0 . This initial choice of coefficients corresponds to some point on the quadratic MSE surface in the M dimensional space of coefficients. With each new sample, the gradient vector G_0 , having the M components $\frac{\partial}{\partial C_k} j(e_k^2)$ ($1 < k < M$), is then computed at a point on the MSE surface, and each tap weight is changed in the direction opposite to its corresponding gradient component. The change in the j -th tap weight is proportional to size of the j -th gradient component.

Next, the whole setup of adaptive LMS DFE equalizer will be discussed. As in the case of the linear adaptive equalizer, the coefficients of the feedforward filter and the feedback filter in a decision-feedback equalizer may be adjusted recursively, instead of inverting a matrix. Based on the minimization of the MSE at the output of the DFE, the steepest-descent algorithm takes the form:

$$C_{k+1} = C_k + \mu E(e_k V_k) \quad (2.9)$$

Since the exact cross-correlation vector is unknown at any time instant, an estimate the vector $e_k V_k$ and average out the noise in the estimated through the recursive equation is used, here μ is the step size controller, $V_k = [\hat{y}_k, \dots, \hat{y}_{k-M}]^T$ is the vector of received samples at time k , C_k is the vector of M tap coefficients. This is the LMS algorithm for the DFE.

A training sequence to adjust the initial DFE coefficient values can be used in the case of a linear equalizer [30-32]. Upon convergence to optimum coefficients, a decision-directed mode is entered where in the decisions at the output of the detector are used in forming the error signal and are fed to the feedback filter.

The adaptive mode of the DFE is illustrated in Figure 2.8.

In this research work, a DFE without feedforward filter (FFF) structure is chosen. This approach has two main advantages, namely simple hardware implementation and the

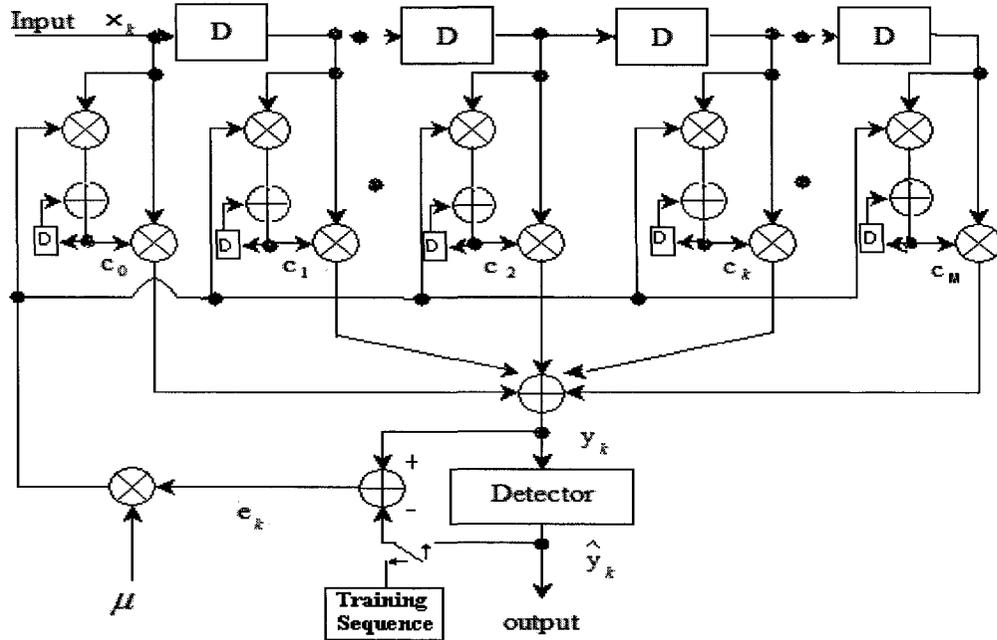


Figure 2.8: Linear adaptive equalizer based on MSE criterion

rapid convergence of the DFE-without-FFF architecture in the studied channel and at the transmission speeds of interests.

In Chapter 3, the parameters of an adaptive decision-feedback equalizer (DFE) are estimated by a MATLAB procedure. Here an LMS algorithm [22] is the basis of a real-time DFE equalizer whose coefficients adapt to changing channel characteristics. The particular case study involves estimating the changes in the FIR filter coefficients brought about by signal changes on a 34" FR-4 channel and finding the ISI values. At the same time, two and three different equalizer orders are compared as to error-probability and SNR performance.

The most significant advantage of LMS decision feedback equalization over a linear equalizer is the lack of noise enhancement because DFE only cancels ISI-caused tails of previously received symbols and it is not necessary to invert the channel's frequency response to compensate for the high frequency component that are attenuated by the lossy channel.

2.4.3 DFE circuits

Three examples of DFE circuits design are provided in this sector. First, a conventional mixed-signal RAM-DFE is described that proved to operate at 90 Mb/s [33].

A conventional DFE uses a FIR filter to cancel any ISI that is a linear function of past decisions. To improve the performance when nonlinear ISI is present, a RAM-based DFE is used. Here, the RAM is used as a lookup table to store ISI estimates that are a linear or nonlinear function of the past decisions [33].

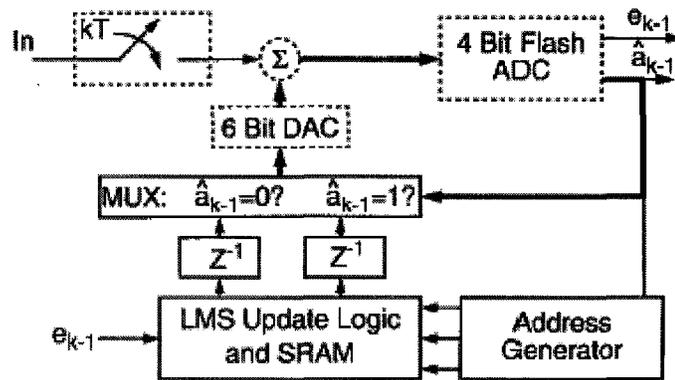


Figure 2.9: Block diagram of the mixed-signal RAM-DFE architecture.

Figure 2.9 [33] shows a block diagram of the mixed-signal RAM-DFE. The analog blocks are distinguished from digital ones using dashed lines. The critical path is shown with thick lines, in this path, all the operations must occur in 11 ns for 90 Mb/s operation, which is one symbol period for 90Mb/s operation.

The analog input signal from the preceding forward equalizer is sampled once during each bit period T . A selected value from the static RAM (SRAM) lookup table is converted to analog form by a 6-bit digital-to-analog converter (DAC) and summed to the input so as to cancel postcursor ISI. The ISI-corrected signal is then converted to digital form by a 4-bit flash ADC after a one period delay. One bit (the decision \hat{a}_{k-1}) of the ADC output is used by a multiplexer to decide on which segment of the SRAM's output to delay and apply to the DAC input. The other bit e_{k-1} is an error used by the LMS update

logic to select one of two bit groups z^{-1} making up the SRAM output. One value is the postcursor ISI estimate to use if the decision happened to be a ‘one’, and the other if the decision was ‘zero’. Then the multiplexer output is latched at the DAC input.

A custom C program was written and behavioral simulations were run to determine specifications for each of the circuit blocks in Figure 2.9.

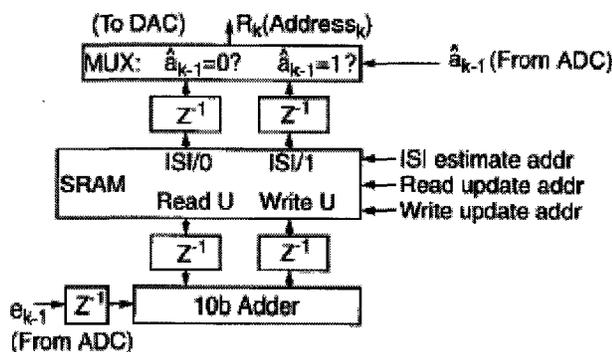


Figure 2.10: Block diagram of the digital portion of the RAM-DFE

Figure 2.10 [33] shows more detail about the digital portion of the IC, which is the LMS update logic and the SRAM. The SRAM has three ports and uses a standard static memory cell with two switches and two inverters added to allow for a simultaneous dual-buffered read and differential write. There are two key I/O paths. The first is the ISI cancellation path. The other path is the LMS update path. The past four decisions are used by the address generator to develop an address for the update. The data at that address is fetched from the SRAM and latched. The error signal is delayed to align with the delayed RAM value, shifted to scale it by the update gain and then summed with the fetched data sample. The 10-bit adder output is latched and then written back to the SRAM.

TABLE 2.1: Mixed-signal RAM-DFE performance [33]

	Key Features	Technology, Die Area	Max Speed, Power Diss. (5V Supply)	BER Performance at 15 dB SNR
DFE IC	4-tap RAM-DFE, Mixed signal, 3-b/1-b error in LMS update, Pipelined RAM access	1 μ m CMOS, 4.5 mm ²	90 Mb/s, 0.26 W	BER = 2×10^{-8}

In the analog domain, the DFE subtracts intersymbol interference caused by the past four outputs. The equalized signal is fed into an ADC to produce the decision output and error signal used to adapt the RAM contents in the digital domain. Table 2.1 shows the performance of this mixed-signal DFE.

A disadvantage of the RAM-DFE is that it converges slower than the linear DFE because only one RAM value is updated each clock cycle, whereas every coefficient in a linear DFE can be updated each clock cycle. Another disadvantage of the RAM-DFE is that the size of its lookup table grows exponentially with the length of the delay line [33].

The second example is a CMOS 2-tap full-rate pipelined DFE Receiver circuit proved to be working at 1.2Gb/s by Sohn [34].

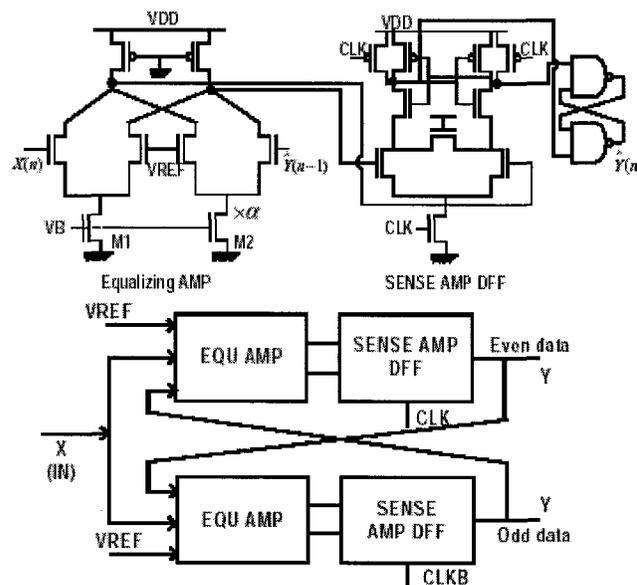


Figure 2.11: Circuit diagram of pipelined DFE receiver

The pipelined DFE receiver shown in Figure 2.11 works with full rate clock [34].

A conventional time-interleaved receiver is an equalizing amplifier driving a sense-amp DFF. The output of each branch of this pipelined DFE receiver, a conventional receiver, is fed back to the input of the other one in a cross-coupled feedback scheme, where the digital decision result of one branch is used in the equalization of the other

branch. The difference between output $\hat{Y}(n)$, the ISI correction (which is also label Y in schematic) and the input signal $X(n)$ is amplified [34] and sent on to the sense-amp. The equalizing amplifier is seen to be made up of two coupled differential pairs, wherein the size ratio of the bias current sources M1 and M2 determines the equalizing ratio a . Drain loads are provided by PMOS transistors operating in their triode regions. The bias control voltage common to M1 and M2, V_B is supplied by a current bias circuit which is not shown [34].

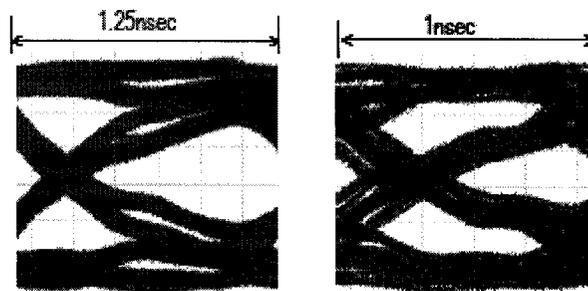


Figure 2.12: Measured eye pattern of receiver

Figure 2.12 [34] shows the eye-patterns measured at the DFE receiver's input for data rates of 800 Mb/s and 1 Gb/s. The bit error rate (BER) was determined to be less than 10^{-12} , and a greatly-lengthened time window was realized.

When operated from a 2.5 Volt power supply, the two-tap DFE receiver consumed only 2.5 mW. The chip's active area was $8000 \mu m^2$ in $0.25 \mu m$ CMOS process.

The three-tap HRDFE which is the subject of this research and based on this pipelined structure, will be fully discussed in the next chapter.

The description of another DFE circuit, a 6.25 Gb/s binary, adaptive device using first post-cursor tap cancellation and intended for legacy applications in serial backplane communications, was published by the Texas Instrument company at ISSCC'05. It was realized in a $0.13 \mu m$ CMOS technology and was powered by a 1.2 Volt supply [37].

In the half baud rate adaptive DFE presented in the TI paper, direct cancellation of the first post-cursor tap is done at 6.25 Gb/s. It was found that when correct decisions were made, the post-cursor channel response could be equalized without an increase in high-frequency crosstalk.

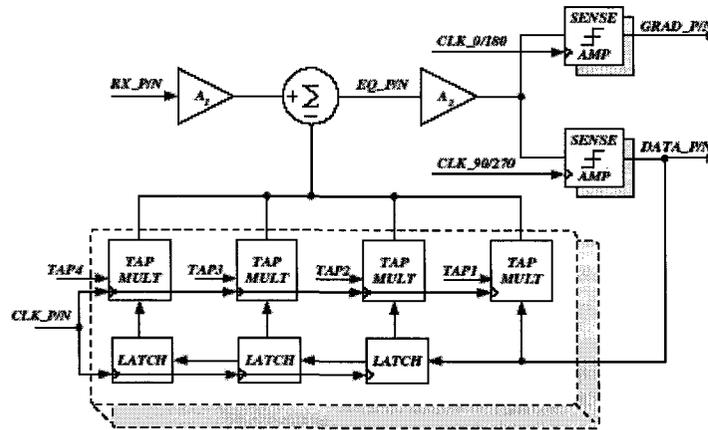


Figure 2.13: DFE architecture

The architecture of the DFE is illustrated in Figure 2.13 [37]. Four half baud rate clocks (CLK_0 , CLK_{90} , CLK_{180} , CLK_{270}) oversample the serial data (RXP/N) by a factor of two, making possible adaptation in both the Clock and Data Recovery (CDR) and in the DFE. In the CDR loop, each data sample ($DATA_P/N$), nominally centered in the data eye, is compared to the previous one and the 90° offset gradient sample ($GRAD_P/N$). Circuit operation can be summarized briefly:

- On each transition, the phase error of the recovered clock is used to update a phase interpolator based CDR.
- The zero-crossing data eye jitter determines a lower bound for the data BER.
- Gradient samples are used to determine whether the eye is over- or under-equalized.
- Gradient and data history are used to adjust tap weights by using a sign-sign LMS method.

If optimum DFE convergence with an SNR of less than 10^{-15} is to be had, the data samples must be resolved in less than 80 ps at the 6.25 Gb/s rate. In other words, the delay should be less than one-half of the symbol period. This was done by feeding the output of a pair of high-speed sense amplifiers that slice and latch the data, followed by a MUX that selectively subtracts a current corresponding to the previous sample, directly back to the first tap.

Optimization using careful parasitic control and statistical simulations led to the design of circuits that could resolve the less-than 20 mV differential signal sufficiently well to enable correction of the next edge within 60 ps. This is well within the 80 ps period mentioned earlier. The resulting half baud rate architecture with direct first-tap feedback minimizes the DFE hardware [37].

2.4.4 Future of Equalizers

Besides the adaptive equalizer mentioned above, another important equalizer should be indicated is the blind equalizer [38], which uses a type of adaptive equalizer that doesn't use a training sequence to characterize the channel. The lack of a training sequence means the blind equalizers do not need to store the error in the receiver, which shortens the data channel transmission time, and it is therefore a topic of considerable research interest. However it may need more convergence time than the adaptive equalizer due to the lack of training sequence structure.

Fractionally spaced equalizers (FSE)

The behavior of FSEs is robust in the presence of symbol timing variation. FSE topology allows the filter to equalize beyond the Nyquist frequency of half the symbol rate, making the system more resistant to aliasing effects, transversal filters do not have this capability. The much-used T/2-spaced equalizer topology is one implementation of an FSE. Several significant papers have proved the superiority of a fractionally spaced

approach over a baud-rate sample time approach under the nonideal conditions often encountered in practice [12].

Orthogonal Frequency Division Multiplexing (OFDM)

OFDM, also known as discrete multitone, or DMT, approaches the equalization problem by multiplexing a single wide-bandwidth signal onto several narrow-bandwidth frequency-modulated components. These are equalized separately and then recombined into an undistorted signal at the receive end. Narrow bandwidth signals are much easier to deal with than are spectrally complex ones, and the method finds application in situations where the channel causes particularly severe distortion, twisted-pair conduits, for example [39].

2.5 Summary

Among many equalization techniques, DFE is outstanding due to its not compensating the channel's transfer function, purely canceling ISI, avoiding noise enhancement as decisions are noise free, and also its less sensitive to the sampling clock jitter. Pipelined DFE allow high-speed operation compared to conventional DFE [33-35, 40-42], however, the existing 1 post-tap full-rate pipelined DFE [34] still can not meet the requirement of 10Gb/s transmission. A half-rate multi post-tap pipelined DFE is proposed to solve this issue in the coming Chapter 3.

The difficult problem of implementing a high-speed equalizer could be greatly alleviated if a receiver-end equalizer that can work with a half-rate clock were available. This is because the pipelined DFE circuit can process double rate incoming data when pipelined branches operate at half-rate clock simultaneously. As a result, the 2:1 MUX output of the DFE doubles the rate of the same DFE output operating at full-rate clock.

It is the purpose of the present work to show that such an equalizer is in fact possible, by designing it and then simulating the design to verify the correctness of its operation.

The new architecture pipelined half-rate DFE (HRDFE), is outlined in Figure 3.1. Proof of concept is done by first using MATLAB to generate the parameters needed by SIMULINK, and then using the latter to run a behavioral simulation. The SIMULINK results, especially the optimized tap coefficients, are used as initial tap coefficients in the transistor level simulation of the circuit in Chapter 4.

3.1 Circuit Description

The circuit of a conventional full-rate pipelined 2-tap DFE was described in Chapter 2. These are suitable to restore the characteristics of transmitted data only at lower transmission rates approximately 1.2 Gb/s in backplane application.

It is assumed that the system performance enhancement is to be the result of equalizer modifications to the receiving block, it is assumed that the clock recovery problem has already been solved, and furthermore that this clock has the 50% duty cycle needed for proper operation of the DFE circuit elements [36]; please refer to Figure 3.1.

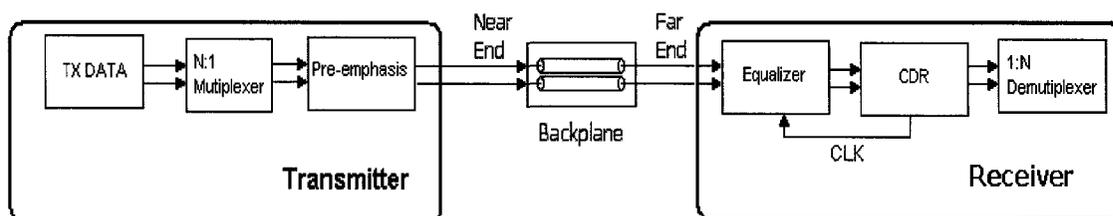


Figure 3.1: Simplified transceiver block diagram

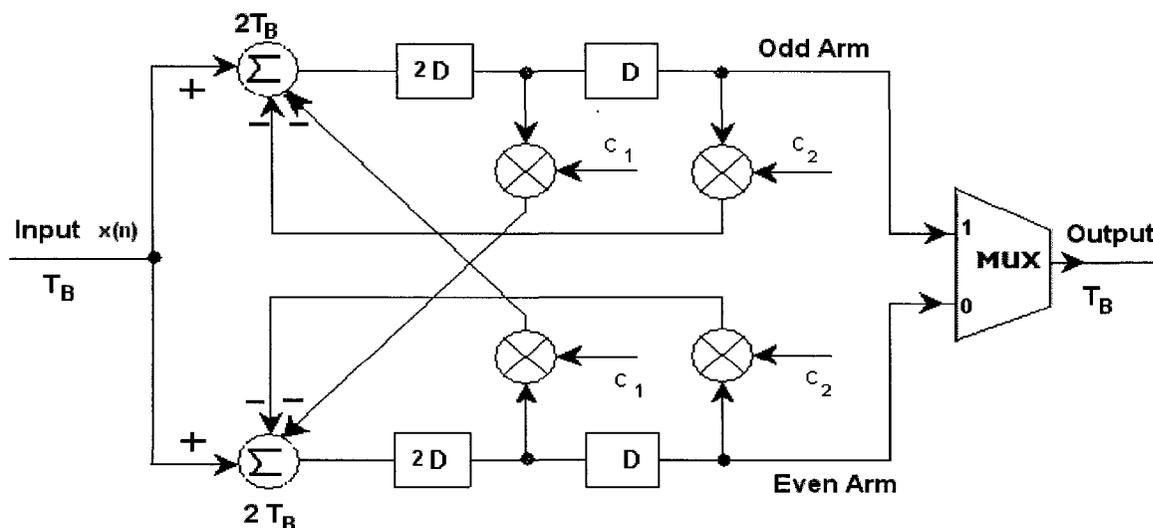


Figure 3.2: Structure of half rate 3-tap DFE

Structure of the proposed DFE is shown in Figure 3.2. The pipelined DFE has two data process branches: odd arm and even arm. Input data sequence $x(n)$ has a period of T_B , in both arms, the first delay cell provides 2-symbol delay recovered data, the second delay cell provides another 1-symbol delay recovered data. The output data of the adder will have a period of $2T_B$ with recovered data cross-coupled and feedback. The output of the circuit will have a period of T_B after a 2:1 MUX. The circuit of proposed DFE is shown in Figure 3.3. The adder is implemented by a linear FIR filter, the odd arm and even arm DFF triggered at opposite phase of half-rate clock produces 2-symbol delay. Dual-edge triggered flip-flop (DETFF) produces 1-symbol delay. Note the DFF and DETFF is part of phase detector circuit in CDR. The half-rate outputs of the 'even' and 'odd' branches are re-interleaved into a full-rate stream by a 2:1 multiplexer. The half rate clock signal is used to separate the incoming stream of pulses into two new even and odd half-rate sequences.

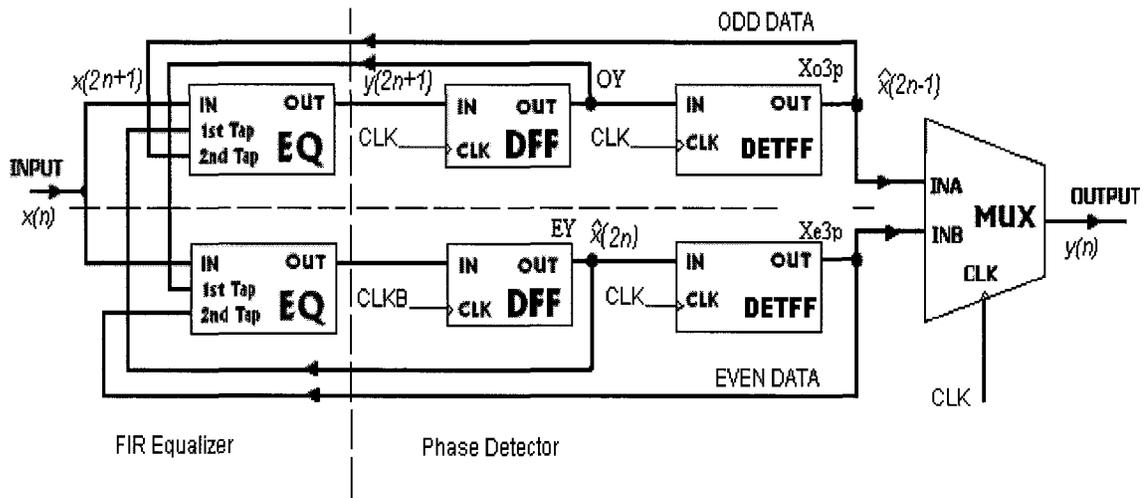


Figure 3.3: Circuit of half rate 3-tap DFE

3.1.1 Operation of the Half-Rate DFE

This design uses a parallel pipelined structure, with one side processing evenly-indexed samples and the other the odd-indexed ones. Partitioning of the incoming stream

into even and odd parts is done using the positive and negative transitions of a 50% duty-cycle clock which is running at one-half the data rate. The relative timing of the input, even and odd streams is shown in Figure 3.4. T is the input serial data symbol period. Half-rate recovered clock samples in the middle of the serial data symbol. T_{CQ} is the DFF delay, T_S is the equalizer delay.

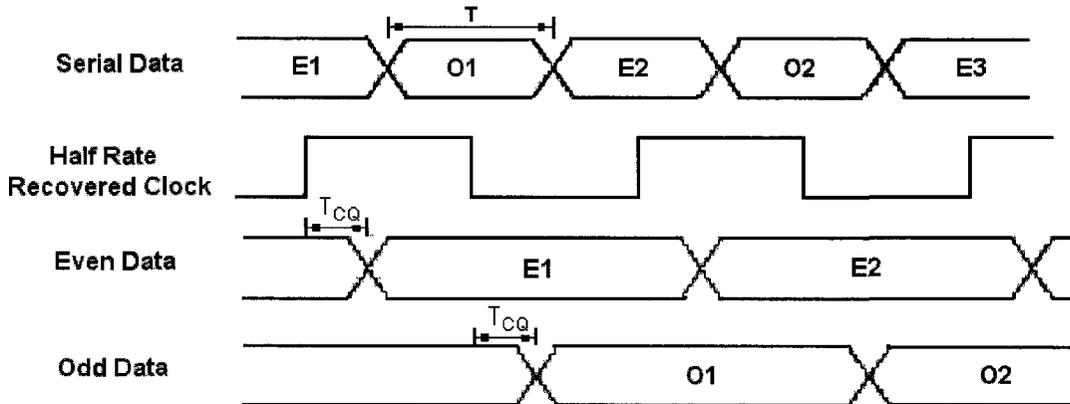


Figure 3.4: Odd and even data partitioning

This timing diagram, along with the more-detailed, DFE diagram of Figure 3.2 shows how the cross-coupled feedback of the phase-shifted decision signals works.

The linear equalizers at the DFE input have a conventional FIR filter structure as shown in Figure 3.5 with delays of one symbol period.

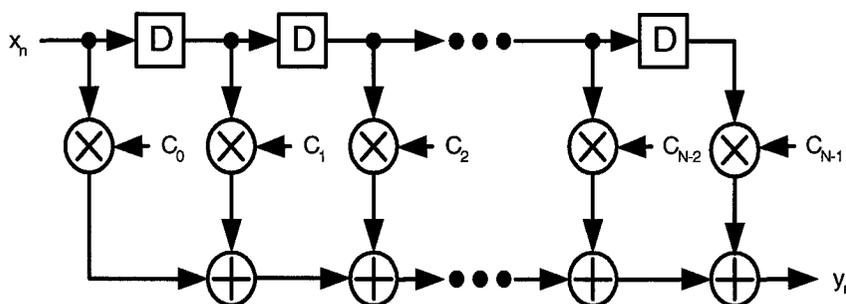


Figure 3.5: Multi-tap FIR equalizer structure

They implement the convolution:

$$y(n) = x(n) + \sum_{i=1}^M c_i \hat{y}(n-i) \tag{3.1}$$

where in general, the c_i are the tap coefficients and M is the number of delays plus one. In the half-rate DFE design used in this project, $M = 2$. Because assigning the parity of each of the interleaved streams is arbitrary, the same coefficients are used in the FIR filters of the two branches.

The design of the equalizer blocks in Figure 3.3, also shows the connections of the sampling feedback to the second and third tap.

If the even/odd symbols are indexed in steps of $2n/2n+1$, the equalizer outputs are written

$$y(2n) = x(2n) + c_1\hat{x}(2n-1) + c_2\hat{x}(2n-2) \quad (3.2)$$

and

$$y(2n+1) = x(2n+1) + c_1\hat{x}(2n) + c_2\hat{x}(2n-1) \quad (3.3)$$

for the even and odd branches respectively. $\hat{y}(n)$ indicates sampled value, note here $\hat{x}(n) = \hat{y}(n)$.

The pipelined half-rate DFE operational details will be presented below. The input serial data stream $x(1), x(2), \dots$, is regarded as an interleaving of half-rate even and odd sequences as shown in the Figure 3.3. Figure 3.3 shows the data operation principles.

The need for the 50% clock duty-cycle is apparent in the diagram: CLK and \overline{CLK} must have the same period for symmetrical operation of the circuit.

OY is the output of the odd arm DFF - it causes a two-symbol delay of the input signal since the sampling clock is half rate. Output OY is the sequence $x(3), x(5), \dots$. Each signal period is twice that of the input serial signal. DETFFs are designed to have a one-symbolic delay so the output of DETFF $Xo3p$ will be the sequence $x(1), x(3), \dots$. The same reasoning applies to the even-branch signals EY and $Xe3p$. EY and $Xo3p$ feedback to the odd arm. With the condition that

$$T_{CQ} + T_S < 1/2 T,$$

which is less than half the transmitting data symbol period, $x(2)$ will be fed back from EY at the time that $x(3)$ feeds into the odd arm equalizer, and $x(1)$ will be fed back from $Xo3p$ will also appear at the same time of Odd arm equalizer input side as 1st-tap and 2nd-tap respectively.

All the equations under the FIR Equalizer block in Figure 3.3 show the data processing of the equalizer. Table 3.1 is made to show the data operating of the DFE architecture shown in Figure 3.3. Each $x(n)$ is one symbol period signal.

TABLE 3.1: Data sequence of the pipeline 3-tap half-rate DFE

Inputdata	X(1)	X(2)	X(3)	X(4)	X(5)	X(6)
OY	X (1)	X (1)	X(3)	X(3)	X(5)	X(5)
Xo3p	#	#	X (1)	X (1)	X(3)	X(3)
EY	#	X(2)	X(2)	X(4)	X(4)	X(6)
Xe3p	#	#	#	X(2)	X(2)	X(4)

Consider, as an example, the case when input data is $x(5)$. From the table, when $x(5)$ arrives, the odd arm samples the data and output OY presents $x(5)$, and ready to transmit to $Xo3p$, where $Xo3p$ still shows data $x(3)$ at this time due to each odd data last two symbol and the one symbol delay of the DETFF, where EY still presents $x(4)$ at the same time. So from the architecture, the output of odd arm FIR equalizer is:

$$x(5) - c_1 EY - c_2 Xo3p = x(5) - c_1 \hat{x}(4) - c_2 \hat{x}(3)$$

For the same reason, when $x(6)$ arrives, the even arm samples the data and output EY presents $x(6)$, and OY still holds data $x(5)$ where $Xe3p$ holds $x(4)$ so output of even arm FIR equalizer is:

$$x(6) - c_1 OY - c_2 Xe3p = x(6) - c_1 \hat{x}(5) - c_2 \hat{x}(4)$$

That is how the 3-tap half-rate DFE portages. This DFE structure has been verified both in behavioral modeling and in transistor level simulation which will be presented in Chapter 4.

3.2 Demonstration of Functionality

The response of a MATLAB model of the device to the input signals from simulation that could be expected in an actual operating environment was measured from simulation. The software tools used included MATLAB Communications Toolbox and SIMULINK simulator.

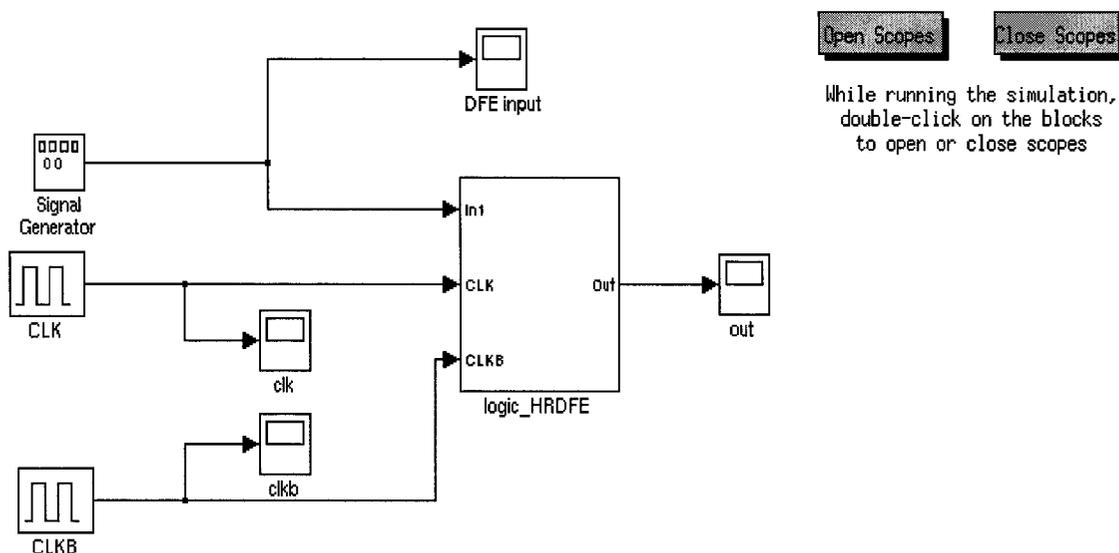


Figure 3.6: Testing model block diagram

In Figure 3.6, the SIMULINK signal generator was programmed to provide a square wave with 1V amplitude at the projected data rate, and the pulse generator was chosen to produce the necessary half-rate differential clock pair (labelled as CLK and CLKB). The details of the half-rate DFE block in this diagram and of its connections to external data sources and displays are shown in Figure 3.7.

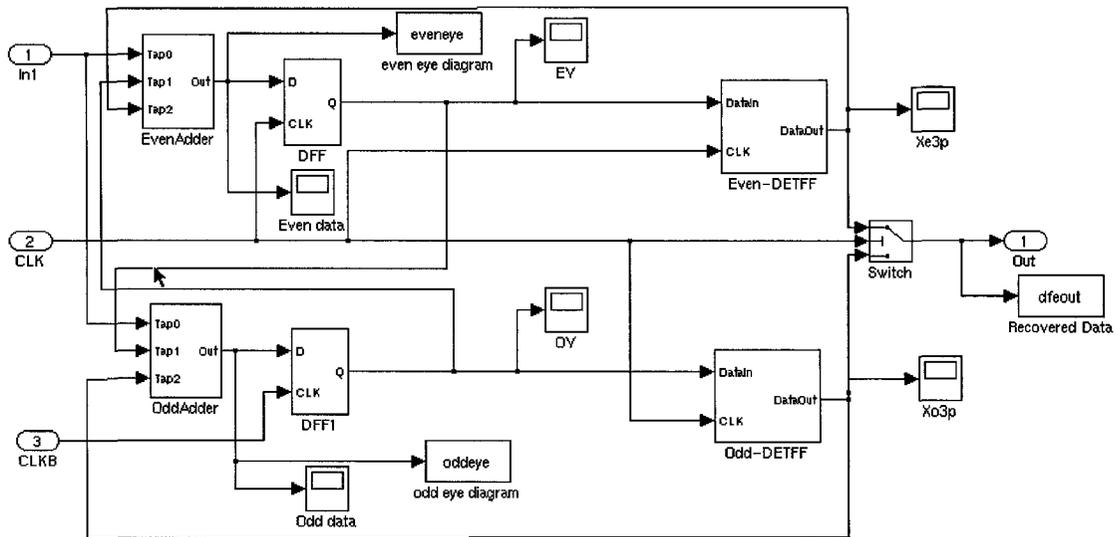


Figure 3.7: Logic_HRDFE block diagram

For the test purpose, the FIR filter coefficients ($\{C_i\}$) are set to -0.3 for the first post-tap, and -0.1 for the second post-tap. The testing points for the FIR equalizer outputs are respectively named *Odd Data* and *Even Data*, DFF outputs *OY* and *EY*, and the DETFE signals feedback into the FIR two post-taps are named *Xo3p* and *Xe3p*. The 2:1 multiplexing action needed to reintegrate the even and odd streams is effected by the switch shown in Figure 3.7. The signal at each labelled circuit node is monitored by 'oscilloscopes', the outputs of which are shown in Figure 3.8 for the 6.25 Gb/s and Figure 3.9 for the 10Gb/s. The simulation results are similar to each other though they have different symbol period. The proposed half-rate DFE logical operation proves to in these tests.

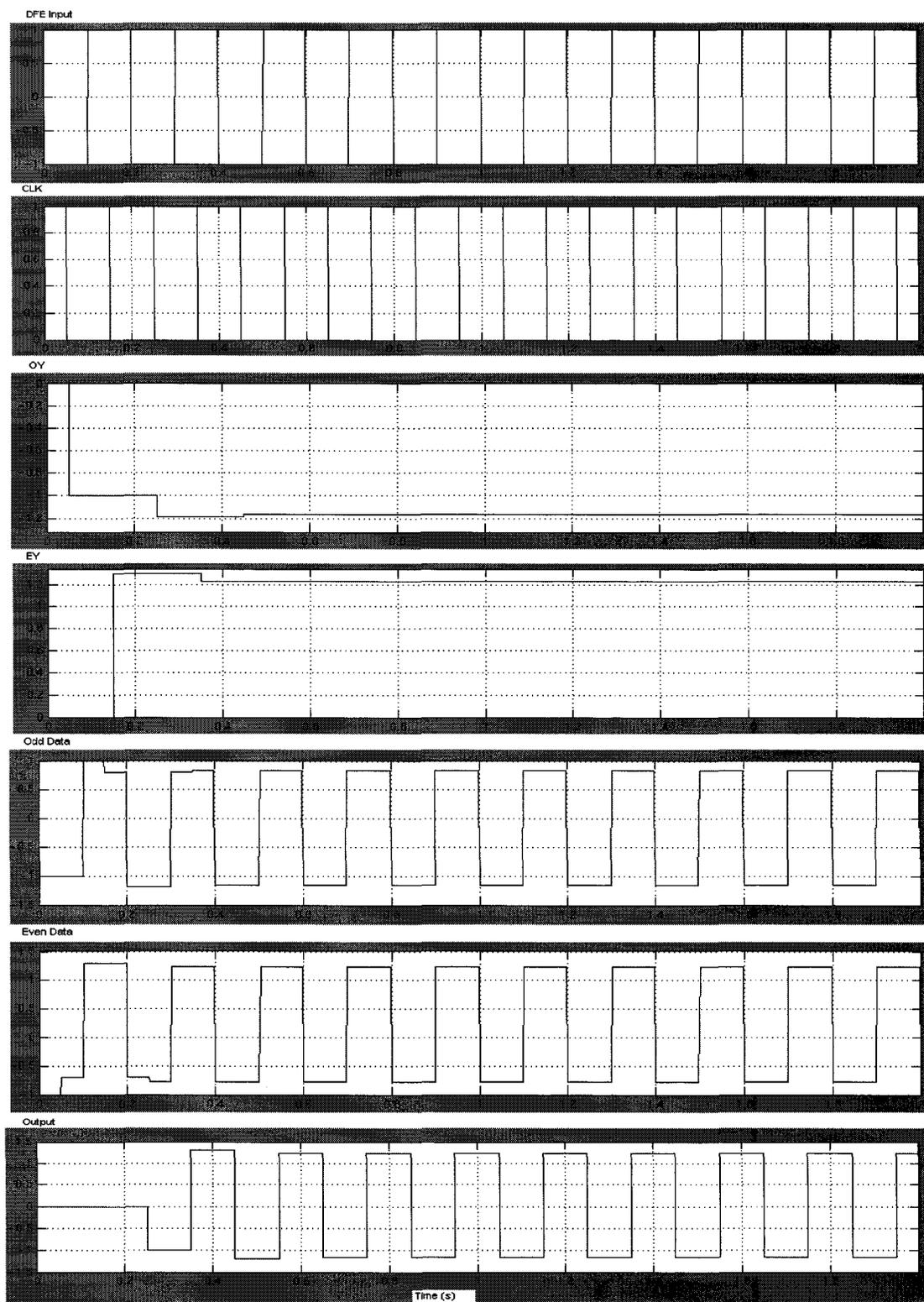


Figure 3.9: DFE data logic flow at data rate of 10Gb/s

3.3 Behavioral Modeling

Behavioral Modeling is very important in circuit design because it enables a top-down design style, it make it's possible to reliably improve a complete DFE design.

3.3.1 Modeling Half Rate DFE Operation

A complete half rate DFE behavior model was built. It was composed of two parts:

- 1) MATLAB code [28] to obtain necessary parameters;
- 2) System level and transistor level functional model blocks built in SIMULINK to simulate the performance of DFE in high speed backplane.

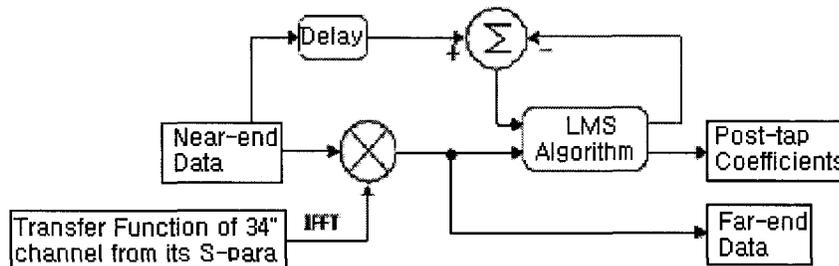


Figure 3.10: Flow diagram of first part of simulation diagram

The structure of DFE was already decided in Figure 3.3. The effective compensation for channel characteristics depends upon the values of the input FIR filter coefficients, which was obtained by MATLAB coding including LMS algorithm. The coefficient values were those which corresponded to the minimization of the sum of squared input-output errors found when comparing the values of a pseudo-random bit sequence (PRBS) [30] at either end of the transmission/reception link, a 34 inch FR-4 channel. The MATLAB simulation code for this task is shown in outline form in Figure 3.10.

Code included functions for the generation of transmitter-end PRBS, convolving it with the channel impulse function, recovery of it at the reception end and finally the LMS

code to evaluate the most favorable post tap coefficients to be used in subsequent behavioral modeling [28].

3.3.2 Channel Model

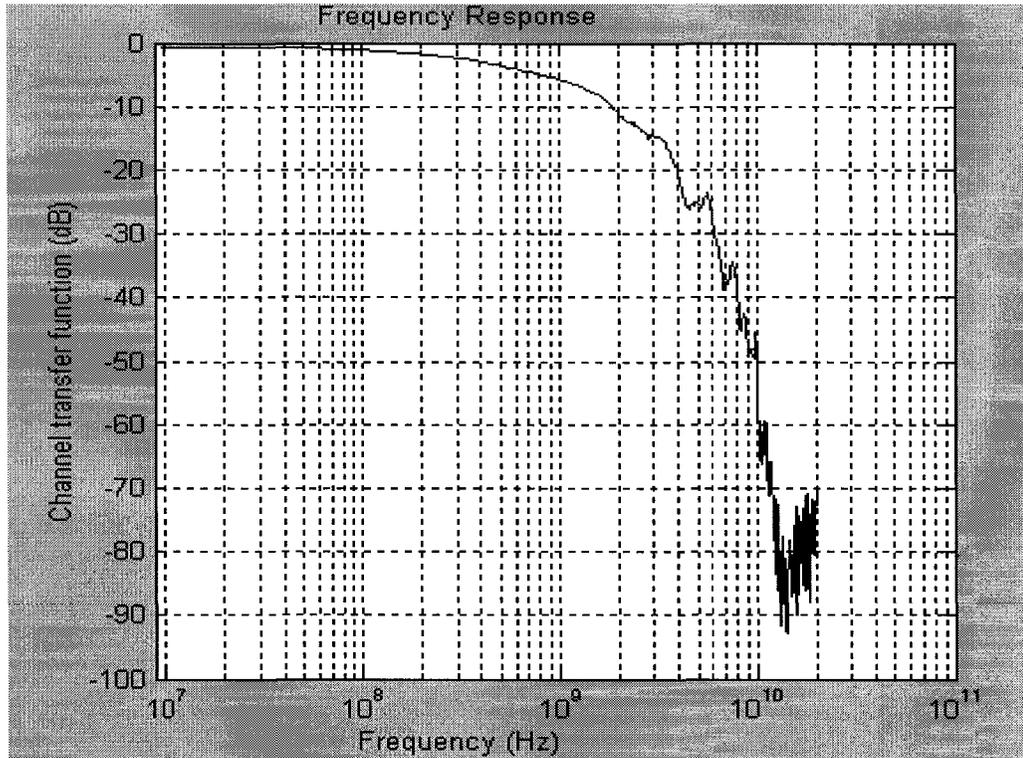


Figure 3.11: Channel transfer function of 34'' FR-4 channel

The transmitted data is distorted by the channel, and the channel impulse response depends strongly on the application. For the purposes of this thesis in the present case a thirty-four inch FR-4 channel model was chosen as being representative of the problems to be expected in high speed backplane communication arrangements.

Its frequency and impulse response are shown in Figure 3.11 and Figure 3.12 respectively [28]. Both the PRBS data generator and LMS code used in this research were developed by [28].

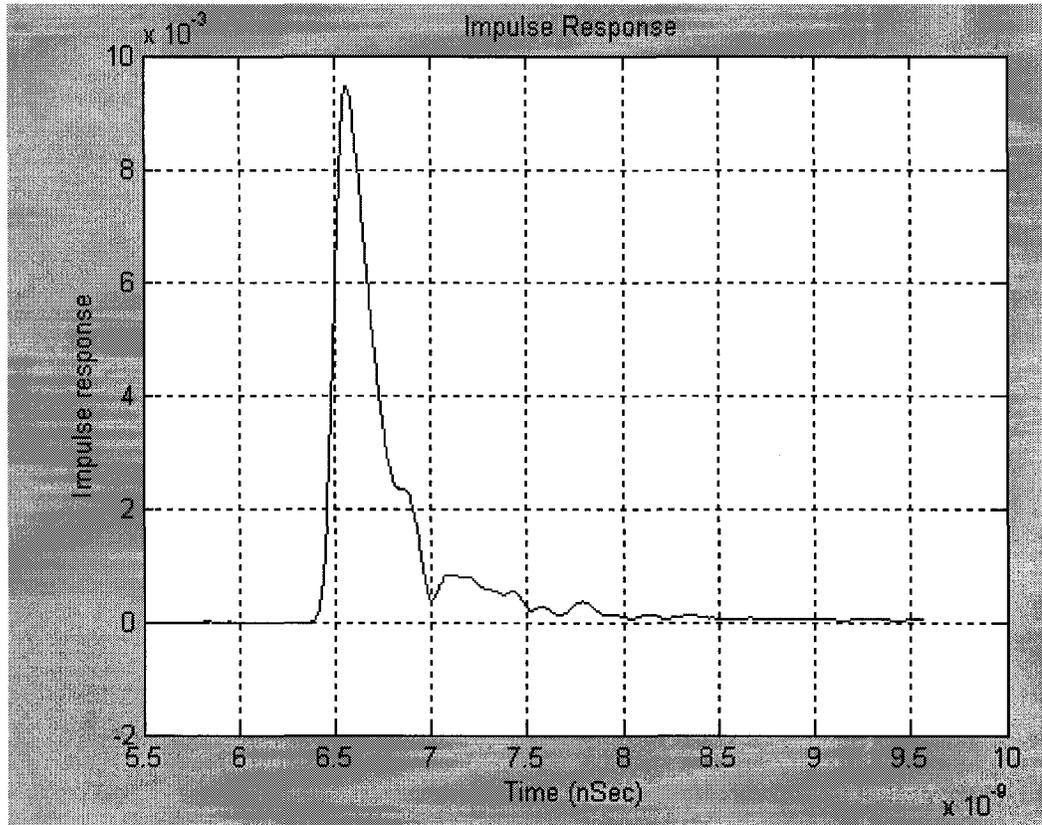


Figure 3.12: Impulse response of 34'' FR-4 channel at 8Gb/s

3.3.3 System Level Model in SIMULINK

The FIR filter coefficients having been obtained, it is now possible to import these parameters to the SIMULINK to start the behavioral modeling of the half rate DFE (HRDFE) in 34'' backplane, the success of which would mean that the DFE was feasible and that transistor-level design and implementation could begin.

With this in mind, simulation of the functional blocks was carried out, including that of the FIR equalizer, the DFF, the DETFF, the MUX and the entire integrated, pipelined DFE.

The test arrangement for the MATLAB/SIMULINK system level behavioral model used is shown in Figure 3.13. The interconnections of the individual functional blocks making up the HRDFE were outlined in Figure 3.3, and will be described in detail here.

The received data was that resulting from the passage of the MATLAB-generated transmit data through a 34" FR-4 channel.

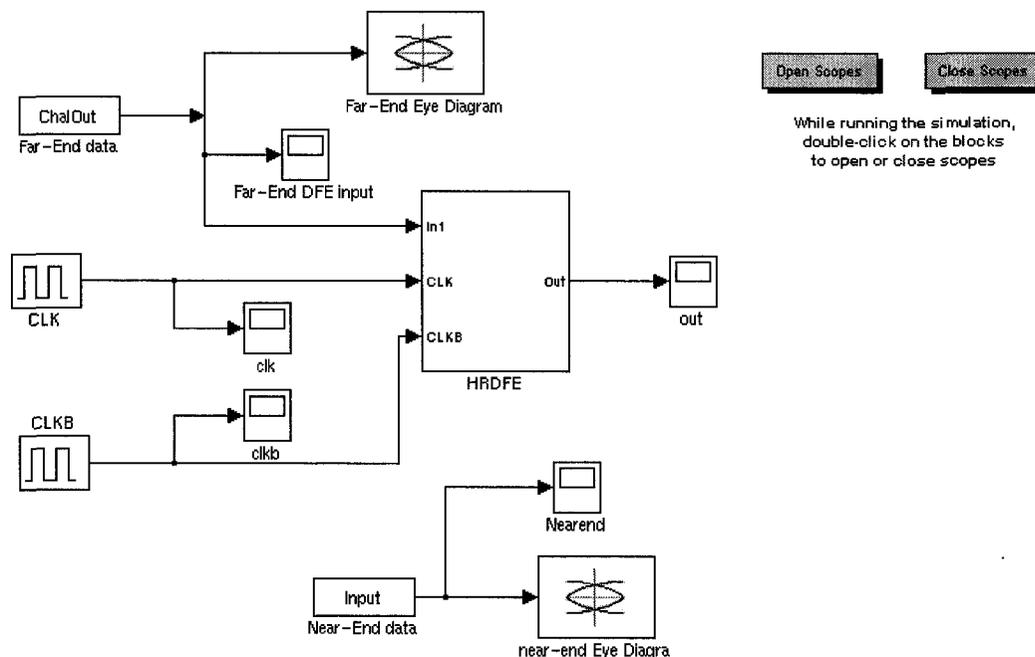


Figure 3.13: Modeling environment using SIMULINK

As described before, the SIMULINK pulse generator was used to supply the differential half-rate clock, and the clock was monitored by scope 'clk' and 'clkb'. The transmit-end PRBS9 $2^9 - 1$ bit data was compared with the received data to detect any discrepancies.

3.3.3.1 The Adder Block

Figure 3.14 is the adder block diagram. Its operation has been described in Section 2.2.1. The adder is composed of three gain blocks, the outputs of which are summed to form the block's output.

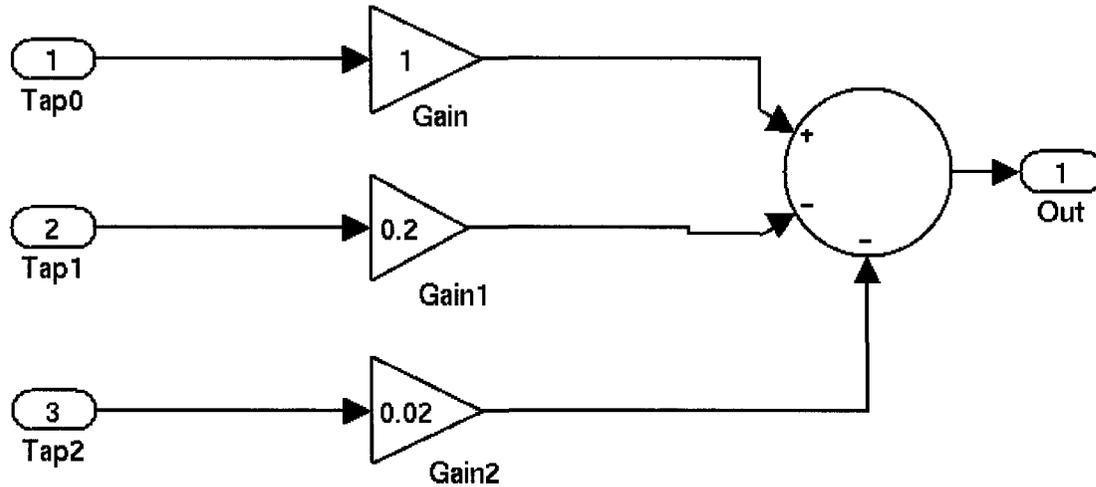


Figure 3.14: Adder block diagram

The gain blocks are analog multipliers, which form the products of the DFF and DETFF outputs with constant convolution coefficients computed with the LMS method.

The simulated coefficient values from LMS algorithm are shown in Table 4.2, – the first tap is the current, or reference tap, these values are used as initial ones.

TABLE 3.2: FIR coefficients calculated by MATLAB coding

	tap0	tap1	tap2
coefficient	1.0000	-0.44	-0.03

3.3.3.2 The D Flip-Flop (DFF) Block

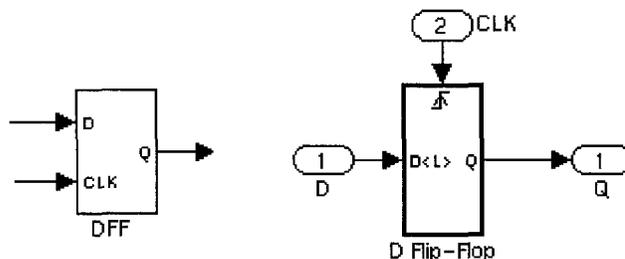


Figure 3.15: DFF block diagram

Figure 3.15 shows the SIMULINK D Flip flop model. The D flip-flop block has the following state table:

TABLE 3.3: DFF state table

$Q(t)$	$D(t)$	$Q(t_{next})$
0	0	0
0	1	1
1	0	0
1	1	1

$Q(t_{next})$ is the output immediately subsequent to an active (rising) clock edge which occurs when the chip is enabled ($\overline{CLR} = 1$).

The D flip-flop transfers data into a memory element (flip-flop) on each clock pulse (CLK). The chip-enable input signal, \overline{CLR} , is given the designation G (for gate) to indicate that this input enables the gated latch allowing data entry into the flip-flop.

The inputs and outputs of a modeled DFF are connected to the other blocks of a system by an 'Inport' (D), 'Outport' (Q) and 'Triggerport' (CLK) blocks. This is also true of the DETFF block.

An ‘Inport’ is a block that connects a level from an outside source to a simulated input – Inport blocks are distinguished from one another by port numbers which are assigned automatically by SIMULINK. Outport blocks likewise connect internal levels to external destinations (port numbers of these too are assigned automatically).

DFF Initial output: The initial output value is set to 0 before the subsystem executes, and also during times that it is disabled.

Trigger: The *CLK* active edge triggers the DFF subsystem. It stores a new data bit at the *Q* output until the arrival of the next *CLK* edge.

Trigger type: This parameter specifies the event type (‘rising’ or ‘falling’) which triggers a subsystem’s execution.

3.3.3.3 *The Multiplexer*

A 2:1 multiplexer is modeled by a 2-pole, single-throw switch (Figure 3.16), where the center connection is the selection input, and not a switch contact.

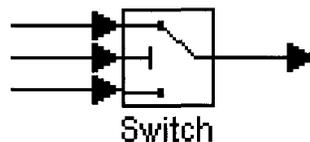


Figure 3.16: Switch block diagram

3.3.3.4 *The Dual-Edge Triggered Flip Flop (DETFF) Block*

The block diagram of a DETFF is shown in Figure 3.17. The model has six parts, namely an Inport, an Output, a Triggerport, two D-type Flip-Flop blocks and a Switch block. The relationship between the components will now be described.

Switch Block: Data from either of the DFF outputs is transferred by the switch, the source being determined by the state of CLK .

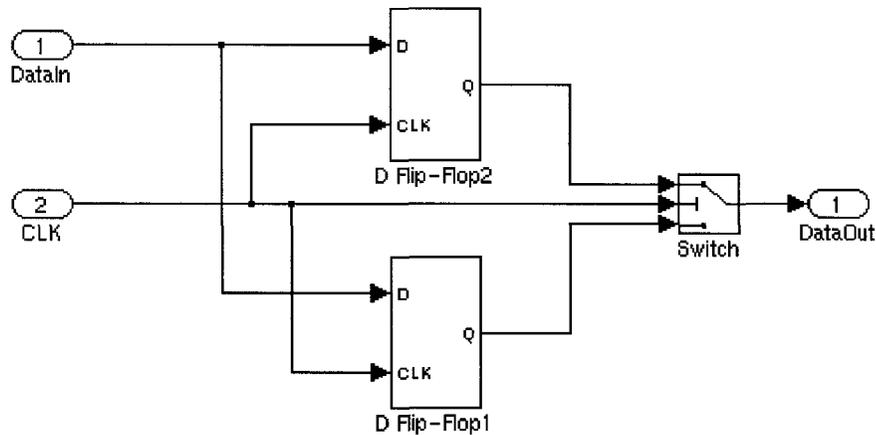


Figure 3.17: DETFF block diagram

Switch operation is determined by whether the control input value satisfies the condition that the control input value (clock pulse) be greater-than or equal-to a threshold value, or if it is not. If it is, then the input data to DFF #1 is transferred to the output; if it is not, then the input data to DFF #2 is transferred to the output. Note DFF #1 is triggered by $CLKB$ where DFF #2 is triggered by CLK .

The threshold is set to '0' in the case at hand. Zero Crossing Detection is turned on. When the system is disabled, a 'reset' level appears at the DETFF's output.

3.3.3.5 The Pipelined DFE Block

The complete pipelined 3-tap HRDFE is constructed in SIMULINK, the diagram is as Figure 3.18. Far-end data is imported to the DFE by port labelled 'In1', a differential pair of half-rate clock is imported to the port 'CLK' and 'CLKB'. Real-time monitors and eye diagram generators are inserted to the DFE circuit to obtain the simulation performances of even and odd branches equalizers and samplers. Recovered DFE output data is saved into file and output by output 1.

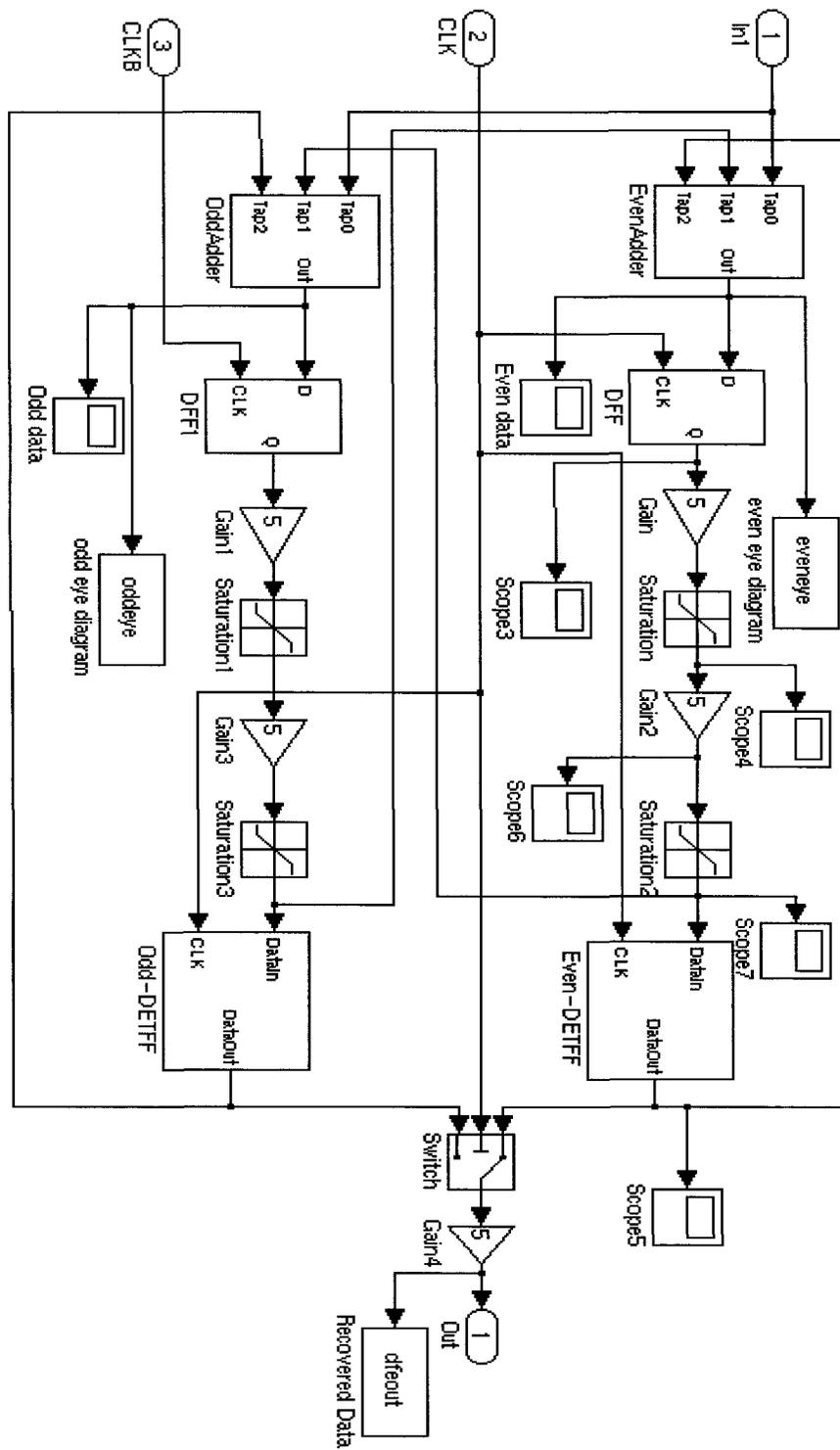


Figure 3.18: HRDFE

3.4 Simulation Results

In this section, results of the fixed coefficient 3-tap HRDFE simulation will be presented. The performance was evaluated in two ways: comparison of eye diagrams and of the input and output data streams. PRBS9 data generated from MATLAB coding was used to exercise the 34" FR-4 channel model at rates of 3.125Gb/s, 6.25Gb/s and 10Gb/s, the channel model comes from the measured S-parameters.

3.4.1 SIMULINK Results: 3.125Gb/s Input Data

The 3-tap receiver HRDFE correctly recovered 3.125 Gb/s input data.

Figures 3.19 through to 3.23 show eye diagrams involving transmit and receive-end data, odd arm and even arm equalizer outputs, and of recovered data respectively. The transmit-end eye diagram of Figure 3.19 shows that the transmitted data are basically ideal. But the receive-end eye diagram is almost closed – a result of channel attenuation at this speed. The data collected in the even and odd arms showed that the equalization resulted in a widening of the eyes, along both of the time and amplitude axes as can be seen in Figures 3.21 and 3.22. Figure 3.23 is the eye diagram of the simulated recovered data – one can see that the data is totally recovered. Eye-widening to 0.96 UI in the horizontal (time) direction is observed, and to 0.5 V in the vertical amplitude comparing to 0.16V at the DFE input. The eye diagram after a even/odd branch DFE has a vertical opening of 0.12 V.

Figure 3.24 compared the near-end data and recovered data, from the graphic it is observed that all the data are matched, there are no BER with PRBS9 input data at 3.125Gb/s transmission speed.

3.4.2 SIMULINK Results: 6.25Gb/s Input Data

The behavioral modeling results of the 3-tap HRDFE running at 6.25 Gb/s are shown in Figures 3.25 to 3.30. The Figures show the eye diagrams of the transmitted data stream in Figure 3.26, of the received data in Figure 3.27, of the odd in Figure 3.28 and even-arm equalizer output in Figure 3.29, and of the recovered data in Figure 3.30. Once again, the transmitted data exhibits a nearly perfect eye-diagram. And the far-end eye diagram is almost closed, a consequence of channel attenuation at this data rate. Eye-widening to 0.96 UI in the horizontal (time) direction is observed, and to 0.5 V in the amplitude direction after the DFE recovered and data integrated comparing to far-end 0.1 V. The eye diagram after a even/odd branch DFE has a vertical opening of 0.034 V.

Nonetheless, accurate recovery of the transmitted data is clearly shown by Figure 3.30.

3.4.3 SIMULINK Results: 10Gb/s Input Data

At data rate of 10Gb/s, the results of the 3.125 and 6.25 Gb/s experiments were duplicated.

Figures 3.31 and 3.32 show the eye diagrams of the transmitted data and of the received data. In Figures 3.33 and 3.34 can be seen the eye diagrams of the odd and even arms of the equalizer, and in Figure 3.35 that of the recovered data. While the transmitted data shows an almost perfect eye diagram, the reverse is true of the unequalized data at the receiving end, where extreme effects of dispersion and attenuation of the arriving signal are noticed. The even and odd-branch eye diagrams indicate considerable improvement over this. Widenings on the time and amplitude axes to 0.45UI and 0.5 V in the amplitude direction after the DFE recovered and data integrated comparing to far-end 0.075 V. The eye diagram after a even/odd branch DFE has a vertical opening of 0.015 V are observed.

The equalizer seems to be able to recover the sent data accurately in this last case, 10Gb/s, which was the design goal.

Figure 3.36 compares the transmitted data to the recovered data. From the graphic it is observed that all the data are matched up to a time shift, and that there is a zero BER with PRBS9 input data at 10Gb/s transmission speed.

3.5 Conclusion

The eye diagrams of Section 3.4 show significant improvement in the received data quality when the new 3-tap half-rate Decision Feedback Equalizer is used to compensate for intersymbol interference on a FR-4 backplane transmission channel. The necessary speed was achieved by moving from a conventional full-rate one post-tap circuit to a half-rate pipelined multi post-taps structure, a change which lightened the design burdens normally encountered by the high-speed communication engineer by reducing the sampling frequency to half of what it would otherwise be at the new bandwidth. The results, which were adequate for a 34 inch FR-4 channel carrying 10Gb/s data, were achieved with a two post-tap scheme; an extension of the idea, to an equalizer design of a higher order, would probably be made to work in yet more challenging environments.

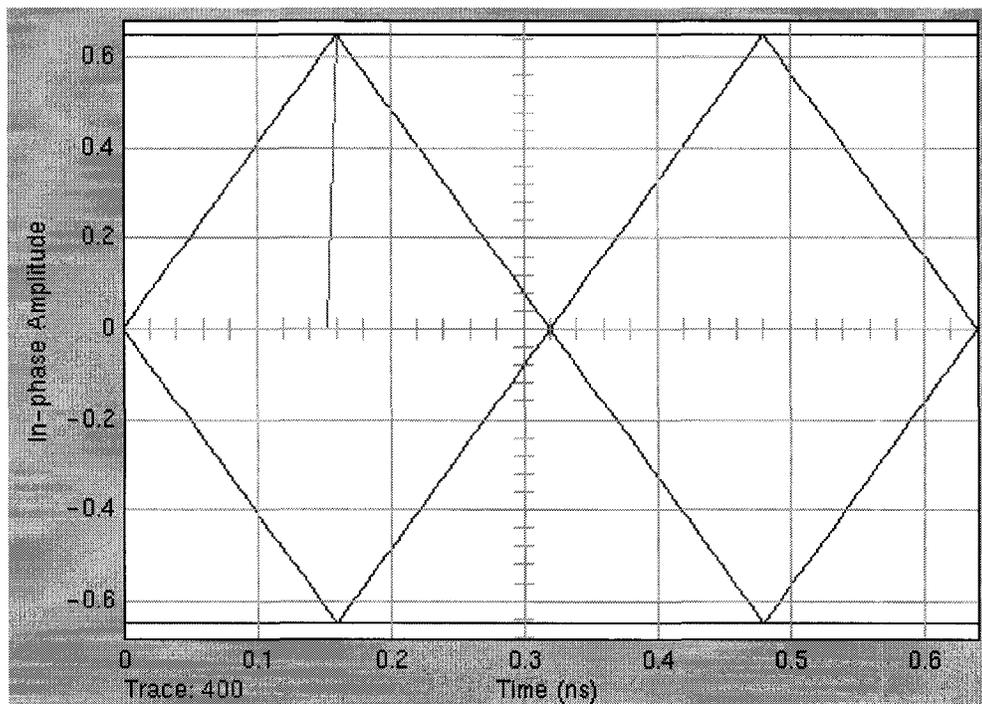


Figure 3.19: Near-end data eye at 3.125Gb/s

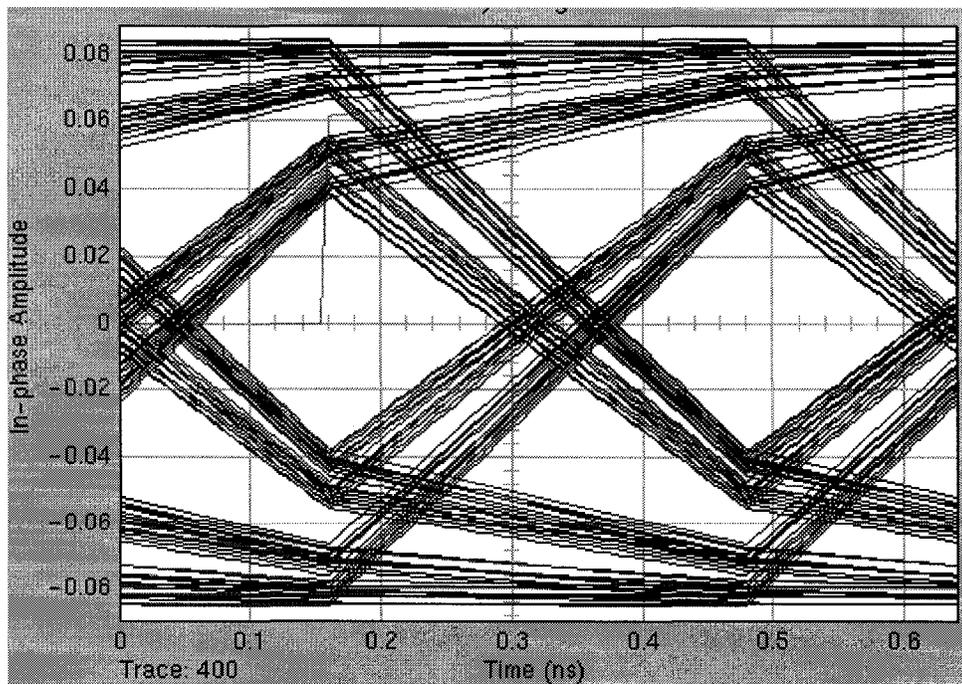


Figure 3.20: Far-end data eye at 3.125Gb/s

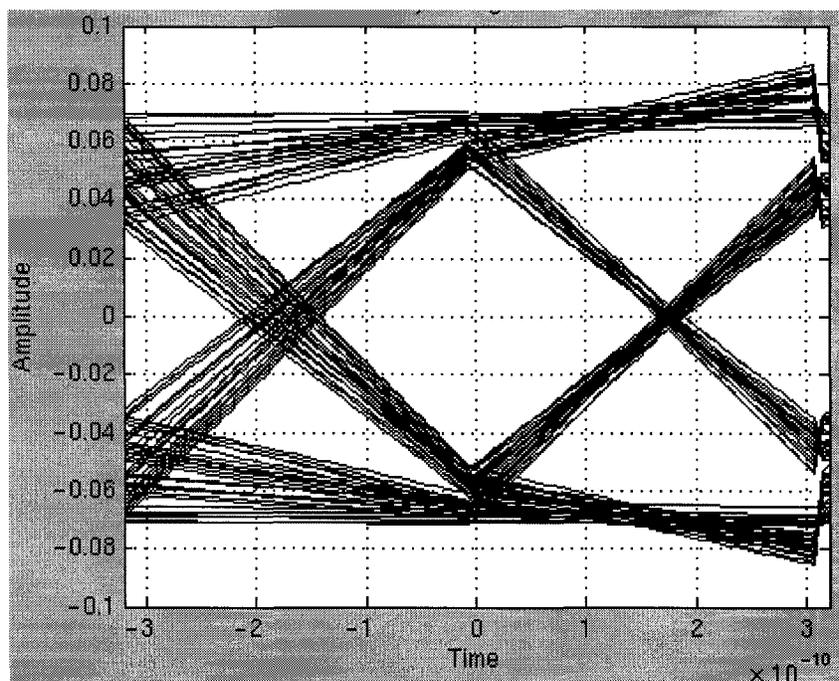


Figure 3.21: Eye diagram of output of odd arm equalizer at 3.125Gb/s

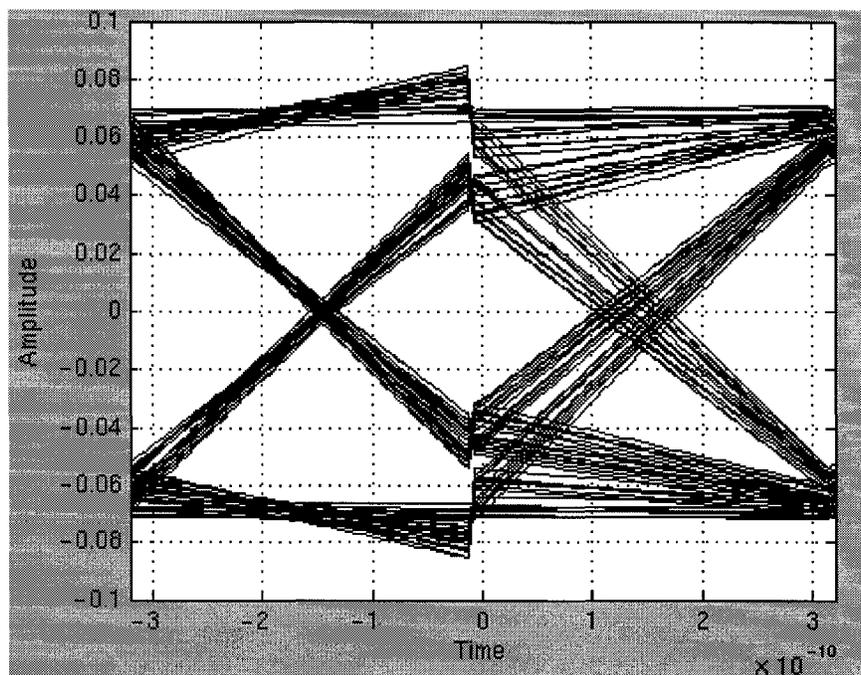


Figure 3.22: Eye diagram of output of even arm equalizer at 3.125Gb/s

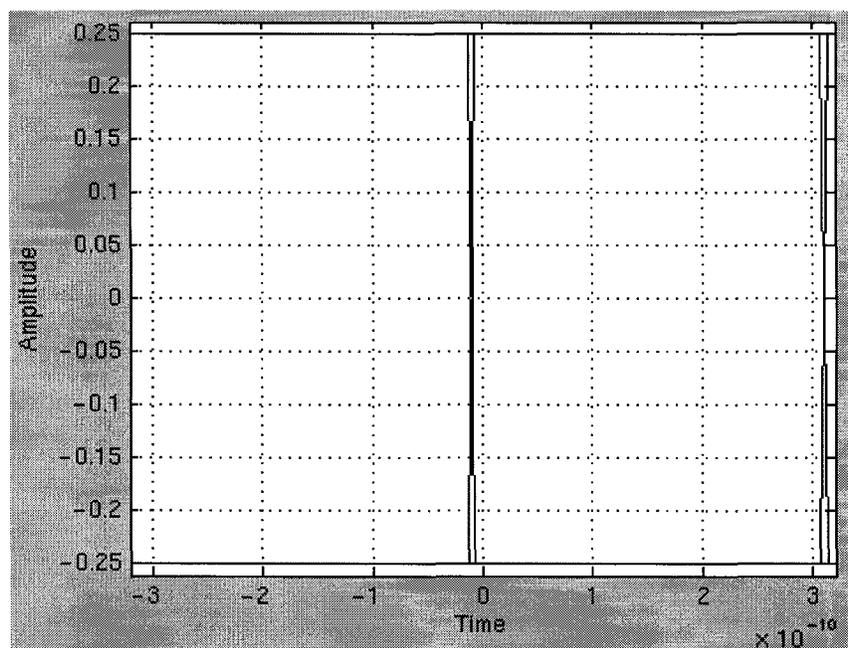


Figure 3.23: Eye diagram of output of equalizer at 3.125Gb/s

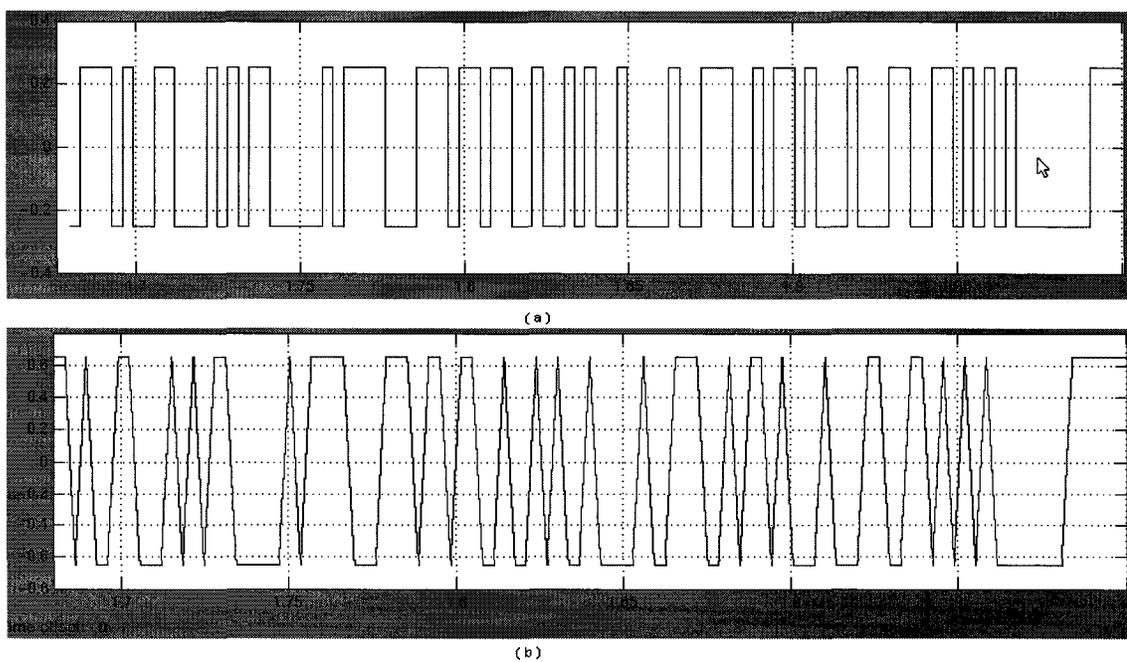


Figure 3.24: Input output stream comparison (a) near-end data vs. (b) HRDFE recovered data at 3.125Gb/s operation speed

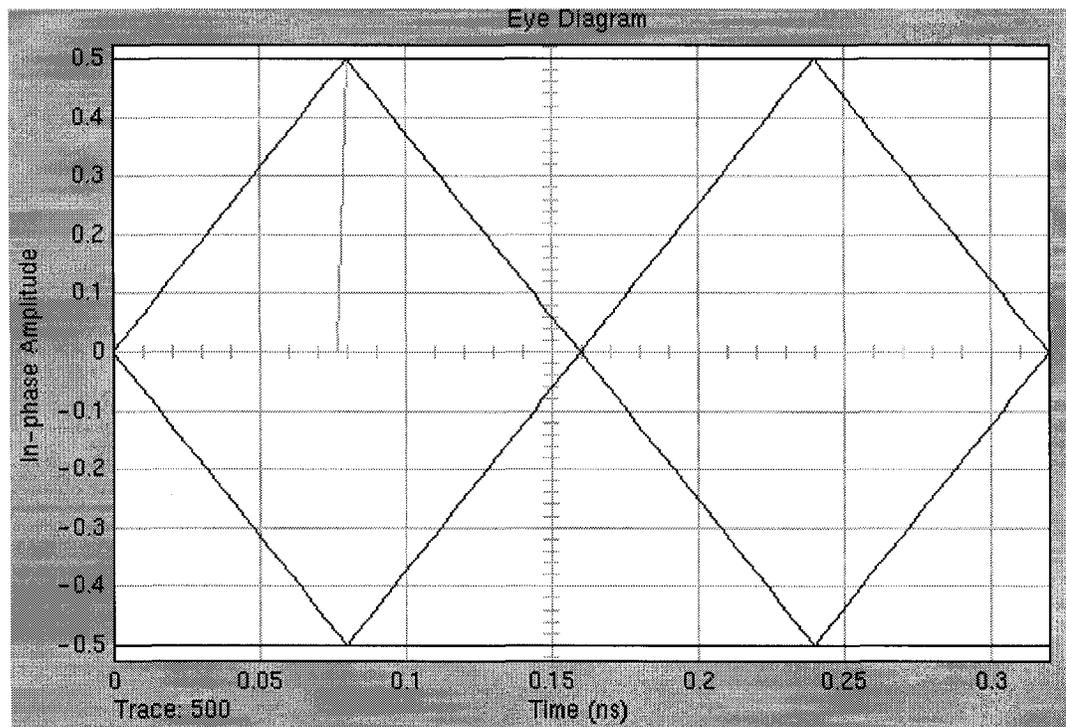


Figure 3.25: Near-end data eye at 6.25Gb/s

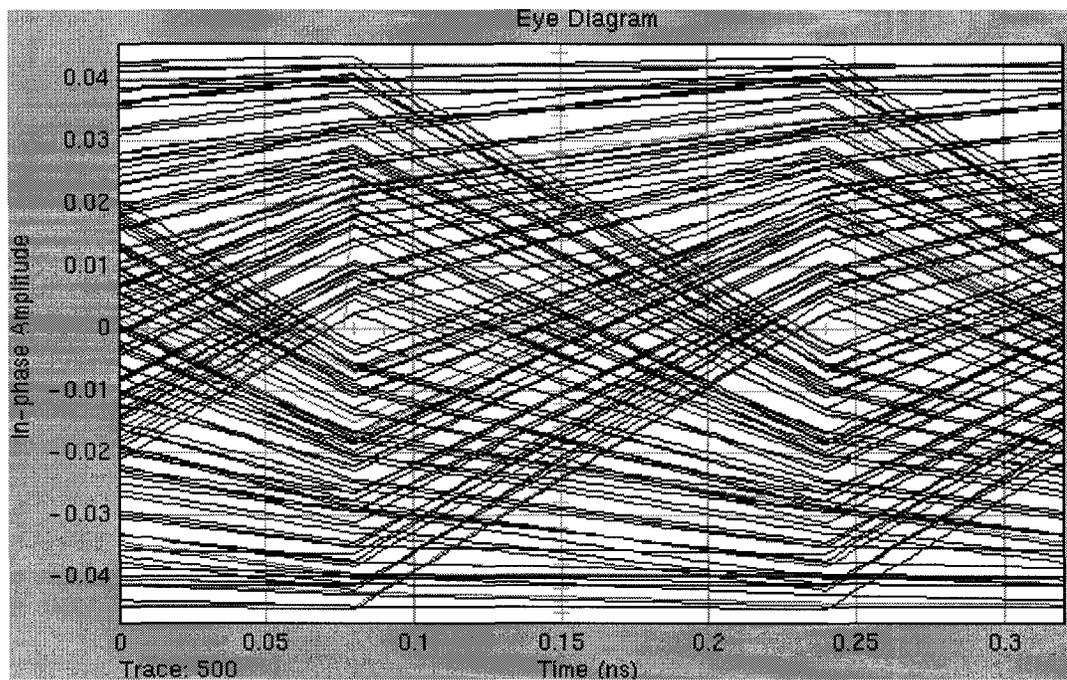


Figure 3.26: Far-end data eye at 6.25Gb/s

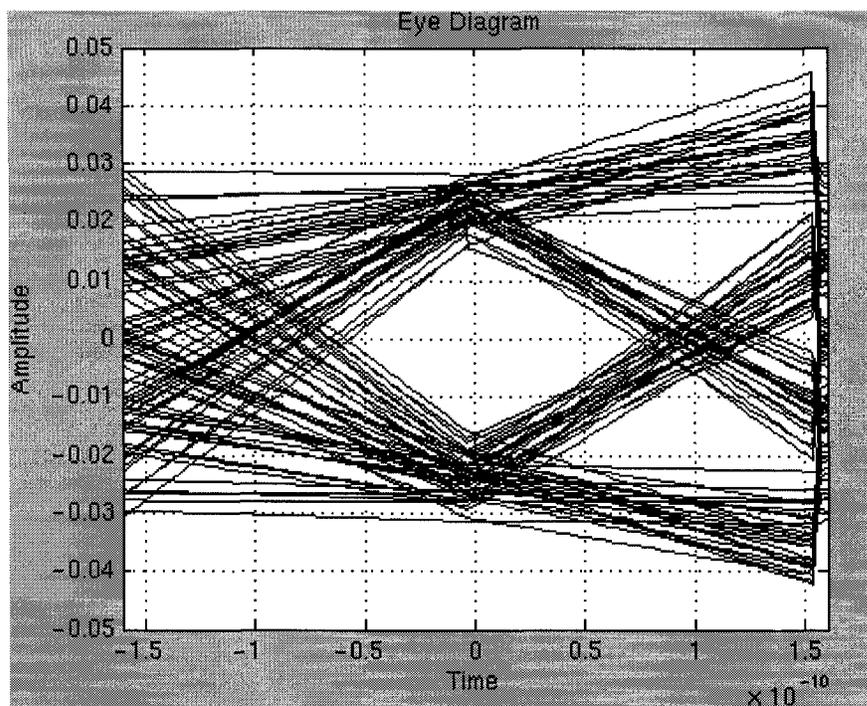


Figure 3.27: Eye diagram of output of odd arm equalizer at 6.25Gb/s

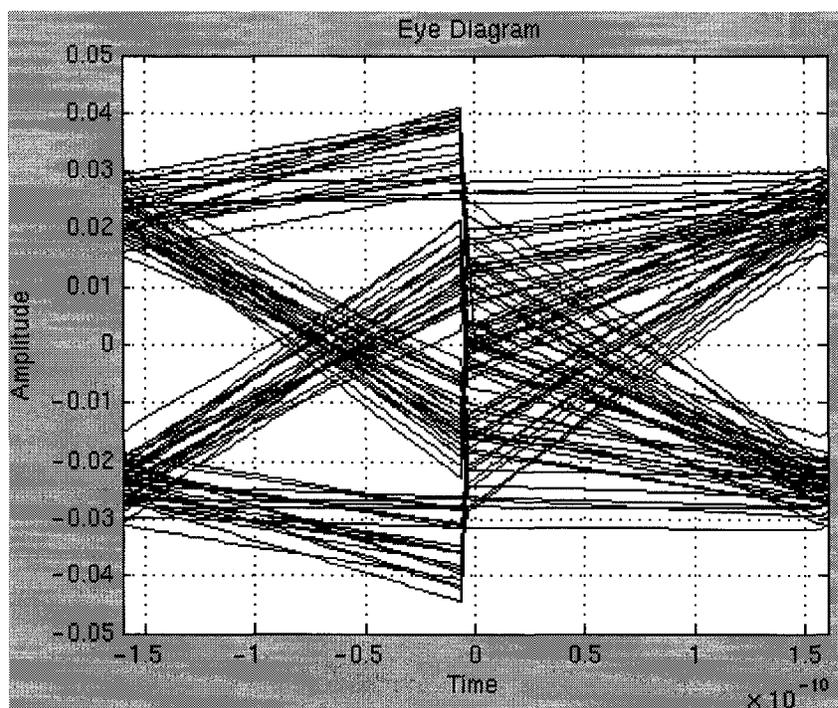


Figure 3.28: Eye diagram of output of even arm equalizer at 6.25Gb/s

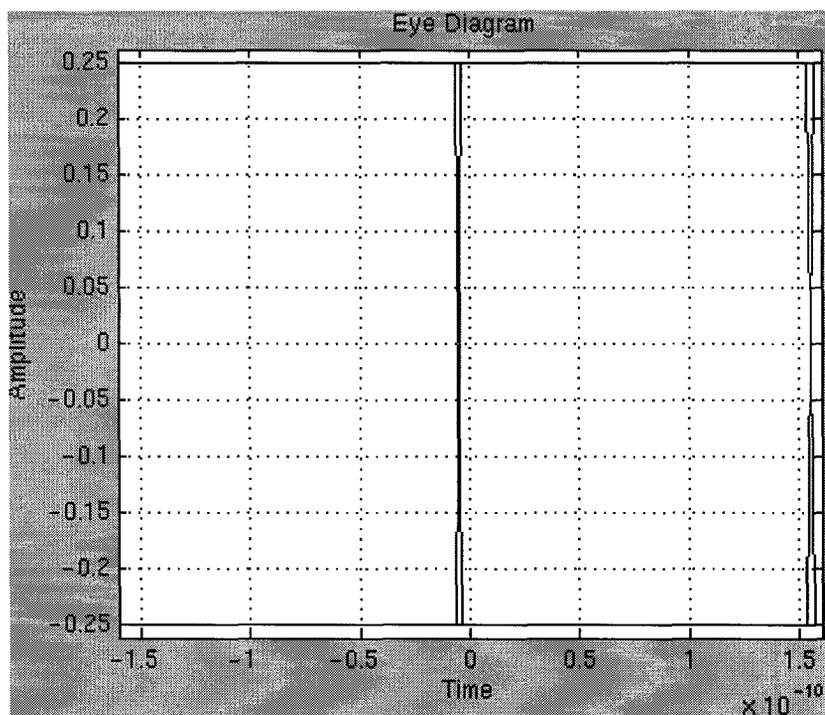


Figure 3.29: Output of DFE equalizer at 6.25Gb/s

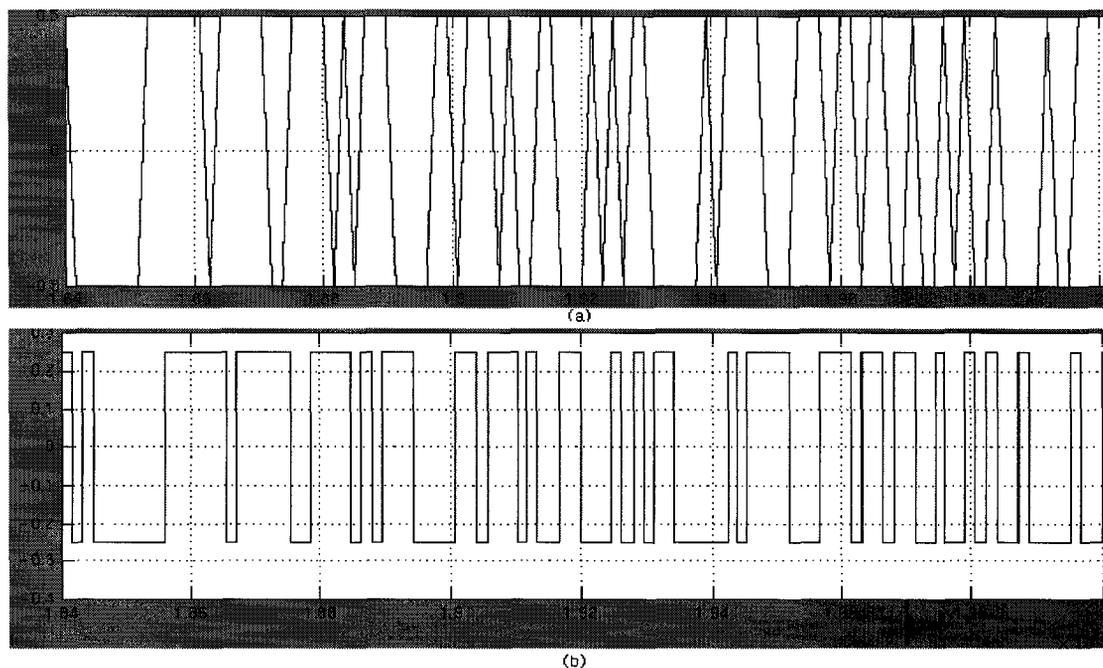


Figure 3.30: Input output stream comparison (a) near-end data vs. (b) HRDFE recovered data at 6.25Gb/s operation speed

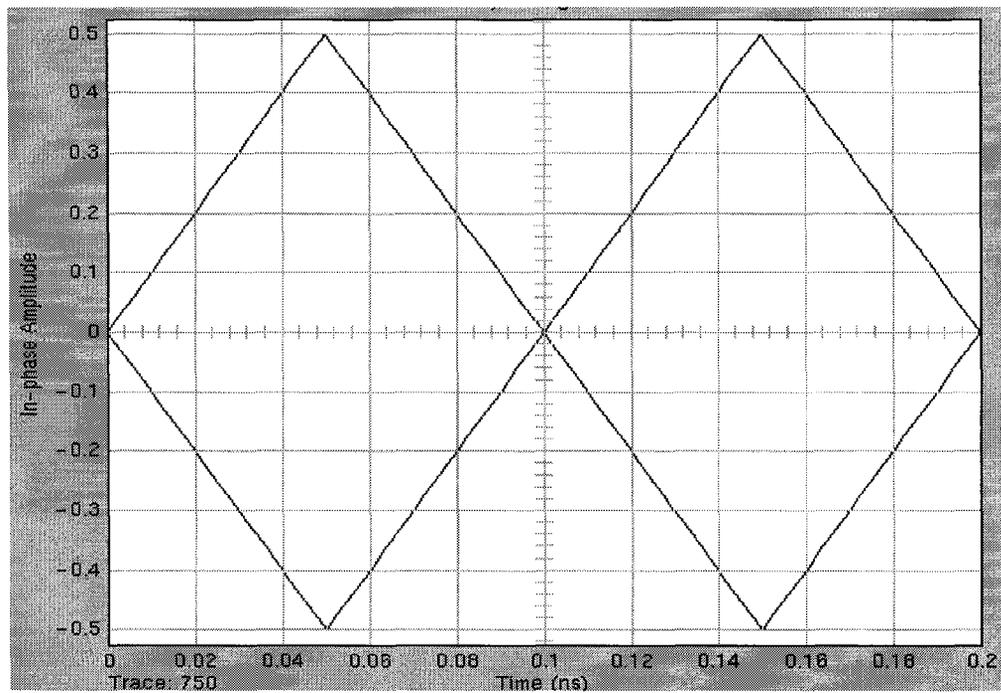


Figure 3.31: Near-end data eye at 10Gb/s

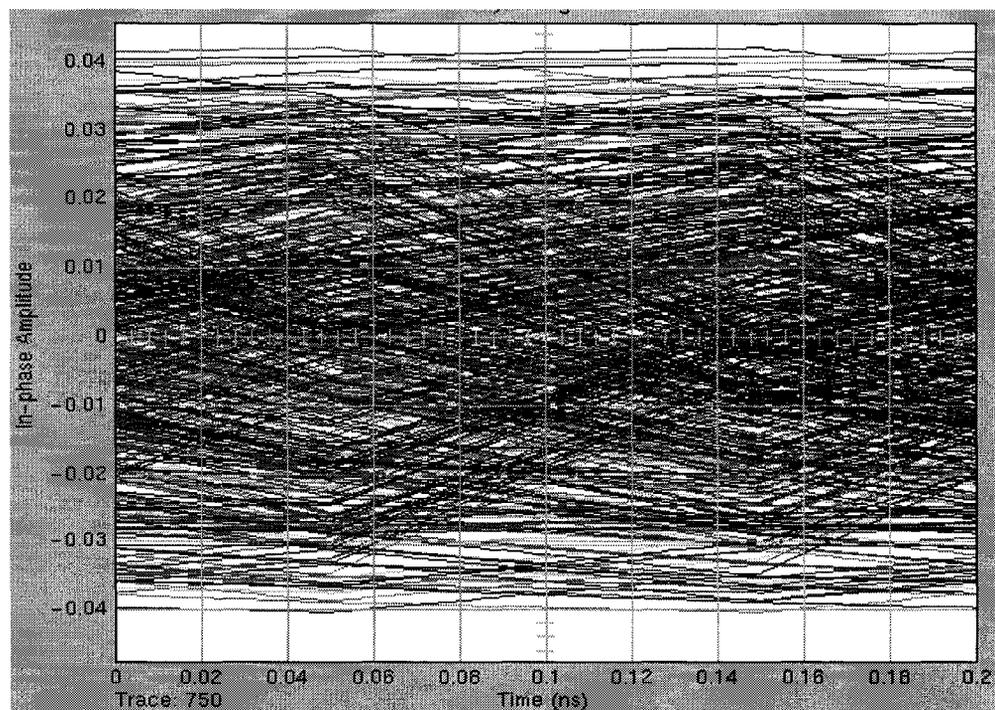


Figure 3.32: Far-end data eye at 10Gb/s

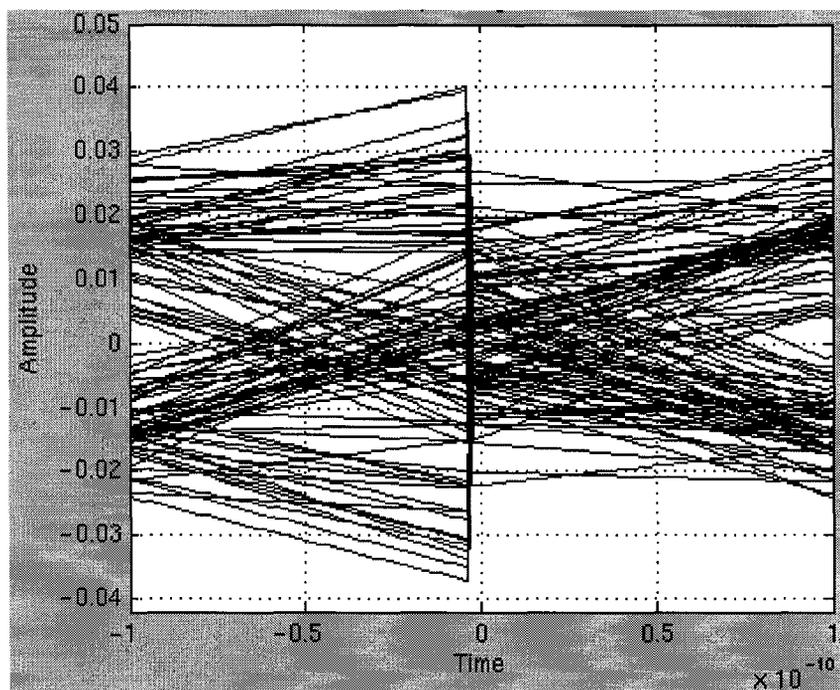


Figure 3.33: Eye diagram of output of odd arm equalizer at 10Gb/s

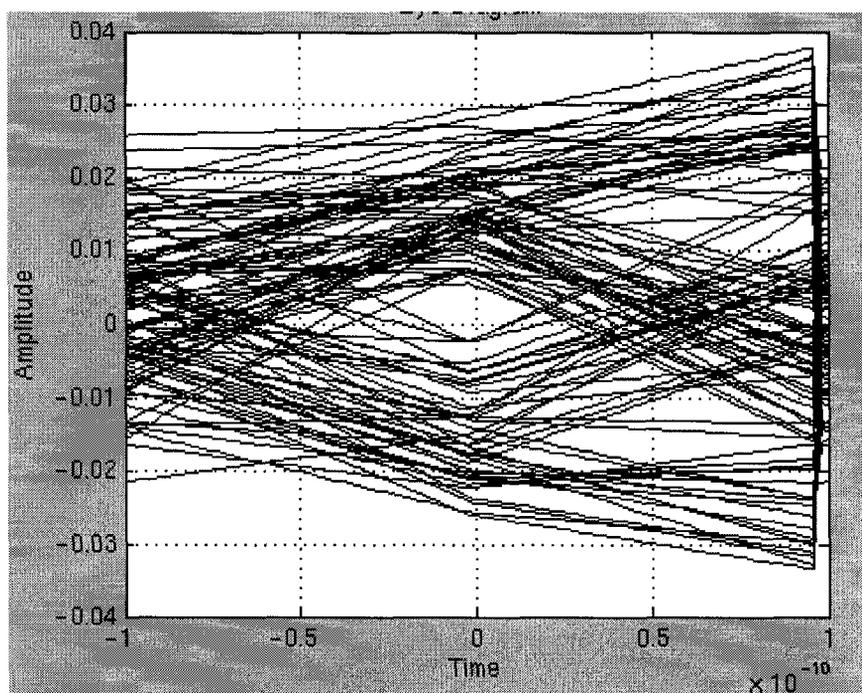


Figure 3.34: Eye diagram of output of even arm equalizer at 10Gb/s

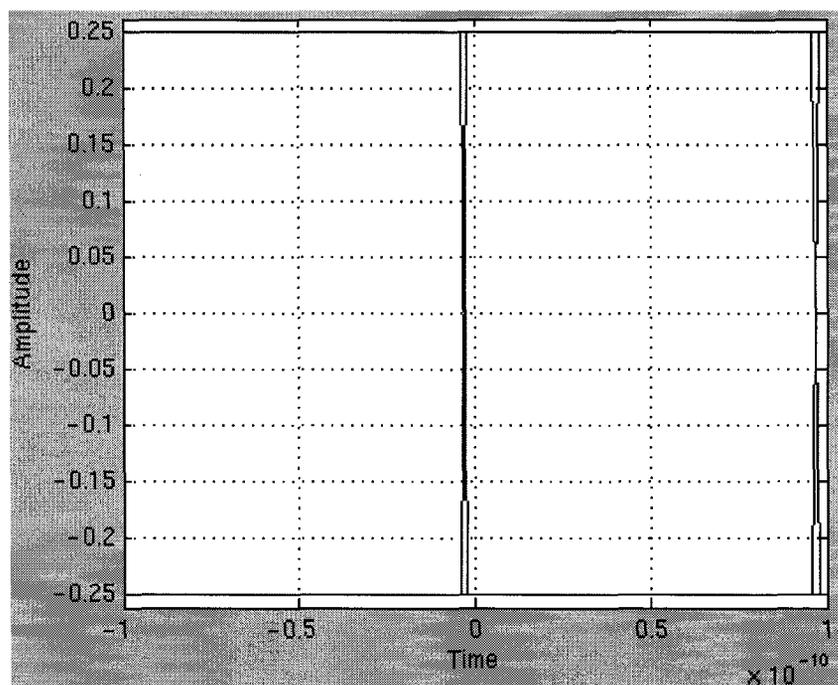


Figure 3.35: Output of DFE equalizer at 10Gb/s

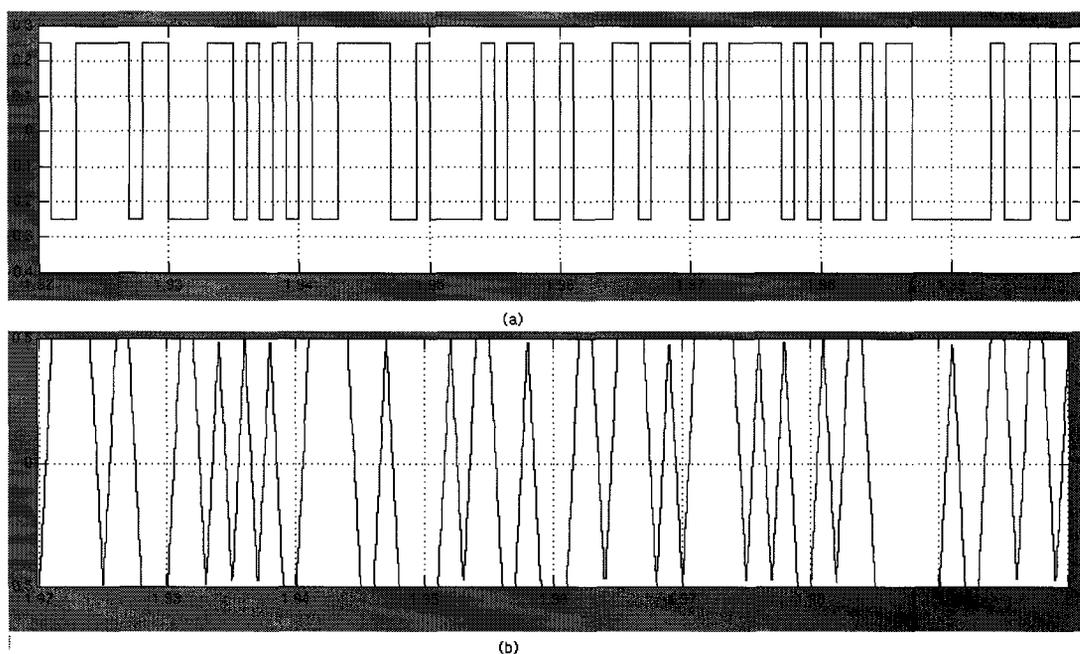


Figure 3.36: Input output stream comparison (a) near-end data vs. (b) HRDFE recovered data at 10Gb/s operation speed

Design of the Half Rate DFE at the Transistor Level

The behavioral modeling described in the last section provided a proof of concept for the new half rate DFE design, but specific parameter values to be used in the circuit design remain to be determined. The next step is taken in this chapter, the functional blocks used in Chapter 3, the FIR equalizer, the D flip flop (DFF), the dual-edge triggered flip flop (DETFF) and assorted buffers will be designed at the device level and then simulated to verify correct operation of the assembly of same.

Current mode logic (CML) circuit technique chosen for the implementation under TSMC CMOS 0.18 μm design rules because of its low propagation delay and small voltage swing.

The application of pre- and post-layout simulation to validate the design for data rates of up to 8Gbps will be described. A bit-error-rate estimation will be derived from the simulation results.

4.1 Transistor Level Design

4.1.1 Realization of the Three-Tap FIR Equalizer

A CML structured three-tap FIR equalizer is shown in Figure 4.1. In transistor level design, the tap coefficients are controlled by current sources, the tap coefficients C_i are defined as normalized currents I_i with respect to the main tap current I_0 .

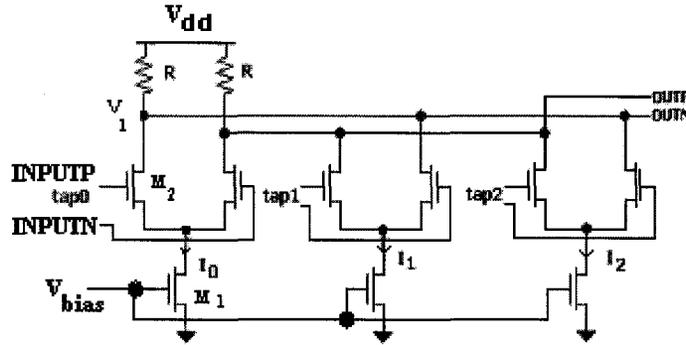


Figure 4.1: 3-tap FIR equalizer circuit

The expression for C_i is:

$$|C_i| = \frac{I_i}{I_0} \quad (4.1)$$

As is usual for a CMOS 0.18 μm process, $V_{dd} = 1.8\text{V}$. The common-mode voltage for the differential inputs is set to $V_{com} = 1.3\text{V}$. A current source of $150\mu\text{A}$ is provided. In either of the two arms of the equalizer, a 5x size for transistor M1 is selected and with its gate connected to V_{bias} , a current of $I_0 = 750\mu\text{A}$ for the main tap (tap0) is obtained. Length of M_1 is chosen big enough to keep the current I_0 stable when V_{Ds} is varying within saturation region.

Note that all tap currents I_i obey (4.2),

$$I_i = K_c \left(\frac{W}{L} \right)_i (V_{GS} - V_{th})^2 \quad (4.2)$$

where K_c has a constant value of $8.17e-5$ amp/Volt² and the threshold voltage, V_{th} , is obtained from SPECTRE simulation results $V_{th} = 516mV$.

The ratio of transistor width to length (W/L) can be obtained by solving (4.2) for I, thus

$$\left(\frac{W}{L}\right)_0 = \frac{I_0}{K_c(V_{GS} - V_{th})^2} \quad (4.3)$$

Substitute all the parameters to (4.3) we can obtain that:

$$\left(\frac{W}{L}\right)_0 \cong 44.62 \quad (4.4)$$

If (W/L)= 750nm/180nm is defined to be one cell unit, the first tap transistor, M2, will have a W/L of 5 of these units. And all the transistor in the three differential pairs share the same W/L size in the FIR equalizer.

Next step is to find the load resistance of this circuit. Set V1 as 1.3 V as common mode voltage, and the circuit can maximum have a swing of 1 V, it is seen to satisfy:

$$V_1 = V_{dd} - (I_0 + I_1 + I_2) \times R \quad (4.5)$$

from which a preliminary value for R is found to be 512 Ω . After pre-layout simulation, the optimal value of R for the circuit operation is found to be 500 Ω .

4.1.2 D-Latch Flip-Flop Implementation

The CML based Master-Slave DFF circuit, whose SPECTRE model of which is shown in Figure 4.2, is composed of two identical D-latches. The DFF circuit is triggered by a half-rate clock and generates a two-symbol delay in the data sequence. The transistor size of the signal input pair and clock input pair is designed to be 3X driving capability in order to ensure proper operation of the pipelined feedback structure. A current-mirror transistor size of $20\mu/1\mu$ is selected to guarantee stability of the current supply. The load

resistance R_{DFF} is found again using simulation and turned out to be 700Ω . The DFF will introduce two-symbol delay into the data stream.

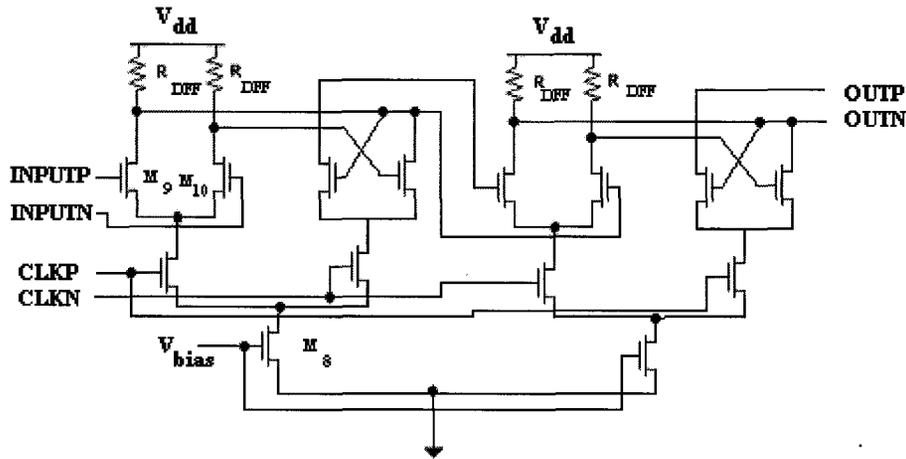


Figure 4.2: DFF cell

4.1.3 2:1 Multiplexer Implementation

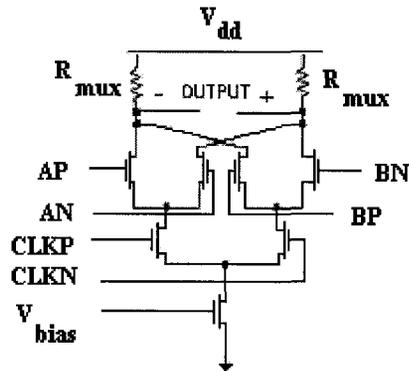


Figure 4.3: Multiplexer Cell

The CML-based 2:1 multiplexer (MUX) circuit of Figure 4.3 is composed of two differential pairs having cross-coupled outputs. This circuit is triggered by the same half-rate clock as is applied to the DFF, when the clock level at port $CLKP$ is high, the signals

at Port A (AP and AN) will be transferred to the MUX output, and when it is low the signals at Port B (BP and BN) will be passed.

4.1.4 Dual Edge Triggered Flip Flop (DETFF) Implementation

The cell structure of a Half-rate DETFF, an adaptation of the dual-edge triggered flip-flop described in [46], is shown in Figure 4.4. Its role in the DFE is the generation of symbol-spaced sequences by multiplexing the outputs of two DFFs clocked on opposite clock phases.

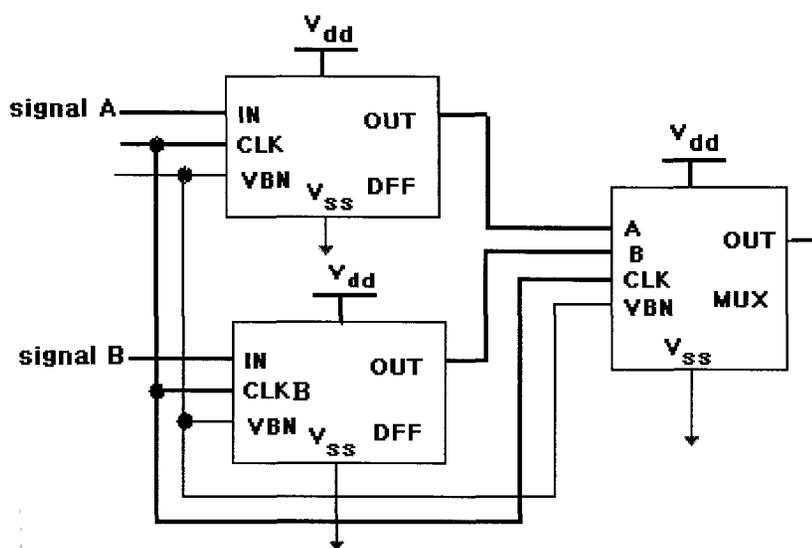


Figure 4.4: DETFF cell

4.1.5 Three-Tap Half Rate DFE

A complete half rate DFE circuit is obtained on combining the circuit blocks previously described. The structure of one arm of the parallel, cross-coupled structure is shown in Figure 4.5 part I and Figure 4.6 part II.

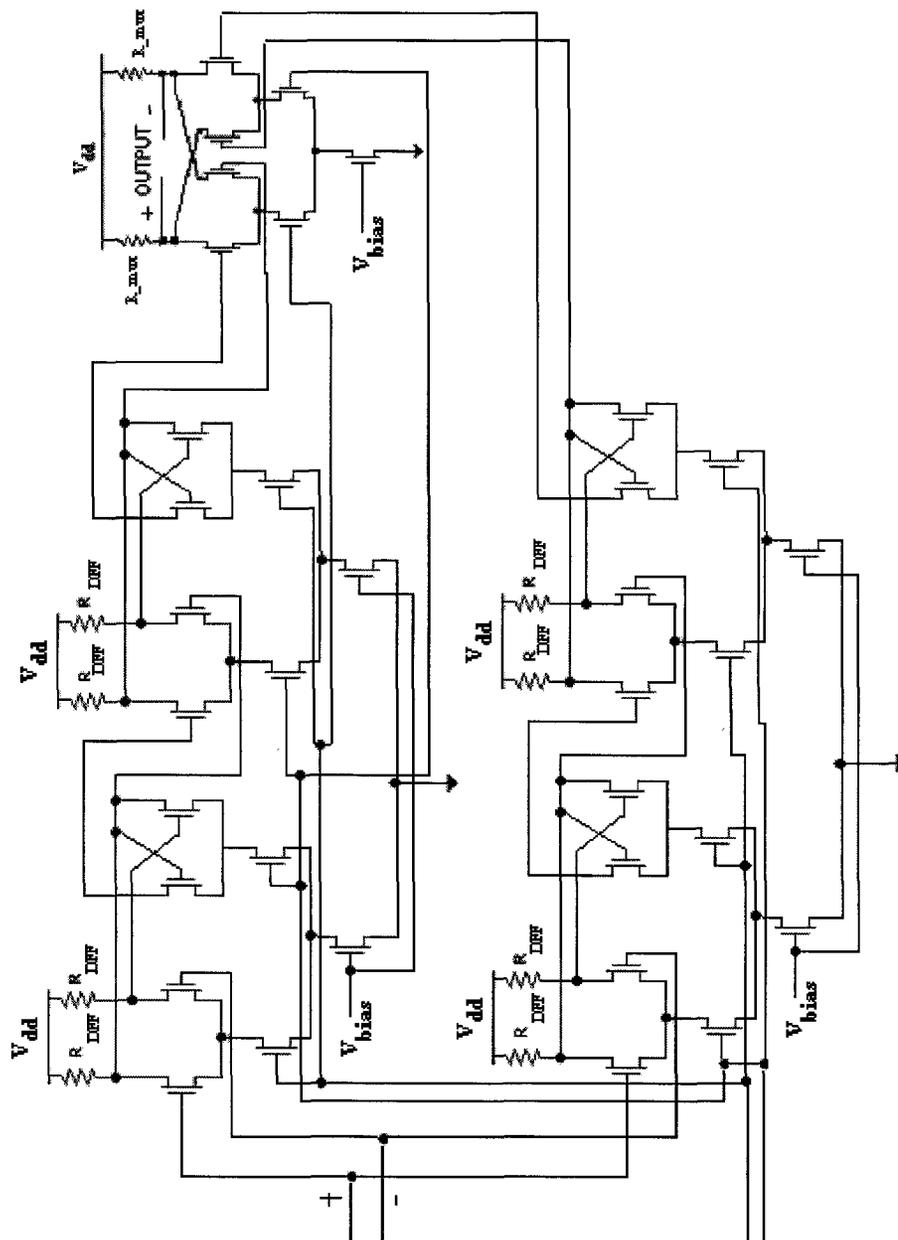


Figure 4.6: Structure of one arm of half-rate DFE circuit (II)

The testbench of designed DFE is shown in Figure 4.7. The data presented to the DFE input is a MATLAB coding generated RPBS9, 511 bits in length. The polynomial used in the generator was primitive so that non-trivial bit pattern repetitions are not possible. The differential components of this signal being labelled *CHAL_OUTP* and *CHAL_OUTN* in this graphic. The components of the DFE output signal are likewise denoted *DFE_OUTP* and *DFE_OUTN*. Furthermore, a comparison between the Matlab-generated transmitted data *CHAL_INP* and *CHAL_INN*, corresponding to the channel-distorted *CHAN_OUTs*, and the DFE-processed received data is made. The half rate clock signals are also recovered as indicated schematically in the lower part of the diagram

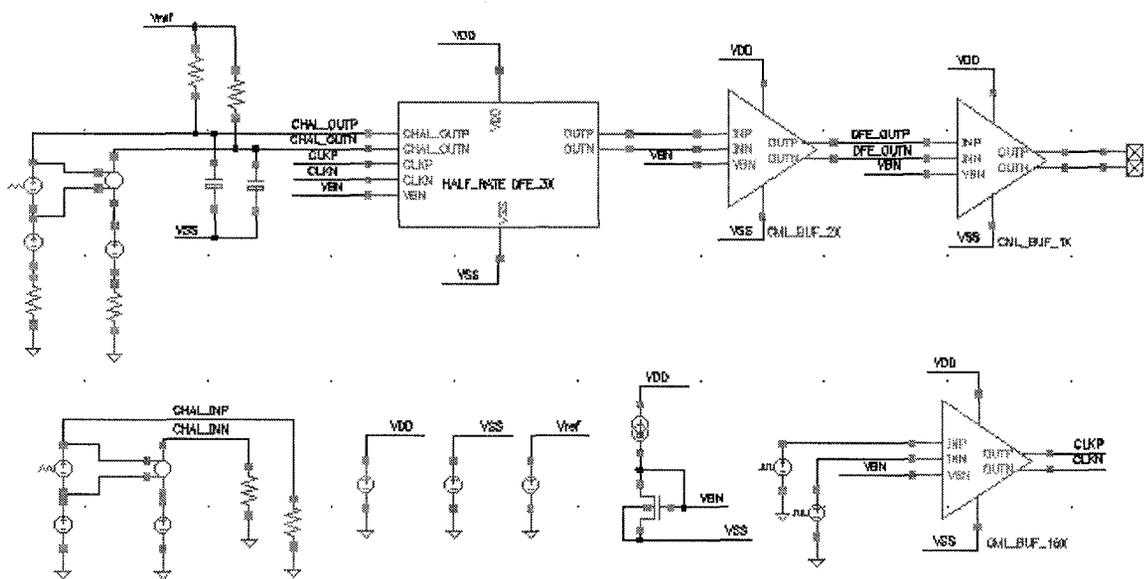


Figure 4.7: DFE test arrangement

4.1.6 Testing the Three-Tap Half Rate DFE (HRDFE)

In Chapter 3, the logic functions of the DFE were validated with behavioral block level testing using SIMULINK. In this section, SPECTRE simulation is used to demonstrate that the same is true at the transistor level.

4.2 DFE Step Response

To start with, the step response of the DFE circuit at 8Gb/s will be examined.

An explicit form for the convolution of (3.2) is that of (4.6), where coefficients are used whose values are approximately equal to the optimized ones obtained with behavioral modeling:

$$y(n) = x(n) - 0.2\hat{x}(n-1) - 0.1\hat{x}(n-2) \quad (4.6)$$

The MATLAB obtained coefficients: 1, 0.2, 0.02, however 0.02 can not be implemented in transistor level and a coefficient 0.1 is found to be proper in transistor level simulation and selected for the 2nd post-cursor. Differential input pulses $x(n)$, having a 1-Volt swing centred on common mode voltage 1.3 V (0.8 - 1.8V) are applied for a period of 20 nanoseconds, which is long enough to be considered as step signal to the DFE. A symbol at an 8 Gb/s data rate has a 125ps period, so that the half-rate sampling clock's period will be 250 ps. If the circuit is designed to have a gain of 0.8, the first 3 amplitude values of $y(n)$ can be calculated from (4.6) as 1.8V, 1.64V and 1.56V.

The actual outputs of the FIR equalizer in both even and odd arm, as determined in a SPECTRE simulation, are shown in the sequence of plots in Figure 4.8.

The bottom trace in Figure 4.8 shows an input pulse arriving at the equalizer's input, 20ns time label is the start of a unit step. As was described in Chapter 3, the first recovered symbol comes from first odd symbol which is 1.8V as curve labelled B in Figure 4.8, the second recover symbol comes from the second symbol in even arm data which is 1.67V as labelled A in the graph, the 3rd symbolic signal comes from the 3rd symbol in the odd arm data which is 1.57V as mark B shows in graph.

These values are very close to the LMS obtained ones. Note here the optimized DFE circuit has a gain of $|Y(n)/X(n)|=0.8$.

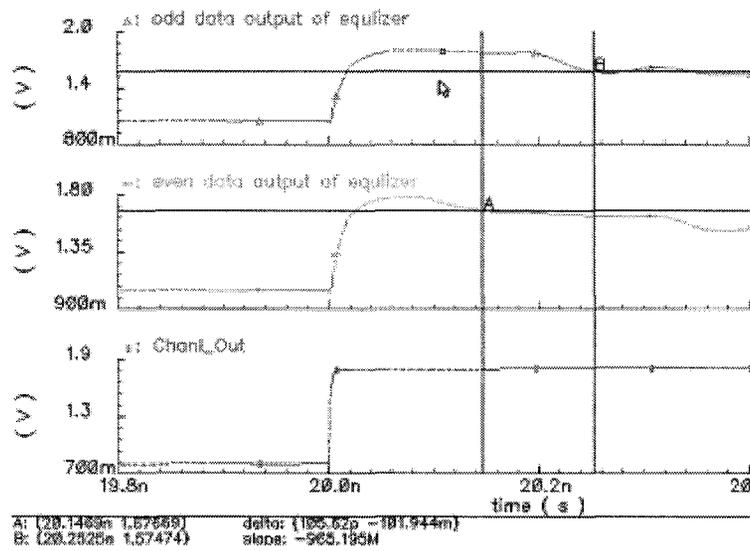


Figure 4.8: Step response of DFE at 8Gb/s

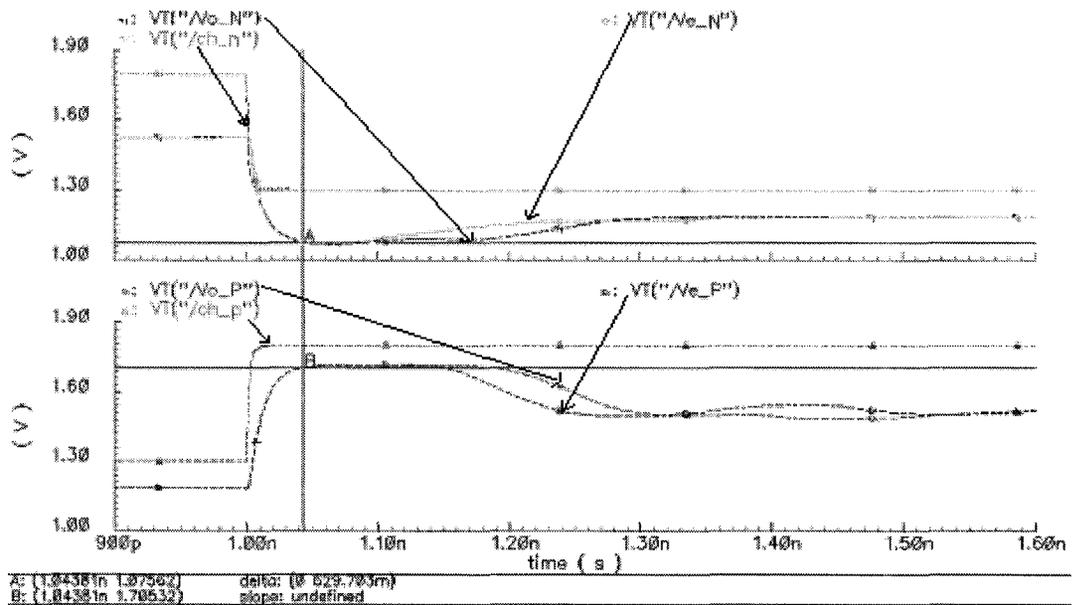


Figure 4.9: Delay time of HRDFE at 8Gb/s

TABLE 4.1: Comparison of step response voltages at 8Gb/s in LMS obtained and simulation

	Symbol 0	Symbol 1	Symbol 2
LMS obtained (V)	1.8	1.64	1.56
simulated (V)	1.8	1.67	1.57

Delay time: the waveforms in Figure 4.9 show the response of the equalizer to a step input. The rise and fall times are nearly equal, with a measured value of 43.81 ps and so half of it, 22 ps can be taken as the T_s of the 3-tap DFE. T_{CQ} is measure to be around 42 ps.

4.3 Pulse Response of Three-Tap HRDFE

Once proper response to a step input was verified, the next step was to perform analog tests involving operation at 8Gb/s. The input used in this case was the sequence $\{X(n)\} = [01100]$ with symbol period equal to 125ps.

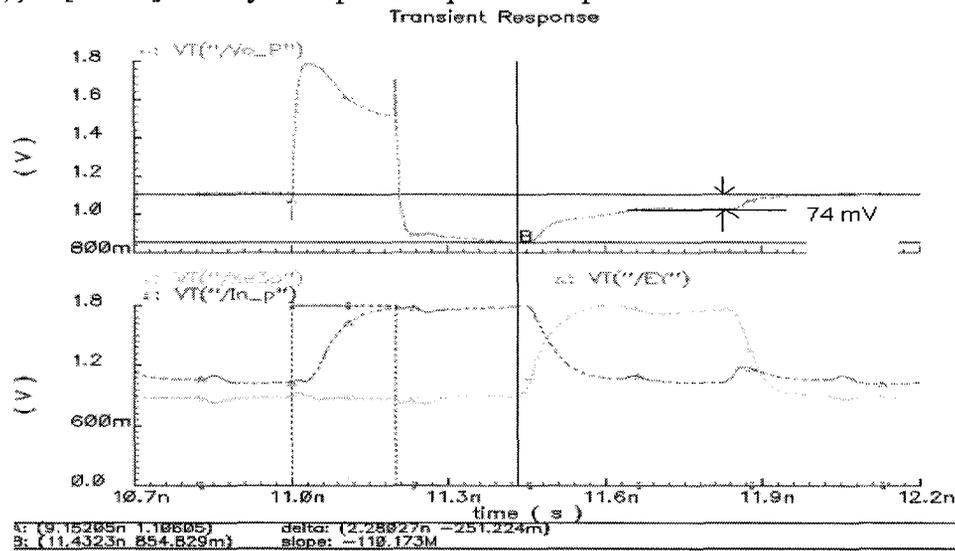


Figure 4.10: In_P vs Vo_P signal

The convolved output $Y(n)$ is once again given by (4.3). The odd and even output streams $\{Y(2n+1)\}$ and $\{Y(2n)\}$ are described by (3.2) and (3.3).

For the SPECTRE simulation, parameter values of $a=0.4$, $b=0.1$ and $V_{com}=1.1$ V, and $V_{swing} = 1.4$ V were used. And so for the positive input of the differential input pair, the weighted signal $\Delta V = a \cdot 0.7$ of the first post tap should be $0.4 \times 0.7 = 280$ mV and that of the second post tap should be $0.1 \times 0.7 = 70$ mV.

In the SPECTRE simulation, In_P is the input sequence $X(n)$ with a 125ps symbol period. The resulting output sequence in odd branch is labelled Vo_P in Figure 4.10.

The dotted line (V_{o_P} in the schematic) is as predicted logically by (3.3). The downward slope is the result of subtracting the feedback signal EY in the even arm. SPECTRE simulation results similar to those predicted.

For the first post-tap: $\Delta V = -251mV$, and the second post-tap: $\Delta V = -74mV$. Figure 4.10 also shows the delayed output sequence of the even branch of the HRDFE, and shows the expected 2 symbol input/output delay.

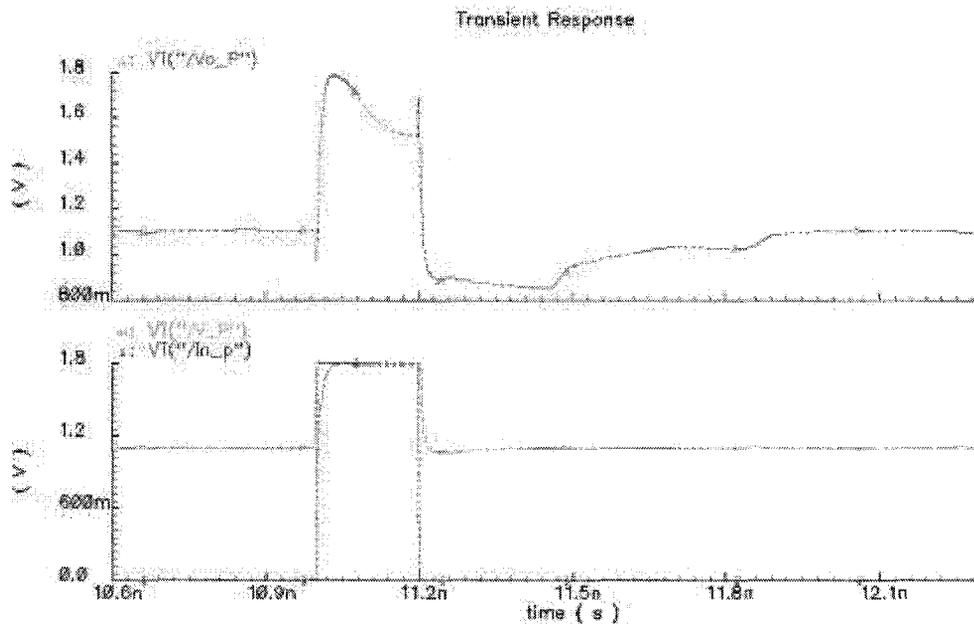


Figure 4.11: V_P VoP vs In_P signal

In Figure 4.11 V_P is the output of the DFE, the recovered output data. It is the result of reintegrating the even and odd arm output streams.

4.4 Transistor Level Pre-Layout Simulation Results

4.4.1 Two-Tap HRDFE Simulation Results

The reason that the three-tap HRDFE is the lowest-order of devices feasible for work at 10Gb/s can be ascertained when studying an analogous two-tap device, dia-

grammed in Figure 4.11. Its best performance when used with a 34-inch FR-4 channel will be examined.

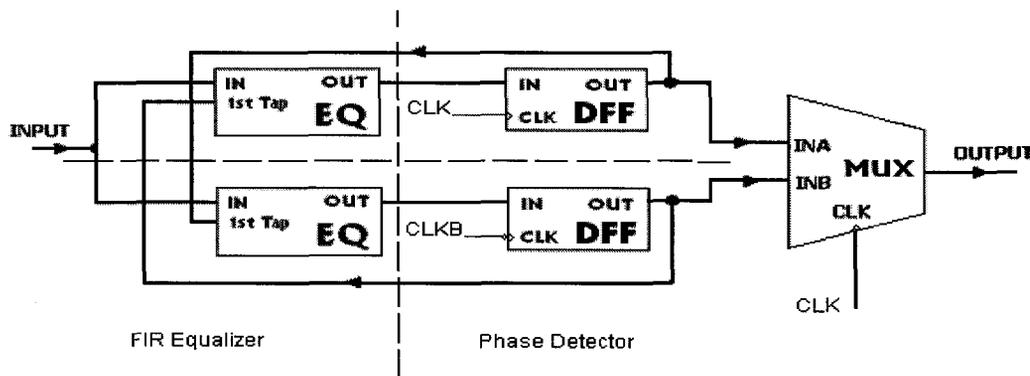


Figure 4.12: 2-tap HRDFE structure

The response to a step input indicates a rising/fall time ratio of 18.5ps, and so 9.8 ps is counted as the equalizer delay as before, please refer to Figure 4.12.

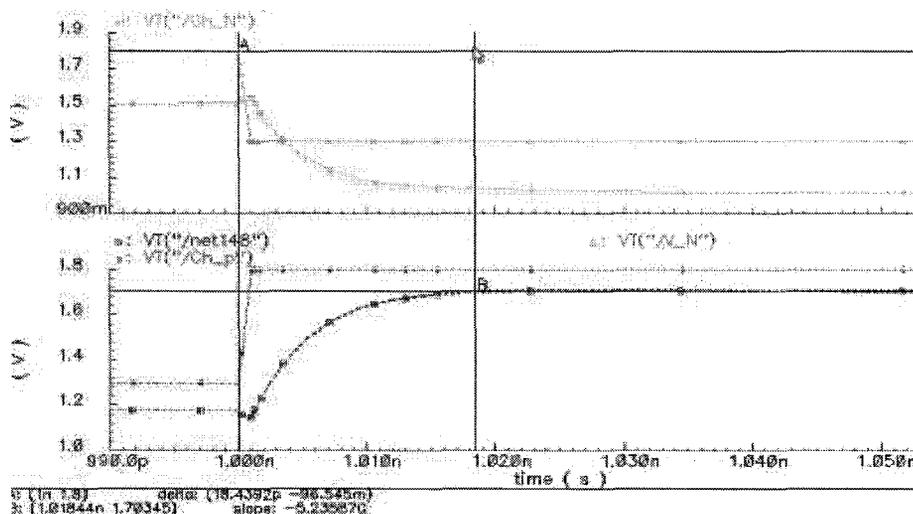


Figure 4.13: Step response of 2-tap HRDFE

At a data rate of 3.125Gb/s, the 2-tap DFE produces the correct $Y(n)$ sequence when a PRBS7 sequence is applied to its input. The outputs of the odd and even branches of the equalizer are well-defined, and there is no BER at the output. The simulation results are shown in the Figure 4.13 as a) the input data eye b) the DFE output data vs the near-end data c) even eye diagram of the DFE equalizer d) odd eye diagram of the DFE equalizer.

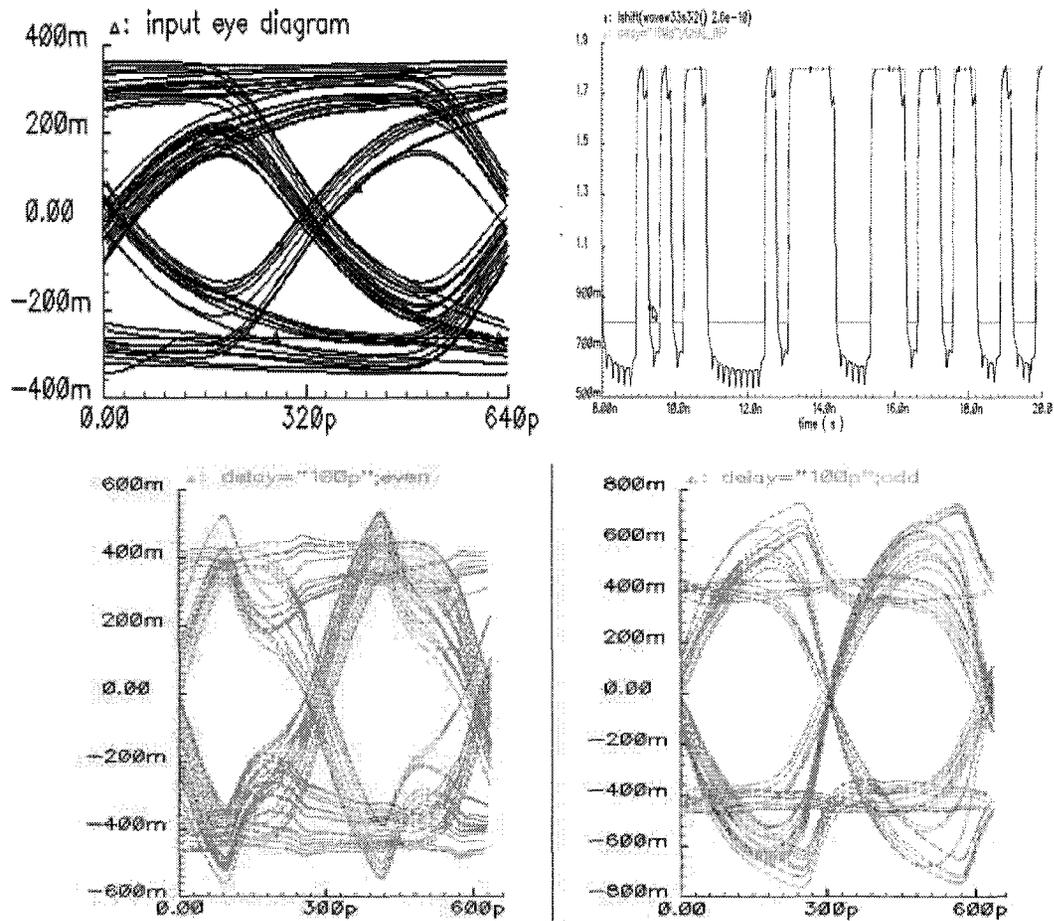


Figure 4.14: 2-tap HRDFE performance operating at 3.125Gb/s a) input eye b) near-end data vs output data c) even eye d) odd eye

But at data rate of 5Gb/s, even though the use of a 2-tap DFE enlarges the eye diagram at the equalizer's output, the input and output data streams do not match, please refer to Figure 4.14. The reason for this can be that the feedback decision was not made correctly, or that the decision made at the first post-tap was not sufficiently accurate for channel ISI cancellation.

From these results, it can be concluded that an optimized 2-tap pipelined half rate DFE performs reliably at rates up to 3.125Gb/s, but definitely fails at 5Gb/s. This is to be compared with the performance of Sohn's 2-tap pipelined full-rate DFE, whose operating maximum was only 1.35Gb/s [27].

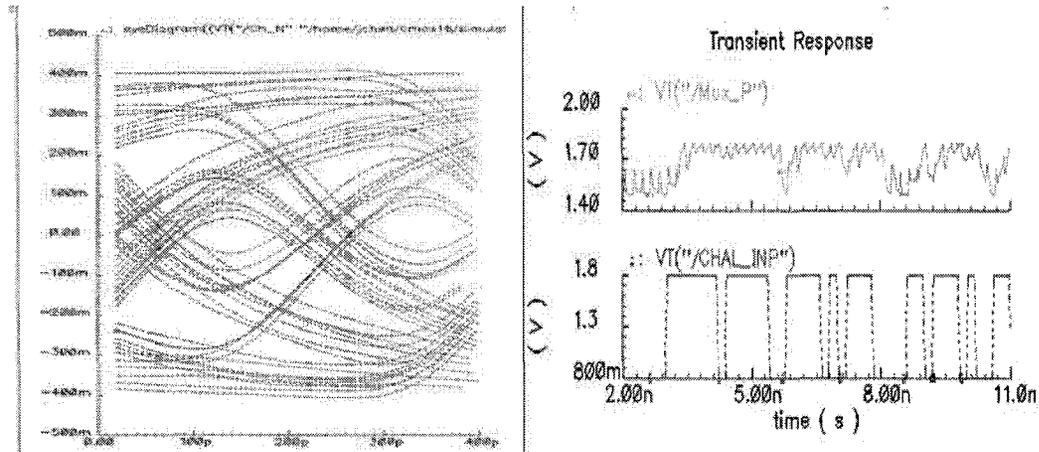


Figure 4.15: 2-tap HRDFE performance operating at 5Gb/s
a) input eye b) transmitted data and output data

4.4.2 Three-Tap HRDFE Pre-layout Simulation Results

A three-tap DFE circuit with FIR equalizer is designed in $0.18\mu\text{m}$ TSMC standard CMOS technology. A PRBS9 data is transmitted over a 34" FR-4 backplane channel. Eye diagrams at the transmit-end, the HRDFE input and at its output are plotted in Figures 4.15 and 4.16. Figure 4.15 shows the eye diagrams at data rate of 6.25Gb/s, while Figure 4.16 shows the eye diagrams at data rate of 8Gb/s.

As mentioned earlier, behavioral modeling speed can reach 10Gb/s (behavioral with time delays included), but this is not so in the case of hardware simulation. Some possible reasons for this are:

The critical path of the proposed structure is different from the pipelined structure as Sohn's paper shown. In Sohn's and TI's structure, which is a conventional pipelined one, if there are $n-1$ taps after the MUX recover the data, the critical path then could be

$$1) T_{CQ} + T_S, 2) T_{CQ} + T_{mux}, 3) T_{CQ}, \dots n) T_{CQ},$$

T_{CQ} is the DFF delay, T_S is the equalizer delay, as defined in Chapter 3. T_{mux} is the 2:1 MUX delay. 1), 2)...n) is the number of loops in the circuit. In this design work, the

MUX is placed to extend to the end of the parallel pipelined structure, and if there are $n-1$ taps, the critical path could be

$$1) T_{CQ} + T_S, 2) T_{CQ}, 3) T_{CQ}, \dots, n) T_{mux}.$$

Sohn's critical path obviously have a second critical path which is not what we like to see. In my design the critical path is different from the Sohn's and TI's which results in more delay time in the critical path, however there is no risk of the second critical path.

Also, the deviation of delay time of each analog cell in behavioral model from the SPECTRE model, the hardware simulation delay time takes longer than the ideal models and can not satisfy the operation limitation: the delay time must be less than half of the data symbol period.

The sampling clock in the hardware simulation monitors the real clock recovered from CDR and has rise/fall time as 25%-30% of the clock period, which results in the increasing of jitter of sampled data and decrease the eye opening in both vertical and horizontal directions. That can be another reason that the circuit can not operate at 10Gb/s as aimed.

A clear differential signal (near-end data) at rate of 6.25G/s transmit through 34-inch channel, its eye is shown as Figure 4.15(a). Total eye-closure, both horizontally and vertically for frequencies larger than 6.25Gb/s, can be seen in Figure 4.15(b) for the data arriving over the channel (far-end data). But one sees that upon being processed by the HRDFE, the eye openings at the even and odd arm outputs of the FIR equalizer being 94.11mV and 98.96 mV as shown in Figure 4.16 (c) and (d). The DFE recovered data eye diagram is shown in Figure 4.16(e) with measured jitter of 17.75ps and a horizontal eye-opening of 0.91 UI ('unit interval' unit), a vertical eye opening of 0.92V. Figure 4.16(f) shows a comparison of the recovered and near-end data at rate of 6.25Gb/s.

At a rate of 8Gb/s, the corresponding near-end data eye and far-end data eye are shown in Figures 4.17 (a) and (b). The eye openings at the even and odd arm outputs of

the FIR equalizer being 57.82mV and 58.37 mV as shown in Figure 4.17 (c) and (d). The DFE recovered data eye diagram is shown in Figure 4.17(e) with measured jitter of 22.4ps and a horizontal eye-opening of 0.86UI, a vertical eye opening of 0.87V. Figure 4.17(f) shows a comparison of the recovered and near-end data at rate of 8Gb/s.

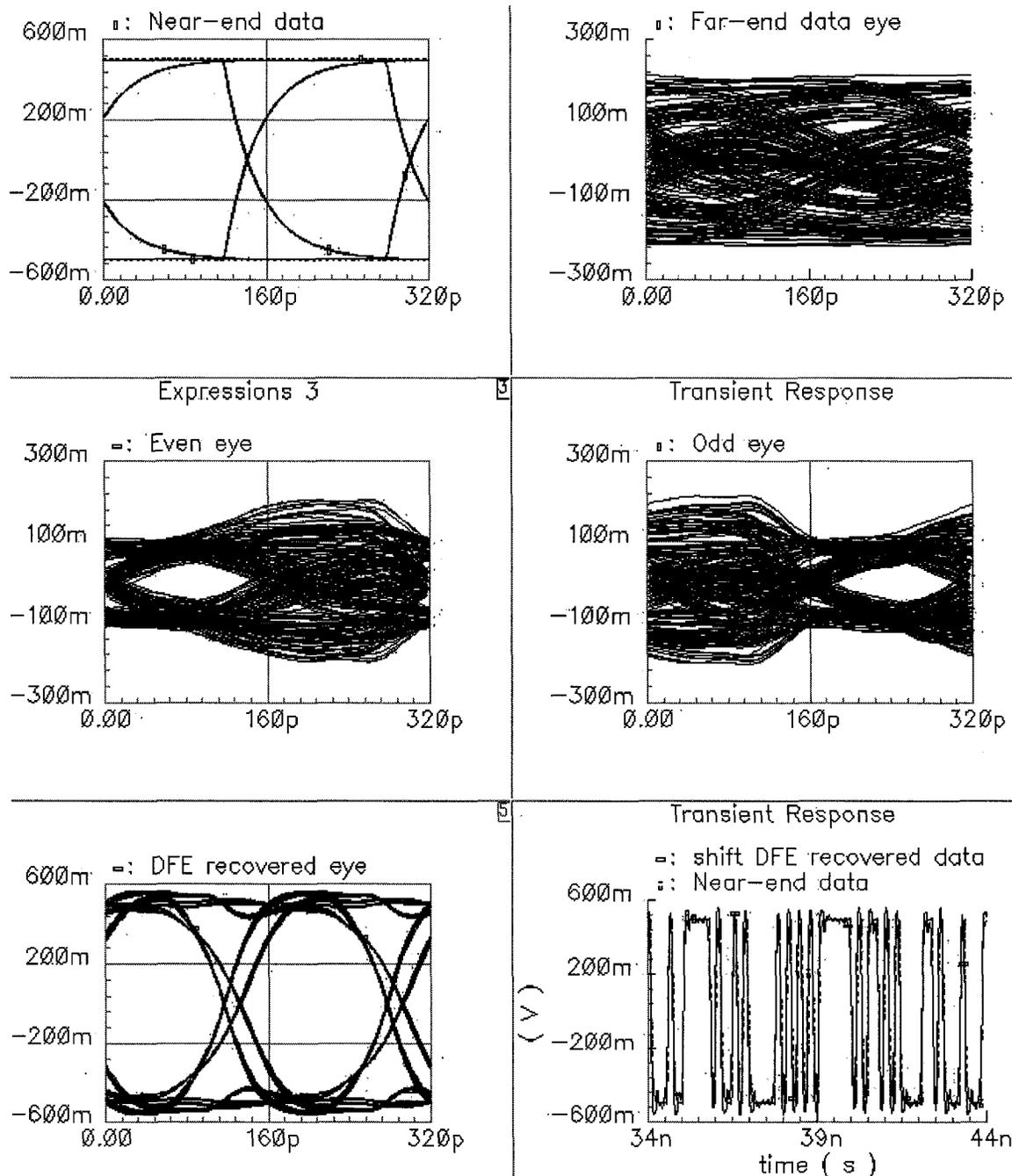


Figure 4.16: 3-tap HRDFE performance operating at 6.25Gb/s a) near-end eye b) far-end eye c) even eye d) odd eye of 3 tap DFE e) DFE recovered data eye f) near-end data vs recovered data

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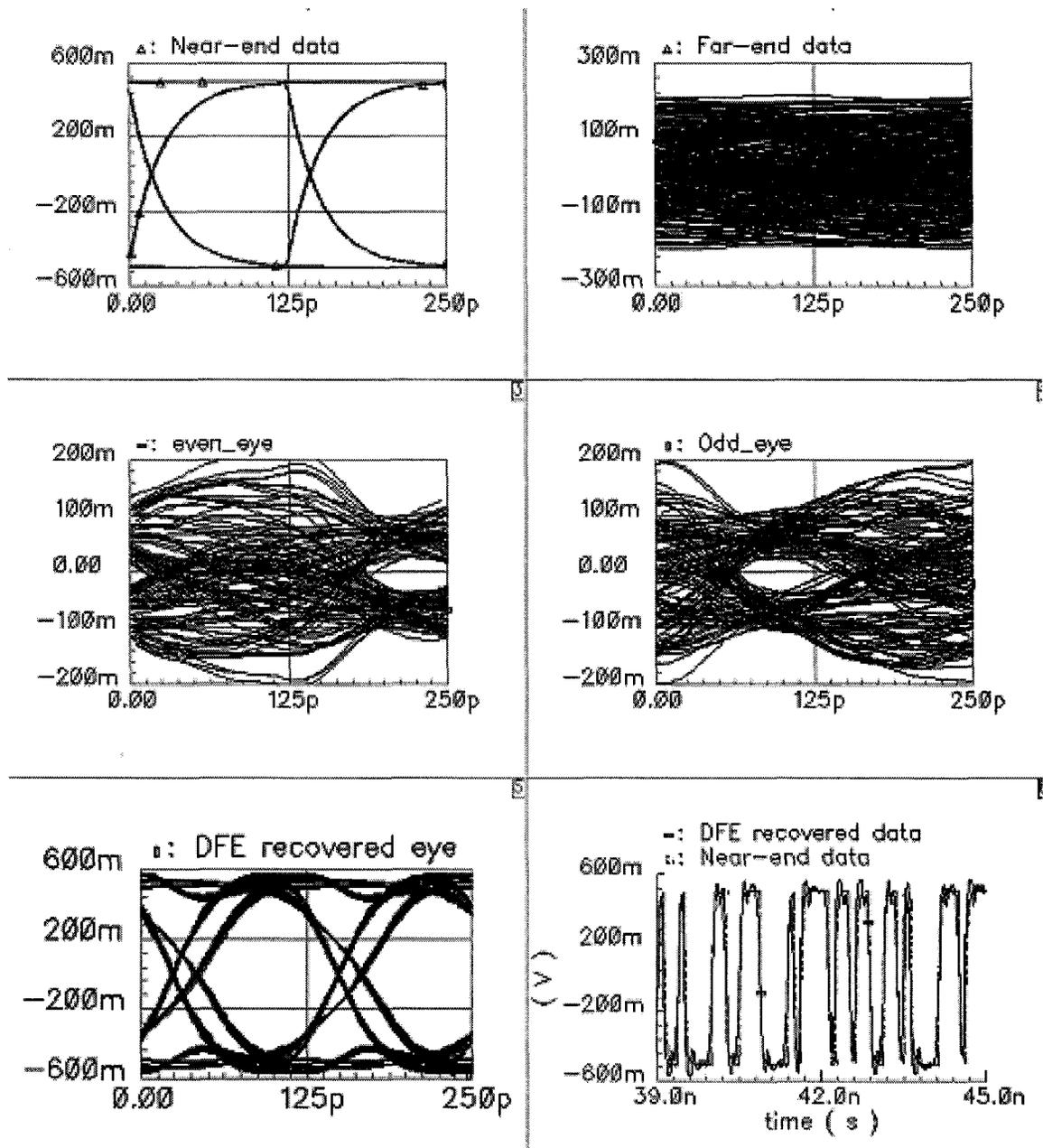


Figure 4.17: 3-tap HRDFE performance operating at 8Gb/s a) near-end eye b) far-end eye c) even eye d) odd eye of 3 tap DFE e) DFE recovered data eye f) near-end data vs recovered data

4.5 Three-Tap HRDFE Post-Layout Simulation Results

Parasitic effects are becoming increasingly important as process technologies move towards $0.18\mu\text{m}$, to the point that they can no longer be neglected in circuit design. The estimation of postlayout parasitics has become an essential step in delivering a successful design. The large number of parasitic resistances and capacitances occurring in typical postlayout netlists present a significant challenge to most circuit simulation tools [50], but the Cadence SPECTRE layout simulator was designed to accommodate this exigency, and so is chosen for work on this project at the present stage.

In addition, SPECTRE enable postlayout simulations in the presence of a huge amount of parasitic RC elements, including device parasitic capacitors and interconnect capacitors, which is very important at $0.18\mu\text{m}$. Such an RC estimating technique makes it possible to reduce the number of parasitic RCs in the post-layout modification of design and increase accuracy of simulation results.

The flow chart of basic post-layout simulation is shown in Figure 4.18 [47].

With layout implemented for each cell defined in section 4.1, and all cells including Buffers are extracted, and connected with metal trace, an integrated 3-tap DFE layout was implemented. Post-layout simulation shows 3-tap half-rate DFE works well at data rate up to 8Gb/s.

Post-layout simulation results for data rate of 6.25Gb/s are shown in Figure 4.19 and those for 8Gb/s in Figure 4.20. The horizontal eye opening of the recovered 6.25Gb/s data at the output of DFE is measured at 0.89 UI (Figure 4.19(c)), the vertical is 0.88V. The odd/even eye opening at the output of FIR equalizer is 57.29mV and 58.47mV in Figure 4.19 (a) and 4.19(b).

Similarly, the odd/even eye opening at the output of FIR equalizer is 37.30mV and 40.30mV in Figure 4.20 (a) and 4.20(b) for 8Gb/s, the horizontal eye opening of the

recovered 8Gb/s data at the output of DFE is measured at 0.73UI in Figure 4.20(c), and a vertical opening is 0.83V.

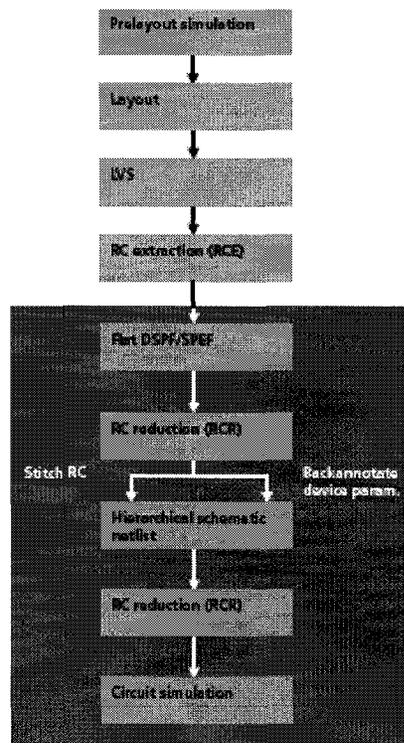


Figure 4.18: Postlayout simulation flow chart

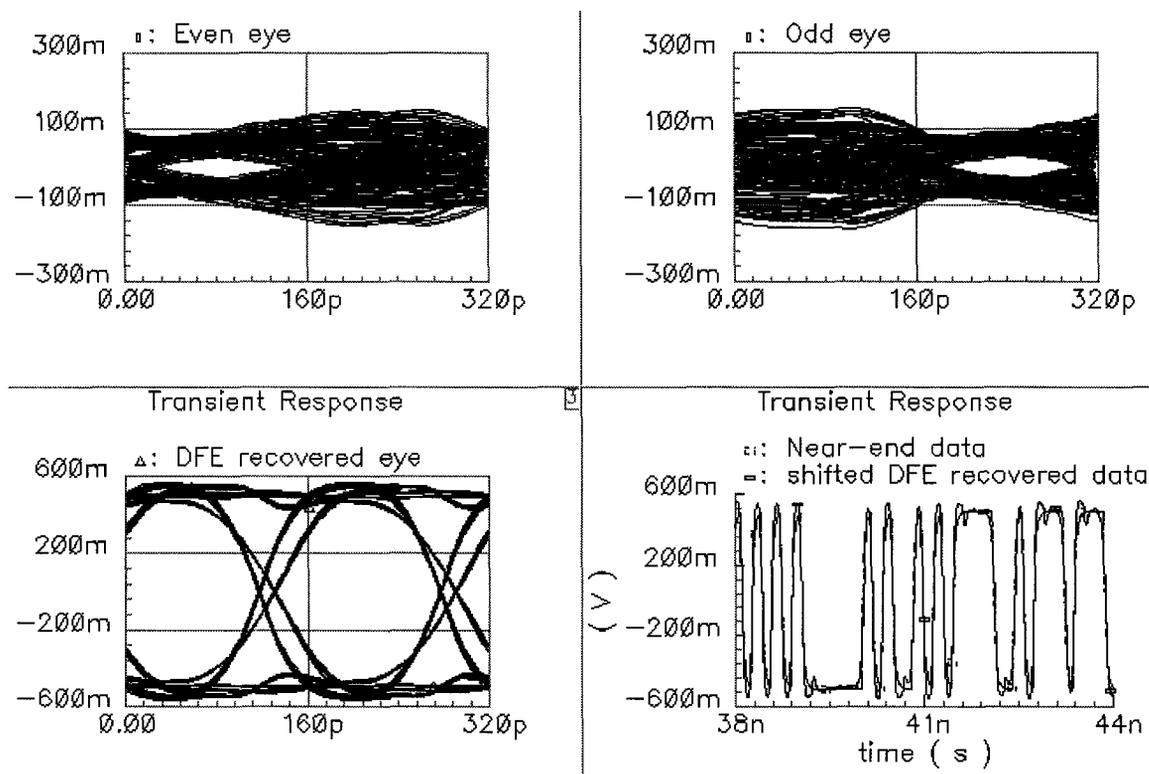


Figure 4.19: 3-tap HRDFE performance operating at 6.25Gb/s a) even eye b) odd eye c) DFE recovered eye d) near-end data vs recovered output data

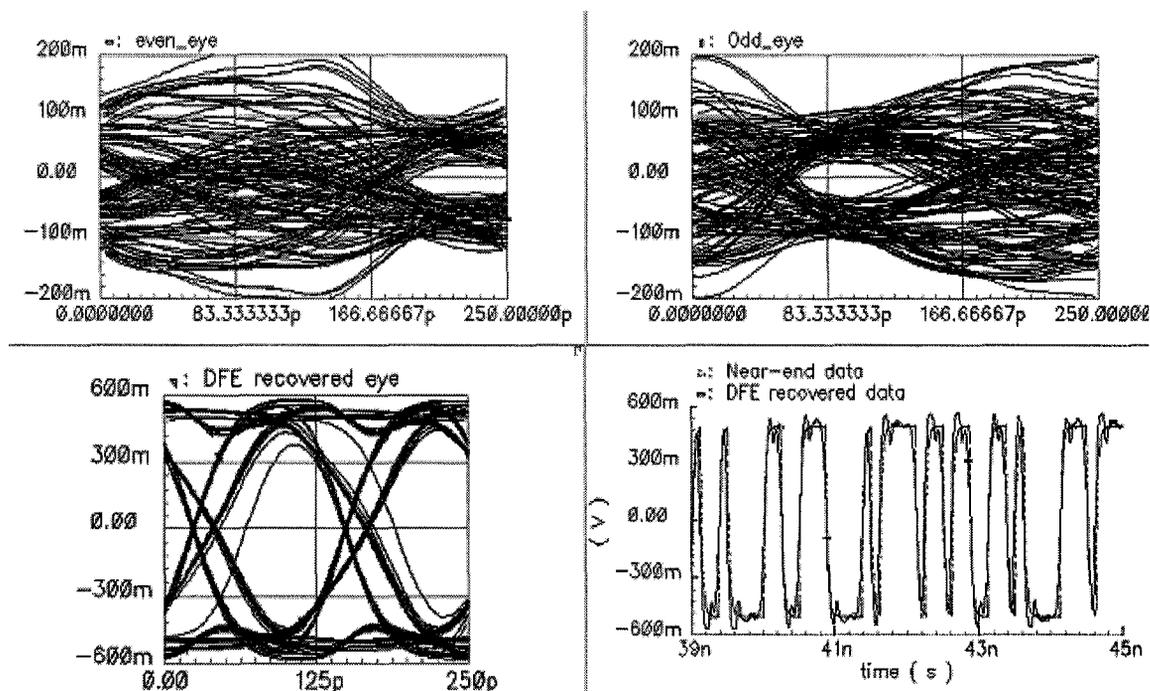


Figure 4.20: 3-tap HRDFE performance operating at 8Gb/s a) even eye b) odd eye c) DFE recovered eye d) near-end data vs recovered output data

4.6 BER Estimation and Design Conclusion

Superimposing the eye diagram of the PRBS9 data sequences gives the deterministic jitter at 8Gb/s, as shown in Figure 4.20(c). To approximately estimate the bit error rate(BER), the estimation (4.7) is given by [48],

$$BER(\tau, W, \sigma) = \frac{1}{4\sqrt{\pi}} \left[\begin{array}{l} \operatorname{erfc}\left(\frac{\tau - \frac{W}{2}}{\sqrt{2}\sigma}\right) + \operatorname{erfc}\left(\frac{\tau + \frac{W}{2}}{\sqrt{2}\sigma}\right) + \\ \operatorname{erfc}\left(\frac{\tau - \frac{W}{2} - 1}{\sqrt{2}\sigma}\right) + \operatorname{erfc}\left(\frac{\tau + \frac{W}{2} - 1}{\sqrt{2}\sigma}\right) \end{array} \right] \quad (4.7)$$

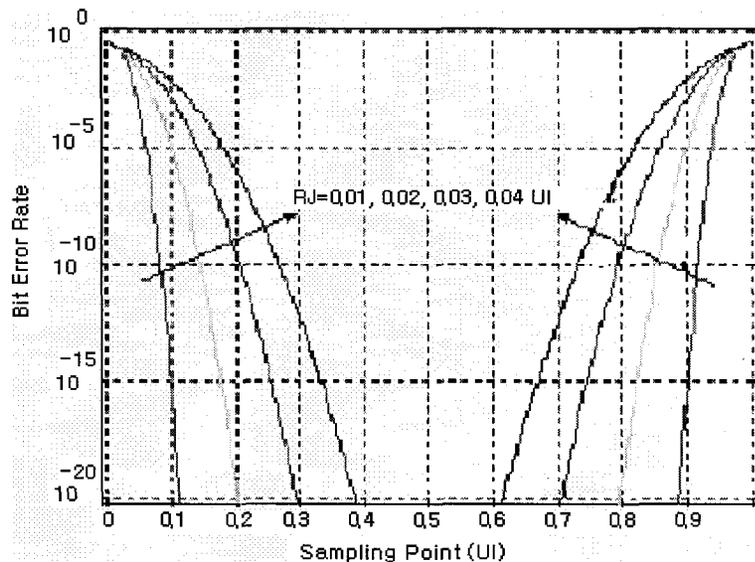


Figure 4.21: Bathtub Plot

Here is W deterministic jitter, σ is random jitter, and τ is the sampling point at receive side. All variables are in terms of unit intervals (UI). Here deterministic jitter are combined of ISI and duty cycle. A meaningful prediction of the BER is still possible though. The ‘bathtub’ plot which corresponds to (4.7) is drawn in Figure 4.21. The mea-

sured jitter value is used as deterministic jitter, and the random jitter is swept from 0 to 0.04UI with 0.01UI step size. Assuming the random jitter is 0.04UI, and taking proper sampling point from the SPECTRE simulation, an observed BER of less than 10^{-15} is noted. Table 4.2 provides a summary of the implemented DFE's characteristics.

TABLE 4.2: Summary of the implemented 3-tap half-rate DFE's characteristics

Parameter	Value
maximum operation speed	8Gb/s
delay time	~ 64 ps
1st post-tap coefficient	~ 0.2
2nd post-tap coefficient	~ 0.1
supply voltage	1.8 V
BER	$< 10^{-15}$
power consumption	12.2 mW

Conclusions and Continuation Suggestions

5.1 Significance of this Research

The problem of equalizing very high-speed data streams is convincingly solved by developing a means of processing high-rate data using half-rate technology. In particular, a pipelined 3-tap half-rate Decision Feedback Equalizer (HRDFE) has been successfully designed, optimized and simulated to the post-layout stage at 8Gb/s.

5.2 Summary and Conclusions

Important problems of backplane data transfer, ones mainly due to transmission line imperfections, have been identified and described in some detail. The problems that occur in high speed transmission systems and current ways of dealing with these, mainly equalization methods, have been reviewed.

The HRDFE idea was first tested using behavioral modeling, where the HRDFE was subdivided into functional blocks and then the interactions of these were simulated. The characteristics of each block were described with MATLAB functions and these were used as the time-dependent device parameters in an HRDFE simulation using SIMULINK. The behavioral modeling was done for data being transferred at rates of up to 10Gb/s over a thirty-four inch FR-4 channel. The results of this process indicated that the

proposed design would work, and also provided optimized values for the tap coefficients to be used in the HRDFE.

Once the general concept of the HRDFE had been shown feasible, a transistor-level simulation was done, wherein an analog CMOS $0.18\mu\text{m}$ technology was assumed. The performance of this three-tap HRDFE was then compared to that of the simpler and analog two-tap device. The pre-layout simulations indicated that a three-tap device was the simplest that could be expected to work at 10Gb/s. In fact, the two tap HRDFE simulation predicted an unacceptable BER at even 5Gb/s. Post-layout simulation of the three-tap HRDFE confirmed the pre-layout results. To a point – unfortunately, the critical path of the design restricted the maximum data rate to 8 Gb/s.

The overall result of this work was a Half-Rate Decision-Feedback Equalizer which works at 8Gb/s. This represents a doubling of equalizer bandwidth at the insignificant expense of doubling the amount of hardware and not at the considerable one of doubling the speed of the hardware. The new device supplies a simple and economical route to performance-enhanced backplane systems.

5.3 Future work

This document has described the successful design of an HRDFE only up to the post-layout simulation stage. All of the necessary preparation has been completed, and submission of the design to CMC for fabrication using standard TSMC CMOS $0.18\mu\text{m}$ technology can be done.

The next logical step is to add adaptability to the design. The present one uses fixed tap coefficients, optimized for one particular situation. The device's usefulness would be greatly improved if these coefficients could be computed internally, without needs for time-consuming and expensive environment specific customization would

greatly enhance the HRDFE's marketplace appeal. This step in the HRDFE's evolution could well involve the development of an efficient adaptation algorithm.

Another path is to design the DFE with feedforward filters which can have a faster convergence time.

Also, in order to achieve a higher speed at 10Gb/s in backplane data transmission, faster CMOS technologies such as 0.13 μ m or beyond will be an option.

Appendix A: LVS Reports

LVS Report for the 3X HRDFE circuit and test circuit

```
now running
"/CMC/tools/cadence.2004a/IC.5.0.33.USR2/tools.sun4v/dfII/local/.simrc"
finished running
"/CMC/tools/cadence.2004a/IC.5.0.33.USR2/tools.sun4v/dfII/local/.simrc"
```

Running simulation in directory: "/home/jchen/cmos18/LVS".

```
Begin netlist:   Mar 27 11:31:54 2005
  view name list   = ("auLvs" "extracted" "schematic")
  stop name list   = ("auLvs")
  library name     = "milidfe"
  cell name        = "HR_DFE_time_3X"
  view name        = "extracted"
  globals lib     = "basic"
Running Artist Flat Netlisting ...
End netlist:     Mar 27 11:31:56 2005
```

```
Moving original netlist to extNetlist
Removing parasitic components from netlist
  presistors removed: 0
  pcapacitors removed: 0
  pinductors removed: 0
  pdiodes removed: 0
  trans lines removed: 0
  196 nodes merged into 196 nodes
```

```
Begin netlist:   Mar 27 11:31:56 2005
  view name list   = ("auLvs" "schematic")
  stop name list   = ("auLvs")
  library name     = "milidfe"
  cell name        = "HR_DFE_time_3X"
  view name        = "schematic"
  globals lib     = "basic"
Running Artist Flat Netlisting ...
End netlist:     Mar 27 11:31:57 2005
```

```
Moving original netlist to extNetlist
Removing parasitic components from netlist
  presistors removed: 0
  pcapacitors removed: 0
  pinductors removed: 0
```

trans lines removed: 0
 447 nodes merged into 447 nodes

Running netlist comparison program: LVS
 Begin comparison: Mar 27 11:31:57 2005
 @(#) \$CDS: LVS version 5.0.0 04/30/2004 01:42 (cds12107) \$

108 net-list ambiguities were resolved by random selection.

The net-lists failed to match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	871	249
total	871	249

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	191	175
total	191	175

	terminals	
un-matched	0	0
matched but		
different type	0	0
total	13	1

End comparison: Mar 27 11:31:59 2005

Comparison program completed successfully.

CML 1X Buffer LVS report

now running
 "/CMC/tools/cadence.2004a/IC.5.0.33.USR2/tools.sun4v/dfII/local/.simrc"
 finished running
 "/CMC/tools/cadence.2004a/IC.5.0.33.USR2/tools.sun4v/dfII/local/.simrc"

Running simulation in directory: "/home/jchen/cmos18/LVS".

```
Begin netlist:    Mar 27 10:51:33 2005
  view name list  = ("auLvs" "extracted" "schematic")
  stop name list  = ("auLvs")
  library name    = "preem"
  cell name       = "CML_BUF_1X"
  view name       = "extracted"
  globals lib     = "basic"
Running Artist Flat Netlisting ...
End netlist:     Mar 27 10:51:33 2005
```

```
Moving original netlist to extNetlist
Removing parasitic components from netlist
  presistors removed: 0
  pcapacitors removed: 0
  pinductors removed: 0
  pdiodes removed: 0
  trans lines removed: 0
  12 nodes merged into 12 nodes
```

```
Begin netlist:    Mar 27 10:51:34 2005
  view name list  = ("auLvs" "schematic")
  stop name list  = ("auLvs")
  library name    = "preem"
  cell name       = "CML_BUF_1X"
  view name       = "schematic"
  globals lib     = "basic"
Running Artist Flat Netlisting ...
End netlist:     Mar 27 10:51:34 2005
```

```
Moving original netlist to extNetlist
Removing parasitic components from netlist
  presistors removed: 0
  pcapacitors removed: 0
  pinductors removed: 0
  pdiodes removed: 0
  trans lines removed: 0
  12 nodes merged into 12 nodes
```

```
Running netlist comparison program: LVS
Begin comparison:    Mar 27 10:51:34 2005
@(#)SCDS: LVS version 5.0.0 04/30/2004 01:42 (cds12107) $
Warning: Devices on a command "permuteDevice" that are not present in
netlist:
    "3Vnfet" "3Vnfet_na" "3Vpfet" "capacitor" "mimcap" "nfet_na"
    "pfet".
Warning: Devices on a command "pruneDevice" that are not present in
netlist:
    "3Vnfet" "3Vnfet_na" "3Vpfet" "nfet_na" "pfet".
Warning: Devices on a command "parameterMatchType" that are not present
in netlist:
    "3Vnfet" "3Vnfet_na" "3Vpfet" "capacitor" "mimcap" "nfet_na"
    "pfet".
```

2 net-list ambiguities were resolved by random selection.

The net-lists match.

layout	schematic	instances	
un-matched		0	0
rewired		0	0
size errors		0	0
pruned		0	0
active		16	9
total		16	9

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	12	12
total	12	12

	terminals	
un-matched	0	0
matched but different type	0	0
total	7	7

End comparison: Mar 27 10:51:36 2005

Comparison program completed successfully.

CML 2X Buffer LVS report

now running
"/CMC/tools/cadence.2004a/IC.5.0.33.USR2/tools.sun4v/dfII/local/.simrc"
finished running

Running simulation in directory: "/home/jchen/cmos18/LVS".

Begin netlist: Mar 27 10:55:05 2005
view name list = ("auLvs" "extracted" "schematic")
stop name list = ("auLvs")
library name = "preem"
cell name = "CML_BUF_2X"
view name = "extracted"
globals lib = "basic"
Running Artist Flat Netlisting ...
End netlist: Mar 27 10:55:06 2005

Moving original netlist to extNetlist
Removing parasitic components from netlist
presistors removed: 0

```

pcapacitors removed: 0
pinductors removed: 0
pdiodes removed: 0
trans lines removed: 0
12 nodes merged into 12 nodes

```

```

Begin netlist:      Mar 27 10:55:06 2005
view name list     = ("auLvs" "schematic")
stop name list     = ("auLvs")
library name       = "preem"
cell name          = "CML_BUF_2X"
view name          = "schematic"
globals lib       = "basic"
Running Artist Flat Netlisting ...
End netlist:       Mar 27 10:55:06 2005

```

```

Moving original netlist to extNetlist
Removing parasitic components from netlist
presistors removed: 0
pcapacitors removed: 0
pinductors removed: 0
pdiodes removed: 0
trans lines removed: 0
12 nodes merged into 12 nodes

```

```

Running netlist comparison program: LVS
Begin comparison:   Mar 27 10:55:06 2005
@(#) $CDS: LVS version 5.0.0 04/30/2004 01:42 (cds12107) $
Warning: Devices on a command "permuteDevice" that are not present in
netlist:
      "3Vnfet" "3Vnfet_na" "3Vpfet" "capacitor" "mimcap" "nfet_na"
      "pfet".
Warning: Devices on a command "pruneDevice" that are not present in
netlist:
      "3Vnfet" "3Vnfet_na" "3Vpfet" "nfet_na" "pfet".
Warning: Devices on a command "parameterMatchType" that are not present
in netlist:
      "3Vnfet" "3Vnfet_na" "3Vpfet" "capacitor" "mimcap" "nfet_na"
      "pfet".

```

2 net-list ambiguities were resolved by random selection.

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	28	9
total	28	9

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	12	12
total	12	12

	terminals	
un-matched	0	0
matched but different type	0	0
total	7	7

End comparison: Mar 27 10:55:08 2005

Comparison program completed successfully.

CML 16X Buffer LVS report

now running
"/CMC/tools/cadence.2004a/IC.5.0.33.USR2/tools.sun4v/dfII/local/.simrc"
finished running

Running simulation in directory: "/home/jchen/cmos18/LVS".

Begin netlist: Mar 27 11:01:06 2005
view name list = ("auLvs" "extracted" "schematic")
stop name list = ("auLvs")
library name = "preem"
cell name = "CML_BUF_16X"
view name = "extracted"
globals lib = "basic"
Running Artist Flat Netlisting ...
End netlist: Mar 27 11:01:07 2005

Moving original netlist to extNetlist
Removing parasitic components from netlist
presistors removed: 0
pcapacitors removed: 0
pinductors removed: 0
pdiodes removed: 0
trans lines removed: 0
8 nodes merged into 8 nodes

Begin netlist: Mar 27 11:01:07 2005
view name list = ("auLvs" "schematic")

Running Artist Flat Netlisting ...
 End netlist: Mar 27 11:01:07 2005

Moving original netlist to extNetlist
 Removing parasitic components from netlist
 presistors removed: 0
 pcapacitors removed: 0
 pinductors removed: 0
 pdiodes removed: 0
 trans lines removed: 0
 8 nodes merged into 8 nodes

Running netlist comparison program: LVS
 Begin comparison: Mar 27 11:01:07 2005
 @(#)SCDS: LVS version 5.0.0 04/30/2004 01:42 (cds12107) \$
 Warning: Devices on a command "permuteDevice" that are not present in netlist:
 "3Vnfet" "3Vnfet_na" "3Vpfet" "capacitor" "mimcap" "nfet_na" "pfet".
 Warning: Devices on a command "pruneDevice" that are not present in netlist:
 "3Vnfet" "3Vnfet_na" "3Vpfet" "nfet_na" "pfet".
 Warning: Devices on a command "parameterMatchType" that are not present in netlist:
 "3Vnfet" "3Vnfet_na" "3Vpfet" "capacitor" "mimcap" "nfet_na" "pfet".

2 net-list ambiguities were resolved by random selection.

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	146	5
total	146	5
	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	8	8
total	8	8
	terminals	
un-matched	0	0
matched but different type	0	0
total	7	7

End comparison: Mar 27 11:01:09 2005

Comparison program completed successfully.

CML 3-tap FIR equalizer LVS report

```
now running
"/CMC/tools/cadence.2004a/IC.5.0.33.USR2/tools.sun4v/dfII/local/.simrc"
finished running
```

Running simulation in directory: "/home/jchen/cmos18/LVS".

```
Begin netlist:   Mar 27 11:08:24 2005
  view name list   = ("auLvs" "extracted" "schematic")
  stop name list   = ("auLvs")
  library name     = "milidfe"
  cell name        = "HR_EQ_2TAP"
  view name        = "extracted"
  globals lib     = "basic"
Running Artist Flat Netlisting ...
End netlist:     Mar 27 11:08:24 2005
```

```
Moving original netlist to extNetlist
Removing parasitic components from netlist
  presistors removed: 0
  pcapacitors removed: 0
  pinductors removed: 0
  pdiodes removed: 0
  trans lines removed: 0
  13 nodes merged into 13 nodes
```

```
Begin netlist:   Mar 27 11:08:25 2005
  view name list   = ("auLvs" "schematic")
  stop name list   = ("auLvs")
  library name     = "milidfe"
  cell name        = "HR_EQ_2TAP"
  view name        = "schematic"
  globals lib     = "basic"
Running Artist Flat Netlisting ...
End netlist:     Mar 27 11:08:25 2005
```

```
Moving original netlist to extNetlist
Removing parasitic components from netlist
  presistors removed: 0
  pcapacitors removed: 0
  pinductors removed: 0
  pdiodes removed: 0
  trans lines removed: 0
  14 nodes merged into 14 nodes
  "3Vnfet" "3Vnfet_na" "3Vpfet" "nfet_na" "pfet".
Warning: Devices on a command "parameterMatchType" that are not present
in netlist
```

```
netlist:
    "3Vnfet" "3Vnfet_na" "3Vpfet" "capacitor" "mimcap" "nfet_na"
fet".
```

net-list ambiguities were resolved by random selection.

e net-lists failed to match.

	layout	schematic	
	instances		
un-matched	0	0	
rewired		0	0
size errors	0	0	
pruned		0	0
active		48	11
total	48	11	
	nets		
un-matched	1	2	
merged		0	0
pruned		0	0
active		13	14
total	13	14	
	terminals		
un-matched	1	1	
matched but			
different type		0	0
total	11	11	

d comparison: Mar 27 11:08:27 2005

mparison program completed successfully.

CML 3X MUX LVS report

```
now running
"/CMC/tools/cadence.2004a/IC.5.0.33.USR2/tools.sun4v/dfII/local/.simrc"
finished running
```

Running simulation in directory: "/home/jchen/cmos18/LVS".

```
Begin netlist: Mar 27 10:35:42 2005
view name list = ("auLvs" "extracted" "schematic")
stop name list = ("auLvs")
...
```

```

    library name      = "preem"
    cell name        = "MUX_3X"
    view name        = "extracted"
    globals lib      = "basic"
Running Artist Flat Netlisting ...
End netlist:      Mar 27 10:35:43 2005

```

```

Moving original netlist to extNetlist
Removing parasitic components from netlist
  presistors removed: 0
  pcapacitors removed: 0
  pinductors removed: 0
  pdiodes removed: 0
  trans lines removed: 0
  18 nodes merged into 18 nodes

```

```

Begin netlist:      Mar 27 10:35:43 2005
  view name list    = ("auLvs" "schematic")
  stop name list    = ("auLvs")
  library name      = "preem"
  cell name        = "MUX_3X"
  view name        = "schematic"
  globals lib      = "basic"
Running Artist Flat Netlisting ...
End netlist:      Mar 27 10:35:43 2005

```

```

Moving original netlist to extNetlist
Removing parasitic components from netlist
  presistors removed: 0
  pcapacitors removed: 0
  pinductors removed: 0
  pdiodes removed: 0
  trans lines removed: 0
  18 nodes merged into 18 nodes

```

```

Running netlist comparison program: LVS
Begin comparison:   Mar 27 10:35:43 2005
@(#)SCDS: LVS version 5.0.0 04/30/2004 01:42 (cds12107) $
Warning: Devices on a command "permuteDevice" that are not present in netlist:
       "3Vnfet" "3Vnfet_na" "3Vpfet" "capacitor" "mimcap" "nfet_na" "pfet".
Warning: Devices on a command "pruneDevice" that are not present in netlist:
       "3Vnfet" "3Vnfet_na" "3Vpfet" "nfet_na" "pfet".
Warning: Devices on a command "parameterMatchType" that are not present in
netlist:
       "3Vnfet" "3Vnfet_na" "3Vpfet" "capacitor" "mimcap" "nfet_na" "pfet".

```

3 net-list ambiguities were resolved by random selection.

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0

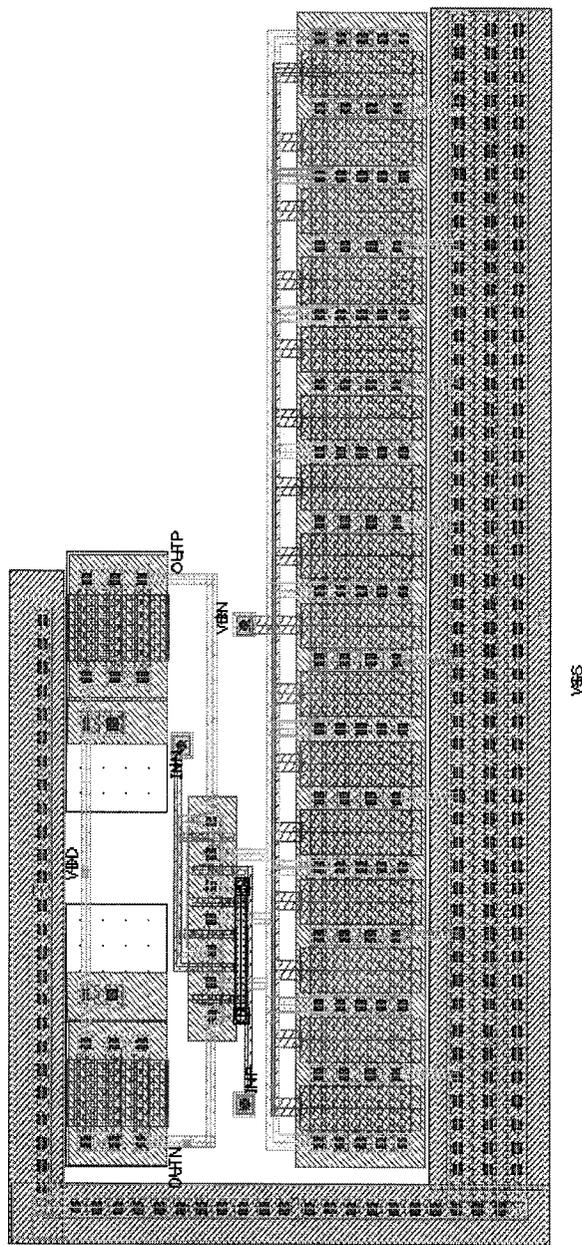
pruned	0	0
active	39	13
total	39	13

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	18	18
total	18	18

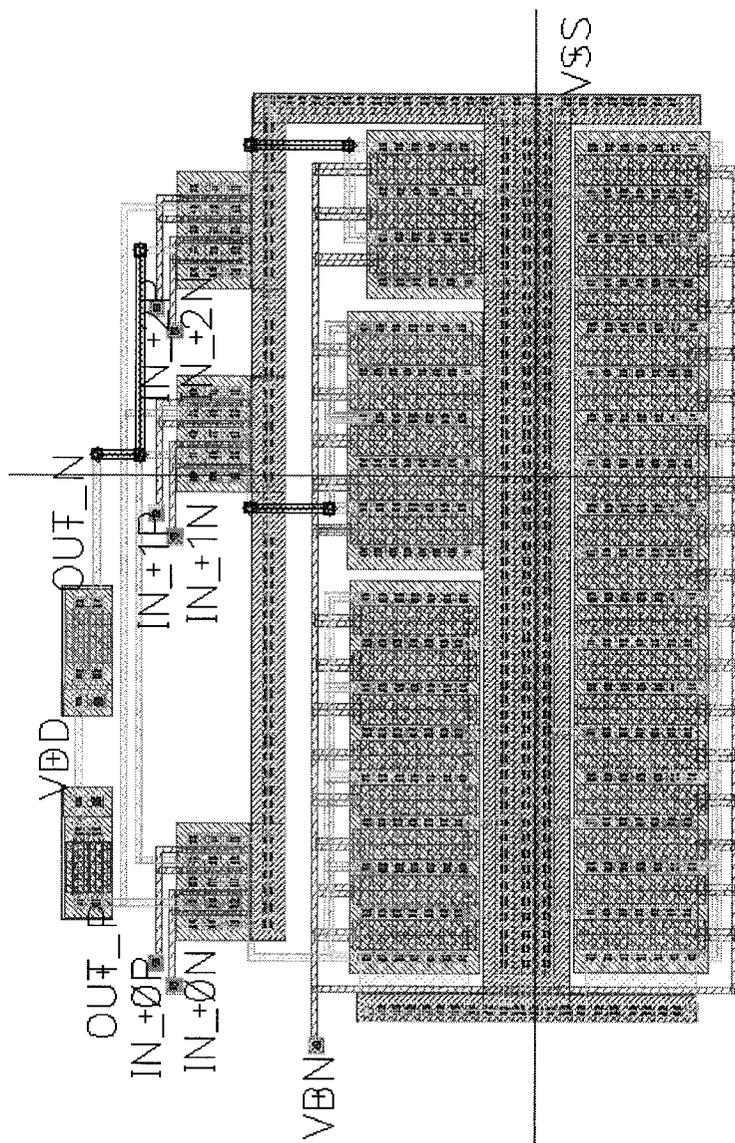
	terminals	
un-matched	0	0
matched but different type	0	0
total	0	11

End comparison: Mar 27 10:35:45 2005

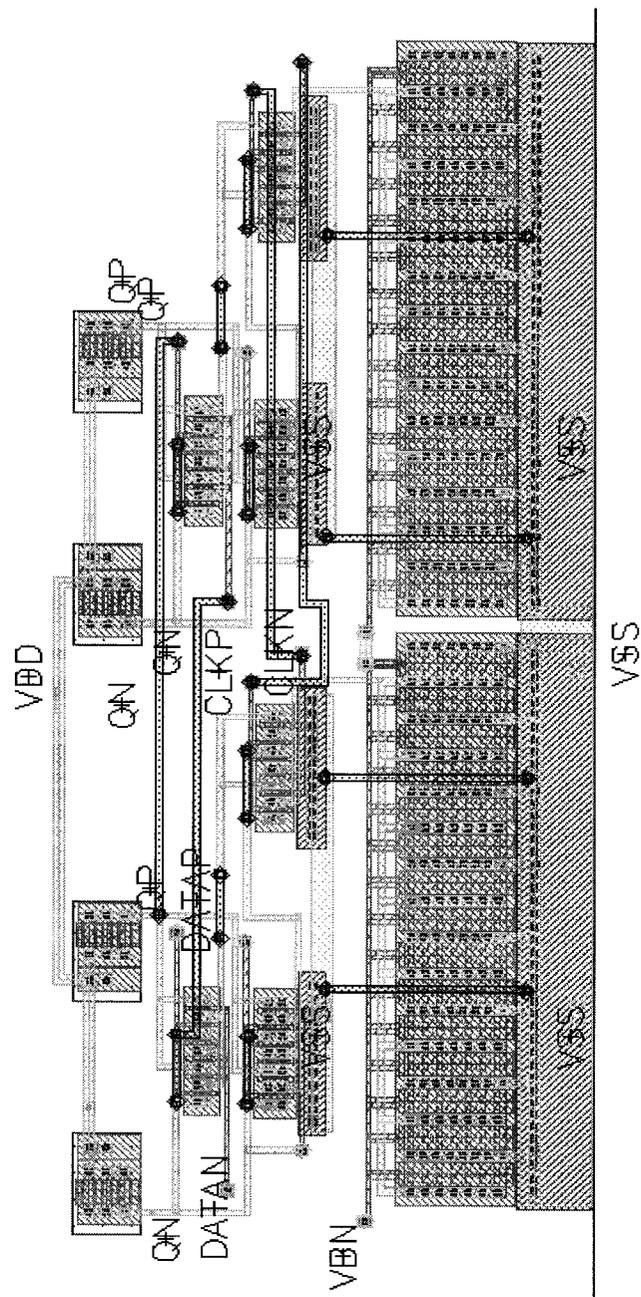
Comparison program completed successfully.



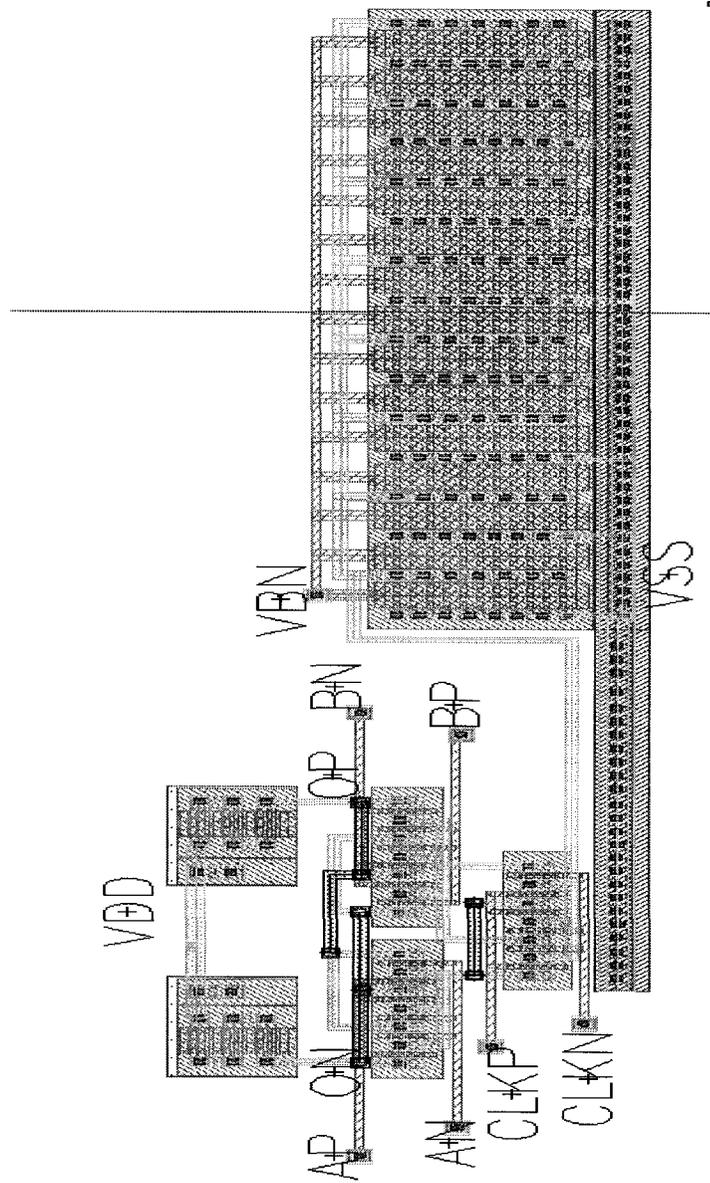
Appendix B.2: Layout of CML 2X Buffer



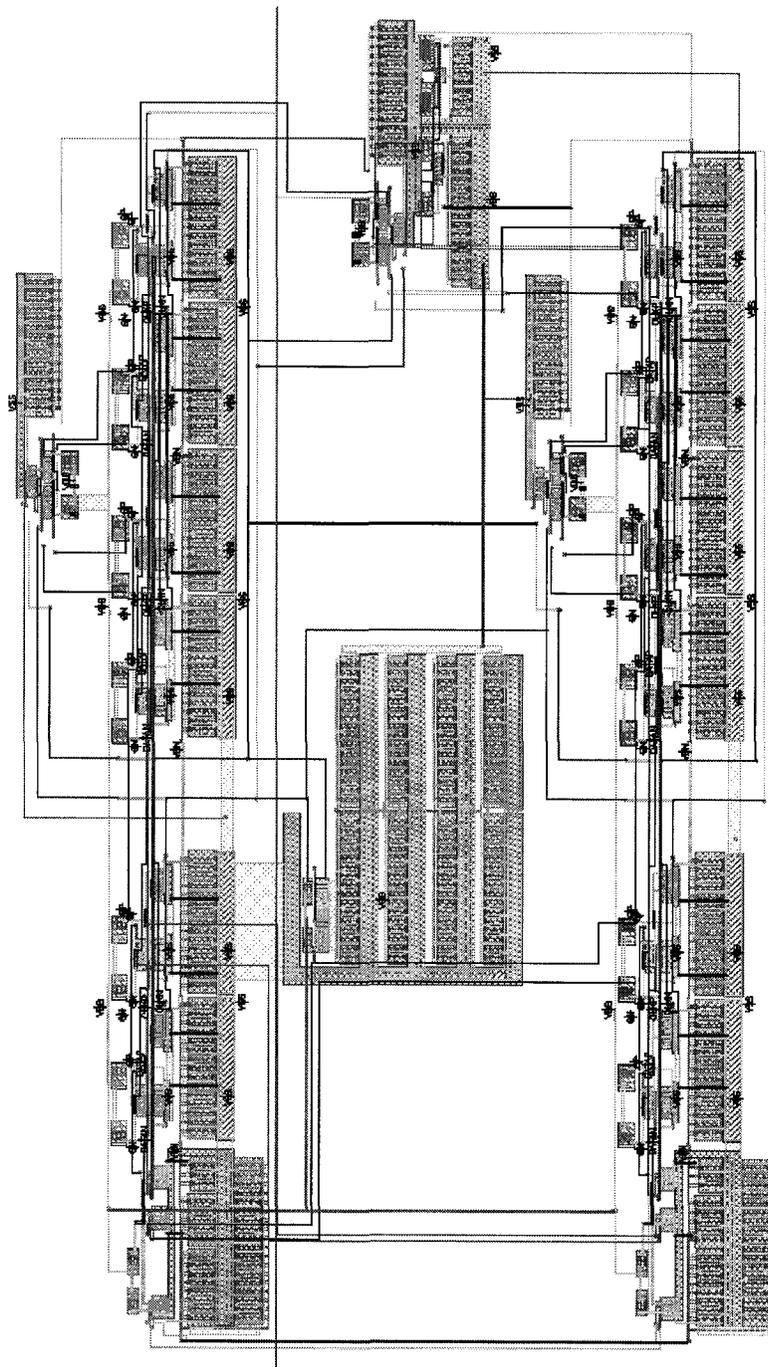
Appendix B.4: Layout of CML FIR equalizer



Appendix B.5: Layout of CML 3X DFF



Appendix B.6: Layout of CML 3X MUX



Appendix B.7: Layout of CML 3-tap HRDFE

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