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A Novel CMOS Integrated Alpha Particle Detector

by

Abdullah Ahmed

A thesis submitted to the Faculty of Graduate
Studies and Research in partial fulfillment
of the requirements for the degree of

Master of Engineering

Department of Electronics
Faculty of Engineering
Carleton University
Ottawa, Ontario, Canada

May 1996

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The undersigned recommend to the Faculty of Graduate Studies and Research
acceptance of the thesis

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in partial fulfillment of the requirements
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Thesis Supervisor

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Abstract

This thesis presents issues concerning design, layout and testing of an Integrated Alpha Particle Detector. The design was based on using a reverse-biased well to substrate p-n junction, in a conventional CMOS process, as a sense capacitor to provide a large collection area for the incident alpha particles. A CMOS inverter was implemented as an analog amplifier to detect the small potential change, induced by an alpha particle strike across the sense capacitor. Prior to fabrication, the design was simulated using a voltage source in series with the sense capacitor to model an alpha strike. An output voltage swing of approximately 2.5 V was obtained for the simulated alpha event. The design was laid out in CMOS4S, BATMOS and MITEL1.5 technologies. Tests were carried out on chips from BATMOS technology under vacuum conditions using a calibrated ^{241}Am source for alpha particles. Analysis of the measured results shows that the detector has good immunity to noise and high detection efficiency for alpha particles. The results validate the idea of detecting alpha particles using a CMOS integrated circuit.

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List of Symbols

BATMOS	Northern Telecom 0.8 μm BICMOS process
C	Capacitance
C_s	Sense Capacitor
CMC	Canadian Microelectronics Center
CMOS	Complementary Metal Oxide Semiconductor
CMOS4S	Northern Telecom 1.2 μm twin well process
C_{ox}	Oxide Capacitance of a MOS transistor; $C_{ox} = \epsilon_{ox}/t_{ox}$
Ci	Curies, a measure of radioactivity, 1Ci= 3×10^{10} disintegrations/sec
EPA	Environmental Protection Agency
MITEL 1.5	Mitel 1.5 μm CMOS process
NMOS	n-type metal oxide semiconductor (MOS)
PMOS	p-type metal oxide semiconductor
Qdep	immobile charge within the depletion region of a p-n junction
Qgen	charge generated within the sense capacitor due to an alpha strike
μ_n	electron mobility
μ_p	hole mobility
V_t	threshold voltage of a MOS transistor
ΔV_{in}	change in the voltage due to generated charge within the sense capacitor
$\Delta V_{in}'$	effective change at the input node of the inverter due to an alpha strike
ΔV_{out}	change in the output voltage due to generated charge
V_{DD}	5 V power supply
WL	Working Level; specifies alpha energy released by the decay of radon progeny.
SEDAN3	Stanford University program for 1-D device analysis of doping profiles

1

Introduction

1.1 Motivation and Objective

Recently there has been mounting interest in optimizing the measurement, detection and monitoring techniques of radon gas which is known to play a significant role in induction of lung cancer in humans [1] [5]. A recent study conducted by Henshaw [2] suggests that indoor radon may well contribute in induction of some other types of cancers as well. It is also reported by Henshaw that electromagnetic (EM) fields in the vicinity of power cables attract radon decay products by polarization of radon daughter aerosols [8], so that radon may be implicated in the increased rates of cancer some studies have associated with exposure to EM fields. The main objective of this thesis is to employ conventional CMOS VLSI technology to develop an efficient and yet simple and potentially inexpensive detector for alpha particles produced in the decay of radon gas and radon progeny. It is expected that such an alpha particle detector could be used to construct an inexpensive, direct-reading monitor for environmental radon.

The design of a sensitive and simple integrated circuit for radon detection is based on

the knowledge of interaction of the alpha particles, produced in radon decay, with silicon.

1.2 Radon: Sources, Health Hazards and Monitoring Techniques

1.2.1 Radon Generation and Decay

Radon is a naturally occurring colorless, odorless, almost chemically inert, and radioactive gas. Radon is produced in the radioactive decay of the naturally occurring radioactive elements, uranium and thorium. The three naturally occurring isotopes of uranium have atomic weights of 234, 235 and 238. ^{238}U is by far the most abundant uranium isotope, making up more than 99.2% of natural uranium [1]. ^{222}Rn with a half life of 3.82 days, is formed in the decay of ^{238}U . ^{235}U makes up approximately 0.7% of natural uranium. The decay of ^{235}U yields ^{219}Rn as an intermediate daughter product. ^{219}Rn is of little importance owing to its low abundance and very short half life [2]. ^{234}U makes up a very small fraction of natural uranium, approximately 0.0055% and therefore is not of importance. The only naturally occurring isotope of thorium is Thorium-232. ^{220}Rn is produced from the decay of ^{232}Th , with a half life of 55 seconds. ^{220}Rn is sometimes known as thoron.

Figures 1-1 and 1-2, taken from Wilkening [3], show the complete decay sequence of uranium and thorium with their progeny, their half lives and type and energy of radiation emitted during the decay.

Figure 1-1: Decay Sequence of Uranium-238

Figure 1-2: Decay Sequence of Thorium-232

1.2.2 Indoor Radon

Following production in the ground, both ^{220}Rn and ^{222}Rn move by diffusion. ^{222}Rn is able to move considerable distances during its lifetime whereas much of ^{220}Rn decays before reaching the earth's surface [3]. Consequently, the concentration of ^{220}Rn in air is lower than that of ^{222}Rn [3]. For this reason, ^{222}Rn is of primary concern in terms of being a potential health hazard.

As discussed earlier, radon is produced in rock and soil. Consequently radon may diffuse from the soil through the foundations and basements to enter buildings. A significant driving force for the entry of radon into houses is the pressure difference maintained within the building [4]. The use of indoor heating appliances, exhaust ventilation systems or dryers that exhaust air to the outside, all contribute in lowering the indoor pressure. This negative pressure within the house draws in air along with radon from the ground. Subsequently, indoor radon undergoes radioactive decay through the sequences shown in Figures 1-1 and 1-2.

1.2.3 Health Hazards

Radon and its progeny make a large contribution to the natural radiation dose received by the human respiratory tract due to the following factors: (1) the wide availability of the parent nuclides, ^{226}Ra and ^{224}Ra , in the rocks and soils and building materials, (2) the transport process available for radon as an inert gas, (3) the short life of the daughter products and (4) the subsequent energy released in each decay series.

During normal respiration, radon being an inert gas is likely to be exhaled before decaying [1]. However, radon daughters affixed to airborne dust particles are inhaled and accumulated in the lungs. These subsequently decay by alpha, beta and gamma emissions exposing the tissue to radiation and thereby increasing the risk for lung cancer. Figure 1-1 shows that the most energetic radioactive particles among the ones emitted during the decay series are the alpha particles. The damage induced is primarily due to these alphas which expend their energy in the sensitive surface tissue in the bronchial epithelium. The result is that radon progeny account for 55% of the average annual dose to the human lungs compared to nearly equal doses of about 15% each from other natural ionizing radiation, including cosmic rays terrestrial radiation and natural radionuclides [3]. The U.S. Environmental Protection Agency (EPA) estimates that between 5,000 and 20,000 lung cancer deaths annually are due to radon exposures [1]. It is also estimated by EPA that indoor radon poses a health risk in eight million U.S. homes [1].

1.2.4 Low Count Rate

The acceptable limit on radon concentration in the air, set as a guideline by EPA, is 4 pCi/l [4]. (The Curie[Ci] is a commonly-used unit of radioactive source activity [6]; 1Ci = 3.7×10^{10} disintegrations/second). At 4 pCi/l concentration of radon there are 8.9 decays per minute in one liter of air. Most of these decays will not reach a typical small-area detector due to the fact that alpha particles travel in the range of 3.5 to 5 cm in air [22]. A

rough calculation for the number of alpha particles that would reach a detector of 1cm^2 area, assuming a radon concentration of 4 pCi/l , shows that the detected number is of the order of one count per hour. This low counting rate presents a potential problem in detecting the alpha particles. To obtain accurate measurements it is necessary to count for extended time periods.

Radon monitoring systems either measure the concentration of radon or the concentration of radon progeny in the air. Determination of radon daughter concentrations require measurement of the sample with very little delay because of the short half-lives of the progeny. Determination of radon concentration is sometimes accomplished by measuring decays of radon progeny that grow in a radon sample and reach steady state concentration within 3-4 hours [1].

Therefore, to design a radon monitor, (1) an efficient means for collecting radon and/or the progeny is required, and (2) a sensitive detection scheme is needed to detect the radioactive decay of the radon or the progeny.

1.2.5 Present Monitoring Techniques

To develop methods for reducing health risk due to radon, it is necessary to determine the concentration of radon and/or radon progeny. There are various detectors which are employed in radon monitoring systems. Some of these detectors measure radon concentration while others measure the concentration of radon progeny. A majority of radon detectors, in radon monitoring systems, primarily detect alpha particles from the

decay of radon progeny [1]. In general radon detectors are classified under the following categories [1]:

Activated Charcoal Absorption, AC, and Charcoal Loaded Liquid Scintillators, CLS

Electret Ion Chambers, EIC

Alpha-Track Etch Detectors, ATD

Continuous Radon Monitors, CRM

Grab-Sample Radon Monitors, GRM

Continuous Working Level Monitors, CWLM

Grab-Sample Working Level Monitors, GWLM

AC, CLS, EIC and ATD are grouped as passive detectors systems using no power source. Radon enters and leaves the detectors by diffusion, and an additional reader system is involved to convert the data collected by these passive detectors into radon concentration or working level units. The Working Level, WL, unit was originally developed to compute radon progeny exposure to miners. It describes the total available alpha energy released in the decay of radon progeny. $1\text{WL} = 1.3 \times 10^5$ Mev of alpha energy in one liter of air [5]. This numerical value is derived from the alpha energy released by the total decay of short-lived radon progeny in radioactive equilibrium with 100 pCi of ^{222}Rn per liter of air [5]. The passive detectors primarily measure ^{222}Rn concentration directly and express the results in picocuries per liter of air.

The remaining detectors are called active detectors, since an air pump is employed to

pump radon containing air into or through the detector [1]. These detectors monitor the concentration of radon progeny in the air. The results are expressed in units of working levels, WL.

Detectors like AC and CLS require expensive equipment such as gamma ray spectroscopy or liquid scintillators to analyze and interpret the collected data. This equipment ranges in price from \$5000 to \$15,000 [1].

Alpha track detectors contain an alpha particle sensitive plastic film that only responds to alphas having energies close to 4 Mev. These alphas damage the film such that in a subsequent chemical etching step the alpha tracks are visible under a microscope. The number of alpha tracks per unit area is counted by an automated optical reader. ATDs are employed in continuous measurement of long term average radon concentration. These detectors are not suitable for short duration screening measurements and are clearly not direct-reading.

CRMs are employed for indoor radon monitoring. These are very sophisticated and expensive systems, costing from \$2,400 to \$10,000 [1]. Trained technicians are required for performing indoor radon measurements using CRM systems. An example of a continuous radon monitor is the Honeywell Digital Radon Monitor Systems. These systems employ silicon photodiodes using off-the-shelf components for amplification of a small voltage change produced by the alpha particles within the diode.

GRMs provide a near instantaneous measurement of the radon concentration. Due to the inherent variability of indoor radon levels, EPA does not recommend their use for

screening or follow-up measurements of radon. These are suitable for pre-screening measurements to assist in deciding the optimum location for screening instruments [1].

In CWLM systems, air is pumped at a steady rate through a filter paper. The filter is continuously monitored by an alpha detector. The detector may be an alpha scintillator which is viewed by a photomultiplier tube. It may also contain a silicon detector such as diffused-junction or surface barrier alpha detector. These detectors are responsive only to the alpha radiation. An example of a lightweight CWLM is one produced by Thomson & Nielson Electronics, Ltd. of Kanata, Canada which employs a silicon solid state detector and gives a visual readout in alpha counts.

An attempt was also made to develop a reliable low cost radon monitor based on spark discharge technology as reported by Vandish [7].

1.3 Summary

This chapter presented an overview on sources and properties of radon. The health hazards associated with radon were discussed. The present monitoring techniques for indoor radon were also briefly discussed.

An efficient monitoring technique for indoor radon has to be developed as an initial step to implement methods for reducing the risks associated with indoor radon.

The next chapters will present a design methodology for an *integrated alpha particle detector* which is intended to detect alpha particles produced by the decay of radon or radon progeny.

2

Alpha Particle Interaction with Silicon

2.1 Introduction

Research interest has grown in the area of alpha particles and their effects in integrated circuits due to the presence of uranium and thorium in minute proportions within the materials used to make IC packages [9][10]. In the radioactive decay of these impurities alpha particles are emitted, which are known to produce soft errors in integrated semiconductor memory chips [10] [11] [12].

In this chapter the fundamental concepts of alpha particle properties and interaction with silicon are reviewed. This discussion will provide the required background knowledge to deal with the subtleties involved in modeling the effects of alpha particle penetration in a biased silicon based p-n junction for designing a detector circuit. The inherent constraints on the design aspects that are a direct result of the internal interaction of alpha particles with silicon are also presented.

2.2 Alpha Particles

2.2.1 General Properties

Alpha particles consist of two protons and two neutrons (a helium nucleus) and hence are doubly charged. Alpha particles produced in the decay of naturally occurring radioactive isotopes have energies in the range 4-5 Mev [9]. The mass of an alpha particle is thousands of times heavier than that of an electron [6]. It loses energy at a rate of approximately 150 keV/ μm [12] in silicon.

2.3 Interaction with Matter

Alphas interact strongly with matter mainly because of their charge and high energy. When an alpha particle strikes silicon, it loses energy along its straight path [13]. The length of travel is known to be a function of the particle's energy [13]: typically 20-25 μm [9] for a 4-6 Mev alpha particle. Figure 2-1 below, shows the range of alpha particles in silicon.

Figure 2-1: Range of alpha particles in silicon. Taken from May and Woods [12]

The arrow in Figure 2-1 indicates the range of energies for the naturally occurring alpha particles.

Initially, the energy lost by an alpha particle is expended in creating high energy electron-hole pairs [13]. These highly energetic electron-hole pairs then decay into a cascade of carriers. Finally, this complex process results in one electron-hole pair generated for every 3.6 eV of energy lost by the alpha particle [13]. Therefore, a typical 4-5 MeV alpha particle emitted in the decay series of ^{238}U , will generate approximately 1×10^6 electrons. This process occurs within a time of the order of picoseconds, in a radius of about $0.1 \mu\text{m}$. The generated electron-hole pairs form a cylindrical plasma column with a net neutral charge [13] [14].

2.4 Funneling Phenomenon

The process of *funneling* can be explained by understanding how the column of generated carriers, under the influence of an electric field such as the depletion region of a p-n junction, disturbs the depletion layer. Due to the fact that the column of generated carriers is charge neutral and acts as a conductor that will not support any large potential difference between its two ends, it causes the potential difference that initially appeared across the junction to spread itself into the previously quasi-neutral region of the substrate. As the track forms, the initial depletion region in the immediate vicinity of the column becomes neutralized. As a result, the electric field is pushed down into the substrate along the alpha track. This extension along the alpha track into the initially field free region of the substrate is called *funneling*, and occurs within a few picoseconds of the alpha strike [13]

[14]. Figures 2-2 and 2-3, taken from Dunsmore [21], below show the extension of the equipotential lines in a biased p-n junction.

Figure 2-2: Distribution of electron hole pairs after an alpha hit

Figure 2-3: Elongation of Equipotential lines Due to Funneling

Inside the depletion region, the carriers drift in opposite directions under the influence of the electric field there [14]. This results in a pile up of positive charge on one edge of the depletion region and of negative charge at the opposite edge of the depletion region. The resulting field opposes the field in the depletion region and causes the carriers to be collected by drift rather than slowly by diffusion [13]. As steady state is approached, the electrons and hole start compensating some of the ionized donors and acceptors inside the depletion region, effectively reducing the depletion width and causing the potential between the n and p regions to drop [15]. *This phenomenon of reduction in the initial potential difference across a diode due to an alpha strike will form the basis for detecting the alpha particles.* An important assumption made is that the charge collected from the α -particle track greatly exceeds that contained in the section of the track that spans the depletion region [14]. The validity of this assumption can be justified by comparing the depletion charge (Q_{dep}) within the area spanned by the alpha track to the generated charge (Q_{gen}) within the $0.1\ \mu\text{m}$ radius column.

The drift dominated charge collection in a p-n junction was reported by Hsieh in 1981 [10]. Figure 2-4 below, taken from Hsieh, shows a comparison between the total charge collected, with drift component and the calculated equivalent charge within the original depletion layer if the field had not been distorted after the alpha strike.

Figure 2-4: The charge collected as a function of alpha-particle energy for a substrate with a resistivity of 2 ohm-cm at a bias voltage of 7.5 volts. Total charge collected is shown by solid line, the drift component by dashed line. The dash-dot lines show the calculated equivalent charge generated within the depletion layer if the field had not distorted.

It can therefore be concluded from the results shown in Figure 2-4 that a node which is struck by an alpha particle collects most of the charge due to the drift dominated funneling effect.

2.4.1 Delay in the Onset of Funneling Phenomenon

It is of prime importance to know what will happen if the alpha particle misses the depletion region. Hsieh and Murley [13] performed simulations which prove that charge will still be collected by funneling but with some finite time delay. This delay occurs due to the fact that generated carriers will initially spread by diffusion until the charge cloud reaches the junction depletion region. At this instant, the built-in field is disturbed, as described previously, and the funneling process begins, assuming the carrier density is

sufficiently high. Figure 2-5, taken from Hsieh [13], shows the amount of charge collected when the alpha particle misses the depletion region at the strike.

Figure 2-5: The charge collected versus time when an alpha particle misses the depletion region. The simulation was performed by placing e-h pairs (a) 1 μm below (b) 2 μm below the depletion region. For comparison the charge collected when the particle strikes the region is also shown.

It can be seen from the above figure that if an alpha particle strikes a region close to but not exactly in the depletion region, detection is still possible because the charge collected is not solely due to diffusion but also due to funneling with an added delay.

2.5 Dependency on Substrate Type and Doping

Hsieh has reported that most of the charge is collected during the time the electric field relaxes after the funneling. This time is a function of mobility of the collected minority carriers and the substrate impurity concentration [13]. It was also reported by Hsieh that a

junction with n-type substrate collected two thirds of the charge that was collected by a junction with p-type substrate for the same doping. This results from the fact that the mobility of minority electrons in p-type substrate is higher than the mobility of minority holes in n-type substrate, allowing more efficient collection within the time the field relaxes [15].

Thus, using junctions with a p-type substrate will be more favorable for charge collection, giving higher probability of alpha particle detection.

2.6 Collection Area Dependency

Large sensing area is preferred as larger number of alphas will reach the detector area, maximizing the collection efficiency. If the depletion capacitance of a p-n junction is used as a sense capacitor, there exists an upper limit for the size due to the fact that the generated charge must not be negligible compared to the charge already stored in the depletion region. This point is further discussed in the next chapter.

Thus, if a diode is precharged to a known potential and one of its node is left floating, then a subsequent alpha particle strike is expected to lower the potential across the diode by a finite amount. This reduction in the potential across the diode is calculated in the following section.

2.7 Voltage Drop Due to an Alpha Event

As indicated in section 2.2.1, a typical alpha particle emitted during the decay sequence

of radon has an energy of 4-5 Mev which when absorbed in silicon, generates 1×10^6 e-h pairs. If alpha particles are incident on a diode, whose depletion capacitance is used as a sense capacitor, the generated electrons and holes after undergoing the complex process of funneling, will reduce the initial bias across the diode by a known amount. The reduction of the bias is a direct result of compensation of the ionized donors and acceptors within the depletion region. The amount of charge, assuming an average of 1×10^6 e-h pairs are generated, can be calculated as:

Total charge generated (Q_{gen}):

$$Q_{gen} = 1 \times 10^6 \text{ electrons} \cdot (1.6 \times 10^{-19} \text{ Coulombs/electron})$$

$$Q_{gen} = 160 \text{ fC.}$$

The change in potential is:

$$\Delta V \text{ in volts} = \Delta Q \text{ in Coulombs} / \text{Capacitance in farads.}$$

$$\Delta V = (160 \times 10^{-15} \text{ C/F}) \cdot (1 \text{ Farad} / 1 \times 10^{-12} \text{ pF})$$

$$\Delta V = 0.16/C \text{ ----- } C \text{ is capacitance in pF}$$

This result suggests that a well to substrate depletion capacitance, in a conventional CMOS process, can be used, due to larger capacitance per unit area, to maximize ΔV .

2.8 Summary and Conclusion

The study of the complex electrostatic interaction of alpha particles with silicon shows

that the following factors have to be taken into consideration in designing a detection scheme for alpha particles.

First, due to the fact that the minority electrons have higher mobility than the minority holes, it is suggested that a p-type substrate should be used as it will enhance the charge collection. Second, the sensing area has to be optimized such that ΔV is maximized, along with maximizing the probability of an alpha particle strike occurring. Third, the funneling effect being directly proportional to the applied bias [13], the diode should be biased at relatively high voltage, otherwise the effect of net loss in charge collection due to low bias should be compensated by making the sensing circuitry highly sensitive. The final step will involve designing circuitry that is sensitive enough to detect low voltage changes.

Using the above information and the simulation results a systematic design methodology will be presented in the next chapter.

3

Detector Circuit Design

3.1 Introduction

As a design objective, a highly sensitive circuitry is required to efficiently detect the small voltage changes produced due to alpha generated charge Q_{gen} , within the sense area. Furthermore, this constraint is aggravated due to the fact that the effect of generated charge in producing voltage offsets will be lower than expected as not all the generated charge would be collected by the sensing area, a point discussed in chapter 2. This also implies, that appropriate measures have to be taken to enhance the collection of the alpha charge to obtain optimum efficiency for the detector. These issues were explored using the simulation results and various modeling techniques, and a schematic for the detector is proposed. The simulation results are presented in this chapter.

3.2 CMOS Inverter as an Amplifier

The need for a highly sensitive circuit can well be satisfied by employing a CMOS inverter as an analog amplifier, such that the inverter is biased near its point of maximum gain. This choice is very simple, consumes minimum area, and yet is a very efficient scheme in detecting the voltage offsets. The schematic for an alpha particle detector employing the CMOS inverter as an analog amplifier is depicted in Figure 3-1 below.

Figure 3-1: Detector Schematic.

3.2.1 General Overview on Operation of the Detector

The capacitor, C_s , in Figure 3-1 serves as the collection area, the choice of which will be discussed later. The CMOS inverter is designed with the $V_{in}=V_{out}$ point, which is referred to as the “bias point”, shifted towards zero to lower the current, I_{DD} , and to achieve high gain. The transfer characteristic for the above circuit is shown in Figure 3-2 below.

Figure 3-2: Inverter Characteristic for the Detector

The inverter designed with high gain, if biased at the $V_{in}=V_{out}$ point, is expected to provide large voltage swing at the output due to a corresponding small change in the input

voltage. The operation of the circuit commences as follows: Initially, switch S_1 closes, precharge phase, forcing bias point to be the intersection of $V_{in}=V_{out}$ with static transfer characteristic. The circuit is designed so that this point is just below the point of maximum gain. S_1 opens, onset of collection time, after which a change in the input voltage by ΔV_{in} produces a large change ΔV_{out} at the output. C_s is connected to a high impedance point, the input of the inverter.

For the MITEL1.5 P-well process the detector can be designed by shifting the bias point of the inverter symmetrically towards the V_{DD} . The need for shifting the bias point arises due to the positive direction of ΔV_{in} induced by the generated charge, for P-well, so that corresponding logic threshold, ΔV_{out} , can be obtained in the opposite direction. This is depicted in Figure 3-2 below. The bias point has to be symmetrical towards the V_{DD} rail. After an alpha strike the input voltage is increased by ΔV_{in} due to which a corresponding ΔV_{out} is achieved.

The detector design is therefore compatible with p or n well technologies. It can be implemented using a digital process, as no analog components are required in the design.

Figure 3-3: Inverter Characteristic for the Detector for MITEL1.5

3.3 Sense Capacitor Design

Increasing the collection area compared to the surrounding circuitry, will greatly enhance the probability of collecting the alpha particles, as larger number of particles will be collected. The limiting factor on the size of C_s arises from the fact that the effect of Q_{gen} should not be obscured by the total charge present within C_s before the alpha hit. The

various types of capacitors that could be utilized as a sense capacitor using a CMOS technology are: (1) polysilicon capacitor (2) n-well to p-substrate, in an n-well technology, (3) p^+ diffusion to n-well (4) n^+ to p-well capacitances.

In a polysilicon capacitor there is no p-n junction, consequently no funneling would take place, to facilitate the separation of electron and holes. This implies that the amount of change in potential that will be obtained by using a polysilicon capacitor will not be as large as in a depletion capacitance. Therefore, designing C_s with polysilicon is not a good choice.

To achieve large sensing area with a low value of C_s , the capacitance per unit area should be low. This can be achieved by using the depletion capacitance of a well to substrate p-n junction to form C_s . The n^+ or p^+ diffusion to well capacitance is another alternative, but due to the heavier doping concentration of the well, the depletion width for the junctions is much narrower than that of the well to substrate p-n junction, thereby producing higher capacitance per unit area.

Therefore, for the purpose of this detector, the sense capacitor was designed using the well to substrate depletion capacitance. Figure 3-4 and 3-5 below show a cross section of an n-well to substrate depletion capacitance and a n^+ diffusion to p-well capacitance.

Figure 3-4: CMOS N-Well to Substrate Depletion Capacitor

Figure 3-5: N⁺ Diffusion to P-Well Capacitance

C_s , being a depletion capacitance arising from the p-n junction, as depicted in Figure 3-4, is a function of the applied bias. To determine the value of C_s , the junction profiles for CMOS4S and MITEL1.5 technologies were approximated and the depletion capacitance per unit area for various reverse-bias conditions was estimated by numerical solution of Poisson's equation using SEDAN3 [16]. The extracted values for the capacitance were plotted using Matlab as shown below in Figure 3-6.

Figure 3-6: Plot of well to substrate depletion capacitance as a function of bias. The plot shows the capacitance in F/cm² for reverse bias conditions only.

Since the sense capacitor is reverse biased by the inverter which was designed for a low bias point, around 1.5 volts, the capacitance value at this reverse bias is in the range of 4.2 nF/cm² and 8.2 nF/cm² for CMOS4S and MITEL1.5 respectively. Comparing both the processes, it is seen that capacitance values for the MITEL1.5 process are higher due to the heavier substrate doping used, resulting in a narrower depletion width hence increased

capacitance per unit area. Due to the unavailability of a profile for the junction in BATMOS, the capacitance values could not be extracted, instead CMOS4S capacitance values were used as the basis of sizing the sense capacitor for the detector design in BATMOS. Since both the processes are similar using the same kind of p-type substrate, the approximation should be valid. The primary reason for the choice of above technologies was the fact that these were accessible through the Canadian Microelectronics Center (CMC).

C_s was chosen to be $100\text{ }\mu\text{m} \times 100\text{ }\mu\text{m}$ in size to obtain a capacitance in the range of 0.4 pF for CMOS4S and BATMOS designs at a reverse bias in a range of 1.4 to 1.5 volts. The resulting potential change across the sense capacitor for CMOS4S due to an alpha strike can be calculated to be, as mentioned in section 2.7:

$$\Delta V = 0.16\text{V}/0.4\text{pF}$$

$$\Delta V = 0.4\text{ volts}$$

Since the sense capacitor is under reverse bias, there is a nonzero leakage current that will eventually discharge C_s . The effect of leakage current is discussed in the next chapter.

3.4 Inverter Design

The two major factors that are of significance in the design of the inverter are the need for high sensitivity and low power consumption. The need for reducing power consumption arises due to the fact that the inverter implemented as an analog amplifier, as

discussed in section 3.2, has high current, I_{DD} , at the bias point. Subsequently, power consumption can be decreased by lowering the bias point below the point of maximum gain as described in section 3.2.

Through the basic analysis of the inverter characteristics [17], it is evident that the voltage transfer characteristics are dependent on the ratio β_n/β_p of the devices, taken from [17]. A complete analytical model for inverter transfer characteristics can be derived, but incorporating the short channel effects (channel length modulation) to achieve a realistic model would increase the complexity of the analytical expression, therefore a complete expression involving the β terms was not derived. The β factor, in the analytical model, is given as:

$$\beta = \mu C_{ox} \left(\frac{W}{L} \right) \quad (3.2)$$

where μ = surface mobility of the carriers; C_{ox} = gate oxide capacitance.

The subscripts n and p refer to the respective device types. The β factor being dependent on device geometry can be changed for a given process. Therefore, if the ratio of the physical dimensions for both the devices is changed, a corresponding change will be obtained in the transfer characteristics of the inverter. Thus, the bias point, $V_{in}=V_{out}$, of the inverters will also be different with different device geometries, i.e different β_n/β_p . A corresponding shift will be observed in the transfer characteristics. A dc analysis was performed for an inverter, for various width ratios with a constant length. The simulation results are shown below.

Figure 3-7: Inverter Transfer Characteristics with W_n/W_p decreasing, from left to right, at $L_n=L_p=3.2\mu\text{m}$, with $V_{in}=V_{out}$. The centre plot is for $W_n=W_p=1.4\mu\text{m}$, with equal lengths of $3.2\mu\text{m}$ for all the curves. Going from left to the centre, the width are: $W_n=8.4$, 5.6 , and $2.8\mu\text{m}$ with W_p as $1.4\mu\text{m}$. The curves to the right of the centre are for widths: $W_p=8.4$, 5.6 , and $2.8\mu\text{m}$ with $W_n=1.4\mu\text{m}$.

The center curve is for $W_n/W_p=1$. The curves on the left are for $W_n/W_p>1$, on the right for $W_n/W_p<1$. It is clearly evident that the bias point can be lowered by making the width of NMOS device larger than that of the PMOS. The implication of making $W_n/W_p\gg 1$ is the inequality in charging and discharging times, which is not of significance for this design.

Therefore, the sizing of the inverters should be such that the bias point will be lowered

considerably. The actual dimensions are discussed section 3.4.1.

The second factor of importance is the need to enhance the gain of the inverter. Again, from the basic transistor theory it is evident that the small signal gain is an increasing function of drain to source resistance r_{ds} [17]. This implies that increasing the r_{ds} value by increasing the length of both the transistors, will enhance the sensitivity of the inverter. This improvement in the gain is achieved at the expense of speed which is tolerable as the circuit is assumed to function at kilohertz frequencies. A dc analysis of the inverter with varying lengths $L_n=L_p$ and a constant W_n/W_p was performed to show the possible enhancement in gain through the varying slopes of the transfer characteristics. The results are shown in Figure 3-8 below.

Figure 3-8: Transfer characteristics of a CMOS inverter with varying L_n, L_p , with $W_n/W_p=4$ with $W_p=W_{min}=1.4 \mu m$, and $W_n=5.6 \mu m$

The above simulation results show the transfer characteristics for increasing lengths from $L_n=L_p=L=0.8 \mu\text{m}$ to $L=4.0 \mu\text{m}$ from left to right, with $W_n/W_p=4$, and $W_p=W_{\text{min}}=1.4 \mu\text{m}$.

It is clearly seen that gain can be maximized by increasing the length of the inverter transistors. The actual selection of the lengths is discussed in the next section.

3.4.1 Selection of Transistor Width Ratio and Gate Lengths

The overall design is thus based on three design parameters two of which were mentioned in the above section, namely high gain and low power consumption. The third parameter of interest is the maximum area coverage by C_s compared to that of the remaining circuitry.

To construct a basic design methodology, a time domain analysis was performed on the circuit from which the ΔV_{out} and current I_{DD} were extracted. ΔV_{out} is taken to be the difference between the minimum V_{out} and the maximum V_{out} before and after an alpha strike. These two parameters were extracted for various lengths and width ratios. The plots below in Figures 3-9 and 3-10 show the ΔV_{out} and I_{DD} as a function of transistor length L , for various W_n/W_p .

Figure 3-9: Extracted ΔV_{out} as function of Transistor lengths for varying width ratios

Figure 3-10: Extracted I_{DD} as function of transistor lengths with varying width ratios

The above plots show that gain and the peak current are dependent on the transistor width ratio and gate lengths. By moving to a larger width ratio one can obtain high gain, thereby enhancing the sensitivity of the detector, at the expense of an increase in current. A decrease in the current can be achieved by choosing larger lengths, thereby consuming more area and consequently reducing the percentage of total area covered by C_s . It is suggested that the PMOS transistor should be designed with a minimum width of $1.4 \mu\text{m}$, as increasing the width of PMOS transistor provides no enhancement in gain nor in reduction of the operating current. It is also evident that as the transistor lengths increase, the corresponding input capacitance also increases, thereby attenuating the gain for

transistors with large gate lengths. The attenuation in ΔV_{out} is a direct consequence of the fact that finite Q_{gen} is distributed over a larger capacitance, thus reducing the change in the potential across the sense capacitor.

In concluding the above section, it can be said that the actual sizing of the transistor depends on how area coverage, gain, and the current requirements are set.

The actual dimensions of the inverter transistors that were chosen for the chip are tabulated in Table 3-1. As discussed above, the width of PMOS transistor was kept at the minimum value allowed by the design rules. The width for the NMOS transistor was chosen to be four times the width of the PMOS transistor. The length was kept at four times the minimum length of $0.8 \mu\text{m}$. This choice of dimensions provide the maximum gain but at the expense of higher current. The reason for designing the inverter transistors with the above dimensions was the fact there was as an uncertainty in predicting the amount of charge that can be collected by the sense capacitor C_s . This uncertainty was the basis for aiming towards the highest gain although tolerating higher operating current. Results from dc analysis are shown below in Figure 3-11.

Table 3-1: Transistor dimensions for the inverter

Transistor	Length	Width
PMOS	$3.2 \mu\text{m}$	$1.4 \mu\text{m}$
NMOS	$3.2 \mu\text{m}$	$5.6 \mu\text{m}$

Figure 3-11: Static Transfer characteristic for the detector inverter.

3.5 Simulation

The actual circuit that was simulated initially using the above transistor dimensions is shown in Figure 3-12 below. A PMOS transistor was used as a switch to precharge the inverter at the bias point. For simulation of the detector schematic, the sense capacitor was initially modeled as a polynomial capacitor inside the simulation file. The polynomial model specifies the value of a capacitor as a function of the applied bias. The polynomial coefficients were extracted by fitting a polynomial, using Matlab, on the points that were extracted for well to substrate depletion capacitance from SEDAN3. Although the polynomial capacitor models the actual dependence of the C_s value on the voltage across

its nodes, the effect of leakage current is not taken into account. Later, a diode model was used, to replace the polynomial capacitor, to represent the well to substrate depletion capacitance C_s , with the depletion capacitance of the diode modeling the sense capacitor. The simulation results were obtained using the diode model for the sense capacitor, C_s .

Figure 3-12: Detector Schematic.

3.5.1 Modeling the α -Strike

It was discussed on page 27 section 3.3, that the change in potential following an alpha

strike, for the case where C_s is designed in BATMOS, was approximately 0.4 volts, assuming that all the generated charges are collected by C_s . As the actual percentage of the charge that would be collected by C_s is uncertain, a pessimistic approach was taken and the value of alpha generated charge was arbitrarily reduced to 40% in simulating the detector. Using the available tools, the ΔV_{in} due to this charge was modeled with a voltage source using a pulse function, in series with C_s . The amount of ΔV_{in} for the pulse was taken as -0.16V, which was calculated using 64 fC as the generated charge, 40% of 160 fC that would be generated by an alpha strike, and 0.4 pF for the sense capacitor, as discussed in section 3.3. The negative value for ΔV_{in} implies that the Q_{gen} lowers the potential across C_s by ΔV . Initially the pulse was set to zero and the onset of an α -hit was simulated by lowering the pulse below its initial value of zero and then returned to zero just before the next precharge cycle.

3.5.2 Simulation of the Detector

The schematic shown in Figure 3-12 was simulated with the voltage source in series with C_s as described in the above section. The potential across C_s was set initially set to zero, to make sure that C_s is discharged before the circuit is precharged to $V_{in}=V_{out}$, the bias point, using the .IC command in HSpice. The complete clocking scheme was split into two cycles, namely the precharge phase and the collection phase. The precharge phase starts when ϕ goes low closing S_1 and thereby biasing the circuit at the $V_{in}=V_{out}$ point. The

collection cycle commences when ϕ goes high, opening S_1 . It is during this phase that an alpha strike is simulated by dropping the input by $\Delta V_{in} = -0.16$ V. Since C_s is precharged to the bias point, any change in the potential at the input will be amplified by the inverter. A time domain analysis was performed for the above circuit, as shown in Figure 3-13 below.

Figure 3-13: Time domain analysis of the Alpha Particle Detector

The plot for the input and the output, third from the top, shows that the circuit is biased at approximately 1.4 V, the bias point. The duration of the precharge pulse was made considerably shorter than the collection time. At the onset of the collection cycle (around 3

μsec), the output is expected to stay at $V_{\text{in}}=V_{\text{out}}$, the point to which it was precharged, unless an α event occurs during the collection time. On the contrary it is seen in the above plot that the output goes lower than the precharge value at the onset of the collection cycle. The decrease in the output implies that the input had moved from the bias point thereby causing the output of the inverter to go low. This fluctuation of the input is a direct consequence of a well known clock feedthrough phenomenon. The clock feedthrough concept and cancelling techniques are discussed in the next section.

3.5.3 Clock Feedthrough

The clock feedthrough phenomenon originates from the charge sharing capacitances associated with the feedback transistor switch S_1 at the input node. During the precharge cycle, when the clock ϕ is low, the gate to source capacitance C_{gs} and the sense capacitor in parallel are charged to the bias point of 1.4 V. At the onset of the collection cycle, when the clock ϕ goes to 5 volts, the gate node of C_{gs} switches from the previous ground potential towards 5 volts. Both these capacitances form a voltage divider. This change in the node potential causes an increase in the charge which is subsequently shared with the sense capacitor, causing its potential to rise. Since the inverter input is floating at the bias point, and is designed to have a high gain, this subsequent increase in the potential on C_s is greatly amplified by the inverter thereby lowering the inverter output.

An approach towards cancelling the feedthrough problem was implemented by using

a charge cancelling scheme. The scheme involves an addition of a dummy transistor M_c connected at the input node with its drain and source shorted and a complementary gate signal ϕ' . Since the source and the drain are shorted, both C_{gs} and C_{gd} capacitances associated with M_c participate in clock feedthrough, while only C_{gs} of the feedback transistor is effective. Therefore the width of the cancelling transistor was made half of that of the feedback transistor, while the lengths of the two devices were made equal [18][19]. The stray capacitances of the cancelling transistor and C_s also form a voltage divider with node potentials switching in the complementary manner thereby removing the extra charge that was initially introduced on C_s . The schematic of the detector with the cancelling transistor is shown below.

Figure 3-14: Complete Schematic for the Detector

The dimensions for the cancelling transistor and the feedback transistor are tabulated below in Table 3-2, along with those of the transistors in the inverter itself.

Table 3-2: Physical dimensions for the transistors

Transistor	Length	Width
PMOS M_1	$3.2 \mu\text{m}$	$1.4 \mu\text{m}$
NMOS M_2	$3.2 \mu\text{m}$	$5.6 \mu\text{m}$
Feedback Tr S_1	$0.8 \mu\text{m}$	$2.8 \mu\text{m}$
Cancelling Tr, M_c	$0.8 \mu\text{m}$	$1.4 \mu\text{m}$

The lengths of M_1 and M_c are kept at minimum. As the width of S_1 is supposed to be twice of that of the cancelling transistor M_c , the width for M_c was chosen as the minimum width allowed by the technology rules.

A time domain analysis for the complete detector schematic was performed, the results of which are shown below in Figure 3-15

Figure 3-15: Transient Analysis of the Complete Detector Schematic

It is evident from the above simulation results that the clock feedthrough effect is greatly reduced, although exact cancellation is not achieved. The output is now only about 25 mV below the bias point after the precharge, which is negligible.

3.6 Sensitivity Variation

Variation in sensitivity is expected due to a shift in the bias point as a result of process parameter variation and threshold voltage fluctuations. Additional time domain analyses were performed to predict the performance of the detector under these inevitable variations.

3.6.1 Effect due to Process Parameter Variation

Using the available simulation tools, it was not practical to predict the change in gain due to variations in all the process parameters. Instead, a Monte Carlo analysis was performed with a Gaussian distribution of channel dimensions with 3 sigma deviation of +/- 10%. This was necessary since CMC did not provide the variance of model parameters. The effect of any practical variations in process parameters on sensitivity of the detector are expected to be reflected by performing the above Monte Carlo analysis with the +/- 10% variation on the physical dimensions of the transistors. Thus, a transient analysis with 30 Monte Carlo sweeps was performed to predict the effects. The results are shown below in Figure 3-16.

Figure 3-16: Transient Simulation of the detector showing the effect of parameter variation on the output.

The above results show that the effect of variation in parameters is not detrimental to the circuit functionality. The variation in the output is confined within a definite region and the reduction in the gain is tolerable.

3.6.2 Effect of Change in Temperature

The effect of temperature on the gain is primarily due to the dependence of the threshold voltage, V_t and the leakage current on temperature. The dependence of mobility on temperature is not of concern due the dependence of inverter transfer characteristics on the ratio of the mobilities [17], thus cancelling the temperature dependence through the

ratio of the carrier mobilities. The dependence of threshold voltage of a MOS transistor on temperature stems from the temperature dependence of the intrinsic carrier density, which is modeled within the bulk potential ϕ_b , in the V_t equation. This temperature dependence of V_t is expected to cause a shift in the bias point thereby affecting the gain. Thus, in order to predict the functionality of the detector under extreme temperatures, a transient analysis of the detector schematic was performed at -70, +25 and +70 degrees celsius. The results are shown in the Figures 3-17 to 3-19.

Figure 3-17: Transient simulation of the detector at room temperature of 25 degrees celsius.

Figure 3-18: Transient simulation of the detector at +70 degrees celsius

Figure 3-19: Transient simulation of the detector at -70 degrees Celsius

Comparing the response of the detector at room temperature, -70 and +70 °C, the ΔV_{out} at -70 degrees is slightly greater than at the room temperature. Similarly, the ΔV_{out} at +70 degrees is 0.1 V lower than at -70 degrees. This suggests that depending on the operating temperature of the detector, the sensitivity will vary slightly but not enough to affect a logic threshold swing. The results are summarized below in Table 3-3.

Table 3-3: Summary of results at various temperatures

Temp	Bias Point	V _{out}	Output Swing
Room	1.43 V	4.01 V	2.58 V
-70 °C	1.40 V	4.06 V	2.66 V
+70 °C	1.42 V	3.98 V	2.56 V

3.6.3 Power Supply Variation

To explore the effect of variation in power supply on the detector a time domain and dc analyses were performed. The transient analyses were performed with varying the power supply between 4 to 5 volts with a 0.2 V step, and to predict the effect of power supply noise on the detector a step of 50 mV with a 0.1 µsec duration was given on the power supply. The dc analysis was performed to see how switching point shifts. The simulation results are shown below from Figure 3-20 to 3-22.

Figure 3-20: Static transfer Characteristics Varying with power Supply Variation from 4.0 to 5.0 volts.

Figure 3-21: Transient Simulation of the Detector with Power Supply Varying from 4.0 to 5.0 volts.

Figure 3-22: Transient Simulation of the Detector with 50 mV Noise on the Power Supply for 0.1μsec duration.

The dc simulation shows that as the power supply is varied the switching point shifts towards the left which would subsequently decrease the ΔV_{out} , as apparent from Figure 3-21. A total of one volt change in the power supply changes the ΔV_{out} by approximately half a volt. Figure 3.22 shows the effect of power supply noise. The interesting point is to observe the effect of noise during the collection time wherein the input node is floating and thus vulnerable to noise. It is clear that the output also rises by only 0.4 V due a noise spike of the same amount. The two spikes in the opposite directions are in response to two spikes of noise on the supply in the opposite directions.

This suggests that an output transient due to noise is unlikely to be erroneously interpreted as an alpha event.

3.7 Sensitivity of the Detector to an Alpha Strike

To predict the behavior of the detector in detecting the alpha strikes from a sample of radon containing air, it is necessary to know the minimum amount of collected charge the detector could sense. Therefore, a transient analysis was performed in which the ΔV_{in} due to an alpha strike was varied as: -0.16, -0.08, -0.04, -0.02, -0.018, -0.016, -0.014, -0.012, -0.01 and -0.005 volts respectively. The simulation result is shown below in Figure 3-23.

Figure 3-23: Transient Analysis of the Detector with alpha strike pulse varying as: -0.16, -0.08, -0.04, -0.02, -0.018, -0.016, -0.014, -0.012, -0.01 and -0.005 volts. The corresponding V_{out} pulses are shown from top to bottom.

From the above simulation it is evident that no appreciable output swing is obtained for ΔV_{in} of -0.01 and -0.005 V. Considering, possibility of noise due to electromagnetic interference and other factors, a threshold of -0.014 V can be arbitrarily set as a minimum voltage detectable due to an alpha particle strike. For the size of capacitor in the design this corresponds to a collected charge of 5.8 fC. This collected charge would be generated due to an incident alpha particle of approximately 1 MeV energy. This calculation can be used to predict the maximum distance of an alpha particle in a sample of air, from the detector surface, that could be detected. Using a plot of alpha energy versus distance, in air [22], it is estimated that alpha particles lose energy in air at a rate of approximately 1.3 MeV/cm. This implies that almost all of the alphas from a sample of air enriched in radon within 3–4.5 cm,

from the detector surface, can be detected.

This result shows that the sensitivity of the detector is high. By varying the threshold limit on the minimum ΔV_{in} , a discrimination can be made between the alpha particles detected from the decay of radon and those from the short lived radon progeny.

3.8 Summary

This chapter presented the design schematic for layout and fabrication of an Integrated Alpha Particle Detector. The main concern in the design was the requirement of high gain to achieve high sensitivity, due to the uncertainty in predicting the collection efficiency. As a first design the gain was made extremely high, consequently the standby current was large. A step by step methodology was presented and a CMOS inverter was suggested to be used as an analog amplifier to amplify the low voltage offset due to an alpha particle.

It was concluded that the depletion capacitance of a well to substrate p-n junction could serve as the sense capacitor for the detector.

The CMOS inverter amplifier was studied in detail and with the support of simulation results the proper size for the inverter transistors were determined.

The clock feedthrough problem was discussed, a cancellation technique was employed for the proper functionality of the circuit.

Factors affecting the sensitivity of the detector were discussed and various simulation results were presented including Monte Carlo analysis to predict the behavior of the detector in response to these factors.

It is therefore concluded that the suggested design could work under all the practical process, temperature and power supply variations. To increase the noise immunity, a stabilized power supply should be sufficient.

4

Detector Layout

4.1 Introduction

This chapter will focus on layout issues and testing procedures of the proposed detector.

A comparison is made in the simulation parameters for the three different technologies along with their influence on the performance of the detector. The simulation results of the layouts are also presented and susceptibility to the interconnect parasitics is discussed. Appropriate routing of the interconnects to minimize the parasitics, and a specific layout approach to obtain better compaction is presented. The various designs that were submitted for fabrication to resolve uncertainties in quantizing the collected charge due to an alpha strike are also mentioned.

4.2 Technology Selection

The layout was carried out at Carleton using the CADENCE design software supplied by CMC. The accessible technologies were CMOS4S, BATMOS and MITEL1.5. The proposed design schematic was laid out for submission in all the three technologies. The

primary reason for submitting the design in all the above technologies was to explore the performance of the detector fabricated through each of the technologies. The simulation of the extracted layouts was performed using the spice parameters provided by CMC [20]. The major differences in the parameters between each of the technologies is tabulated below in Table 4-1.

Table 4-1: Simulation parameters for different technologies

Parameters	CMOS4S	BATMOS	MITEL1.5
Minimum Gate Length	1.2 μm	0.8 μm	1.5 μm
T_{ox}	25.0 nm	17.52 nm	27 nm
V_T	0.79, -0.84 V	0.81, -0.90 V	0.828, -0.56V
μ_n , electron mobility	577 cm^2/Vs	475 cm^2/Vs	532 cm^2/Vs
μ_p hole mobility	205 cm^2/Vs	154 cm^2/Vs	138 cm^2/Vs

Although the above tabulated parameters differ from one technology to the other, they present no restriction for the detector to be implemented using any of the above technologies. The difference in the parameters will present some advantages and disadvantages between the technologies. Comparing the above data it is seen that BATMOS technology has the smallest device size, 0.8 μm gate length, implying that area consumption can be reduced. Lower oxide thickness implies that the current at the operating point of the detector would be higher, comparing to the inverter with the same transistor dimensions in CMOS4S or MITEL1.5. The current consumption can thus be

reduced by moving to other technologies at the expense of increased chip area. Also, the cost of BATMOS is much higher than that of the others with no added advantage for this application.

For the initial design phase, the layout was carried out in CMOS4S, MITEL1.5 and BATMOS technologies. A time domain analysis of the detector layouts in BATMOS and CMOS4S is shown below in Figures 4-1 to 4-4.

Figure 4-1: Transient Simulation of the detector Layout in BATMOS technology.

Figure 4-2: Transient Simulation of the Detector Layout in CMOS4S technology.

Figure 4-3: Bias Point with effective ΔV_{in} for BATMOS and CMOS4S layouts.

Figure 4-4: Total Current at the Bias Point for BATMOS and CMOS4S designs.

The bias points, gain and the effective ΔV_{in} , V_{in}' are summarized in Table 4-2 below.

The effective ΔV_{in} is defined as the effective voltage drop that appears at the input node of

Table 4-2: Simulated results for BATMOS and CMOS4S

Parameter	CMOS4S	BATMOS
Bias Point	1.46 V	1.43 V
$\Delta V_{in}'$	0.12 V	0.13 V
ΔV_{out}	2.56 V	2.58V
Gain	21.3	19.8
Current	111 μ A	374 μ A

the inverter as a result of an alpha strike on the sense capacitor, where an alpha strike was modeled with a pulse of -0.16 V as discussed in section 3.5.1.

Inspecting the above results it can be seen that $\Delta V_{in}'$ in CMOS4S is reduced by 40mV, whereas in BATMOS the reduction is only by 30mV, compared to the applied ΔV_{in} of

0.16V in simulation. The extra loss in ΔV_{in} for the CMOS4S design can be attributed to larger parasitics, for example larger input capacitance, in CMOS4S due to relatively larger device geometries than in the BATMOS design. The gain in CMOS4S is seen to be larger than in BATMOS by a factor of 1.5. Since the gate lengths of the transistors in CMOS4S are larger than that of the BATMOS, therefore the drain to source resistance, r_{ds} , in CMOS4S design is larger than that of the BATMOS. Thus, the devices in CMOS4S having larger r_{ds} value contribute towards higher gain.

The total current for CMOS4S at the bias point is approximately 111 μ A and 374 μ A for the BATMOS design. As discussed earlier, this difference is due to the smaller gate length and thinner oxide layer in BATMOS. The above simulation results were obtained for same W_n/W_p and $L_n=L_p$, as described in chapter 3.

In concluding the above section it can be said that CMOS4S would serve as a better and appropriate technology for the implementation of the detector.

4.3 Layout Design

The proposed schematic design was laid out and submitted, in all the three technologies, with on chip clock generation circuitry and a non-inverting output buffer. The output buffer as well as the clock generation circuitry designs were based on the available cell library. The layouts were extracted and the generated netlists were simulated along with the interconnect parasitics.

4.3.1 Sense Capacitor Layout

The sense capacitor was laid out in $100\text{ }\mu\text{m} \times 100\text{ }\mu\text{m}$ square geometry. The metal layer and contacts were made around the periphery in order to reduce energy loss of the incident alpha particles that would have been expended in penetrating through the metal layer. The n+ diffusion was made all throughout the well. A guard ring was made around the outside of the capacitor and grounded primarily for reducing the possibility of any latch up due to the generated charge and to isolate the individual sense capacitors, if required. The layout of the sense capacitor is depicted in Figure 4-5.

Figure 4-5: Sense Capacitor Layout

4.3.2 Interconnect Parasitics

During the simulation of the layouts it was observed that the interconnect parasitics contributed in increasing the clock feedthrough. The interconnect parasitics that contributed to the additional feedthrough were identified to exist in the close proximity of the input node, node common between the well capacitor, the inverter input, and the source end of the feedback transistor participating in extra charge sharing. Figure 4-6 highlights

the region where the coupling gives this problem. The transient analysis of such a layout is shown below in Figure 4-7.

Figure 4-6: Layout area highlighting the region sensitive to parasitics, pointed by the arrow.

Figure 4-7: Transient analysis of the layout showing V_{in} vs. V_{out} with the effect of interconnect parasitics on the output voltage.

The arrow points towards the change in the output voltage at the end of the precharge cycle, due to an additional charge sharing contributed by the interconnect parasitics. The 40 mV of change at the output of the high gain inverter gives an estimate of how little the charge was removed from the input node. Therefore, careful attention has to be paid on routing the interconnects. The new approach in routing the interconnects was combined with an approach, presented in the following section, for obtaining better compaction in the area consumed by the inverter transistors.

4.3.3 Layout Compaction

As discussed in section 3.4.1, maximizing the area coverage for C_s , thereby reducing the area taken up by the transistors, demands careful attention in the layout of the circuitry. The trade-offs involved were considered and a methodology is proposed in the Figure 4-8 as a basis in allocating the area for the transistors.

The lengths, in determining the contours points, at various width ratios were calculated. Using these two points for each contour, subsequent simulations were performed and the corresponding ΔV_{out} was then extracted. In calculating the lengths, the fraction of total area occupied by the inverter transistors was identified as a variable. The area taken up by the extra circuitry was considered as a constant. The percentage of area coverage required by C_s was then used to calculate the corresponding lengths of the inverter transistors for the three different width ratios. Using these two parameters the corresponding value for ΔV_{out} was extracted through simulation.

Figure 4-8: ΔV_{out} as a function of transistor length for various widths, with contours showing the area coverage for C_s .

The contours in the above plot show the various combination of transistor lengths and widths to achieve a certain percentage of area coverage by C_s , and the subsequent tradeoffs involved. Thus, if an 84% area coverage is desired then one can choose a combination of $L_n=L_p=4.8 \mu\text{m}$ with $W_n=4 \times W_p$ and $W_p=W_{min}$. The same coverage can be achieved by choosing a width ratio of $W_n=2 \times W_p$ and $W_p=W_{min}$ with $L_n=L_p=8 \mu\text{m}$, with a subsequent decrease in current but at the expense of reduction in ΔV_{out} . Similar is the case of going to an increased length and lower width ratios, thereby reducing the current with a further loss

in ΔV_{out} , to obtain the same percentage of area coverage. Thus, in order to assign the physical dimensions for the transistors one has to specify the desired area coverage, ΔV_{out} and the operating current.

4.3.4 Circuit Layout and Interconnect Routing

As discussed in section 4.3.2, the need for careful attention for routing the interconnects stems from the additional charge sharing caused by the interconnect parasitics at the input node causing an instability in the output voltage at the end of the precharge cycle. In order to minimize the charge sharing at the input node the crossover of the interconnects at the input node had to be minimized. Due to this requirement on the routing of the interconnects and the need for better compaction for the transistors, the nodes common to the various transistor source and drain ends were determined and laid out on the same diffusion. Inspection of the schematic in Figure 4-6 shows that the common nodes for the PMOS transistors are of the inverter PMOS, the feedback switch transistor and the cancelling transistors. The drain ends of inverter PMOS and that of the feedback switch transistor shared a common diffusion layer. Similarly, the source end of the feedback switch transistor and the shorted drain and source ends of the cancelling transistors shared a common diffusion layer. This subsequently minimized the crossover of the interconnects at the input node as the interconnects to the input node were on one side and the remaining interconnects at the opposite side. The figure below shows the layout of

the transistors using the above strategy in the BATMOS technology.

Figure 4-9: Layout section showing the compaction achieved for the transistors with no crossover between the interconnects for the input node and interconnects carrying the clock signals. The arrow points to the input node interconnect going to the sense capacitor C_s .

The simulation results of the layout for the detector with no crossover of the concerned interconnects are shown below.

Figure 4-10: Time domain analysis of the detector layout with minimized interconnect parasitics. The plot shows V_{in} & V_{out} before and after an α event.

Inspecting the results above it can be clearly seen that the effect of interconnect parasitics is greatly reduced by careful routing of the interconnects in the layout of the detector circuit. Since the effect of interconnect parasitics was seen in the later designs the above strategy was implemented in later submissions of the design. The layouts for the initial and later design submissions are shown in Appendix A.

4.3.5 Design Submissions

All the layouts were checked for DRC violations, extracted and subsequently simulated prior to their submissions. In the initial phase of submissions, the detector was laid out in all the three technologies with on chip clock generation and a digital output buffer. The designs were submitted through CMC for fabrication. In the second phase of the submissions the detector was laid out with an on chip analog buffer at the input and output nodes, in addition to the digital buffer at the output node.

The submitted design layouts are shown in Appendix A where:

Figure A-1: Layout of the detector in BATMOS with a digital buffer at the output and an uncommitted sense capacitor. (This was the chip that was tested)

Figure A-2 Layout of the detector in BATMOS with analog buffer both at the input and the output with an additional digital buffer at the output node. It also consists of an uncommitted opamp.

Figure A-3 Layout in CMOS4S with a digital buffer at the output, compact layout, with an uncommitted sense capacitor.

Figure A-4 Same as in Figure A-3 but with an additional analog buffer at the input node.

Figure A-5 Same as in Figure A-4 with an additional analog buffer at the output node.

4.4 Summary

This chapter dealt with layout issues of the detector. A comparison was made between the three technologies and tradeoffs involved with each one were explored. The possibility of implementing the design layout in all three technologies was confirmed.

The effects of interconnect parasitics were shown through simulation results and subsequently methods for reducing interconnect parasitics and achieving compaction in the layout were presented.

5

Testing

5.1 Introduction

This chapter focuses on testing of the fabricated detector chip. There is a brief discussion of the experimental set-up. A comparison is made between the measured results and those predicted.

The designs submitted in the initial phase, from all three technologies, were received and tested. The CMOS4S chips were in 60-PGA packages and the MITEL1.5 and BATMOS chips were in 40 pin DIP packages. The chips from CMOS4S and MITEL1.5 were found to be nonfunctional due to a layout error. The error was in the use of a split substrate contact instead of a plain substrate contact for the switch and the feedthrough cancelling transistors. This error was not detected by simulation of the layouts. Due to the presence of split contacts the input node was pulled high, to V_{DD} , after precharge. Visual inspection of the layout confirmed the above error. This error was not present in the BATMOS layout. Therefore, the BATMOS chip was tested for which the results are presented in the following sections.

5.1.1 Experimental Setup

The testing was initially performed in the CRPP (Center for Research in Particle Physics) lab of the Physics Department at Carleton. ^{241}Am was used as the alpha particle source for testing purposes. The source was calibrated using a commercial photodiode detector and a preamplifier that was available at the CRPP lab. The source was found to have an intensity of 0.9 μCi to 1.0 μCi .

The chip to be tested was mounted on the inside of a vacuum chamber lid and the source was located inside the cylindrical chamber as depicted in Figure 5-1. The vacuum condition was required so that the alpha particles could reach the detector surface with no energy loss. Feedthrough sockets were employed for I/O connections with the chip inside the chamber. A digital counter was used to provide a visual reading capability of an alpha strike. The figure below shows some of the essential blocks of the setup with approximate dimensions.

Figure 5-1: The Experimental Setup for Testing

The test equipment included an oscilloscope and a pulse generator. The pulse generator was used for clocking the detector with a clock of 1.5 ms repetition rate, and a precharge pulse of 100 μsec . Thus, the precharge time was only around 6.7% and the collection time around 93.3% of the total time. The measurements were performed at three different distance between the source and the detector.

5.1.2 Predicted and Measured Results

The ^{241}Am source with an intensity of 1 μCi is expected to produce 2.22×10^6 disintegrations/min. During measurements, if the source and the detector are separated by a distance r , then from solid geometry one can see that the number of alpha particles

reaching the detector will obey an inverse square law with the distance r . This dependence can be calculated by taking the solid angle subtended by the source. This is depicted in the figure below.

Figure 5-2: Fraction of alpha particles reaching the detector.

Thus, the number of disintegration the detector will count, can be computed as:

where

$$C = \frac{2.22 \times 10^6}{4\pi r^2} (\text{Detector Area}) \text{ dis}/(\text{min})$$

Simplifying the above equation, the total counts per hour, cph, are $1.06 \times 10^7 / r^2$. For a detection area of $100 \mu\text{m} \times 100 \mu\text{m}$ the predicted counts will have a dependence on the distance as, $1.06 \times 10^3 / r^2$ with r in centimeters. The predicted counts per hour at three different distances are tabulated below.

Table 5-1: Predicted counts as a function of distance.

Distance in cm	Counts per hour cph
12.4	6.9
10.4	9.8
7.1	21

The ten packaged chips were tested out of which nine were found to be functional. One possibility for chip non-functionality is static discharge.

The counter that was used for the measurements was an in-house digital counter, primarily made for teaching purposes. The input threshold for counting was at 2.5 volts.

All the nine chips were monitored for 90 minutes at a distance of 12.4 cm from the source. Since the chips were designed with an on chip digital buffer at the output, the actual output swing, ΔV_{out} , was not possible to observe. Instead, a 0 to 5 volts pulse transition was observed at the output for each alpha strike. The measured counts per hour, cph, are tabulated below. For a Poisson distribution of counts the expected error is given by:

$$\text{Error} = \frac{\sqrt{\text{Counts}}}{\text{Totaltime}}$$

Table 5-2: Measured counts for nine chips at a distance of 12.4 cm from the source

Chip Number	Counts per hour cph
1	8.4 ± 0.6
2	34 ± 4.8
3	27 ± 4.2
4	27 ± 4.2
5	32 ± 4.6
6	44.7 ± 5.4
7	38.7 ± 4.6
8	36 ± 4.9
9	14.7 ± 3.2

Comparing the counts in Tables 5-1 and 5-2, it is seen that the measured counts are much larger than the predicted counts. Two possible mechanisms could be responsible: susceptibility of the detector to electromagnetic interference, or an effective detection area larger than $100 \mu\text{m} \times 100 \mu\text{m}$. To test the former possibility, two of the nine chips were tested over a period of 72 hrs under vacuum without an alpha source, to check for the possibility of noise or interference pickup. After a complete period of 72 hrs the count was still found to be zero.

Since the area taken up by the transistors connecting to the input node of the inverter is not negligible, therefore there is a high chance that an alpha strike in the region outside the sense capacitor area could easily be sensed. For the verification of the above possibility,

further measurements were performed with three different chips at three distances between the source and the detector. The results of this measurements are tabulated in Table 5-3.

Table 5-3: Measured counts for three chips at three distances

Chip	12.4cm	10.4 cm	7.1 cm
1	8.4 ± 0.6	12.9 ± 0.7	21.3 ± 3.7
3	27 ± 4.2	35.3 ± 4.8	88 ± 7.6
6	44.7 ± 5.4	64 ± 6.5	118 ± 8.9

If the factor contributing to the increased number of measured counts is really a larger effective area then it is expected that a $1/r^2$ fit can be plotted within the error bars of the measured counts using one of the point from the measured results. This plot was generated as shown below in Figure 5-3

Figure 5-3: Measured count rate for the three with a $1/r^2$ fit within the error bars.

The above plot shows that the $1/r^2$ characteristic can be plotted within the measured error bars. This implies that the measured results are in reality the respective alpha counts and thus obey the inverse square law. The extra measured counts can therefore be contributed to the increased effective area.

From Table 5-2 variation in measured counts is seen between the chips, implying the existence of sensitivity variation between the chips. The variation in sensitivity in turn could be a consequence of process parameter variations between die. To explore the effects of parameter variations, the leakage currents for the well to substrate depletion capacitance were measured for all the nine chips. The data for the extracted leakage currents is tabulated below.

Table 5-4: Extracted leakage currents at -1.5 V, and cph at 12.4 cm. from the source

Chip Number	Leakage Current at -1.5 Volts	Counts per hour cph
1	250 fA	8.4 ± 0.6
2	3350 fA	34 ± 4.8
3	750 fA	27 ± 4.2
4	550 fA	27 ± 4.2
5	700 fA	32 ± 4.6
6	5005 fA	44.7 ± 5.4
7	650 fA	38.7 ± 4.6
8	400 fA	36 ± 4.9
9	1400 pA	14.7 ± 3.2

Variation in leakage currents can cause variation in sensitivity due to the fact that a chip with high leakage currents will require less charge to lower the potential at the input node. Thus, chips with higher leakage currents are expected to be more sensitive, thereby exhibiting higher counts. The plot below shows the measured counts as a function of leakage current for each chip.

Figure 5-4: Leakage current versus counts per hour. The numerical figure specify the chips number.

From the above graph it can be seen that the chips along the line are expected to have variation in sensitivity when operated at fast clocks, thereby exhibiting variation in counts.

To verify the above predictions, two chips were tested from those along the line for a duration of 90 minutes at clock rates of 1.5 msec and 150 μ sec duration. The results are tabulated below.

Table 5-5: Counts for chips at different clock rates

Chip Number	Clock Rate	
	1.5 msec	150 μ sec
6	44.7 ± 5.4	20 ± 3.65
2	34 ± 4.76	28 ± 3.74
5	32 ± 4.6	31.6 ± 1.35
3	27.3 ± 4.2	25.8 ± 1.19

The above results show that sensitivity variation between the chips is somewhat dependent on variation in leakage currents. The chips, 3, 4, 5, 7, 8 seem to have sensitivity dependence on a factor other than the leakage current. This second possible mechanism for variation in sensitivities of these chips is the possible variation in the gain of each chip. Since gain is dependent on the output conductance of a MOS device [17], any variation in the conductance will directly affect the gain. For example, the number of measured counts for chip #2, with leakage current of 3350 fA, do not change much when operated at a faster clock rate. This implies that the sensitivity variation is not a consequence of higher leakage but a consequence of variation in the gain or in the minority carrier diffusion length.

Thus, for certain chips the variation in the measured counts between the chips is a consequence of all the above factors, while for some of the other chips only one of the factors is contributing.

The above discussion provides an explanation for the variation in the measured results.

More accurate results, with long duration of measurements to reduce the statistical errors are required. This point is further considered in chapter 6.

5.2 Summary

This chapter was devoted to experimental results from the chips tested. Test results were presented and analyzed to show that the inverse square law was obeyed. The susceptibility to interference and noise was negligible. The variation, in the measured counts, between chips was discussed and an attempt was made to identify the factors responsible. The disagreement between the predicted and measured count was shown to be the consequence of increase in the effective detection area, attributed to high leakage currents for some chips, and variation in gain due to a possible variation in the output conductance of the devices and maybe to variation in minority carrier diffusion length too.

The test results confirm that it is possible to detect alpha particles using a simple on-chip sense amplifier in designing an integrated alpha particle detector.

6

Conclusions and Recommendations

6.1 Summary and Conclusions

The goal of this thesis was to demonstrate the principle of detecting alpha particles, produced in radon decay, with an integrated circuit compatible with conventional CMOS technology and to design and test the detector.

Chapter 1 gave an overview on the properties and hazards of radon gas. Chapter 2 focussed on the interaction of the alpha particles, which are produced in radon decay, with silicon. The amount of charge produced by an alpha particle strike, within a biased pn-junction was calculated to be 160 fC. The effect of this generated charge in changing the potential across a sense capacitor, implemented using the depletion capacitance of a well to substrate p-n junction, was the basis for developing an integrated circuit for the purpose of detecting the alpha particles produced in radon decay.

In Chapter 3, design methodology was presented for developing a circuit to amplify the small voltage change, caused by the generated charge within a sense capacitor. It was suggested that a CMOS inverter, biased at the $V_{in}=V_{out}$ point of approximately 1.5 V,

would serve as an analog amplifier to amplify the potential change across the sense capacitor. Issues concerning the design constraints were also addressed. The basis for choosing the geometry of the inverter transistors was identified as the need for high gain, low operating current and maximizing the area coverage for the sense capacitors. A dummy transistor with source and drain terminals connected together was employed as a cancelling technique for the clock feedthrough problem. This dummy transistor was connected to the floating node of the sense capacitor. Simulation results were presented to show the validity of the feedthrough cancelling technique. The effect of an alpha strike on the sense capacitor was modeled using a voltage source in series with the sense capacitor, with a ΔV_{in} specified as -0.16 V. Finally, a schematic for the design of an alpha particle detector was presented in chapter one, with the supporting simulation results.

Chapter 4 dealt with issues concerning the layout of the proposed detector schematic. It was shown that the detector design can be implemented CMOS4S, BATMOS and MITEL1.5 technologies. Thus, a digital process with no analog components can be employed for implementing the detector. Interconnect parasitics can contribute towards the clock feedthrough problem. Therefore, better routing of the interconnects, for reducing the interconnect parasitics, and subsequent compaction in the layout of the transistors was obtained by sharing a common diffusion layer for source and drain ends of the PMOS transistor in the inverter with those of the switch and dummy transistors.

Chapter 5 dealt with the testing of the chips that were fabricated. The measured results were slightly in disagreement with the predicted ones. The cause for disagreement was

attributed to the possibility of an increased effective sense area. The results however, were in agreement with the inverse square law, implying that the susceptibility to noise and interference was negligible. The difference in the measured counts between various chips was attributed to the variation in sensitivity due to variations in the leakage currents and gain of the inverter. *From the analyses of the measured results, the principle of alpha particle detection with an integrated circuit has been verified.*

6.2 Recommendation for Future Work

The test results show the validity of the principle for developing a prototype for an Integrated Alpha Particle Detector. There are some areas that need to be addressed in order to develop a prototype for the detector.

The designs during the second phase of submissions were laidout with provisions for observing the bias point of the analog inverter, along with on chip analog buffers at the input and output nodes, to find out the amount by which the potential at the input node changes due to one alpha strike and the subsequent change at the output node. This would also give an estimate of the actual gain of the inverter. Further tests will be conducted on the second batch of the chips to get a better understanding of the above factors.

Furthermore, the results presented in chapter 4, are in agreement with the theory within the statistical variation, but the measurements were only performed for a time duration of 90 minutes. Longer duration of measurements would refine the errors and the

data would be more accurate to make a comparison with the predicted count rate.

Although the initial design took a pessimistic approach and concentrated on maximizing the sensitivity, analysis of the measured results shows that the size of the sense capacitor could also be increased considerably to maximize the sense area, since the sensitivity of the detector is very high. This would reduce the potential change at the input node, which is subsequently compensated by having high sensitivity. Exploring the above possibility would give a better understanding on the sizing of the sense capacitor.

Further simulation work is also needed to develop a prototype for the detector, with an array of sense capacitors. The various possible designs, with an array of sense capacitors, that would serve the purpose of detection with large sense area are discussed below.

6.2.1 Design One

Figure 6-1 below, shows one of the possible designs that could be implemented with an array of sense capacitors. It is seen that the scheme below involves precharging all the capacitors simultaneously and sequentially reading the capacitors for alpha strikes. Extensive simulation work is required in exploring the effect of the interconnect capacitance between each capacitor and the input node of the inverter amplifier. This interconnect capacitance would lower the effective change in the potential at the input node. Also whether there is a need for feedthrough cancelling transistor at each access transistor or whether a single transistor could perform the required feedthrough cancellation is another factor to be explored. A decoder would also be required to provide

a suitable clocking scheme. Work will be continued in exploring the above issues.

Issues such as lowering the operating current are also to be addressed. If the detector is powered by a battery then the operating current would have to be lowered so that the battery can supply the required current for a sufficient period of time before it has to be replaced. This would imply that the length of the inverter transistors has to be increased which would subsequently decrease the gain. To achieve the same amount of ΔV_{out} it would require an increase in the transistor widths. Ultimately, the area for the transistors would be increased. The above issues can be explored using Figure 4-8 in section 4.3.3.

Figure 6-1: Possible detector design with an array of sense capacitor, with an access transistor for each capacitor.

6.2.2 Design Two

A better scheme for reducing the current consumption is by having the amplifier disconnected from the power supply after precharge and reconnecting it before sensing.

This scheme implies that current would be consumed for a very short duration of time. The sense capacitor is expected to hold the charge for the time interval within which the inverter amplifier is reconnected to it. Whether there will be any extra clock feedthrough due to the inverter being reconnected is an issue to be addressed. Should the inverter be precharged to the bias point before connecting it to the sense capacitor is another factor to be explored. Figure 5-2 below shows the possible configuration.

Transistor M_s could be used for disconnecting the inverter from the supply. Transistor M_a could be used for connecting/disconnecting the inverter with the sense capacitors. Both M_a and M_s will switch at the same time. The presence of M_s will produce a finite voltage drop, the effects of this will have to be explored.

The possibility of using the above scheme in order to reduce the current consumption has to be explored by performing extensive simulations.

of 20 μm , then charge may be distributed between the two capacitors. To avoid such risks, careful attention is needed in spacing the capacitors.

Using the minimum spacing allowed by the design rules in BATMOS the two sense capacitors with their respective guard rings would be 12.6 μm apart. Therefore an extra 8 μm spacing would avoid the risk of an alpha strike changing the potential across two sense capacitors simultaneously. As mentioned previously, if the capacitor size is increased by a factor of three, then the possibility of having a change inside the neighboring sense capacitor large enough to cause a corresponding change at the output would also be reduced.

Therefore, proper sizing and spacing of the sense capacitors would avoid the risk of such a problem.

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Appendix

Figure A-1: Layout in BATMOS of the tested detector chip with a digital buffer at the output and an uncommitted well to substrate depletion capacitance.

Figure A-2: BATMOS layout of the detector with analog buffer at the input and output node with an additional digital buffer at the output node. Also an uncommitted opamp

Figure A-3: Detector Layout in CMOS4S with a digital buffer at the output with an uncommitted well to substrate depletion capacitance.

Figure A-4: Detector Layout in CMOS4S with an analog buffer at the input, a digital buffer at the output nodes and a well to substrate depletion capacitance.

Figure A-5: Detector Layout in CMOS4S with analog buffers at the I/O with an uncommitted well to substrate depletion capacitance.