A Miniaturized Delay-Line Discriminator

by

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Abstract

This thesis presents the design of a miniaturized delay-line discriminator (DLD) array for electronic warfare (EW) applications. Over very wide bandwidths, delay-line discriminators can provide the high accuracy, low latency measurements desired in many EW systems. The drawback to these circuits is that they can be quite bulky due to the long time delays they require. To miniaturize the discriminator's delay line, the design employed a slow-wave transmission line that allowed for a length reduction of approximately 60 %. An array consisting of four discriminators with delay ratios of 1, 2, 4, and 16 was fabricated on a 4-layer printed circuit board. The design obtained a measurement range of over 2 GHz with better than 4 MHz RMS accuracy. Additional processing of the discriminators' outputs is required to further improve this accuracy. Measurements of pulses with phase and frequency modulation present have demonstrated the potential for the identification of these modulation schemes.

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Table of Contents

Abstract	ii
Acknowledgments	iii
Table of Contents	iv
List of Tables	vi
List of Figures	vii
Nomenclature	xiii
1 Introduction	1
1.1 The Evolving Electromagnetic Battle-space	1
1.2 Thesis Objectives	3
1.3 Thesis Contributions	3
1.4 Thesis Overview	4
2 Background	5
2.1 An Introduction to Radar	5
2.2 An Introduction to Radar EW	8
2.3 The Delay Line Discriminator	11
3 Delay Line Miniaturization	19
3.1 Metamaterials	19
3.2 Planar Slow-wave Structures	22
3.3 Delay-line Unit Cell	28
3.4 Conclusion	35

4	The Delay-Line Discriminator	37
4.1	Design Specification	37
4.2	The Phase Detector Block	39
4.3	The Delay Split Block	47
4.4	The Input Split	50
4.5	Delay-Line Discriminator Design	53
4.6	Discriminator Array	60
4.7	Conclusion	69
5	Conclusion	71
5.1	Future Work	72
	List of References	74
	Appendix A Radar Bands	79

List of Tables

1.1	Specifications for the delay-line discriminator array.	3
3.1	Comparison of parameters for the unit cells and native transmission lines.	36
4.1	Design parameters for the discriminator array	39
4.2	Comparison of the extracted $\Delta\tau$ values for the simulated and measured discriminator array. The deviation from the design value is in parentheses. A negative value indicates a delay line that is too long. .	65
4.3	Summary of the delay-line discriminator array's measured performance	70
5.1	Comparison of this work to other discriminators presented in the literature. Unless otherwise specified, frequency accuracy is expressed as an RMS value.	72
A.1	International Telecommunication Union (ITU) frequency allocation for radar bands [12, 68, 69]. Radar bands of interest (i.e. between 0.5–18 GHz) have been bolded.	79

List of Figures

1.1	The three categories of EW [2].	1
2.1	Basic block diagram of a radar system. The transmitted signal is shown in orange, and the reflected signal shown in blue [12].	6
2.2	General block diagram of an instantaneous frequency measurement (IFM) receiver [16]	11
2.3	Block diagram of the delay-line discriminator, which has been divided into four sub-circuits: the input split, the delay line, the delay split, and the phase detector.	12
2.4	Vector representation of simultaneous signals in the discriminator. Points A and B are the output vectors for each individual signal. Point C is the resultant output vector of the discriminator when both signals are present [22].	16
2.5	The effect of frequency spacing and relative amplitude on a discriminator's measurement error when simultaneous signals are present. It was assumed the desired signal had the larger amplitude [17].	17
3.1	Permittivity-permeability diagram outlining the five types of metamaterials: (I) double-positive, (II) ϵ -negative, (III) μ -negative, (IV) double-negative, and (O) zero index media at the origin [32].	20
3.2	The equivalent circuit for a metamaterial unit cell of length ℓ . The series capacitor and shunt inductor (shown in blue) realize negative permeabilities and permittivities. The series inductor and shunt capacitor (shown in red) realize positive permeabilities and permittivities. The resistive elements model the dielectric and conductor losses [29].	21

3.3	(a) A split-ring resonator (μ -negative) (b) A metal wire (ϵ -negative). (c) A complimentary split-ring resonator (ϵ -negative), which is the dual of (a). (d) A slot line (μ -negative), which is the dual of (b). [32] (e) The unit cell of the first double-negative metamaterial consisting of a split-ring resonator and metal wire [34].	22
3.4	Geometry of a metallic wire substrate. $h1$ and $h2$ are the heights of the insulating and host media. d is the via hole diameter, while p is the via hole spacing. The width of the microstrip transmission line is denoted by w [41].	24
3.5	Geometry of the slow-wave substrate integrated waveguide. $h1$ and $h2$ are the heights of the insulating and host media. d is the via hole diameter. p refers to the via spacing in the longitudinal direction, while p_1 is the spacing in the transverse direction. The width of the waveguide is denoted by W_{SIW} [52].	25
3.6	Geometry of the substrate integrated waveguide loaded by complimen- tary split-ring resonators (CSRR). The resonators are in a face-to-face configuration [55].	26
3.7	(a) Geometry of the co-planar cross-tie transmission line [56]. (b) Ge- ometry of the modified cross-tie structure to support microstrip trans- mission lines [58].	27
3.8	The two unit cell configurations. Both cells have a length (ℓ) of 1.27mm, a line width (W) of 100 μm , and twin radial stubs with angles (ψ) of 55° and 60° . (a)'s radial stubs have radii (R) of 0.79 mm. (b)'s radial stubs have radii of 0.71 mm. (b) also has a 0.2 mm x 1.14 mm cutout of the lower ground plane to enhance the line inductance. The cutout is shown in green.	28
3.9	The substrate used to realize the unit cells and delay-line discrimina- tors. The stackup has a height of approximately 1.45 mm and mainly consists of Rogers RO4350B dielectric material ($\epsilon_{r,dielectric} = 3.66$). The RO4350B core layers are held together by two 89 μm thick layers of Rogers RO4450F prepreg material ($\epsilon_{r,dielectric} = 3.52$). 0.5 oz. copper was used for all layers. An electroless nickel/immersion gold (ENIG) finish was used on the top and bottom metal layers.	29

3.10	Extracted values of characteristic impedance and refractive for the microstrip unit cell	31
3.11	Extracted group delay of the microstrip unit cell	32
3.12	Extracted values of characteristic impedance and refractive index for the stripline unit cell	33
3.13	Extracted group delay of the stripline unit cell	33
3.14	The two curves for meandering the delay line. Both curves are made up of three unit cells, one oriented vertically and the other two at 45° angles. All unit cells have lengths (ℓ) of 1.27mm, line widths (W) of $100\mu\text{m}$, and radial stubs subtended at an angle (ϕ) of 60° . (a) has radial stubs with radii (R) of 0.98 mm (vertical) and 0.95 mm (45° angle). (b) has radial stubs with radii of 0.89 mm (vertical) and 0.86 mm (45° angle). (b) also has 0.2 mm x 1.14 mm cutouts of the lower ground plane to enhance the line inductance. The cutouts are shown in green.	34
3.15	Extracted (a) characteristic impedance and dielectric constant, and (b) group delay for the microstrip curve.	35
3.16	Extracted (a) characteristic impedance and dielectric constant, and (b) group delay for the stripline curve.	35
4.1	The effect of the relative DC offset on the measured phase error, θ_ϵ . (a) Phase error with a relative DC offset of 0.1 on both of the I and Q outputs. (b) Peak phase error for varying DC offsets ($\nu_I = \nu_Q$). . . .	40
4.2	Simulated DC offset for an ideal mixer with varying LO-RF, LO-IF, and RF-IF port isolations.	41
4.3	Measured DC offset of an ML1-0110LSM mixer when the IF port is terminated with a wideband 50Ω match and with a low-pass filter . .	42
4.4	Simulated effect of RF power on peak phase error for the ML1-0110LSM.	44

4.5	Layout for phase detector block. <i>MX1</i> and <i>MX2</i> (ML1-0110LSM) are mixers from Marki Microwave. <i>FL1</i> and <i>FL2</i> each consist of two cascaded XLF-151+. A single OPA2846 realizes both <i>A1</i> and <i>A2</i> . <i>R1</i> , <i>R2</i> , <i>R4-R6</i> , and <i>R8</i> are $50\,\Omega$ resistors (FC0603E50R0BTBST1). <i>R3</i> and <i>R7</i> are $453\,\Omega$ resistors (ERJ-3EKF4530V). <i>C1</i> and <i>C2</i> are 100 nF decoupling capacitors (LLL185R71A104MA11L). <i>C3</i> is a 10 nF decoupling capacitor (LLL185R71E103MA11L). <i>J1</i> and <i>J2</i> are SMA connectors (901-10513-2). Traces in red are on the top layer (L1) of the PCB, while traces in blue are on the inner layer (L3).	45
4.6	Simulated voltage outputs of the phase detector block.	46
4.7	Simulated DC offset on the I and Q outputs of the phase detector block.	46
4.8	The effect of phase imbalance on the measured phase error, θ_ϵ . (a) Phase error with a phase imbalance of 5° . (b) Peak phase error for varying phase imbalances.	47
4.9	The effect of amplitude imbalance on the measured phase error, θ_ϵ . (a) Phase error with a amplitude imbalance of 1.0 dB. (b) Peak phase error for varying amplitude imbalances.	48
4.10	Coupling between the I and Q arms of the discriminator causing additional self-mixing [23].	49
4.11	Layout for delay split block. <i>PD2</i> is the Mini-Circuits power splitter GP2X+. Traces in red are on the top layer (L1) of the PCB.	49
4.12	(a) The insertion loss for the I and Q paths. (b) Phase imbalance between the I and Q paths.	50
4.13	Simulated group delay of the delay split block.	50
4.14	The effect of amplitude imbalance on the ML1-0110LSM mixer when it is present at the RF and LO ports.	51

4.15	Layout for input split block. <i>PD1</i> (GP2X+) and <i>HY1</i> (QCS-592+) are a power splitter and quadrature hybrid from Mini-Circuits. Amplifier <i>A1</i> (PMA3-83LN+) and attenuator <i>AT1</i> (YAT-6+) are also Mini-Circuit parts. The DC blocking capacitor <i>C1</i> (C04BL121X-5UN-X0T) is from Dielectric Laboratories. <i>C2</i> (GJM1555C1H100JB01D) and <i>C3</i> (LLL185R71E103MA11L) are 10 pF and 10 nF decoupling capacitors. Inductors <i>L1</i> (LQW18AN18NG00D) and <i>L2</i> (LQW18AN39NG00D) are 18 pH and 39 pH respectively. <i>R1</i> (FC0603E50R0BTBST1) is 50 Ω . Traces in red are on the top layer (L1) of the PCB.	52
4.16	(a) The insertion loss to the I, Q, and delayed paths. (b) The amplitude and phase imbalance between the I and Q paths.	53
4.17	Simulated group delays for the v_{DELI} , $v_{LO,I}$, and $v_{LO,Q}$ outputs of the input split block.	53
4.18	Layout of the 305 ps delay-line discriminator, including the input split, delay split, and phase detector blocks, as well as the 562 ps delay line.	55
4.19	EM simulation results for the 562 ps delay line: (a) Insertion and return losses, and (b) group delay.	55
4.20	Co-simulation results for the 305 ps delay-line discriminator: (a) I and Q output voltages, and (b) measured phase and phase error	55
4.21	Layout of the 610 ps delay-line discriminator, including the input split, delay split, and phase detector blocks, as well as the 867 ps delay line.	56
4.22	EM simulation results for the 867 ps delay line: (a) Insertion and return losses, and (b) group delay.	57
4.23	Co-simulation results for the 610 ps delay-line discriminator: (a) I and Q output voltages, and (b) measured phase and phase error	57
4.24	Layout of the 1.22 ns delay-line discriminator, including the input split, delay split, and phase detector blocks, as well as the 1.48 ns delay line.	58
4.25	EM simulation results for the 1.48 ns delay line: (a) Insertion and return losses, and (b) group delay.	58
4.26	Co-simulation results for the 1.22 ns delay-line discriminator: (a) I and Q output voltages, and (b) measured phase and phase error	58
4.27	Layout of the 4.88 ns delay-line discriminator, including the input split, delay split, and phase detector blocks, as well as the 5.14 ns delay line.	59

4.28	EM simulation results for the 5.14 ns delay line: (a) Insertion and return losses, and (b) group delay.	60
4.29	Co-simulation results for the 4.88 ns delay-line discriminator: (a) I and Q output voltages, and (b) measured phase and phase error	60
4.30	The top side of the printed circuit board implementing the delay-line discriminator array.	61
4.31	The bottom side of the printed circuit board implementing the delay-line discriminator array.	62
4.32	The test setups for measurements of the delay-line discriminator array.	63
4.33	Measured frequency-voltage characteristics of the fabricated discriminator array: (a) 305 ps DLD, (b) 610 ps DLD, (c) 1.22 ns DLD, (d) 4.88 ns DLD.	64
4.34	Extracted phase error from the fabricated discriminator array's frequency-voltage characteristic	65
4.35	Measured response of the fabricated discriminator array to a 100 ns pulse: (a) 305 ps DLD ($f_{in} = 4.1$ GHz), (b) 610 ps DLD ($f_{in} = 4.1$ GHz), (c) 1.22 ns DLD ($f_{in} = 3$ GHz), (d) 4.88 ns DLD ($f_{in} = 3$ GHz).	67
4.36	Measured response of the 4.88 ns discriminator to a phase modulated signal with a phase deviation of (a) 90° and (b) 180°	68
4.37	Measured response of the discriminator array to a pulse with linear frequency modulation.	68
4.38	Measured return loss of the discriminator array's RF input.	69

Nomenclature

ADC	Analog-to-digital converter
ADS	Advanced Design System
CW	Continuous wave
DC	Direct current
DLD	Delay-line discriminator
DRFM	Digital radio frequency memory
EA	Electronic attack
EM	Electromagnetic
ENIG	Electroless nickel/immersion gold
EP	Electronic protection
ES	Electronic warfare support
EW	Electronic warfare
FPGA	Field programmable gate array
IF	Intermediate frequency
IFM	Instantaneous frequency measurement
IREWTS	Integrated Radar EW Test Set
ITU	International Telecommunication Union
J/S	Jamming-to-signal ratio
LO	Local oscillator

NRI	Negative refractive index
OFDM	Orthogonal frequency division multiplexing
P1dB	1dB-compression point
PCB	Printed circuit board
PNT	Positioning, navigation, and timing
PRI	Pulse repetition interval
RCS	Radar cross section
RF	Radio frequency
RMS	Root-Mean Square
SDR	Software-defined radio
SF	Slowing factor
SIW	Substrate-integrated waveguide
SRR	Split-ring resonator
VNA	Vector network analyzer

Chapter 1

Introduction

1.1 The Evolving Electromagnetic Battle-space

Although it is not always something that is easy to see or hear, EW is critical to ensuring both the success of a military operation and the safety of the personnel involved. EW refers to military tactics that aim to control the electromagnetic (EM) spectrum and attack enemy forces through the use of EM or directed energy [1]. These tactics fall into the three categories shown in Figure 1.1 [2]. Electronic attack (EA) involves actions that use the spectrum to degrade the performance of, or even destroy, an adversary's assets. Electronic protection (EP) aims to protect one's own assets from adversarial and friendly EA activities. Electronic warfare support (ES) involves actions that search for, locate, and identify threats based on radiated EM energy [3]. The gathered intelligence supports decisions as to which EA and EP tactics would be most effective in an operating environment.

The EM spectrum has become a vital resource in military operations, as many of

Figure 1.1: The three categories of EW [2].

the systems that are relied upon to provide situational awareness and battlespace agility require continuous access to the spectrum. These systems include radar, communications, and positioning, navigation, and timing (PNT). Today's militaries are continuously developing new strategies and technologies to attain a 'degree of dominance in the EMS that permits the conduct of operations at a given time and place without prohibitive interference, while affecting an adversary's ability to do the same' [4, p. v]. There has been a recent push to improve EW capabilities among governments and militaries as they recognize the important role it plays in achieving the goal of spectrum superiority [5, 6].

Severe size and weight restrictions can be problematic in defense applications as aircraft, UAVs, and even ships can have limits on how much space equipment can take up. Furthermore, fuel budgets restrict the amount of weight that can be carried at a given time. Miniaturization is a topic of particular interest because the reduced size and better integration it enables can result in the same capabilities being delivered in smaller footprints. The freed up space could then be allocated to additional functionality that would otherwise be missing.

The rapid evolution of technology has provided the field of radar EW with a variety of new challenges. Advances in sampling technology have resulted in the ability to generate complex new waveforms that can decrease a radar's susceptibility to EA activities [7, 8]. In the past, radar systems had long development times and service lives, which meant that they were not frequently changing. EW engineers would gather intelligence on these radars, and then design a specific countermeasure to use against each threat. This methodology was viable since the tactic that was developed would still be effective years from now. The adoption of reconfigurable digital technologies in radar, such as the field programmable gate array (FPGA) and software-defined radios (SDRs), means that these systems are no longer static. The development and deployment of new waveforms and counter-countermeasures can occur much more rapidly, meaning intelligence gathered on a radar today could be outdated tomorrow. Real-time adaptability has recently been demonstrated in a radar that can optimize its waveform to avoid background clutter and EM interference within its environment [9]. In response to these developments, the field of EW has begun to explore the concepts of adaptive and cognitive EA. Tomorrow's EW system needs to be able to react in real-time to changes in a threat or the environment. It also should be able to discern when it's jamming is not effective and make appropriate adjustments,

thereby learning the optimum tactic to deploy in a given situation [10]. To support these new capabilities, EW receivers need to be able to operate instantaneously over larger frequency ranges so that agile and wideband radars can be continuously tracked and engaged.

Another challenge facing EW systems is a congested EM environment that includes friendly, adversarial, and civilian transmitters and receivers. Military platforms, such as aircraft and naval vessels, contain many different systems that require access to the spectrum [11]. If a radar jammer cannot accurately identify a threat and apply its jamming specifically against that signal, it can interfere with the other friendly systems and reduce their effectiveness. The surgical jamming capabilities needed to operate in a congested environment demand that EW systems be able to more accurately measure the characteristics of the threats they engage.

1.2 Thesis Objectives

The primary objective of this thesis is to develop a miniaturized DLD array for EW applications. The design has been performed in collaboration with MC Countermeasures Inc., and the discriminator array is to be incorporated into their adaptive radar jamming system called IREWTS. The specifications for the circuit were dictated by MC Countermeasures and are provided in Table 1.1.

Table 1.1: Specifications for the delay-line discriminator array.

Parameter	Specification
Frequency Range	3.5–6.5 GHz
Frequency Accuracy	1 MHz RMS
Pulse Width	100 ns to CW

1.3 Thesis Contributions

This research contributes a miniaturized delay line for DLD circuits. The delay line's structure supports slow-wave propagation, allowing for the same delay value to be realized in a smaller transmission line. The planar structure, which requires a single

signal layer and no blind or buried vias, can be easily and cost-effectively integrated into a multi-layer substrate, leveraging the additional layers to significantly reduce the overall circuit area. This work also provides an in-depth analysis of the major phase error contributors within a delay-line discriminator.

1.4 Thesis Overview

The remainder of this thesis presents the design of the miniaturized delay-line discriminator array. Chapter 2 provides a brief summary of radar and radar EW concepts. Operation of the IFM receiver and delay-line discriminator are covered in-depth. The background section ends with a review of delay-line discriminators that have been reported in the literature.

Chapter 3 presents the design of a unit cell to miniaturize the discriminator's delay line. The chapter begins with an overview of metamaterials, and then discusses planar structures from the literature that have demonstrated slow-wave propagation. Two versions of the unit cell were created, one in a microstrip configuration and the other in stripline. Simulations of both circuits were performed in ADS to extract the effective refractive index of the unit cells.

In Chapter 4, a detailed description of the DLD array's design is provided. The performance impacts of each sub-circuit are discussed. The final circuit was implemented on a printed circuit board (PCB) and consisted of an array of four discriminators operating from 3.5–6.5 GHz. The discriminators had delay ratios of 1, 2, 4, and 16. The fabricated circuit was measured to determine its frequency-voltage characteristic, as well as its response to fixed frequency and modulated pulses.

A summary of the thesis and some considerations for future work are given in Chapter 5.

Chapter 2

Background

This chapter provides a brief introduction to radar and radar EW, as well as a high-level description of a delay-line discriminator's operation. The first section discusses the basic functionality of a radar, its typical characteristics, and possible EP measures. This is followed by an overview of radar EW that includes the topics of noise jamming, deception jamming, and the IFM receiver. Some of the ways that a more capable EW receiver can help improve jamming effectiveness are also mentioned. The last section describes the operation of a delay-line discriminator and presents some of the designs that have been previously reported in the literature.

2.1 An Introduction to Radar

A radar is a system that uses EM energy to locate objects within an environment. A basic block diagram of a radar is shown in Figure 2.1 [12]. The transmitter (TX) generates high-powered RF pulses that are radiated in a specific direction by the antenna. Objects within the antenna's beamwidth will reflect the transmitted EM energy back towards the radar. The antenna picks up these returns, allowing for them to be detected by the receiver (RX). A signal processor uses the results from the receiver to extract information about the targets. The T/R device isolates TX and RX modules, protecting the receiver from the high-powered signals generated by the transmitter.

The main target parameters that a radar can measure are range, azimuth angle, elevation angle, and radial velocity [12]. Since the radar pulse travels at the speed of light, the range can simply be determined from the time between when a pulse

Figure 2.1: Basic block diagram of a radar system. The transmitted signal is shown in orange, and the reflected signal shown in blue [12].

was transmitted and when the reflected return was detected. Azimuth and elevation angle measurements are based on the direction of the antenna when the detections occurred. Due to the Doppler effect, any relative motion between the radar and the target will result in the reflected EM wave having a slight change in frequency. By measuring the size of this frequency shift, the radial velocity of the target can be extracted.

The power received by the radar is dependent on both the radar and the object reflecting the EM energy. It is expressed in the radar range equation below:

$$P_r = \frac{P_t G_t G_r \lambda^2 \sigma}{(4\pi)^3 R^4} \quad (2.1)$$

where

- P_t is the power transmitted by the radar
- G_t is the gain of the transmit antenna
- G_r is the gain of the receive antenna
- λ is the wavelength of the signal
- σ is the radar cross section (RCS) of the target
- R is the range to the target

RCS is a measure of how much energy a target will reflect back to the radar and it is typically expressed as an effective area. There will be a minimum signal-to-noise

ratio that the radar receiver needs to detect a return from a target. This minimum power level will limit maximum range that the radar can see. Due to the R^4 term in (2.1), improving the maximum detection range can take a significant increase in transmit power, antenna gains, or receiver sensitivity. To reach these high power levels required by military radars, the transmitter block will often use vacuum tube devices, such as klystrons and magnetrons. This can limit the fractional bandwidth of the transmitter to about twenty percent [12]. Regulations also limit the bandwidth that a radar can occupy, as specific frequency ranges have been designated for radar use. These frequency bands have been listed in Appendix A.

There are several key parameters that dictate the performance of the radar. The pulse width of its signal determines both the range resolution and minimum range that can be detected. Using shorter pulses allows the radar to have higher range accuracy and detect targets closer to itself. The drawback to these narrow pulses is that they contain less energy, making it harder for the receiver to detect the echoes from targets and limiting the radar's maximum range. There are also trade-offs when choosing a pulse repetition interval (PRI). A short PRI allows for more accurate velocity measurements, but at the cost of introducing ambiguities in the range measurement. Some radars will mitigate this by using a more complex waveform with multiple PRIs in a pattern to resolve the ambiguity [12]. Using phase or frequency modulated signals is one way that radars can improve their range accuracy without reducing the length of their pulses, thus maintaining the same transmitted power. This is known as pulse compression, and the range resolution becomes a function of the waveform's bandwidth instead of its pulse width [13].

Electronic protection is an integral aspect of radar design, as it helps mitigate the effects of jamming activities and clutter within an environment. Pulse compression is one type of EP. It reduces the signal-to-jamming ratio against noise jamming because the noise will not have the same modulation as the radar signal, and therefore will not receive any processing gain [13]. Frequency agility and diversity are other ways to reduce the effects of jamming, as the jammer will have to spread out its energy across a wider bandwidth or be able to quickly re-tune itself to follow the radar's frequency. Also, the RCS of large targets can change significantly with frequency, so using multiple frequencies lessens the likelihood of missing detections due to small echoes [13]. Side lobe blanking techniques are currently being used to protect against angle deception, where a jammer injects a strong signal into the radar antenna's side

lobe, making it think that there is a target in the direction of its antenna's main beam. Lastly, EP processing techniques, which include moving target indicators and constant false alarm rates, allow the radar to filter out echoes from unwanted clutter from an environment (e.g. the ground, trees, rain, and bodies of water) [7].

2.2 An Introduction to Radar EW

There are two main types of active radar EW: noise jamming and deception jamming. Noise jamming involves transmitting a signal that has similar characteristics to the internal noise of the victim radar's receiver. This signal raises the radar receiver's noise floor, reducing the probability of it detecting targets. In deception jamming, copies of the radar's signal are played back to generate false targets, which the radar can track instead of real targets [3]. A more detailed discussion of these jamming techniques is provided later in this section.

One of the most important parameters in radar EW is the jamming-to-signal ratio (J/S), which represents the power in the jamming signal relative to the power in the target echo at the input to the victim radar's receiver [3]. The ratio can be expressed as follows:

$$\frac{J}{S} = \frac{4\pi P_j G_j R^2}{P_t G_t \sigma} \quad (2.2)$$

where

- P_j is the power transmitted by the jammer
- G_j is the gain of the jammer's antenna
- R is the range between the radar and the jammer/target
- P_t is the power transmitted by the radar
- G_t is the gain of the radar's transmit antenna
- σ is the RCS of the target

The R^2 term in the numerator is due to the fact that the radar's echo experiences two-way path loss, while the jamming signal only experiences one-way path loss. The result of this is that higher J/S ratios will occur when the jammer is further away from the radar. All radar countermeasures have a minimum jamming-to-signal ratio that

needs to be reached to be effective. This value is a function of the countermeasure itself, the radar being jammed, and the operating environment. Tactics with lower minimum jamming-to-signal ratios will be able to maintain effectiveness at closer ranges to the radar and also potentially allow the jammer to use a lower power transmitter, reducing its size, weight, and power consumption.

Noise Jamming

Noise jamming techniques will typically either fall into the categories of spot, barrage, or swept jamming. In spot jamming, the jammer will put all of its power into a small frequency range that matches the bandwidth of the victim radar's receiver. This can be ineffective against frequency agile radars, as they will simply switch their operating frequency to one that does not have the interference present. In these cases barrage and swept noise can be used instead. Barrage jamming averages the jammer's noise power over a wide bandwidth, ensuring there is always some jamming signal present at each the frequency in the band. Swept noise averages the noise power over time, hitting each frequency with a large burst of power for a brief period of each sweep [13].

The drawbacks to barrage and swept jamming are that the average noise power seen by the victim radar will be reduced, resulting in a lower jamming-to-signal ratio. Another method to counteract frequency agility is to use set-on-receive techniques, where the EW receiver re-tunes the jammer if it detects that the radar has changed its RF. The latency of the frequency measurement must be very short because the radar will be able to acquire a track on the target if it takes too long for the jammer to re-tune itself. Once a track has been established it can be more difficult, and require higher J/S ratios, to effectively jam a radar [14]. A more accurate frequency measurement can help improve the J/S ratio by allowing the noise energy to be more efficiently allocated into the radar receiver's bandwidth. If the measurement accuracy is reduced, the jamming signal has to be spread over a wider bandwidth to account for the potential measurement errors.

Deception Jamming

There are a wide variety of deception techniques, but in general they aim to hide a real target among false targets so that the radar will not track the real one. Modern deception jammers use a digital radio frequency memory (DRFM) to record and

playback the radar's own pulses. Deception jamming can introduce range, velocity, and angle errors into the radar's measurements [13]. It is the role of the EW receiver to decide whether a measured pulse belongs to the victim radar or to other systems operating in the EM environment. The receiver will trigger the DRFM to record, store, and playback the pulse if it was identified as being from the threat to be jammed. The pulse de-interleaving and identification algorithms [15] in the EW receiver require fast, accurate measurements to be able to operate on a pulse-by-pulse basis.

The IFM Receiver

The IFM receiver is popular in EW because it has many of the characteristics desired in these types of applications. The receiver's architecture allows it to make the low-latency measurements needed to adapt quickly to changes in a radar. High measurement accuracy can be maintained both over wide bandwidths and on narrow pulses. A block diagram of a typical IFM receiver is shown in Figure 2.2 [16]. The core frequency measurement element of an IFM receiver is the delay line discriminator, which provides voltage outputs that are a function of the input signal's frequency. The voltages are digitized by analog-to-digital converters (ADCs) so that they can be further processed. An array of parallel discriminators may be required in some applications to overcome the design trade-off between unambiguous bandwidth and accuracy of the frequency measurement [17]. The limiting amplifier at the RF input of the IFM receiver is a high-gain, multi-staged amplifier that produces approximately the same output power for all input amplitudes within its dynamic range. This desensitizes the discriminator voltage outputs from amplitude changes in the input signal [16]. The limiting amplifier should be designed to be low noise, as its high gain will make it the dominant component in the receiver's noise figure [18]. Limiting amplifiers can also provide a video signal that represents the envelope of the pulse. This allows the IFM to make amplitude measurements over a wide dynamic range. The logarithmic transfer characteristic of the limiting amplifier results in the peak voltage of the video signal being proportional to the input amplitude in dBm [19]. The IFM's digital processor uses the frequency and amplitude data to generate pulse descriptor words containing information such as frequency, peak amplitude, pulse width, PRI, and intra-pulse modulation [16].

The main drawback to the IFM receiver is that it can only measure one signal

Figure 2.2: General block diagram of an IFM receiver [16]

at a time. The presence of simultaneous signals can introduce large errors in its measurements. To mitigate these errors in high-density environments, some frequency selectivity may be required. This can be accomplished by using a hybrid receiver architecture, such as a channelized IFM or a heterodyned IFM [16]. The amount of error caused by the simultaneous signals will also be dependent on their relative amplitudes [17]. The capture effect in the IFM's limiting amplifier can help improve measurement accuracy when two signals overlap by suppressing the lower amplitude one by up to 6 dB [16]. Although these techniques can improve measurement accuracy in dense signal environments, they still do not remove the restriction that only one signal at a time can be processed. The interferer cannot be measured because it will be either suppressed or filtered out.

Another issue with the IFM receiver is that their size can be quite large. Arrays with more than seven DLDs have been designed [20] and bulky cable assemblies may be required to achieve the delays in those discriminators [17]. The fact that the delay line is the biggest component in the discriminator makes it a good candidate for the application of miniaturization techniques.

2.3 The Delay Line Discriminator

Delay-line discriminators allow for the direct and near instantaneous conversion of a signal's frequency to a DC voltage. It operates by comparing the phase of an input signal to a delayed version of that signal. Figure 2.3 provides a detailed block

Figure 2.3: Block diagram of the delay-line discriminator, which has been divided into four sub-circuits: the input split, the delay line, the delay split, and the phase detector.

diagram of the circuit. For ease of design, the discriminator has been divided up into four sub-circuits.

The input split block generates three outputs: the signal to be delayed, the in-phase (I) LO, and the quadrature (Q) LO. $PD1$ is a power divider and produces the signal to be delayed. The LO signals require a 90° phase shift between them, which is introduced by the hybrid coupler $HY1$. Amplifier $A1$ ensures that the LO ports of the mixers are driven with an appropriate power level. The delay line introduces a time delay that will result in a frequency dependent phase difference between the signals at the RF and LO ports of the mixers. The two voltages driving the RF ports are generated $PD2$ in the delay split block. The phase detector contains two mixers, $MX1$ and $MX2$, to perform the phase comparisons for the I and Q arms of the discriminator. Low-pass filters $FL1$ and $FL2$ remove undesired high frequency components from the mixer outputs, leaving a DC signal that is then amplified by $A2$ and $A3$. The two quadrature voltages, V_I and V_Q , form a vector representation of the input signal. Its amplitude and frequency can be extracted directly from the vector's magnitude and phase.

Basic Operation

Suppose the sinusoidal waveform $v_{in}(t)$ is applied to the input of the discriminator. The amplitude and phase modulation, $A(t)$ and $\phi(t)$, which may be present in the signal will be considered to be changing slowly relative to the time delays in the delay-line discriminator.

$$v_{in}(t) = A(t) \cos(\omega t + \phi(t)) \quad (2.3)$$

All of the components between the input and the LO and RF ports of the mixer will introduce a gain or loss to the signal, as well as a time delay. The LO and RF voltages can be represented by the following expressions:

$$v_{LO,I} = \alpha_{LO} \cos(\omega t - \omega\tau_{PD1} - \omega\tau_{A1} - \omega\tau_{HY1} + \phi_0) \quad (2.4)$$

$$v_{LO,Q} = \alpha_{LO} \sin(\omega t - \omega\tau_{PD1} - \omega\tau_{A1} - \omega\tau_{HY1} + \phi_0) \quad (2.5)$$

$$v_{RF,I} = \alpha_{RF} \cos(\omega t - \omega\tau_{PD1} - \omega\tau - \omega\tau_{PD2} + \phi_0) \quad (2.6)$$

$$v_{RF,Q} = \alpha_{RF} \sin(\omega t - \omega\tau_{PD1} - \omega\tau - \omega\tau_{PD2} + \phi_0) \quad (2.7)$$

The α terms account for the signal amplitude $A(t)$ and any component gains/losses. The mixers multiply the LO and RF signals together to produce sum and difference frequency components at 2ω and DC. Depending on their implementation, the mixers can also introduce a small time delay difference, $\Delta\tau_{mix}$ [21]. The 2ω term is removed by the low-pass filters, leaving only a DC voltage at the output that is a sinusoidal function of the input frequency.

$$V_I = \alpha \cos(\omega\Delta\tau) \quad (2.8)$$

$$V_Q = \alpha \sin(\omega\Delta\tau) \quad (2.9)$$

$$\Delta\tau = \tau + \tau_{PD2} - \tau_{A1} - \tau_{HY1} - \Delta\tau_{mix} \quad (2.10)$$

The instantaneous frequency of the input signal can then be determined by extracting the phase of the vector formed by V_I and V_Q .

$$\theta = \arctan\left(\frac{V_Q}{V_I}\right) = \omega\Delta\tau \quad (2.11)$$

If a four-quadrant arc tangent is performed in (2.11), the frequency measurement will be $2\pi/\Delta\tau$ periodic. Therefore, the range of frequencies for which the discriminator will provide an unambiguous reading is given by

$$\omega_{UA} = \frac{2\pi}{\Delta\tau} \quad (2.12)$$

The effect of $\Delta\tau$ on the resolution of the delay-line discriminator can be seen by differentiating (2.11).

$$\partial\theta = \partial\omega\Delta\tau \quad (2.13)$$

From (2.13) it can be seen that for larger values of $\Delta\tau$, smaller frequency deviations will result in the same change in phase, θ . This means that longer delay lines produce a higher frequency resolution. $\Delta\tau$ is the main design parameter for a discriminator as it dictates both the unambiguous range and the frequency resolution [17]. For pulsed signals, the minimum pulse width that can be detected will be determined by the discriminator's delay and the bandwidth of filters *FL1* and *FL2* [17]. This minimum pulse width can be expressed as

$$PW_{min} = \Delta\tau + \frac{1}{2.5B_V} \quad (2.14)$$

where

- PW_{min} is the minimum pulse width detectable by the delay-line discriminator
- B_V is the bandwidth of the baseband filters.

The Discriminator Array

In the case where both a high resolution and unambiguous bandwidth are required, an array of parallel discriminators can be used. The discriminator with the shortest delay line will define the unambiguous measurement range and resolve the ambiguities in the discriminators with longer delay lines, which realize the desired resolution. All values of $\Delta\tau$ should be integer multiples of each other. This mechanism works similarly to a clock, where a wider range measurement (i.e. the hour hand) resolves the ambiguities in a higher resolution measurement (i.e. the minute hand). The number of ambiguities that can be resolved by a pair of discriminators is dependent on the accuracy to which the phase, θ , can be measured [17]. The relationship between the measured phases

of two delay-line discriminators whose delays are related by an integer ratio of $p : n$ ($p < n$ and $(p, n) = 1$) can be found using (2.11). Since only phases between 0 and 2π can be measured, a $2\pi N$ term has been added to unwrap the measured phase.

$$\frac{\theta_p + 2\pi N_p}{\theta_n + 2\pi N_n} = \frac{p\omega\tau}{n\omega\tau}$$

$$n\theta_p + 2\pi nN_p = p\theta_n + 2\pi pN_n \quad (2.15)$$

Errors in the measured phase of either discriminator may cause ambiguity resolution to fail, which can result in the measured frequency deviating significantly from the actual value. The phase errors can be due to noise, component mismatches, or simultaneous signals being present. Assuming the worst case conditions, where the phase errors from the two discriminators are of opposite sign, an upper limit can be placed on the phase error such that the ambiguity resolution will not fail [17]. For noise and component mismatches the errors in the discriminators should be of comparable magnitude, which allows (2.16) to be simplified to (2.17).

$$|n\theta_{p,\epsilon} + p\theta_{n,\epsilon}| < \pi \quad (2.16)$$

$$\therefore |\theta_\epsilon| < \frac{\pi}{p+n} \quad (2.17)$$

Effects of Simultaneous Signals

As mentioned in Sec. 2.2, simultaneous signals can cause large measurement errors in the discriminator. The presence of a secondary interferer modifies the output vector of the discriminator as shown in Figure 2.4 [22]. When only a single signal is present at its input, the discriminator will measure either vector **A** or vector **B**. When both signals are present the amplitude and phase of the discriminator's output are modified, resulting in vector **C**. Assuming that **A** is the desired signal and ambiguity resolution does not fail, the measured frequency error will be a function of the longest delay line length and the angle between vectors **A** and **C**, θ_ϵ . It should be noted that absolute phase is not preserved in the resultant vector, which means that the measured θ values in the discriminator array will not necessarily maintain the delay line ratios when simultaneous signals are present [17]. Ambiguity resolution will fail if the phase error between discriminators exceeds the limit from (2.16).

Figure 2.4: Vector representation of simultaneous signals in the discriminator. Points **A** and **B** are the output vectors for each individual signal. Point **C** is the resultant output vector of the discriminator when both signals are present [22].

The phase errors from simultaneous signals are dependent on both the relative amplitudes of the two signals, and the frequency difference between them [17]. Because multiple tones will be present at the mixer, intermodulation products will be generated. The resultant phase error must be treated differently depending on whether the intermodulation products fall within or outside of *FL1* and *FL2*'s bandwidth. If the intermodulation products are filtered out by *FL1* and *FL2*, the peak phase error can be expressed as

$$\theta_{\epsilon} = \arcsin(P_B/P_A) \quad (2.18)$$

- P_A is the power in the desired (i.e. larger) signal
- P_B is the power in the interfering (i.e. smaller) signal

When the intermodulation products fall within the filter bandwidths, the phase error changes with time. The worst-case error can be expressed as [17]

$$\theta_{\epsilon} = 2 \arcsin(P_B/P_A)^{1/2} \quad (2.19)$$

Figure 2.5: The effect of frequency spacing and relative amplitude on a discriminator’s measurement error when simultaneous signals are present. It was assumed the desired signal had the larger amplitude [17].

The phase error for both cases has been plotted in Figure 2.5. For a discriminator array with binary ratios, signals spaced far apart in frequency can have almost equal amplitudes before ambiguity resolution fails; However, if the frequencies are closely spaced, ambiguity resolution can fail even if the interferer has one-fifth the power of the desired signal. The IFM’s limiting amplifier should improve tolerance to simultaneous signals because it can suppress the interferer by up to 6 dB.

A Review of the Literature

Several delay-line discriminator designs have been reported in the literature. In [23] the designs of two discriminator arrays, one from 2–6 GHz and the other from 6–18 GHz, were presented. Each array had four discriminators with ratios of 1, 4, 16, and 64. The author developed a method of compensating the measured phase to account for the mixer’s DC offset. This phase sector compensation achieved a 9% improvement in measurement accuracy. The reported RMS phase error for the two discriminators was 4.23° (2–6 GHz) and 4.81° (6–18 GHz). This corresponded to an RMS frequency accuracy of 0.95 MHz and 1.49 MHz. A discriminator array that can resolve two simultaneous signals has also been reported [24]. Two of the discriminators in the array were related by delay line ratios of 1 : 2, while the other had no delay. A modified version of Prony’s method was employed to extract the frequencies of

the two overlapping signals. The measured results showed good accuracy for signals whose frequency difference was greater than 300 MHz. The discriminator operated over a frequency range of 2–4 GHz.

The possibility of using metamaterials to miniaturize the delay line of the discriminator has also been explored [25]. The author proposed a novel circuit configuration that utilized a double-negative transmission line. The discriminator operated between 50–150 MHz and demonstrated a voltage characteristic that has the opposite slope of conventional discriminators.

A purely digital alternative to the delay-line discriminator is another area of interest. An FPGA-based IFM receiver has realized a fully digital discriminator capable of making frequency measurements over 1.2 GHz with ± 2 MHz of accuracy [26]. The design could handle pulses as narrow as 100 ns. The work in [27] improved on the digital IFM design by incorporating a more advanced pulse detection algorithm. Better alignment with the pulse allowed for optimum timing of the frequency measurement, resulting in readings as accurate as 43 kHz on 50 ns pulses. This type of processing would also be applicable to IFM receivers with analog DLDs. Digital frequency counting could provide another method of frequency measurement for IFM receivers [28]. Instead of comparing phases or using digital correlators, this type of circuit counts number of cycles of the input signal that occur over a period of time and compares it to the number of cycles of a reference clock. The resolution of the measurement is determined by the clock frequency and measurement time. Over a 1 GHz instantaneous bandwidth, the prototype in [28] was able to measure pulses as short as 300 ns with a resolution of 400 kHz.

Chapter 3

Delay Line Miniaturization

One of the key components of a delay-line discriminator is the delay line. In some cases these delay lines need to be quite long, which can consume significant circuit area or even require an external solution, such as a cable assembly [17]. Miniaturization of the delay line is possible by creating a structure in which an electromagnetic wave will propagate at a slower velocity, allowing the same time delay to be realized in a shorter length of transmission line. This structure would therefore have a higher effective permittivity and/or permeability. The growing field of metamaterials has enabled the design of materials with almost any value of permeability or permittivity. Employing these or similar techniques can allow for better integration of the delay line with the rest of the delay-line discriminator, shrinking the overall circuit footprint. Planar structures are of particular interest in this design, as the full discriminator array was to be implemented on a printed circuit board.

This chapter presents the design of a unit cell to miniaturize a delay line, beginning with a brief overview of metamaterials. This is followed by a review of planar slow-wave structures that have been demonstrated in the literature. Unit cells for both microstrip and stripline topologies were developed and simulated using Keysight's Advanced Design System (ADS). These cells were able to be stacked within the printed circuit board, allowing for vertical integration and a further reduced circuit footprint.

3.1 Metamaterials

Electromagnetic metamaterials are a type of engineered material that allow for a specific permittivity and permeability to be realized. Typically metamaterials are

Figure 3.1: Permittivity-permeability diagram outlining the five types of metamaterials: (I) double-positive, (II) ϵ -negative, (III) μ -negative, (IV) double-negative, and (O) zero index media at the origin [32].

made up of metalized elements that are repeated in one, two, or three dimensions to create a periodic structure [29]. The elements, or unit cells, should be sized such that they are smaller than one tenth of the guided wavelength for all frequencies within the band of operation. As long as this condition is met, the structure will look like a uniform material to the applied EM signal and can be represented as an effective permittivity and permeability [30,31]. The effective properties of the metamaterial can be engineered to be almost any value. This includes small and negative values, which are not readily available in nature. The characteristics of metamaterials fall into five categories: double-positive, ϵ -negative, μ -negative, double-negative, and zero-index. These classifications are depicted in Figure 3.1 [32]. Only double-positive and double-negative metamaterials support a propagating wave. The singly-negative materials result in an attenuated wave.

In a similar manner to transmission lines, metamaterials can be represented by an

Figure 3.2: The equivalent circuit for a metamaterial unit cell of length ℓ . The series capacitor and shunt inductor (shown in blue) realize negative permeabilities and permittivities. The series inductor and shunt capacitor (shown in red) realize positive permeabilities and permittivities. The resistive elements model the dielectric and conductor losses [29].

equivalent circuit consisting of distributed impedances and admittances. The lumped element representation is shown in Figure 3.2 [29]. A shunt inductance is needed to achieve a negative permeability, while a negative permittivity is realized with a series capacitance. The series inductor and shunt capacitor produce positive permeabilities and permittivities.

Double-negative metamaterials were first theorized by Veselago in 1968 [33], but a practical implementation was not developed until 2001 with the work by Smith et. al. [34]. Their unit cell paired a metal strip, to generate a negative permittivity, with a split-ring resonator, which produces a negative permeability. These elements, along with their duals, are shown in Figure 3.3. Double-negative metamaterials support backward-wave propagation, where the group and phase velocities are in opposite directions. This gives them the property of having a negative refractive index (NRI) [35]. Because of the resonant nature of the split-ring resonator, NRI materials are dispersive and narrowband, only exhibiting their negative permeability in the region just after resonance [29]. Due to their unique properties, double-negative structures are the main focus of metamaterial research. Some of the more exciting applications of these materials include invisibility cloaks and the Veselago-Pendry superlens, which enables imaging beyond refraction limits [31]. At microwave frequencies, double-negative metamaterials have been applied to a variety of resonant circuits [29, 32]. This includes a new leaky-wave antenna that is scanned by changing the applied

Figure 3.3: (a) A split-ring resonator (μ -negative) (b) A metal wire (ϵ -negative). (c) A complimentary split-ring resonator (ϵ -negative), which is the dual of (a). (d) A slot line (μ -negative), which is the dual of (b). [32] (e) The unit cell of the first double-negative metamaterial consisting of a split-ring resonator and metal wire [34].

signal's frequency [36].

The concept of double-positive metamaterials originated with the work on artificial dielectrics by Kock [37]. Kock designed microwave lenses consisting of a lattice of small conductors that created dipoles when in the presence of an electric field. This resulted in an increased effective permittivity. One of the issues with the metallic spheres that Kock used in his lattice is that the effective permeability decreases, limiting the overall refractive index [38]. More recent works on double-positive metamaterials have mitigated this effect by using a structure that does not significantly reduce the material's effective permeability. These designs include the dogbone/dumbbell particles from [39] and [40], as well as the metallic wire substrates from [41–45].

3.2 Planar Slow-wave Structures

Both double-positive and double-negative metamaterials can support slow-wave propagation, which occurs when the phase velocity of an electromagnetic wave is slower

within a structure than in the host medium [46]. In the case where the conducting elements are separated by air, slow-wave propagation will occur if the magnitude of the effective refractive index is greater than unity [30]. The slowing factor (SF) of a structure represents how much it reduces the phase velocity of an EM wave and can be expressed as a ratio of refractive indexes.

$$SF = \frac{n_{eff}}{n_{host}} \approx \frac{n_{eff}}{\sqrt{\epsilon_{r,host}}} \quad (3.1)$$

where

- n_{eff} is the effective refractive index of the metamaterial
- n_{host} is the refractive index of the material containing the structure
- $\epsilon_{r,host}$ is the effective dielectric constant of the material containing the structure

The approximation in (3.1) that uses the host material's dielectric constant arises from the fact that most non-magnetic materials have a relative permeability of approximately one [47].

Slow-wave propagation is desirable in the discriminator's delay line, since a slower propagating velocity will result in a shorter circuit length to achieve the same time delay. The following sections discuss some of the miniaturization methods that have been demonstrated in the literature and can be applied to a printed circuit board.

Metallic Wire Substrates

Metallic wire substrates are one method of implementing a double-positive structure in a planar configuration. Microstrip circuits at RF and microwave frequencies have been demonstrated on printed circuit boards using this technique [41–44]. For millimeter-wave applications, microstrip lines on a metallic-nanowire-filled membrane have also been presented [45]. The structure of the metallic wire substrate, which is shown in Figure 3.4, is made up of a dielectric material containing a two-dimensional array of via holes. The vias are connected together by the backing ground plane and are spaced such that the distance between them is much smaller than the guided wavelength [41]. As noted in Sec. 3.1, this small spacing is required for the structure to appear as a homogeneous material to the impinging EM wave [31]. An insulating

Figure 3.4: Geometry of a metallic wire substrate. $h1$ and $h2$ are the heights of the insulating and host media. d is the via hole diameter, while p is the via hole spacing. The width of the microstrip transmission line is denoted by w [41].

layer is placed between the substrate and the microstrip transmission lines to ensure that the line is not short-circuited to the vias [41].

The metallic wire substrate acts to enhance both the host material's permeability and permittivity [41]. The tops of the closely spaced vias appear as a ground plane to the transmission line, increasing the line's equivalent capacitance. This corresponds to an increase of the material's effective permittivity. When an EM wave is traveling along the transmission line, horizontal currents are generated in the microstrip trace, while vertical currents are generated in the vias. The magnetic flux densities produced by these two currents add in phase, resulting in a higher magnetic flux for the same current flowing along the transmission line. This means that the microstrip trace on the metallic wire substrate has a higher transmission line inductance, and therefore an increased effective permeability [44].

Fabricated circuits on metallic wire substrates have demonstrated both paraelectric and paramagnetic properties. Enhancement of the permittivity and permeability by factors of 2.2 and 1.7 have been reported [41]. A patch antenna realized on this structure achieved a 30 % size reduction in its resonant length [42]. A low-pass filter and branch-line coupler have also been demonstrated on this type of substrate [44]. These circuits had size reductions of 16 % and 33 %, respectively.

Figure 3.5: Geometry of the slow-wave substrate integrated waveguide. $h1$ and $h2$ are the heights of the insulating and host media. d is the via hole diameter. p refers to the via spacing in the longitudinal direction, while p_1 is the spacing in the transverse direction. The width of the waveguide is denoted by W_{SIW} [52].

Substrate Integrated Waveguides

Development of the substrate-integrated waveguide (SIW) was driven by the desire to integrate low-loss waveguides with planar circuits. An SIW closely resembles a rectangular waveguide, except that the sidewalls have been replaced by arrays of closely spaced vias [48–51]. The width of the SIW determines its cut-off frequency, which will be smaller than air-filled rectangular waveguides due to the dielectric constant of the substrate [50]. This makes substrate-integrated waveguides very attractive for microwave and millimeter wave applications, but limits its viability below 10 GHz due to the large dimensions required [52]. Half-mode [53] and folded [54] substrate-integrated waveguide structures have demonstrated the ability to reduce the width of the waveguides by up to one-third, but less attention has been paid to minimizing circuit length [52].

A substrate-integrated waveguide filled with a metallic wire substrate has demonstrated the ability to miniaturize both the width and length of SIW structures [52]. The geometry of the waveguide is shown in Figure 3.5 and adds a two-dimensional array of closely-spaced blind vias between the post walls. Like the previously discussed metallic wire substrates, these vias enhance the permittivity and permeability of the host material filling the waveguide. For the same cut-off frequency, the fabricated slow-wave SIW was able to achieve a 40 % width reduction relative to conventional SIW structures. The phase velocity within the waveguide was also reduced by 40 %, allowing for comparable reductions in circuit length [52].

Figure 3.6: Geometry of the substrate integrated waveguide loaded by complimentary split-ring resonators (CSRR). The resonators are in a face-to-face configuration [55].

Complimentary split ring resonators provide another potential miniaturization option for SIW structures. By loading an SIW with these resonators, it has been shown that it is possible to operate the waveguide well below its cut-off frequency [55]. In an unloaded waveguide, an evanescent wave will occur below its cut-off. This is due to the fact that the dielectric constant becomes negative, resulting in the waveguide acting as a ϵ -negative material [32]. When the SIW is loaded by complimentary split ring resonators, as shown in Figure 3.6, a forward-propagation region occurs below the cut-off frequency. This means that the ϵ -negative characteristic existing below the waveguide's cut-off has been reversed by adding an additional ϵ -negative structure [32]. The loaded SIW exhibits a bandpass response, and the orientation of the resonators determine the shape [55]. Enhancement of the SIW's permittivity by factors greater than 3 have been demonstrated [32]; however, the permeability also approaches zero in the pass-band, potentially limiting the possible circuit length reduction. The structure is also dispersive and has a narrow bandwidth due to the high Q-factor of the resonator.

Cross-Tie Transmission Lines

The cross-tie transmission line consists of a co-planar waveguide above a layer of periodic floating conductors [56,57]. Modifications of this structure have been made to utilize it with microstrip transmission lines by alternating grounded conducting strips

Figure 3.7: (a) Geometry of the co-planar cross-tie transmission line [56]. (b) Geometry of the modified cross-tie structure to support microstrip transmission lines [58].

at different heights [58]. These two configurations are shown in Figure 3.7. Cross-tie circuits achieve slow-wave propagation by alternating high and low-impedance sections. This spatially separates the storage of electric and magnetic energy if the section spacing is much less than the guided wavelength. The magnetic energy is mostly stored in the high-impedance section, while the electric energy is mostly held in the low-impedance section. The characteristic impedance of the resulting transmission line is the geometric mean of the two impedances, while the slowing factor is a function of their ratio [56]:

$$SF = \frac{\sqrt{Z_A/Z_B} + \sqrt{Z_B/Z_A}}{2} \quad (3.2)$$

where:

- Z_A is the characteristic impedance of the low impedance section
- Z_B is the characteristic impedance of the high impedance section

Large impedance ratios are required to achieve moderate slowing factor values.

Both the microstrip and co-planar cross-tie transmission lines can achieve high relative dielectric constants [56,58]. The dielectric constant of the cross-tie microstrip was approximately six times larger than conventional microstrip transmission lines. The length reduction resulting from this was only 61.6%, indicating that there is a decrease in permeability that opposes the increased permittivity [58].

Figure 3.8: The two unit cell configurations. Both cells have a length (ℓ) of 1.27mm, a line width (W) of 100 μm , and twin radial stubs with angles (ψ) of 55° and 60° . (a)'s radial stubs have radii (R) of 0.79 mm. (b)'s radial stubs have radii of 0.71 mm. (b) also has a 0.2 mm x 1.14 mm cutout of the lower ground plane to enhance the line inductance. The cutout is shown in green.

3.3 Delay-line Unit Cell

The delay line will be implemented using an artificial transmission line with a double-positive characteristic. A narrow, high-impedance trace was used realize $L_{\mu p}$ from the equivalent circuit in Figure 3.2. Butterfly stubs form the capacitor C_{ep} . The design targeted a slowing factor of 1.6 and a characteristic impedance of 50Ω . The unit cell was made 1.27 mm long. Both microstrip and stripline versions of the unit cell were realized in a four layer PCB using Rogers RO4350B dielectric material. The unit cells are shown in Figure 3.8, while the PCB substrate can be seen in Figure 3.9.

Figure 3.9: The substrate used to realize the unit cells and delay-line discriminators. The stackup has a height of approximately 1.45 mm and mainly consists of Rogers RO4350B dielectric material ($\epsilon_{r,die} = 3.66$). The RO4350B core layers are held together by two 89 μm thick layers of Rogers RO4450F prepreg material ($\epsilon_{r,die} = 3.52$). 0.5 oz. copper was used for all layers. An ENIG finish was used on the top and bottom metal layers.

The unit cell can be analyzed using the equivalent lumped element model from Figure 3.2. For a double-positive material, the circuit is in the form of a T-network and has a low-pass frequency response. Within its pass-band, the unit cell looks like it has an effective refractive index of n_{eff} . An impinging EM wave will have a propagation constant γ and see a characteristic impedance Z_0 when traveling through the structure. Both the equivalent circuit and effective transmission line representations can be expressed using an $ABCD$ matrix.

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh(\gamma\ell) & Z_0 \sinh(\gamma\ell) \\ Y_0 \sinh(\gamma\ell) & \cosh(\gamma\ell) \end{bmatrix} = \begin{bmatrix} 1 + ZY & 2Z + Z^2Y \\ Y & 1 + ZY \end{bmatrix} \quad (3.3)$$

$$\gamma = \alpha + j\beta \quad (3.4)$$

$$\beta = \frac{\omega}{c_0} n_{eff} \quad (3.5)$$

$$Z = \frac{1}{2}(R + j\omega L_{\mu p}) \quad (3.6)$$

$$Y = (G + j\omega C_{ep}) \quad (3.7)$$

Using the assumption of a lossless transmission line ($R = 0$ and $G = 0$), the matrices in (3.3) can be solved to express the values of $L_{\mu p}$ and $C_{\epsilon p}$ with respect to the desired impedance and propagation constant of the double-positive material.

$$L_{\mu p} = \frac{2Z_0}{\omega} \sqrt{\frac{1 - \cos(\beta\ell)}{1 + \cos(\beta\ell)}} \quad (3.8)$$

$$C_{\epsilon p} = \frac{2(1 - \cos(\beta\ell))}{\omega^2 L} \quad (3.9)$$

The cutoff frequency of the low-pass response is found by equating the two expressions for A in (3.3).

$$\begin{aligned} \cosh(\gamma\ell) &= 1 + ZY \\ \cosh(\alpha\ell) \cos(\beta\ell) + j \sinh(\alpha\ell) \sin(\beta\ell) &= 1 - \frac{1}{2}\omega^2 L_{\mu p} C_{\epsilon p} \end{aligned} \quad (3.10)$$

Two cases arise from (3.10) because the right-hand side of the equation is purely real. The first condition is a propagating wave ($\alpha = 0$, $\beta \neq 0$), while the second condition results in an evanescent wave that does not propagate ($\alpha \neq 0$, $\beta = 0$) [46]. For the propagating case, the value of β is only defined when the magnitude of the right-hand side of the equation is less than or equal to one. Solving this identity results in the following restriction on ω .

$$\begin{aligned} 0 \leq \omega &\leq \sqrt{\frac{2}{L_{\mu p} C_{\epsilon p}}} \\ \therefore f_c &= \frac{1}{\pi \sqrt{L_{\mu p} C_{\epsilon p}}} \end{aligned} \quad (3.11)$$

Each unit cell configuration must ensure that its cut-off frequency, f_c , is much higher than its frequency of operation.

Microstrip Unit Cell

To achieve the slowing factor of 1.6, an n_{eff} of 2.77 was selected for the microstrip configuration. For this refractive index, the unit cell needed to have an inductance of 601 pH and capacitance of 229 fF. The inductance value was realized using a 1.27 mm long trace with a width of 100 μm . A butterfly stub with radius 0.79 mm and angle

Figure 3.10: Extracted values of characteristic impedance and refractive for the microstrip unit cell

of 55° formed the 229 fF capacitor. With these values, the cut-off frequency of the unit cell is close to 27.0 GHz, far higher than the required frequencies of operation.

The structure in Figure 3.8a was analyzed using the ADS Momentum simulator. The extracted S-parameters were converted to an $ABCD$ matrix, and the values of Z_0 and ϵ_{eff} were calculated using equations (3.3)-(3.5) (see Figure 3.10). The results show the unit cell has a characteristic impedance of $50\ \Omega$ and a refractive index of 2.79. This corresponds to a slowing factor of 1.61. At 6.0 GHz, which is the highest frequency of interest, the guided wavelength within the structure is 17.9 mm, more than ten times the length of the unit cell.

The simulated group delay of the unit cell is shown in Figure 3.11. A $50\ \Omega$ microstrip trace on the PCB would have a delay of 5.8 ps/mm. To produce the same delay as the unit cell, the microstrip line would need to be 2.04 mm long. The unit cell has resulted in a 62 % reduction in length.

Figure 3.11: Extracted group delay of the microstrip unit cell

Stripline Unit Cell

To achieve the slowing factor of 1.6, an n_{eff} of 3.07 was selected for the stripline configuration. For this refractive index, the unit cell needed to have an inductance of 661 pH and capacitance of 249 fF. The minimum trace width in the process was 100 μm , which could not achieve the required inductance with a 1.27 mm long trace. A 0.2 mm x 1.14 mm cut-out of the lower ground plane was required to increase the inductance value to 661 pH. A butterfly stub with radius 0.71 mm and angle of 60° formed the 229 fF capacitor. With these values, the cut-off frequency of the unit cell is close to 25.0 GHz, far higher than the required frequencies of operation.

The structure in Figure 3.8b was analyzed using the ADS Momentum simulator. The extracted S-parameters were converted to an $ABCD$ matrix, and the values of Z_0 and n_{eff} were calculated using equations (3.3)-(3.5) (see Figure 3.12). The results show the unit cell has a characteristic impedance of $50\ \Omega$ and a refractive index of 3.06. This corresponds to a slowing factor of 1.6. At 6.0 GHz, which is the highest frequency of interest, the guided wavelength within the structure is 16.4 mm, more than ten times the length of the unit cell.

The simulated group delay of the unit cell is shown in Figure 3.13. A $50\ \Omega$ stripline trace in the PCB would have a delay of 6.4 ps/mm. To produce the same delay as the unit cell, the stripline line would need to be 2.03 mm long. The unit cell has resulted in a 63% reduction in length.

Figure 3.12: Extracted values of characteristic impedance and refractive index for the stripline unit cell

Figure 3.13: Extracted group delay of the stripline unit cell

Curves

To facilitate the meandering of the delay line, two curved cells were developed. The curves each used three unit cells, two of which were at 45° angles. Radial stubs were used instead of butterfly stubs because the butterfly stubs would have overlapped each other. The two curves are shown in Figure 3.14.

Figure 3.14: The two curves for meandering the delay line. Both curves are made up of three unit cells, one oriented vertically and the other two at 45° angles. All unit cells have lengths (ℓ) of 1.27mm, line widths (W) of $100\ \mu\text{m}$, and radial stubs subtended at an angle (ϕ) of 60° . (a) has radial stubs with radii (R) of 0.98mm (vertical) and 0.95mm (45° angle). (b) has radial stubs with radii of 0.89mm (vertical) and 0.86mm (45° angle). (b) also has 0.2mm x 1.14mm cutouts of the lower ground plane to enhance the line inductance. The cutouts are shown in green.

The curves were EM simulated using ADS Momentum. The results for the microstrip configuration are shown in Figure 3.15, while the results for the stripline configuration are shown in Figure 3.16. Both simulations show that the curves are well matched to $50\ \Omega$. The extracted values of n_{eff} are just slightly lower than that of the unit cells. As expected, the curves produce approximately three times the delay of a single unit cell.

Figure 3.15: Extracted (a) characteristic impedance and dielectric constant, and (b) group delay for the microstrip curve.

Figure 3.16: Extracted (a) characteristic impedance and dielectric constant, and (b) group delay for the stripline curve.

3.4 Conclusion

Slow-wave propagation is a desirable characteristic when miniaturizing delay lines, as the reduced phase velocity allows for the same time delay to be achieved with shorter circuit length. Metamaterials offer a possible solution, as they allow for high values of permittivity and permeability to be engineered. Both double-positive and double-negative metamaterials could achieve the desired length reduction; however, the narrow bandwidth and dispersive properties of double-negative materials make them less attractive for delay-line discriminator applications. Double-positive materials can be used to realize a significantly reduced phase velocity over a wide bandwidth, and with minimal dispersion. Several methods of enhancing permittivity and/or permeability have been presented in the literature. Typically, these structures involve

periodically loading a transmission line or waveguide.

In this chapter, the design of two unit cells for a delay line was presented. Both unit cells consisted of a high impedance trace loaded by a butterfly stub. The structure was sized to be smaller than a tenth of the guided wavelength over a frequency range of 3–6 GHz. The two cells differed in their transmission line configuration, with one being in microstrip and the other being in stripline. This allowed the delay line to be stacked on multiple layers within a printed circuit board. The unit cells provided a 62 % length reduction compared to standard microstrip and stripline transmission lines. Table 3.1 summarizes the simulation results for the designs, and compares them to the properties of standard transmission lines within the same substrate.

Table 3.1: Comparison of parameters for the unit cells and native transmission lines.

Parameter	Microstrip	Microstrip Unit Cell	Stripline	Stripline Unit Cell
Refractive Index, n_{eff}	1.73	2.79	1.91	3.06
Slowing factor	—	1.61	—	1.6
Guided Wavelength, λ_g ($f = 6$ GHz)	28.8 mm	17.9 mm	26.2 mm	16.4 mm
$\ell \leq \lambda_g/10$	—	Yes	—	Yes

Chapter 4

The Delay-Line Discriminator

4.1 Design Specification

The IREWTS system currently uses a heterodyned IFM receiver operating between 0.5–18 GHz. The delay-line discriminator developed in this work will increase the instantaneous bandwidth of the IREWTS receiver from 1 GHz to over 2 GHz. The 2 GHz target bandwidth is a good compromise between the wide range required for tracking frequency agile radars and the selectivity required for operating an IFM in dense environments. The design is performed assuming the discriminator voltage outputs will be digitized by a 14-bit ADC sampling faster than 250 MHz and expecting $1 V_{\text{pk-pk}}$ input. Because the measured frequency will be digitized, it is desirable for a 1 MHz increment to be easily represented as a digital number.

The shortest delay line was selected to be 305 ps long, corresponding to an unambiguous range of 3.2768 GHz. This range can be represented in 100 kHz increments using a 15-bit frequency word. 15-bit resolution can be achieved if the discriminator array provides an additional two bits. An extra bit has been added for margin in case the discriminator outputs don't exactly match the full-scale range of the ADCs. The additional bits can be realized with one (1 : 4 ratio) or two (1 : 2 ratio) additional discriminators. Based on equation (2.17), the error tolerance of these two configuration would be 45° and 60° respectively. Although the two discriminator array has cost and size benefits, a ratio of 1 : 2 provides the best error immunity [17, 20] and is the preferred solution.

To be able to identify radars with pulse compression, the discriminator needs to be able to detect frequency and phase modulation on a pulse. Measurement of frequency modulated signals is achievable as long as the following two conditions are met [24]:

1. The signal's frequency deviation is much higher than the discriminator's resolution.
2. The signal's rate of change is significantly less than the sampling rate of the ADCs.

Phase modulation poses a more difficult measurement problem. Radar signals will typically use binary or quadrature phase-shift keying with a barker code pattern to minimize side lobes [12]. Just after a phase step, the phase of the signal in the discriminator's delayed path can be expressed as

$$\phi(t - \Delta\tau) = \begin{cases} \phi(t) + \Delta\phi & \text{if } t < \Delta\tau \\ \phi(t) & \text{if } t > \Delta\tau \end{cases} \quad (4.1)$$

where $\Delta\phi$ is the size of the phase step. For a brief time of $\Delta\tau$ after the phase change the measured phase of the discriminator will be

$$\theta = \omega\Delta\tau + \Delta\phi \quad (4.2)$$

If the sampling period of the ADC is less than the delay line length $\Delta\tau$, this short glitch can be detected and measured. This would allow for not only the detection of phase modulated signals, but the identification of the modulation scheme. For an ADC sampling at 250 MHz, a delay line of at least 4 ns is required. To maintain integer delay line ratios, a $16\times$ delay line could be added to the array for the detection of phase modulated signals. This would provide an additional two bits of frequency resolution to the IFM as well.

Table 4.1 outlines the design parameters for each of the discriminators in the array. The minimum pulse width with a filter bandwidth of 300 MHz was also calculated. All four delay lines have a minimum pulse width less than the required 100 ns.

Table 4.1: Design parameters for the discriminator array

Parameter	1 : 1 Ratio	1 : 2 Ratio	1 : 4 Ratio	1 : 16 Ratio
Unambiguous Range, ω_{UA}	3.2768 GHz	1.6384 GHz	819.2 MHz	204.8 MHz
Delay, $\Delta\tau$	305 ps	610 ps	1.22 ns	4.88 ns
Resolution (14-bit)	200 kHz	100 kHz	50 kHz	12.5 kHz
Error Tolerance	60°	60°	45°	45°
Minimum Pulse Width	1.6 ns	1.9 ns	2.5 ns	6.2 ns

4.2 The Phase Detector Block

The phase detector block is critical to the performance of the delay-line discriminator. A degradation of the discriminator's frequency accuracy can be caused by a DC offset at the circuit's I and Q outputs. Similar effects are also possible if the mixers are pushed into compression. A failure to take into account these factors when selecting components and operating points can result in a higher probability of the ambiguity resolution in the IFM failing. There are typically two categories of baseband circuits for a delay-line discriminator: AC coupled and DC coupled. The AC coupled version avoids most of the problems associated with the DC offset, but cannot detect continuous wave signals since they produce a constant voltage output. To allow detection of these types of signals, the DC coupled version of the phase detector is required.

The Effect of DC Offset

A DC offset present at either of the I or Q outputs will shift the sinusoidal characteristics of V_I and V_Q , resulting in an error in the measured phase. Equation (2.11) can be rewritten to include the terms ν_I and ν_Q , which represent the magnitude of the DC component relative to the peak amplitude of the discriminator characteristic.

$$\theta = \arctan \left(\frac{\sin(\omega\Delta\tau) + \nu_Q}{\cos(\omega\Delta\tau) + \nu_I} \right) \quad (4.3)$$

The resulting phase error, $\theta_\epsilon = \omega\Delta\tau - \theta$, has been plotted in Figure 4.1. The error characteristic is a periodic function of $\omega\Delta\tau$. For small offsets, the maximum phase error is approximately proportional to the relative DC shift. The curve's large slope means that even small changes in the DC offset can cause large increases in phase

Figure 4.1: The effect of the relative DC offset on the measured phase error, θ_ϵ . (a) Phase error with a relative DC offset of 0.1 on both of the I and Q outputs. (b) Peak phase error for varying DC offsets ($\nu_I = \nu_Q$).

error.

Both the baseband amplifiers and mixers can contribute to the DC offset. For a DC coupled discriminator, the amplifiers will typically be high-speed operational amplifiers. Mismatches in the input stage of the op-amps produces a small input offset voltage. This means that even if one was to short the op-amp's two input terminals to ground, the amplifier's output will be non-zero because the input offset voltage will be amplified by the gain. For an op-amp in the non-inverting configuration, both the signal and input offset will have the same gain [59]. Therefore, the amplifier should be selected such that its input offset voltage is small relative to the expected peak DC output of the mixer. The origin of the mixer's DC offset is in its port isolations. When the applied LO and RF signals leak through to the other ports of the mixer, they can recombine and generate an undesired DC component at the IF output [60]. Simulations of an ideal mixer were performed in ADS to determine the effect that LO-RF, LO-IF, and RF-IF isolation have on the mixer's DC offset. The isolation between each pair of ports was swept individually from 10 dB to 60 dB and both the LO and RF power levels were set to 10 dBm. The resulting DC offsets are shown in Figure 4.2. They demonstrate that the LO-RF isolation is the main contributor to the mixer's DC offset, while LO-IF and RF-IF isolation have little effect on it.

The expressions for V_I and V_Q can be modified to include the DC offset term [61]. The voltages at the RF port of the mixer were rewritten to include attenuated and delayed versions of the LO signals from (2.4)-(2.5). As a result, the voltages at the

Figure 4.2: Simulated DC offset for an ideal mixer with varying LO-RF, LO-IF, and RF-IF port isolations.

IF port will be

$$V_I = \alpha \left[\cos(\omega\Delta\tau) + \frac{\alpha_{LO}}{K_{RF-LO}\alpha_{RF}} \cos(\omega\tau_{RF-LO}) \right] \quad (4.4)$$

$$V_Q = \alpha \left[\sin(\omega\Delta\tau) + \frac{\alpha_{LO}}{K_{RF-LO}\alpha_{RF}} \cos(\omega\tau_{RF-LO}) \right] \quad (4.5)$$

$$\therefore \nu_I = \nu_Q = \frac{\alpha_{LO}}{K_{RF-LO}\alpha_{RF}} \cos(\omega\tau_{RF-LO}) \quad (4.6)$$

where

- K_{RF-LO} is the mixer's LO-RF isolation
- τ_{RF-LO} is the time delay between the mixer's LO and RF ports

Both the I and Q signals have the same relative DC offset. The value is inversely proportional to the RF-LO isolation, matching the results from Figure 4.2. It also varies sinusoidally with frequency due to the propagation delay between the RF and LO ports. Another effect introduced in (4.6) is the dependence on the relative amplitudes of the LO and RF signals. To minimize the DC offset, their amplitudes should be kept as close as possible.

Another consideration when minimizing the DC offset of the mixer is the method of filtering the high-frequency components at the IF output. The mixer expects to see

Figure 4.3: Measured DC offset of an ML1-0110LSM mixer when the IF port is terminated with a wideband $50\ \Omega$ match and with a low-pass filter

a wideband impedance match for all of the frequency components it generates. A low-pass filter will only present that matched condition in its pass-band, reflecting back to the mixer most of the power in the filter's stop-band. The reflected components can degrade the mixer's port isolations, causing an increase in the undesired DC offset [62]. The data in Figure 4.3 shows the effect that a filter can have on a mixer's DC offset. DC offset measurements of a Marki Microwave ML1-0110LSM mixer were performed by terminating the mixer's RF port and then applying a signal to its LO port. The signal generator was configured to provide an 11 dBm output swept between 3 GHz and 6 GHz. The DC offset on the IF port was measured by an oscilloscope in two different configurations. For the wideband match, a DC feed was used to extract the DC offset while also providing a $50\ \Omega$ termination. A VLF-320+ low-pass filter was used for the filtered configuration. The results show that for this mixer the DC offset can be up to five times larger with a filter present than without. Therefore, the IF port of the mixer should be terminated with a wideband $50\ \Omega$ match to achieve optimum performance as a phase detector.

Absorptive filter architectures can be used to provide both a wideband match to the mixer and sufficient rejection to the undesired high-frequency components it generates. One method of achieving this is to put an isolator between the filter

and the mixer to prevent reflections. Another option is to use a diplexer with the high-pass port connected to a $50\ \Omega$ termination. The reflectionless filter architecture from [63, 64] is a potential compact absorptive filtering solution, as it can provide a wideband match in both of its pass and stop-bands. While the rejection of this type of filter is limited, they can be cascaded to achieve a desired rejection value.

Mixer Compression

When a small signal is applied to the mixer's RF port, any changes in its amplitude will result in a proportional change to the IF output. This is known as linear operation. If the RF power becomes too large, the mixer's conversion loss will begin to increase. In this compressed operation, the IF output amplitude is no longer linearly proportional to the signal amplitude at the RF port. The increase in conversion loss is due to the fact that the LO signal no longer dominates the diode switching action within the mixer when the LO and RF signals are at comparable power levels [65]. The 1dB-compression point (P1dB) of the mixer occurs when its conversion loss falls to 1 dB below the small-signal value. Operating within 3 dB of a mixer's P1dB produces degraded and unpredictable performance [65].

In the case where a mixer is operated as a phase detector, compression can distort the sinusoidal output characteristic, causing errors in the measured phase [21]. This is a design trade-off when selecting what power levels the delay-line discriminator will operate at. Increasing the RF input power to the mixer may decrease the phase error from the DC offset, but it will also increase the error contribution due to compression. Simulations were performed on Marki Microwave's ML1-0110LSM mixer to demonstrate this. The RF input power was varied between -15 dBm and 0 dBm, while the LO power was kept constant at 11 dBm. The resulting peak phase error is shown in Figure 4.4. For low input powers, the curve follows what is expected from equation (4.6); however, above -4 dBm the phase error begins to increase as the mixer compresses. The minimum phase error of 1.7° occurs 7 dB below the mixer's P1dB.

Design and Simulation

Marki Microwave's ML1-0110LSM was selected for mixers *MX1* and *MX2*. It has a 7 dB conversion loss and better than 35 dB of LO to RF isolation. The mixer requires

Figure 4.4: Simulated effect of RF power on peak phase error for the ML1-0110LSM.

an LO drive of 8–13 dBm and, based on the results in Figure 4.4, should have an amplitude of -4 dBm applied to its RF port for minimum phase error. With these power levels, the peak output voltage at the IF port will be 90 mV and the relative DC offset should be approximately 0.1 V/V. To provide a 1 V_{pk-pk} output, the baseband amplifiers will need to provide 14 dB of gain. Texas Instrument’s OPA2846 was chosen for amplifiers *A2* and *A3* because it can provide 14 dB gain over a 300 MHz bandwidth. The input offset voltage of the OPA2846 is 150 μ V and should be insignificant relative to the DC offset produced by the mixer. To minimize the effect that filters *FL1* and *FL2* have on the mixers, the XLF-151+ reflectionless filter from Mini-Circuits was used. Up to 12 GHz the XLF-151+ typically provides better than 10 dB return loss. This filter has the lowest 3 dB cut-off frequency in Mini-Circuits’ reflectionless filter series at 300 MHz. Two filters were cascaded to achieve additional rejection of the fundamental and sum frequency components. The layout of the circuit is shown in Figure 4.5.

To EM simulate the layout in Figure 4.5, the component footprints were removed and the remaining metal traces were analyzed using ADS Momentum. The results from the EM simulation were combined with the circuit models for the components to co-simulate the phase detector block. Since the mixers are non-linear devices, a harmonic balance analysis was performed. The RF and LO ports were driven by sources with amplitudes of -4 dBm and 11 dBm, respectively. A 1 ns delay was added to the sources on the RF ports to allow for the extraction of the intrinsic mixer delay

Figure 4.5: Layout for phase detector block. *MX1* and *MX2* (ML1-0110LSM) are mixers from Marki Microwave. *FL1* and *FL2* each consist of two cascaded XLF-151+. A single OPA2846 realizes both *A1* and *A2*. *R1*, *R2*, *R4*-*R6*, and *R8* are $50\ \Omega$ resistors (FC0603E50R0BTBST1). *R3* and *R7* are $453\ \Omega$ resistors (ERJ-3EKF4530V). *C1* and *C2* are $100\ \text{nF}$ decoupling capacitors (LLL185R71A104MA11L). *C3* is a $10\ \text{nF}$ decoupling capacitor (LLL185R71E103MA11L). *J1* and *J2* are SMA connectors (901-10513-2). Traces in red are on the top layer (L1) of the PCB, while traces in blue are on the inner layer (L3).

$\Delta\tau_{mix}$. The signal frequency was varied between 3 GHz and 6 GHz, and at each frequency point the phase difference between the RF and LO sources was swept from 0° and 360° . The measured phase was extracted using equation (2.11), and is plotted along with the I and Q output voltages in Figure 4.6. The peak voltages of the I and Q outputs were both 390 mV. A linear fit was performed on the unwrapped measured phase determined that the value of $\Delta\tau$ for test bench was 949 ps. Based on that result and the 1 ns delay added in the test bench, the mixer's LO port has 51.4 ps more delay than the RF port.

The DC offset at each frequency was calculated by averaging the maximum and minimum voltages of the I and Q outputs across the phase sweep. Figure 4.7 shows the extracted results. The worst case offset is 10 mV, which corresponds to a relative DC offset of 2.83% or a peak phase error of 1.5° .

Figure 4.6: Simulated voltage outputs of the phase detector block.

Figure 4.7: Simulated DC offset on the I and Q outputs of the phase detector block.

4.3 The Delay Split Block

The delay split block consists of the power divider *PD2*. Similar to the mixer's DC offset, amplitude and phase imbalance in the power divider can cause errors in the measured phase. This is due to the fact that the I and Q arms of the discriminator will have small differences in amplitude and be slightly out of quadrature. These imbalance terms can be represented by $\alpha_{IMB}^{\pm}$ and ϕ_{IMB} .

$$\theta = \arctan \left(\frac{\alpha_{IMB}^{+} \sin(\omega\tau + \phi_{IMB})}{\alpha_{IMB}^{-} \cos(\omega\tau - \phi_{IMB})} \right) \quad (4.7)$$

The effect of the two types of imbalances were simulated and the results are shown in Figures 4.8 and 4.9. In both cases the phase error is a periodic function of $\omega\Delta\tau$, with two cycles occurring over a full 360° sweep. When the phase imbalance is less than 15° , the peak error is approximately equal to the imbalance. Amplitude imbalance is also directly proportional to peak error for small values. A 1 dB increase in amplitude imbalance will produce approximately a 6° increase in peak phase error.

The delay split can also contribute to the DC offset in the phase detector through coupling between the I and Q arms of the discriminator. As discussed previously, the RF ports of the mixers will have LO components present that can self-mix due to finite mixer isolation. The power divider will also have finite isolation between its two outputs. This allows the LO from the discriminator's I arm to leak into the Q arm and vice versa, a phenomenon that is depicted in Figure 4.10. In [23] equation

Figure 4.8: The effect of phase imbalance on the measured phase error, θ_{ϵ} . (a) Phase error with a phase imbalance of 5° . (b) Peak phase error for varying phase imbalances.

Figure 4.9: The effect of amplitude imbalance on the measured phase error, θ_{ϵ} . (a) Phase error with a amplitude imbalance of 1.0 dB. (b) Peak phase error for varying amplitude imbalances.

(4.6) was modified to include the effect of the power divider.

$$\nu_I = \frac{\alpha_{LO}}{K_{RF-LO}\alpha_{RF}} \left[\cos(\omega\tau_{RF-LO}) - \frac{1}{K_{PD2}} \sin(\omega\tau_{cpl}) \right] \quad (4.8)$$

$$\nu_Q = \frac{\alpha_{LO}}{K_{RF-LO}\alpha_{RF}} \left[\cos(\omega\tau_{RF-LO}) + \frac{1}{K_{PD2}} \sin(\omega\tau_{cpl}) \right] \quad (4.9)$$

where

- K_{PD2} is the isolation between the two outputs of power divider $PD2$
- τ_{cpl} is the time delay between the LO port in one arm of the discriminator and the RF port in the other

A high isolation in the power divider is desirable so that the sine terms from the above expressions become insignificant relative to the cosine ones. It should be also noted that the DC offsets in the I and Q arms will be different due to the sine terms having opposite signs.

Mini-Circuits' GP2X+ was selected for $PD2$. The power divider has low insertion loss, high isolation, and good amplitude imbalance in a small surface mount package. The GP2X+ does have a worst case phase of 9° , but it is typically less than this value. The low insertion loss means that less power is needed at the input to the discriminator to achieve the optimum RF drive level of the mixers in the phase detector block. The layout for the delay split block is shown in Figure 4.11.

Figure 4.10: Coupling between the I and Q arms of the discriminator causing additional self-mixing [23].

Figure 4.11: Layout for delay split block. $PD2$ is the Mini-Circuits power splitter GP2X+. Traces in red are on the top layer (L1) of the PCB.

ADS Momentum and measured S-parameters provided by the vendor were used to perform an EM co-simulation of the layout in Figure 4.11. Plots of the insertion loss, isolation, and phase imbalance are shown in Figure 4.12. Over the entire band the insertion loss is less than 4 dB and both the I and Q paths are within 0.1 dB of each other. The phase imbalance is also better than 1.0° over the frequency range of interest. Therefore, the imbalances within delay split block should contribute less than 1° of error to the measured phase. The worst case isolation is 16 dB and occurs at 6 GHz. This will result in a 15% increase in the phase detector's DC offset. Figure 4.13 shows the simulated group delay of the circuit, which has a mean value of 169 ps. The curve has a negative slope which will help compensate for the positive

Figure 4.12: (a) The insertion loss for the I and Q paths. (b) Phase imbalance between the I and Q paths.

Figure 4.13: Simulated group delay of the delay split block.

group delay slope in the unit cells that make up the delay line.

4.4 The Input Split

Phase and amplitude imbalance in *HY1* can cause measured phase error in similar ways to *PD2* from the delay split block. *HY1* provides the 90° shift required for the discriminators I and Q arms to be in quadrature. Any deviation from this ideal 90° shift will result in the same phase error characteristic as in Figure 4.8. Since the LO signal is predominantly a switching signal, small amplitude variations in it

Figure 4.14: The effect of amplitude imbalance on the ML1-0110LSM mixer when it is present at the RF and LO ports.

will not have a significant effect on the phase detector's output. This means that the mixer's LO port is less susceptible to the effects of amplitude imbalance. Figure 4.14 shows the peak phase error of the ML1-0110LSM mixer when its RF and LO ports are subjected to amplitude imbalances ranging from 0 dB to 10 dB. The mixer's LO produces much less phase error than the RF port when amplitude imbalance is present. It is for this reason that *HY1* was used in the LO path and not the RF path.

Figure 4.15 shows the layout for the input split circuit. The design used the same power divider as the delay split block. For the quadrature hybrid coupler, the QCS-592+ from Mini-Circuits was chosen. It provided an insertion loss better than 4 dB, as well as amplitude and phase imbalances within 1.5 dB and 5°. Amplifier *A1* was required to provide at least 15 dB of gain and have a P1dB greater than 15 dBm to provide an LO drive of 11 dBm to the mixers. Mini-Circuits PMA3-83LN+ met these requirements and required only a few external components for biasing. Because of its excess gain, a 6 dB pad was added to the input of *A1* so that the difference in amplitude between the RF and LO signals would be close to the optimum value of 15 dB.

ADS Momentum and measured data provided by the vendor were used to perform

Figure 4.15: Layout for input split block. *PD1* (GP2X+) and *HY1* (QCS-592+) are a power splitter and quadrature hybrid from Mini-Circuits. Amplifier *A1* (PMA3-83LN+) and attenuator *AT1* (YAT-6+) are also Mini-Circuit parts. The DC blocking capacitor *C1* (C04BL121X-5UN-X0T) is from Dielectric Laboratories. *C2* (GJM1555C1H100JB01D) and *C3* (LLL185R71E103MA11L) are 10 pF and 10 nF decoupling capacitors. Inductors *L1* (LQW18AN18NG00D) and *L2* (LQW18AN39NG00D) are 18 pF and 39 pF respectively. *R1* (FC0603E50R0BTBST1) is 50 Ω . Traces in red are on the top layer (L1) of the PCB.

an EM co-simulation of the layout in Figure 4.15. Plots of the insertion loss, amplitude imbalance, and phase imbalance are shown in Figure 4.16. The gain in the I and Q paths range from 6 dB to 8 dB. Therefore, an input of 4 dBm will provide the necessary LO drive for the phase detector block. In the delayed path, the combined loss of 8 dB between this circuit and the delay split block will result in an amplitude close to -4 dBm at the RF ports of the mixers. The amplitude imbalance, which is largest at the band edges, should have a negligible effect on the measured phase, while the phase imbalance will introduce an additional 3° of error. The $v_{LO,I}$ and $v_{LO,Q}$ outputs have 375 ps more group delay than the v_{DEL1} output. The sloped characteristic that is caused by the GP2X+ is present for all paths meaning the delay differences are relatively flat across frequency. The group delay plots can be seen in Figure 4.17.

Figure 4.16: (a) The insertion loss to the I, Q, and delayed paths. (b) The amplitude and phase imbalance between the I and Q paths.

Figure 4.17: Simulated group delays for the v_{DEL1} , $v_{LO,I}$, and $v_{LO,Q}$ outputs of the input split block.

4.5 Delay-Line Discriminator Design

The final sub-circuit of the discriminator is the delay line. Four different delay lines were designed, each following the same procedure. Using the mean group delays simulated for the input split, delay split, and phase detector blocks, the required delay line length was estimated using equation (2.10). The delay line was formed by cascading the unit cells from Chapter 3 in a meandering fashion. A full EM (ADS Momentum) and circuit co-simulation was performed on each delay-line discriminator to extract its value of $\Delta\tau$. The same test bench was used for all four discriminators:

- The simulation used harmonic balance analysis

- The discriminator's input was driven by a $50\ \Omega$ source with an amplitude of 4 dBm
- The input frequency was swept from 3–6 GHz in 10 MHz steps
- The I and Q outputs of the discriminator were terminated with $50\ \Omega$ resistors
- A four-quadrant arctangent was performed on the I and Q output voltages to calculate θ
- The value of $\Delta\tau$ was extracted by unwrapping the value of θ and applying a linear fit
- The phase error was calculated using $\theta_\epsilon = 2\pi f\Delta\tau - \theta$

Adjustments were made to the delay lines if the value of $\Delta\tau$ was too small or too large.

305 ps Discriminator

For the 305 ps discriminator, the delay line needed to be 562 ps long. This delay was realized with 31 microstrip unit cells, 6 stripline unit cells, and 1 microstrip curve. Figure 4.18 shows the full discriminator layout, while Figure 4.19 shows the simulated S-parameters and group delay for the delay line. The output voltages from the co-simulation of the discriminator are plotted in Figure 4.20a. The peaks of the voltage characteristic range from 375 mV down to 340 mV. This is slightly less than the peak voltage simulated for the phase detector block because of the 0.7–1.2 dB insertion loss in the delay line. Figure 4.20b shows the measured phase and phase error. The maximum phase error of $\pm 12.5^\circ$ is well within the 60° tolerance for ambiguity resolution. The extracted value of $\Delta\tau$ was 304 ps, resulting in an unambiguous range of 3.29 GHz. This is within 1.41 ps of the desired value.

Figure 4.18: Layout of the 305 ps delay-line discriminator, including the input split, delay split, and phase detector blocks, as well as the 562 ps delay line.

Figure 4.19: EM simulation results for the 562 ps delay line: (a) Insertion and return losses, and (b) group delay.

Figure 4.20: Co-simulation results for the 305 ps delay-line discriminator: (a) I and Q output voltages, and (b) measured phase and phase error

610 ps Discriminator

For the 610 ps discriminator, the delay line needed to be 867 ps long. This delay was realized with 41 microstrip unit cells, 19 stripline unit cells, and 1 microstrip curve. Figure 4.21 shows the full discriminator layout, while Figure 4.22 shows the simulated S-parameters and group delay for the delay line. The output voltages from the co-simulation of the discriminator are plotted in Figure 4.23a. The peaks of the voltage characteristic are slightly lower than the 305 ps delay line because of the extra 0.5 dB insertion loss in the 867 ps delay line. Figure 4.23b shows the measured phase and phase error. The maximum phase error of $\pm 12.5^\circ$ is well within the 60° tolerance for ambiguity resolution. The extracted value of $\Delta\tau$ was 609 ps, resulting in an unambiguous range of 1.64 GHz.

Figure 4.21: Layout of the 610 ps delay-line discriminator, including the input split, delay split, and phase detector blocks, as well as the 867 ps delay line.

Figure 4.22: EM simulation results for the 867 ps delay line: (a) Insertion and return losses, and (b) group delay.

Figure 4.23: Co-simulation results for the 610 ps delay-line discriminator: (a) I and Q output voltages, and (b) measured phase and phase error

1.22 ns Discriminator

For the 1.22 ns discriminator, the delay line needed to be 1.48 ns long. This delay was realized with 66 microstrip unit cells, 40 stripline unit cells, 2 microstrip curves, and 1 stripline curve. Figure 4.24 shows the full discriminator layout, while Figure 4.25 shows the simulated S-parameters and group delay for the delay line. The output voltages from the co-simulation of the discriminator are plotted in Figure 4.26a. The peaks of the voltage characteristic have been reduced to approximately 270–330 mV, which corresponds to the 1.7–3.1 dB insertion loss of the 1.48 ns delay line. Figure 4.26b shows the measured phase and phase error, the latter being well within the required 45° tolerance. The extracted value of $\Delta\tau$ was 1.22 ns, resulting in an unambiguous range of 821 MHz.

Figure 4.24: Layout of the 1.22 ns delay-line discriminator, including the input split, delay split, and phase detector blocks, as well as the 1.48 ns delay line.

Figure 4.25: EM simulation results for the 1.48 ns delay line: (a) Insertion and return losses, and (b) group delay.

Figure 4.26: Co-simulation results for the 1.22 ns delay-line discriminator: (a) I and Q output voltages, and (b) measured phase and phase error

4.88 ns Discriminator

For the 4.88 ns discriminator, the delay line needed to be 5.14 ns long. This delay was realized with 197 microstrip unit cells, 172 stripline unit cells, 7 microstrip curves, and 6 stripline curve. Figure 4.27 shows the full discriminator layout, while Figure 4.28 shows the simulated S-parameters and group delay for the delay line. The output voltages from the co-simulation of the discriminator are plotted in Figure 4.29a. Significant reductions to the peak amplitude of the I and Q voltage characteristics, as well as a noticeable slope across frequency, can be seen for the $16\times$ ratio discriminator. The insertion loss of the 5.14 ns delay line ranges from 7–11 dB, which is about 7 dB higher than the next longest delay line. The slope on the insertion loss would suggest the need for gain compensation for the longer delay lines in future iterations of this design. Figure 4.29b shows the measured phase and phase error. The maximum phase error of $\pm 17^\circ$ is well within the 45° tolerance for ambiguity resolution. The extracted value of $\Delta\tau$ was 4.81 ns, resulting in an unambiguous range of 208 MHz. The 72.1 ps error in the delay value for this discriminator occurred because the full EM co-simulation of the delay line was only completed post-fabrication. Simulations of the design were performed by cascading the extracted S-parameters of the delay line unit cells since the length of time required to complete the EM analysis was so

Figure 4.27: Layout of the 4.88 ns delay-line discriminator, including the input split, delay split, and phase detector blocks, as well as the 5.14 ns delay line.

Figure 4.28: EM simulation results for the 5.14 ns delay line: (a) Insertion and return losses, and (b) group delay.

Figure 4.29: Co-simulation results for the 4.88 ns delay-line discriminator: (a) I and Q output voltages, and (b) measured phase and phase error

large.

4.6 Discriminator Array

To feed four discriminators in parallel, a 4-way splitting network was required. Three GP2X+ power splitters were used to realize the splitting network, which had approximately 8 dB of insertion loss between the input and each of the discriminators. With the additional loss, the optimum input power to the discriminator array was 12 dBm. Figures 4.30 and 4.31 show the fabricated PCB, which includes the splitting network and the four discriminators. The board requires 5 V and -5 V supply voltages. Two additional 2.2 μ F decoupling capacitors (TPSA225K020R3000) were added between

Figure 4.30: The top side of the printed circuit board implementing the delay-line discriminator array.

the supply voltages and ground. The dimensions of the PCB are 10 cm $\times$ 15 cm.

Figure 4.31: The bottom side of the printed circuit board implementing the delay-line discriminator array.

The fabricated circuit was measured using the test setup in Figure 4.32 to extract its frequency-voltage characteristics and pulsed response. Rohde & Schwarz's SMB100A-20 signal generator provided the input signal for the fixed frequency measurements. An MCCM-00520-02 radar signal simulator generated the stimuli for the measurements of pulses with frequency or phase modulation. One oscilloscope was a Rohde & Schwarz RTO2024 while the other was an RTO1014.

To measure the frequency-voltage characteristics, the SMB100A-20 was configured to drive the circuit with a 12 dBm amplitude and sweep its frequency from 3–6 GHz in 1 MHz steps. The output voltages of the discriminators were measured

Figure 4.32: The test setups for measurements of the delay-line discriminator array.

by taking the mean value of each oscilloscope trace. These output voltages, and the corresponding values of θ calculated from equation (2.11), are plotted in Figure 4.33. From the plots it can be seen that the output levels are considerably smaller than the simulated values from Sec. 4.5 and have a steeper slope across frequency. These effects are more noticeable for the discriminators with longer delays, indicating that there is an increased attenuation in the delay lines. The peaks in the 4.88 ns discriminator's outputs can be as low as 30 mV, which corresponds to a delay line loss of about 20 dB. The additional loss is likely due to the ENIG surface plating used on the printed circuit board. ENIG is a lead-free surface plating that provides good solderability and a high resistance to oxidation. The main drawback of this finish for high frequency circuits is that nickel has less than one third the conductivity of copper, resulting in higher conductor losses [66]. Exacerbating this is the fact that nickel is also ferromagnetic ($\mu_r \approx 600$ [47]), making its skin depth much smaller than that of copper or gold. The manufacturer specified that the nickel plating thickness on the board was approximately 4.6 μm , which is 65 times larger than nickel's skin depth at 6 GHz. This means that almost all of the current is flowing in the less conductive metal. Measurements of 50 Ω microstrip traces with an ENIG finish have shown higher per-unit losses than bare copper traces and a steeper slope across frequency [66]. At 6 GHz the loss was 60 % higher in the ENIG trace relative to bare copper. Future design iterations of the discriminator array should use a less lossy surface finish, such

Figure 4.33: Measured frequency-voltage characteristics of the fabricated discriminator array: (a) 305 ps DLD, (b) 610 ps DLD, (c) 1.22 ns DLD, (d) 4.88 ns DLD.

as immersion silver.

The value of $\Delta\tau$ was extracted from the slope of the unwrapped θ curve for each discriminator. With this value known, the phase error of the discriminator could also be calculated. Table 4.2 summarizes the simulated and measured values of $\Delta\tau$. The delays of the 305 ps, 610 ps, and 1.22 ns circuits were all measured to be about 150 ps too long. It was discovered after fabrication that de-embedding was not performed on the manufacturer provided component data for the PMA3-83LN+. This resulted in an overestimation of the required delay line length. Based on the test board material and a rough estimate of trace lengths, it is expected that test fixtures added around 140 ns of delay to the measured component data. Along with the effects of the matching inductor $L1$ from the input split block, which were also not de-embedded in the component data, these estimated test bench delays are in line with the errors seen on the extracted values of $\Delta\tau$. The 4.88 ns discriminator has slightly less error on its delay because it was already 72 ps shorter than what the simulation expected it to be

Figure 4.34: Extracted phase error from the fabricated discriminator array's frequency-voltage characteristic

to achieve the design value. The phase error for each of the delay-line discriminators is shown in Figure 4.34 and all values are within the tolerances required for ambiguity resolution. The worst case phase error of 18.8° occurs at 3.1 GHz in the 4.88 ns discriminator. Aside from this peak, the phase errors track well between the four circuits. The longest delay-line discriminator, which determines the overall accuracy of the array, has an RMS phase error of 6.75° . This corresponds to an RMS frequency accuracy of 3.74 MHz. Calibration [22] and compensation [23] techniques can be used to further improve the accuracy of the circuit.

Table 4.2: Comparison of the extracted $\Delta\tau$ values for the simulated and measured discriminator array. The deviation from the design value is in parentheses. A negative value indicates a delay line that is too long.

Discriminator	Simulated $\Delta\tau$	Extracted $\Delta\tau$
305 ps DLD	304 ps (1.41 ps)	455 ps (−150 ps)
610 ps DLD	609 ps (0.817 ps)	760 ps (−150 ps)
1.22 ns DLD	1.22 ns (1.52 ps)	1.38 ns (−159 ps)
4.88 ns DLD	4.81 ns (72.1 ps)	5.02 ns (−135 ps)

To measure the pulsed response of the circuit, the SMB100A-20 was set up to produce a signal with a pulse width of 100 ns. The input remained at an amplitude of 12 dBm. The 305 ps and 610 ps discriminators were measured with an RF of 4.1 GHz, while 3 GHz was used for the 1.22 ns and 4.88 ns discriminators. The pulsed responses are plotted in Figure 4.35 along with the measured phase, which was only calculated within the limits of the pulse because of a noisy arctangent result with no signal present. Rise and fall times were measured on the oscilloscopes, with all values being less than 3 ns. The clean shape of the pulses would indicate the ability to measure the frequency accuracy at narrower pulse widths. The baseband filter bandwidth could also be reduced without significant reduction in measurement accuracy on narrow pulses. A narrower bandwidth is desirable since it would allow for the application of simultaneous signal estimation methods, such as the one proposed in [24], on signals with more closely spaced frequencies. From equation (2.14), the minimum filter bandwidth needed to be able to measure a 100 ns pulses with the longest delay discriminator is about 10 MHz. A hybrid filtering scheme that pairs an XLF-151+ with a lower cut-off low-pass filter could be employed to better balance the need for a wideband match at the mixer's output and the desire for a narrower video bandwidth.

Figure 4.35: Measured response of the fabricated discriminator array to a 100 ns pulse: (a) 305 ps DLD ($f_{in} = 4.1$ GHz), (b) 610 ps DLD ($f_{in} = 4.1$ GHz), (c) 1.22 ns DLD ($f_{in} = 3$ GHz), (d) 4.88 ns DLD ($f_{in} = 3$ GHz).

To test the discriminator's response to a phase modulated pulse, the MCM-00520-02 radar signal simulator was configured to produce a 3 GHz, 1 μ s pulse that changed phases every 0.25 μ s. Both 90° and 180° phase steps were tested. The shorter delay discriminators did not show any significant deviations in their measured phase when the modulation was present. The 4.88 ns discriminator showed detectable deviations in its measured phase for both cases (see Figure 4.36). The deviations were triangularly shaped and approximately 30 ns wide. The peak excursion was dependent on the phase step size, being approximately 15° for 90° steps and approximately 60° for 180° steps. These deviations are likely detectable in digital processing to determine if phase modulation is present. More effort is required to determine the relationship between the peak θ deviation and the phase step so that a coarse estimate of the modulation scheme can be made.

Figure 4.37 shows the DLD array's response to a pulse with a linear frequency chirp. The pulse was 50 μ s wide and had a 1 GHz chirp changing at a rate of

Figure 4.36: Measured response of the 4.88 ns discriminator to a phase modulated signal with a phase deviation of (a) 90° and (b) 180° .

Figure 4.37: Measured response of the discriminator array to a pulse with linear frequency modulation.

20 MHz/ μs . The plot shows all four θ values varying linearly with time. The misalignment between the pulses is due to the slight differences in trigger position between the two oscilloscopes.

The return loss of the discriminator array was measured on a ZNB20 vector network analyzer (VNA). The VNA and test cable were calibrated using open, short, and matched loads. S_{11} was measured across the frequency range of the circuit at a power level of 10 dBm. The results of the measurement are shown in Figure 4.38. The input return loss is better than 14 dB across the entire operating band of the discriminator.

Figure 4.38: Measured return loss of the discriminator array's RF input.

4.7 Conclusion

This chapter presented the design and analysis of a miniaturized delay line discriminator array. The array consisted of four discriminators with delays of 305 ps, 610 ps, 1.22 ns, and 4.88 ns. The analysis explored possible sources of measurement error, which included amplitude/phase imbalance in the power splitting components and DC offset in the mixers, while the design attempted to minimize these effects. A reduction in delay line length of approximately 60 % was achieved by using the unit cells developed in Chapter 3. The circuit was fabricated on a 4-layer PCB that consisted mainly of Rogers RO4350B dielectric material. Measurements of the discriminator array showed higher losses and shorter delays than expected from the simulation results. These inconsistencies can likely be attributed to the ENIG surface finish on the board, as well as the fact that circuit models for the PMA3-83LN+ included test fixture delays. Measured phase errors are well within the tolerances required for proper ambiguity resolution. An overall frequency accuracy of 3.74 MHz RMS was achieved with the array. Additional calibration and compensation techniques can be employed to further improve this accuracy. The performance of the discriminators is summarized in Table 4.3.

Table 4.3: Summary of the delay-line discriminator array's measured performance

	305 ps DLD	610 ps DLD	1.22 ns DLD	4.88 ns DLD
Delay, $\Delta\tau$	455 ps	760 ps	1.38 ns	5.02 ns
Unambiguous Bandwidth	2.2 GHz	1.32 GHz	725 MHz	199 MHz
RMS Frequency Accuracy	26 MHz	14.9 MHz	8.75 MHz	3.74 MHz
Peak Phase Error	11°	10.1°	14.3°	18.8°
Rise Time (I/Q)	1.9 ns/1.7 ns	2.2 ns/1.7 ns	2.1 ns/1.7 ns	1.9 ns/3 ns
Fall Time (I/Q)	2.2 ns/2.2 ns	1.8 ns/2 ns	2.4 ns/2 ns	1.9 ns/1.9 ns

Chapter 5

Conclusion

In this thesis, the design of a miniaturized delay-line discriminator array for electronic warfare applications was presented. The array consisted of four discriminators with delay line ratios of 1, 2, 4, and 16. The circuit was fabricated on a four-layer PCB with dimensions $10\text{ cm} \times 15\text{ cm}$ and made up of Rogers RO4350B dielectric material. Miniaturization of the discriminator was achieved through the use of an artificial transmission line with enhanced permittivity. The unit cell for the delay line consisted of a high impedance trace loaded by butterfly stubs and was sized to be less than one-tenth of the guided wavelength within the structure. Both a microstrip and stripline version of the unit cell were developed, allowing for line to be stacked vertically within the PCB. A slowing factor of 1.6 was realized with this structure, allowing for a 60 % length reduction of the delay line.

The fabricated discriminator array demonstrated the ability to measure frequency unambiguously over a frequency range greater than 2 GHz. Measurement accuracy was within 3.74 MHz RMS. Calibration and correction techniques will need to be employed to achieve better than 1 MHz accuracy. A discrepancy of approximately 150 ps was seen in the extracted delay values of each discriminator. This limited the design to a 2.2 GHz range when the design targeted an unambiguous measurement range greater than 3 GHz. The errors in the delay values were due to the circuit models for the PMA3-83LN+ amplifier including the group delays from the manufacturer's test fixtures. A larger than expected insertion loss in the delay lines was also measured. The cause of this was likely the ENIG surface finish on the PCB traces. The pulsed response of the discriminators showed fast rise and fall times, as well as a clean pulse shape with little ringing. Accurate frequency measurements on pulses less than 100 ns should be possible.

Table 5.1: Comparison of this work to other discriminators presented in the literature. Unless otherwise specified, frequency accuracy is expressed as an RMS value.

	This work	[23]	[23]	[24]	[26]
Type	Analog DLD	Analog DLD	Analog DLD	Analog DLD	Digital discriminator
Longest Delay Line	$\times 16$	$\times 64$	$\times 64$	$\times 2$	$\times 128$
Frequency Range	3.5–6.5 GHz	2–6 GHz	6–18 GHz	2–4 GHz	—
Measurement Bandwidth	2 GHz	4 GHz	12 GHz	2 GHz	1.2 GHz
Frequency Accuracy	3.74 MHz	0.95 MHz	1.49 MHz	—	± 2 MHz
Miniaturization Factor	62 %	—	—	—	—

Table 5.1 provides a comparison of the discriminator array developed in this thesis with others presented in the literature. Although some of the designs demonstrate the ability to operate over wider bandwidths, the measurement bandwidth of 2 GHz was specifically chosen for MC Countermeasures’ application. The frequency accuracy achieved in this work is similar to that of the all-digital design from [26]. The delay-line discriminator arrays from [23] were able to achieve higher accuracies due to the longer delay lines that were used ($\times 64$ as opposed to $\times 16$); however, both the discriminators from this design and those from [23] exhibited a typical RMS phase error of approximately 4° - 5° . The design in [23] also employed compensation techniques to further improve its frequency accuracy. The delay-line discriminator array from this work could also benefit from such techniques to achieve the desired accuracy of 1 MHz RMS. Overall, this work was able to achieve comparable performance of the DLD array while also achieving a 62 % size reduction in the circuit.

5.1 Future Work

There is significant room for development on the topic of delay-line discriminators and their processing algorithms. Future iterations of this design should look to correct the component models and surface finish issues. This should extend the instantaneous

bandwidth of the discriminator to above 3 GHz. Even with a less lossy surface finish, there still would have been a slope on the outputs of the larger delay discriminators. Gain equalization techniques could be employed to ensure the ADCs are being driven to their full range across the entire frequency range of the discriminator. Further work on the digital processing of the discriminator's outputs is needed. Improved pulse detection algorithms have improved measurement accuracy in an all digital design by providing better timing for the frequency measurement [27]. These algorithms could be modified to provide improved measurement accuracy on narrow pulses in an analog DLD. Improved methods of measuring frequency and phase modulated pulses should be developed, while the detection of other modulation schemes, such as orthogonal frequency division multiplexing (OFDM), should be explored. Lastly, a promising method of frequency estimation with overlapping signals was reported in [24]. The accuracy of the estimate was dependent on how close the two signals were in frequency. The effect of the baseband filters on these algorithms should be studied to determine the optimum bandwidth for balancing narrow pulse detection with accurate measurement of simultaneous signals.

Applying re-configurable circuit concepts to the delay-line discriminator also presents the possibility of a much more robust design. In the current design, each of the shorter delay discriminators within the array act as a single point of failure. If one were to fail, it would prevent the ambiguities in the longer delay discriminators from being resolved. Instead of using four different DLDs with varying delay line lengths, a single discriminator with a tunable delay line could be repeated four times to realize the array. This adds a layer of redundancy because if one of the circuits fail, another one could be re-configured to take its place. Although the discriminator array would be operating at a reduced capacity (e.g. lower accuracy), it would still be able to provide most of its functionality. This idea of self-healing systems is very attractive in military applications, as long deployments in remote locations may make it difficult to get access to the parts and/or personnel required to make repairs. Recent developments in re-configurable metamaterial-based waveguides [67] could enable this new type of delay-line discriminator array.

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Appendix A

Radar Bands

Table A.1: ITU frequency allocation for radar bands [12, 68, 69]. Radar bands of interest (i.e. between 0.5–18 GHz) have been bolded.

Band Designation	Frequency Range	Radar Bands
HF	3–30 MHz	
VHF	30–300 MHz	138–144 MHz 216–225 MHz
UHF	0.3–1.0 GHz	420–450 MHz 890–942 MHz
L	1–2 GHz	1.215–1.400 GHz
S	2–4 GHz	2.3–2.5 GHz 2.7–3.7 GHz
C	4–8 GHz	5.250–5.925 GHz
X	8–12 GHz	8.50–10.68 GHz
Ku	12–18 GHz	13.4–14.0 GHz 15.4–17.7 GHz
K	18–27 GHz	24.05–24.25 GHz 24.65–24.75 GHz

Band Designation	Frequency Range	Radar Bands
Ka	27–40 GHz	33.4–36.0 GHz
V	40–75 GHz	59.0–64.0 GHz
W	75–110 GHz	76.0–81.0 GHz 92–100 GHz
mm	110–300 GHz	126.0–142.0 GHz 144.0–149.0 GHz 231.0–235.0 GHz 238.0–248.0 GHz