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**Noise Analysis and Simulation of
Switched-Capacitor Circuits
Using a Continuous Time
Circuit Simulator**

— by —

Jonathan Kwan, B.A.Sc.

**This thesis is submitted to the
Faculty of Graduate Studies and Research
in partial fulfillment of the
requirements for the degree of**

Master of Engineering

Ottawa Carleton Institute for Electrical Engineering

**Department of Electronics
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June, 1988

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Using a Continuous Time Circuit Simulator"

submitted by Jonathan Kwan in partial fulfillment of the requirements for the degree of Master of Engineering.

Prof. M.A. Copeland
Thesis Supervisor

Prof. M.A. Copeland
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June, 1988

Abstract

In this thesis, a methodology for the analysis and simulation of random noise in switched-capacitor circuits is described. Based on a detailed analysis of the origins and occurrences of random noise in switched-capacitor circuits, a novel approach of using a continuous time circuit simulator to perform noise analysis on switched-capacitor circuits has been developed. The validity of the approach is supported by extensive experimental data. Although not central to the thesis, the technique of using correlated double sampling to reduce low frequency noise in switched-capacitor circuits has also been studied.

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Chapter 1

Introduction

1.1 Thesis Motivation

The main objective of this thesis is to develop a methodology for the analysis and simulation of random noise in switched-capacitor (SC) circuits. In order to design high performance, wide dynamic range analog SC circuits, it is necessary to understand the internal mechanisms by which noise is generated, and to establish the link between various noise sources and the overall circuit noise performance. The ability to use simulation tools to predict the circuit noise performance efficiently and economically, within the context of readily available continuous time circuit simulation programs like SPICE, is very important. This thesis shows the possibilities and the limitations in performing such simulations, with extensive measurements for verification.

Over the past decade, MOS technology has evolved as the mainstream VLSI technology. The implementation of high performance monolithic active filters in MOS technology was first achieved with the development of switched-capacitor technology in 1977 [1,2]. As MOS technology advances, the minimum feature size shrinks and the complexity of integrated circuits is increasing rapidly. The SC technique is now employed in a very wide range of applications, and high performance is demanded. Examples of these applications are filtering for high quality voice channel (16 bits) data transmission, and high speed, high resolution (over 15 bits) AD/DA

converters [3,4]. The ability to achieve wide dynamic range is essential to the successful development of these products.

The dynamic range of a circuit is defined as the ratio of the maximum input signal amplitude that the circuit can handle without generating excessive distortion, to the minimum input signal that the circuit can resolve. For a given operating voltage and circuit topology, internally generated noise and harmonic distortion often impose an upper limit on the achievable dynamic range. Random noise, which is considered the dominant factor, will be the subject of investigation in this thesis. Specifically, a novel approach to the simulation of random noise in SC circuits will be presented.

1.2 The Switched-Capacitor Principle

The idea of using a periodically switched capacitor to emulate a resistor started in the early seventies [5]. The concept is best illustrated with the aid of Figure 1-1. S1 and S2 are MOS switches that are controlled by the two non-overlapping clock signals, $\phi 1$ and $\phi 2$. When S1 is closed with $\phi 1$ being high, the capacitor C_R is charged to V_1 . When $\phi 2$ becomes high, S2 is closed and C_R is now charged to a new voltage V_2 . If V_1 and V_2 are different, then there is a net transfer of charge ΔQ , where

$$\Delta Q = (V_1 - V_2)C_R$$

and the transfer current,

$$I = \frac{\Delta Q}{\Delta t} = \frac{\Delta Q}{T}$$

Figure 1-1 A switched-capacitor resistor

$$I = (V_1 - V_2) \frac{C_R}{T} \quad (1-1)$$

The current in the resistor equivalent circuit of Figure 1-1 can be obtained by applying Ohm's Law, yielding

$$I = (V_1 - V_2) \frac{1}{R} \quad (1-2)$$

Comparing equations 1-1 and 1-2, the equivalent resistance of the SC circuit, R_{EQ} , is then

$$R_{EQ} = \frac{T}{C_R}$$

or

$$R_{EQ} = \frac{1}{f_S C_R} \quad (1-3)$$

where f_S is the clock frequency. Hence under ideal conditions a periodically switched capacitor has the charge transfer characteristics of a resistor.

The most common and the most difficult application of the SC technique is frequency domain filtering of analog signals. The basic building block in active SC filters is the SC integrator. The SC version of the continuous time integrator of Figure 1-2a is obtained by replacing the resistor R by the SC equivalent of Figure 1-1, as shown in Figure 1-2b. Due to the sampled-data nature of the circuit, its transfer function is expressed in the z domain. It can be shown that for $f \ll f_S$, the transfer function of SC integrator can be approximated by replacing R in the transfer function of the continuous time circuit

Figure 1-2a Continuous time integrator

Figure 1-2b Switched capacitor integrator

with equation 1-3. If we denote $H_{SC}(f)$ as the low frequency transfer function of the SC integrator, then

$$H_{SC}(f) = \frac{1}{2\pi f R_{EQ} C_I}$$

Hence the time constant of the SC integrator is given by

$$\tau = \frac{1}{R_{EQ} C_I} = f_s \frac{C_R}{C_I} \quad (1-4)$$

The major advantage that a SC filter has over its continuous time counterpart in MOS technology is the way time constants are formed. The implementation of high performance continuous time active filters has not been very successful due to the difficulties associated with producing high precision resistors. In SC circuits, the time constant is a function of the clock rate and the ratio of two capacitors as given in equation 1-4. An accurate frequency reference can be generated externally and capacitor matching with tolerance in the order of 0.1% [6] is easily attainable with modern MOS technology. These factors, among others, are responsible for the popularity of using the SC technique to perform analog signal processing.

1.3 Random Noise in SC Circuits

Noise at the output of a SC circuit originates either internally or externally. Power supply noise is the main external noise source of concern and is attenuated by the power supply rejection capability of the circuit. Internally generated noise generally belongs to one of

three categories: thermal noise of switches, thermal noise of op amps, and $1/f$ noise of op amps.

A MOS switch is made up of a single or a pair of complementary MOSFETs connected in parallel. In CMOS technology, the latter is the standard practice because of wider voltage swing and reduced clock feedthrough. The closing of a switch is accomplished by turning the transistors on hard. A finite 'ON' resistance exists between the source and drain terminals of the conducting transistors. This resistance gives rise to random voltage fluctuations across the conduction channel. A MOS switch can hence be modelled by an ideal switch connected in series with a resistor and a voltage source as depicted in Figure 1-3. The resistor R_{ON} represents the 'ON' resistance of the switch. The voltage source models the thermal noise with a two sided power spectral density (PSD), $S_N(f)$, where [8]

$$S_N(f) = 2KTR_{ON} \quad (1-5)$$

The noise of an op amp can be modelled as an ideal op amp with a noise source at one of its input terminals. The PSD of the noise source generally follows the shape as given in Figure 1-4. The overall spectrum can be divided into two regions. $1/f$ noise, often referred to as flicker noise, dominates at low frequencies while thermal noise is more significant at high frequencies.

The $1/f$ noise is related to the surface states that exist at the Si/SiO₂ interface of a MOSFET. These energy states trap and release carriers from the channel, causing current fluctuation. The charging

Figure 1-3 A CMOS switch and its equivalent noise model

Figure 1-4 Typical op amp input referred noise spectrum

and discharging of these states is a slow process, and hence the effect is more prominent at low frequencies. The location of F_K in Figure 1-4 depends on the fabrication process, and the op amp circuit. In a modern CMOS technology this frequency lies in the 1 KHz to 50 KHz range [8]. The $1/f$ noise of a MOSFET is almost independent of biasing conditions and can be approximated by the following simplified model [8]:

$$S_{N1/F}(f) = \frac{K}{C_{OX}WLf^n} \quad (1-6)$$

where K is a process dependent empirical parameter, C_{OX} is the gate oxide, n is the slope factor that lies in the range of 0.8 to 1.2, and W and L are the width and length of the device respectively.

The thermal noise of the op amp is due to the random thermal motion of carriers in the conduction channel of MOSFETs. Similar to the thermal noise of a resistor, this noise has a constant white spectrum. For a transistor in saturation, the PSD of thermal noise can be expressed in terms of its transconductance g_m [8]:

$$S_{NT}(f) = \frac{8}{3} \frac{KT}{g_m} \quad (1-7)$$

The complete noise model of the SC integrator of Figure 1-2 is given in Figure 1-5. All switches have been replaced by the noise model of Figure 1-3, and the input referred $1/f$ and thermal noise of the op amp are included. It can be seen that while switch S_1 is closed, C_R is charged to the input voltage, with the noise voltage V_{N1} superimposed. When S_2 is closed during ϕ_2 , both the input and the

Figure 1-5 Complete time-variant noise model of SC integrator

noise signal are transferred to the integrating capacitor C_I . Because the noise signal is sampled, it represents a discrete time signal. Its transfer function to the output is then the z domain transfer function from C_R to the output. In other words, the sampled noise reaches the output by way of a sampled-data path. Noise can also reach the output directly. For example, S_2 is open during ϕ_1 , and the op amp with the feedback capacitor C_I behaves like a voltage follower for high frequency noise from $V_{N1/F}$ and V_{NT} . Each of the four noise sources can contribute to the overall noise through either direct path or sampled-data path, or both. The relative significance of each component varies with circuit parameters. A generalized methodology will be developed in this thesis to aid in the analysis of noise performance of SC circuits which are subject to the noise mechanisms summarized here.

1.4 Thesis Organization

Some basic insight into the area of noise analysis in SC circuits has been given in this chapter. In Chapter 2, more detailed discussions on the modelling of various noise sources will be provided. Based on the understanding of the nature of the noise sources developed in Chapter 2, Chapter 3 presents a methodology for the simulation and analysis of random noise in SC circuits. Experimental data that support simulation results are reported in Chapter 4. In Chapter 5, the technique of Correlated Double Sampling as a means of improving dynamic range, together with some experimental results, will be discussed. Finally, conclusions and recommendations for future work are presented in Chapter 6.

Chapter 2

Random Noise in Switched-Capacitor Circuits

2.1 Introduction

In this chapter, the fundamental concepts of random noise in SC circuits are reviewed. The discussions will provide the background knowledge necessary to deal with the more subtle issues of modelling such noise in circuit simulators to be presented in the next chapter.

The output noise of a SC circuit has three main origins: op amps, switches, and power supplies. An op amp is a network of MOSFETs so its noise behavior can best be understood by studying the noise of individual MOSFETs. Noise from switches represents broadband thermal noise due to the finite 'ON' resistance of MOS transistors. Unlike op amp noise and switch noise, power supply noise is not generated internally. The finite impedance of power supply lines transforms changes in supply current into supply voltage fluctuations. This noise gets coupled into the signal path, degrading the signal to noise ratio. Although internally generated noise is the main subject of interest in this thesis, all three components will be discussed in this chapter.

2.2 The Representation of Random Noise

Random noise in circuit elements causes fluctuations in certain circuit parameters (voltage at a node, current through a branch) that are continuous in the time domain. This noise signal, $V_N(t)$, has

infinite energy but a finite time-average of energy, i.e. power. The spectral density of such a random signal is represented by its power spectral density function (PSD), $S_N(f)$. This function is in units of power over frequency: in square volts per Hertz (V^2/Hz) or square amperes per Hertz (A^2/Hz) if normalized to the power of a one ohm resistor. The mean square power of the signal is obtained by integrating the function over the entire frequency spectrum. Mathematically,

$$\overline{V_N^2(t)} = P_N = \int_{-\infty}^{\infty} S_N(f) df \quad (2-1)$$

and the RMS voltage of the signal is simply the square root of the above. $S_N(f)$ describes the relative power contribution at various frequencies and forms the basis for meaningful measurements of noise signals. In this thesis, the noise signal $V_N(t)$ is assumed to represent fluctuations in voltage, so $S_N(f)$ has units of V^2/Hz . For noise sources that are uncorrelated, their PSDs are added together to obtain the total noise contribution.

2.3 Noise in MOSFETs

Noise in MOSFETs is mainly generated by two distinct mechanisms that can be considered separate noise sources: $1/f$ noise and thermal noise. These noise sources were briefly described in Chapter 1 and simple models were presented. In the following sections more detailed discussion on the origin and modelling of these noise sources will be provided.

2.3.1 1/f Noise of MOSFETs

The low frequency noise behavior of a MOS transistor is generally dominated by 1/f noise (Fig. 1-4). Many theories have been proposed to explain the origin of this noise [9,10,11,12] and the most widely accepted is the 'tunnelling' theory.

The Si/SiO₂ interface under the gate of a MOSFET gives rise to energy states that are energetically distributed in the semiconductor band gap, referred to as surface states. Mobile carriers in the conducting channel communicate with these states via a capture and generation process obeying Shockly-Reed Hall statistics [11]. These carriers then tunnel into and out of traps that are located in the oxide near the interface. The interaction between carriers in the interface states and the oxide traps is the dominant process responsible for variations in the number of carriers in the channel. This in turn contributes to fluctuations in drain current which can be modelled as a noiseless transistor with a noise voltage source at its gate.

The frequency spectrum of this noise is determined by the characteristic time constant, which is related to a discrete trap energy level within the semiconductor band gap. Moreover, the probability of carriers being trapped depends exponentially on the distance of the traps in the oxide. The distribution of traps within the oxide layer and the distribution of trap energy levels in the band gap provide a wide range of time constants. This wide dispersion of time constants is responsible for the 1/f spectral distribution.

A $1/f$ noise model is incorporated in the continuous time circuit simulator that will be used to perform noise analysis in Chapter 4. This model, which is based on the 'tunnelling' theory, is more elaborate than the simple model of equation 1-6. It supports the temperature and bias dependent nature of experimental noise data. The formulation of the model is quite involved and the reader is directed to the reference [12] for the full derivation. Basically, the spectral intensity of the fluctuation in the total number of trapped carriers is first derived from quantum statistics. The variance in the number of carriers is then transformed to reflect the variance in the drain current, and consequently the variance in the gate voltage. The transformation involves the drain current and the total mobile charge in the channel, resulting in a bias dependent model. In addition, ~~model parameters~~ like density of surface states, effective distance of traps from the interface, and surface mobility of carriers provide further temperature and bias dependence of the model.

2.3.2 Thermal Noise in MOSFETs

In a real resistor, the electrons are constantly in random thermal motion. Even in the absence of an external circuit, a noise voltage will appear across the resistor. Basic thermodynamics dictates that the noise spectrum is white with a two-sided power spectral density of [8]

$$S_N(f) = 2KTR \quad (2-2)$$

where

K = Boltzmann's constant

T = absolute temperature in degrees Kelvin

R = resistance in ohms

Thermal noise in MOSFETs is due to the random thermal motion of free carriers in the conduction channel. Analogous to the thermal noise of a real resistor, the thermal noise of a MOSFET is proportional to the resistance between the source and drain terminals, which can be expressed in terms of the transconductance (g_m) of the device. Since g_m is bias dependent, the thermal noise of a MOSFET also varies with bias conditions. In the circuit simulator that will be used to perform noise analysis, the thermal noise model developed by Klassen and Prins [13] is used. Again the reader is directed to the reference for the full model. In its simplified form, the thermal noise PSD is modelled as follows:

$$S_N(f) = 2KTR_{ON} \quad (2-3)$$

where

$$R_{ON} = \frac{\beta}{g_m} f(V_G, V_D, C_{OX}, N_A)$$

$f(V_G, V_D, C_{OX}, N_A)$ is a complex function of gate voltage, drain voltage, gate capacitance, and substrate doping. g_m is the transconductance and β is a fitting parameter for model calibration. The combination of $f(V_G, V_D, C_{OX}, N_A)$ and g_m tracks the bias dependent nature of thermal noise.

2.4 Switched-Capacitor Resistor Noise

It was mentioned in Chapter 1 that thermal noise due to the 'ON' resistance of switches is sampled and superimposed on the

signal in a SC circuit. In general, broadband noise that is sampled on a switched-capacitor and transferred to the output as a discrete time signal is also referred to as switched-capacitor resistor (SCR) noise.

2.4.1 Band-Limited Thermal Noise

The noise model of a MOS switch has been introduced in Chapter 1. Figure 2-1a shows the circuit of a simple switched-capacitor stage. The noise model of the circuit with its input shunted to ground and the switch closed is given in Figure 2-1b. The broadband thermal noise source $V_N(t)$ due to the 'ON' resistance of the switch causes voltage fluctuations $V_{NO}(t)$ to appear across C . The 'ON' resistance and the capacitor C form a low pass filter which acts on $V_N(t)$. Assuming that the bandwidth of $V_N(t)$ is infinite, the PSD of $V_{NO}(t)$, is then

$$S_{NO}(f) = S_N(f)|H(f)|^2 \quad (2-4)$$

where

$$S_N(f) = 2KTR_{ON}$$

$$H(f) = \frac{1}{1 + j2\pi fR_{ON}C}$$

$H(f)$ represents the transfer function of the RC filter. The low pass filtering action band-limits the noise signal $V_N(t)$. The mean square noise signal at the output from equation 2-1 is therefore

$$\overline{V_{NO}^2(t)} = \int_{-\infty}^{\infty} S_{NO}(f) df$$

Figure 2-1a A simple switched-capacitor stage

Figure 2-1b Noise model with grounded input

$$\begin{aligned}
 &= \int_{-\infty}^{\infty} \frac{(2KTR_{ON})}{(1 + (2\pi fR_{ON}C)^2)} df \\
 &= \frac{KT}{C}
 \end{aligned} \tag{2-5}$$

The result indicates that the noise power is independent of the 'ON' resistance of the switch. This can be explained by the fact that while $S_N(f)$ is directly proportional to R_{ON} , the bandwidth of the RC filter is inversely proportional. These two effects cancel, yielding the above result.

2.4.2 Equivalent Noise Bandwidth

The PSD of an ideal thermal noise source is constant throughout the entire spectrum. In reality, physical conditions such as RC filtering due to non-ideal circuit elements as described in the previous example band-limit the available noise. The PSD function of an ideal band-limited white noise source is depicted in Figure 2-2a. The power of the noise signal is therefore,

$$\begin{aligned}
 P_N &= \int_{-\infty}^{\infty} S_N(f) df \\
 &= \int_{-B_N}^{B_N} 2KTR df \\
 &= 4KTRB_N
 \end{aligned} \tag{2-6}$$

where B_N is the finite noise bandwidth. The PSD function of a first order low pass filtered white noise is given in Figure 2-2b. This noise

Figure 2-2a PSD of an ideal band limited noise signal

Figure 2-2b PSD of a first order low pass filtered noise signal

Figure 2-2c Equivalent noise bandwidth of a first order low pass filtered noise signal

is essentially band-limited, since most of the energy is concentrated at the low frequencies. It is often easier to represent the PSD function of such a signal as if it were an ideal band-limited noise. This is accomplished by defining an equivalent noise bandwidth B_N , such that the area under the rectangular spectral density function is equal to that of the case of a first order low pass filtered signal, as illustrated in Figure 2-2c [14]. For the RC low pass filtered noise of Figure 2-1b, the equivalent noise bandwidth can be determined by equating equations 2-5 and 2-6:

$$\begin{aligned} B_N &= \frac{KT}{C} \frac{1}{4KTR_{ON}} \\ &= \frac{1}{4R_{ON}C} \text{ Hz} \end{aligned} \quad (2-7)$$

It is important to note that B_N is in units of Hertz, despite the $1/RC$ factor which may suggest units of radians per second. The cutoff frequency of a low pass filter, f_C , is expressed as

$$f_C = \frac{1}{2\pi RC} \text{ Hz}$$

The translation factor between the cutoff frequency of a first order RC filter and the equivalent bandwidth is then

$$\begin{aligned} k &= \frac{f_C}{B_N} \\ &= \frac{2}{\pi} \end{aligned} \quad (2-8)$$

Although the derivation of this conversion factor is based on a first order RC filtered noise, it can be applied to determine the equivalent

noise bandwidth of white noise band-limited by other mechanisms with first order roll off.

2.4.3 Sampling of Band-Limited White Noise

Discussion in the previous section revealed that thermal noise reaching switched-capacitors is band-limited due to the finite 'ON' resistance of switches. The bandwidth of the noise is governed by the $R_{ON}C$ time constant, where C is the value of the switched-capacitor. In a practical SC circuit, this time constant has to be much less than the sampling period of the circuit, so as to provide enough settling time for signal transients. Thus the noise bandwidth with the switch closed is much greater than the sampling frequency. This leads to extensive aliasing of this noise, which increases the noise spectral density. In sampling theory, the condition when the bandwidth of a signal being sampled is greater than half the sampling frequency is defined as undersampling.

In addition to thermal noise from switches, op amp thermal noise also reaches switched-capacitors through continuous signal paths. This noise is also broadband in nature and is band-limited by the unity gain bandwidth (UGBW) of an op amp. Due to similar transient settling requirements, the UGBWs of op amps in a SC circuit are also much higher than the sampling frequency. When this band-limited noise is sampled, aliasing again takes place as a result of undersampling.

The PSD of an undersampled band-limited white noise will now be derived. Consider the general model of a sample and hold system

as illustrated in Figure 2-3a. A signal $f(t)$ is sampled by an ideal train of impulses. The sampled discrete time signal $f_D(nT)$ then goes through a linear time-invariant filter with an impulse response $g(t)$ as shown in Figure 2-3b. The resulting output signal $f_{SH}(nT)$ is a series of pulses having the same shape as $g(t)$. The amplitude of each pulse is proportional to sampled value of $f_D(nT)$. In the frequency domain, the spectrum of the output pulse train is the product of the spectrum of the ideally sampled signal $f_D(nT)$ and the frequency transfer function of the hold function filter $G(f)$. If we denote the Fourier transform of $f_D(nT)$ and $f_{SH}(nT)$ as $F_D(f)$ and $F_{SH}(f)$ respectively, then

$$F_{SH}(f) = F_D(f) G(f) \quad (2-9)$$

From sampling theory, the spectrum of a ideally sampled signal is the infinite sum of spectral replicas of the original signal, i.e.

$$F_D(f) = \sum_{k=-\infty}^{\infty} F(f - kf_s) \quad (2-10)$$

where $F(f)$ is the Fourier transform of the input signal $f(t)$ and f_s is the sampling frequency. The transfer function of the hold function filter is the Fourier transform of $g(t)$, or

$$G(f) = (\tau/T) \text{sinc}(\pi\tau f) \quad (2-11)$$

When dealing with noise, power is usually the quantity of interest. Combining the last two equations, in terms of power,

$$|F_{SH}(f)|^2 = \left| \sum_{k=-\infty}^{\infty} F(f - kf_s) \right|^2 (\tau/T)^2 \text{sinc}^2(\pi\tau f) \quad (2-12)$$

Figure 2-3a Model for a Sample and Hold Circuit

Figure 2-3b Impulse response of hold function filter $G(f)$

Now let us consider the PSD of an ideally sampled band-limited white noise of noise bandwidth $B_N = 2f_S$. Figure 2-4a depicts the location of the spectral replicas according to equation 2-10. The effect of undersampling is illustrated in Figure 2-4b by stacking all spectral replicas. Since the noise due to the frequency shifted replicas are uncorrelated, power terms rather than voltage terms are added in computing the overall PSD. In this case, over the entire spectrum, the PSD of the sampled signal is increased by a factor of three. In general, it can be shown that the PSD of an ideally undersampled band-limited white noise with a PSD of S_N and bandwidth of B_N is [15]

$$S_{NS}(f) = \sum_{k=-\infty}^{\infty} S_N(f - kf_S) = S_N \frac{2B_N}{f_S} \quad (2-13)$$

The term $(2B_N/f_S)$ is considered the 'foldover' factor due to undersampling. Substituting the above into equation 2-12 we get the PSD of a sampled-and-held white noise:

$$S_{NSH}(f) = S_N \frac{2B_N}{f_S} (\tau/T)^2 \text{sinc}^2(\pi\tau f) \quad (2-14)$$

The above expression was derived assuming a ideal band-limited white noise source (Figure 2-2a). The spectral density of a sampled first order low pass filtered white noise has been studied [16]. Figure 2-5 shows the circuit used in the analysis. The output signal $V_{NSH}(t)$ is a sampled-and-held version of $V_N(t)$, a first order low pass filtered white noise. The PSD of $V_{NSH}(t)$, $S_{NSH}(f)$, is obtained

Figure 2-4a Spectral replication due to sampling

Figure 2-4b PSD of undersampled signal

Figure 2-5 Circuit model for analysis of sampled first order low pass filtered noise spectrum

by taking the Fourier transform of the autocorrelation function of $V_{NSH}(t)$:

$$S_{NSH}(f) = S_N \frac{(\pi f_C / f_S) \sinh(2\pi f_C / f_S)}{\cosh(2\pi f_C / f_S) - \cos(2\pi f / f_S)} (\tau / T)^2 \text{sinc}^2(\pi \tau f) \quad (2-15)$$

where

S_N = PSD of $V_N(t)$ at DC

$$f_C = \frac{1}{2\pi RC} \text{ Hz}$$

For undersampling cases, $f_C / f_S \gg 1$, the $\cos(2\pi f / f_S)$ term becomes negligible compared to $\cosh(2\pi f_C / f_S)$, and the equation reduces to :

$$S_{NSH}(f) = S_N (\pi f_C / f_S) (\tau / T)^2 \text{sinc}^2(\pi \tau f) \quad (2-16)$$

Rewriting in terms of equivalent noise bandwidth B_N yields

$$S_{NSH}(f) = S_N \frac{2B_N}{f_S} (\tau / T)^2 \text{sinc}^2(\pi \tau f) \quad (2-17)$$

which is exactly the same as equation 2-14. This illustrates the validity of the concept of equivalent bandwidth in the modelling of first order low pass filtered white noise.

If we consider again the special case of the sampling of band-limited white noise of Figure 2-1b, where the sample is held for the entire period, i.e. $\tau = T$, as in the case of sampled noise appearing at the output of a SC circuit, then

$$S_{NSH}(f) = (2KT R_{ON}) \frac{2}{4R_{ON}Cf_S} \text{sinc}^2(\pi f / f_S) \quad (2-18a)$$

$$= \frac{KT}{f_s C} \text{sinc}^2(\pi f/f_s) \quad (2-18b)$$

In the baseband, $-f_s/2 < f < f_s/2$, the sinc function is almost constant at unity, so the PSD is approximately constant, hence

$$S_{NSH}(f) \approx \frac{KT}{f_s C} \quad (2-19)$$

The power of the sampled noise signal in the baseband, can be obtained by integrating $KT/f_s C$ from $-f_s/2$ to $f_s/2$. This yields

$$\begin{aligned} P_N &= \int_{-f_s/2}^{f_s/2} (KT/f_s C) df \\ &= \frac{KT}{C} \end{aligned} \quad (2-20)$$

which is exactly the same as equation 2-4. Thus aliasing due to the undersampling of broadband noise concentrates the full noise power of the noise source into the baseband. This represents a fundamental limit to the achievable dynamic range of a SC circuit [17]. It is clear that for good dynamic range, large capacitors should be used. However, this increases the overall chip area and increases time constants, which contradicts the requirement for high speed circuits. Because of the KT/C relationship, switched-capacitor resistor noise is often referred to as KT/C noise.

2.4.4 Continuous Time Equivalent Noise Model of a Switched-Capacitor Resistor

Consider the noise due to switches only in a SC integrator as given in Figure 2-6a. The noise sources V_{N1} and V_{N2} are uncorrelated

Figure 2-6a Time variant noise model of SC integrator

Figure 2-6b Noise model during ϕ_2

Figure 2-6c Noise model during ϕ_1

so their contributions to the output can be evaluated separately. The output noise consists of two components: a direct broadband noise due to V_{N2} while $S2$ is closed and a sampled-and-held component due to both sources. Noise source V_{N1} does not contribute to the direct broadband noise because no direct path exists. In the calculation of the total output noise PSD an ideal (infinite bandwidth) op amp is assumed. This assumption greatly simplifies the mathematics involved but produces a slightly higher output noise estimate. The effects of this assumption will be discussed in Chapter 3.

Direct noise from V_{N2} only reaches the output during $\phi2$ (Figure 2-6b). The PSD of this noise component at the output can be derived in a straight-forward manner [31]:

$$S_{NOD}(f) = 2KTR_{ON}(C_R/C_I)^2(\tau/T) \quad (2-21)$$

where $2KTR_{ON}$ is the PSD of V_{N2} , (C_R/C_I) is the voltage gain from V_{N2} to the output and τ/T is the duty cycle of $\phi2$.

The PSD of sampled-and-held noise at the output is obtained by multiplying the sum of the PSDs of sampled-and-held noise stored on C_R due to V_{N1} and V_{N2} by the square of the transfer function from C_R to the output. The transfer function can be obtained by first writing the difference equation representing the integrator:

$$V_{OUT}(n) = V_{OUT}(n-1) - (C_R/C_I) V_{IN}(n - \frac{1}{2})$$

then transforming into the z domain:

$$V_{OUT} = V_{OUT} z^{-1} - (C_R/C_I) V_{IN} z^{-1/2}$$

$$V_{OUT}(1 - z^{-1}) = - (C_R/C_I) V_{IN} z^{-1/2}$$

Rearranging,

$$H(z) = - (C_R/C_I) \frac{z^{-1/2}}{1 - z^{-1}} \quad (2-22)$$

The transfer function in the continuous frequency domain can then be obtained by evaluating $H(z)$ on the unit circle:

$$H(\omega T) = - (C_R/C_I) \frac{e^{j\omega T/2}}{1 - e^{j\omega T}}$$

and

$$|H(\omega T)|^2 = (C_R/C_I)^2 \frac{1}{4 \sin^2(\omega T/2)} \quad (2-23)$$

Source V_{N1} is connected to C_R during $\phi 1$ and sampling occurs at the end of $\phi 1$. The noise model of the integrator during $\phi 1$ (Figure 2-6c) is exactly the same as the example of Figure 2-1b. The PSD of sampled-and-held noise stored on C_R due to V_{N1} is therefore given by equation 2-18b. Substituting $\omega = 2\pi f$, and $T = 1/f_s$,

$$S_{NSH1} = \frac{KT}{f_s C_R} \text{sinc}^2(\omega T/2) \quad (2-24)$$

Noise from V_{N2} is sampled-and-held on C_R at the end of $\phi 2$ (Figure 2-6b). If the op amp in the circuit has infinite gain and bandwidth, node A is a virtual ground and the PSD of noise sampled on C_R due to V_{N2} will be exactly the same as that due to V_{N1} . Therefore,

$$S_{NSH2} = S_{NSH1} = \frac{KT}{f_S C_R} \text{sinc}^2(\omega T/2) \quad (2-25)$$

The PSD of sampled-and-held noise at the output is then, according to equations 2-23 to 2-25:

$$\begin{aligned} S_{NOSH} &= (S_{NSH1} + S_{NSH2})|H(\omega T)|^2 \\ &= \frac{2KT}{f_S C_R} \text{sinc}^2(\omega T/2)(C_R/C_I)^2 \frac{1}{4\sin^2(\omega T/2)} \end{aligned}$$

and since

$$\text{sinc}^2(\omega T/2) = \frac{\sin^2(\omega T/2)}{(\omega T/2)^2}$$

after substitution and reduction,

$$S_{NOSH} = \frac{2KTf_S C_R}{(\omega C_I)^2}$$

Furthermore, substituting equation 1-3, $R_{EQ} = 1/f_S C_R$,

$$S_{NOSH} = \frac{2KTR_{EQ}}{(\omega R_{EQ} C_I)^2} \quad (2-26)$$

Now we can combine equations 2-21 and 2-26 to yield the overall PSD of noise at the output of the integrator due to switches only:

$$\begin{aligned} S_{NOUT} &= S_{NOD} + S_{NOSH} \\ &= 2KTR_{ON}(C_R/C_I)^2(\tau/T) + \frac{2KTR_{EQ}}{(\omega R_{EQ} C_I)^2} \end{aligned} \quad (2-27a)$$

Since $R_{EQ} \gg R_{ON}$ and $1/\omega R_{EQ} C_I \gg 1$ within the passband of the integrator, the sampled-and-held term dominates. We can therefore ignore the direct component in modelling switched-capacitor resistor noise. Rewriting the above,

$$S_{\text{NOUT}} = 2KT R_{\text{EQ}} \frac{1}{(\omega R_{\text{EQ}} C_I)^2} \quad (2-27b)$$

Equation 2-27b is expressed as the product of two terms. The first term is analogous to the PSD of a 'noisy' resistor of value R_{EQ} . The second term resembles the square of the transfer function of a continuous time integrator with time constant $R_{\text{EQ}} C_I$. This implies that the random noise of a SC integrator due to its switches can be modelled as a continuous time integrator with time constant $R_{\text{EQ}} C_I$ and a noise source with PSD of $2KT R_{\text{EQ}}$ at its input as shown in Figure 2-7.

In the development of the continuous time noise model, the simple parallel SC integrator of Figure 1-2b, as it has been implemented in early SC realizations, was used. The major drawback of the circuit is the high sensitivity of its frequency response to stray capacitances of the switches [18]. In recent practical SC filters, the stray free integrator [19] of Figure 2-8 is used as the basic building block. During each clock phase, two transmission gates are switched simultaneously to transfer charge. The noise model of the inverting stray free integrator with grounded input is given in Figure 2-9a. This model is obtained by replacing each switch with the series combination of an ideal switch, a resistor and a noise source, as in the parallel SC integrator case.

At the end of $\phi 1$, when both S1 and S2 open, noise due to both switches (V_{N1} and V_{N2}) will be sampled. Similarly at the end of $\phi 2$, V_{N3} and V_{N4} are sampled simultaneously on C_R . Since all these noises are uncorrelated and that each pair has the same continuous time

$$S_{NEQ} = 2KTR_{EQ}$$

Figure 2-7 Continuous time equivalent noise model of SC integrator

Figure 2-8 Stray free switched-capacitor integrator

Figure 2-9a Time variant noise model of stray free SC integrator

Figure 2-9b Noise model of stray free integrator during ϕ_2

Figure 2-9c Noise model of stray free integrator during ϕ_1

transfer function to C_R , the effects of each pair of noise sources can be lumped together. The equivalent circuits during ϕ_1 and ϕ_2 are presented in Figure 2-9b and 2-9c respectively. These noise models are essentially the same as those presented for the parallel integrator, except for the value of the 'ON' resistance and the associated noise source PSD. It was established previously that the continuous time model of a switched-capacitor resistor is independent of the 'ON' resistance. Therefore, the continuous time noise model of Figure 2-7 also applies to stray free SC integrators.

Despite the sampled-data nature of a SC integrator, and the fact that thermal noise of switches is aliased due to undersampling, the continuous time noise model of a switched-capacitor resistor is remarkably simple. In the absence of noise from the op amp, the noise can be modelled by the thermal noise of the continuous time resistor that the SC circuit is emulating. Since most circuit simulators support the modelling of resistor noise, one obvious approach to noise analysis of SC circuits is to replace all SC resistors by their continuous time equivalent, and then perform noise analysis of the transformed circuit. The subject of noise analysis of SC circuits will be discussed in Chapter 3.

2.5 Power Supply Rejection

In most applications, SC filters are integrated on the same chip with digital circuits or other analog circuits. A number of analog and digital signal currents can enter the supply lines. Since these lines have non-zero impedances, digital and analog noise will be

superimposed on the DC supply voltages. This noise will appear at the output of analog circuits, constituting cross talk and limiting the dynamic range. Due to the sampled-data nature of SC filters, high frequency supply noise will be aliased into the baseband, further degrading the performance.

Power supply rejection (PSR) is a measure of the ability of a circuit to reject power supply noise. It represents the extent to which power supply noise is attenuated before appearing at the circuit output. Power supply rejection ratio (PSRR) is the ratio of the open loop gain of a circuit $A(f)$ to the AC gain of power supply noise to the output. Mathematically,

$$\text{PSRR}(f) = \text{PSR}(f) A(f)$$

In a SC circuit, power supply noise can be introduced by three mechanisms: through op amps, capacitive coupling into high impedance nodes, and clock feedthrough via switches.

2.5.1 Op Amp Power Supply Rejection

The most likely path through which supply noise can be coupled to the signal is via the op amps. The PSRR of an op amp depends on its design and all practical op amps have finite PSR. At low frequencies, power supply noise is coupled the op amp mainly through the bias circuit, or due to asymmetries in the differential input stage [8]. At high frequencies, capacitive coupling is the dominant mechanism.

The circuit diagram of an internally compensated CMOS op amp is shown in Figure 2-10. The use of a supply independent bias voltage generator [8] greatly reduces V_{SS} noise coupled into the circuit through the current sources M5 and M7. Noise entering the circuit via M5 is common mode and propagates to the output with a low common mode gain. Noise entering via M7 is added to the signal and attenuated at the same rate as the signal by C_L since the noise output impedance is high. The PSRR for V_{DD} noise is much poorer. At moderate frequencies, the compensation capacitor C_C behaves like a short circuit and the output stage of the op amp can be modelled as shown in Figure 2-11a. Since the current through M6 is constant, $V_{GS6} = I_7/g_{m6}$ is also constant. The output impedance of M6 driving C_L is low. As the open loop gain of the op amp decreases at high frequencies, the output voltage follows the V_{DD} supply noise with unity gain. Hence the PSRR rolls off at the same rate as the open loop gain of the op amp.

The poor PSRR at high frequencies is undesirable for SC circuits. Broadband supply noise coupled to the output will be sampled and aliased back into the baseband. An effective technique for increasing the high frequency PSRR [20] is illustrated in Figure 2-11b. Cascode transistors M8 and M9 are added to the input stage. The compensation capacitor is therefore decoupled from the gate of M6. This approach reduces the common mode input range of the op amp and slightly increases the internally generated noise. Another approach is to use single pole amplifiers, which are compensated by their loading capacitance at the output. Having the dominant pole at

Figure 2-10 Conventional internally compensated CMOS op amp

Figure 2-11a Output stage of conventional op amp at high frequencies

Figure 2-11b Internally compensated CMOS op amp with improved PSRR

the output band-limits any noise that is coupled into the op amp. Both the signal and noise are attenuated at the same rate at frequencies beyond the pole frequency, thus maintaining a constant PSRR.

2.5.2 Coupling into High Impedance Nodes

The internal parasitic capacitances of an op amp in closed loop provide another mechanism for power supply noise injection in SC circuits. An op amp with an external feedback capacitor, as in a SC integrator, is shown in Figure 2-12. C_{GD} and C_{GS} denote the gate to drain and gate to source overlap capacitance of M1 respectively. Any voltage fluctuations at the drain or source of M1 due to power supply noise will be coupled into node A via C_{GS} and C_{GD} . At frequencies below the UGBW of the op amp, this node is held at virtual ground by feedback, serving as the charge summing node of the integrator. Power supply noise coupled to the output via C_{GS} and C_{GD} can be expressed as follows [21]:

$$\frac{dV_{OUT}}{dV_{DD}} = \frac{-1}{C_I} \left(C_{GD} \frac{\partial V_X}{\partial V_{DD}} + C_{GS} \frac{\partial V_Y}{\partial V_{DD}} \right) \quad (2-28a)$$

$$\frac{dV_{OUT}}{dV_{SS}} = \frac{-1}{C_I} \left(C_{GD} \frac{\partial V_X}{\partial V_{SS}} + C_{GS} \frac{\partial V_Y}{\partial V_{SS}} \right) \quad (2-28b)$$

and for the op amp of Figure 2-12 [26],

$$\frac{dV_{OUT}}{dV_{DD}} = \frac{C_{GD}}{C_I} \left(1 - \frac{\partial I}{\partial V_{DD}} \frac{1}{2g_{m3}} \right) \quad (2-29a)$$

$$\frac{dV_{OUT}}{dV_{SS}} = \frac{C_{GS}}{C_I} \left(\frac{\partial V_{T1}}{\partial V_{SS}} + \frac{\partial I}{\partial V_{SS}} \frac{1}{2g_{m1}} \right) \quad (2-29b)$$

Figure 2-12 Power supply noise coupling into virtual ground of integrator

where g_{mi} and V_{Ti} represent the transconductance and threshold voltage of transistor M_i respectively. These equations imply that the PSR of the integrator can be improved by using a power supply independent current source to bias the input stage. The first term of equation 2-29b models the threshold voltage variations of M_1 due to substrate noise. This factor can be eliminated by placing the input devices in a separate well. This is only possible, however, if the input pair is NMOS in a P-well process, or PMOS in a N-well process. By tying the well potential to the source potential, the substrate is isolated from the power supplies. The threshold voltage fluctuations due to supply noise are thus eliminated. With the use of a supply independent current source, the only path for V_{DD} noise injection is via the drain of M_3 and C_{GD} . The effects can be minimized by making the ratio of C_{GD}/C_I as small as other constraints will allow. The situation can also be improved by using cascode devices in the input stage as illustrated in Figure 2-11b.

Parasitic capacitances between the virtual ground node and the supplies provide another path of noise injection. In Figure 2-12, the parasitic junction capacitance of the drain/source diffusion of switch M_9 , together with stray capacitances between lines connected to the virtual ground and the supply lines (including substrate) is lumped together as C_P . In classical CMOS clock buffer design, the high and low clock levels are obtained by shorting the clock signal to V_{DD} and V_{SS} respectively. The gate to drain/source overlap capacitance of switch M_9 thus serves as yet another route for power supply noise injection that can be included in C_P . A noise signal ΔV_N injects a

charge $\Delta Q = \Delta V_N C_P$ into node A. This charge is transferred to C_I and causes the output to change by $-(C_P/C_I)\Delta V_N$. The noise gain is therefore (C_P/C_I) .

Obviously, in designing SC filters, the ratio of C_P/C_I should be minimized. The use of large integrating capacitors and small switches is one solution, at the expense of silicon area and speed. Extreme care should also be taken in laying out SC circuits. Capacitors and lines connected to high impedance nodes should be shielded from substrate noise. Only the top plates of capacitors should be connected to high impedance nodes. Digital and analog circuits should be kept as far apart as practical, and if possible, separate power supply buses should be used.

2.5.3 Clock Feedthrough

Another non-ideal effect associated with the use of MOS transistors as switches in SC circuits is clock feedthrough. Consider the switch M_9 that passes charge from C_R to C_I in Figure 2-12. When the clock signal ϕ is high, the transistor is turned on and an inversion channel of carriers is formed underneath the gate. When the device is turned off, the carriers are dispersed, flowing either into the substrate, or to the source and drain. In general, the current flowing into the substrate is negligible [22]. The distribution of charge between the source and drain depends on the relative size of C_R and C_I , the fall time of the clock signal, and other factors. As the gate voltage falls below the threshold voltage, the channel is cut off and depleted of carriers. Only the overlap capacitance continues to inject

charge into C_I . In addition to coupling the clock signal to the output of the integrator, clock feedthrough causes DC offset and a shift in the frequency response of the integrator [17].

The switching off behavior of a MOS transistor in the circuit of Figure 2-13a has been analyzed [23]. Circuit models for the two phases of switching off: gate voltage above threshold and gate voltage below threshold, are depicted in Figure 2-13b and 2-13c respectively. It can be shown that for a slow transition from V_H to V_L , the switch-induced error ΔV_N approaches

$$\Delta V_N = \frac{C_{OL}}{C_L} (V_S + V_T - V_L) \quad (2-30)$$

and for a fast transient,

$$\Delta V_N = \frac{C_{OL}}{C_L} (V_S + V_T - V_L) + V_{HT} \frac{C_{OL} + C_{OX}}{C_L} \quad (2-31)$$

where

$$V_{HT} = V_H - V_S - V_T$$

In the case of slow falling rate, most of the charge has sufficient time to return to the low impedance source, so the error voltage is mainly due to the charge injected through C_{OL} after the transistor is turned off (Figure 2-13c). For a short fall time the channel disappears very quickly, and half the charge in the channel reaches C_L , contributing to additional error voltage. Since clock feedthrough is due to parasitic capacitance of MOS switches, the use of small switches is again recommended. For CMOS technology, trans-

Figure 2-13a Switching off of a MOS Transistor

Figure 2-13b Circuit model for $\phi > V_T$ Figure 2-13c Circuit for $\phi < V_T$

mission gates made up a pair of complementary devices connected in parallel provide first order charge injection cancellation. For high frequency filters, where large switches and small integrating capacitors are inevitable, fully differential circuit techniques, or active compensation schemes [24,25] may become necessary.

Chapter 3

Continuous Time Noise Analysis of SC Circuits

3.1 Introduction

In this chapter, the more detailed aspects of how random noise occurs in SC circuits will be studied. The methods of modelling such noise in a manner compatible with the use of readily available continuous time circuit simulation programs like SPICE will be presented. The limitations and applications of the approach will also be discussed.

There are two mechanisms by which internally generated noise in a SC circuit propagates to the output: direct coupling or sampled-data path. An exact noise analysis of a SC network, therefore, requires that both components be accounted for in the evaluation of the total output noise power. The contribution due to direct noise coupling can be evaluated in a straight-forward manner, using conventional continuous time circuit analysis methods [15,27]. Sampled-data techniques (z domain) can be used to analyze the discrete time sampled-and-held noise component.

A number of exact noise analysis methods for SC circuits has been reported in the last few years. The method proposed by Furrer and Guggenbuhl [28] uses the autocorrelation technique. The autocorrelation functions at the output due to each noise source, for both direct and discrete signal cases, are first calculated. The PSD of each component is then evaluated by taking the Fourier transform of

its autocorrelation function. The total output PSD is finally obtained by summing all individual contributions. Other methods use a combination of discrete and continuous time techniques [27,29,30], and they differ mainly in the way the PSD of sampled noise on a capacitor is obtained. In all cases, the analysis leads to the formulation of an analytic expression for the output noise.

3.2 Noise Analysis in Sampled-data Domain

Noise analysis of SC circuits can be performed using sampled-data techniques by assuming that the direct noise component at the output is negligible. The validity of this assumption was illustrated in the example of a SC integrator in Section 2.4.4. In most practical filters where the passband lies well below the sampling frequency, it is reasonable to consider only the sampled noise in performing noise analysis.

In a SC circuit, at the end of each clock phase, noise from various uncorrelated noise sources is sampled onto switched-capacitors. The noise sample on a capacitor represents a discrete time signal. The transfer of sampled noise from a capacitor to the output is described by the z domain transfer function from the capacitor to the output. If the PSD of the noise sampled on a capacitor is known, the output noise due to these samples can be obtained.

It was shown in Section 2.4.3 that the PSD of sampled first order low pass filtered white noise is constant and proportional to the 'foldover' factor for $f \ll f_s$. Undersampled broadband noise in a SC circuit can therefore be modelled as a baseband ($f < f_s/2$) noise

source of PSD as given in equation 2-13. This is very important to this thesis as it implies that noise analysis of SC circuits can be carried out using standard SC analysis programs that do not take into account aliasing effects.

The noise contribution at the output due to broadband noise sampled on a capacitor is obtained by multiplying the PSD of the noise samples by the magnitude square of the z domain transfer function evaluated on the unit circle ($z = e^{j\omega T}$). If we denote the PSD of noise sampled on capacitor C_j as S_{Nj} , $H_j(\omega T)$ as the z domain transfer function after the $z = e^{j\omega T}$ substitution, and S_{NOUTj} as the noise at the output due to S_{Nj} , then

$$S_{NOUTj} = S_{Nj} |H_j(\omega T)|^2 \quad (3-1)$$

Under the assumption that noise samples on different capacitors are uncorrelated, the PSD of total noise at the output, S_{NOUT} , can be defined as

$$S_{NOUT} = \sum_{j=1}^k S_{NOUTj} \quad (3-2)$$

where k is the total number of switched-capacitors. To obtain the mean square power, S_{NOUT} is integrated over the frequency range of interest. The analysis of $1/f$ noise of op amps is performed in a similar fashion. The PSD of the noise source is the input referred $1/f$ noise and the transfer function to the output is that from the positive input terminal. However, the procedure is complicated by the fact that the noise spectrum is now frequency dependent.

3.3 Noise Analysis in Continuous Time Domain

Most SC circuit analysis programs do not have a noise analysis capability. The calculation of source PSDs, the summation of individual contributions and the integration have to be done separately. For circuits where a large number of switched-capacitor resistors and op amps are used, the process can become very laborious, time consuming and error prone.

An alternative is to perform noise analysis in the continuous time domain using readily available circuit simulation programs like SPICE. By replacing all switched-capacitor resistors with their continuous time equivalent, the transfer function of the sampled noise charge from a capacitor to the output becomes the transfer function from the corresponding resistor to the output. The example of the SC integrator illustrates that analogy. The advantage of using a continuous time simulator is the built-in noise analysis capability. Noise due to switches and op amps can easily be simulated using models of resistor thermal noise, and MOSFET $1/f$ and thermal noise. In addition, the built-in noise analysis capability provides the total noise PSD at the output, and the integrated noise power over any frequency range, which also greatly simplifies the task of noise analysis.

The noise analysis method proposed in this thesis is based on the simulation of SC filters as continuous time active filters using the equivalent of SC resistors. The approach is different from a similar one published by Fischer [15] in that more accurate modelling of

aliased broadband noise is employed. In his approach, the PSD of the noise of a SCR is assumed to be $2KT R_{EQ}$. He also assumes that the broadband thermal noise of op amps is only sampled at the output of integrators. In practical filters, both assumptions are not necessarily true, as will be shown subsequently. The validity of the circuit model enhancements proposed in this chapter is supported by significantly improved agreement between simulation and measured data, presented in the following chapter.

3.4 Noise Analysis of SC Circuits using a Continuous Time Circuit Simulator

In the derivation of the continuous time noise model of a switched-capacitor resistor in Section 2.4.4, it was revealed that under certain assumptions the aliased thermal noise sampled on a switched-capacitor due to the 'ON' resistance of switches has the same PSD as the continuous time equivalent resistor (equation 2-27b). It was also indicated that for $f \ll f_s$, the transfer function of sampled noise from a switched-capacitor to the output is the same as that from the corresponding resistor to the output in the equivalent circuit. It can further be shown that for $f \ll f_s$, the transfer function from the positive terminal of the op amp in the SC integrator of Figure 1-2b is also the same as that in the continuous time case. This implies that the output fluctuations due to the $1/f$ noise of the op amp, which is usually significant for $f \ll f_s$, can also be simulated in the continuous time domain.

Up to this point, the discussion on noise has mainly been focused on the KT/C noise of switches and $1/f$ noise of op amps. There is another source of noise that also reaches the output via sampled-data signal paths: the broadband thermal noise of op amps. The noise model of a parallel SC integrator is presented in Figure 3-1 with the input referred thermal noise of the op amp shown as V_{N3} . Since the spectrum of this noise is white, its PSD is represented as $2KTR_{OA}$, where R_{OA} is the value of a 'noisy' resistor that has the same PSD as the input referred noise of the op-amp. Similar to the broadband noise of V_{N2} , the op amp thermal noise influences the output through both direct and sampled-data paths. The direct noise component at the output is considered negligible, for reasons given in the discussion of direct noise from V_{N2} in Section 2.4.4. We shall next consider the modelling of sampled op amp thermal noise.

During $\phi 2$, the switched-capacitor C_R is connected to the negative input of the op amp via $S2$ as shown in Figure 3-1b. The noise source V_{N2} has been omitted, since its contribution can be studied separately. Negative feedback forces the two input terminals of the op amp to be at the same potential so any noise at node A will also be seen at node B. The noise model can therefore be redrawn as shown in Figure 3-1c. V_{N3D} contributes to the direct noise component that we shall omit. V_{N3S} causes voltage fluctuations across C_R , and when $S2$ opens at the end of $\phi 2$, a noise sample will be left on C_R . This sample represents a discrete signal that will be transferred to the output via a sampled-data path. The situation is analogous to the sampling of noise due to $S2$ previously discussed. The resemblance

Figure 3-1a Time-variant noise model of SC integrator

Figure 3-1b Integrator op amp thermal noise model during $\phi 2$

Figure 3-1c Alternate op amp thermal noise model during $\phi 2$

can be observed by comparing Figure 3-1c to Figure 2-6b. Noise due to V_{N3S} reaching C_R is either band-limited by the UGBW of the op amp or the low pass filter formed by R_{ON} and C_R , depending mainly on the design of the op amp. Regardless, its bandwidth will be higher than the sampling frequency, and aliasing will take place. The PSD of the noise samples, S_{NOASH} , can hence be calculated using equation 2-17:

$$S_{NOASH} = 2KTR_{OA} \frac{2B_N}{f_s} \text{sinc}^2(\omega T/2)$$

where B_N is the corresponding noise bandwidth. For $f \ll f_s$, the PSD is almost constant and can be approximated by

$$S_{NOASH} \approx 2KTR_{OA} \frac{2B_N}{f_s} \quad (3-3)$$

Comparing the above equation to equation 2-13, the similarity between sampled switch and op amp noise suggests that the latter can also be simulated in the continuous time circuit context. The complete circuit model for the analysis of a SC integrator is given in Figure 3-2. Assuming that direct noise components are negligible, there are three noise sources: $V_{N1/F}$ represents the input referred 1/f noise of the op amp, V_{NSH} and V_{NOASH} model the undersampled broadband thermal noise due to switches and the op amp respectively. All three noise sources are uncorrelated, and V_{NSH} and V_{NOASH} have the same transfer function to the output.

Figure 3-2 Complete continuous time equivalent noise model of SC integrator

3.4.1 Modelling of Random Noise Sources for Continuous Time Noise Analysis

In the previous section the general approach of using continuous time circuit simulators to perform noise analysis of SC circuits was presented. For $f \ll f_s$, which is usually the frequency range of interest, it was shown that all significant noise sources inherent to a simple SC integrator can be modelled in the continuous time domain. The generalized implementation of noise models applicable to all SC circuits will be the subject of discussion in this section.

3.4.1.1 Modelling of Op Amp $1/f$ Noise

The spectrum of $1/f$ noise ideally extends from DC to infinity. This implies that for any finite sampling frequency the 'folding back' of high frequency spectral components into the baseband is inevitable. It has been shown that 'foldover' effects can be closely approximated by adding a constant to the presampled spectrum [15]. In most practical situations, this constant is negligible in the frequency range where $f \ll f_s$, due to the diminishing PSD at high frequencies. In this thesis, the aliasing effects are assumed to be negligible. The close agreement between simulated and measured results to be presented in Chapter 4 validates that assumption.

The $1/f$ noise of an op amp can be modelled in two ways in a continuous time circuit simulator. One way is to use a network of 'noisy' MOSFETs that represents the actual circuit implementation on

silicon. This method is accurate, provided that the $1/f$ noise and small signal models of MOSFETs are well calibrated. The main disadvantage is that for complicated circuits, where a large number of op amps are employed, the simulation time may become excessive. The alternative is to model the op amp and its $1/f$ noise using voltage controlled voltage sources (VCVS) [15] as shown in Figure 3-3.

VCVS1 together with R_P and C_P simulates an op amp having a one pole roll off with its gain function $A(f)$ described by:

$$|A(f)| = \frac{A}{\sqrt{1 + (2\pi f R_P C_P)^2}} \quad (3-4)$$

The value of C_P is chosen such that it is much larger than other capacitors in the filter circuit. VCVS2 and M1 are used to generate the input referred $1/f$ noise, which is AC coupled to VCVS1 via R_{AC} and C_{AC} . The size of M1 and the bias current I_B are chosen to produce the desired noise spectrum.

For designs that use a standard cell approach, where the noise behavior of a chosen op amp is well characterized, the latter approach is preferred. In the development of high performance SC circuits, each circuit element has to be optimized in order to achieve a certain design goal. In this case, the former approach is preferred. As the design of the op amp changes, so does the noise behavior. By modelling the op amp at the MOSFET circuit level, the resulting effects on the overall noise performance of the filter can be directly observed.

Figure 3-3 Modelling of op amp $1/f$ noise

3.4.1.2 Detailed Aspects of Aliased Broadband Thermal Noise.

Broadband thermal noise in a SC circuit has two origins: MOS switches and op amps. In both cases, the noise signal available for sampling onto a capacitor is first order low pass filtered during a particular clock phase. For switch thermal noise, the filtering is inherent in the implementation of switched-capacitors: the 'ON' resistance of a switch and the sampling capacitor form a first order low pass filter of high bandwidth. For op amp thermal noise, the frequency limitation is imposed by either the roll-off of the gain of the amplifier or the RC filtering of the switched-capacitor. In practical filters, transient settlement requires that the bandwidths of both frequency limitation processes exceed the sampling frequency. Consequently the sidebands of the undersampled noise signal are 'folded back' into the baseband, exaggerating the PSD of baseband noise. The spectrum of undersampled first order low pass filtered white noise was analyzed in Section 2-4. It was revealed that for $f \ll f_s$, the PSD of the sampled noise is approximately the product of the PSD of the presampled noise and a foldover factor:

$$S_{NSH} = S_N \frac{2B_N}{f_s} \quad (3-5)$$

In deriving the above equation, the presampled noise is band-limited by a passive low pass filter of unity DC gain. The situation is representative of the sampling of switch thermal noise by switched-capacitors. For op amp thermal noise, there may be a voltage gain between the noise source and the switched-capacitor. Consider Figure

3-4 where the output of the integrator is sampled by C_2 during the same clock phase as charge is transferred from C_1 to C_I . Input referred noise of the op amp appears across C_1 with unity gain. However, the noise signal propagates to C_2 with a gain of $(1+C_1/C_I)$. If the equivalent bandwidth of noise across C_2 is B_N , and the PSD of the op amp input referred noise is S_N , then the PSD of the sampled noise will become

$$S_{NSH} = S_N \frac{2B_N}{f_S} (1 + C_1/C_I)^2 \quad (3-6)$$

which differs from equation 3-5 by the extra gain factor $(1+C_1/C_I)^2$. We may generalize equation 3-5 to include cases where there is a voltage gain A from the noise source to the sampling capacitor:

$$S_{NSH} = S_N \frac{2B_N}{f_S} A^2 \quad (3-7)$$

This general equation describes the PSD of the sampled version of a band-limited thermal noise of equivalent bandwidth B_N , and a presampled PSD of S_N . In continuous time simulations, the expression represents the PSD of the noise source that is to be placed in series with the corresponding resistor.

In SC circuits, samples of aliased noise from different sources can be held on the same capacitor. The sampling can also occur at different clock phases, but all samples on the same capacitor are transferred to the output via the same transfer function. If we assume that noise samples from different sources are uncorrelated,

Figure 3-4 Sampling of op amp output noise

then for a switched-capacitor C_j , the PSD of samples due to k sources, S_{NSHj} is then

$$S_{NSHj} = \sum_{i=1}^k S_{Ni} A_{ji}^2 \frac{2B_{Nji}}{f_s} \quad (3-8)$$

where S_{Ni} , A_{ji} , and B_{Nji} represent the presampled PSD, voltage gain to C_j , and bandwidth as seen at C_j of noise source V_{Ni} , respectively. Referring back to the example of the simple SC integrator of Figure 3-1a where there is only one switched-capacitor, $k=3$, as C_R samples noise from V_{N1} , V_{N2} and V_{N3} . If we now assume that the op amp is ideal ($V_{N3} = 0$, infinite gain and bandwidth), then from equations 3-7 and 3-8,

$$\begin{aligned} S_{NSH} &= 2KTR_{ON} \frac{2B_{N1}}{f_s} + 2KTR_{ON} \frac{2B_{N2}}{f_s} \\ &= 2KTR_{EQ} \end{aligned} \quad (3-9)$$

which is the theoretical thermal noise of the equivalent input resistor. Realistically, integrated op amps are far from ideal. Finite gain and bandwidth, and the existence of noise, result in the deviation of the PSD of a SC resistor from the $2KTR_{EQ}$ model. The sampling of noise from V_{N1} during $\phi 1$ is independent of the op amp, so equation 3-5 holds. We have shown that in addition to noise from V_{N2} , op amp thermal noise is also sampled onto C_R during $\phi 2$. This has the effect of increasing the PSD of sampled noise by the amount as given in equation 3-3. The PSD of the noise samples from V_{N2} is equal to that expressed in equation 3-5 only if $B_{N2} = 1/(4R_{ON}C_R)$. This condition is only true if the UGBW of the op amp exceeds the cut off

frequency of the $R_{ON}C_R$ low pass filter. In practical filters, the bandwidth of the lowpass filter is designed to be wider than the UGBW of the op amp, to avoid distortion. The UGBW of the op amp therefore also band-limits noise from V_{N2} . This implies that equation 3-5 will overestimate the PSD of noise samples from V_{N2} .

Let us assume that the UGBW of the op amp is f_{UG} and that it band-limits the noise of V_{N2} and V_{N3} . If we further assume that f_{UG} corresponds to the cut off frequency of a first order low pass filter, then we can determine the equivalent noise bandwidth by applying the transformation of equation 2-8 so that

$$B_{N2} = B_{N3} = \frac{f_{UG}\pi}{2} \quad (3-10)$$

We can now apply equation 3-8 to determine the PSD of all sampled noise on C_R :

$$\begin{aligned} S_{NSH} &= 2KTR_{ON} \frac{2B_{N1}}{f_s} + 2KTR_{ON} \frac{2B_{N2}}{f_s} + 2KTR_{OA} \frac{2B_{N3}}{f_s} \\ &= \frac{4KT}{f_s} (R_{ON} B_{N1} + R_{ON} B_{N2} + R_{OA} B_{N3}) \end{aligned} \quad (3-11)$$

This equation shows the incorrectness of using $S_{NSH} = 2KTR_{EQ}$ to model the PSD of a SCR. How it compares to the $2KTR_{EQ}$ case depends on the circuit and the fabrication process. For more complex circuits, the number of terms in equation 3-8 will increase. Note that all terms in equation 3-11 are uncorrelated and all have white noise spectrum.

3.4.1.3 Modelling of Aliased Broadband Thermal Noise

Based on the discussions of the previous section, we can now propose a generalized way of accounting for the various broadband thermal noise components sampled on a switched-capacitor. The PSD of resulting noise samples on the switched-capacitor C_j can be expressed as

$$S_{NSH_j} = \gamma_j 2KTR_{EQ_j} \quad (3-12)$$

where γ_j is simply a weighting factor. This γ_j factor can be utilized to facilitate noise analysis using continuous time circuit simulators. The validation of such an approach is central to this thesis.

When a continuous time simulator is used to perform noise analysis of a continuous filter circuit, a noise source with a PSD of $2KTR_j$ is typically placed in series with each resistor R_j , and for each frequency point, the total noise at the output is calculated using

$$S_{NOUT}(f) = \sum_{j=1}^k (2KTR_j) |H_j(f)|^2 \quad (3-13)$$

where $H_j(f)$ is the transfer function from R_j to the output. The fact that the PSD of a SCR may differ from the ideal $2KTR$ model poses a problem in noise analysis of SC circuits. The equivalent resistance values, R_j , cannot be changed without altering the operation of the circuit. One solution is to place a voltage controlled voltage source in series with each resistor, similar to the modelling of $1/f$ noise using VCVSs (Figure 3-3). This method can be quite tedious for the user.

An alternative, followed here, is to modify the circuit simulator such that the PSD of any resistor can be changed by a constant scaling factor γ . The γ factor is passed to the simulator as an extra parameter which defaults to unity. In performing noise analysis, the PSD of resistor R_j becomes $\gamma_j 2KT R_j$. This method is preferred since the modification required is straight-forward to implement and it greatly simplifies the noise analysis process.

From equations 3-8 and 3-12,

$$\gamma_j = \frac{\sum_{i=1}^k S_{Ni} A_{ji}^2 \frac{2B_{Nii}}{f_s}}{2KTR_{EQj}} \quad (3-14)$$

Applying this to a SC integrator, using equation 3-11,

$$\begin{aligned} \gamma &= \frac{\frac{4KT}{f_s} (R_{ON} B_{N1} + R_{ON} B_{N2} + R_{OA} B_{N3})}{\frac{2KT}{f_s C_R}} \\ &= \frac{\frac{1}{2} (R_{ON} B_{N1} + R_{ON} B_{N2} + R_{OA} B_{N3})}{\frac{R_{ON}}{4C_R R_{ON}}} \end{aligned}$$

after making the substitution $B_N = 1/4R_{ON}C_R$ (equation 2-7),

$$\gamma = \frac{1}{2} \left(\frac{R_{ON} B_{N1}}{R_{ON} B_N} + \frac{R_{ON} B_{N2}}{R_{ON} B_N} + \frac{R_{OA} B_{N3}}{R_{ON} B_N} \right) \quad (3-15)$$

Each of the three terms is the product of two ratios. The first one is the ratio of equivalent noise resistance, while the second one is the ratio of noise bandwidth. Intuitively, each term represents the ratio

of the PSD of sampled noise due to a noise source to the PSD of sampled noise due to the 'ON' resistance of a switch. Since the PSD of sampled first order low pass filtered noise is proportional to the resistance and the noise bandwidth according to equation 3-5, the ratio of the PSDs is simply the ratio of resistances and bandwidths. We can rewrite equation 3-15 for the general case:

$$\gamma_j = \sum_{i=1}^k \frac{1}{2} \frac{R_i A_{ji}^2 B_{Nji}}{R_{ON} B_{Nj}} \quad (3-16)$$

or in terms of equivalent cut off frequencies (equation 2-8),

$$\gamma_j = \sum_{i=1}^k \frac{1}{2} \frac{R_i A_{ji}^2 f_{Cji}}{R_{ON} \frac{1}{2\pi R_{ON} C_j}} \quad (3-17)$$

For SC circuits that use stray free SCRs, a similar expression for the γ factors can be derived. In the stray free implementation, more switches are employed so the number of terms in equation 3-17 will increase accordingly. If R_{ON} denotes the 'ON' resistance of one switch, following the model of Figure 2-9a, it can be shown that the general expression for the γ factors becomes

$$\gamma_j = \sum_{i=1}^k \frac{1}{2} \frac{R_i A_{ji}^2 f_{Cji}}{2R_{ON} \frac{1}{4\pi R_{ON} C_j}} \quad (3-18)$$

All the variables in equations 3-17 and 3-18 except A_{ji} and f_{Cji} are fixed for a given design. A_{ji} is the gain from the noise source V_{Ni} within a particular clock phase, and f_{Cji} is the cut off frequency of the presampled noise signal due to V_{Ni} as seen at C_j during the same

clock phase. A_{ji} and f_{Cji} can be determined analytically for simple circuits or simulated within individual clock phases using a continuous simulator and the circuit topology within the corresponding clock phase. In the next section, a formalized two step approach to performing noise analysis on SC circuits will be presented. The approach will use continuous time circuit simulators at two levels, microscopically within each clock phase to determine A_{ji} and f_{Cji} , and macroscopically for the overall equivalent continuous filter.

3.4.2 A Novel Approach to Continuous Time Noise Analysis of SC Circuits

Based on the results of the previous section, a general approach for the continuous time noise analysis of SC circuits will be presented. The simple parallel SC integrator has been used extensively in the development of some of the concepts. In this section, a SC biquad filter (Figure 3-5) will be used to demonstrate the methodology. Besides being a more complicated circuit, the filter employs stray free SC integrators as building blocks. These changes are intended to illustrate that the approach can be applied to any SC circuits.

The basic idea is straight-forward. A SC circuit is translated to its continuous time equivalent by replacing each SCR with a resistor according to equation 1-3. For each resistor, a γ factor calculated from simulations within individual clock phases is passed to the circuit simulator to modify the PSD of the thermal noise due to that resistor.

Figure 3-5 A switched-capacitor biquad filter (Biquad A)

1/f noise of op amps is accurately modelled by simulating each op amp as a network of 'noisy' MOSFETs. Since the broadband thermal noise of the op amps reaching the output through direct signal paths is assumed negligible, the thermal noise model of MOSFETs should not be activated. The aliased component is accounted for by other means, within the γ factors. With the circuit translation to its continuous equivalent and with noise source modelling in place, noise analysis can now be carried out.

The key to the proposed approach lies with the evaluation of the γ factor associated with each SCR. Equations 3-17 and 3-18 imply that the knowledge of the bandwidths and voltage gains from various noise sources to each switched-capacitor is required. These parameters can be accurately obtained by means of continuous time simulations. Sampling occurs at the end of each clock phase, and the circuit topology is different during each clock phase. As a result, for the biquad filter of Figure 3-5 which is controlled by a two phase clock, two simulations are necessary. For each clock phase, the circuit model is obtained by substituting each opened switch with an open circuit, and replacing each closed switch with the series combination of a resistor and a signal source. The value of the resistor should correspond to the 'ON' resistance of the switch. A signal source is also added to the positive terminal of each op amp to complete the circuit. The two continuous time circuits for the example biquad are given in Figures 3-6a and 3-6b.

When one clock phase is active, conductive paths connect each switched-capacitor to a number of noise sources. For example, capa-

Figure 3-6a Noise model of biquad filter (Biquad A) during ϕ_1

Figure 3-6b Noise model of biquad filter (Biquad A) during ϕ_2

citor C_1 is connected to V_{N1} and V_{N4} during $\phi 1$; V_{N2} , V_{N3} , V_{N5} , V_{N8} and V_{N20} during $\phi 2$. Each of these noise sources causes voltage fluctuations across C_1 that will be sampled at the end of the corresponding clock phase. Not all noise sources will have significant influence on C_1 . Node A in Figure 3-6b is pinned at virtual ground by OA1 and the feedback capacitor C_{11} , so noise from V_{N5} and V_{N8} will have no effect on C_1 . However, all connected noise sources will be included in the simulations for completeness.

The biquad filter of Figure 3-5 has been implemented with a $1.5 \mu\text{m}$ CMOS technology. The circuit parameters are listed in Table 3-1. The simulated cut off frequencies, f_{Cji} , and voltage gains, A_{ji} are tabulated in Table 3-2. Using these values, we can calculate the value of γ_1 :

$$\gamma_1 = \frac{1}{2} \left(\frac{R_{ON}}{2R_{ON}} \frac{(442 + 141 + 141 + 442)}{442} + \frac{R_{OA}}{2R_{ON}} \frac{96.5}{442} \right)$$

$$= 1.3163$$

Similarly, the other γ factors have been calculated and the values are listed at the bottom of Table 3-2. All four γ factors are higher than unity, so one can infer that aliased op amp thermal noise is a significant contributor of output noise. The situation is more prominent for C_2 and C_4 , as indicated by the relatively higher γ values. This can be explained by the fact that thermal noise from both op amps are sampled by these capacitors. Moreover, gain factors of greater than unity are involved. In low noise filter designs, the γ factors should be optimized to be as low as possible. This can be accomplished by reducing the thermal noise of the op amp, as well as its UGBW in this example.

C_1	0.361 pF
C_2	1.083 pF
C_3	0.217 pF
C_4	0.217 pF
C_{I1}	1.083 pF
C_{I2}	1.444 pF
R_{ON}	500 Ohms
R_{OA}	6000 Ohms
f_{LG}	95 MHz
DC Gain	60 dB
f_S	900 KHz
$V_{DD} - V_{SS}$	5.0 Volts

Table 3-1 Biquad A circuit parameters

	C_1		C_2		C_3		C_4	
V_{Ni}	f_{C1i}	A_{1i}^2	f_{C2i}	A_{2i}^2	f_{C3i}	A_{3i}^2	f_{C4i}	A_{4i}^2
1	442M	1	-	-	-	-	-	-
2	141M	1	-	-	-	-	-	-
3	141M	1	-	-	-	-	-	-
4	442M	1	-	-	-	-	-	-
5	-	-	-	-	-	-	565M	1
6	-	-	-	-	-	-	665M	1
7	-	-	-	-	-	-	665M	1
8	-	-	-	-	-	-	565M	1
9	-	-	47M	1	45M	0.42	81M	0.42
10	-	-	147M	1	-	-	-	-
11	-	-	47M	1	45M	0.42	81M	0.42
12	-	-	147M	1	-	-	-	-
13	-	-	-	-	859M	0.76	-	-
14	-	-	-	-	735M	1	-	-
15	-	-	-	-	859M	0.76	-	-
16	-	-	-	-	735M	1	-	-
20	97M	1	48M	1.56	46M	0.66	96M	1
21	-	-	47M	1	52M	0.66	60M	3.26
	f_{C1}		f_{C2}		f_{C3}		f_{C4}	
	442M		147M		735M		735M	
	γ_1		γ_2		γ_3		γ_4	
	1.3163		3.1496		1.2195		2.2072	

Table 3-2 Biquad A simulated KT/C noise parameters

The continuous time equivalent of the biquad filter for noise analysis is shown in Figure 3-7. In calculating the resistor values, a clock frequency of 900 KHz is used. The switching scheme of equivalent resistor R_{EQ2} is such that it emulates an inverting resistance. As a result, an inverting buffer is placed between the output of OA1 and R_{EQ2} . The results of noise analysis using this circuit will be presented in Chapter 4.

3.5 Limitations and Applications

The soundness of the proposed approach to noise analysis of SC circuits depends mainly on the validity of the assumptions made. A summary of the assumptions is listed below:

- i) filter passband $\ll f_s$
- ii) all switches are identical
- iii) noise reaching output through direct paths is negligible
- iv) 'foldover' effects of $1/f$ noise are negligible
- v) all broadband noise sources are first order low pass filtered
- vi) all noise from different sources are uncorrelated
- vii) aliased components of noise reflected to the baseband are uncorrelated
- viii) noise samples on different capacitors due to the same noise source are uncorrelated

In most practical filters, the assumptions i) through v) are inherently true. Assumptions vi) and vii) are based on the fact that a noise signal represents a random process. They have been verified experimentally to be valid [16]. The last assumption contradicts the

Figure 3-7 Continuous time equivalent circuit model of Biquad A

approach published by other authors [32], which assumes total correlation among samples from the same noise source.

The question of whether noise samples on different capacitors due to the same noise source are correlated is very difficult to answer. The assumption of being uncorrelated made in this thesis certainly appears reasonable from certain perspectives. Consider the switched-capacitors C_1 and C_4 in the biquad filter of Figure 3-5, in the special case where the op amps in the filter are ideal (infinite bandwidth with no noise). This implies that the PSD of the noise sampled on a switched-capacitor can be approximated by $2KT R_{EQ}$. From Figure 3-5, during ϕ_1 , C_1 is discharged through S1 and S4 while C_4 is discharged through S6 and S7. The switch thermal noise sampled by the two capacitors at the end of ϕ_1 is therefore uncorrelated and can be modelled as shown in Figure 3-8a. The mean square power of the sampled noise in the baseband, according to equation 2-20, is then

$$P_{N1} = \frac{KT}{C_1}$$

for C_1 , and

$$P_{N4} = \frac{KT}{C_4}$$

for C_4 . Since these two terms are uncorrelated, the mean square power at the output of the filter due to noise sampled on C_1 and C_4 at the end of ϕ_1 is then

$$P_{NO} = P_{N1}A_1^2 + P_{N4}A_4^2 \quad (3-19)$$

Figure 3-8a Uncorrelated sampling of switch thermal noise

Figure 3-8b Correlated sampling of switch thermal noise

where A_1 is the gain from C_1 to the filter output. Because of the high open loop gain of the filter, the filter gain is determined by the feedback network. As a result, $A_1 = C_1/C_4$, and $A_4 = 1$. Substituting into 3-19, the mean square power at the output becomes

$$P_{NO} = \frac{KT}{C_1} \left(\frac{C_1}{C_4} \right)^2 + \frac{KT}{C_4} \quad (3-20)$$

If we now consider the case where a switch is shared between SCRs C_1 and C_4 , for example, in the circuit of Figure 3-9a. The circuit can be modelled to a first order as shown in Figure 3-8b. Noise sampled on C_1 and C_4 is now correlated and the mean square power of noise sampled on the capacitors is then given by

$$P_{NT} = \frac{KT}{C_1 + C_4} \quad (3-21)$$

which can be transformed to yield the uncertainty charge stored on the two capacitors, Q_T , as follows:

$$Q_T^2 = P_{NT}(C_1 + C_4)^2 = KT(C_1 + C_4) \quad (3-22)$$

Feedback action of the filter in closed loop has the net effect of causing all of this uncertainty charge to be transferred to C_4 in a two step process, so the mean square noise power at the output of the filter is given by

$$\begin{aligned} P_{NO} &= \left(\frac{Q_T}{C_4} \right)^2 \\ &= \frac{KT}{C_1} \left(\frac{C_1}{C_4} \right)^2 + \frac{KT}{C_4} \end{aligned} \quad (3-23)$$

Figure 3-9a Input section of a biquad filter

Figure 3-9b Noise model of input stage during $\phi1$

2 of/de 2

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which is exactly the same as equation 3-20, the case where the samples are uncorrelated. This shows that under certain circumstances the question of whether noise samples from the same source are correlated is irrelevant.

For completeness, the effects of switches that are not shared in Figure 3-9a should also be considered. The continuous time noise model during $\phi 1$ is shown in Figure 3-9b. V_{N2} , V_{N4} , V_{N6} are uncorrelated thermal noise sources due to the 'ON' resistance of $S2$, $S4$ and $S6$ respectively. Despite the fact that noise signal from V_{N4} is sampled by both C_1 and C_4 , it has been shown [29] that the noise samples stored on C_1 and C_4 are uncorrelated. Close agreement between simulated results and the measured noise of two biquad filters (to be presented in Chapter 4) further supports the uncorrelated assumption.

Total correlation can lead to higher estimated noise at the output, because noise is added in voltage terms as supposed to power terms. Interestingly, the simulated noise assuming total correlation obtained through z domain analysis as reported in [32] is approximately 3 dB higher than measured data. Perhaps the discrepancy is in part related to the modelling of noise samples from the same noise source. In reality, noise samples from the same noise source are probably correlated to some extent, depending on the circuit context. This problem has been overlooked in the literature, as most research on noise analysis has been based on simple SC circuits. Future research aimed at studying the effects of sampled noise

correlation will certainly be beneficial to the understanding of noise in SC circuits.

The discussed noise analysis approach can easily be applied to SC circuits which have continuous time equivalents. In other words, each switched-capacitor in a circuit can be replaced by an equivalent resistor. Although only single ended circuits have been cited in the examples, the approach can be applied to the differential case as well. In addition to performing noise analysis on internally generated random noise, the continuous time simulation technique can also be applied to study the PSRR of a circuit. Since op amps play a major role in power supply noise injection, complete op amp circuit models must be used. Capacitors should be inserted between all high impedance nodes and power supplies to model coupling due to parasitic capacitances external to op amps. A small signal analysis from the supplies to the filter output will then yield information regarding the baseband supply noise rejection capability of the circuit [33]. Effects of aliased power supply noise in the baseband can also be studied. Wideband power supply noise at the output of integrators is sampled and aliased by switched-capacitors. Hence a set of γ factors can be determined based on only power supply noise, by assuming a certain supply noise PSD. Using these γ factors and suppressing the modelling of other noise sources, the amount of noise in the passband of a filter can thus be simulated.

Chapter 4.

Verification of Continuous Time Approach to Noise Analysis of SC Circuits

4.1 Introduction

A methodology for analyzing the noise performance of switched-capacitor circuits using a continuous time circuit simulator was presented in the last chapter. In this chapter, the validity of the approach is verified with experimental data. A set of test structures has been designed and fabricated to facilitate the verification process. The experiments are divided into two separate parts. The first part deals with the verification of the ability to perform noise analysis on a continuous time MOSFET circuit. This capability allows a designer to predict the noise behavior of an op amp, which is a crucial circuit element and a significant noise source in SC circuits. It also enables the modelling of op amp $1/f$ noise in simulating the noise of a SC circuit. Having established the confidence level of predicting and modelling noise of op amps, the second part of the verification process experimentally validates the proposed SC circuit noise analysis methodology. Measured noise data from two SC biquad filters will be compared with simulated results.

4.2 Test Structures

Most measurements covered in this thesis were performed on three test structures on the same test chip. The first structure is an array of 4 N channel and 4 P channel transistors. All transistors of

the same channel type share common gate, source and substrate terminals. The four sizes for each channel type are the same: $30/1.5\ \mu\text{m}$, $30/3\ \mu\text{m}$, $30/20\ \mu\text{m}$ and $4/20\ \mu\text{m}$. The array is mainly used for transistor noise and DC characterization.

The second structure is a single ended high frequency ($f_s = 10$ to $20\ \text{MHz}$) SC biquad filter with a voltage follower at the output. The schematic diagram of the circuit is shown in Figure 4-1. The filter is basically a two loop ISDN oversampled A/D converter [34] with the one bit quantizer removed. As such the knowledge of the noise behavior of this filter is valuable in designing for wide dynamic range in such converters. All op amps are high speed folded cascode implementations with the dominant pole at the output as shown in Figure 4-2. The input to the voltage follower can be disconnected from the filter and accessed for noise characterization. Another feature of the circuit is that correlated double sampling (CDS) has been incorporated into the design as an option for the first integrator. By setting the appropriate control signals, the filter can operate with or without CDS. The effectiveness of CDS as a technique to remove low frequency noise in a SC circuit will be discussed in Chapter 5.

The third structure is essentially a modified version of the op amp of Figure 4-2. The bias network has been removed, and access to some of the internal nodes has been added (Figure 4-3). With all four terminals of most transistors available, the DC and small signal parameters can be measured. In addition to the modified op amp, two N channel transistors were also included in the structure. One is

Figure 4-1 A Switched-Capacitor biquad filter with CDS option

Figure 4-2 Schematic diagram of folded cascode op amp

exactly the same as the input transistor of the op amp. The gate of this transistor is laid out in a serpentine fashion to minimize area. The second one has exactly the same 'extracted' W/L ratio, but laid out with rectangular gates. The last two structures were implemented by the author. The layouts of all three structures are provided in Appendix A. The test chip has been fabricated in a $1.5\ \mu\text{m}$, N well, double level metal CMOS process.

4.3 Noise Analysis of Continuous MOSFET Circuits

Noise from op amps can be the major factor in determining the dynamic range of a SC circuit. The ability to predict confidently the noise characteristics of an op amp in its design stage is therefore essential. The noise analysis capability of a circuit simulator is merely an extension of frequency domain signal analysis. A frequency domain simulation usually involves two steps. The first step finds the DC solution of the circuit. From the DC solution, linearized small signal parameters of individual transistors are obtained. The AC analysis is then performed by replacing the transistors with their small signal model. When a noise analysis is performed, the same small signal circuit is used and the PSD of the total noise is obtained by summing the PSD of each noise source multiplied by the square of the corresponding voltage gain to the output. The accurate noise simulation of MOSFET circuits, therefore, requires that the DC characteristics, the small signal parameters, and the noise PSD be modelled properly. In this section, all these aspects of the MOSFET model used by the chosen circuit simulator will be

evaluated. The objective is to establish the confidence level of utilizing the simulation tools to design low noise circuits.

4.3.1 MOSFET DC Characteristics

For transistor DC characterization, both P and N channel transistors with aspect ratio of 30/1.5 μm , 30/3 μm and 30/20 μm were measured. Basically, for each die characterized, a set of I_D - V_D curves was generated for each device type and size. The average data from a number of dies were then compared to what the MOSFET model predicted. The observed variation of transistor characteristics from die to die is very small. The tolerance on measured saturation current is less than 4.5% for N channel and 6% for P channel devices.

Figure 4-4 shows the simulated and measured curves for short channel ($W=1.5\mu\text{m}$) P and N channel devices. From these curves it is quite clear that the MOSFET model predicts DC performance that is quite close to measured results. For gate voltages below 2V and in the saturation region, as in typical analog applications, the matching is excellent. In all cases, the amount of deviation is certainly within the tolerance of process variations. Even better agreement is observed for wider channel devices [35]. For further verification, the bias voltages of the op amp of Figure 4-2 were simulated. The results are within 70 mV of measured values.

4.3.2 Low Frequency Small Signal Parameters

In the context of noise analysis of MOSFET circuits, the low frequency small signal parameters are the most important. Specifi-

Figure 4-4a Short channel NMOS $I_D - V_D$ characteristics

Figure 4-4b Short channel PMOS $I_D - V_D$ characteristics

cally, the small signal transconductance g_m and output drain conductance g_d are the two key elements in the low frequency model. To determine how well the circuit simulator can model these small signal parameters, the fragmented op amp of Figure 4-3 was used. The op amp is essentially a single stage transconductance amplifier with its dominant pole at the output. The feedback network composed of transistors M21 to M24 pins the voltage of node V_{OUT} to analog ground. This converts the differential signal that would otherwise be seen across V_{OUT} and V_{OUT-} to a single sided signal at V_{OUT} . The gain seen at V_{OUT} is therefore doubled. The simplified low frequency model of the op amp is given in Figure 4-5. Using this model, the DC gain of the op amp in terms of small signal parameters is

$$A_{DC} = \frac{g_{m1}(g_{m2} + g_{d2})}{g_{d2}(g_{d1} + g_{d5}) + \frac{(g_{m2} + g_{d2} + g_{d1} + g_{d5})(g_{d3} g_{d4})}{(g_{m3} + g_{d3} + g_{d3})}} \quad (4-1)$$

The DC gain was measured by sweeping the negative input terminal V_{IN-} from 2.45 V to 2.55 V in 1 mV steps while V_{IN+} was tied to analog ground (2.5 V). The slope of the V_{OUT} versus V_{IN-} plot at $V_{OUT} = 2.5$ V yields the DC gain. The average measured value is 54 dB. The circuit of Figure 4-2 was simulated with transistor physical dimensions extracted from layout. The circuit simulator predicted a gain of 60.5 dB. The difference of 6.5 dB is significant enough to raise questions about the source of error for analog circuit simulations. The linearized small signal parameters from the simulation are listed in Table 4-1, Column 1. The DC gain calculated by substituting these

Figure 4-5 Small signal model of folded cascode op amp

parameters into equation 4-1 is 58.7dB. This confirms that the equation is a reasonable model of the DC gain.

To find out why the simulated gain is higher, the approach taken was to measure these small signal parameters and compare the two sets of data. Equation 4-1 suggests that only the parameters of five transistors, M1 through M5 are required. For each transistor g_m and g_d can be measured directly, given that the voltages at all four terminals of the device are known. From Figure 4-3 this implies that voltage V_X , V_A , V_B and V_{OUT} must be determined. The measurement of these small signal parameters began with the selection of an op amp with close to average gain. The device was then connected in the unity gain configuration. This put the circuit in a stable state and the internal voltages were measured. Then for each of the five transistors, the circuit was set up so that the transistor under test was electrically isolated and biased appropriately. A set of I_D - V_D curves from which g_m and g_d for the device under test were derived was finally generated. Under exactly the same biasing conditions as in the measurements, g_m and g_d were simulated for each transistor. The measured and simulated parameters from the individual transistors are entered in Table 4-1 as Columns 2 and 3 respectively. With the exception of g_{d1} , data in the two columns match well. The discrepancy in the value of g_{d1} will be discussed. The DC gain was also calculated using equation 4-1 with the two sets of parameters, and in both cases the result is quite close to the measured gain of 54 dB.

	column 1	column 2	column 3	column 4
g_{m1}	2.16E-3	2.70E-3	2.47E-3	2.17E-3
g_{d1}	12.31E-6	30.00E-6	14.68E-6	12.16E-6
g_{m2}	1.99E-3	2.34E-3	2.30E-3	2.24E-3
g_{d2}	66.66E-6	73.80E-6	86.38E-6	84.44E-6
g_{m3}	1.82E-3	2.34E-3	2.28E-3	2.07E-3
g_{d3}	15.45E-6	24.00E-6	23.03E-6	18.55E-6
g_{d4}	131.00E-6	412.00E-6	422.00E-6	342.00E-6
g_{d5}	32.79E-6	38.63E-6	37.15E-6	42.67E-6
Gain	58.7 dB	53.3 dB	53.0 dB	53.3 dB

column 1: initial op amp circuit simulation

column 2: measured from individual transistors

column 3: individual transistor simulation

column 4: circuit simulation with correct M5 width

Gain : calculated using equation 4-1

Table 4-1 Op amp small signal parameters

The major differences between Column 1 and 2 of Table 2 are the parameters g_{d1} and g_{d4} , the output conductance of M1 and M4 respectively. Analysis of the DC gain equation shows that a factor of two change in the g_{d1} contributes to less than 1 dB of change in the DC gain. On the other hand, a factor of three change in the value of g_{d4} alters the DC gain by over 4.4 dB. The problem appears to be associated with device M4. However, a closer look at the measured data reveals that the problem actually lies with device M5. The current level predicted by the simulator is 20% lower. This was verified experimentally for a number of dies, and under various bias conditions. The only logical conclusion is that the physical dimensions supplied to the model are incorrect. The transistor M5 is laid out with serpentine gate structures with an extracted gate width of $370\text{ }\mu\text{m}$. Taking the centerline approach, manual measurement of the layout yields a device width of $480\text{ }\mu\text{m}$! The exact dimensions of the transistor are difficult to model, due to its long gate length ($5\text{ }\mu\text{m}$) and high number of 45 degree bends. A device width of $445\text{ }\mu\text{m}$ was established by matching simulated saturation current to measurement.

The difference in the value of DC gain between Column 1 and the rest of Table 2 can now be explained. In the circuit of Figure 5, M5 acts as a current source that supplies current to M1 and M3. The circuit was designed such that with the bias voltages used, the voltage at V_B is just high enough for M4 to be in saturation, where its output conductance is low. In the fabricated circuit, M5 is much wider, and the current through M3 is higher. With the bias voltages

as designed, the higher current in M3 causes V_B to sit at a lower voltage. This forces M4 out of saturation, and its output conductance g_{d4} becomes higher. The DC gain, which is inversely proportional to g_{d4} , is therefore lower than the designed target.

After modifying the op amp circuit to reflect the "real" width of M5, the circuit was simulated again. The results are presented in Column 4 of Table 4-1. Comparing Column 2 to 4, it is found that with the exception of g_{d1} , corresponding parameters are within 20% of each other. This indicates that the transistor model can be used to simulate complex analog circuits with sufficient accuracy, provided that the physical dimensions are properly extracted.

The data in Column 2 and 3 of Table 4-1 are in good agreement with the exception of the parameter g_{d1} . There are two reasons for the discrepancy. The first one is related to the modelling of the physical dimensions of the transistor. The layout of M1 is similar to the layout of M5. The gate length of M1 is shorter but the serpentine gate structure still poses a modelling problem. The second reason is the high substrate bias under which the transistor operates. It appears that for short channel devices, the transistor model loses its accuracy with high substrate bias. This has been verified experimentally. It is believed that the accuracy of the model can be improved with transistor parameters that are properly extracted for analog simulations.

It was pointed out in previous discussion that transistors with non-rectangular gates are difficult to model. The width of 45 degree

segments is never identical to the width of horizontal or vertical segments due to the finite resolution of the physical design system. The source and drain resistance, which depends on the location and number of source and drain contacts, also affects the transistor characteristics. Finally, if the layout is not symmetrical, the source and drain terminals cannot be interchanged. The output conductance becomes geometry dependent [36]. The only way that non-rectangular transistors can be accurately modelled is by fitting simulation to measurements.

The DC characteristics of two N channel transistors of exactly the same extracted aspect ratio were compared. One device has a serpentine gate structure, while the other one has rectangular gates. As expected, the rectangular transistor bears more resemblance to the simulation model. In general, the saturation current of the non-rectangular device is about 90% of that of the rectangular one. The increased source and drain resistance accounts for part of the discrepancy observed. Differences in the effective physical dimensions between the two devices are also partially responsible. Another observation made while measuring these transistors is that the DC characteristics of the non-rectangular devices are less consistent from die to die. It is suspected that the high number of 45 degree corners makes the transistor more susceptible to process variations.

4.3.3 Noise Analysis of MOSFET Circuits

Having established that the circuit simulator can accurately simulate the AC performance of analog circuits in the frequency range of interest, this section presents the results of noise analysis. The process began with a re-calibration of the $1/f$ noise model to fit present experimental data. The input referred noise of the op amp of Figure 4-2 was then simulated and compared with experimental data.

4.3.3.1 Transistor Noise Model Calibration

Transistor noise measurements were performed using a special noise setup at Northern Telecom Electronics Ltd. Seven frequency points were selected from 37 Hz to 2 KHz to avoid 60 Hz harmonics. For both P and N type transistors, a drain voltage of 2.5 V and a gate voltage of 2 V were used. It is believed that substrate current can contribute to device noise [37]. Under these bias conditions, substrate current was minimized. In both cases, a 30/1.5 μm device was used.

Figure 4-6 shows the plot of input referred noise of both channel types. At 1 KHz, the average measured noise is 142 $\text{nV}/\sqrt{\text{Hz}}$ for N channel devices and 41.6 $\text{nV}/\sqrt{\text{Hz}}$ for P channel transistors. Comparing the two sets of data it is apparent that the $1/f$ noise of a P channel transistor is about 10 dB lower than a N channel device of the same size. This is probably due to the fact that P channel transistors in the chosen technology are actually buried channel devices, where the conducting channel is formed away from the Si-SiO₂ interface. Using the charge pumping technique [38], an estimate

Figure 4-6 Measured versus simulated transistor 1/f noise

of the surface state density and the capture cross section for both types of devices was obtained. Together with another model parameter, the noise model was calibrated to match measured results. The simulated noise for N and P channels are given as solid lines in the plot.

4.3.3.2 Op Amp Noise Results

The purpose of incorporating a noise model into the transistor model is to allow designers to perform noise analysis on complex circuits. It was established earlier that the chosen circuit simulator can accurately predict the small signal behavior of the op amp of Figure 4-2. Logically, the same circuit was chosen to verify the noise analysis capability.

A total of 12 op amps were tested. The noise measurements were performed on packaged devices to minimize system noise. The power supplies to the op amp were filtered and the entire test fixture was mounted in a shielded box. The gain and noise floor were first measured, and compensations were made in calculating the input referred noise. The simulated and measured data are presented in Figure 4-7 for supply voltages of 5 V and 3.3 V. It is clear that the results are in good agreement, especially at low frequencies. According to simulation results, the major noise sources in the circuit are the two input transistors (M1, M2 in Figure 4-2). They contribute 70% of the input referred noise power. The remaining 30% mainly comes from the two bottom N channel transistors (M3, M4) of the output cascode stage.

Figure 4-7 Measured versus simulated op amp input referred noise

For the $V_{DD} = 5\text{ V}$ case, over a 10 MHz frequency range, the difference between measured and simulated data is less than 3dB. The discrepancy is probably due to high substrate bias conditions of M1 and M4. It was pointed out in the previous section that the MOSFET model with default model parameters cannot model DC characteristics of devices with high substrate bias very well. Since $1/f$ noise is bias dependent, and the two devices contribute most of the noise power, the conjecture seems reasonable. The fact that matching in the 3.5 V case is significantly better, further supports the argument. Again it is believed that higher accuracy in noise simulation can be achieved with a better calibrated MOSFET transistor small signal model.

From the findings of noise characterization presented, there is a clear indication that improvements can be made in the op amp design to enhance noise performance and modelling accuracy. By turning the structure of the op amp upside down, in that the input pair and the current source will now be P channel transistors, etc., substrate bias on the input pair can be eliminated by placing the devices in their own N-well. Without substrate bias, modelling accuracy is improved, and more importantly, the transconductance (g_m) of the devices is increased. From equation 4-1, the DC gain of the op amp is directly proportional to the transconductance of the input device. Simulations show that smaller P channel input devices without substrate bias can achieve the same transconductance as N channel devices with substrate bias. In addition to saving chip area, the parasitic gate overlap capacitance is also reduced, leading to

improved PSRR of the op amp. Finally, an op amp with P channel input devices will have more desirable noise characteristics since P channel transistors have inherently lower $1/f$ noise.

4.4 Verification of Noise Analysis of SC Circuits

In Chapter 3, a methodology for noise analysis of SC circuits in the continuous time domain was presented. In this section, the validity of the approach will be verified with results from two biquadratic filters. The first filter (Biquad A) is that of Figure 3-5 while the second one (Biquad B) is given in Figure 4-1. The two filters use the same op amp of Figure 4-2, the same switches, and are fabricated with the same process. However, the filters are also different in several respects. Firstly, all the capacitors of Biquad B were made four times bigger to reduce KT/C noise. Biquad A has a low pass transfer function with some peaking at resonance. The peaking in the response of Biquad B has been reduced. Although the transfer functions are similar, the implementations of the clocking schemes are different. Lastly, the number of switches in Biquad B has been reduced by means of switch sharing. In addition to having fewer noise sources, switch sharing also creates the situation where the thermal noise of a switch is sampled by two capacitors as illustrated in Figure 3-8. These differences will serve as a test to determine if the methodology is universal and to provide some insight into the effects of correlated sampling as discussed in Section 3.5.

Extreme caution was exercised to cut down noise penetration from external sources. In laying out the circuits, several steps were taken to reduce power supply noise coupling. All capacitors were shielded from the substrate by means of grounded N wells. All virtual ground connections were made in the top metal layer with grounded lower metal layer underneath for shielding where possible. The analog section was separated from the clock generators and drivers. Finally, independent power buses and pads were used to minimize crosstalk between digital and analog circuits. All filters were tested in bonded packages. A pin grid array with 68 pins was chosen so that every other adjacent pin was grounded to eliminate crosstalk. A simple test board was built for each of Biquad A and Biquad B. Power supply lines were heavily filtered and abundant decoupling was provided on board. The test board was mounted in a shielded box located immediately next to a HP3835A spectrum analyzer, so that minimum length cables could be used.

The measurement system basically consists of an HP 200 series microcomputer, a spectrum analyzer, function generators and power supplies. The function generators provided the two phase non-overlapping clocks required by the filters. A program has been written which controls the spectrum analyzer to perform the measurement of filter gain, system noise floor, and filter noise. After the measurements are completed, the program processes the data and generates a plot of the input referred noise of the filter.

The simulated versus measured op amp input referred noise has been given in Figure 4-7. Discrepancies are observed because of

inadequacies in the MOSFET model. Since the purpose of this section is to validate the approach of using a continuous time simulator to perform noise analysis on SC circuits, it is important that the op amp $1/f$ noise is correctly simulated. Consequently, the parameters in the MOSFET noise model were adjusted so that the simulated input referred $1/f$ noise of the op amps matched measured data.

4.4.1 Biquad A Experimental Results

Because of an error in the digital clock generation circuitry, the clock frequency of Biquad A is limited to 2 MHz. A number of samples were characterized at a clock frequency of 900 KHz. The measured output noise and the filter gain are plotted in Figure 4-8. The simulated results are obtained using the circuit of Figure 3-7, the circuit parameters of Table 3-1 and the γ factors of Table 3-2. Figure 4-8 shows that the output noise exhibits a $1/f$ behavior at frequencies below 1 KHz. This indicates that $1/f$ noise due to the op amps dominates in this region. At higher frequencies, SCR thermal noise becomes more prominent, and the noise spectrum levels off. The shape of the noise spectrum follows the designed filter transfer function from the input, suggesting that noise sources near the input dominate.

In determining the dynamic range of a circuit, the minimum input signal is generally limited by the input referred noise. Hence input referred noise is the parameter of interest when comparing simulation to measured results. Figure 4-9 shows that the simulated and measured input referred noise of Biquad A are in good agree-

Figure 4-8 Measured gain and output referred noise of Biquad A

Figure 4-9 Biquad A input referred noise

ment within the entire passband of the filter. Slightly increased deviation is observed near the resonant frequency. In this region, the transfer function goes through very rapid changes due to the high Q of the filter. Since noise is divided by the transfer function when referred back to the input, small discrepancies of measured noise at the output will be magnified in the referral process. Another attribute to the deviation at high frequencies is the imperfect mapping from the sampled-data z domain to the continuous s domain.

Over most of the passband of the filter, aliased broadband noise is the major noise component. This is expected as a result of the the low clock frequency and small capacitors used. We have ~~concluded~~ that SCRs near the input are responsible for most of the noise, and this can be confirmed by a simple analysis of the continuous time circuit of Figure 3-7. We can assume that R_{EQ1} and R_{EQ4} are the main sources of noise, since they are near the input. Noise due to R_{EQ1} will see the DC gain of the filter in propagating to the output while noise due to R_{EQ4} will experience unity gain. Because of the high open loop gain of the filter, its DC gain is governed by the gain of the feedback network. In this case, the DC gain is given by R_{EQ4}/R_{EQ1} . Therefore, we can make an estimate of the thermal noise at the output due to these two resistors as follows:

$$\begin{aligned} S_{NO} &= \gamma_1 4KTR_{EQ1} (R_{EQ4}/R_{EQ1})^2 + \gamma_4 4KTR_{EQ4} \\ &= 373 \times 10^{-15} \text{ V}^2/\text{Hz} \end{aligned}$$

and the measured value at 10 KHz (Figure 4-8) is $370 \times 10^{-15} \text{ V}^2/\text{Hz}$. The result confirms that the thermal noise of a SC biquad filter is dominated by the KT/C noise of SCRs near the input.

4.4.2 Biquad B Experimental Results

Using the method described in Chapter 3, the biquad filter of Figure 4-1 was analyzed. With Correlated Double Sampling disabled, the circuit has the same continuous time equivalent circuit as Biquad A. Output noise was measured for three operating conditions: 5 V supply at 9.6 MHz, 5 V supply at 4.8 MHz, and 3.5 V at 4.8 MHz. The circuit parameters and calculated γ factors are listed in Table 4-2. At reduced supply voltage, the 'ON' resistance of the switches and the thermal noise of the op amp are altered. Since the changes of these two key parameters are not proportional, a new set of γ factors results. The variations in both the clock frequency and the supply voltage are designed to challenge the viability of the proposed simulation approach. The supply voltage reduction also serves the purpose of providing insight into low voltage analog circuit design.

The simulated and measured results for the two cases with 5 V supply are superimposed and plotted in Figure 4-10. The results for the filter at 3.5 V is given in Figure 4-11. In all cases, the simulated input referred noise is in excellent agreement with measured data. Similarity between Biquad A and Biquad B confirms that overall noise is dominated by sources near the input. Higher sampling frequencies and larger capacitors have reduced KT/C noise drastically, making $1/f$ noise the major noise generating mechanism

C_1	1.309 pF	1.309 pF
C_2	0.982 pF	0.982 pF
C_3	0.982 pF	0.982 pF
C_4	0.785 pF	0.785 pF
C_{I1}	3.927 pF	3.927 pF
C_{I2}	1.309 pF	1.309 pF
R_{ON}	500 ² Ohms	990 Ohms
R_{OA}	6000 Ohms	12.9 KOhms
f_{UG}	95 MHz	25 MHz
DC Gain	60 dB	64 dB
f_s	9.6 & 4.8 MHz	4.8 MHz
$V_{DD} - V_{SS}$	5.0 Volts	3.5 Volts
γ_1	2.0686	2.0165
γ_2	5.5561	5.6081
γ_3	1.5012	1.4711
γ_4	4.1604	4.3406

Table 4-2 Biquad B circuit parameters

Figure 4-10 Biquad B input referred noise

Figure 4-11 Biquad B input referred noise at 3.5 V

over most of the passband. We can estimate the 1/f noise contribution at the output from the first op amp by performing the following analysis at 1 KHz:

$$\begin{aligned} S_{NO1/F}(1 \text{ KHz}) &= S_{N1/F}(1 \text{ KHz})(1 + R_{EQ4}/R_{EQ1})^2 \\ &= 114 \times 10^{-15} \text{ V}^2/\text{Hz} \end{aligned}$$

where $S_{N1/F}(1 \text{ KHz})$ is the simulated op amp noise at 1 KHz. The simulated filter output noise is $130 \times 10^{-15} \text{ V}^2/\text{Hz}$. As expected, the majority of 1/f noise is contributed by the first op amp.

Referring to Figure 4-10, we can see that the input referred noise for the two clock rates are identical at low frequencies, where 1/f noise is the predominant factor. At higher frequencies, where 1/f noise drops out, the thermal noise of the two cases differs by 3 dB. Biquad B has a low pass transfer function with a cut off frequency that is approximately 1/20 of the clock rate. Within the passband, the gain of the filter is the same regardless of clock rate. The 1/f noise, which is independent of the clock frequency and concentrated at low frequencies, is therefore comparable in the two cases. On the other hand, thermal noise which originates from the undersampling of broadband noise is inversely proportional to the sampling frequency, as given by equation 2-19. When sampling rate is halved from 9.6 MHz to 4.8 MHz, the PSD of KT/C noise is doubled, yielding the observed difference.

The analysis of results for the case with reduced supply voltage yields similar conclusions regarding contributions from various

sources. It is interesting to note that despite increased 'ON' resistance of switches and thermal noise of op amps (Table 4-2) the overall thermal noise of the filter remains close to that of normal supply voltage. This can be explained by the fact that the UGBW of the op amp is lower at 3.5 V, thereby curtailing the foldover effects. The closeness of the thermal noise of the two cases is reflected in the two sets of γ factors of Table 4-2. This is a good example of how each of a number of inter-related factors plays a role in determining the noise performance of a SC circuit. Being able to perform noise analysis using a simple methodology, as described in this thesis, is certainly valuable to circuit designers.

Chapter 5

Correlated Double Sampling

5.1 Low Frequency Noise Reduction Techniques

The central part of the thesis has been presented in chapters 3 and 4. This chapter explores a particular circuit technique that is relevant to the design of high performance SC circuits. It will also be shown that the proposed circuit simulation methodology can be modified to predict the noise performance of such more complex circuits.

The noise analysis results in Chapter 4 have shown that for certain SC filters, the low frequency input referred noise is dominated by the $1/f$ noise of the input stage op amp. For filters with a low pass transfer function, especially in voice band applications, $1/f$ noise can be the limiting factor in determining the achievable dynamic range. Consequently, it is desirable to be able to minimize the $1/f$ noise of op amps.

The main contributors of noise in an op amp are the input devices. Since $1/f$ noise in a MOSFET is inversely proportional to the gate area, the most common practice is to increase the gate area while maintaining the proper aspect ratio. An increase in gate area, and hence chip area, also increases the parasitic capacitances, thereby degrading the PSRR and potentially affecting stability for single stage op amps. The benefits attainable using this approach are therefore very limited.

The second technique for eliminating low frequency noise is chopper stabilization [39] as shown in Figure 5-1a. The input signal is modulated by the first multiplier which is driven by a chopper square wave. This translates the spectrum of the signal to the odd harmonics of the chopper waveform. The $1/f$ noise of the amplifier is not translated, so the signal spectrum now resides in a region where $1/f$ noise is low. After the second multiplier, the input signal is demodulated while the $1/f$ noise is modulated and translated to higher frequencies. The net effect is having the $1/f$ noise of the amplifier translated so that the concentration of noise power is significantly reduced in the baseband. The equivalent circuit with the modified noise spectrum is given in Figure 5-1b.

The third technique is correlated double sampling (CDS). The concept was introduced in 1974 to reduce low frequency noise and offset associated with output circuits in charge coupled device imagers [40]. The principal of CDS can be illustrated with the model of Figure 5-2a. During the initializing phase ($\phi 1$), the input referred noise of the amplifier $V_N(t)$ is sampled-and-held. During $\phi 2$, the held sample is subtracted from the instantaneous noise voltage. If the noise signal represents a DC offset, total cancellation is achieved. For $1/f$ noise, the equivalent noise of an amplifier with CDS is shown in Figure 5-2b. Mathematically, the z domain transfer function of $V_N(t)$ can be described as

$$|H_N(z)| = \frac{V_{OUT}}{V_N} = A(1 - z^{-1/2}) \quad (5-1)$$

Figure 5-1a Concept of chopper-stabilization technique

Figure 5-1b Equivalent input referred noise of chopper-stabilized amplifier

Figure 5-2a Concept of correlated double sampling

Figure 5-2b Equivalent input referred noise of amplifier with correlated double sampling

If we denote $S_N(f)$ as the PSD of the original $1/f$ noise, the PSD of the equivalent noise at the input, $S_{NEQ}(f)$, is then

$$S_{NEQ}(f) = 2(1 - \cos(\pi f/f_s))S_N(f) \quad (5-2)$$

The above equation indicates that CDS introduces zeros at DC and even integral multiples of the sampling frequency. As a result, for $f \ll f_s$, the input referred noise of the amplifier is essentially high pass filtered.

5.2 Correlated Double Sampling in SC Circuits

The implementation of CDS in SC circuits to reduce offset and $1/f$ noise was reported by Lam and Copeland [41] in 1983. The circuit of a low noise inverting integrator is depicted in Figure 5-3a. The basic operation is to store a sample of the op amp input referred noise or offset on C_{CDS} during the initializing phase (ϕ_1) by shorting the op amp output to its negative terminal. Feedback forces the virtual ground node A to track the input referred noise. When S_4 opens, $V_N(t)$ is sampled onto C_{CDS} . During ϕ_2 , when charge is transferred from the input capacitor C_1 to the feedback capacitor C_f , node B becomes the virtual ground. The noise as seen at node B is then the difference between the instantaneous noise $V_N(t)$ and the sampled value stored on C_{CDS} . The z domain transfer function of $V_N(t)$ to the output can be derived from the following difference equations at the end of ϕ_2 :

$$V_{OUT}(n) = V_A(n) + V_{CI}(n) \quad (5-3a)$$

where

Figure 5-3a Original inverting SC integrator with correlated double sampling

Figure 5-3b Typical output waveform of original CDS integrator

$$V_A(n) = V_N(n) - V_N(n - \frac{1}{2}) \quad (5-3b)$$

$$V_{CI}(n) = V_{CI}(n - 1) + (C_1/C_I)V_A(n) \quad (5-3c)$$

Substituting equations 5-3b and 5-3c into 5-3a and rewriting in the z domain, the transfer function becomes:

$$H_N(z) = \frac{1 - z^{-1} + C_1/C_I}{1 - z^{-1}} (1 - z^{-1/2}) \quad (5-4)$$

The $(1 - z^{-1/2})$ term in $H_N(z)$ reflects the CDS action of the integrator.

The main disadvantage of the circuit is the requirement for high op amp slew rate. Since the integrator output is short-circuited to the negative input of the op amp during $\phi 1$, the output alternates between the output voltage and virtual ground during each clock period as shown in Figure 5-3b. The op amp must be able to slew and settle quickly to the final voltage. High slew rate can be achieved by increasing bias currents, but only at the expense of increased area and power dissipation.

Several new schemes have since been reported that do not require high op amp slew rate [42,43]. All implementations require extra capacitors and switches to achieve the function. Any increase in the number of switches can increase clock feedthrough and offset, making some of these schemes not very practical. Nagaraj proposed a scheme that requires the addition of only one extra switch and capacitor [44]. The schematic diagram of the improved integrator with CDS is provided in Figure 5-4.

Figure 5-4 Improved inverting SC integrator with correlated double sampling

The operation of this circuit is similar to that of Figure 5-3. During the initialization phase ($\phi 1$) the feedback capacitor C_I is placed between the output and the inverting input of the op amp, rather than short-circuiting the two nodes. The feedback capacitor action allows V_N to be sampled by C_{CDS} . This implementation hence enables V_{OUT} to stay very close to its value at the end of $\phi 2$ during $\phi 1$, eliminating the high slew rate requirement. The noise transfer function has been derived and is given as follows:

$$H_N(z) = \frac{1 - z^{-1} + C_I/C_I}{1 - z^{-1}} (1 - z^{-1/2}) + \frac{C_{CDS}}{C_I} z^{-1/2} \quad (5-5)$$

A comparison between equations 5-4 and 5-5 reveals that the new scheme generates an extra noise component at the output. However, the quantitative performance degradation due to this term is very small. This extra term represents a translated component of $V_N(t)$, not an integrated component. The low frequency noise of a conventional SC integrator is mainly due to the integration of the input referred noise, because of the high gain at low frequencies inherent to the integration process. Consequently, the capability of the circuit to suppress low frequency noise is not seriously affected. The calculated noise responses of the two integrators with CDS and the conventional integrator are given in Figure 5-5. In all cases, $(C_I/C_I) = 0.2$, $C_{CDS} = C_I$ and $f_s = 1$ MHz. The low frequency noise suppression capability of CDS is obvious from these curves. The difference between the two CDS cases is due to the extra term of equation 5-5. Since this term is proportional to the ratio of C_{CDS}/C_I , the performance gap can be narrowed by using a smaller C_{CDS} .

Figure 5-5 Noise gain of integrators

5.3 Implementation of a SC Biquad Filter with CDS

In order to evaluate the effectiveness of CDS in a SC circuit, a biquad filter was designed with the integrator of Figure 5-4 as the first stage. Figure 4-1 shows the complete implementation where CDS can be optionally selected. The schematic diagram of the filter in CDS mode is provided in Figure 5-6.

The size of C_{CDS} has been chosen to be the same as C_{I1} . The relatively large value is needed to swamp any parasitic capacitance to ground at the virtual ground node that will cause charge transfer error. Moreover, during ϕ_2 , C_{CDS} and OA1 form a composite amplifier with reduced $1/f$ noise. The gain of this composite amplifier is sensitive to parasitic capacitance between the negative input terminal and the output of OA1, shown as C_p in Figure 5-7. The high frequency gain of the amplifier is determined by the ratio C_{CDS}/C_p . Clearly, a large C_{CDS} is necessary to reduce finite gain effects [18].

5.4 Experimental Results and Analysis

The output noise of the biquad filter with CDS was measured using the same set up as Biquad B. The same clock rates of 9.6 MHz and 4.8 MHz were applied. The measured input referred noise for each clock rate is plotted with the corresponding filter without CDS in Figure 5-8. The $1/f$ dominance at low frequencies is noticeably absent from the spectrum of the CDS filters. As expected, CDS has removed the $1/f$ noise of the first op amp, leaving behind a relatively flat noise spectrum. However, the level of thermal noise is higher than the filters without CDS by 6 dB. This is recognized by

Figure 5-6 A Switched Capacitor biquad filter with correlated double sampling

Figure 5-7 Equivalent op amp with correlated double sampling during integration phase

Figure 5-8a Measured input referred noise of Biquad B at 9.6 MHz

Figure 5-8b Measured input referred noise of Biquad B at 4.8 MHz

comparing the noise levels at 100 KHz, where the thermal noise is dominant for non-CDS filters. If we compare the noise of the CDS filters at the two clock rates, a difference of 3 dB is observed. The noise level decreases with higher sampling rate, just like the thermal noise of the filters without CDS. This suggests that the extra noise is sampled-data in nature. Since the only difference between the two modes of operation is the implementation of CDS in the first stage, the extra noise is suspected to be generated by the associated switching elements. One can proceed to analyze the origin of the extra noise by concentrating on the input stage of the filters. The time-invariant circuit diagrams of the input stage of the two filters at each clock phase are shown in Figures 5-9 and 5-10. Switches S1 and S3 and the sampling capacitor C_{CDS} constitute the the extra components required to implement CDS.

In the non-CDS filter, S1 is always closed, short-circuiting node A to node B. Feedback action via C_{I1} makes node A the virtual ground. During ϕ_1 , input referred noise of OA1 causes voltage fluctuations across C_{CDS} . At the end of ϕ_1 , when S3 and S4 open, noise is sampled onto C_{CDS} . Assuming that C_{CDS} is initially uncharged and a voltage ΔV_N appears across C_{CDS} at the end of ϕ_1 , then a charge, $\Delta Q = \Delta V_N C_{CDS}$ will be transferred from C_{I1} to C_{CDS} . The voltage across C_{I1} therefore changes by an amount $\Delta V_{C_{I1}} = \Delta Q / C_{I1}$. During ϕ_2 S3 remains open and C_{CDS} stays charged with ΔQ . At the next ϕ_1 phase, S3 and S4 are closed and noise will again be sampled onto C_{CDS} at the end of the clock phase. If $\Delta V_N = 0$ when S3 and S4 open, then $\Delta Q = 0$ and the charge that has been transferred from C_{I1} to C_{CDS} at the end

Figure 5-9a Filter input stage in non-CDS mode during ϕ_1 Figure 5-9b Filter input stage in non-CDS mode during ϕ_2

Figure 5-10a Filter input stage in CDS mode during ϕ_1 Figure 5-10b Filter input stage in CDS mode during ϕ_2

of the previous $\phi 1$ phase will be returned to C_{11} . In other words, there is no destruction of charge stored on C_{CDS} at any time, so the noise sampled on C_{CDS} is not integrated by C_{11} . The noise due to the extra switching elements is thus negligible, compared to the noise sampled on C_1 and C_4 , which is integrated. This has been confirmed by the experimental and simulated results of Biquad B presented in Chapter 4.

The circuit of the CDS filter during $\phi 1$ is exactly the same as the non-CDS case. At the end of $\phi 1$, S_1 and S_4 open, S_2 closes and S_3 remains closed. When S_4 opens, the $1/f$ noise of $OA1$ is sampled on C_{CDS} . The closing of S_2 short-circuits nodes B and C, making node C the charge summing node of the integrator. Capacitor C_{CDS} is now placed between the negative input of $OA1$ and node C. For $1/f$ noise, because of the high correlation between the sample on C_{CDS} and the instantaneous noise during $\phi 2$, the noise seen at node C is greatly reduced. This is the basic principle of CDS which has been verified with experimental data.

If $1/f$ noise were the only noise sampled by C_{CDS} , then the thermal noise of the CDS filter should be the same as Biquad B. However, broadband thermal noise of S_3 , S_4 and $OA1$ are also sampled by C_{CDS} . All three noise sources are uncorrelated and each influences the voltage across C_{CDS} via a different transfer function. The PSD of the noise sampled on C_{CDS} can be calculated in exactly the same manner as noise sampled on switched-capacitors. During $\phi 2$, when C_{CDS} is connected between nodes A and C, unlike $1/f$ noise, the aliased broadband noise sample stored on C_{CDS} is not correlated to

the instantaneous component. This means that the sampled noise on C_{CDS} represents an additional noise contribution. The sampled noise on C_{CDS} can be modelled as a noise source between nodes A and C. The voltage gain from this noise source to the output of the filter, in the context of the continuous time equivalent circuit, is given by

$$A_{NOA} = 1 + \frac{R_{EQ4}}{R_{EQ1}} \quad (5-6)$$

Due to this extra noise source, the thermal noise of the CDS filter is expected to be higher than the non-CDS case. In fact, the transfer characteristic of a CDS circuit with first order low pass filtered op amp input referred noise has been analyzed [45]. The results indicate that with undersampling, the PSD of input noise is magnified by the 'foldover' factor given as equation 2-13. The extra noise thus depends on the PSD of noise sampled on C_{CDS} , which in turn varies with the clock rate, and the gain and bandwidth of each noise source.

An attempt was made to calculate the expected thermal noise of the CDS filter. The circuit of Figure 5-6 was used to evaluate the PSD of noise sampled on C_{CDS} and to generate a set of γ factors for KT/C noise simulation. The PSD of noise sampled on C_{CDS} was multiplied by the square of A_{NOA} (equation 5-6) to obtain spectral contribution at the output. This was added to the simulated KT/C noise power due to SCRs and then referred back to the filter input. For both clock rates, the calculated noise is over 3 dB lower than measured data. It can be inferred that other underlying mechanisms are also responsible for the generation of aliased broadband noise.

The discrepancy can be attributed to subtle differences in operation between the CDS and non-CDS modes. One important difference lies with the parasitic capacitance to ground of the bottom plate of C_{CDS} . The capacitors in the filter are fabricated with two parallel plates of polysilicon, and each capacitor is shielded from the substrate by a grounded N-well. Inherent to this structure is the parasitic capacitance between the bottom plate and the grounded N-well. In typical stray free SC filter implementations, the bottom plates of all capacitors are driven by low impedance sources. For example, the bottom plate of C_4 in Figure 5-10 is connected so that the parasitic capacitance C_{P4} is switched between the low impedance filter output and analog ground. Charge stored on C_{P4} during $\phi 2$ is discharged to ground during $\phi 1$, never interfering with the charge transfer between C_4 and C_{I1} .

In Figure 5-10, the bottom plate parasitic capacitance of C_{CDS} , C_{PCDS} , is not always connected to a low impedance node. During $\phi 1$, C_{PCDS} is discharged to ground through S3 and S4. During $\phi 2$, C_{PCDS} is connected between ground and node C. Since node C is the virtual ground node, it tracks any input referred noise of OA1. Just like C_1 and C_4 , C_{PCDS} will alias this noise and transfer charge to C_{I1} when S2 opens. Since C_1 and C_{PCDS} are in parallel at all times, they can be grouped together as a single capacitor $C_1' = C_1 + C_{PCDS}$ in determining the effect of aliased thermal noise of OA1. As far as the transfer of input referred noise of OA1 is concerned, the value of R_{EQ1} in the continuous time equivalent circuit has been reduced to

$$R_{EQ1}' = \frac{1}{f_s C_1'} = \frac{1}{f_s (C_1 + C_{PCDS})} \quad (5-7)$$

Consequently, the DC gain of sampled noise of OA1 to the output now given by

$$A_{NOA}' = 1 + \frac{R_{EQ4}}{R_{EQ1}'} \quad (5-8)$$

has increased. In addition to sampled op amp noise stored on C_1' , the increased gain also applies to the noise sampled on C_{CDS} at the end of ϕ_1 . However, the noise due to switches is not sampled on C_{PCDS} , so the transfer function of noise stored on C_1 remains as (R_{EQ4}/R_{EQ1}) .

Due to the different gain seen by the two groups of noise samples, two separate simulations are required to predict the noise performance. The first simulation uses the normal value of R_{EQ1} and the γ factors are derived by considering all broadband noise sources except that from OA1. In the second simulation, R_{EQ1} is replaced by R_{EQ1}' and the γ factors are evaluated by considering the thermal noise of OA1 only. The sum of the output noise power from the two simulations is then added to the noise component due to the sampling action of C_{CDS} to yield the total noise power.

The simulation has been carried out and the results for $f_s = 9.6$ MHz are presented in Figure 5-11. A 2 dB difference is still observed between the measured and simulated data. Similar results are obtained for $f_s = 4.8$ MHz. This implies that there may be other subtle differences between the two modes of operation that cause the level of aliased thermal noise to increase.

Figure 5-11 Simulated versus measured data in CDS mode at 9.6 MHz

Referring to the circuits of Figure 5-9 and 5-10 again, in the non-CDS case, node A is the virtual ground during both clock phases. Power supply noise coupled into this node will appear at the output of the integrator. If the sum of all parasitic capacitances is C_P , the noise sees a voltage gain of C_P/C_{I1} . In the context of a biquad filter, the effect of this noise will be small, as the sampled noise on C_1 and C_4 dominates. In the CDS case, the same situation applies during $\phi 1$ since the circuits are identical. During $\phi 2$, however, noise injected into node A will appear at node C with a gain of C_P/C_{CDS} . Power supply noise coupled into node C by this route is subject to aliasing by C_1 , C_4 and C_{PCDS} , further increasing the circuit noise. Other factors, like the fact that the op amp is temporarily open loop between clock phases when S1, S2, and S4 are all open, may contribute to some additional noise.

Although the principal behind CDS and its implementation seem rather simple, it has been shown that the noise performance of the circuit is complicated by non-ideal conditions combined with subtleties in circuit operation. Despite the increased thermal noise, the merit of CDS is undeniable for voice band applications. For high frequency circuits, the viability of CDS is process and circuit dependent. It can only be assessed by means of a detailed analysis. In this chapter, it has been shown that the proposed noise analysis methodology can be modified to provide a first order estimate of the noise performance of this type of circuit.

Chapter 6

Conclusions

6.1 Summary

The major objective of this thesis is to develop a methodology to perform noise analysis on SC circuits accurately and efficiently. The increasing demand for high performance, wide dynamic range SC circuits has provided the motivation.

Noise in SC circuits has three main origins: thermal noise of op amps, $1/f$ noise of op amps and thermal noise of switches. The nature and modelling aspects of these noise sources were discussed in Chapter 2. Depending on the location of a noise source in a circuit, noise can propagate to the output through either direct coupling or sampled-data signal paths, or both. It was shown that the direct coupling component is generally negligible and its effects can be omitted in determining the noise of a SC circuit. In practical filters, broadband thermal noise from op amps and switches reaching a switched-capacitor is band-limited by the RC network formed by the finite resistance of a switch and the capacitor, or by the UGBW of an op amp. The resulting bandwidth is typically greater than the sampling frequency of the circuit. Consequently, when band-limited thermal noise is sampled, aliasing results. The noise spectral density of undersampled noise on a switched-capacitor is thereby increased.

It was shown in Chapter 2 that under certain conditions the PSD of noise sampled on a switched-capacitor is identical to the PSD

of its continuous time equivalent resistor. The noise model of a SC circuit is simply the continuous time equivalent circuit that the SC version is emulating. This implies that one possible approach to noise analysis of SC circuits is to use a continuous time circuit simulator and equivalent circuits.

A continuous time approach to noise analysis of SC circuits has been presented in Chapter 3. The advantages of this approach are the availability of general purpose continuous time circuit simulators and the built in noise modelling and analysis capabilities. The most important aspect in performing noise analysis is the modelling of the various noise sources. Based on the extensive analysis of the origin of the various components and how they occur in SC circuits presented in Chapter 2, the modelling issues were covered.

The $1/f$ noise of op amps can be accurately simulated by modelling op amps as they are implemented at the transistor level. A switched-capacitor, on the other hand, can sample and alias noise from a number of broadband noise sources. In practical filters these noise sources may be due to switches or op amps. It was shown that the PSD of a switched-capacitor resistor may be different from the PSD of its equivalent resistor and must be modelled properly. This is accomplished by simulating the SC circuit microscopically during each clock phase to determine the extent of aliasing due to each noise source, and then by modelling all the aliased broadband noise sampled on a switched-capacitor as a single white noise source. Since the PSD of this noise source may differ from the PSD of the

continuous equivalent resistor, the circuit simulator has been modified so that the PSD of a resistor can be altered accordingly.

The proposed approach applies to both single-ended and differential circuits. It can also be used to study the power supply rejection capability of SC circuits. The major uncertainty in the accuracy of the approach lies in the modelling of noise sampled onto different capacitors from the same noise source. In this thesis, these samples are assumed to be uncorrelated. This assumption was supported in theory for a special case, presented in Chapter 3, and by extensive experimental data in Chapter 4.

A series of test structures has been fabricated to facilitate experimental validation. The capability to predict and model noise at a continuous MOSFET circuit level and at the SC circuit level were verified. At the MOSFET circuit level, generally good agreement between simulation and measured data has been observed in the areas of circuit and noise performance. Discrepancies are attributed to the failure of the MOSFET transistor model to predict accurately the small signal behavior of short channel devices with high substrate bias. The viability of the noise analysis approach has been verified with extensive measurements of two biquadratic SC filters that are different in implementation. Noise characterization was performed under various operating conditions. In all cases, the matching between measured noise and simulated results obtained using the proposed approach is excellent. The comparison of the two sets of data was provided in Chapter 4.

The low frequency noise reduction technique of correlated double sampling was the subject of Chapter 5. Although not central to this thesis, the topic is relevant to the design of wide dynamic range SC circuits. It was revealed that CDS is effective in removing the the $1/f$ noise dominance of the input referred noise of certain SC filters. However, the additional switches, capacitors and associated parasitic capacitances tend to increase the white noise component of a filter, potentially offsetting the benefits of CDS. It was also shown that with minor modifications, the proposed approach can be used to provide a first order estimate of the noise performance of such more complicated SC circuits.

6.2 Recommendations For Future Work

In the discussion of the limitations of the proposed approach, it was pointed out that the question of correlation among samples on different capacitors due to the same noise source has been overlooked in the literature. This is one area that requires more research in order to get a better understanding of the underlying issues. Knowledge in the area is essential to the development of more accurate models of noise sources.

Another area that is worth pursuing is the integration of the approach into a CAD environment. The work involved includes the automatic generation of the noise models for op amps, translation to the continuous circuits during each clock phase, calculation of the γ factors, and translation to the continuous equivalent circuit for noise

analysis. Such a integrated system would greatly simplify the task of noise performance optimization for SC circuits.

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Appendix A
Layout of Test Structures

Figure A-1 Transistor Array

Figure A-2 Fragmented op amp

Figure A-3 Biquadratic SC filter

END

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