Double Quadrature Mixer for Adaptive System-Level Spur
Cancellation in UWB Radios

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of my thesis, including any required final revisions, as accepted by my examiners. I understand that my thesis may be made electronically available to the public.

Abstract

Direct Digital Synthesizers (DDS) are known to be very spurious due to the use of Digital-to-Analog Convertors (DAC). This thesis presents the phase behaviour of spurs of the commercial AD9912 DDS and its SpurKiller cancellation system. A great variation in spur-carrier phase offset and a large variation of over 20 dB in its increased Spurious-Free Dynamic Range (SFDR) was observed. As a result, an adaptive system is proposed using a Double Quadrature Mixer and a variable phase Local Oscillator (LO). This system is tested at an Intermediate Frequency (IF) of 1.2 GHz, simulating the input of an Ultra-Wideband (UWB) radio. In simulation, an increase in SFDR of 29 dB resulted. In system prototype, an increase in SFDR of 10 dB was achieved. The spur-carrier phase offset was found to be unrelated to the phase of the Double Quadrature LO to achieve maximum spur reduction.

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List of Abbreviations

Abbreviation	Definition
5G	Fifth Generation Wireless
AD9912	<i>Analog Devices</i> Direct Digital Synthesizer
BER	Bit Error Rate
BB	Baseband
BOM	Bill of Materials
BPF	Band Pass Filter
CMC	Canadian Microelectronics Corporation
DAC /ADC	Digital to Analog Converter / (Reverse)
dB	Decibel
dBc	Decibels above the carrier
DDS	Direct Digital Synthesizer
Double Quad	Double Quadrature Mixer
DSP	Digital Signal Processing
FCC	Federal Communications Commission
FFT	Fast-Fourier Transform
FPGA	Field-Programmable Gate Array
IC	Integrated Circuit
IF	Intermediate Frequency
ITAR	International Traffic in Arms Regulations
LO	Local Oscillator
Narrowband	Narrowband
NCO	Numerically-Controlled Oscillator
NLEQ	Non-linear Equalizer
OFDM	Orthogonal Frequency-Division Multiplexing

Abbreviation	Definition
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
RBW	Resolution Bandwidth
Ref DIV	Reference Divider
RF	Radio Frequency
SIR	Signal-to-Interference Ratio
SFDR	Spurious-free Dynamic Range
SOC	System on chip
SPI	Serial Peripheral Interface
UWB	Ultra Wideband (> 500 MHz)
VBW	Video Bandwidth
VCO	Voltage-Controlled Oscillator

Chapter 1: Introduction to Spur Reduction

1.1: Description of Thesis Objectives

Spurs are a significant source of interference in radios. Since the radio spectrum is becoming increasingly dense, improved utilization efficiency is required. Also, as UWB Software-Defined-Radios are more widely used in military applications where small signal detection is important, extremely large Spurious-Free Dynamic Ranges (SFDR) are essential. A spur is a frequency component within the spectrum that is undesired and causes signal quality to degrade. Indoor and dense urban areas are significant areas where spur reduction is essential.

In the commercial wireless industry, 5G (fifth generation) cellular will be deployed starting in 2020, with a strong proposed use of small cell millimetre-wave technology where interference mitigation becomes extremely important [1]. Since the signal quality depends highly on interference, undesired interference such as spurs need to be highly mitigated for the cellular arrays to work, especially in dense wireless environments.

The goal of this thesis is to explore the many sources of spurs within the RF (Radio Frequency) front end (synthesizer, mixer, etc.). Then, instead of mitigating the spurs at the component level, a system-level approach to mitigating spurs will be proposed. This architecture should be adaptable as interference within the spectrum changes depending on user and environmental conditions.

1.2: Signal Quality and SDFR

Spurious-Free Dynamic Range (SFDR) in practical terms is a measure of how well a transceiver can perform in a dense spectrum. Technically, it's the difference in amplitude between the desired signal and the spur or interfering signal with the greatest amplitude. A signal should not only be visible above the noise floor, but also above blockers which can mix with your desired signal and degrade its quality [2] as in Figure 1 and 2 below. An example of using a spur would be in military tactics, involve the jamming of radar (the ship to aircraft link is a jammer), as in Figure 1. Also, channel environments having clutter from environmental effects are always present. Spurs can also be simply generated by the radio itself.

Figure 1: Radar Receiver System Example [3]

Figure 2: Radar Receiver System Interference + Noise Environment [3]

There are significant system-level approaches on mitigating spurs to increase dynamic range as in Figure 2 above. For example, *MIT Lincoln Labs*, a research facility, has produced a Nonlinear Digital Equalizer (NLEQ) shown in Figure 3 below. Based on their complex DSP (Digital Signal Processing) and IC (Integrated Circuit) technology, they were able to significantly improve ADC (Analog-to-Digital Converter) SFDR based on non-linear distortion from the ADC. Instead of working on improving the performance of the analog devices within the radio, the NLEQ works on the digital side. It relies on a highly efficient systolic architecture, a specialized form of parallel computing, and low-threshold voltage digital logic circuits [4]. This NLEQ power efficiency is one thousand times better than typical computer microprocessors. The result is a maximum improvement of 20-25 dB in SFDR as seen in Figure 3 below.

Figure 3: MIT Lincoln Lab's Nonlinear Equalizer Performance [3]

As another example, a commercial enterprise, *Mercury Systems*, specifically its subsidiary *Echotek*, produces an UWB downconverter with a -80 dBc SFDR shown in Figure 4 below [5]. FPGA (Field-Programmable Gate Array) techniques are widely used in this system to reduce spurs, but their exact techniques are not published, and unfortunately ITAR controlled (International Traffic and Arms Regulations). However, its high performance is based on direct digital synthesis, which indicates that they have developed a method on the digital side of the radio front end to mitigate spurs. The only known reference material by *Echotek* is that some of the techniques used were dithering or, digitally implemented NCOs (Numerically-Controlled Oscillators) [6]. The use of FPGAs and dithering are discussed in Chapter 3 as a potential solution for system-level spur cancellation.

Figure 4: Echotek Series RFM-1802RF with Synthesizer ADV-1800S Dual-Channel Wideband Microwave Tuner [5]

The SFDRs discussed above, especially an increase of 20-25 dB is a benchmark for the goal of this thesis. Even though there are powerful circuit based techniques available, the goal of this thesis still remains to add to the library of system-level spur reduction techniques, especially at the lower end of cost and complexity. The NLEQ is not yet commercially available, and the system in Figure 4 is quite expensive and heavily limited to use by the United States Military. The utilization of existing designs will help to create future work as discussed in Chapter 6.

1.3: Sources of Spurs

In Figure 5 below is an example of a spurious IF (Intermediate Frequency) spectrum; the output spectrum of *D-TA Systems'* 9590 UWB receiver that features two DDSs.

Figure 5: Example of a spurious spectrum

Above is the output IF spectrum of the D-TA 9590; at a centre frequency of 1.2 GHz and with a bandwidth of 500 MHz. The RF input in this case, is a low-noise, 5 GHz signal, at -20 dBm input power. The other components within the spectrum are either spurs, as they are undesired and could be seen as jamming, or could be signals of interest. However, the spurs in this spectrum are actually generated from a variety of sources within the radio:

- **Mixing Products:** For example, the LOs within the downconversion process are mixed with RF and LO leakage creating an additional component, which then cascades through the mixing process.
- **Crosstalk:** At high frequencies, traces on the PCB (Printed Circuit Board) as well as metallic components, can act as mini antennas, which can cause reflection and interference.
- **DAC Nonlinearities:** If a DDS is used, its DAC will create both harmonic spurs and non-harmonic spurs. These are created by aliasing and linearity errors respectively.

IC (Integrated Circuit) designers and system designers continually look to reduce the spurs at the source. For example, in Figure 6 below, is a list of the history of ADC design, rate, and associated SFDR. Recently an absolute value of -80 dBc was recorded for a sampling rate exceeding 1 GSamples/sec.

Figure 6: A survey of A/D-Converter performance evolution [7]

However, even with improvement in one source of spurs, others remain. Most are inevitable, and require post-processing to achieve a significant SFDR. Notice in Figure 5 that the spurs are 83 MHz offset from the carrier. In OFDM (Orthogonal Frequency-Division Multiplexing), most subcarriers are 10-20 MHz in width and would be significantly affected by spurs. As channels are being aggregated in cellular 5G, system-level spur reduction becomes increasingly important. In the future, 5G and current military technology may draw similarities.

1.4: UWB Radios

UWB radios (>500 MHz BW) are widely used to search and track signals, especially in military applications, due to their wide spectrum observation. One commercial product by *D-TA Systems*, the D-TA 9590 is shown in Figure 7 below. In the case of UWB radios, synthesizers are often swept so signals can be identified and locked onto [8]. The LO in Figure is DDS-based and is swept to achieve a constant IF frequency of 1.2 GHz. The signal is digitized and then stored in hard drives in the particular application below. As there are several points in this system where spurs could be created, the receiver is the most susceptible and will be the main focus of this thesis, as it uses several UWB mixing stages.

Figure 7: System Application for D-TA 9590 [8]

In a narrowband system, mixers use a limited range of fixed synthesizer frequencies [9]. In this case, one can simply design the radio with a carrier frequency where the spurs created have a large offset frequency and can be filtered out. However, in a UWB sweeping system, a band-pass filter is not the best way of reducing spurs within the 500 MHz band. Therefore, cancellers (removing spurs using destructive interference) have been considered to be better approach [10]. The challenge is determining the phase of a particular spur that will be used to cancel it.

1.5: Direct Digital Synthesizers

DDSs are commonly used in UWB radios that are used for searching and tracking signals within the spectrum [11]. They are known to have microhertz resolution and nanosecond tuning speed. These features are especially important in military applications. The disadvantage of DDSs is that their output is quite spurious. Since the DAC within the DDS has limited resolution, it introduces quantization errors (amplitude and phase), which in combination with aliasing, create harmonic spurs. In addition, DACs have linearity errors, which create non-harmonic spurs. Finally, their switching transients and clock feedthrough are known sources of spurs [12]-[13].

The DDSs used in the D-TA 9590 (*Analog Devices AD9912*) system have a varying SFDR over frequency as shown in Figure 8 below. Its SFDR ranges from -55 to -80 dBc. As a result, to maintain receiver signal quality, and still maintain its speed and resolution, the DDS spurs need to be reduced to achieve a -80 dBc SFDR.

Figure 4. Variation of Wideband SFDR vs. Frequency over DAC Power Supply Voltage, SYSCLK = 1 GHz (SYSCLK PLL Bypassed)

Figure 7. Wideband SFDR at 201.1 MHz, SYSCLK = 1 GHz (SYSCLK PLL Bypassed)

Figure 8: AD9912 Spurious Performance from Data Sheet [14]

1.6: Thesis Overview

Chapter 1 provides an introduction to UWB radio and the causes of spurs. Chapter 2 describes the performance considerations for UWB radio systems. Chapter 2 also describes the UWB Receiver and the DDS that is used as a case study of radio with a spurious spectrum. Chapter 3 describes Harmonic Spur Cancellation, and the limitations of current implementations. Chapter 4 outlines the theory behind the contribution of this thesis, the Double Quadrature Mixer. The Double Quadrature Mixer is simulated to demonstrate its spur reduction capability. Chapter 5 describes the design of a prototype and presents its tested results. Finally, Chapter 6 draws conclusions from the final comparison between simulated and tested results, and presents an outline for future work.

Chapter 2: UWB Receiver Overview and System Hardware

2.1: Background and Common Noise Challenges in UWB

As in Chapter 1, UWB radios are advantageous due to their high data rate. However, internally generated spurs are derived from a variety of sources, and are often problematic [15].

An UWB signal has many forms, for example, a RADAR short pulse, also known as a Gaussian monocycle, is shown in Figure 9 below. Notice that the frequency domain representation of this signal has a BW greater than 6 GHz. Signals such as these have both advantages and disadvantages in wireless communications.

Figure 9: A 500 ps Gaussian monocycle in (a) the time domain and (b) the frequency domain [15]

The FCC's (Federal Communications Commission) power requirement of -41.3 dBm/MHz allows UWB radios to coexist with narrowband radios, depending on the modulation [15]. Also, UWB allows for extremely high data rates, but again, as per the FCC, their transmission is limited to 10 meters of range [15]. This is perfect for future pico-cell mmWave technologies, a proposed candidate for 5G wireless. The Hartley-Shannon capacity formula captures this idea as in (2.1) below. As an example, the target SNR or SFDR is -80 dBc, which allows for a maximum channel capacity (C) of 18.814 Gbits/sec given a BW (B) of 500 MHz for the D-TA 9590.

$$\begin{aligned}
 C &= B \log_2(1 + SNR) & (2.1) \\
 &= (500 \text{ MHz}) \log_2(1 + 10^8) \\
 &= 18.814 \text{ Gbits / sec}
 \end{aligned}$$

From the result, one infers that the channel capacity is not affected strongly by low SNR, and as a result, by low SFDRs. It is the bandwidth that greatly dictates the channel capacity. However, if one is searching the spectrum for an unknown signal, interference becomes suddenly the crucial issue.

UWB systems share the spectrum with narrowband systems. As a result, those narrowband signals will be detected, causing significant interference. In Figure 10 below, is the BER (Bit Error Rate) plot of an UWB system in the presence of a variety of narrowband OFDM interferers. Differences in modulation cause little effect in this example. However, notice that the BER remains virtually

unaffected below -20 dB Signal-to-Interference ratio (SIR). This is realistic in some scenarios, but as the transmission power requirement of narrowband signals can be quite high (approximately -40 dB SIR for example), a robust UWB system must be designed to have effective interference mitigation.

Figure 10: BER vs SNR of UWB system in Narrowband interference [16]

Narrowband interference greatly affects BER, and thus requires a robust UWB receiver in turn. Some of the major system challenges attributed with UWB systems are high-frequency synchronization, multiple-access interference and low transmission power. The difficulties in achieving these challenges are: very fast ADCs, difficult detection (compared to narrowband), and transmission can only extend to short distances. As such, more classical considerations need to be

explored and improved on within the radio such as noise, injection, and synthesis.

By definition phase noise is the frequency ‘skirt’ or ‘roll-off’ of an LO frequency, at a low power level. As UWB signals are typically low power, strong narrowband signals can mix with phase noise and act as blockers. A blocker in the case of UWB would be a narrowband signal that would mix down into the desired IF UWB signal. As an example, suppose we have a minimum UWB IF channel power level ($P_{rf \min}$) of -60 dBm and a narrowband maximum adjacent channel power ($P_{adj \max}$) of -20 dBm. Also, as per Figure 10, for good BER, suppose $SNR_{\min} = 20$ dB. Using the formula [17] to achieve the maximum phase noise ($PN_{\max}$) allowed across a 20 MHz NB BW (OFDM), one must attenuate adjacent NB channels after mixing by (RL_{adj}):

$$\begin{aligned} RL_{adj} &= P_{adj \max} - (P_{rf \min} - SNR_{\min}) \\ &= (-20 \text{ dBm}) - (-60 \text{ dBm} - 20 \text{ dB}) \\ &= 60 \text{ dB} \end{aligned} \tag{2.2}$$

$$\begin{aligned} PN_{\max} &= -RL_{adj} - 10 \log(BW) \text{ dBc} / \text{Hz} \\ &= -(60 \text{ dB}) - 10 \log(20 \text{ MHz}) \\ &= -133 \text{ dBc} / \text{Hz} \end{aligned} \tag{2.3}$$

Notice that in (2.2), the (RL_{adj}) results in 60 dB. But as the narrowband signals need to remain in band for searching, again, filtering is not an option. Alternatively, this means that the total power of the LO signal across the

bandwidth of the narrowband interfering channel must be lower than the UWB signal power by -100 dB, which in (2.3) results in a maximum allowable phase noise of -133 dBc/Hz. This is very low for commercially available synthesizers. For example, the DDS-based LOs used in the D-TA 9590 were measured to have the following phase noise profile below:

Figure 11: Phase noise profile for DDS-based synthesizer within the D-TA 9590

Note that at 1kHz offset, the phase noise was measured to be approximately -100 dBc/Hz. In the presence of narrowband interferers, this LO (used in the UWB D-TA 9590), would cause significant interference, depending on the frequency offset of NB to LO. Also notice the presence of spurs in the phase noise measurement in Figure 11. The combination of these absolutely need to be mitigated, as proposed in this thesis, or else the resulting desired IF channel will

be significantly degraded due to a high BER. Phase noise, and spurs close to the carrier and LO need to be mitigated, and in the case of this thesis, at the system level, as the sources are limitless.

Another challenge in high performance UWB is improving LO injection. For example, in the mixing process of any of the sources within a radio, whether from the LO path or RF path, the LOs used for mixing tend to 'leak' into the main signal path (RF or IF). On NB channels, filtering out this leakage can be achieved using a band-pass filter. But in UWB, filters cannot be used, therefore, LO leakage into the signal chain can mix with all interferers. Preventing this leakage at the IC level is known as isolation. In Figure 12 below, is the LO to IF isolation for a typical RF mixer, with typical performance for its diode-based design. Notice that the minimum isolation, which is considered to be high in this implementation, is roughly 30 dB. This isolation is a representation of the energy being coupled from the LO channel to the IF channel at microwave frequencies [18]. If the LO power used is nominally 17 dBm, the resulting IF leakage at 100 MHz offset would be -13 dBm, resulting in an even lower SIR than desired as in Figure 10 (ex. +27 dB if IF typically at -40 dBm). If at the device level, this leakage cannot be improved, then a system-wide approach to interference will be most useful. The D-TA 9590's DDS-based LO limitations were used as motivation to develop the Double Quadrature Mixer concept.

Figure 12: L-I Isolation for *Mini Circuits* ZX05-17H [19]

2.2: D-TA 9590 UWB Downconverter Design and Performance

The UWB system studied in this thesis is part of D-TA Systems' *RFvision-2*, which includes a receiver (D-TA 9590) and a recorder as in Figure 13 below. The analog section of the receiver will be the scope of the hardware explored in this thesis. The digital side of the D-TA 9590 will be detailed briefly for reference.

Figure 13: System Block Diagram for the D-TA 9590 [8]

Overall, some notable system specifications for the D-TA-9590 are listed below:

- Tuning Range of 500 MHz - 18 GHz, 500 MHz BW
- Tuning Resolution of 10 Hz
- Tuning speed of $10\ \mu s$
- IF Frequency of 1.2 GHz
- Receiver Noise Figure of 15 dB
- ADC SFDR > 63 dB

These specifications are major factors in understanding sources of spurs within the D-TA 9590, and in UWB implementations in general. For the scope of this thesis, the RF chain will be considered. The RF chain of the D-TA 9590, is shown in Figure 14. This includes some control elements as well such as SPI (Serial Peripheral Interface) of the two DDS modules.

Figure 14: RF System Block Diagram for D-TA 9590

The RF Front-End uses two DDS synthesizers that have a DAC and a series of multipliers which generate spurs in the 500 MHz BW IF band of 1.2 GHz. DDS-based LOs (WB DDS) were chosen due to their high frequency resolution ($4\ \mu\text{Hz}$) and an overall tuning speed of $10\ \mu\text{s}$. The WB DDS LOs are derived from three external reference synthesizers of 100 MHz, 3.0 GHz, and 3.3 GHz. Each of these synthesizers have some phase-noise, which carries out through the RF chain. Also, the mixing performed in the WB DDS, contains LO leakage, along with digital spurious issues which will be explored in detail in Chapter 3. In addition to the synthesizers, is a downconverting stage. This downconverter is known to have an SFDR of -60 dBc and a tuning speed of less than $1\ \mu\text{s}$. As in all mixing stages, the LO isolation, due to the significant improvement on the microwave side, is not as much an issue as on the WB DDS. Lastly, the system includes a highly complex and fast IF to BB conversion, and recorder used for data processing. Overall, this UWB receiver is designed as a unique military solution, since speed and accuracy is essential. However, due to the spurious nature of the RF front-end, further interference management is required as means of increased sensitivity. As this system is purely based on system integration, a system-level spur reduction solution is proposed at the IF frequency starting in Chapter 4.

2.2: DDS Design & Performance

In the D-TA 9590, two DDS-based synthesizers are used in the downconversion stage. The architecture for these synthesizers is outlined in Figure 15 below.

Figure 15: D-TA LO Block Diagram [20]

This DDS-based LO above was designed for its high speed and resolution. Notice that synthesis begins with the AD9912 DDS which requires a 1 GHz system clock that the DDS DAC uses to sample the output of the DDS for upconversion. As a result, the DDS produces a fundamental carrier from 100-400 MHz (Image 0) along with its image at 600-900 MHz (Image 1). This is due to the Nyquist Sampling Theorem as illustrated in Figure 16 below.

Figure 16: AD9912 Output Spectrum [14]

The Nyquist limit in this system is 500 MHz ($f_s/2$). As a result, the first image (Image 0) occurs below the sampling frequency of 1 GHz. As suggested in Figure 16 above, external filters are used in the D-TA DDS LO to make use of Image 0 and Image 1 frequencies for upconversion. This occurs in a range of 2.1 GHz - 7.7 GHz by use of mixing, bandpass filtering (BPF) and frequency doubling. Since the AD9912's output is spurious and there are five LOs contributing to the spectrum, an IF signal results as in Figure 17 below. The exact source of these spurs is difficult to trace, and once determined, requires great effort and time, to reduce at its source. This would require an IC redesign. Aliasing, linearity errors, and LO injection are often unavoidable. The approach of this thesis is to post-process the IF spectrum.

Figure 17: Spurious D-TA 9590 Output IF Spectrum

2.3: Chapter Summary

This chapter provides a background on Ultra-Wideband radio (UWB). Based on this, curves are provided to show the relationship between SNR, BER, and NB interference. The effects of phase noise and LO injection on BER are also outlined. This chapter then provides an overview of the hardware (the D-TA 9590) used to study spurs in a UWB radio. Finally, an example of where the majority of the spurs occur in the D-TA 9590 is described. Their sources will be described in detail in Chapter 3.

Chapter 3: Harmonic Spur Cancellation

The basis of this thesis is to develop a system-wide spur cancellation architecture to mitigate spurs at the IF level, rather than to redevelop individual blocks of the RF chain. In UWB communications, the use of filters to remove spurs is not possible when the radio is being used for scanning. However, there are other methods such as cancellation through destructive interference. The *Analog Devices AD9912*, used in the LOs within the D-TA-9590, makes use of a harmonic spur canceller known as “SpurKiller” as an attempt to mitigate spurs. Its analysis is the basis for Chapter 3.

3.1: Analog Devices “SpurKiller” Testing

A form of post-processing that Analog Devices includes on their AD9912 DDS chip is a two channel harmonic spur canceller, known as “SpurKiller” with a programmable phase, as in Figure 18 below.

Figure 18: AD9912 SpurKiller Architecture [14]

Each SpurKiller channel digitally produces a signal aimed to interfere with a spur produced by the DDS chip. The SpurKiller is limited to harmonic spurs and typically reduces only second and third harmonic numbers, based on the frequency tuning word from the accumulator. Also, by setting the gain bit to 1, the cancellation signal is approximately -54 dBc. Then the phase must be set on each channel for maximum cancellation. These two channels are recombined and fed to the input of the DAC on the DDS.

Again, as filters cannot be used to isolate each spur, its phase must be determined empirically. In order to do so, the *Analog Devices* “SpurKiller” algorithm below was used:

1. Determine which offending harmonic spur to reduce and its amplitude
2. Adjust the amplitude of the SpurKiller channel so that it matches the amplitude of the offending spur.
3. Adjust the phase of the SpurKiller channel so that maximum interference is achieved.

The algorithm above was tuned manually using evaluation software to determine the SpurKiller channel phase for maximum destructive interference. The harmonic number was chosen to reduce the harmonic spur with the highest magnitude as per the algorithm. Also, the amplitude multiplier of the SpurKiller channel was found to always be the maximum value of 1 (as input SFDRs were found to be greater than -54 dBc), resulting in maximum reduction. As a result, the skirt of the harmonic cancelling signal was found to additionally eliminate non-harmonic spurs. This testing process is described on the following pages.

To predict the behaviour of these spurs, a more detailed characterization of the spurs around the DDS fundamental (Image 0) (100-400MHz) and the image (Image 1) (600-900MHz) frequencies were measured in steps of 1 MHz. The following test setup was used:

Figure 19: SpurKiller Optimization Setup

The test equipment used was as follows:

- Signal Generators: *Agilent E8257D*, *Rhode & Schwarz SME 06*
- Spectrum Analyzers: *HP 8566A*, *Agilent N1996A*, *Agilent E4408-BAS*
ESA-L
- DC Supply: *GwINSTEK GPC-1850D*
- Shielded cabling and appropriate coaxial connectors were used.

Using the measurement setup above, the frequencies, and power levels of the spurs generated by the fundamental and the image were measured and plotted in the following pages. These intervals were controlled using the AD9912 evaluation software included with the evaluation board (PCBZ). The following software settings were used, as in Figure 20 below:

Figure 20 - AD9912 DDS Evaluation board Driver Software

Notice that in Figure 20, the external clock was set to 1 GHz as mentioned previously with a DDS output of 100 MHz. Internal multipliers were not used. This output frequency (100 MHz above) was stepped by 1 MHz and measured as below.

First, the minimum frequency offset between the closest spur and its respective carrier was plotted in Figure 21. The minimum offset was measured since the filter after the AD9912 in Figure 15 has a BW of 300 MHz. Note the red square in the plots below; this is the region where the spur would be at a frequency within the passband of the filter of the D-TA LO. In Figure 21, this red area has a width of around 130 MHz, half the BW of the BPF in the D-TA LO. This region is where the spurs cannot be filtered. The goal using SpurKiller would be to focus on reducing spurs at these frequency offsets from the carrier. But

ultimately, spurs outside the filter could be brought back in-band through mixing. Thus cancellation across the entire DDS band needs to be considered.

Figure 21 - AD9912 Output Frequency Offset from the Carrier: Image 0 (Fundamental) , Image 1

As the SpurKiller algorithm requires the phase knowledge of spurs, the phase over frequency behaviour of the spurs was characterized. Using the same setup above, the spur-carrier phase offset was measured at the point where maximum spur reduction occurs within the 130 MHz BW above. In the characterization, three instances of the same AD9912 chip batch number were used in three identical modules of the D-TA LOs. Using the algorithm with the controls in Figure 20, and Figure 22 below, the phase of the minimum offset spur was determined at the point of maximum reduction, through trial and error. In Figure 22, one can control the harmonic multiple of each SpurKiller channel, and change its phase relative to the carrier. The phase offset was stepped though to determine where maximum spur cancellation occurred at a given DDS frequency.

Figure 22 - Harmonic Spur Reduction Controller for AD9912

As a result, in Figure 23 below, one notices that there is significant variation in the SpurKiller channel phase. Note that in the experiment, four individual plots (two SpurKiller cancellation channels for two DDS bands) were created but SpurKiller Channel 1 (i.e. “Spur A” in Figure 22 above), DDS Image 0 (100-400 MHz) had the largest variation in phase. The resolution of the plot is limited as 1 MHz steps were used. Also, the quantization in frequency occurs as the spur harmonic number changes suddenly when the previous SpurKiller harmonic number (two to three) no longer has an effect on the SFDR. The quantization in phase is due to simplification of trial an error; only a few degree steps were taken within a 10-20 degree range.

Figure 23 - DDS Channel 1 Phase vs. Frequency Image 0 for 3 D-TA LO Boards

The harmonic spur canceller module that is part of the IC is limited to harmonic multiples of the carrier. In sequence, spurs are modified variably with phase and frequency. Even whilst characterizing the same batch of IC, the amount of reduction as seen in Figure 23 below varies from 10-30 dB (-50 to -70 dBc SFDR). This was achieved by trial and error which is imprecise and impractical for complex systems. In future work, a PLL could have been used to track each spur, and automate the SpurKiller algorithm. At the analog level of the DDS chip, a series of techniques were found to help improve this imprecision, but as described in the next section, did not prove to be effective.

Figure 24 - Achieved Reduction in SFDR

3.2: Discussion of “Spur Killer” and Alternatives

The AD9912 DDS was originally chosen for its low cost and its high performance. However, through the testing of its evaluation board, the DDS was proven not have an SFDR of -60 dBc. In Section 3.1 above, the DDS was found to have spurs up to -48 dBc. However, these spurs were not harmonic in nature, they were derived from intermodulation. When SpurKiller was used, it didn't eliminate any of the non-harmonic spurs. Non-harmonic spurs were generated as follows, as per an *Analog Devices* application note:

“The frequency offset of the spur relative to the fundamental varies with a change in the DDS tuning word, then the DDS/DAC is most likely the source of the spur. Discovery of the spur's source is facilitated by ensuring that the frequency tuning word change includes changes in both the truncated and untruncated parts of the frequency tuning word” [21].

On the DDS evaluation board, the frequency tuning word was observed, and it did change as stated above, but the spurs still remained at the output. Alternative spur reduction techniques were to use six individual power supplies for noise isolation. These techniques were performed and a 10dB reduction in the power levels was not observed, as anticipated [22]. Lastly, other known methods of reducing spurs were explored [23] including:

- using 950 MHz, 1050 MHz Clocks
- Reducing the DAC current

- Using the Clock Multiplier in the AD9912 driver software

None of these suggestions reduced the spurs. After mixed results on the AD9912, the AD9858 was thought to prove to be a better choice of DDS, but it quotes the same SFDR in its specification, of -60dBc [24].

Overall, the AD9912 is a fast option for LO synthesis, however, even after testing all known spur reduction techniques, it does not prove to have a suitable SFDR for military application (-80 dBc as suggested in Chapter 1). The AD9912 is another example of a system component that has a highly spurious output.

3.3: FPGA Spur Reduction

An analog solution to the spurs of the AD9912 is not suitable for high SFDR UWB communication. However, as outlined in Chapter 1, digitally implemented LOs may prove to have greater SFDRs, as commercially advertised. *Mercury Computer Systems (Echotek RF 1800GT Wideband Microwave Tuner)* has a competing device to the D-TA 9590. They state their device as having a “patented spur-reduction technique” that creates an SFDR of -80 dBc. A large number of them use *Xilinx VIRTEX* chips, as shown in Figure 25 [5][25].

Figure 25 - Echotek Series DCM-V6-4R160-1T1000-XMC Module [25]

Using the *VIRTEX 7* Chip and its DDS *LogicCore* IP would allow the 100-400 MHz frequencies to be generated. This software supports an SFDR of -150 dBc. It uses phase dithering (reducing quantization error) and Taylor Series correction (a form of cancellation) as options to increase the SFDR [26]. Figure 26 below is a representation of the architecture of the *Mercury* DDS. However all DDS require the use of a DAC, and a DAC has spurs, as in Figure 6. Also, current DAC implementations are limited to a few GBits/sec.

Figure 26 - Echotek RF 1800GT Wideband Microwave Tuner Block Diagram [27]

As 60 GHz radios become more prevalent in use, the FPGA realization of an adaptive spur cancellation system is not realistic [26] due to processor speed limitation (the *LogicCore* can only generate sub-GHz frequencies). It also has poor phase noise, and tuning speed [26]. Even if the low frequencies are synthesized and upconverted by the costly *VIRTEX 7 FPGA*, other sources of spurs remain, including LO injection. Preventing these analog issues, again, requires increased complexity, and cost at the device level. Also, the FPGA and Core cost together nearly \$5000, far too costly for mobile devices. As there are many challenges, a system-level approach is required, so that it could be adaptive for a variety of wireless applications, not just military.

3.4: Chapter Summary

This chapter explores two digital implementations of known spur reduction techniques including harmonic spur cancellation, and dithering. The *Analog Devices* “SpurKiller” only allows, on average an SFDR of -48 dBc. The *Xilinx* DDS Core permits some SFDRs as high as -150 dBc, but only with increased upconversion cost, and complexity. Only a simpler solution would be appropriate for commercial solution. The solution that is proposed is a mixer that adaptively eliminates spurs as a form of IF post-processing. The following section proposes a Double Quadrature Mixer for Adaptive System-Level Spur Cancellation in UWB Radios.

Chapter 4: Double Quadrature Mixer Theory and Simulation

As the challenges of UWB, DDS, and current harmonic spur cancellation techniques were discussed in Chapters 1-3, it became apparent that a system-level approach might prove to be a better solution. This chapter introduces the theory of the proposed Double Quadrature Mixer, an IF post-processing architecture. The design goals, again, are to achieve an additional 10-20 dB SFDR given the use of the AD9912's "SpurKiller," whilst maintaining the original tuning speed (10 us), the use of DDSs, a BW of 500 MHz, and an IF frequency of 1.2 GHz as in the D-TA 9590 discussed in Chapter 2.

4.1: Double Quadrature Mixer Theory

To cancel spurs more effectively, a second IF stage is introduced with variable LO phase, as in Figure 27 below, known as the Double Quadrature Mixer [28]. It should be designed to have a fixed LO, for example a low phase noise PLL, with a very high SFDR so that additional spurs aren't introduced. This architecture makes use of two stage I and Q channels that are mathematically operated on (as in the addition and subtraction blocks) so that the spurs are cancelled and filtered at the output (I and Q Channel 1). Lastly, the final mixing stage upconverts the output so that the original IF frequency is maintained.

Figure 27 - Double Quadrature Mixer: Functional Block Diagram

The mathematical operation of this architecture is represented in (4.1)-(4.10) below. First, suppose at the input, the signal is demodulated, resulting in I and Q channels in quadrature (4.1 and 4.2 respectively). The quadrature is represented by the use of sine and cosine functions, as the I and Q channels are 90° apart. Also, the spurs are coherently related to the carrier, and are 90° offset from the carrier with the use of sine and cosine functions. This phase offset is the ideal case where maximum cancellation occurs (fixed phase and frequency offset from the carrier). There are two spurs in each channel, with identical phase offset from the carrier, but at higher and lower equidistant frequencies. The frequency is embedded in the overall phase of each term as explained with the note below (4.2) :

$$IF_I = \sin(\theta_{spur_low}) + \cos(\theta_{carrier}) + \sin(\theta_{spur_high}) \quad (4.1)$$

$$IF_Q = \cos(\theta_{spur_low}) + \sin(\theta_{carrier}) + \cos(\theta_{spur_high}) \quad (4.2)$$

where $\theta_x = 2\pi * f_x$ and the phase offsets are embedded in the use of sin and cos.

Then, the Double Quadrature mixing is represented by (4.3) and (4.4) below. In the I Channel, an addition of mixing products between the phase shifted LO and the input occurs (4.3). Similarly, in the Q Channel, a subtraction of mixing products between the phase shifted LO and the input occurs (4.3). As a result of this operation, and as the spurs are 90° offset from the carrier, maximum cancellation occurs when the Phase Shift A = 0° and B = 90° [28] as proven in the calculation of (4.7, 4.10). The LO shifted by A is represented by a sine, and B, by a cosine.

$$IF_{-1_I} = \sin(\theta_{LO}) * IF_Q + \cos(\theta_{LO}) * IF_I \quad (4.3)$$

$$IF_{-1_Q} = \cos(\theta_{LO}) * IF_Q - \sin(\theta_{LO}) * IF_I \quad (4.4)$$

If (4.1) is substituted into (4.3), and the multiplication is expanded into mixing products using trigonometric identities [29], a series of cancellations occur. Notice the upconverted products in (4.5) are underlined in red, and the downconverted products are underlined in blue. Some of the resulting mixing products are identical in amplitude and frequency. Also, some of those products are also 180° in phase offset. Those terms cancel each other out by destructive interference, as indicated by a strikethrough in (4.6). As a result, in (4.7), remains an upconverted ($\theta_{LO} + \theta_{spur}$) spectrum where the carrier is eliminated by destructive interference. Similarly, a downconverted spectrum ($\theta_{LO} - \theta_{carrier}$) also results where the spurs are eliminated. This destructive interference is a result of phase shifts caused by sine and cosine multiplication [29].

$$IF_{-1_I} = \sin(\theta_{LO}) * IF_Q + \cos(\theta_{LO}) * IF_I \quad (4.3)$$

$$\begin{aligned}
&= \frac{1}{2} \sin(\theta_{LO} + \theta_{spur_low}) + \frac{1}{2} \sin(\theta_{LO} - \theta_{spur_low}) + \frac{1}{2} \cos(\theta_{LO} - \theta_{carrier}) \\
&\quad - \frac{1}{2} \cos(\theta_{LO} + \theta_{carrier}) + \frac{1}{2} \sin(\theta_{LO} + \theta_{spur_high}) + \frac{1}{2} \sin(\theta_{LO} - \theta_{spur_high}) \\
&\quad + \frac{1}{2} \sin(\theta_{LO} + \theta_{spur_low}) - \frac{1}{2} \sin(\theta_{LO} - \theta_{spur_low}) + \frac{1}{2} \cos(\theta_{LO} - \theta_{carrier}) \\
&\quad + \frac{1}{2} \cos(\theta_{LO} + \theta_{carrier}) + \frac{1}{2} \sin(\theta_{LO} + \theta_{spur_high}) - \frac{1}{2} \sin(\theta_{LO} - \theta_{spur_high})
\end{aligned} \quad (4.5)$$

$$\begin{aligned}
&= \frac{1}{2} \sin(\theta_{LO} + \theta_{spur_low}) + \cancel{\frac{1}{2} \sin(\theta_{LO} - \theta_{spur_low})} + \frac{1}{2} \cos(\theta_{LO} - \theta_{carrier}) \\
&\quad - \cancel{\frac{1}{2} \cos(\theta_{LO} + \theta_{carrier})} + \frac{1}{2} \sin(\theta_{LO} + \theta_{spur_high}) + \cancel{\frac{1}{2} \sin(\theta_{LO} - \theta_{spur_high})} \\
&\quad + \frac{1}{2} \sin(\theta_{LO} + \theta_{spur_low}) - \cancel{\frac{1}{2} \sin(\theta_{LO} - \theta_{spur_low})} + \frac{1}{2} \cos(\theta_{LO} - \theta_{carrier}) \\
&\quad + \cancel{\frac{1}{2} \cos(\theta_{LO} + \theta_{carrier})} + \frac{1}{2} \sin(\theta_{LO} + \theta_{spur_high}) - \cancel{\frac{1}{2} \sin(\theta_{LO} - \theta_{spur_high})}
\end{aligned} \quad (4.6)$$

$$\begin{aligned}
IF_{-1_I} &= \underbrace{\sin(\theta_{LO} + \theta_{spur_low})}_{\text{Up}} + \underbrace{\cos(\theta_{LO} - \theta_{carrier})}_{\text{Down}} + \underbrace{\sin(\theta_{LO} + \theta_{spur_high})}_{\text{Up}}
\end{aligned} \quad (4.7)$$

And similarly, given a subtraction in the Q channel (4.4), the same cancellation of mixing products occurs in (4.9) with the spurs upconverted, and the carrier downconverted (4.10).

$$IF_{-1Q} = \cos(\theta_{LO}) * IF_Q - \sin(\theta_{LO}) * IF_I \quad (4.4)$$

$$= \frac{1}{2} \cos(\theta_{LO} - \theta_{spur_low}) + \frac{1}{2} \cos(\theta_{LO} + \theta_{spur_low}) + \frac{1}{2} \sin(\theta_{LO} + \theta_{carrier}) \quad (4.8)$$

$$- \frac{1}{2} \sin(\theta_{LO} - \theta_{carrier}) + \frac{1}{2} \cos(\theta_{LO} - \theta_{spur_high}) + \frac{1}{2} \cos(\theta_{LO} + \theta_{spur_high})$$

$$- \frac{1}{2} \cos(\theta_{LO} - \theta_{spur_low}) + \frac{1}{2} \cos(\theta_{LO} + \theta_{spur_low}) - \frac{1}{2} \sin(\theta_{LO} + \theta_{carrier})$$

$$- \frac{1}{2} \sin(\theta_{LO} - \theta_{carrier}) + - \frac{1}{2} \cos(\theta_{LO} - \theta_{spur_low}) + \frac{1}{2} \cos(\theta_{LO} + \theta_{spur_low})$$

$$= \frac{1}{2} \cos(\theta_{LO} - \theta_{spur_low}) + \frac{1}{2} \cos(\theta_{LO} + \theta_{spur_low}) + \frac{1}{2} \sin(\theta_{LO} + \theta_{carrier}) \quad (4.9)$$

$$- \frac{1}{2} \sin(\theta_{LO} - \theta_{carrier}) + \frac{1}{2} \cos(\theta_{LO} - \theta_{spur_high}) + \frac{1}{2} \cos(\theta_{LO} + \theta_{spur_high})$$

$$- \frac{1}{2} \cos(\theta_{LO} - \theta_{spur_low}) + \frac{1}{2} \cos(\theta_{LO} + \theta_{spur_low}) - \frac{1}{2} \sin(\theta_{LO} + \theta_{carrier})$$

$$- \frac{1}{2} \sin(\theta_{LO} - \theta_{carrier}) + - \frac{1}{2} \cos(\theta_{LO} - \theta_{spur_low}) + \frac{1}{2} \cos(\theta_{LO} + \theta_{spur_low})$$

$$IF_{-1Q} = \cos(\theta_{LO} + \theta_{spur_low}) - \sin(\theta_{LO} - \theta_{carrier}) + \cos(\theta_{LO} + \theta_{spur_high}) \quad (4.10)$$

Up Down Up

Overall, the spurs are completely cancelled out at the downconverted frequency of “I Channel 1” and “Q Channel 1” (see Figure 27) and the spurs remain only at the upconverted frequency summarized in (4.7) and (4.10).

$$IF_{-1I} = \sin(\theta_{LO} + \theta_{spur_low}) + \cos(\theta_{LO} - \theta_{carrier}) + \sin(\theta_{LO} + \theta_{spur_high}) \quad (4.7)$$

$$IF_{-1Q} = \cos(\theta_{LO} + \theta_{spur_low}) - \sin(\theta_{LO} - \theta_{carrier}) + \cos(\theta_{LO} + \theta_{spur_high}) \quad (4.10)$$

At this point, the spurs can be easily filtered out (using a BPF as in Figure 27) given the LO frequency is greater than half the tuning BW. In Section 4.2, this filtering will be done outside the 500 MHz IF BW of the UWB radio. After filtering, the remaining carrier is simply upconverted back up to the input IF frequency. Overall, given the spurs and the phase shifted LO are of equal magnitude, spurs

can be completely cancelled out. But in a simulated noisy environment, complete cancellation will not be as ideal.

4.3: Simulation Design

The system in Figure 28 below was simulated in MATLAB using an input IF spectrum with a 1.2 GHz carrier and two non-harmonic spurs offset from the carrier by 20 MHz, and an SFDR of -40 dBc, as in Figure 30. The MATLAB code for this input begins starting with Figure 29 and ends at Figure 36 with supplementary information in Appendix A. Note that in simulation, the input is demodulated and additional amplification has been added on the output as in Figure 28, differing from Figure 27.

Figure 28 - Modified Double Quad Digram for Simulation

In Appendix A, the individual code blocks in the schematic above are written as functions such as FFT, LO, and amplifiers. These code blocks add noise, phase noise, and appropriate phase shifts to the system. Their function

calls are described in the main code on the following pages. First, in Figure 29 below, the time variables are set up as input parameters to the FFT. A time step size (tstep variable) of 10 ns, and a simulation length (time variable) of 1 ms are provided. In MATLAB, a custom FFT function (fft_pwr() in Figure 31) takes this variable to sample the time domain variables at 100 Msamples/sec. These were estimated to simulate a noise floor of roughly -60 dBm at a 2 MHz resolution bandwidth (RBW), typical for spectrum analyzers used for measurement of UWB spurious spectrum.

```
tstep = 1e-10;
time = 0:tstep:1e-3;

NoiseFloor=-174+10*log10(2e6)

LO_IF_I = LO_Imp_I(0,268e6,-110, -130,0.5e6,10e6,
-1500,time,tstep, 0); % very low phase noise and spurs to model
ideal LO signal
LO_IF_Q= LO_Imp_Q(0,268e6,-110, -130,0.5e6,10e6,
-1500,time,tstep, 0); % very low phase noise and spurs to model
ideal LO signal

IF_I = 1e-2*sin(2*pi*1.22e9.*time)+1e-2*sin(2*pi*1.18e9.*time)
+1*cos(2*pi*1.2e9.*time)+ wgn(1, length(time), -110 +
10*log10(1/(2*tstep)), 1, 'dBW');
IF_Q = 1e-2*cos(2*pi*1.22e9.*time)+1e-2*cos(2*pi*1.18e9.*time)
+1*sin(2*pi*1.2e9.*time)+ wgn(1, length(time), -110 +
10*log10(1/(2*tstep)), 1, 'dBW');
```

Figure 29 - Double Quad Main Function: Instantiation

Continuing in Figure 29, the non-ideal LOs (LO_IF_I and LO_IF_Q variables) are instantiated with a frequency of 268 MHz, necessary to upconvert and downconvert the spectrum outside of the original 500 MHz bandwidth for an UWB radio. Essentially, the spur reduction is performed out of band, and the

resultant signals are mixed back in band. The LO in and out-band noise floors were set to be quite low, at -110 and -130 dBm respectively, with a 1 MHz phase noise BW. Lastly, the LO spurs were omitted with function parameter of -1500 dBc, which is approximately infinitesimally small. This is the ideal case, when the Double Quad LO does not generate any additional spurs. Note that the difference between LO_Imp_Q() and I() is 90° as explained in Section 4.1. This is performed within the LO_Imp_Q() as in Appendix A. Then, lastly, in Figure 29, the input I and Q channels are instantiated using trigonometric functions. As mentioned above, the demodulated input channels, I and Q are 90° apart through the use of sine and cosine functions. The carrier, as in the D-TA 9590 spectrum is set at 1.2 GHz with spurs at 20 MHz offset at -20 dBc. This simulates the output IF spectrum of the D-TA 9590 as in Figure 17 where the strongest spur is 83 MHz offset at an SFDR of -45 dBc. The spurs in the spectrum below were chosen to be greater in amplitude and closer in offset frequency as an example worst case scenario. For maximum cancellation, the phase offset from the carrier of the simulated spurs is set to be 90° (as sine is used for the carrier, and cosine for the spur). However, the spur-carrier phase offsets of the D-TA 9590 IF spectrum is unknown. Lastly, the noise floor is established using a white-gaussian noise function, `wgn()`, high time resolution, resulting in a non-dominating (FFT is dominant) noise floor of -130 dBm. After performing the FFT, using the code in Appendix A, the input spectrum below in Figure 30 results:

Figure 30 - Input I and Q Channels with added spurs

As in the mathematical description of the Double Quadrature Mixer in Section 4.2, the input I and Q channels are operated on in Figure 31 below. After adding and subtracting the appropriate mixing products, the upconverted spurious spectrum is then filtered out (as described in section 4.1). The filter was chosen (extremely ideal for proof of concept) to be a Chebyshev, band-pass filter with a BW from 682 MHz - 1.182 MHz. This specific BW was chosen as a 500 MHz IF BW downconverted by 268 MHz, the Double-Quad LO frequency (as specified in the `fdesign.bandpass()` call). This filters out the upconverted spurs as discussed in Section 4.1. A sixth order filter was chosen for extreme ideality, with a ripple of 0.1, and a sampling rate of 10 GHz, reflecting the time step used in the simulation. The spectrum was filtered multiple times for numerical accuracy.

```

IF_II = LO_IF_I.*IF_I;
IF_IQ = LO_IF_Q.*IF_I;
IF_QI = LO_IF_I.*IF_Q;
IF_QQ = LO_IF_Q.*IF_Q;

IF_I_Double = IF_II + IF_QQ;
IF_Q_Double = IF_QI - IF_IQ;

%IF Filter
d = fdesign.bandpass('N,Fp1,Fp2,Ap',6,682E6,1182E6,0.1,1e10);
f = design(d, 'cheby1');
IFfiltered = filter(f,IF_I_Double);
IFfiltered = filter(f,IFfiltered);
IFfiltered = filter(f,IFfiltered);
IFfiltered = filter(f,IFfiltered);

IF_Q_filtered = filter(f,IF_Q_Double);
IF_Q_filtered = filter(f,IF_Q_filtered);
IF_Q_filtered = filter(f,IF_Q_filtered);
IF_Q_filtered = filter(f,IF_Q_filtered);

[freq, pwr_IFfiltered] = fft_pwr(tstep, IFfiltered, 50);

```

Figure 31 - Main Code: I and Q manipulation and BPF

As a result of the code above, the filtered I Channel spectrum after the Double Quad is shown in Figure 32 below. Note that in the passband of the filter, only the carrier remains and at the upper end of the spectrum, the spurs remain, which are then filtered out.

Figure 32 - Double Quad: Channel I post-BPF

The final stage, in Figure 33 below, of the Double Quad is an upconversion back to the original IF frequency of 1.2 GHz. This can be modified depending on the application. Lastly, each channel is amplified (with the `amplifier_simon()` functions) by 5 dB to maintain the original carrier power of 0 dBm, but can easily be adjusted as needed. Also the mixers were simulated to have an IIP3 of 80 dBm, IIP2 of 150 dBm, and a noise figure of 0 dB to simulate an extreme ideal case. Also, harmonics generated by the mixers were omitted such that the original spurs could be identified in the cancellation process. In future work, realistic values should be used, especially simulation at the transistor level.

```

IF_I = IFfiltered.*LO_IF_I;
IF_Q = IF_Q_filtered.*LO_IF_Q;

GaindBMixer = 5;
% IF = amplifier_simon(IF,GaindBMixer,IIP3Mixer,IIP3Mixer
+15,NFMixer,tstep);
IF_I = amplifier_simon(IF_I,GaindBMixer,80,150,0,tstep); %
very high linearity and zero noise to model ideal amplifier
IF_Q = amplifier_simon(IF_Q,GaindBMixer,80,150,0,tstep);

```

Figure 33 - Double Quad: Final Upconversion

4.4: Simulation Results

After the final upconversion and amplification stage, an increase of 29 dB in SFDR resulted in both channels, as in Figure 34 below. Due to the choice of gain, a conversion loss of 20 dB resulted due to the loss embedded into the mixer code blocks in Appendix A. This occurs in both I and Q channels. Note the top graph in green is the result having only used a single downconversion stage, essentially the input, displayed for comparison. Overall, this is a significant improvement for system-level spur reduction, even in the situation where the spurs are 90° offset from the carrier in both I and Q channels. However, note that the magnitudes of I and Q channel spurs and carriers are equal. In terms of modulation, in theory, the constellation points where maximum phase cancellation occurs are at odd multiples of absolute spur phase of 45°, for example QPSK modulation. But as constellation density in modern spectrum can have hundreds of points, phase variation of the Double Quadrature Mixer should be explored. This system needs to adapt to variations in modulation scheme.

Figure 34: Double Quad Final Results Comparison

4.5: Phase Variation

To characterize the Double Quadrature Mixer's phase variation and its adaptability, the modulation path on the 64 QAM constellation in Figure 35 was followed, for proof of concept by modifying the spur I and Q amplitudes in the code in Figure 36 below. The input I and Q channel amplitudes are equal as described in the ideal case in the previous section. The red dots in Figure 35 below indicate these points. If the carrier phase is 90° offset from the spur, maximum cancellation occurs.

Figure 35: Constellation Followed for Simulated Phase Variation

```

IF_I = 7e-2*sin(2*pi*1.22e9.*(time))
+7e-2*sin(2*pi*1.18e9.*(time))+1*cos(2*pi*1.2e9.*time)+wgn (1,
length(time), -110 + 10*log10(1/(2*tstep)), 1,'dBW');

IF_Q =
-1e-2*cos(2*pi*1.22e9.*(time))-1e-2*cos(2*pi*1.18e9.*(time))
+1*sin(2*pi*1.2e9.*time)+wgn (1, length(time), -110 +
10*log10(1/(2*tstep)), 1,'dBW');

```

Figure 36: Code for Constellation Phase Variation

Recall that the carrier frequency is 1.2 GHz and the spurs are at 1.22 and 1.18 GHz, as in Figure 34 above. The frequency dependence in this scenario was not explored, and assumed to be coherent with the carrier. For simplicity, the carrier phase is kept approximately at 45° ($I = +1e-2$ V, $Q = +1e-2$ V), and the spur phase, for example in Figure 36, in the sweep, is at 351° ($I = +7e-2$ V, $Q = -1e-2$ V). Thus, the spur-carrier phase offset, with this example is 54° , where improvement is only 5 dB. Following all the points on the constellation, including the red ideal case, SFDR improvement was plotted over spur-carrier phase offset in Figure 37 below. Notice that contrary to the original hypothesis, the peak values in the plot occur only at $\pm 90^\circ$. Notice, max SFDR improvement is 40 dB instead of 30 dB. This is due to the fact that at 30 dB improvement, the input SFDR was -39 dBc, however at 40 dB, it was -29 dBc. This resulted since the I and Q magnitudes were larger in the constellation sweep.

Figure 37: SFDR Improvement vs Constellation Phase Spur Offset

Notice also in Figure 37, in some instances such as when the spur phase offset is -40° as in the example code, SFDR improvement is negative. This is due to constructive interference. In practicality, the Phase Shifts A and B (recall ideally, $A = 0$ and $B = 90^\circ$) would have to be adjusted to offset the I and Q phase mismatch, thus tracking the phase of the spurs, to maximize destructive interference. This phase mismatch is caused by the S-parameters between components on a PCB, and will be discussed in Chapter 5. As constellation points are changed at the designed modulation rate, the Phase Shifts A and B would need to have a fast response time. The simulated phase response serves as a reference for the phase response of the prototype in Chapter 5. This work

will also help serve as a guide for future work in the effects of modulation on the Double Quadrature Mixer. Overall, as long as the spur phase offset remains within $\pm (70-110)^\circ$ from the carrier, the goal of increased SFDR of 10 dB will be achieved, as verified in Chapter 5.

4.6: Chapter Summary

This chapter introduces the concept of the Double Quadrature Mixer to significantly reduce non-harmonic spurs that in the ideal case are 90° offset in phase from the carrier. Using MATLAB simulation, a 29 dB improvement in SFDR was achieved. This chapter also verifies that a $\pm (70-110)^\circ$ spur phase offset from the carrier would prove to achieve the desired minimum 10 dB improvement in SFDR. This will be verified in a hardware prototype in Chapter 5.

Chapter 5: Prototype and Testing

After significant results were simulated, a Double Quadrature Mixer prototype using block elements was designed, as an integrated circuit design was avoided due to time limitations. The list of block elements is provided in Table 1 on the following page. Figure 38 below is the final revision of this prototype based on the optimization process outlined in this chapter. The tests performed in this thesis were to verify the maximum improvement in SFDR of the prototype and to compare it to the simulated results in Chapter 4. Also, tests verify the SFDR as the Phase Shift B is varied across its range to track the phase offset of the spur to the carrier. In the earlier stages of testing, the D-TA 9590 UWB receiver with two DDS-based LOs was used as input. Later, as in Figure 38, a DDS-based LO D-TA evaluation board was used as input (platform on the left below).

Figure 38 - Full Testing Setup for Double Quadrature Mixer

5.1: Equipment Selection

The Double Quadrature Mixer on the right of Figure 38 above was prototyped based on Figure 39 below using *Mini-Circuits* and *Analog Devices* components. Given the spurious D-TA 9590 output of 1.2 GHz, an initial frequency plan of 1200 MHz downconverted to 1060 MHz and then upconverted to 1200 MHz was designed. Note that below, the demodulator (ADRF6820) requires an external reference signal, which was chosen as 2 GHz, +4 dBm, later optimized for the demodulator's internal LO. This internal LO is a fractional-N PLL with VCO (Voltage-Controlled Oscillator). The demodulator evaluation board allows the PLL's internal settings to be programmed to minimize noise and are optimized in Section 5.2 below. The LO was chosen to be 140 MHz, +10 dBm, based on the frequency range of the phase shifters (*Mini Circuits* JSPHS-150). Unfortunately, *Mini Circuits* doesn't produce phase shifter blocks capable of operating at 268 MHz as designed in simulation in Chapter 4.

Figure 39 - Double Quad Prototype Block Diagram

Thus the equipment list in Table 1 below was purchased and consolidated.

TABLE 1 - DOUBLE PROTOTYPE BILL OF MATERIALS (BOM)

Type	Legend	Part Number	Spec	Price	Supplier
Demod. (1)	A	ADRF6820		\$200	Analog Devices
Op Amp Eval Board		AD8045ARD-EBZ	600 MHz	\$55	Analog Devices
Op Amp		AD8045	SOIC	\$9	Analog Devices
Power Conn	B	22-23-2031	x10	3.52	Mouser
Mate Conn	B	22-01-2037	x20	4.22	Mouser
		08-50-0113	x100	4.5	Mouser
		22-03-2031	x10	1.37	Mouser
Filter (x2)	C	BPF-A950+		\$60	Mini Circuits
Filter Test Board (x2)	C	TB-363+		\$60	Mini Circuits
Doubler		ZX90-2-11+	20 dB Loss Tested	\$36	Mini Circuits
Doubler		MK-3BR		\$50	Mini Circuits
Amplifiers	D	ZX60-3011+	10-20 dB, 600-1200 MHz		
Mixers (x6)	E	ZX05-17H-S		\$84	Mini Circuits
Phase Shifters (x2)	F	JSPHS-150		\$70	Mini Circuits
Test Board (x2)	F	TB-152+		\$60	Mini Circuits
Adder	G	ZFRSC-42-5+			
Subtractor	H	ZAPDJ-2		\$82	Mini Circuits
Total:				779.61	

Test boards (for the operational amplifiers (op-amp), the phase shifters, and the filters) were purchased and populated, for example, with a 1:1 feedback network for the op-amps. High frequency op-amps were chosen initially to convert the differential outputs of the demodulator to single-ended outputs. However, their harmonic performance turned out to be quite poor, so the output positive

connectors of the demodulator were connected as single-ended with the negative ends terminated instead (as suggested in the datasheet). Also, the doubler's outputs were found to be quite spurious; their harmonics would mix with other spurs, and were omitted. Both the phase shifters and the demodulator were known to attenuate the signal quite severely, and thus, cascaded amplifiers were added resulting in 22 and 36 dB in LO and IF gain respectively. The mixers chosen (ZX05-17H-S, 100-1700 MHz, ~36 dB I-R Isolation) were considered to have high isolation, but in the following sections, posed as a limiting factor for SFDR improvement. Mixer harmonics were not considered, but affected the final results. The adder and subtracter (90°) were chosen with a BW of 1000-2000 MHz, and an isolation of 26 dB, affecting SFDR. Lastly a BPF (700-1200 MHz) was chosen to filter out the upconverted spurs (centred around 1340 MHz). The system was then connected and built as shown in Figure 40 with the corresponding legend in Table 1. Notice that the overall cost was \$800, far less than the \$5000 FPGA solution discussed in Chapter 1. This prototype cost could only be further reduced after an integrated circuit is developed in future work, for example.

Figure 40 - Built Double Quad Prototype

To begin testing the prototype, the D-TA 9590's IF output of 1.2 GHz as in Figure 36 above was connected to the input of the demodulator, the input of the Double Quadrature Mixer. All measurements were performed using a RBW and video bandwidth (VBW) of 30 kHz, which created a noise floor of -80 dBm. The simulated IF spectrum in Chapter 4 was based on that in Figure 41. This RF input downconverted by the D-TA 9590 was a clean 5 GHz, -20 dBm, unmodulated signal. It was generated with the *Agilent* E8257D, using the "Continuous Wave" mode. Unmodulated signals were used in the simulation, and were not chosen here for comparison. Notice that the input IF spectrum was spurious as it had two DDS-based synthesizers used for downconversion. The largest spur of interest was 83 MHz offset from the carrier of 1.21 GHz at an SFDR of -45.44 dBc. Here,

“SpurKiller” had already been applied using a phase for maximum cancellation (as discussed in Chapter 3). The desired benchmark of -80 dBc was difficult to achieve as only an increase of 30 dB in the ideal case was simulated. However, this spur at 83.3 MHz offset was reduced using the Double Quadrature Mixer to see an improvement in SFDR. But in order to achieve adequate reduction, both the demodulator PLL and Double Quad LO had to be optimized.

Figure 41- Spurious Spectrum, Output of D-TA 9590

5.2: Demodulator Optimization

The demodulator used (*Analog Devices ADRF6820*) has an internal PLL that demodulates the 1.2 GHz carrier in Figure 41. Even though the RF input signal is unmodulated, the demodulator creates I and Q channels that are 90° offset from each other. Depending on the PLL frequency, the step size of the loop, the reference frequency, and its divider, the PLL itself creates a large number of spurs as in Figure 42 below. These spurs are due to the non-linear nature of the phase detector and the VCO. These settings are controlled via software as in Figure 43 below:

Figure 42 - Spurs Added from Demodulator PLL

Figure 43 - Demodulator PLL Controller Software

First, a high-side demodulator LO was designed at a frequency of 2.4 GHz with a reference of 2 GHz, such that the downconverted demodulated IF spectrum remained at 1.2 GHz. Both were found to be sufficient for reducing the number of spurs from the PLL. Notice that the spectrum was downconverted by 200 MHz from the original 1.2 GHz IF input, as the centre is at 1 GHz. In theory, this should have not occurred, but the PLL was found to have poor accuracy. This demodulator with internal PLL offers an external LO option, which was also tested using signal generators. However, the signal generators used were not optimal as the demodulator requires a differential external LO, which was not available. Also signal generators are not practical for military deployment due to their size. Therefore, the internal PLL was chosen for demodulation based on form factor, and ease of use. Lastly, to help minimize noise, and intermodulation,

a BPF of 980-1150 MHz on both I and Q channels was added after demodulation. A step size of 15 kHz, with a reference divider (REF DIV of 8) was designed to reach lock as suggested by the data sheet. Again, it was found to minimize the number of spurs, and after optimization, the demodulator produced a spectrum with minimal phase noise as shown in Figure 44 below.

5.3: Double Quad LO Optimization

The strong sources of spurs on the IF path of the Double Quadrature Mixer were generated by the DDSs and the demodulator. Similarly, the LO path of the Double Quad was found to generate spurs as well. The LO in the Double Quad was chosen to be 140 MHz instead of 268 MHz (as discussed above). This not only narrowed the BW of the Double Quad, but also had a negative effect on the SFDR. The signal generator used to synthesize this frequency had large harmonics within a 500 MHz BW that mixed with the existing spurs in the IF and LO channels. This was due to the fact the second harmonic of the LO was at 280 MHz. Also the phase shifters had strong harmonics. A lowpass filter couldn't be used as the phase shifters change the amplitudes of the harmonics to phase shift the LO. Unfortunately, as the mixers have very poor LO isolation, additional spurs were added on the output of the Double Quad. The injected spur (1.092 GHz) from the LO path can be seen in Figure 44 below. The optimal LO design of 140 MHz, +10 dBm was then found to produce minimal spurs, as the phase shifter attenuated the higher frequency spurs generated by the LO. After detailed optimization, the final optimized result is discussed in section 5.4 below.

Figure 44 - LO Injection on Output of Double Quad

5.4: Final Results

After optimization, in final testing, the last mixing stage was omitted in the Double Quad, as this upconversion added a second set of spurs from its LO chain. Only the Q channel was plotted in Figure 45 below for simplicity, as the I channel performed identically. As such, the output carrier frequency was measured to be 1.147 GHz, with a high-side spur at 83 MHz offset matching that discussed in RF downconversion, and a BW of 282 MHz. Note that the grid spacing is 10 MHz. The blue plot in Figure 45 below was measured when both Phase Shifters (A and B) were set to 0°, where no spur reduction was achieved. Notice that with no reduction, the SFDR became -20.8 dBc, a worsening of the original SFDR by 24.7 dB due to the added LO injection and PLL phase noise of the block components discussed previously.

Figure 45 - Double Quad SFDR Improvement Comparison

However, the red plot was measured when maximum reduction was achieved. Overall, a maximum of 10 dB improvement in SFDR was achieved ($A = 0^\circ$, $B = 190^\circ$) due to the reduction of a non-harmonic input spur at 83 MHz offset. This high-side spur was reduced by 20 dB resulting in the low-side, LO generated spur dictating the new SFDR of -30 dBc. The determined $B = 190^\circ$ (A and B not in quadrature) disproves the hypothesis in Chapter 4 that only within a range of ± 70 - 110° spur offset, could SFDR be improved be greater than 10 dB. This signifies that Phase Shifter B did not directly track the phase offset of the spur. This was due to the S-parameters of the mixers, shifters, and other components. The S-parameter phase of each device was causing maximum destructive interference to occur outside the ± 70 - 110° range [18]. This also interacts in combination with the phase of the LO-IF leakage. Unfortunately, S-parameter phase data is not provided in many of the component data sheets. The use of a VNA (Vector Network Analyzer), and reverse engineering of each component could help better predict the Phase Shift B variation. Note also that the carrier is amplified in maximum spur reduction, and not degraded by additional spurs within a typical OFDM BW of 10 MHz, for example. Lastly, even though the Double Quadrature Mixer was able to reduce the spurs originating from the DDS, it also added spurs generated from LO injection and PLL phase noise within the demodulator. Additionally, it was later discovered, that the PLL was not locked based on this optimization, which caused further noise. The external reference signal used was not in the required range. These results are discussed further in Chapter 6.

5.5: Phase Variation

Modulating the RF input of the D-TA 9590 was omitted as adding an upconversion stage vastly increases complexity of the spur analysis. In the testing of the prototype, a different phase variation was plotted from that in Chapter 4. Instead of varying the spur phase offset from the carrier to a specific constellation point, Phase Shift B was varied with a DC voltage from 0-12 V. This variation was performed to determine the unknown phase offset of a spur at approximately 37 MHz from the carrier. This difference in spur frequency offset was due to the RF signal being intentionally set to 4 GHz instead of 5 GHz. Also, the demodulator PLL setting was optimized differently from above to minimize its spurs. In Figure 46 below, max cancellation occurs where SFDR improvement is the greatest, approximately 10 dB at Phase Shift B = 70°. This 10 dB is in reference to the -20.8 dBc with no SFDR improvement (where Phase B = 53° instead of 0°). The full phase range was not plotted as the *Mini-Circuits* phase shifter used has a range of 240° approximately. In future work, this Phase Shift B can be adapted real time by adding feedback mechanisms, such as a PLL to track spurs.

Figure 46 - SFDR Improvement vs Phase Shift B on Double Quad Prototype

As a final verification that the reduced spurs were not mixing products of the phase shifter harmonics, the frequency offset between spurs was measured in Figure 47(a) and between phase shifter harmonics (b) on the following page. Notice that in (a) the offset between spurs is 103 MHz, a non-harmonic multiple of 140 MHz, the Double Quad LO frequency used in (b). Also, this 103 MHz offset is not a combination of harmonics from the two D-TA LOs (6 GHz and 3.93 GHz).

Figure 47 (a) (Top) Double Quad SFDR Spur Offset, (b) (Bottom) Phase Shifter Harmonic Offset

Lastly, in Figure 47(b) the harmonics of the phase shifter are multiples offset by 140 MHz which vary in amplitude with varying voltage control. In summary, these harmonics succeed by mixing with existing spurs to reduce them. This effect was unintentional.

5.6: Supplementary Testing

As the D-TA 9590 was later modified by replacing one of the DDS modules with a low noise PLL, the previous test setup could no longer be used. Thus, the Double Quad was subsequently tested with a DDS-based LO as input as previously depicted in Figure 38 in section 5.1. The input IF frequency was chosen to be 2.1 GHz, unmodulated with an SFDR of -20 dBc. After PLL, and LO optimization, an increase of 10 dB in SFDR occurred at a Phase Shift B of 20°, again which was outside of the +/- 70-110° range. Thus, there is no direct relationship between modulation phase and Phase Shift B due to the S-parameter phases of each component.

5.7: Chapter Summary

This chapter describes the implementation of the Double Quadrature Mixer prototype designed with block components. Using the D-TA 9590 as input, the demodulator PLL settings, and LO frequency were optimized to minimize spurs added by the prototype. Overall, an improvement of 10 dB in SFDR was observed, but with variation in the phase at which maximum interference occurred.

Chapter 6: Conclusion

6.1: Summary

The research in this thesis has been focused on improving SFDR of UWB radios through an adaptive system-level approach. The sources of spurs range from digital to analog components, and can be quite unpredictable. This was discussed in Chapter 1. Chapter 2 outlined the noise challenges of UWB and how they relate to classical RF constraints such as phase noise, and LO isolation. Then, the D-TA 9590 UWB receiver and its DDS-based LO's sources of spurs were described. The AD9912 DDS was introduced with its integrated spur reduction system "SpurKiller". This provides a range of 10-20 dB in improved SFDR, but only for harmonic spurs. In Chapter 4, the Double Quadrature Mixer was introduced to reduce harmonic and non-harmonic spurs, so that all sources of spurs can be dealt with on a system level. The system was simulated in MATLAB and then prototyped in Chapter 5 to produce the results discussed below.

6.2: Discussion of Results

The results of the three test cases of the Double Quadrature Mixer are summarized below. The system was tested in simulation and in prototype using the D-TA 9590, and then using a D-TA DDS LO module as input. The design goal of 20 dB in SFDR improvement was met relative to the minimum output SFDR of -20.8 dBc, with an achieved maximum of -30 dBc. "SpurKiller" was also able to

achieve a reduction on average of 10 dB. In theory, the combination of these two improvements would have met the design goal. However, the overall SFDR worsened from -45.5 dBc to -30 dBc. In all cases, there were ranges in phase where constructive interference occurred, as expected. But in all three cases, the ranges where destructive interference occurred were vastly different as below. Lastly, the BW narrowed from 500 MHz to 280 MHz due to the phase shifter BW design. This would halve the UWB data rate as calculated in Section 2.1 to 9 Gbits/sec. The spurs were upconverted and downconverted only outside this bandwidth and then cancelled.

TABLE 2 - RESULTS COMPARISON

<u>Result</u>	<u>Thesis Goal</u>	<u>Simulation</u>	<u>Prototype, 9590 Input</u>	<u>Prototype, DDS Input</u>
Max SFDR Improvement	10-20 dB	29 dB	10 dB	10 dB
SFDR	-80 dBc	-68.72 dBc	-30 dBc	-30 dBc
SFDR Improvement Range	0-20 dB	-10 to +40 dB*	-20 to +10 dB	-20 to +10 dB
Phase Shift B	N/A	90°	190° @ 5 GHz RF 70° @ 4 GHz RF	20° @ 2.1 GHz IF
SFDR Improvement Range, Phase	N/A	+,- [70°,100°]	+ [55°,95°] @ 4 GHz RF	Not Calculated
BW	500 MHz	500 MHz	280 MHz	280 MHz
Maximum Spur Offset	N/A	20 MHz	83 MHz @ 5 GHz RF 37 MHz @ 4 GHz RF	25 MHz @ 2.1 GHz IF

***40 dB due to the larger I and Q channel amplitudes used in simulating the phase sweep**

The overall worsening of 10 dB in SFDR was due to the poor demodulator PLL phase noise, and LO injection, even after optimized minimization. As development continues, LO phase shifters at higher frequencies could be used (to reduce LO harmonics falling in-band), and the noise performance of 90° phase shifters instead of integrated demodulators could be compared. As the overall SFDR still negative, it does not have a significant effect on BER as discussed in Chapter 2, however, spurs even at -60 dBc, can still look like phantom signals. These results are a starting point for the motivation for spur reduction and future work.

Similarly, the variation in Phase Shift B causing maximum SFDR depends on the non-linearities of the system, which also causes the phase offsets between spur and carrier to vary. Also, the simulated phase offset followed a 64 QAM constellation as an example. But in reality, the spur phase offset will be a combination of constellation and spur phase caused by non-linearities. The phase variation between two prototype inputs as above proves these nonlinearities exist. Phase-carrier offset is quite variable, and even a time variation was noticed in some instances. Lastly, there was also the interaction of S-parameter phase of each component, causing the A and B shifters not to be in quadrature. Overall, there was no direct relationship between modulation phase and Phase Shift B. The root of this thesis was not to determine the phase of the spur before reduction, but to determine it by variation in LO phase. The next steps would be to integrate and establish an automatic real-time algorithm based

on these variations, and to determine a real-time phase response using time sampling.

6.3: Thesis Contributions

Major contributions developed with this thesis include:

1. The *Analog Devices* AD9912 DDS was analyzed using its “SpurKiller”.
This method proved useful for approximating the spur-carrier phase offset. It was proven that even between ICs with the same batch number, significant variation in spur phase occurred.
2. The reduction achieved with “SpurKiller” was only found to affect harmonic spurs.
3. The Double Quadrature Mixer was conceived to meet the specifications for UWB and simulated to demonstrate an improvement in SFDR of over 29 dB based on the reduction of a non-harmonic spur.
4. In simulation, it was also demonstrated that if the spur-carrier phase offset was within the range of $\pm 70^\circ$ - 100° , that an SFDR improvement would occur. This was observed at fixed spur-carrier offset frequency.
5. In prototype, an increase of 10 dB in SFDR occurred, despite significant noise degradation. However, the Phase Shifts A and B, often not in quadrature, for maximum SFDR improvement, were found not to be related to the ideal phase range in (4) above.

6.4: Future Work

As discussed in Chapter 1, *MIT Lincoln Labs* has produced ground-breaking results at the IC level with increasing the SFDR of ADCs. They have produced an IC using the process in Figure 48 below, and is quite complex. It is also not commercially available and is unreliable [30].

Figure 48 - MIT *Lincoln Labs* Nonlinear Digital Equalizer IC Design [5]

In future work, the goal would be to take some of this research and apply its principles to the Double Quad and use a simpler SOC integration approach.

Figure 49 - MIT *Lincoln Labs* Nonlinear Digital Equalizer IC (yellow block) [31]

But unlike the Double Quadrature Mixer prototype from this thesis, a small IC (as in the NLEQ in Figure 49 above) would need to be developed for cellphones and a relatively small PCB for short-range 5G base stations. Also, in military applications, this would be useful for urban mobile radios. In either situation, mitigating the unpredictability of spurs would be of tremendous commercial interest.

The overall concepts that need to be improved for success in integration and commercialization are summarized as follows:

- Modulation: The effect of signal modulation (ex. 16QAM, 64QAM) on spur phase variation should be explored, varying frequency across a 500 MHz band as well. The complexity of constellations need to be studied, so that spur cancellation can be adapted to unique situations. Phase shifters with high modulation bandwidths and higher phase ranges should be used, for example *Hittite's* phase shifter shown in Figure 50 below.

Figure 50 - Hittite HMC934LP5E (1-2 GHz, 400°) Phase Shifter [32]

- LO Injection and Phase Shifter Isolation: The mixers and phase shifters added spurs to the final output of the system. High wideband SFDRs would require mixers with extremely low LO injection. The phase shifters were known to be quite spurious as well. Reducing these two injections through further investigation is key to high dynamic range for commercialization. The

demodulator PLL had phase noise and random non-linearities. Simple phase shifters, or external PLLs could prove to reduce added spurs to the system.

- Adaptive Algorithms: Wireless spectrum is always dynamic, and as high spur phase variation was observed, reduction would have to be adapted to maintain high SFDR. An algorithm, such as a Dithered Linear Search to predict this variation, and the technology to implement it should be studied [10].
- Combining Double Quadrature and Nonlinear Digital Equalizer: *MIT Lincoln Labs* has developed a Nonlinear Digital Equalizer that greatly reduces spurs added from ADCs [4]. However, its IC design is also extremely complex and costly. A blend of technology between previous work and this thesis is proposed for future research.
- System-on-Chip (SOC) Integration. To make the form-factor more practical for military and cell applications [5], SOC integration must be explored. IP technology will be utilized to simplify transistor level design, and maintain the system-level nature of this research

Appendix A - MATLAB Simulation: Block Functions

FFT:

```
function [ freq, pwr ] = fft_pwr( tstep, voltage, R )
%   This fuction is going to take in voltage array and give
%   a
%   scalled fft. The voltage elements must be equally
%   spaced in time.
%   The tstep input is the time spacing of the voltage
%   points.
%   It is a single real number. The input R specifies the
%   resistance the
%   power is to be calculated for. The default value is
%   50ohms if this
%   input is ommited.
%   The output will be an array of frequency in MHz and one
%   of power in dBm.

clearvars freqP freqN freq pwr z x y w j;

%Determine the frequency step knowing the total time of the
simulation.
freqstep = 1/tstep/length(voltage);

% The reference impedance is assumed to be 50ohms if it
isn't specified.
if nargin < 3
    R = 50;
end

%if even.

if (length(voltage)) == (2*round(length(voltage)/2))

    freqP = 0:freqstep:freqstep*(length(voltage)/2-1);
    freqN = -freqstep*(length(voltage)/2):freqstep:-
freqstep;
    freq = [freqN freqP];

%if odd.
else
```

```

        freqN = -freqstep*(length(voltage)/2):freqstep:-freqstep;
        freq = [freqN freqP];

    %if odd.
else
    freqP = 0:freqstep:freqstep*(length(voltage)/2-1);
    freqN = -freqstep*round(length(voltage)/2):freqstep:-
freqstep;
    freq = [freqN freqP];

end

    %Scale to MHz.

freq = freq ./1e6;

% Compute the fft.
z = abs(fft(voltage));

%Scale the fft to give the peak amplitude of the waveform.
z = z/length(z);
z = z * 2;
w = fftshift(z);

%Now convert the voltage into dBm.
pwr = 10*log10(w.^2/(2*R))+30;

```

Local Oscillator:

```
function[vlo]= LO_Imp_I(CarrierdBm, CarrierFreq,
NoiseFloorIn, NoiseFloorOut, CornerFreq, SpurOffset,
SpurdBc, time, tstep, phase_deg)

phase = phase_deg*pi/180; % covert phase_deg to radians

% let the input carrier amplitude be in dbm

% calculate the CarrierAmplitude in voltage
CarrierAmplitude = sqrt(2*10^(CarrierdBm/10)*1e-3*50);

NoiseFloorIndBm = NoiseFloorIn;
NoiseFloorOutdBm = NoiseFloorOut;

vlo = zeros(1, length(time));

vnoisein = wgn (1, length(time), NoiseFloorIndBm +
10*log10(1/(2*tstep)), 1, 'dBW');
vnoiseout = wgn (1, length(time), NoiseFloorOutdBm +
10*log10(1/(2*tstep)), 1, 'dBW');

fil = tf(2*pi*CornerFreq, [1 2*pi*CornerFreq]); % cut_off
should be 1 MHz
vfil = (lsim(fil,vnoisein,time))';

SpurLinear = 2*10^(SpurdBc/20); % multiply by 2 to becuse
the power is split to each side of the carrier
spur = SpurLinear*sin(2*pi*SpurOffset*time);

vnoise = vfil + vnoiseout + spur;

for i = 1:length(time)
vlo(i) = CarrierAmplitude*cos(2*pi*CarrierFreq.*time(i) +
vnoise(i) + phase); %Mathematically, the noisefloor is
correct in dBc/Hz
end
end
```


Amplifier:

```
function [vout]= amplifier_simon(vin, GaindB,IIP3dB,  
IIP2dB, NF, tstep)  
  
R = 50;  
NoiseFloor = -174;  
F = 10^(NF/10);  
Gain = 10^(GaindB/20);  
  
% From this equation  $F = 1 + (N_{added}/N_{source})$   
Nsource = wgn (1, length(vin), NoiseFloor + 10*log10(1/  
(2*tstep)), R, 'dBm');  
Nadded = Nsource*sqrt(F - 1);  
  
%Power Series Coefficients  
k1 = Gain;  
VIP3 = sqrt(10^(IIP3dB/10)*1E-3*50)*sqrt(2);  
k3 = -(4*k1)/(3*VIP3)^2;  
VIP2 = sqrt(10^(IIP2dB/10)*1E-3*50)*sqrt(2);  
k2 = k1/VIP2;  
  
% add noise to the input signal  
vin = vin + Nadded;  
  
% create the output signal which has gain, linearity and  
noise  
vout = k1*vin + k2*vin.^2 + k3*vin.^3;  
  
end
```

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