Power Supply Induced Jitter Including the Ground Bounce and Transmission Media Effects

by

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Abstract

In this thesis, an efficient method for estimation of power supply induced jitter (PSIJ) in high-speed designs is presented. EMPSIJ [34] method is advanced to handle the combined effects of both the transmission media and ground bounce in the presence of supply noise. Semi-analytical relations are developed based on small-signal noise analysis for quick estimation of PSIJ and one bit simulation of the large signal model. For this purpose, small-signal configuration of a voltage-mode driver circuit is considered to evaluate the differential output response. Also, an alternative and systematic approach is proposed based on MNA tridiagonal formulation and Thomas Algorithm for PSIJ analysis. It avoids re-derivation of the expressions in the case of any change in load conditions.

Also, a novel closed-form model for transmission line type interconnects is developed relating the input and the output nodes of the transmission line which enables efficient PSIJ analysis in the presence of PCB traces. The proposed closed-form expression for transmission line type interconnects is also advanced to include the effect of load.

Several validating examples are presented for the proposed approaches using different types of noise sources. The results are compared with HSPICE simulator to validate the accuracy and efficiency.

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List of Abbreviations

AWE	Asymptotic Waveform Evaluation
CFH	Complex Frequency Hopping
CPU	Central Processing Unit
Decaps	Decoupling capacitors
DJ	Deterministic Jitter
ESL	Equivalent Series Inductance
EMPSIJ	Efficient Modelling of Power Supply Induced Jitter
ESR	Equivalent Series Resistance
IC	Integrated Circuit
IFFT	Inverse Fast Fourier Transform
IR drop	current (I) passing through resistance (R) (Resistive voltage drop)
KCL	Kirchhoff's Current Law
LFSR	Linear-Feedback Shift Register
MCM	Multi-Chip Module
MNA	Modified Nodal Analysis
MOR	Model Order Reduction
PRBS	Pseudo-Random Binary Sequence Macromodelling Algorithm
PRIMA	Passive Reduced-order
PCB	Printed Circuit Board
PDN	Power Distribution Networks
PSIJ	Power Supply Induced Jitter
p.u.l	Per Unit Length
RJ	Random Jitter
SMC	Surface Mounted Capacitance
TIE	Time Interval Error (Jitter)
TL	Transmission Line
VDM	Voltage Mode Driver
VRM	Voltage Regulator Module

List of Symbols

α	Slope of the rising/falling edge of the output response
β, γ	Small signal parameters related to Thévenin equivalent impedance
$\tilde{\beta}, \tilde{\gamma}$	Small signal parameters including ground bounce
λ	Small signal parameter associated to differential output response of a voltage mode driver circuit
$\tilde{\lambda}$	Small signal parameter including ground bounce
ϵ_r	Relative permittivity of PCB trace
Γ	Accumulated jitter percentage
σ	Number of lumped- π segments used to represent a transmission line (TL)
$\frac{\partial}{\partial t}, \frac{\partial}{\partial x}$	Partial derivative w.r.t time, position
τ	Delay in transmission line
a_i, b_i, c_i	Coefficients of tridiagonal coefficient matrix (T)
f_i	Coefficients of the unknown vector of the tridiagonal system
b	Source vector of tridiagonal system
b1, b2	Source vectors related to supply noise and ground bounce noise, respectively
C	Per unit length capacitance of a transmission line
C_σ	Coefficient associated with σ^{th} segment of a transmission line
C_{decap}	Overall lumped capacitance for decoupling effect
g_m	Transconductance of a n-channel transistor
G	Per unit length conductance of a transmission line
i_{sc}	Short circuit current between nodes of TL1 and TL2
$\tilde{i}_{sc}$	Short circuit current including ground bounce
$i(x, t)$	Current associated with distributed transmission line
$I(f)$	Current profile for a power distributed network
$J(f)$	Jitter spectrum
J_r^k	Peak-to-peak jitter over a ‘ k ’ number of bits
L	Per unit length inductance of a transmission line
R	Per unit length resistance of a transmission line
$R_{on-chip}$	Lumped resistance for on-chip power grid

R_{sh}	On-chip shunt resistance
R_L	External load resistance
$S(f)$	Jitter sensitivity for transistor level circuits
t_r	Rising time for propagating signals
$\mathbf{T}$	Coefficient matrix of a tridiagonal system
$\mathbf{v}$	Vector associated with differential output node voltages of tridiagonal system
v_g	Ground bounce noise
v_{1a}, v_{1b}	Voltages at the 1 st segment of TL1 and TL2
v_{2a}, v_{2b}	Voltages at the 2 nd segment of TL1 and TL2
$v'_{\sigma-1}, v''_{\sigma-1}$	' $\sigma - 1$ ' node voltages of TL1 and TL2
v_n	Power supply noise
v_{th}	Thévenin equivalent voltage between nodes of TL1 and TL2
$\tilde{v}_{th}$	Thévenin equivalent voltage including ground bounce
v_{Rn}	Output voltage including the noise contribution
$v(x, t)$	Voltage of distributed transmission line
$V(f)$	Supply noise spectrum
$V_{n_{m_i}}$	Amplitude of small-signal noise response for i^{th} frequency component
V_{sup}	Relatively constant supply voltage for the H-bridge circuit
V_{ref}	Reference voltage at negative terminal of an op-amp
$V(s)$	Voltage of TL in Laplace domain
z_1, z_2	Transmission line p.u.l impedances
$Z_1 \dots Z_6$	Equivalent impedances associated with small signal circuit of a voltage mode driver circuit
Z_{PDN}	PDN impedance profile
Z_{th}	Thévenin equivalent impedance of the small signal circuit of a voltage mode driver circuit
$\tilde{Z}_{th}$	Thévenin equivalent impedance including ground bounce

Chapter 1

Introduction

Over the years, rapid innovations in the semiconductor industry and device scaling has enabled integration of large number of transistors on a single chip [1], [2]. The scaling of CMOS transistors has helped to maintain relatively constant power per unit area [3] while allowing more for transistors to be packed in the same chip-area. Not only making the devices smaller, the continuous scaling of integrated circuit technology has also made them faster.

In order to produce and maintain integrity of signals in modern high-speed high-density ICs, the interconnect design becomes very challenging due to various parasitic effects. The effects such as signal delay, ringing, attenuation and crosstalk can degrade the signals [4]-[7] at high frequencies. These interconnects are present at various levels of design hierarchy, such as on-chip, packaging structures, MCMs, PCBs, backplanes and cables [3]. The overall circuit behaviour is significantly influenced by the on-chip and off-chip interconnect structures.

Depending on the desired accuracy, the interconnects present in a power distribution network can be represented as lumped models or distributed models. In case of using conventional approach [8] of lumped modelling, interconnect is divided into large number of segments which can lead to large circuit size causing the simulation to become CPU inefficient. With operating frequencies in the GHz regime, interconnects behave as a transmission line because the length of an interconnect can become a significant fraction of the operating wavelength.

The frequency-domain simulation of transmission line interconnects is conventionally done by formulating and solving modified nodal analysis (MNA) matrices [9]. At each frequency point, LU decomposition of the MNA matrix and forward-backward substitution are needed to obtain the solution. Transmission lines carrying signals with higher operating speeds and sharper rise edges require more segments and consequently, simulation becomes highly inefficient.

There are several techniques that address both the mixed frequency-time problem and large circuit sizes which arise due to high-speed interconnects. With the help of model-order reduction (MOR) approach, a large distributed network can be represented with fewer equations or lower-order systems. Several MOR techniques such as asymptotic waveform evaluation (AWE) [10], complex frequency hopping (CFH) [11], Padé approximation [12], Arnoldi algorithm [13] and PRIMA [14] have proven to be efficient in reducing the order of large linear interconnect networks. The time-domain circuit reduction techniques that reduce circuits including linear as well as nonlinear terminations have been proposed in [15]. In addition to MOR techniques, the development of efficient macro-models for transmission lines [16], [17] have also been the topic of intense research.

Additionally, in the modern designs, while the higher speeds are becoming important, lower power consumption is also emerging as a key requirement. Designing of power distribution networks (PDNs) has become increasingly challenging for high-speed and high-density circuits. Over the time, the power dissipation in modern designs has increased from few Watts to 100 Watts while the supply voltage has reduced from 5V to around 1V. This reduction in supply voltage leaves little room for supply voltage variations and has resulted in reduced noise margins. Several systematic methodologies [18]-[20] for the analysis and design of power distribution networks have been developed to ensure the power integrity and performance of the system. Low-power consumption technologies operating at higher frequencies typically require reduced noise margins and pose significant power integrity challenges [21]-[23].

Ensuring power integrity requires a stable PDN that minimizes the power noise. It is to be noted that both, off-chip and on-chip PDN components contribute to power supply

noise [18]. This is because even though the process technologies continue to improve the off-chip package design methods remain relatively unchanged. Due to inductive nature of the off-chip components, current cannot change fast enough between off chip and on-chip components, which results in high-frequency switching noise [19]. On the other hand, the on-chip IR drop [18], [24] critically impacts circuit operations at high frequencies and is a major contributor to the power supply noise.

Timing variation in the digital signal (often referred to as jitter [25]) that are caused by the power supply noise is known as power supply induced jitter (PSIJ). Sensitivity of a circuit due to the supply noise is a major contributor to the power supply induced jitter [26]. These two factors are largely decoupled and can be characterised independently. The noise on the power rail is influenced by both the PDN impedance and the supply current drawn by the on-chip circuits. The jitter sensitivity depends on the ratio of stabilised jitter response to noise amplitude at a single-tone frequency [25].

In literature, power supply induced jitter (PSIJ) has been extensively addressed. Impact of supply noise in high-speed interface was discussed in [26]. In [27], transfer of noise through power distribution network from transmitter to receiver was investigated. Equalization techniques based on jitter sensitivity and jitter reduction via architectural level changes were addressed in [28]. The effect of a silicon interposer channel and paths of noise via different transfer functions can be found in [29]. [30] presents a method for jitter estimation based on experimental design techniques and [31] addresses RC delay based technique to estimate PSIJ sensitivity of a CMOS buffer chain.

Conventional approach for jitter analysis requires thousands of SPICE based circuit simulations for a reasonable jitter estimation. In such simulations, input data pattern are represented as a pseudo-random binary sequence (PRBS). It is a binary sequence generated with a deterministic algorithm using linear feedback shift registers (LFSR) [32]. Simulation based on PRBS can take excessive CPU time depending on the number of bits used. For example, PRBS-31 has a sequence of length 2^{31} bits. At the bit rate of 100 Mbps, simulating even one sequence can take approximately 1.5 hours. For reasonable jitter estimation, multiple repetitions of PRBS-31 are needed to be simulated [33] which

can make the process prohibitively CPU expensive.

Further advancing the field, in [34], an efficient modelling of power supply induced jitter (EMPSIJ) was introduced. Analysis in this method considered voltage-mode driver circuits and was based on separating the large signal response and small signal noise output. It uses just one bit full simulation (unlike the conventional methods that require simulation of hundreds of bits) and consequently leads to significant speed-up. The method was also extended to current-mode driver based circuits [35] as well as differential traces with ground bounce in [36]-[38].

1.1 Contributions

The goal of this thesis is to efficiently estimate the power supply induced jitter (PSIJ) in the presence of power supply noise as well as ground bounce and transmission media effects. Using EMPSIJ method, the combined effects of both transmission media and ground bounce are analysed. The main contributions of this thesis are as follows:

1. A closed-form expression for the transmission media is derived using lossy lumped π -model of the transmission line [38]. Finite numbers of sections (σ) are considered while modelling the transmission line with R, L, G and C parameters. Based on nodal analysis, a recursive relation for obtaining transfer function with σ -sections of transmission line is developed. The validity of the relations are tested by implementing in MATLAB for various lumped- π sections and results are compared with HSPICE [39].
2. The relations developed in contributions (1) are combined with a voltage mode driver (VMD) circuit [38], which is widely used in low voltage differential signaling [40], for PSIJ analysis. Using small signal model of the driver, expressions for the differential output noise response across the load is derived. Subsequently, the analytical jitter expressions in the presence of both the supply noise and ground bounce are developed.
3. Proposed method in contribution (2) is generalized to overcome the need of deriving analytical expressions for different number of segments and load settings every

time (which otherwise is a computationally tedious task [38]). A systematic and recursive approach based on Thomas Algorithm [41], [42] is developed to obtain the differential noise response.

4. Practical examples with different types of waveforms for supply noise and ground bounce are presented along with their impacts on power supply induced jitter.

1.2 Thesis Organization

Rest of the thesis is organized as follows:

Chapter 2: In this chapter, power distributed network (PDN), power supply induced jitter (PSIJ) and EMPSIJ methods are briefly described. In addition, voltage mode driver (VMD) and transmission line type interconnects are also reviewed.

Chapter 3: Chapter 3 presents development of closed-form expression for transmission lines based on lossy lump π -model. It also presents the validating numerical examples.

Chapter 4: Semi-analytical repressions for PSIJ are developed relating the supply noise and transmission media. Also, semi-analytical expressions for PSIJ are developed including supply noise, ground bounce noise in the presence of transmission media followed by the practical case studies.

Chapter 5: In this chapter, an alternative and systematic method is proposed to estimate the power supply induced jitter (PSIJ) including the effects of transmission media, supply noise and ground bounce. The proposed approach is based on Thomas Algorithm and EMPSIJ method.

Chapter 6: Chapter 6 presents conclusions and proposed future research.

Chapter 2

Overview of Power Distribution Networks and Power Supply Induced Jitter

Modern high-speed and high-density systems require quality power supply modules in order to power billions of devices contained in them. Due to numerous factors such as temperature, large current and corresponding power dissipation, as well as electromagnetic interference, the quality and performance of these electronic systems can be greatly affected. Hence designing to ensure power integrity becomes critical in modern electrical products.

This chapter reviews some of the relevant literature associated with the power integrity. The chapter is organized as follows:

- Sections 2.1 and 2.2 present an overview of power distribution networks (PDNs) and power supply noise, respectively.
- In Section 2.3, the description of voltage-mode driver circuit is presented.
- Section 2.4 describes the modelling of transmission line type interconnects.
- A brief review of jitter and PSIJ is presented in Section 2.5.

2.1 Power Distribution Network

The primary goal of a power distribution network is to deliver stable power supply to on-chip grids with maximum efficiency and minimal noise [1]. The physical power distribution network consists of several levels of hierarchy: the voltage regulator module (VRM), printed circuit board (PCB), decoupling capacitors, the package and power distribution on silicon chip as illustrated in Figure 2.1.

Figure 2.1: Illustration of power distribution network (PDN)

Voltage regulator module (VRM) is a DC-DC converter [38] that converts an input DC voltage to a specified supply voltage as required by the IC chip. *Printed circuit board (PCB)* mechanically supports various components in the system. It also provides an electrical path between the VRM and the package via power and ground planes. *IC package* is connected to the PCB by an array of contacts (e.g., ball grid array or pin grid array). Power planes are connected to the chip PDN using either a flip-chip or bond-wire technology. *Decoupling capacitors (decaps)* are placed on-board, on-package and on-chip in order to reduce the overall impedance. Each stage determines the impedance characteristics of the PDN for a given range of frequencies.

A lumped circuit representation of a typical PDN is shown in Figure 2.2 [4]. It corresponds to modelling and extraction of three distinct stages: off-chip, on-chip and supply current profiles. Off-chip PDN components such as VRM, PCB and package are modelled with lumped resistances (R_{vrn} , R_{pcb} and R_{pkg}) and inductances (L_{vrn} , L_{pcb} and L_{pkg}), respectively. The decoupling capacitors (decaps) are associated with the parasitic equivalent series resistance (ESR) and equivalent series inductance (ESL) due to the finite conductivity and magnetic field, respectively. Decaps placed on the PCB ($C_{pcb-decap}$) and

package ($C_{pkg-decap}$) are usually designed at low and medium frequencies depending on the operating range.

Figure 2.2: Simplified equivalent circuit model for a typical PDN

On-chip power grids are simplified and lumped into $R_{on-chip}$, which can be estimated using resistive voltage drop (IR drop) at nominal DC power supply current. C_{decap} represents the overall capacitive decoupling effect. It includes intentional decaps as well as parasitic and interconnect capacitance. The loss associated with C_{decap} is represented by R_{decap} . The shunt resistance (R_{sh}) and feedback current (I_f) are given as:

$$R_{sh} = \frac{V_{DC}}{\alpha I_{DC}}; \quad I_f = \alpha I_{DC} \quad (2.1)$$

where α is an empirical factor [4] representing how much current should be scaled from ideal DC current (I_{DC}) in order to model the effective decrease in the total current. In Figure 2.2, the lumped models are used to represent a typical power distribution network. Usually, lumped models are used in pre-layout noise analysis to obtain an estimation of the early stage noise. In post-layout noise verification, for higher accuracy, distributed models for on-chip PDN and current profiles are desired.

2.2 PDN Supply Noise

The design of power distribution networks (PDNs) has become increasingly challenging because of higher load currents while the supply voltage has scaled down; leaving little room for noise margins. Power supply variations occur due to factors such as power

delivery paths and interference from the other systems. The contribution to noise from each design hierarchy (VRM, PCB, package and silicon chip) must be controlled in order to meet the supply noise targets. Nature of the noise associated with each of these modules is briefly described below.

2.2.1 Voltage Regulator

The voltage regulator module (VRM) and bulk decoupling capacitors may produce DC offset and supply noise which is dominant at lower frequencies (below 10 kHz). Since the VRM loop has limited bandwidth, any change in the load can produce additional AC noise. Also, switching regulator can create distortion due to their switching characteristics. These noise contributions need to be controlled through a proper VRM regulator loop and PCB decoupling [19], [20].

2.2.2 Printed Circuit Board (PCB) and Package

Printed circuit board and package may also introduce DC offset due to resistive voltage loss (IR drop). It is often compensated using a feedback sense line, running from the component to VRM. PCB (and capacitors placed on it) contributes to the supply noise mainly in the frequency range of 1 kHz to 10 MHz. In power supply design methodology, the major focus is the number, type and placement of these PCB decoupling capacitors on the board.

Typically the package affects supply noise in the frequency range of 1 MHz to 250 MHz. The supply is critical in this frequency range due to the issue of package/chip resonance. Inductances of package and PCB combined with on-chip capacitance create package/chip resonance (LC resonance) and can generate excessive supply noise. Since package and PCB are the dominant contributors to the PSIJ at medium frequency range (near package resonance), several methodologies [21]-[23] have been proposed for their accurate modelling. A plane model, the equivalent series inductance (ESL) of the surface mount capacitance (SMC) and the on-chip decap area are required in analysing the overall PCB and package PDN impact on power supply noise.

2.2.3 On-chip Power Distribution Network

On-chip power distribution network contributes to supply noise with further DC offsets. The DC offset in this case occurs due to on-chip wires (thin on-chip metal layers) that are highly resistive and can cause high resistive voltage loss. The on-chip IR drop is location dependent. Some circuits close to supply pads might see low loss whereas circuits far away from pads may experience higher drops. This DC offset is difficult to compensate using a feedback sense line to the VRM. The IR drop is dependent on bump/pad placement, power routing on the chip and current distribution over the chip area. Therefore, the on-chip DC IR drop must be analysed at early (pre-layout) stages to avoid the late changes in the bump or pin assignments.

The on-chip switching activity also generates high frequency (typically more than 100 MHz) supply noise. The inductive nature of the package pins tend to provide higher impedance for fast switching currents thereby hindering high frequency switching activity. High-frequency supply noise is controlled using on-chip capacitors for which sufficient decap area must be budgeted and allocated. Next, important circuit configurations that are often used in PDNs are reviewed.

2.3 Voltage Mode Driver (VMD)

Voltage mode driver (VMD) circuit is widely used as a low voltage differential signalling transmitter in high-speed serial links [34], [39]. In differential signalling applications, it is used to achieve a very good power supply rejection ratio. VMD consists of a voltage regulator and a H-bridge driver as shown in Figure 2.3 .

Voltage regulator consists of an op-amp and a n-channel transistor (M_0) with a negative feedback loop (Figure 2.3). Voltage regulator helps to eliminate power supply noise (v_n) induced variations so that there is a constant voltage (V_{sup}) at the output of the regulator. The supply voltage at power rail is V_{DD} and op-amp is powered by V_{DD1} . Usually, V_{DD1} is greater than V_{DD} to maintain M_0 in saturation. If noise infiltrates the system, the current through (M_0) that charge the capacitor (C_3) varies and correspondingly V_{sup} varies. Consequently, the gate voltage of the transistor M_0 follows the variations in V_{sup} .

Since gate voltage is controlled by the negative feedback loop, accordingly transistor and capacitor currents vary. As a result, the V_{sup} starts to adjust to its nominal reference value.

Figure 2.3: Voltage mode drive (VDM) [34]

In Figure 2.3, transistors $M1$, $M2$, $M3$ and $M4$ make a H-bridge driver with an external load resistor (R_L) which is connected between two transmission lines (TL1/TL2). Voltage regulator generates a constant supply voltage (V_{sup}) at the drains of $M1$ and $M2$. For the 400mV regulated voltage generated at the source of M_0 , the output differential voltage across the terminals DP/DN is ± 200 mV. However, this can be associated with significant delay and ringing due to transmission lines.

In the proposed work, small-signal analysis is used to model the impact of PDN noise. The equivalent small-signal model (for the case of $M2$ in saturation) is shown in Figure 2.4.

When M_2 is in saturation region, the p-channel transistor of the inverter operates in linear region which can be modelled by drain-to-source capacitor (C_{dsp}) and ON-resistance (R_{onp}). In this case, since transistor $M3$ also operates in linear region, ON-resistance (R_{on3}) and drain-to-source capacitor (C_{ds3}) are also added to the small-signal model. Gate-to-drain capacitors of $M2$ and $M3$ are represented by C_{gd2} and C_{gd3} , respectively. Similarly for transistors $M2$ and $M3$, drain-to-source capacitors (C_{ds2} , C_{ds3}) and gate-to-source capacitors (C_{gs2} , C_{gs3}) are added to the small signal model, respectively. gm_2 represents the transconductance and r_{o2} is the intrinsic output resistance of the n-channel transistor ($M2$) while in saturation mode.

Figure 2.4: Small signal schematic of VMD with $M2$ in saturation region

To estimate the power supply induced jitter in the presence of supply noise (v_n), node voltages v_x and v_y order in to obtain small-signal differential voltage (v_{r_n}) across the external resistor (R_L) (*i.e.*, $v_{r_n} = v_y - v_x$).

Transmission lines are modelled using RLGC lumped parameters between nodes v_q and v_e . The method in [34], enables analytical evaluation of the equivalent circuit of Figure 2.4, instead of simulating the entire voltage-mode divider circuit in a conventional simulator for every bit and provides significant speed-up. Since the model used for the transmission media critically impacts the estimated jitter, a brief review of the transmission line modelling is provided below.

2.4 Modelling of Transmission Line

Modelling of interconnect in the VDM of Figure 2.3 becomes a major bottleneck at higher frequencies. Often a transmission line model is required to accurately represent its electrical behaviour of the interconnect. Such interconnects are characterized by distributed R , L , G and C per unit length (p.u.l.) parameters.

2.4.1 Telegraphic's Equation and TL Models

Consider the transmission line structure as shown in Figure 2.5 . The voltages and

Figure 2.5: Transmission line representation of an interconnect

currents along the transmission line are described by partial differential equations known as Telegrapher's equations [6] which are the functions of time (t) and position (x).

$$\frac{\partial}{\partial x} v(x, t) = -R i(x, t) - L \frac{\partial}{\partial t} i(x, t) \quad (2.2)$$

$$\frac{\partial}{\partial x} i(x, t) = -G v(x, t) - C \frac{\partial}{\partial t} v(x, t) \quad (2.3)$$

where R , L , G and C are per unit length parameters. The Laplace transformation of above equations can be written as:

$$\frac{\partial}{\partial x} V(x, s) = -Z I(x, s) \quad (2.4)$$

$$\frac{\partial}{\partial x} I(x, s) = -Y V(x, s) \quad (2.5)$$

where Z and Y are the transmission line p.u.l impedance and admittance parameters, defined as:

$$Z = R + sL \quad ; \quad Y = G + sC \quad (2.6)$$

where s is a Laplace operator ($s = j\omega$).

2.4.2 Conventional Lumped Segmentation

At low frequencies, a transmission line can be approximated via lump segmentation model, which can be easily simulated in a SPICE based conventional simulator. Figure 2.6 shows the discretization of a transmission line using lumped segmentation model. In this conventional approach, partial differential equations (2.2) and (2.3) can be rewritten as difference equations:

$$v_{k+1}(t) - v_k(t) \cong -\Delta x R i_k(t) - \Delta x L \frac{\partial}{\partial t} i_k(t) \quad (2.7)$$

$$i_{k+1}(t) - i_k(t) \cong -\Delta x G v_k(t) - \Delta x C \frac{\partial}{\partial t} v_k(t) \quad (2.8)$$

where (Δx) is the segment length and $k = 1, 2, \dots, M$. The total length of the line is (d) and the line is divided into (M) segments. Hence, $\Delta x = d/M$. Although, the approximation is only valid if (Δx) is chosen to be a small fraction of the wavelength. At high frequencies many lumped segments are required. The number of segments required depends on the electrical length of the line. It is important to know how many segments (M) are needed to obtain the accurate results. The general rule of thumb [6] for this purpose is:

$$M \geq 10\tau/t_r \quad (2.9)$$

where (t_r) is rising time of propagating signals and (τ) is the delay of the line,

$$\tau = d\sqrt{LC} \quad (2.10)$$

Figure 2.6: Discretization of a transmission line

2.5 Jitter

Jitter refers to variations of a digital signal from its ideal position in time. It is one of the major timing related concerns in the design of high-speed systems. It can be classified mainly into two groups: Random Jitter (RJ) and Deterministic Jitter (DJ)[19].

Random jitter is unpredictable and unbounded in nature. The main cause of RJ is the thermal noise in the transistors. It can be represented as a Gaussian distribution [20]. RJ is best represented by statistical standard deviations. Deterministic jitter is bounded and repeatable. Its sources are mostly known or can be predicted. It is usually quantified in terms of peak-to-peak value.

The deterministic jitter (DJ) consists of jitter components such as data-dependent jitter (DDJ) and bounded uncorrelated jitter (BUJ). DDJ are correlated with data pattern in the link. Often passive channel induced several non-idealities (e.g. crosstalk and reflection, etc.) lead to DDJ. Both inter-symbol interference (ISI) and duty cycle distortion (DCD) contribute to DDJ. On the other hand, BUJ is not correlated with the data stream. Sinusoidal jitter (SJ) and periodic jitter (PJ) are the examples of BUJ. SJ is a single-tone of PJ, whereas PJ consists of multiple frequency contents.

2.5.1 Review of Power Supply Induced Jitter (PSIJ)

Component of jitter caused by the power supply variations is known as power supply induced jitter. There are two main factors that determine the PSIJ. First factor is the supply noise. It depends on circuit implementation, data activity and power delivery network. The second factor is how the system timing jitter responds to the noise present in its supply. This factor is determined by the circuit implementation and clocking architecture choice. The traditional modelling approach for PSIJ is shown in Figure 2.7.

Jitter spectrum ($J(f)$) can be developed by combining supply noise spectrum ($V(f)$) and frequency-dependent jitter sensitivity ($S(f)$), as

$$J(f) = V(f) \times S(f) \quad (2.11)$$

Figure 2.7: Power supply induced jitter modelling methodology [3]

Supply noise ($V(f)$) and jitter sensitivity ($S(f)$) are largely decoupled and can be characterised independently. $V(f)$ is the interaction between current profile ($I(f)$) and power delivery network as shown in Figure 2.7. $V(f)$ can be expressed as:

$$V(f) = I(f) \times Z_{PDN}(f) \quad (2.12)$$

where Z_{PDN} is the PDN impedance profile.

Jitter sensitivity ($S(f)$) can be obtained by simulation of pre/post-layout of the transistor level circuit. Usually, a single-tone sinusoidal signal is injected into the supply node as the stimulus. By sweeping the noise frequency over the frequency range of interest, the sensitivity profile can be obtained.

The time-domain jitter ($J(t)$) is constructed by using an inverse Fourier transform, as

$$J(t) = \int_0^\infty J(f) e^{j2\pi f t} df \quad (2.13)$$

Determining worst peak-to-peak (J_{pp}) and identifying the maximum jitter contribution are useful to relate to the system's operating conditions (e.g., clock frequency, data rate, data pattern and so on).

The worst case peak-to-peak (J_{pp}) and accumulated jitter (Γ) can be obtained as:

$$J_{pp} = 2 \times \int_0^\infty J(f) df \quad (2.14)$$

$$\Gamma = \frac{\int_0^f J(f) df}{\int_0^\infty J(f) df} \quad (2.15)$$

The above approach of estimating PSIJ has two fundamental assumptions. First, the supply noise is sufficiently small to be qualified as a small signal. Second, the system jitter response can be approximated as a linear function of the noise [41], [42]. Second assumption may not hold true in general but it is useful as a first-order quantitative analysis tool.

2.5.2 Efficient Modeling of Power Supply Induced Jitter

Efficient Modeling of power supply induced jitter (EMPSIJ) [34], [35] method estimates the PSIJ using just one bit simulation of the entire circuit that leads to significant speed-up. This method is based on analyzing the small and large signal responses, separately. Small signal response is calculated based on the slope of the rising/falling edge of the output response.

The process of estimating PSIJ via EMPSIJ method is shown in Figure 2.8. Figure 2.8(a) represents the large-signal output response ($V_R(t)$) without PND supply noise, which is obtained by one-time simulation of the large signal circuit. The overall response ($v_{R_n}(t)$) of the system is shown in Figure 2.8(b) when the PDN exhibits the noise of v_n , which is obtained using analytical expressions involving the small signal equivalent circuit.

The response of the large signal circuit can be represented as:

$$v_R(t) = \alpha t + k \quad (2.16)$$

where α is the slope of the line, k is the intercept and $v_R(t)$ is the large signal voltage across the load. In the presence of PDN, small signal noise (v_n) at the midpoint of the rising edge (t_m), can be written as:

$$v_{R_n}(t) = \alpha t + k + V_{n_m} \quad (2.17)$$

Figure 2.8: Output responses without (a) and with (b) PND noise

where V_{nm} is the amplitude of small signal noise response (v_{rn}) at the midpoint (t_m) and $v_{Rn}(t)$ is an overall response including the noise contributions.

Next, the midpoints of the rising edge with and without PDN (i.e, t_m and t_{m_o} , respectively) can be obtained by equating (2.16) and (2.17) to zero. Hence, jitter can be obtained as:

$$V_{nm} = \alpha(t_{m_o} - t_m) \quad (2.18)$$

or

$$J_r = \frac{V_{nm}}{\alpha} \quad (2.19)$$

Equation (2.19) can be re-written as:

$$J_r^k = \frac{V_{nm}^k}{\alpha} \quad (2.20)$$

where V_{nm}^k represents the amplitude of the small signal noise response (v_{rn}^k) at the midpoint of its rising edge.

Power supply induced jitter (PSIJ) is usually calculated in terms of peak-to-peak values over ' N ' number of bits. PSIJ can be written as:

$$PSIJ = \max(J_r^1 \dots J_r^k \dots J_r^N) - \min(J_r^1 \dots J_r^k \dots J_r^N) \quad (2.21)$$

The small signal noise has maximum and minimum values over the larger stream of bits. Let $(v_{rn})_{max}$ and $(v_{rn})_{min}$ are the maximum and minimum values, respectively. Hence,

peak-to-peak power supply induced jitter can be obtained as:

$$PSIJ = \frac{(v_{r_n})_{max}}{\alpha} - \frac{(v_{r_n})_{min}}{\alpha} \quad (2.22)$$

$$PSIJ = \frac{(v_{r_n})_{pp}}{\alpha} \quad (2.23)$$

where $(v_{r_n})_{pp}$ is the peak-to-peak output voltage due to power supply noise.

The instantaneous jitter (2.19) is based on the slope of the line (α) and the response V_{n_m} . In frequency domain, v_{r_n} depends on η which represents the transfer function $|H(f)|$ from PDN to the output. Hence, jitter at a particular rising edge due to all frequency can be obtained as:

$$J_r = \frac{1}{\alpha} \sum_{i=1}^{\infty} \eta_i V_{n_{m_i}} \quad (2.24)$$

where the subscript i represents the i^{th} frequency component, η_i represents the i^{th} transfer function and $V_{n_{m_i}}$ represents the amplitude of the noise input corresponding to the i^{th} frequency component at the midpoint of the rising edge. The main advantage of estimating PSIJ using EMPSIJ method is that, it only needs one large signal evaluation when there is no noise in the power supply. On the other hand, effect of noise is considered via transfer function. Unlike conventional methods which requires simulation of thousands of bits, EMPSIJ method enables quick PSIJ estimation based on one bit simulation.

2.6 Summary

This chapter reviewed some of the relevant literature associated with the power integrity. The primary design target of a PDN is to deliver stable power with maximum efficiency and minimal noise. A complete PDN includes off-chip, on-chip and current profile that are required to simulate the supply noise and frequency spectrum. Off-chip components such as VRM, PCB and package are modelled with the corresponding resistances, inductances and capacitances. Off-chip PDN produces DC off-set and contributes to supply noise in the lower-medium frequency range. On the other hand, on-chip power grids and decaps are lumped into resistance and capacitance, respectively. The on-chip switching activity generates high frequency supply noise. In order to reduce this noise, sufficient decap area must be budgeted and allocated.

The PSIJ sensitivity is an important parameter that describes the system jitter response to the supply noise. Traditionally, jitter spectrum is obtained by combining supply noise spectrum and frequency-dependant jitter sensitivity. Furthermore, noise supply is the interaction between current profile and impedance profile of PDN. EMPSIJ method is introduced to estimate PSIJ using just one bit simulation that leads to significant speed-up. This method is based on analyzing the small and large signal responses.

Also, important circuit configurations that are often used in PDNs are reviewed. Voltage mode driver circuit and calculation of its output differential voltage across the load resistor are also reviewed. The output response is often associated with significant delay and ringing due to transmission lines. VMD circuit is further simplified to equivalent small-signal models in order to estimate the power supply induced jitter. Also, transmission line model that is required to accurately represent its electrical behaviour of the interconnect is reviewed.

Chapter 3

Proposed Closed-Form Expressions for Transmission Lines

As discussed in chapter 2, model that is used during PSIJ analysis can have significant impact on the accuracy as well as the CPU cost. Using distributed TL models can be CPU expensive, however, can provide higher accuracy. In the case of the conventional lumped segmentation approach [26], [27], which divides the transmission line into σ number of segments and each segment can be replaced with lumped R, L, G and C components. For accuracy, many lumped segments are required that leads to large circuit matrices and hence simulation becomes CPU inefficient. In order to address this, a new model for TLs is developed which provides an analytical expression in the case of using large number of lumped models. Also, a closed-form expression for transmission line type interconnects including the effect of load is derived.

Sections 3.1, 3.2 and 3.3 describe the modeling of single segment, 2-segments and 3-segments, respectively. In Section 3.4, a generalized closed-form equation for transmission line with σ -segments is derived. In order to check the validity of the closed-form expression, examples with lossless, low-loss and lossy mediums are considered in Section 3.5.

3.1 Modeling with Single Segment and Load

The lumped- π segmentation of a transmission line is shown in the Figure 3.1 with R , L , G and C p.u.l parameters.

Figure 3.1: Equivalent model used for a single unit cell of a transmission line

From Figure 3.1, z_1 and z_2 are defined as:

$$z_1 = (R + j\omega L)/\sigma \quad (3.1)$$

$$z_2 = (G + j\omega C)/2\sigma \quad (3.2)$$

Figure 3.2 shows a single segment with load impedance (z_L). Applying K.C.L at node (v_1) gives:

Figure 3.2: Single segment with load impedance (z_L)

$$(v_i - v_1)y_1 = y_2v_1 + (v_1 - v_o)y_L \quad (3.3)$$

$$(y_1 + y_2 + y_L)v_1 = y_1v_i + y_Lv_o \quad (3.4)$$

$$Yv_1 = y_1v_i + y_Lv_o \quad (3.5)$$

where

$$y_1 = \frac{1}{z_1}; \quad y_2 = \frac{1}{z_2}; \quad y_L = \frac{1}{z_L} \quad (3.6)$$

and

$$Y = y_1 + y_2 + y_L \quad (3.7)$$

are the admittances.

3.2 Modeling with Two Segments and Load

A schematic of two segments ($\sigma = 2$) set up is given in Figure 3.3. Applying KCL at node (v_1) gives:

Figure 3.3: Two segments with load impedance (z_L)

$$(v_i - v_1)y_1 = (2y_2)v_1 + (v_1 - v_2)y_1 \quad (3.8)$$

$$(2y_1 + 2y_2)v_1 = y_1v_i + y_1v_2 \quad (3.9)$$

$$yv_1 = v_i + v_2 \quad (3.10)$$

where

$$y = \left(2 + \frac{2y_2}{y_1}\right) \quad (3.11)$$

Let $C_1 = y$ and $C_0 = 1$. Next, equation (3.10) can be re-written as:

$$C_1v_1 = v_i + C_0v_2 \quad (3.12)$$

KCL at node (v_2) yeilds:

$$Yv_2 = y_1v_1 + y_Lv_0 \quad (3.13)$$

3.3 Modeling with Three Segments and Load

Three segments ($\sigma = 3$) system with load is shown in Figure 3.4. KCL at each node generates the following equations:

$$yv_1 = v_i + v_2 \quad (3.14)$$

$$yv_2 = v_1 + v_3 \quad (3.15)$$

$$Yv_3 = y_1v_2 + y_Lv_0 \quad (3.16)$$

Figure 3.4: Three segments with load impedance (z_L)

Substituting (3.14) into (3.15) produces:

$$(y^2 - 1)v_2 = v_i + yv_3 \quad (3.17)$$

Let $C_2 = (y^2 - 1)$ and we have $C_1 = y$ from (3.12). Hence, (3.17) can be written as:

$$C_2v_2 = v_i + C_1v_3 \quad (3.18)$$

Next, we generalize the above relations for ‘ σ ’ segments.

3.4 Generalization with σ segments and Load

Figure 3.5 shows the transmission line representation with σ –segments. In order to preserve the response upto the maximum frequency of interest (f_{max}), a general rule of thumb [6] that is often used is:

$$\sigma \geq \frac{10\tau l}{t_r} \quad (3.19)$$

where l is the length of the line, t_r is the rise time of the propagating signal and $\tau = \sqrt{LC}$ represents delay per unit length of the line. Once RLGC p.u.l parameters are extracted and ‘ σ ’ is calculated, analytical response of the lumped segmentation model can be obtained as follows. In order to generalize the closed form solution of the transmission line, the relations obtained from the previous sections are used to get the recursive expressions relating the ‘ σ ’ and ‘ $\sigma - 1$ ’ node voltages as shown in Table 3.1.

Figure 3.5: Transmission line with σ -segments.

Using the two general expressions from Table 3.1, a recursive closed-form solution for the transmission line interconnects can be expressed as:

$$y_1 v_i + (y_L C_{\sigma-1}) v_0 = (Y C_{\sigma-1} - y_1 C_{\sigma-2}) v_\sigma \quad (3.20)$$

where, $C_{\sigma-1}$ and $C_{\sigma-2}$ are the coefficients belong to ' $\sigma - 1$ ' and ' $\sigma - 2$ ' segments, respectively. Using the mathematical induction for σ -lumped segments as shown in Figure 3.5, the coefficient (C_σ) can be calculated as:

$$C_\sigma = y C_{\sigma-1} - C_{\sigma-2} \quad (3.21)$$

The coefficients $C_1 \cdots C_{10}$ are given in Table 3.2. Also, the coefficients with the negative subscripts are zeros (for example, $C_{-2} = C_{-1} = 0$) and $C_0 = 1$). Since C_σ depends on the number of segments, it is important to know how many segments (σ) are needed to obtain the accurate results.

Table 3.1: Demonstration of recursive expressions relating ' σ ' and ' $\sigma - 1$ ' node voltages for σ -segments

Number of segments	Node (v_σ)	Node ($v_{\sigma-1}$)
1	$Y v_1 = y_1 v_i + y_L v_0$	—
2	$Y v_2 = y_1 v_1 + y_L v_0$	$C_1 v_1 = v_i + C_0 v_2$
3	$Y v_3 = y_1 v_2 + y_L v_0$	$C_2 v_2 = v_i + C_1 v_3$
4	$Y v_4 = y_1 v_3 + y_L v_0$	$C_3 v_3 = v_i + C_2 v_4$
$\vdots$	$\vdots$	$\vdots$
$\vdots$	$\vdots$	$\vdots$
σ	$Y v_\sigma = y_1 v_{\sigma-1} + y_L v_0$	$C_{\sigma-1} v_{\sigma-1} = v_i + C_{\sigma-2} v_\sigma$

The closed-form solution (3.19) directly relates the input and the output nodes of the transmission line. Using (3.19) eliminates the need for LU decomposition or matrix inversion. It only requires forward-substitution in order to obtain the coefficients in (3.20) which leads to significant speed-up.

Table 3.2: Coefficients (C_σ) of first ten lumped- π segments

Units	Coefficient (C_σ)
$\sigma = 1$	y
$\sigma = 2$	$y^2 - 1$
$\sigma = 3$	$y^3 - 2y$
$\sigma = 4$	$y^4 - 3y^2 + 1$
$\sigma = 5$	$y^5 - 4y^3 + 3y$
$\sigma = 6$	$y^6 - 5y^4 + 6y^2 - 1$
$\sigma = 7$	$y^7 - 6y^5 + 10y^3 - 4y$
$\sigma = 8$	$y^8 - 7y^6 + 15y^4 - 10y^2 + 1$
$\sigma = 9$	$y^9 - 8y^7 + 21y^5 - 20y^3 + 5y$
$\sigma = 10$	$y^{10} - 9y^8 + 28y^6 - 35y^4 + 15y^2 - 1$

3.5 Numerical Examples

In this section, the proposed analytical expressions for the transmission media are validated. For this purpose, several examples with σ -segments are considered and compared with the HSPICE interconnect model based simulations.

3.5.1 *Example-1*

In this example, a 5 cm long lossless microstrip line shown in Figure 3.6 is considered. It is 1.276 mm wide (w) and has 1 μm thick (t) conducting strip over a 0.635 mm thick (h) substrate with a relative permittivity of ($\varepsilon_r = 9.8$). The line is considered to be lossless and the RLGC-parameters of the line are extracted at 1.794 GHz: $R = G = 0$, $C = 266.04$ pF/m and $L = 295.43$ nH/m.

Input and output terminals of the microstrip are attached with 50Ω resistors as shown in Figure 3.7. Corresponding results using the proposed transmission line expression (3.19) for 5-segments, 15-segments and 30-segments are given in Figure 3.8, 3.9 and 3.10, respectively.

Figure 3.6: Cross-section area of a microstrip line.

Figure 3.7: Network with lossless transmission line of Fig. 3.6

These results are compared against the T-element (considered as an accurate response) and the U-element (which represents the lumped segmentation model) interconnect model based simulations using HSPICE. While using the U-model, same number of segments are used as is used for the corresponding graphs while employing the proposed analytical expressions.

As can be seen, with the increasing number of segments of the transmission line, the response of the lumped segmentation model captures the higher bandwidth and becomes comparable to the response of the distributed model response.

Figure 3.8: Comparison of responses for lossless microstrip line with 5 segments (Example 1).

Figure 3.9: Comparison of responses for lossless microstrip line with 15 segments (Example-1)

Figure 3.10: Comparison of responses for lossless microstrip line with 30 segments (Example-1)

3.5.2 Example-2

In this example, a 15 cm long lossy microstrip line is considered. Table 3.3 provides the physical and extracted lumped parameters of the interconnect using W-element in HSPICE. The circuit similar to the one in Figure 3.7 is considered for the analysis, with

Table 3.3: Physical and extracted RLGC-parameters of lossy microstrip line

Physical Parameters		Extracted RLGC Parameters	
Width (w)	5 mil	Inductance (L)	149.83 nH/m
Height (h)	1 mil	Resistance (R)	5.27 Ω /m
Thickness (t)	1 mil	Conductance (G)	0.5 mS/m
Permittivity (ϵ_r)	5.8	Capacitance (C)	328.62 pF/m

$R_g = 50\Omega$ and $R_L = 50\Omega$. The output responses for segments $\sigma = 5, 15$ and 40 are simulated using the proposed model (3.19), U-element model (which provides lumped segmentation based response) and the W-element model (considered as an accurate response for the lossy distributed line) of the HSPICE. As seen in Figures (3.11), (3.12) and (3.13), the results using the proposed closed-form relations and W-element model of HSPICE match reasonably well with the increase in the number of segments.

Also, as can be seen, the results obtained from the proposed closed-form relations and U-element model match accurately. An error comparison between the U-element model and the proposed analytical expression based evaluations as well as with the W-element is given in Table 3.4. Table 3.5 gives the CPU time comparisons while using the U-element and the proposed model.

Figure 3.11: Comparison of responses for lossy microstrip line with 5 segments (Example-2)

Figure 3.12: Comparison of responses for lossy microstrip line with 15 segments (Example-2)

Figure 3.13: Comparison of responses for lossy microstrip line with 40 segments (Example-2)

Table 3.4: Maximum percentage error comparison for lossy line

σ	U-Element vs. W-element	U-Element vs. Proposed Model
5	100 %	0.000010 %
15	5.33 %	0.000012 %
40	0.05 %	0.000017 %

Table 3.5: CPU time comparison for lossy line

σ	U-Element	Proposed Model	Speed-up
5	0.365 sec	0.019 sec	19.20
15	1.850 sec	0.084 sec	22.02
40	4.57 sec	0.160 sec	28.56

It is to be noted that HSPICE (U-element) sets up the MNA matrix of a circuit and evaluates the response using LU decomposition and forward-backward substitution for each iteration. As the number of segments increases, matrix size grows and the simulation becomes CPU inefficient. On the other hand, proposed closed-form expression solves the system analytically. This leads to lower computational cost. It is to be noted that the proposed analytical expressions are implemented in MATLAB and experiments are conducted on a Dell XPS desktop computer (with 4.2 GHz Intel 4-Core processor). As seen, the proposed method yields good speed-up compared to the HSPICE U-element.

3.6 Summary

In this section, new analytical expressions are developed for modelling of transmission lines while using ' σ ' segments and load. The output response of the analytical expression is evaluated and compared with HSPICE simulator. It is observed from several examples that, with the increasing number of segments, the proposed model achieves higher bandwidth, and matches the results from HSPICE, thus validating the accuracy of the proposed closed-form relations.

Chapter 4

Proposed Jitter Estimation Algorithm Including Supply Noise, Ground Bounce and Transmission Media

In this chapter, the EMPSIJ method [34], [35] (reviewed in Chapter 2) for estimating power supply induced jitter is advanced to handle the combined effects of both ground bounce and transmission media. Also, representing the transmission media, the closed-form expressions for the transmission lines developed in Chapter 3 are employed for estimating the PSIJ. Details of the chapter are outlined as follows:

- Thévenin equivalent circuit and small-signal differential output of voltage mode driver with supply noise is presented in Sections 4.1 and 4.2, respectively.
- In Sections 4.3 and 4.4, the analysis are also advanced to include the ground bounce.
- In Section 4.5, validating examples are provided with different noise sources to estimate power supply induced jitter.

4.1 Thévenin Equivalent with Supply Noise

For the purpose of development of the proposed semi-analytical expressions for power supply induced jitter (PSIJ), an illustrative case of voltage mode driver (VMD) circuit shown in Figure 4.1 is considered. VDM circuit is widely used as a low voltage differential signalling in high-speed serial links [39] and discussed in detail in Section 2.3. The external load resistor (R_L) is connected to M1 and M2 through two transmission lines (TL1 and TL2). The power rail has a supply noise (v_n) and ground bounce voltage (v_g) is attached to the ground node.

Figure 4.1: Voltage mode driver with transmission media, supply noise and ground bounce

Transmission lines (that characterizes the transmission media) in Figure 4.1 represent the PCB traces connecting the differential output to the load. Ground bounce (v_g) represents the shift in ground voltage from the reference level.

The semi-analytical expressions for PSIJ estimation are derived via a small signal analysis for each of the sources at a time and later combined using the Super Position Theorem. For this purpose, in the first step, the small-signal equivalent circuit of Figure 4.1 (without ground bounce) is used as shown in Figure 4.2. Figure 4.2 is further simplified using the Thévenin equivalent between nodes v_q and v_e as illustrated in Figure 4.3 which will be used to derive the impact of the power supply noise on the differential output.

Figure 4.2: Small-signal circuit with TLs and load resistor (with $v_g = 0$)

Figure 4.3: Thévenin equivalent simplified circuit

where, v_{th} and Z_{th} are the Thévenin equivalent voltage and impedance, respectively. Note that, Thévenin equivalent voltage (v_{th}) is an open circuit voltage between nodes v_q and v_e , and Thévenin equivalent impedance (Z_{th}) is the ratio of Thévenin voltage and short circuit current (i_{sc}) between nodes v_q and v_e . Thévenin equivalent impedance can be defined as:

$$Z_{th} = v_{th}/i_{sc} \quad (4.1)$$

Both v_{th} and Z_{th} are dependent on the small signal parameters and the corresponding detailed relations are derived in the next section.

4.1.1 Closed-form Expression for the Thévenin Equivalent Voltage

In this section, development of Thévenin equivalent voltage (v_{th}) across v_q and v_e is presented. Using (4.3)–(4.8), Figure 4.2 is simplified in the form of Figure 4.4 and an open circuit voltage between nodes v_q and v_e is defined as:

$$v_{th} = v_q - v_e \quad (4.2)$$

The equivalent impedances of Figure 4.4 are defined relating the corresponding elements in Figure 4.2 as follows:

$$Z_1 = Z_{R_{onp}} || Z_{C_{dsp}} = \frac{R_{onp}}{1 + j\omega_n R_{onp} C_{dsp}} \quad (4.3)$$

$$Z_2 = Z_{C_{gd2}} || Z_{C_{gs3}} = \frac{1}{j\omega_n (C_{gd2} + C_{gs3})} \quad (4.4)$$

$$Z_3 = Z_{C_{gd3}} = \frac{1}{j\omega_n C_{gd3}} \quad (4.5)$$

$$Z_4 = Z_{R_{on3}} || Z_{C_{ds3}} = \frac{R_{on3}}{1 + j\omega_n R_{on3} C_{ds3}} \quad (4.6)$$

$$Z_5 = Z_{C_{gs2}} = \frac{1}{j\omega_n C_{gs2}} \quad (4.7)$$

$$Z_6 = Z_{r_{o2}} || Z_{C_{ds2}} = \frac{r_{o2}}{1 + j\omega_n r_{o2} C_{ds2}} \quad (4.8)$$

Figure 4.4: Thévenin equivalent voltage (v_{th}) between v_q and v_e nodes

Using nodal analysis at nodes v_e , v_q and v_p gives:

$$\left[g_{m_2} + \frac{1}{Z_5} \right] v_p = \left[g_{m_2} + \frac{1}{Z_5} + \frac{1}{Z_6} \right] v_e \quad (4.9)$$

$$v_q = \left(\frac{Z_4}{Z_3 + Z_4} \right) v_p \quad (4.10)$$

$$\frac{v_n}{Z_1} = \left[\frac{1}{Z_1} + \frac{1}{Z_2} + \frac{1}{Z_3 + Z_4} + \frac{1}{Z_5} \right] v_p - \frac{v_e}{Z_5} \quad (4.11)$$

Let β_1 and β_2 be the small-signal parameters related to node v_e and v_q , defined as

$$\beta_1 = \frac{g_{m_2} + Z_5^{-1}}{g_{m_2} + Z_5^{-1} + Z_6^{-1}} \quad (4.12)$$

$$\beta_2 = \frac{Z_4}{Z_3 + Z_4} \quad (4.13)$$

Equations (4.9) and (4.10) can be rewritten as:

$$v_e = \beta_1 v_p \quad (4.14)$$

$$v_q = \beta_2 v_p \quad (4.15)$$

Substituting (4.14) in (4.11) gives:

$$\frac{v_n}{Z_1} = \left[\frac{1}{Z_1} + \frac{1}{Z_2} + \frac{1}{Z_3 + Z_4} + \frac{1}{Z_5} - \frac{\beta_1}{Z_5} \right] v_p \quad (4.16)$$

Let β_3 be the parameter associated with node (v_p) .

$$\beta_3 = \frac{1}{Z_1} \left[\frac{1}{Z_1} + \frac{1}{Z_2} + \frac{1}{Z_3 + Z_4} + \frac{1}{Z_5} - \frac{\beta_1}{Z_5} \right]^{-1} \quad (4.17)$$

Equation (4.16) becomes:

$$v_p = \beta_3 v_n \quad (4.18)$$

Next, Thévenin equivalent voltage (v_{th}) can be computed by substituting v_q and v_e in (4.2). Hence,

$$v_{th} = v_q - v_e = \beta v_n \quad (4.19)$$

where

$$\beta = \beta_3 [\beta_2 - \beta_1] \quad (4.20)$$

4.1.2 Thévenin Equivalent Impedance between Nodes v_q and v_e

In this section, development of Thévenin equivalent impedance (Z_{th}) across v_q and v_e is presented. Thévenin equivalent impedance (Z_{th}) is defined as: the ratio of Thévenin voltage and short circuit current ($Z_{th} = v_{th}/i_{sc}$).

Figure 4.5: Small-signal circuit for Thévenin equivalent impedance (Z_{th})

Figure 4.5 shows the short circuit connection between nodes v_q and v_e . Similar to equations (4.9) and (4.16), KCL at nodes v_e and v_p yield:

$$v_e = \left[\frac{g_{m_2} + Z_8^{-1}}{g_{m_2} + Z_7^{-1} + Z_8^{-1}} \right] v_p \quad (4.21)$$

$$\frac{v_n}{Z_1} = \left[\frac{1}{Z_1} + \frac{1}{Z_2} + \frac{1}{Z_8} - \frac{\beta_6}{Z_8} \right] v_p \quad (4.22)$$

where $Z_7 = Z_4 || Z_6$ and $Z_8 = Z_3 || Z_5$

Let β_6 and β_7 be defined as:

$$\beta_6 = \frac{g_{m_2} + Z_8^{-1}}{g_{m_2} + Z_7^{-1} + Z_8^{-1}} \quad (4.23)$$

$$\beta_7 = \frac{1}{Z_1} \left[\frac{1}{Z_1} + \frac{1}{Z_2} + \frac{1}{Z_8} - \frac{\beta_6}{Z_8} \right]^{-1} \quad (4.24)$$

$$v_e = \beta_6 v_p \quad (4.25)$$

$$v_p = \beta_7 v_n \quad (4.26)$$

Next, short circuit current is determined by using KCL at node v_e .

$$i_{sc} = \left[g_{m_2} + \frac{1}{Z_5} + \frac{1}{Z_6} \right] v_e - \left[g_{m_2} + \frac{1}{Z_5} \right] v_p \quad (4.27)$$

Using (4.25)–(4.27) gives the short circuit current (i_{sc}) as:

$$i_{sc} = \gamma v_n \quad (4.28)$$

where

$$\gamma = \beta_7 \left[(g_{m_2} + Z_5^{-1})(\beta_6 - 1) + \frac{\beta_6}{Z_6} \right] \quad (4.29)$$

Next, Thévenin equivalent impedance (Z_{th}) can be computed as:

$$Z_{th} = \frac{v_{th}}{i_{sc}} = \frac{\beta v_n}{\gamma v_n} = \frac{\beta}{\gamma} \quad (4.30)$$

4.2 Analytical Expression for Differential Output with Supply Noise

The objective of this section is to determine the output differential voltage (v_{r_n}) in the presence of supply noise (v_n). For this purpose, Thévenin equivalent circuit of Figure 4.3 is used to obtain the differential output across the load resistor (R_L) without ground bounce ($v_g = 0$). Hence, both transmission lines with R, L, G and C as p.u.l parameters are modelled using lossy lumped π -model with σ -segments as illustrated in Figure 4.6.

Next, the differential output (v_{r_n}) is the voltage across the resistor (R_L) placed between two transmission lines. The differential output voltage is given as:

$$v_{r_n} = v_x - v_y \quad (4.31)$$

Using nodal analysis at node (v_q):

$$\frac{v_{th}}{Z_{th}} + \frac{v_{1a}}{z_1} = \left[\frac{1}{z_1} + \frac{1}{z_2} + \frac{1}{Z_{th}} \right] v_q \quad (4.32)$$

Parameter λ_1 is defined as:

$$\lambda_1 = \frac{1}{z_1} + \frac{1}{z_2} + \frac{1}{Z_{th}} \quad (4.33)$$

Equation (4.32) can be written as:

$$v_{th} = Z_{th} \left[\lambda_1 v_q - \frac{v_{1a}}{z_1} \right] \quad (4.34)$$

Next, the general expression for the transmission line (TL2) connected between nodes v_e and v_x can be obtained using (3.19) as:

$$y_1 v_e + [y_L C_{\sigma-1}] v_x = [Y C_{\sigma-1} - y_1 C_{\sigma-2}] v_y \quad (4.35)$$

Since v_e is grounded, the above expression becomes:

$$v_x = \left[\frac{Y C_{\sigma-1} - y_1 C_{\sigma-2}}{y_L C_{\sigma-1}} \right] v_y \quad (4.36)$$

Define parameter λ_2 as:

$$\lambda_2 = \frac{Y C_{\sigma-1} - y_1 C_{\sigma-2}}{y_L C_{\sigma-1}} \quad (4.37)$$

Next, (4.36) can be re-written as:

$$v_x = \lambda_2 v_y \quad (4.38)$$

General expression for the transmission line (TL1) connected between nodes v_q and v_y is given as:

$$y_1 v_q + [y_L C_{\sigma-1}] v_y = [Y C_{\sigma-1} - y_1 C_{\sigma-2}] v_x \quad (4.39)$$

Similarly,

$$y_1 v_{1a} + [y_L C_{\sigma-2}] v_y = [Y C_{\sigma-2} - y_1 C_{\sigma-3}] v_x \quad (4.40)$$

Substituting (4.38) into (4.39) and (4.40) yields:

$$v_{1a} = y_1^{-1} [(Y C_{\sigma-2} - y_1 C_{\sigma-3}) \lambda_2 - y_L C_{\sigma-2}] v_y \quad (4.41)$$

$$v_q = y_1^{-1} [(Y C_{\sigma-1} - y_1 C_{\sigma-2}) \lambda_2 - y_L C_{\sigma-1}] v_y \quad (4.42)$$

Let λ_3 and λ_4 be defined as:

$$\lambda_3 = y_1^{-1} [(Y C_{\sigma-2} - y_1 C_{\sigma-3}) \lambda_2 - y_L C_{\sigma-2}] \quad (4.43)$$

$$\lambda_4 = y_1^{-1} [(Y C_{\sigma-1} - y_1 C_{\sigma-2}) \lambda_2 - y_L C_{\sigma-1}] \quad (4.44)$$

Next, v_{1a} and v_q can be evaluated as:

$$v_{1a} = \lambda_3 v_y \quad (4.45)$$

$$v_q = \lambda_4 v_y \quad (4.46)$$

Next, v_y can be evaluated by substituting (4.45) and (4.46) in (4.34) as:

$$v_y = \left[Z_{th} \left(\lambda_1 \lambda_4 - \frac{\lambda_3}{z_1} \right) \right]^{-1} v_{th} \quad (4.47)$$

Define parameter λ_5 as:

$$\lambda_5 = \left[Z_{th} \left(\lambda_1 \lambda_4 - \frac{\lambda_3}{z_1} \right) \right]^{-1} \quad (4.48)$$

which yields

$$v_y = \lambda_5 v_{th} \quad (4.49)$$

Next, the differential output (v_{r_n}) (the difference between v_x and v_y) can be calculated as by substituting v_x (4.38) in (4.31).

$$v_{r_n} = v_x - v_y = \lambda_2 v_y - v_y = (\lambda_2 - 1) v_y \quad (4.50)$$

Using (4.49) and (4.50), the differential output voltage can be obtained as:

$$v_{r_n} = v_x - v_y = \lambda_5 (\lambda_2 - 1) v_{th} \quad (4.51)$$

or

$$v_{r_n} = \lambda v_{th} \quad (4.52)$$

where

$$\lambda = \lambda_5 (\lambda_2 - 1) \quad (4.53)$$

Semi-analytical expressions developed in this section give the small-signal differential output voltage with respect to supply noise. In the next section, analysis are further advanced to include ground bounce in the system.

4.3 Thévenin equivalent Circuit Analysis including Supply Noise and Ground Bounce

In the previous section, only supply noise input was included while evaluating the output noise response. This section focuses on developing semi-analytical expressions for the

differential output voltage (v_{rn}) including the effects of both the transmission media and ground bounce along with the supply noise. The small-signal model shown in Figure 4.7 contains the ground bounce voltage (v_g), noise source (v_n) and transmission lines (TL1 and TL2) with load resistor (R_L).

Figure 4.7 is simplified to Thévenin equivalent circuit Figure 4.8 similar to Figure 4.3. In Figure 4.3, the v_{th} and Z_{th} are replaced with new symbols $\tilde{v}_{th}$ and $\tilde{Z}_{th}$ respectively, to indicate the additional contributions from the ground bounce voltage (v_g).

Figure 4.7: Small-signal circuit including both supply and ground noise

Figure 4.8: Thévenin Equivalent circuit including both supply and ground noise

4.3.1 Thévenin Equivalent Voltage with Ground Bounce

Consider Figure 4.9 with both the power supply noise and ground bounce voltages. The Thévenin equivalent voltage ($\tilde{v}_{th}$) between node v_q and v_e can be expressed as:

$$\tilde{v}_{th} = \beta_n v_n + \beta_g v_g \quad (4.54)$$

where β_n is the parameter related to supply noise and β_g corresponds to ground bounce noise. Applying KCL at node (v_q), (v_e) and (v_p) in the presence of supply noise gives the

Figure 4.9: Small-signal for Thévenin equivalent voltage ($\tilde{v}_{th}$) including ground bounce noise.

following expressions:

$$v_q|_n = \left[\frac{Z_4}{Z_3 + Z_4} \right] v_p|_n = \frac{v_p|_n}{(1 + \frac{Z_3}{Z_4})} \quad (4.55)$$

$$v_e|_n = \left[\frac{g_{m2} + Z_5^{-1}}{g_{m2} + Z_5^{-1} + Z_6^{-1}} \right] v_p|_n \quad (4.56)$$

$$\frac{v_n}{Z_1} = \left[\frac{1}{Z_1} + \frac{1}{Z_2} + \frac{1}{Z_3} + \frac{1}{Z_5} \right] v_p|_n - \frac{v_q|_n}{Z_3} - \frac{v_e|_n}{Z_5} \quad (4.57)$$

where $v_q|_n$, $v_e|_n$ and $v_p|_n$ represent the voltages at node (v_q), (v_e) and (v_p) in the presence of supply noise, respectively.

Let β_{3_g} be defined as:

$$\beta_{3_g} = \frac{g_{m2} + Z_5^{-1}}{g_{m2} + Z_5^{-1} + Z_6^{-1}} \quad (4.58)$$

Using (4.58), $v_e|_n$ (4.56) becomes:

$$v_e|_n = \beta_{3_g} v_p|_n \quad (4.59)$$

Substituting (4.55) and (4.59) in (4.57) leads to:

$$\frac{v_n}{Z_1} = \left[\frac{1}{Z_1} + \frac{1}{Z_2} + \frac{1}{Z_3} + \frac{1}{Z_5} - \frac{1}{Z_3} \frac{1}{(1 + \frac{Z_3}{Z_4})} - \frac{\beta_{3g}}{Z_5} \right] v_p|_n \quad (4.60)$$

Let β_{5g} be defined as:

$$\beta_{5g} = \left[\frac{1}{Z_1} + \frac{1}{Z_2} + \frac{1}{Z_3} + \frac{1}{Z_5} \right] \quad (4.61)$$

and

$$\beta_{6g} = \left[\beta_{5g} - \frac{1}{Z_3} \frac{1}{(1 + \frac{Z_3}{Z_4})} - \frac{\beta_{3g}}{Z_5} \right] \quad (4.62)$$

Next, voltage $v_p|_n$ (4.60) can be expressed as:

$$v_p|_n = \frac{v_n}{Z_1 \beta_{6g}} \quad (4.63)$$

Applying KCL at nodes (v_q) , (v_e) and (v_p) in the presence of just ground bounce noise (v_g) (with v_n sets to zero) generates:

$$v_q|_g = \frac{v_g}{(1 + \frac{Z_4}{Z_3})} + \frac{v_p|_g}{(1 + \frac{Z_3}{Z_4})} \quad (4.64)$$

$$v_e|_g = \frac{1}{Z_6} \left[\frac{1}{g_{m2} + Z_5^{-1} + Z_6^{-1}} \right] v_g + \left[\frac{g_{m2} + Z_5^{-1}}{g_{m2} + Z_5^{-1} + Z_6^{-1}} \right] v_p|_g \quad (4.65)$$

$$\left[\frac{1}{Z_2} + \frac{1}{Z_3 + Z_5} + \frac{\beta_{4g}}{Z_5} \right] v_g = \left[\beta_{5g} - \frac{1}{Z_3} \frac{1}{(1 + \frac{Z_3}{Z_4})} - \frac{\beta_{3g}}{Z_5} \right] v_p|_g \quad (4.66)$$

Let β_{4g} and β_{7g} be:

$$\beta_{4g} = \frac{1}{Z_6} \left[\frac{1}{g_{m2} + Z_5^{-1} + Z_6^{-1}} \right] = \left[1 + \frac{Z_6}{Z_5} + g_{m2} Z_6 \right]^{-1} \quad (4.67)$$

$$\beta_{7g} = \left[\frac{1}{Z_2} + \frac{1}{Z_3 + Z_5} + \frac{\beta_{4g}}{Z_5} \right] \quad (4.68)$$

Using (4.58), (4.62), (4.67) and (4.68), the node voltages $v_e|_g$ (4.65) and $v_p|_g$ (4.66) can be obtained as:

$$v_e|_g = \beta_{4g} v_g + \beta_{3g} v_p|_g \quad (4.69)$$

$$\beta_{6g} v_p|_g = \beta_{7g} v_g \rightarrow v_p|_g = \frac{\beta_{7g}}{\beta_{6g}} v_g \quad (4.70)$$

Next, Thévenin equivalent voltage (v_{th}) with respect to supply noise can be expressed as:

$$v_{th}|_n = v_q|_n - v_e|_n \quad (4.71)$$

Substituting $v_q|_n$ (4.55), $v_e|_n$ (4.59) in above expression leads to:

$$v_{th}|_n = \underbrace{\left[\underbrace{\frac{1}{Z_1\beta_{6g}} \left(\frac{1}{1 + \frac{Z_3}{Z_4}} \right)}_{\beta_{8g}} + \overbrace{\frac{\beta_{3g}}{Z_1\beta_{6g}}}^{\beta_{10g}} \right]}_{\beta_n} v_n \quad (4.72)$$

Similarly, Thévenin equivalent voltage (v_{th}) with respect to ground bounce can be computed as:

$$v_{th}|_g = v_q|_g - v_e|_g \quad (4.73)$$

Substituting $v_q|_g$ (4.64), $v_e|_g$ (4.69) in (4.73) gives:

$$v_{th}|_g = \left[\frac{1}{(1 + \frac{Z_4}{Z_3})} - \beta_{4g} + \frac{\beta_{7g}}{\beta_{6g}} \frac{1}{(1 + \frac{Z_3}{Z_4})} - \frac{\beta_{3g}\beta_{7g}}{\beta_{6g}} \right] v_g \quad (4.74)$$

Rearranging the terms leads to:

$$v_{th}|_g = \underbrace{\left[\underbrace{\left(\frac{1}{(1 + \frac{Z_4}{Z_3})} + \frac{\beta_{7g}}{\beta_{6g}} \frac{1}{(1 + \frac{Z_3}{Z_4})} \right)}_{\beta_{9g}} - \underbrace{\left(\beta_{4g} + \frac{\beta_{3g}\beta_{7g}}{\beta_{6g}} \right)}_{\beta_{11g}} \right]}_{\beta_g} v_g \quad (4.75)$$

Overall Thévenin equivalent voltage ($\tilde{v}_{th}$) between nodes (v_e) and (v_q) is obtained using superposition theorem as a combination of individual Thévenin voltages associated with respect to supply noise and ground bounce. Therefore,

$$\tilde{v}_{th} = v_{th}|_g + v_{th}|_n \quad (4.76)$$

$$\tilde{v}_{th} = \beta_g v_g + \beta_n v_n \quad (4.77)$$

where

$$\beta_g = \beta_{9g} + \beta_{11g} \text{ and } \beta_n = \beta_{8g} + \beta_{10g} \quad (4.78)$$

4.3.2 Thévenin Equivalent Impedance including Supply Noise and Ground Bounce Effects

Thévenin equivalent impedance ($\tilde{Z}_{th}$) is the ratio of open circuit voltage and short circuit currents as described in section 4.1.2. Open circuit voltage ($\tilde{v}_{th}$) is already computed in

section 4.3.1. For short circuit current ($\tilde{i}_{sc}$) analysis, Figure 4.10 is considered. Similar to (4.77), short circuit current can be defined as:

$$\tilde{i}_{sc} = \gamma_g v_g + \gamma_n v_n \quad (4.79)$$

where γ_g and γ_n are the small signal parameters associated with the short circuit current with ground bounce and supply noise, respectively. Therefore, the Thévenin equivalent impedance ($\tilde{Z}_{th}$) is given as:

$$\tilde{Z}_{th} = \frac{\tilde{v}_{th}}{\tilde{i}_{sc}} = \frac{\beta_g v_g + \beta_n v_n}{\gamma_g v_g + \gamma_n v_n} \quad (4.80)$$

Using the nodal analysis as presented in section 4.3.1 and computing the equations at nodes v_e , v_q and v_p with respect to ground bounce noise (v_g) and supply noise (v_n) gives the following parameters:

$$\gamma_{3_g} = \left[g_{m_2} + \frac{1}{Z_5} + \frac{1}{Z_6} \right] - \frac{1}{\beta_{5_g}} \left[g_{m_2} + \frac{1}{Z_5} \right] \left[\frac{1}{Z_3} + \frac{1}{Z_5} \right] \quad (4.81)$$

$$\gamma_{4_g} = \frac{1}{Z_6} - \left[g_{m_2} + \frac{1}{Z_5} \right] \frac{1}{Z_2 \beta_{5_g}} \quad (4.82)$$

$$\gamma_{5_g} = \left[g_{m_2} + \frac{1}{Z_5} \right] \frac{1}{Z_1 \beta_{5_g}} \quad (4.83)$$

$$\gamma_{6_g} = (Z_3^{-1} + Z_5^{-1}) \left[\frac{1}{Z_3 \beta_{5_g}} - 1 \right] \quad (4.84)$$

Figure 4.10: Small-signal circuit for Thévenin equivalent impedance (Z_{th}) including supply noise and ground bounce

Parameters corresponding to noise voltage and ground bounce are calculated as:

$$\gamma_g = \frac{Z_4^{-1} + (Z_2 Z_3 \beta_{5_g})^{-1} + \gamma_{4_g} \gamma_{6_g} (\gamma_{3_g})^{-1}}{1 - \gamma_{6_g} (\gamma_{3_g})^{-1}} \quad (4.85)$$

$$\gamma_n = \frac{(Z_1 Z_3 \beta_{5_g})^{-1} + \gamma_{5_g} \gamma_{6_g} (\gamma_{3_g})^{-1}}{1 - \gamma_{6_g} (\gamma_{3_g})^{-1}} \quad (4.86)$$

Proposed relations for open circuit voltage and Thévenin impedance help to simplify the small-signal circuit with ground bounce to a Thévenin equivalent circuit as shown in Figure 4.11.

Figure 4.11: Thévenin Equivalent circuit including both supply and ground noise

Similar analysis, as described in section 4.2, is performed in order to obtain the small-signal differential voltage across the load resistor (R_L) in the presence of both supply noise and ground bounce voltage as well as transmission media (TL1 and TL2); in the next section.

4.4 Differential Output in the presence of both Supply Noise and Ground Bounce as well as Transmission Media

Similar to the analysis in Section 4.2, transmission lines in Figure 4.11 are replaced with lossy lumped RLGC-parameters with σ -segments as illustrated in Figure 4.12.

Due to the addition of ground bounce noise, v_{th} and Z_{th} (in section 4.1) are replaced with $\tilde{v}_{th}$ and $\tilde{Z}_{th}$, respectively. Similarly, the differential output voltage is symbolised as $\tilde{v}_{r_n}$.

It can be obtained using the set of equations (4.31)–(4.53) as explained in section 4.2. As a result the differential output is given as:

$$\tilde{v}_{r_n} = \tilde{\lambda} \tilde{v}_{th} \quad (4.87)$$

where

$$\tilde{\lambda} = \tilde{\lambda}_5(\lambda_2 - 1) \quad (4.88)$$

and $\tilde{\lambda}_5$ is given as:

$$\tilde{\lambda}_5 = \left[\tilde{Z}_{th} \left(\lambda_1 \lambda_4 - \frac{\lambda_3}{z_1} \right) \right]^{-1} \quad (4.89)$$

Also, $\tilde{Z}_{th}$, λ_1 , λ_3 and λ_4 are defined in (4.80), (4.33), (4.43) and (4.44), respectively. Semi-analytical expression for output differential voltage ($\tilde{v}_{r_n}$) is obtained as in (4.87), in order to estimate the power supply induced jitter. Using EMPSIJ method, the expression for k_{th} bit time interval error (jitter) is given as:

$$\text{TIE}^k = J_r^k = \frac{(\tilde{v}_{r_n}^k)_{t_m}}{\alpha} \quad (4.90)$$

where α is the slope of the output in the absence of any noise and $(\tilde{v}_{r_n}^k)_{t_m}$ is the amplitude of the small-signal differential noise response at the midpoint of the rising edge of the k_{th} bit. The corresponding steps are summarised as a pseudocode in Algorithm-1 for obtaining the jitter due to any periodic PDN noise.

Algorithm-1 Proposed PSIJ estimation including the effects of supply noise, ground bounce and transmission media.

Inputs: Noise inputs $v_n(t)$ and $v_g(t)$

Output: PSIJ

Computational steps:

Initialise number of Bits (N) and $J_{max} = J_{min} = 0$

Frequency of PRBS (f_d) $\rightarrow T_d = \frac{1}{f_d}$

Fourier coefficients of $v_n(t)$ of length Q .

Differential output without noise ($v_R(t)$)

Transfer function ($\eta(f) = v_{r_n}/v_n + v_{r_n}/v_g$)

Calculate: t_{m_0} (at $v_R(t) = 0$) and slope (α)

for $k = 1$ to N

$t_{m_k} = t_{m_0} + (k + 1)T_d$

for $i = 1$ to Q

$\tilde{V}_{m_n}^k = p_i \sin(2\pi f_i t_{m_k})$

Calculate: η_i at $f = f_i$

$J_r^k = \frac{\eta}{\alpha} \left(\tilde{V}_{r_n}^k \right)_{t_{m_i}}$

end for

$J_r^k = \sum_{i=0}^Q J_{r_i}^k$

if $J_r^k \leq 0$ **then**

$J_r^k = -|J_r^k|$

else

$J_r^k = |J_r^k|$

end if

end for

PSIJ = $\max(J_r^1 \cdots J_r^N) - \min(J_r^1 \cdots J_r^N)$

Return PSIJ

4.5 Examples

In this section, validating examples are presented for the proposed semi-analytical expressions. In these examples, voltage mode driver circuit (Figure 4.1) operating at 167 Mbps (with $V_{DD} = 3V$ and $V_{DD1} = 5V$) is considered. Also, LEVEL-49 HSPICE parameters [45] are used to simulate n-channel and p-channel devices. In addition, a single-pole macromodel of an opamp [46] is used in voltage regulator circuit. Results of PSIJ using ‘*Algorithm-1*’ are compared with HSPICE simulator where transmission lines are represented by W-element.

4.5.1 Example-1

This example demonstrates the validity of the proposed method. For this purpose, simplified Thévenin equivalent circuit with transmission lines shown in Figure 4.6 is used to estimate PSIJ and 15-segments (σ) are used to represent these transmission lines. In this example, a 15 mm long lossless microstrip line with 1.276 mm wide (w) conducting strip over a 0.635 mm thick (h) substrate with a relative permittivity of ($\epsilon_r = 9.8$) is considered.

Figure 4.13: Comparison of PSIJ for square wave noise input

The cross-section of the TLs is shown in Figure 3.6. The LC parameters of the line are extracted using W-element in HSPICE. The power supply noise is in the form of a square wave of frequency 446.4 MHz which is superimposed on power supply (V_{DD}). A peak-to-

peak amplitude of the supply noise is varied from 0 to $VDD/15$ and corresponding PSIJ is evaluated in the absence of ground bounce. Also, 30 dominant frequencies are used for reconstruction of the square noise waveform.

Figure 4.13 shows the comparison of responses from the proposed approach with the HSPICE. As seen in Figure 4.13, the results using the semi-analytical relations match reasonably well with HSPICE. Table 4.1 compares the CPU time for PSIJ estimation. As seen, the proposed approach yields significant speed up.

Table 4.1: CPU time comparison for PSIJ

Number of simulated bits	HSPICE	Proposed Algorithm
10,000 bits	64.6 sec	1.19 sec
100,000 bits	598 sec	3.85 sec

4.5.2 *Example-2*

In this example, impact of both lossy transmission line (with 30 segments) and ground bounce ($v_g = 10\text{ mV}$) are investigated. For this purpose, Figure 4.12 is considered and cross-section of the TLs is illustrated in Figure 3.6. PDN noise is in the form of a saw-tooth wave and 250 dominant frequencies are used for reconstruction of the saw-tooth noise waveform. The operating frequency of PDN noise is 980.4 MHz. The PCB trace considered is 15 mm long, 2.745 mm wide and $18\mu\text{m}$ thick. The relative permittivity and thickness of the substrate are 2.5 and 0.625 mm, respectively. Noise peak-to-peak amplitude is considered to be varying from 0 to $VDD/10$ and corresponding PSIJ is evaluated to observe the impact of both the lossy media and ground bounce on PSIJ.

As seen in Figure 4.14, the results from the proposed approach and HSPICE match reasonably well. Table 4.2 compares the CPU time for PSIJ estimation that yields significant speed up (of 155).

Figure 4.14: Comparison of PSIJ for saw-tooth noise input including ground bounce

Table 4.2: CPU time comparison for PSIJ

Number of simulated bits	HSPICE	Algorithm time
10,000 bits	89s	1.90s
100,000 bits	647s	4.15s

4.6 Summary

This chapter focused on developing semi-analytical expressions for the power supply induced jitter (PSIJ) including the effects of both the transmission media and ground bounce along with the supply noise. Also, the closed-form expressions for the transmission lines developed in Chapter 3 are employed using lossy lumped π -model with σ -segments. EMPSIJ method for estimating power supply induced jitter is advanced to handle the combined effects of both ground bounce and transmission media and results are compared with HSPICE simulator. Validating examples demonstrate the accuracy and the speed-up achieved using the proposed method.

Chapter 5

Fast Jitter Estimation via Thomas Algorithm

In this chapter, an alternative and systematic way is proposed to estimate the power supply induced jitter (PSIJ) including the effects of transmission media, supply noise and ground bounce. The main advantage of the proposed approach is that it is generic in nature and the closed-form expressions that are derived for each of the noise sources need not to be re-derived for each case of noise source. The proposed approach is based on combining the Thomas Algorithm [40] with the EMPSIJ method [34]. Implementation of Thomas algorithm provides efficient solution for small-signal differential noise voltage by solving a tridiagonal matrix. Subsequently, EMPSIJ method is used to estimate the jitter. This approach provides for easy implementation at the expense of incremental CPU cost compared to the method in Chapter 4. Details of the proposed method are provided as follows.

The nodal-matrix representation and computationally efficient tridiagonal form for small-signal circuit analysis of voltage mode driver circuit are developed in sections 5.1 and 5.2, respectively. In section 5.3, the analysis is advanced to include the ground bounce. Next, solution based on Thomas algorithm is presented in section 5.4 for efficient solution of the resulting equations. In order to check the validity of the proposed algorithm, several examples with different noise sources are presented in section 5.5.

5.1 Nodal Matrix Representation

In Chapter 3, a closed-form expression for a transmission line with R, L, G and C p.u.l parameters was derived using lossy lumped- π model with σ number of segments. The closed-form recursive expression (3.19) for transmission line type interconnects can be expressed as:

$$y_1 v_i + [y_L C_{\sigma-1}] v_0 = [Y C_{\sigma-1} - y_1 C_{\sigma-2}] v_\sigma \quad (5.1)$$

where corresponding entities in (5.1) are defined in Section 3.4.

In Chapter 4, semi-analytical expressions were developed for small-signal differential voltage ($v_x - v_y$) across the external load resistor (R_L) (see Figure 5.1). The analysis was based on: finding the Thévenin equivalent voltage (v_{th}) and Thévenin equivalent impedance (Z_{th}) between the nodes v_q and v_e . The value of the small-signal differential voltage (using v_{th} , Z_{th} and (5.1)) was calculated at the midpoint of the rising edge, which in turn was used to estimate the power supply induced jitter (PSIJ). However, the implementation of this method may become tedious and any changes in the circuit or load conditions would require re-deriving these expressions. In order to overcome these difficulties, a systematic method based on MNA formulation and efficient solution method based on Thomas algorithm is presented in this chapter.

Using Figure 5.1 and nodal analysis at node v_p gives:

$$Y_p v_p = Y_1 v_n + Y_3 v_q + Y_5 v_e \quad (5.2)$$

where

$$Y_p = Y_1 + Y_2 + Y_3 + Y_5 \quad (5.3)$$

and

$$Y_1 = Z_1^{-1}; \quad Y_2 = Z_2^{-1}; \quad Y_3 = Z_3^{-1}; \quad Y_5 = Z_5^{-1} \quad (5.4)$$

The impedance parameters (Z_1 , Z_2 , Z_3 , Z_4 , Z_5 and Z_6) of Figure 5.1 are defined in (4.3)–(4.8). In order to obtain the expressions for nodes v_q and v_x , transmission lines of Figure 5.1 are replaced with the lossy lumped- π segments as illustrated in Figure 5.2.

Figure 5.1: Small-signal model of voltage mode driver

Nodal analysis at nodes v_q and v_x generates:

$$Y_q v_q = Y_3 v_p + y_1 v_1' \quad (5.5)$$

$$Y v_x = y_L v_y + y_1 v_1'' \quad (5.6)$$

where

$$Y_q = y_1 + y_2 + Y_3 + Y_4; \quad Y = y_1 + y_2 + y_L; \quad (5.7)$$

and

$$y_L = \frac{1}{R_L} \quad y_1 = \frac{1}{z_1}; \quad y_2 = \frac{1}{z_2} \quad (5.8)$$

where $z_1 = (R + j\omega L)/\sigma$ and $z_2 = (G + j\omega C)/2\sigma$

Next, closed-form expression for transmission line (5.1) is used to obtain the following set of equations,

$$y_1 v_q + [y_L C_{\sigma-1}] v_x = [Y C_{\sigma-1} - y_1 C_{\sigma-2}] v_y \quad (5.9)$$

$$y_1 v_1' + [y_L C_{\sigma-2}] v_x = [Y C_{\sigma-2} - y_1 C_{\sigma-3}] v_y \quad (5.10)$$

$$y_1 v_x + [Y_7 C_{\sigma-1}] v_p = [Y_e C_{\sigma-1} - y_1 C_{\sigma-2}] v_e \quad (5.11)$$

$$y_1 v_1'' + [Y_7 C_{\sigma-2}] v_p = [Y_e C_{\sigma-2} - y_1 C_{\sigma-3}] v_e \quad (5.12)$$

where

$$Y_7 = g_m + Y_6 \quad (5.13)$$

$$Y_e = g_m + y_1 + y_2 + Y_5 + Y_6 \quad (5.14)$$

Figure 5.2: Small-signal model with lossy lumped segmentations representing the TL

Let C_{x1} , C_{x2} , C_{p1} , C_{p2} , C_{y1} , C_{y2} , C_{e1} and C_{e2} be defined as:

$$C_{x1} = y_L C_{\sigma-1} \quad (5.15)$$

$$C_{x2} = y_L C_{\sigma-2} \quad (5.16)$$

$$C_{p1} = Y_7 C_{\sigma-1} \quad (5.17)$$

$$C_{p2} = Y_7 C_{\sigma-2} \quad (5.18)$$

$$C_{y1} = Y C_{\sigma-1} - y_1 C_{\sigma-2} \quad (5.19)$$

$$C_{y2} = Y C_{\sigma-2} - y_1 C_{\sigma-3} \quad (5.20)$$

$$C_{e1} = Y_e C_{\sigma-1} - y_1 C_{\sigma-2} \quad (5.21)$$

$$C_{e2} = Y_e C_{\sigma-2} - y_1 C_{\sigma-3} \quad (5.22)$$

Using (5.2)–(5.22), the nodal representation of Figures 5.1 and 5.2 can be expressed as:

$$\mathbf{Ax} = \mathbf{b} \Rightarrow \begin{bmatrix} Y_p & -Y_3 & 0 & 0 & 0 & 0 & -Y_5 \\ -Y_3 & Y_q & -y_1 & 0 & 0 & 0 & 0 \\ 0 & -y_1 & 0 & C_{y1} & -C_{x1} & 0 & 0 \\ 0 & 0 & -y_1 & C_{y2} & -C_{x2} & 0 & 0 \\ 0 & 0 & 0 & -y_L & Y & -y_1 & 0 \\ -C_{p1} & 0 & 0 & 0 & -y_1 & 0 & C_{e1} \\ -C_{p2} & 0 & 0 & 0 & 0 & -y_1 & C_{e2} \end{bmatrix} \begin{bmatrix} v_p \\ v_q \\ v'_1 \\ v_y \\ v_x \\ v''_1 \\ v_e \end{bmatrix} = \begin{bmatrix} Y_1 v_n \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (5.23)$$

Direct solution of (5.23) is obtained through the product of inverse of $\mathbf{A}$ and $\mathbf{b}$ ($\mathbf{x} = \mathbf{A}^{-1} \mathbf{b}$) or through LU decomposition of $\mathbf{A}$ and forward/backward substitutions. However, since the small-signal system illustrated in Figure 5.2, needs to be simulated over several thousands of bits, the total CPU time escalates if using this approach.

To address this difficulty, in the next section, nodal representation (5.23) is translated to a cyclic-tridiagonal [41] form so as to obtain an efficient solution using the Thomas algorithm [40].

5.2 Cyclic-Tridiagonal Matrix Representation for the Transmission Line with Load

An equivalent circuit of σ -lumped segments of a transmission line is shown in Figure 5.3 where z_L is the terminating output impedance.

Figure 5.3: Transmission line with σ -segments.

Also, z_1 and z_2 are defined in terms of R , L , G and C p.u.l parameters.

$$z_1 = \frac{R + j\omega L}{\sigma}; \quad z_2 = \frac{G + j\omega C}{2\sigma} \quad (5.24)$$

Using KCL at node (v_1) gives:

$$yv_1 = v_i + v_2 \quad (5.25)$$

where

$$y = 2 + \frac{2y_2}{y_1}; \quad y_1 = \frac{1}{z_1}; \quad y_2 = \frac{1}{z_2} \quad (5.26)$$

Next, consider first ten lumped- π segments ($\sigma = 10$) and the set of equations at the nodes v_1 to v_9 are given as:

$$yv_1 = v_i + v_2 \quad (5.27)$$

$$yv_2 = v_1 + v_3 \quad (5.28)$$

$$yv_3 = v_2 + v_4 \quad (5.29)$$

$$yv_4 = v_3 + v_5 \quad (5.30)$$

$$yv_5 = v_4 + v_6 \quad (5.31)$$

$$yv_6 = v_5 + v_7 \quad (5.32)$$

$$yv_7 = v_6 + v_8 \quad (5.33)$$

$$yv_8 = v_7 + v_9 \quad (5.34)$$

$$yv_9 = v_8 + v_{10} \quad (5.35)$$

Using (5.27)–(5.34) generates:

$$C_8 v_1 = C_7 v_i + v_9 \quad (5.36)$$

Similarly (5.28)–(5.35) leads to:

$$C_8 v_9 = v_1 + C_7 v_{10} \quad (5.37)$$

The coefficients C_7 and C_8 belong to 7th and 8th segments, respectively. They can be extracted from Table 3.2. Applying KCL at node (v_{10}) gives:

$$Y_L v_{10} = y_1 v_9 + y_L v_o \quad (5.38)$$

where

$$Y_L = y_1 + y_2 + y_L; \quad y_L = \frac{1}{z_L} \quad (5.39)$$

As the number of segments in the transmission line changes, the coefficients (C_7 , C_8) and voltages (v_9 , v_{10}) also change. Hence, C_7 , C_8 , v_9 and v_{10} can be generalised to $C_{\sigma-3}$ and $C_{\sigma-2}$, $v_{\sigma-1}$ and v_σ , respectively. Equations (5.36)–(5.38) can be re-written as:

$$C_{\sigma-2} v_1 = C_{\sigma-3} v_i + v_{\sigma-1} \quad (5.40)$$

$$C_{\sigma-2} v_{\sigma-1} = v_1 + C_{\sigma-3} v_\sigma \quad (5.41)$$

$$Y_L v_\sigma = y_1 v_{\sigma-1} + y_L v_o \quad (5.42)$$

The diagonally dominant representation of (5.23) can be obtained by using the symmetric transmission line equations (5.40)–(5.42).

$$\underbrace{\begin{bmatrix} Y_p & -Y_3 & 0 & 0 & 0 & 0 & 0 & 0 & -Y_5 \\ -Y_3 & Y_q & -y_1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -C_{\sigma-3} & C_{\sigma-2} & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & C_{\sigma-2} & -C_{\sigma-3} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -y_1 & Y_L & -y_L & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -y_L & Y_L & -y_1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -C_{\sigma-3} & C_{\sigma-2} & -1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -1 & C_{\sigma-2} & -C_{\sigma-3} \\ -Y_7 & 0 & 0 & 0 & 0 & 0 & 0 & -y_1 & Y_e \end{bmatrix}}_{\mathbf{T}} \underbrace{\begin{bmatrix} v_p \\ v_q \\ v_1' \\ v_{\sigma-1}' \\ v_y \\ v_x \\ v_1'' \\ v_{\sigma-1}'' \\ v_e \end{bmatrix}}_{\mathbf{v}} = \underbrace{\begin{bmatrix} Y_1 v_n \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}}_{\mathbf{b}} \quad (5.43)$$

The matrix $\mathbf{T}$ is the coefficient matrix, $\mathbf{v}$ is the vector of node voltages and $\mathbf{b}$ is the source vector. Also, v_1' and $v_{\sigma-1}'$ are the first and ' $\sigma - 1$ ' node voltages of TL1, respectively. Similarly, double prime quotation ($''$) is associated with second line (TL2). The matrix $\mathbf{T}$ is not a perfect tridiagonal matrix due to Y_5 and Y_7 elements but the solutions of (5.43) can still be obtained using Thomas algorithm.

5.3 Cyclic-Tridiagonal Representation in the Presence of both Supply Noise and Ground Bounce

The small-signal circuit of a voltage mode divider with lossy lumped- π segments shown in Figure 5.2 is added with a ground bounce voltage (v_g) as shown in Figure 5.4. The analysis presented in the previous section is advanced to include the ground bounce. Since ground bounce voltage is a source, it will have no impact on the coefficient matrix ($\mathbf{T}$) and the unknown voltage vector ($\mathbf{v}$). It will only alter the source vector ($\mathbf{b}$).

Referring to Figure 5.4 (in the presence of both v_n and v_g), (5.2), (5.5), (5.40) and (5.41) can be re-written as:

$$Y_p v_p = Y_1 v_n + Y_3 v_q + Y_5 v_e + Y_2 v_g \quad (5.44)$$

$$Y_q v_q = Y_3 v_p + y_1 v_1' + v_{g1} v_g \quad (5.45)$$

$$C_{\sigma-2} v_1' = C_{\sigma-3} v_q + v_{\sigma-1}' + y_g \sum_{i=1}^{\sigma-3} C_i v_g \quad (5.46)$$

$$C_{\sigma-2} v_{\sigma-1}' = v_1' + C_{\sigma-3} v_y + y_g \sum_{i=1}^{\sigma-3} C_i v_g \quad (5.47)$$

Using KCL at nodes (v_y) and (v_x) yields:

$$Y_L v_y = y_1 v_{\sigma-1}' + y_L v_x + y_2 v_g \quad (5.48)$$

$$Y_L v_x = y_1 v_1'' + y_L v_y + y_2 v_g \quad (5.49)$$

Similar to (5.46) and (5.47), the general expressions of TL2 in the presence of v_g can be expressed as:

$$C_{\sigma-2} v_1'' = C_{\sigma-3} v_x + v_{\sigma-1}'' + y_g \sum_{i=1}^{\sigma-3} C_i v_g \quad (5.50)$$

$$C_{\sigma-2} v_{\sigma-1}'' = v_1'' + C_{\sigma-3} v_e + y_g \sum_{i=1}^{\sigma-3} C_i v_g \quad (5.51)$$

Figure 5.4: Small-signal model with ground bounce noise

Using nodal analysis at node (v_e) leads to:

$$Y_e v_e = Y_7 v_p + y_1 v_{\sigma-1}'' + y_{g2} v_g \quad (5.52)$$

Next, y_{g1} , y_{g2} and y_g are evaluated as:

$$y_g = 2 \left(\frac{y_2}{y_1} \right); \quad y_{g1} = y_2 + Y_3; \quad y_{g2} = y_2 + Y_4 \quad (5.53)$$

It can be recognised from (5.44)–(5.52) that the coefficients associated with nodes of the small-signal circuit (Figure 5.2) are same as formulated in coefficient matrix $(\mathbf{T})$ in (5.43). The only extra term added is the ground bounce voltage (v_g) with a corresponding coefficient. Hence, the tridiagonal representation of the small-signal voltage mode driver system with combined effects of supply noise (v_n) , ground bounce voltage (v_g) and transmission media is proposed in (5.54).

$$\mathbf{T} \cdot \mathbf{v} = \mathbf{b1} \cdot v_n + \mathbf{b2} \cdot v_g \quad (5.54)$$

Or

$$\begin{bmatrix} Y_p & -Y_3 & 0 & 0 & 0 & 0 & 0 & 0 & -Y_5 \\ -Y_3 & Y_q & -y_1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -C_{\sigma-3} & C_{\sigma-2} & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & C_{\sigma-2} & -C_{\sigma-3} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -y_1 & Y_L & -y_L & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -y_L & Y_L & -y_1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -C_{\sigma-3} & C_{\sigma-2} & -1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -1 & C_{\sigma-2} & -C_{\sigma-3} \\ -Y_7 & 0 & 0 & 0 & 0 & 0 & 0 & -y_1 & Y_e \end{bmatrix} \begin{bmatrix} v_p \\ v_q \\ v_1' \\ v_{\sigma-1}' \\ v_y \\ v_x \\ v_1'' \\ v_{\sigma-1}'' \\ v_e \end{bmatrix}$$

$$= \begin{bmatrix} Y_1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} v_n + \begin{bmatrix} Y_2 \\ y_{g1} \\ y_g \sum_{i=1}^{\sigma-3} C_i \\ y_g \sum_{i=1}^{\sigma-3} C_i \\ y_2 \\ y_2 \\ y_g \sum_{i=1}^{\sigma-3} C_i \\ y_g \sum_{i=1}^{\sigma-3} C_i \\ y_{g2} \end{bmatrix} v_g = \begin{bmatrix} d_1 \\ d_2 \\ d_3 \\ d_4 \\ d_5 \\ d_6 \\ d_7 \\ d_8 \\ d_9 \end{bmatrix} \quad (5.55)$$

The coefficient matrix (**T**) expressed in (5.55) is a diagonally dominant cyclic matrix. In the presence of the corner elements (Y_5 and Y_7), Thomas algorithm cannot be implemented directly. Further algorithmic enhancements are proposed for efficient solution of the system in (5.55) in the next section.

5.4 Solution based on Thomas Algorithm

Thomas algorithm is simplified form of Gaussian elimination that can be used to solve tridiagonal systems of equations. A tridiagonal system for (k) unknowns is given in (5.56).

$$\begin{bmatrix} b_1 & c_1 & 0 & 0 & \cdots & 0 \\ a_2 & b_2 & c_2 & 0 & \cdots & 0 \\ 0 & a_3 & b_3 & c_3 & \cdots & 0 \\ 0 & 0 & \ddots & \ddots & \ddots & 0 \\ \vdots & \vdots & 0 & a_{k-1} & b_{k-1} & c_{k-1} \\ 0 & 0 & 0 & 0 & a_k & b_k \end{bmatrix} \begin{bmatrix} f_1 \\ f_2 \\ \vdots \\ \vdots \\ f_{k-1} \\ f_k \end{bmatrix} = \begin{bmatrix} d_1 \\ d_2 \\ \vdots \\ \vdots \\ d_{k-1} \\ d_k \end{bmatrix} \quad (5.56)$$

where a_k , b_k and c_k are the coefficients of unknown vector f_k . The right-hand vector (d_k) usually represents the sources in the system. Since Thomas algorithm performs Gaussian elimination, the solution of f_k can be obtained by backward substitution:

$$f_k = d_k^* \quad (5.57)$$

$$f_i = d_i^* - f_{i+1} c_i^* \quad (5.58)$$

Coefficients c_i^* and d_i^* are calculated from forward sweeping:

$$c_i^* = \begin{cases} \frac{c_i}{b_i} & i = 1 \\ \frac{c_i}{b_i - a_i c_{i-1}^*} & i = 2, 3 \dots k-1 \end{cases} \quad (5.59)$$

and

$$d_i^* = \begin{cases} \frac{d_i}{b_i} & i = 1 \\ \frac{d_i - a_i d_{i-1}^*}{b_i - a_i c_{i-1}^*} & i = 2, 3 \dots k-1 \end{cases} \quad (5.60)$$

Next, Thomas algorithm is implemented to obtain the solution for unknown nodes voltages ($\mathbf{v}$) in (5.55). The tridiagonal coefficient matrix ($\mathbf{T}$) is written in terms of a_i , b_i and c_i where $i = 1, 2 \dots 9$. In addition, vectors ($\mathbf{v}$) and ($\mathbf{b}$) are defined as f_i and d_i , respectively. These changes are made so as to be consistent with equation (5.56). Hence, (5.55) can be rewritten as:

$$\left[\begin{array}{c|cccccccc} b_1 & c_1 & 0 & 0 & 0 & 0 & 0 & 0 & a_1 \\ \hline a_2 & b_2 & c_2 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & a_3 & b_3 & c_3 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & a_4 & b_4 & c_4 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & a_5 & b_5 & c_5 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & a_6 & b_6 & c_6 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & a_7 & b_7 & c_7 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & a_8 & b_8 & c_8 \\ c_9 & 0 & 0 & 0 & 0 & 0 & 0 & a_9 & b_9 \end{array} \right] \left[\begin{array}{c} f_1 \\ f_2 \\ f_3 \\ f_4 \\ f_5 \\ f_6 \\ f_7 \\ f_8 \\ f_9 \end{array} \right] = \left[\begin{array}{c} d_1 \\ d_2 \\ d_3 \\ d_4 \\ d_5 \\ d_6 \\ d_7 \\ d_8 \\ d_9 \end{array} \right] \quad (5.61)$$

Since Thomas algorithm cannot be used directly due to the presence of a_1 and c_9 , the lower right 8×8 square matrix is extracted from (5.61) to implement the algorithm and it can be further decomposed into systems ($\mathbf{A}$ and $\mathbf{B}$).

$$\text{System A:} \quad \begin{bmatrix} b_2 & c_2 & 0 & 0 & 0 & 0 & 0 & 0 \\ a_3 & b_3 & c_3 & 0 & 0 & 0 & 0 & 0 \\ 0 & a_4 & b_4 & c_4 & 0 & 0 & 0 & 0 \\ 0 & 0 & a_5 & b_5 & c_5 & 0 & 0 & 0 \\ 0 & 0 & 0 & a_6 & b_6 & c_6 & 0 & 0 \\ 0 & 0 & 0 & 0 & a_7 & b_7 & c_7 & 0 \\ 0 & 0 & 0 & 0 & 0 & a_8 & b_8 & c_8 \\ 0 & 0 & 0 & 0 & 0 & 0 & a_9 & b_9 \end{bmatrix} \begin{bmatrix} f_{2,a} \\ f_{3,a} \\ f_{4,a} \\ f_{5,a} \\ f_{6,a} \\ f_{7,a} \\ f_{8,a} \\ f_{9,a} \end{bmatrix} = \begin{bmatrix} d_2 \\ d_3 \\ d_4 \\ d_5 \\ d_6 \\ d_7 \\ d_8 \\ d_9 \end{bmatrix} \quad (5.62)$$

and

$$\text{System B:} \quad \begin{bmatrix} b_2 & c_2 & 0 & 0 & 0 & 0 & 0 & 0 \\ a_3 & b_3 & c_3 & 0 & 0 & 0 & 0 & 0 \\ 0 & a_4 & b_4 & c_4 & 0 & 0 & 0 & 0 \\ 0 & 0 & a_5 & b_5 & c_5 & 0 & 0 & 0 \\ 0 & 0 & 0 & a_6 & b_6 & c_6 & 0 & 0 \\ 0 & 0 & 0 & 0 & a_7 & b_7 & c_7 & 0 \\ 0 & 0 & 0 & 0 & 0 & a_8 & b_8 & c_8 \\ 0 & 0 & 0 & 0 & 0 & 0 & a_9 & b_9 \end{bmatrix} \begin{bmatrix} f_{2,b} \\ f_{3,b} \\ f_{4,b} \\ f_{5,b} \\ f_{6,b} \\ f_{7,b} \\ f_{8,b} \\ f_{9,b} \end{bmatrix} = \begin{bmatrix} -a_2 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ -c_9 \end{bmatrix} \quad (5.63)$$

Thomas algorithm can be used to obtain the solutions of both systems in (5.62) and (5.63). These analytical solutions are provided by a series of recursive expressions as described in (5.57)–(5.60). Also, the solution of (5.61) can be obtained as a linear combination of the solutions obtained from system **A** and **B**. The small-signal differential output voltage is associated with elements $f_5 (v_y)$ and $f_6 (v_x)$. Therefore, the output differential voltage is formulated as:

$$v_x - v_y = f_6 - f_5 \quad (5.64)$$

where

$$f_5 = v_y = f_{5,a} + f_1 f_{5,b} \quad (5.65)$$

and

$$f_6 = v_x = f_{6,a} + f_1 f_{6,b} \quad (5.66)$$

Also, f_1 that corresponds to voltage v_p is calculated as:

$$f_1 = v_p = \frac{d_1 - a_1 f_{9,a} - c_1 f_{2,a}}{b_1 + a_1 f_{9,b} + c_1 f_{2,b}} \quad (5.67)$$

Using (5.64)–(5.67), the small-signal differential voltage (of Figure 5.3) can be obtained with combined impact of transmission media and ground bounce noise. In the next section, the value of the differential voltage is calculated using (5.64)–(5.67) which in turn can be used to estimate power supply induced jitter as described in Section 4.4.

5.5 Examples

In this section, the examples presented in Chapter 4 are considered for accuracy and efficiency comparison purposes. The results of PSIJ estimation using both the ‘*Proposed Approach-1*’ (presented in Chapter 4) and ‘*Proposed Approach-2*’ (Thomas algorithm) are compared with HSPICE.

5.5.1 Example-1

In this example, Figure 5.2 is used to demonstrate the validity of the proposed method. The cross-sectional diagram of a 15mm-long PCB traces is shown in Figure 3.6. A lossless microstrip line with 1.276 mm wide (w) conducting strip over a 0.635 mm thick (h) substrate with a relative permittivity of ($\epsilon_r = 9.8$) is considered. The LC parameters of the line are extracted using W-element in HSPICE. The power supply noise is in the form of a square wave of frequency 446.4 MHz which is superimposed on power supply (V_{DD}). A peak-to-peak amplitude of the supply noise is varied from 0 to $V_{DD}/15$ and corresponding PSIJ is evaluated using *Approach-1* and *Approach-2* to observe the impact of noise on PSIJ. Figure 5.5 shows the comparison among the results obtained from all three approaches.

As seen from the plots in Figure 5.5, all three approaches match well, validating the accuracy of the proposed method. Table 5.1 compares the CPU time taken by all the three approaches. *Approach-1* and *Approach-2* yield a significant speed-up compared to HSPICE.

Figure 5.5: Comparison of PSIJ for square wave noise input

Table 5.1: CPU time comparison for PSIJ

Number of simulated bits	HSPICE	Approach-1 (Chapter 4)	Approach-2 (MNA + Thomas Algorithm)
10,000 bits	65.1 sec	1.17 sec	5.4 sec
100,000 bits	594 sec	3.79 sec	15.6 sec

5.5.2 Example-2

In this example, impact of both lossy transmission line (with 30 segments) and ground bounce ($v_g = 10\text{ mV}$) is investigated. For this purpose, small signal model with ground bounce noise shown in Figure 5.4 is used to estimate PSIJ. PDN noise in the form of a saw-tooth wave and 250 dominant frequencies are used for reconstruction of the saw-tooth noise waveform. The PCB trace considered is 15 mm long, 2.745 mm wide and $18\mu\text{m}$ thick. The relative permittivity and thickness of the substrate are 2.5 and 0.625 mm, respectively. Cross-section of the PCB trace can be seen in Figure 3.6. The noise peak-to-peak amplitude is considered to be varying from 0 to $V_{DD}/10$ and plots of all three approaches of corresponding PSIJ is shown in Figure 5.6 which match reasonably accurately. Table 5.2 compares the CPU time taken by the HSPICE, *Approach-1* and *Approach-2* which indicates the speed-up of over 155 and 40 compared to HSPICE, respectively.

Figure 5.6: Comparison of PSIJ for saw-tooth noise input including ground bounce

Table 5.2: CPU time comparison for PSIJ

Number of simulated bits	HSPICE	Approach-1 (Chapter 4)	Approach-2 (MNA+Thomas Algorithm)
10,000 bits	91.0 sec	1.95 sec	9.75 sec
100,000 bits	655 sec	4.25 sec	19.19 sec

5.6 Summary

An alternative approach is presented in this chapter based on MNA tridiagonal formulation and application of Thomas algorithm for a systematic and easy implementation for computing PSIJ with incremental CPU cost while avoiding re-derivation of the expressions for any change in load conditions. The closed-form expression (3.19) for transmission line developed in Chapter 3 is re-derived so that the tridiagonal formulation remains valid. Solution obtained from the Thomas algorithm is used to estimate PSIJ and compared with closed-form semi-analytical approach (Chapter 4) and HSPICE. Validating examples demonstrate the accuracy and significant speed-up achieved by the proposed method.

Chapter 6

Conclusions and Future Work

EMPSIJ method for estimating power supply induced jitter is advanced to handle the combined effects of supply noise, transmission media and ground bounce. Semi-analytical expressions are developed for this purpose using small-signal model of VMD circuit. Also, an alternative and systematic approach for PSIJ analysis based on MNA tridiagonal formulation and Thomas Algorithm is presented. Both of the approaches are validated using various examples in the presence of different types of noise sources. The results of PSIJ estimation using both approaches are compared with the HSPICE simulator validating the accuracy of the proposed model. The proposed method performs computationally superior compared to the existing methods.

Several future works are possible based on the contributions in this thesis:

1. Development of a new transmission line model which would not require recursive calculations as needed in (3.19).
2. Inclusion of data noise in the analysis.
3. Extension of the proposed work to other types of circuits such as current mode drivers.
4. A system level PSIJ analysis using the proposed approach involving various PDN modules.

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Appendix A

Implementation Details for Estimation of Power Supply Induced Jitter

In this appendix, implementation details for the proposed approaches for estimation of power supply induced jitter (PSIJ) are presented. Algorithm-1 (page 52) is used for this purpose, which is based on EMPSIJ method (described in Chapter 4). The corresponding steps for PSIJ estimation using Algorithm-1 are briefly described in the next sections.

A.1 Calculating Midpoint and Slope

In this section, midpoint (t_{m_o}) and the slope (α) of the rising edge for the differential output response ($v_R(t)$) across DP/DN terminals (see Figure 4.1) are obtained in the absence of supply noise (v_n). The midpoint and the slope of the rising edge can be extracted using one-bit HSPICE simulation. As can be seen in an illustrative Figure A.1, t_{m_o} is 690 ps and slope at that point can be calculated as:

$$\alpha = \frac{[34 - (-26.7)]m}{[746 - 664]p} = 7.40 \times 10^8 \text{ V.s}^{-1} \quad (\text{A.1})$$

Calculating slope based on just two points may not be accurate since the differential output voltage response of the rising is not perfectly linear. Therefore, multiple data points are extracted from the rising edge response and a built-in MATLAB `polyfit(x,y,r)` function [42] of order $r = 1$ is used to find an accurate slope and the y-intercept where

the parameters $\mathbf{x}$ and $\mathbf{y}$ are the extracted time and voltage vectors, respectively. The expression for $v_R(t)$ based on extracted data points is given as:

$$v_R(t) = (7.5891 \times 10^8).t - 0.5268 \quad (\text{A.2})$$

Figure A.1: One-bit simulation using HSPICE ($v_n = 0$)

Figure A.2: Responses of the equation (A.2) and differential output using HSPICE

Figure A.2 shows that equation (A.2) matches reasonably well with the rising edge of the Figure A.1. Hence, $\alpha = 7.5891 \times 10^8$ is used to estimate the power supply induced jitter.

A.2 Noise Sources

In this section, various noise sources (v_n) such as sine, sawtooth and square waves are considered and the corresponding Fourier series [43] are given as:

$$v_n(t) = A \sin(2\pi n f_o t) \quad (\text{A.3})$$

$$v_n(t) = \sum_{n=1}^{\infty} (-1)^{n+1} \frac{2A}{n\pi} \sin(2\pi n f_o t) \quad (\text{A.4})$$

$$v_n(t) = \sum_{n=1,3,\dots}^{\infty} \frac{4A}{n\pi} \sin(2\pi n f_o t) \quad (\text{A.5})$$

The sine wave is generated using single Fourier coefficient. On the other hand, sawtooth and square waves are generated using 35-coefficients. The period and peak-to-peak amplitude are 2 ns and 0.1V, respectively. The PDN noises with corresponding Fourier coefficients are shown in Figures A.3, A.4 and A.5.

(a) Sine wave noise

(b) Frequency-domain amplitude spectrum

Figure A.3: Sine wave noise and its frequency-domain amplitude spectrum

(a) Saw-tooth wave noise

(b) Frequency-domain amplitude spectrum

Figure A.4: Saw-tooth wave noise and its frequency-domain amplitude spectrum

(a) Square wave noise

(b) Frequency-domain amplitude spectrum

Figure A.5: Square wave noise and its frequency-domain amplitude spectrum

A.3 Transfer Function

This section focuses on simulating the transfer functions of the proposed approaches as described in Chapter 4 and Chapter 5. For this purpose, small signal circuits of voltage mode driver shown in Figure 4.12 and Figure 5.4 are considered. Both of the approaches are simulated in MATLAB.

The parameters associated with the MOSFETs and transmission media are extracted using HSPICE simulator. In this thesis, RLGC parameters of lossless and lossy microstrip lines presented in Section 3.5 are used to calculate the transfer functions and PSIJ. The small signal parameters associated with MOSFETs M2, M3 and PMOS of the inverter (Figure 4.1) are provided in Table A.1.

Table A.1: Small signal parameters of the MOSFETS

M2		M3		PMOS	
Saturation		Linear		Linear	
C_{gs}	1.6165 fF	C_{gs}	1.3835 fF	C_{gs}	— — —
C_{ds}	693.58 aF	C_{ds}	1.1132 fF	C_{ds}	2.2411 fF
C_{gd}	688.4 aF	C_{gd}	1.0596 fF	C_{gd}	— — —
g_{m2}	566.12 mS	R_{on3}	1.2125 k Ω	R_{onp}	824.5 Ω

The transfer functions obtained using the proposed approaches for lossless and lossy microstrip lines with 10-segments are given in Figure A.6 and A.7, respectively. For comparison, transfer functions for lossless and lossy microstrip lines are also simulated in HSPICE simulator. As can be seen, the proposed approaches match accurately with the HSPICE results.

A.3.1 MATLAB Code

In order to simulate the transfer functions obtained using the proposed approaches, several MATLAB functions are developed. The function **TL_admittances** takes the small signal parameters from **circuit_parameters()** and calculates the equivalent impedances. Next, the differential output response is evaluated by **Thomas_Algorithm**

Figure A.6: Comparison of transfer functions for lossless line with $v_n = 1V$ and $v_g = 0$

Figure A.7: Comparison of transfer functions for lossy line with $v_n = 1V$ and $v_g = 0.1V$

and the transfer functions can be obtained using `tf_th` and `tf_analytical`. A test function (`test_tf`) generates and compare the output responses including HSPICE results.

```

1  function test_tf()
2  clc; clear all; close all;
3  len = 15e-3; sigma = 10; % ---- TL length and # of segments
4  RLGC = [0; 295.43e-9; 0 ; (266.04e-12)/2]*len/sigma; % LOSSLESS
5
6  % Comment the above line and uncomment the below line for lossy
   T-Line
7  % and change tf_spice_lossless to tf_spice_lossy in the plots
8
9  %RLGC = [5.27; 149.83e-9; 0.5e-3 ; (328.62e-12)/2]*len/sigma; %
   LOSSY
10 vn = 1; vg = 0;
11 v_ac = [vn;vg;sigma]; % [vn vg sigma]
12 f_min = 1; f_max = 4e9; % Frequency range
13 f = linspace(f_min,f_max,100);
14 TF_ch5 = tf_th(f,v_ac,RLGC); % Chapter 5
15
16 %% HSPICE DATA
17 f_spice = [0.1212 0.3232 0.5253 0.7273 0.9293 ...
18           1.1313 1.3333 1.5354 1.7374 1.9394 ...
19           2.1414 2.3434 2.5455 2.7475 2.9495 ...
20           3.1515 3.3535 3.5556 3.7576 3.9596]*1e9;
21 % vn = 1, vg=0, TL = Lossless line
22 tf_spice_lossless = [0.1421 0.3282 0.4622 0.5696 0.6770 ...
23                    0.8042 0.9657 1.1612 1.3377 1.3718 ...
24                    1.2301 1.0301 0.8543 0.7159 0.6030 ...
25                    0.4977 0.3760 0.2092 0.0408 0.2349];
26 % vn = 1, vg=0.1, TL = Lossy line
27 tf_spice_lossy = [0.1522 0.3210 0.4124 0.4741 ...
28                 0.5319 0.5990 0.6860 0.8061 ...
29                 0.9778 1.2243 1.5388 1.7520 ...
30                 1.6146 1.2985 1.0296 0.8402 ...

```



```

31             0.7085  0.6141  0.5426  0.4831];
32 TF_ch4 = tf_th(f,v_ac,RLGC); % Chapter 4
33 %% PLOTS
34 figure(1);
35 plot(f*1e-9,abs(TF_ch4),f*1e-9,abs(TF_ch5),'—','Linewidth',2)
36 grid on
37 ylabel('|H(f)| (V/V)','FontSize',12,'FontWeight','bold','Color',
        'k')
38 legend({'Chapter4 – Explicitly derived analytical relation','
        Thomas Algorithm'},'Location','best')
39 xlabel('Frequency (GHz)','FontSize',12,'FontWeight','bold','
        Color','k')
40 set(gcf,'color','w');
41 set(gca,'fontsize',13);
42 figure(2);
43 plot(f*1e-9,abs(TF_ch4),f*1e-9,abs(TF_ch5),'—',f_spice*1e-9,abs
        (tf_spice_lossless),'dg','Linewidth',2)
44 grid on
45 ylabel('|H(f)| (V/V)','FontSize',12,'FontWeight','bold','Color',
        'k')
46 legend({'Chapter4 – Explicitly derived analytical relation','
        Thomas Algorithm','HSPICE'},'Location','best')
47 xlabel('Frequency (GHz)','FontSize',12,'FontWeight','bold','
        Color','k')
48 set(gcf,'color','w');
49 set(gca,'fontsize',13);
50 function vtf = tf_th(freq,v_ac,RLGC)
51
52 [Ron_p,Cds_p,Cgd_2,Cgs_3,Cgd_3,Ron_3,Cds_3, ...
53      Cgs_2,ro2,Cds_2,gm] = circuit_parameters
54      ();

```

```

55  vn = v_ac(1);
56  vg = v_ac(2);
57  sec = v_ac(3);
58  R1 = RLGC(1);
59  L1 = RLGC(2);
60  G1 = RLGC(3);
61  C1 = RLGC(4);
62
63  yL=1/100;
64  ff = freq;
65  for n=1:length(ff)
66      [Y1,Y2,Y3,Y4,Y5,Y6] = TL_admittances(Ron_p,Cds_p,Cgd_2,Cgs_3,
        Cgd_3, ...
67          Ron_3,Cds_3,Cgs_2,ro2,Cds_2,ff(n));
68          %vout1
69      [vout(n),vv(n)] = Thomas_Algorithm(Y1,Y2,Y3,Y4,Y5,Y6,C1,L1,
        yL, ...
70          ff(n),vn,vg,gm,sec);
71  end
72  vtf = abs(vv);
73  end
74
75  function [Ron_p,Cds_p,Cgd_2,Cgs_3,Cgd_3,Ron_3,Cds_3, ...
76          Cgs_2,ro2,Cds_2,gm] = circuit_parameters
        ()
77
78  Ron_p = 1/1.2128e-3;
79  Cds_p = 2.2411e-15;
80  Cgd_2 = 688.4645E-18;
81  Cgs_3 = 1.3835e-15;
82  Cgd_3 = 1.0596e-15;
83  Ron_3 = 1/824.7598e-6;

```

```

84  Cds_3 = 1.1132e-15;
85  Cgs_2 = 1.6165e-15;
86  Cds_2 = 693.5817e-18;
87  gm = 566.1292e-3;
88  ro2 = 1*(1/gm);
89
90  end
91  function [Y1,Y2,Y3,Y4,Y5,Y6] = TL_admitances(Ron_p,Cds_p,...
92      Cgd_2,Cgs_3,Cgd_3,Ron_3,Cds_3,Cgs_2,ro2,
93      Cds_2,f)
94
95  s = 1i*2*pi*f;
96
97  Y1 = (1+s*Ron_p*Cds_p)/Ron_p;
98  Y2 = s*(Cgd_2+Cgs_3);
99  Y3 = s*Cgd_3;
100 Y4 = (1+s*Ron_3*Cds_3)/Ron_3;
101 Y5 = s*Cgs_2;
102 Y6 = (1+s*ro2*Cds_2)/ro2;
103
104 end
105
106 function [vout,vout1] = Thomas_Algorithm(Y1,Y2,Ya,...
107     Y3,Yc,Y4,C1,L1,yL,f,vn,vg,gm
108     ,sec)
109
110 s = 1i*2*pi;
111 y1 = (1/(s*L1*f));
112 y2 = (s*C1*f)/1;
113 Y = y1+y2+yL;
114 yg = (2*y2)/(1*y1);
115 y = 2+yg;
116 yg1 = y2+Ya;
117 yg2 = y2+Y3;

```

```

114 C_9 = y; % 1
115 C_8 = y^2 - 1; % 2
116 C_7 = y^3 - 2*y; % 3
117 C_6 = y^4 - 3*y^2 + 1; % 4
118 C_5 = y^5 - 4*y^3 + 3*y; % 5
119 C_4 = y^6 - 5*y^4 + 6*y^2 - 1; % 6
120 C_3 = y^7 - 6*y^5 + 10*y^3 - 4*y; % 7
121 C_2 = y^8 - 7*y^6 + 15*y^4 - 10*y^2 + 1; % 8
122 Yb = Y1+Y2+Ya+Yc;
123 Yd = y1+y2+Y3+Ya;
124 Ye = y1+y2+Y4+Yc+gm;
125 Yf = Yc+gm; % changed yc to y4
126
127 C_vg = C_9+C_8+C_7+C_6+C_5+C_4+C_3;
128
129 a2 = -Ya; b1 = Yb; c1 = -Ya;
130 a3 = -C_3; b2 = Yd; c2 = -y1;
131 a4 = -1; b3 = C_2; c3 = -1;
132 a5 = -y1; b4 = C_2; c4 = -C_3;
133 a6 = -yL; b5 = Y; c5 = -yL;
134 a7 = -C_3; b6 = Y; c6 = -y1;
135 a8 = -1; b7 = C_2; c7 = -1;
136 a9 = -y1; b8 = C_2; c8 = -C_3;
137 a1 = -Yc; b9 = Ye; c9 = -Yf;
138
139 bb = [a3;a4;a5;a6;a7;a8;a9];
140 aa = [b2;b3;b4;b5;b6;b7;b8;b9]; % b in thesis
141 cc = [c2;c3;c4;c5;c6;c7;c8];
142 dv1 = (vn*Y1)+(vg*Y2); dv2 = vg*(y2+Y3); dv3 = yg*C_vg*vg;
143 dv4 = vg*yg*C_vg;
144 dv5 = vg*y2; dv6 = vg*y2; dv7 = vg*yg*C_vg; dv8 = vg*yg*C_vg;
145 dv9 = vg*(y2+Y4);

```

```

146
147   f1 = [dv2;dv3;dv4;dv5;dv6;dv7;dv8;dv9];
148
149   n1 = length(f1);
150   v1 = zeros(n1,1);
151   y1 = v1;
152   w1 = aa(1);
153   y1(1) = f1(1)/w1;
154
155   d2 = -a2;
156   d9 = -c9;
157   f2 = [d2;0;0;0;0;0;0;0;d9];
158   n2 = length(f2);
159   v2 = zeros(n2,1);
160   y2 = v2;
161   w2 = aa(1);
162   y2(1) = f2(1)/w2;
163
164   for ii=2:n1
165       % The code in this loop is taken from [44]
166       v1(ii-1) = cc(ii-1)/w1;
167       w1 = aa(ii) - bb(ii-1)*v1(ii-1);
168       y1(ii) = ( f1(ii) - bb(ii-1)*y1(ii-1) )/w1;
169
170       v2(ii-1) = cc(ii-1)/w2;
171       w2 = aa(ii) - bb(ii-1)*v2(ii-1);
172       y2(ii) = ( f2(ii) - bb(ii-1)*y2(ii-1) )/w2;
173   end
174   for j=n1-1:-1:1
175       y1(j) = y1(j) - v1(j)*y1(j+1);
176   end
177

```

```

178     d2 = -a2;
179     d9 = -c9;
180     f2 = [d2;0;0;0;0;0;0;0;d9];
181     n2 = length(f2);
182     v2 = zeros(n2,1);
183     y2 = v2;
184     w2 = aa(1);
185     y2(1) = f2(1)/w2;
186     for ii=2:n2
187         v2(ii-1) = cc(ii-1)/w2;
188         w2 = aa(ii) - bb(ii-1)*v2(ii-1);
189         y2(ii) = ( f2(ii) - bb(ii-1)*y2(ii-1) )/w2;
190     end
191     for j=n2-1:-1:1
192         y2(j) = y2(j) - v2(j)*y2(j+1);
193     end
194     ff = (dv1 - a1*y1(8) - c1*y1(1))/(b1 + a1*y2(8) + c1*y2(1));
195     xx = (y1 + ff*y2)';
196     vout = abs(xx(5)-xx(4))/vn;
197     vout1 = vout;
198     end
199     %[44] Mathworks.com, 'Tridiag.m, Tridiagonal matrix equation
        solver (Thomas algorithm)', 2020.
200     %[Online]. Available: https://www.mathworks.com/matlabcentral/
        fileexchange/40722-tridiag-m
201     %[Accessed: 13- May- 2020]
202     end

```

Appendix B

HSPICE Measurements

In this appendix, estimated power supply included jitter obtained from HSPICE simulator is presented using voltage mode driver circuit, shown in Figure 4.1. In Figure B.1, the behavior of differential voltage ($v_r(t)$ green line) across DP/DN terminals is measured in the presence of supply noise (square waveform yellow line). Also, the output of the voltage regulator V_{sup} and PBRs data signal operating at 167 MHz are indicated in blue and red plots, respectively. Note that, V_{sup} is adequately constant as expected. Similarly, the responses for sawtooth noise waveform are illustrated in Figure B.2

Figure B.1: Signal measurements for voltage mode driver circuit with square noise waveform

Figure B.2: Signal measurements for voltage mode driver circuit with sawtooth noise waveform

Next, several PSIJ measurements based on the eye-pattern for various peak-to-peak noise amplitudes are presented. A jitter measurement tool accurately locks the reference level and produces jitter histogram with corresponding mean, standard deviation and jitter values. Figures (B.3) to (B5) and Figures (B.6) to (B8) calculate the jitter for square and sawtooth noises, respectively. For accurate jitter estimation, the output response is simulated over several hundreds of bits.

Figure B.3: Jitter measurement for $0.05 V_{p-p}$ (square waveform)

Figure B.4: Jitter measurement for $0.1 V_{p-p}$ (square waveform)

Figure B.5: Jitter measurement for $0.2 V_{p-p}$ (square waveform)

Figure B.6: Jitter measurement for $0.05 V_{p-p}$ (*saw-tooth waveform*)

Figure B.7: Jitter measurement for $0.1 V_{p-p}$ (*saw-tooth waveform*)

Figure B.8: Jitter measurement for $0.2 V_{p-p}$ (*saw-tooth waveform*)