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ECHO CANCELLATION USING SAMPLED
ANALOG SIGNAL PROCESSING

by

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A thesis submitted to the Faculty of Graduate
Studies and Research in partial fulfillment
of the requirements for the degree of

Master of Engineering

Department of Electronics
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The undersigned recommend to the Faculty of Graduate Studies and Research the acceptance of the thesis:

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ABSTRACT

Arguments supporting the use of sampled analog signal processing techniques for adaptive echo cancellation are presented in this thesis. Proposed advantages over pure digital signal processing approaches include elimination of input signal quantization error, resulting in improved echo cancellation, and reduction in circuit complexity and power dissipation due to the elimination of front end A/D converters, digital signal storage registers, and digital multipliers.

Background mathematics are presented first, followed by the description of a supportive computer simulation. An overview of suitable analog signal processing technology then leads to the design and characterization of a 64-stage echo canceller, built to illustrate the concepts discussed in a practical context.

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LIST OF SYMBOLS AND ABBREVIATIONS

A	Arbitrary constant of integration
BBD	Bucket-brigade device
C	Dynamic amplifier feedback capacitor, cross correlation vector between $x(\cdot)$ and $y(\cdot)$
c'	Gradient adaption weighting constant
$\tilde{C}$	Transformed C vector
$\tilde{C}_k$	k^{th} component of $\tilde{C}$
C_e, C_x	Mid-tread quantization thresholds
C_i	Dynamic amplifier input capacitance
C_o	Dynamic amplifier output capacitor
C_{1k}, C_{2k}	BBC storage capacitors for the k^{th} stage
D_n	Expected misalignment vector
$d(\cdot)_n$	Component of D_n
$E\{\cdot\}$	Ensemble expectation
$E\{\cdot \cdot\}$	Conditional expectation
$e(\cdot)$	Error signal
EPROM	Erasable programmable read only memory
ERL	Echo return loss
ERLE	Echo return loss enhancement
f_s	Sampling frequency
$f_a g, x$	pdf for $a(n)$ with $g(k)_n$ $x(n-k)$ known
$f_z(\cdot)$	pdf for Z
FPN	Fixed pattern noise

G_n	Misalignment vector
$g(.)_n$	Component of G_n
$G_1 G_2$	Amplifier gains in mid-tread quantization circuits
$\hat{H}_n$	Estimated impulse response vector
$\tilde{H}_n$	Transformed impulse response vector
H^*	Optimal impulse response vector
$\hat{h}(.)_n$	Component of $\hat{H}_n$
$\tilde{h}(.)_n$	Component of $\tilde{H}_n$
$h^*(.)$	Component of H^*
IIR	Infinite impulse response
M	Modal matrix
MDAC	Multiplying D/A converter
N	Number of PTF taps
n, k	Sample numbers
$P(.)$	Probability
PCM	Pulse code modulation
pdf	Probability density function
PTF	Programmable transversal filter
Q_n	Noise component of coefficient adjustment vector
Q_1	Dynamic amplifier transistor
R	Channel correlation matrix
R_w	Channel correlation matrix for white noise input
RAM	Random access memory
RMS	Root mean square
SGN[.]	Algebraic sign function
T	Sampling period, matrix transpose
t	Real time

x

$U_g(.)_n$	Coefficient adjustment vectors
$U_s(.)_n$	
$u_g(.)_n$	Components of $U_g(.)_n$ and $U_s(.)_n$
$u_s(.)_n$	
V_{DD}	High MOS supply
V_i	Analog input voltage
V_{ss}	Low MOS supply
V_T	MOS transistor threshold voltage
V_o	Analog output voltage
w	Dummy variable
X_n	Input signal vector
$x(.)$	Component of X_n
$y(.)$	Echo signal
$\hat{y}(.)$	Estimated echo signal
Z	Standard normally distributed random variable
z	Particular value for Z
β	Gradient algorithm convergence constant
γ	Fixed coefficient increment
λ_k, λ_{max}	Eigenvalues of R
v	μ -255 PCM constant
σ_e^2	Error signal power
σ_x^2	Input signal power
σ_y^2	Echo signal power
τ_k	kth convergence time constant

τ_w	Time constant for white noise input
$\phi_x \phi_e$	Mid-tread quantization functions for $e(\cdot)$ and $x(\cdot)$
ϕ_{mk}	kth BBD multiplexing clock
ϕ_1, ϕ_2, ϕ_3	PTF chips clocks
ϕ_4, ϕ_5	
$in-SR,$	
$\phi_1-SR,$	
$\phi_2-SR, R,$	
S, G_1	
ψ	Abbreviation for $g(k)_n x(n-k)$
$\nabla.$	Gradient operator
$ \cdot $	Vector magnitude, scalar absolute value
$\langle \cdot \rangle$	Time average
$+$	Connected conductors
$\uparrow$	Unconnected conductors

CHAPTER 1

INTRODUCTION

1.0 Introduction

This thesis describes the design of a mixed digital/sampled analog echo canceller based on a programmable transversal filter. Although numerous voiceband echo cancellers have been built, studied and marketed [1,2] for telephony, none have yet fully recognized and exploited the potential advantages of analog sample storage.

Echo cancellers described in [1] and [2] report performance which is limited by quantization effects due to digital storage of both tap weights and input signal samples. It is proposed that, by storing and processing the input signal in analog form, one of these sources of quantization noise can be eliminated entirely. Thus, either improved cancellation can be expected for the same digital tap weight resolution or the number of bits required for tap weight storage can be relaxed to establish the same level of performance.

In addition to the above advantage, it is probable that an integrated mixed digital/sampled analog echo canceller would consume less power and chip area than a equivalent digital realization. This is due to both the elimination of the need for a front end A/D converter and the inherent ability of sampled analog transversal filters to offer lower power consumption and chip area usage than digital designs.

The purpose of this thesis is to demonstrate both mathematically and through the design of a laboratory model the following potential advantages of this design approach:

- 1) Performance competitive with state-of-the-art digital cancellers can be achieved with relaxed coefficient precision due to elimination of input quantization effects.
- 2) By using a simplified convergence algorithm, the echo canceller can be realized without the use of an A/D converter or high speed digital computational elements. In fact, such a design could be implemented as part of a larger system on a single silicon chip due to its relative simplicity.

1.1 Review of Echo Cancellation using an Adaptive Transversal Filter

The principle on which virtually all commercial echo cancellers [1,2] operate is illustrated in Figure 1.1. The canceller basically uses the cross-correlation between the receive channel, $x(t)$, and the transmitted channel, $e(t)$, to adjust the tap weights of a programmable transversal filter (PTF). When a steady state has been reached, the power in the correlated component of $e(t)$ is minimized and the filter's tap weights approximate samples of the impulse response of the hybrid/channel combination, $h(t)$.

Since the echo canceller is always in the circuit, it cancels echos even during double talking (although the convergence algorithm may be disabled) and introduces no perceivable switching effects.

1.2 Applications for Echo Cancellers

Echo cancellers have a wide variety of applications,

Figure 1.1: Basic Echo Canceller Concept

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particularly in the field of telephony. In the long distance telephone network for example, 2-wire subscriber circuits undergo 4-wire conversions via hybrid circuits for transmission and amplification purposes. A simplified view of this process is shown in Figure 1.2a). As indicated, leakage between the transmit and receive paths due to imperfect hybrids causes energy to be reflected back to the users. Since the hybrids and users are generally separated by long distances, the effect of this leakage is delayed in time and hence can produce an irritating echo.

The classical solution to this problem, which is still in wide use, is to use echo suppressors which insert loss into the transmit side of each hybrid when the receive side is active as shown in Figure 1.2a). This attenuates the echo without directly affecting the primary communication path. Unfortunately, due to finite switching times, this solution results in occasional clipping of wanted speech passages. It also cannot suppress echoes when both parties are talking simultaneously.

Replacement of echo suppressors with echo cancellers as shown in Figure 1.2b) can reduce the coupling between the transmit and receive sides of each hybrid without introducing primary path loss and hence can eliminate the above problems. Echo cancellers can also be useful at the subscriber end of local loops if true 4-wire appearance is required from the 2-wire lines. As depicted in Figure 1.2c) an echo canceller combined with a hybrid circuit can minimize the leakage between the subscriber's transmit and receive channels. This would enable simultaneous transmission and reception of digital data for example. Other applications include cancellation of speaker/microphone feedback.

a) Standard telephone network echo suppressor

b) Echo canceller replacing echo suppressor

c) Echo canceller used to produce full duplex 2-wire channel

Figure 1.2: Applications for Echo Cancellers

in small amplification systems and stabilization of bidirectional gain circuitry in 2-wire circuits.

1.3 Proposed System Partitioning

The echo canceller to be studied will be partitioned as shown conceptually in Figure 1.3.

Analog input samples, $x(n-k)$, are weighted according to digitally represented estimates of the unknown system's impulse response, $h(n)$. Weighted signals are then summed using analog techniques to produce a filtered output, $y(n)$, which is the canceller's estimate of the unknown system response.

The estimated response is subtracted from the sampled, true response, $y(n)$ to produce an error signal, $e(n)$. This error signal is used along with the input samples by the correlation processor, to digitally update the estimated response during each sampling instant.

Since the input signal is never digitized in such a system, the only source of quantization error originates from the inability of the quantized tap weights to ideally represent samples of the unknown system's impulse response. Note that Figure 1.3 is only intended to define system partitioning between analog and digital circuitry and does not necessarily reflect the choice of an exact architecture.

1.4 Existing Standards for Performance Evaluation

The state-of-the-art for commercially available voiceband digital echo cancellers is typified by the VLSI device described in [1] which has been used with marked success in the North American telephone network. This canceller was developed by Bell Laboratories and is

Figure 1.3: Partitioning of Proposed Echo Canceller

presently being marketed by AT&T. Its high level of performance coupled with the fact that information related to its design and characterization has been published will make it a suitable benchmark for performance comparisons with the proposed architecture throughout this thesis. It dissipates 0.7 watts, occupies 111,428 square mils of chip area (designed for a 5 micron NMOS process) and accepts μ -255 I/O.

Another design, originated by COMSAT [2],[7], has been well documented and contains coefficient adaptation circuitry which bears some similarities to that which will be employed in the laboratory model. Hence it has been chosen as a basis for comparison in certain key areas. It is designed using discrete components.

1.5 Thesis Format

This thesis will begin with a fairly rigorous development of the standard gradient algorithm and of suggested methods for simplifying the algorithm so that it can more easily be integrated with a canceller of the type proposed. The conclusions drawn from this mathematical analysis will then be substantiated by results generated from a computer simulation. This will lead to a description of the design and characterization of an echo canceller, illustrating the principles developed in a practical context.

Finally recommendations pertaining to further research, including suggestions regarding integration of such a canceller on a single IC, will be presented.

CHAPTER 2

ANALYSIS OF ECHO CANCELLER ADAPTATION ALGORITHMS

2.0 Introduction

In this chapter, some classical adaptive transversal filter theory, based on [3] and [4], will be reviewed. This will provide the background for an approximate analysis of the principles behind algorithm simplifications to be employed in the design of the laboratory model. Finally, the mathematical reasoning, leading to the potential performance advantage of sampled analog over existing digital architectures for echo cancellation, will be presented.

2.1 Review of the Gradient Algorithm as applied to Transversal Filter Adaptation

The echo canceller is assumed to operate in a linear environment. That is, it is assumed that the echo is related to the input signal by the convolution:

$$y(t) = \int_{-\infty}^{\infty} h(\tau) x(t-\tau) d\tau \quad (2.1)$$

where $h(t)$ is the unknown impulse response of the reflection source.

Furthermore it is assumed that this process can be approximated via the discrete convolution:

$$\hat{y}(nT) = T \sum_{k=-\infty}^{\infty} \hat{h}(kT) x(nT-kT) \quad (2.2)$$

where T is the sampling period of the system and $\hat{y}(nT)$ and $\hat{h}(nT)$ are estimates of echo and the impulse response of the unknown system respectively.

It is expedient at this stage to suppress reference to sampling period, T , for the major remaining portion of the derivation. Provided that T is sufficiently small to satisfy the Nyquist criterion, it is only significant as a time scaling factor.

It is assumed that the unknown system's impulse response can be approximated by a causal, finite pulse train which has a duration of N sampling periods. Thus, it becomes convenient to define the vectors:

$$\hat{H}_n = \begin{bmatrix} \hat{h}(0)_n \\ \hat{h}(2)_n \\ \vdots \\ \hat{h}(N-1)_n \end{bmatrix} \quad (2.3)$$

and:

$$X_n = \begin{bmatrix} x(n) \\ x(n-1) \\ \vdots \\ x(n-N+1) \end{bmatrix} \quad (2.4)$$

so that equation 2.2 reduces to:

$$\hat{y}(n) = \hat{H}_n^T X_n$$

Here the subscript n signifies the value valid during sampling instant n , and the superscript T signifies the matrix transpose operation.

If $y(n)$ is the sampled response of the unknown system, we define the error sequence, $e(n)$, as the difference between the desired and estimated responses:

$$e(n) = y(n) - \hat{H}_n^T X_n \quad (2.5)$$

It is the objective of the gradient algorithm to minimize the mean-square error:

$$\langle e(n)^2 \rangle = \langle (y(n) - \hat{H}_n^T X_n)^2 \rangle \quad (2.6)$$

Under the assumption that the impulse response vector is adjusted sufficiently slowly so that it appears virtually constant when compared to random variation of the input vector, X_n , equation 2.6 reduces to:

$$\langle e(n)^2 \rangle = \langle y^2(n) \rangle - 2 C^T \hat{H}_n + \hat{H}_n^T R \hat{H}_n \quad (2.7)$$

where R is the $N \times N$ input correlation matrix, defined by:

$$R = \langle X_n X_n^T \rangle \quad (2.8)$$

and:

$$C = \langle y(n) X_n \rangle \quad (2.9)$$

is the cross correlation vector between the input and output of the unknown system.

Assuming a random input signal, the mean-squared error is generally a function of the $\hat{H}_n$ vector in N-space, having an absolute minimum at H^* . Thus H^* is the best possible estimate of the unknown impulse response vector, and the mean-square error is non-decreasing along any path which moves away from it. A simple representation, illustrating this principle in the plane related to the i th component of $\hat{H}_n$, is presented in Figure 2.1.

Under such circumstances, it is a well known fact [3] that the gradient vector:

$$\nabla \langle e^2(n) \rangle = \begin{bmatrix} \frac{\partial}{\partial h(0)} \langle e(n)^2 \rangle \\ \frac{\partial}{\partial h(1)} \langle e(n)^2 \rangle \\ \vdots \\ \frac{\partial}{\partial h(N-1)} \langle e^2(n) \rangle \end{bmatrix} \quad (2.10)$$

which is a function of $\hat{H}$, will indicate the direction of maximum rate of increase of mean-square error as pictured. The gradient algorithm strives to constantly move opposite the gradient vector and thus in the direction of steepest descent toward H^* . Mathematically, this strategy may be stated as:

Mean-Square Error
 $\langle e^2(n) \rangle$

Figure 2.1: Illustration of the Mean-Square Error Function and
Significance of the Gradient Vector

$$\hat{H}_{n+1} = \hat{H}_n - \beta \cdot \nabla \langle e(n)^2 \rangle \quad (2.11)$$

where β is a weighting constant which must be restricted by conditions to be derived.

An expression for the gradient vector is derived by applying equation 2.10 to equation 2.7 to obtain:

$$\nabla \langle e(n)^2 \rangle = -2C + 2R\hat{H}_n \quad (2.12)$$

Since H^* is assumed to be the absolute minimum of the mean-square error function, the gradient vector will null for that value of $\hat{H}_n$ and equation 2.12 will simplify to:

$$H^* = R^{-1}C \quad (2.13)$$

Equation 2.13 is the famous Wiener-Hopf relation in matrix form [4]. This result proves that the point at which the gradient vector nulls indeed identifies the impulse response of the unknown system.

A method of applying the gradient algorithm is designed by substituting equation 2.12 into 2.11 to yield:

$$\hat{H}_{n+1} = \hat{H}_n + 2\beta(C - R\hat{H}_n) \quad (2.14)$$

Referring to the definitions of R and C given in equations 2.8 and 2.9, this implies that the adaptation strategy for the k th tap weight should be:

$$\hat{h}(k)_{n+1} = \hat{h}(k)_n + 2\beta \left(\langle y(n)x(n-k) \rangle - \left\langle \sum_{p=0}^{N-1} \hat{h}(p) x(n-k) x(n-p) \right\rangle \right) \quad (2.15)$$

Using the relationship:

$$\hat{y}(n) = \sum_{p=0}^{N-1} \hat{h}(p) x(n-p) \quad (2.16)$$

in 2.15 and simplifying gives:

$$\begin{aligned} \hat{h}(k)_{n+1} &= \hat{h}(k)_n + 2\beta \langle (y(n) - \hat{y}(n)) x(n-k) \rangle \\ &= \hat{h}(k)_n + 2\beta \langle e(n) x(n-k) \rangle \end{aligned} \quad (2.17)$$

Equation 2.17 states that each tap weight can be adjusted using only information gained from the input samples and the error function. In practice, the expectation operation is usually neglected under the assumption that, with β chosen sufficiently small, the cumulative effect of repetitive application of equation 2.17 will be approximately correct. Hence the actual adaptation strategy which is applied, stated in matrix form, is [4]:

$$\hat{H}_{n+1} = \hat{H}_n + 2\beta e(n) X_n \quad (2.18)$$

The analysis in the following section will be based on the ideal gradient algorithm defined by equation 2.14. The results will, however, approximately model the characteristics of equation 2.18 [4].

2.2 A Review of Stability and Convergence Properties of the Gradient Algorithm

Equation 2.14 can be restated as:

$$\hat{H}_{n+1} = \hat{H}_n - 2\beta M(M^{-1}RM)M^{-1}\hat{H}_n + 2\beta C \quad (2.19)$$

where M is the modal matrix for R . Note here that:

$$\Lambda = M^{-1}RM \quad (2.20)$$

is a diagonal matrix containing the eigenvalues of the input correlation matrix.

Applying the definition in equation 2.20 to equation 2.19, and premultiplying both sides by M^{-1} gives:

$$(M^{-1}\hat{H}_{n+1}) = (M^{-1}\hat{H}_n) - 2\beta \Lambda M^{-1}\hat{H}_n + 2\beta M^{-1}C \quad (2.21)$$

If we move to a new coordinate space defined by the transformations:

$$\tilde{H}_n = M^{-1}\hat{H}_n \quad (2.22)$$

and:

$$\tilde{C} = M^{-1}C \quad (2.23)$$

equation 2.21 becomes:

$$\tilde{H}_{n+1} = \tilde{H}_n - 2\beta \Lambda \hat{H}_n + 2\beta \tilde{C} \quad (2.24)$$

The k th row of this vector equation is:

$$\tilde{h}(k)_{n+1} = (1 - 2\beta \lambda_k) \tilde{h}(k)_n + 2\beta \tilde{c}_k \quad (2.25)$$

where $\tilde{h}(k)$ and $\tilde{c}_k$ are k th components of $\tilde{H}$ and $\tilde{C}$ respectively, and λ_k is the k th eigenvalue of R . This simple difference equation converges if and only if the geometric ratio:

$$|1 - 2\beta \lambda_k| < 1 \quad (2.26)$$

or equivalently:

$$0 < \beta < 1/\lambda_k \quad (2.27)$$

Since all of the transformed components of $\tilde{H}$ are decoupled by the similarity transformation, a sufficient condition for convergence of the entire system is:

$$0 < \beta < 1/\lambda_{\max} \quad (2.28)$$

where $\lambda_{\max}$ is the largest eigenvalue of the input correlation matrix.

The convergence process itself can be modelled by rewriting equation 2.25 as:

$$\tilde{h}(k)_{n+1} - \tilde{h}(k)_n = 2\beta \tilde{c}_k - 2\beta \lambda_k \tilde{h}(k)_n \quad (2.29)$$

and making the continuous approximation:

$$\frac{\partial \tilde{h}(t)}{\partial t} \approx \frac{\tilde{h}(k)_{n+1} - \tilde{h}(k)_n}{T} \quad (2.30)$$

This results in the approximate differential equation:

$$\frac{\partial \tilde{h}(t)}{\partial t} \approx \frac{2\beta \left(\tilde{c}_k - \lambda_k \tilde{h}(t) \right)}{T} \quad (2.31)$$

which has the family of solutions:

$$\tilde{h}(k) = A \exp \left(- \frac{2\beta \lambda_k}{T} t \right) \quad (2.32)$$

where A is a constant.

Equation 2.32 implies that the transient response of the kth mode of the system is a decaying exponential with time constant:

$$\tau_k = \frac{T}{2\beta \lambda_k} \quad (2.33)$$

For the simple case which occurs when the input has a flat spectrum, the channel correlation matrix is simply:

$$R_{\omega} = \sigma_x^2 I \quad (2.34)$$

where I is an N -dimensional identity matrix and σ_x^2 is the mean square input power. Hence the system converges exponentially with time constant:

$$\tau_{\omega} = \frac{T}{2 \beta \sigma_x^2} \quad (2.35)$$

In order to make convergence independent of the power in the input signal, it is desirable to set:

$$2 \beta = c' / \sigma_x^2 \quad (2.36)$$

where c' is a constant. Substituting this into 2.35 gives:

$$\tau_{\omega} = \frac{T}{c'} \quad (2.37)$$

Thus, by making β inversely proportional to the input power, constant, predictable white noise convergence properties can be expected. In fact, the rate of convergence in dB per second will be:

$$\text{dB/sec} = 20 \frac{c}{T} \log_{10} e \quad (2.38)$$

In the VLSI canceller developed by Bell Laboratories for example, $c' \approx .001$, yielding an approximate 70 dB/sec convergence rate. Since this canceller is designed to reduce echo by approximately 27 dB, it converges in approximately 27/70 sec or about 400 msec [1]. Convergence times of this order of magnitude are typical of commercial echo cancellers. Therefore, if an echo canceller with a simplified algorithm is to be competitive, it must be able to converge at a similar speed without compromising steady state cancellation.

2.3 Simplifying the Correction Strategy

The architecture proposed in Section 1.3 stores the input samples and produces the error signal in analog form. In order to directly calculate coefficient corrections for the adaptation strategy defined by equation 2.18, the product of these two signals must be calculated. Furthermore, since the coefficients are stored in digital form, each product must be digitized before it can be used as a correction. Since all of the tap weights are adjusted once per sampling instant, this suggests the need for a multiplier with A/D converter combination, capable of operating at or above the superfrequency of the PTF, Nf_g . Such a device would be very costly. Since one of the aims of this work is to show that a high performance canceller can be designed without the use of an A/D converter, a simpler adaptation strategy must be sought.

Many authors have noted the robustness of the gradient algorithm. It can be shown, in fact, that virtually any sign-preserving approximation of the ideal correction strategy will enable approximate system identification provided that loop gain is kept sufficiently small [5]. The approximation which can most easily be applied to the chosen system architecture uses fixed magnitude corrections which preserve the algebraic signs dictated by the gradient algorithm. This strategy can be stated mathematically as:

$$h(k)_{n+1} = h(k)_n + \gamma \text{SGN}[e(n)] \text{SGN}[x(n-k)] \quad (2.39)$$

Since the SGN function has unit magnitude and the algebraic sign of its argument, all corrections have constant magnitude. The most easily implemented choice for γ in such a system is equal to the magnitude of the least significant bit of the tap weight storage words.

2.4 Convergence Properties of the Simplified Algorithm

Analysis of the convergence properties of the simplified algorithm is significantly less tractable than the equivalent analysis for the gradient algorithm. This is due to the fact that each adjustment is a nonlinear function of the standard gradient algorithm correction:

$$u_g(k)_n = 2\beta e(n) x(n-k) \quad (2.40)$$

Consider the adjustment for the k^{th} tap weight during the n^{th} sampling instant according to equation 2.39:

$$u_s(k)_n = \gamma \text{SGN} [e(n)] \text{SGN} [x(n-k)] \quad (2.41)$$

Substituting for $e(n)$ from equation 2.5 gives:

$$u_s(k)_n = \gamma \text{SGN} [y(n) - \hat{H}_n^T X_n] \text{SGN} [x(n-k)] \quad (2.42)$$

Under the assumption that the Wiener-Hopf solution for the impulse response of the unknown system, given by equation 2.13, can be used to accurately model the echo, $y(n)$, the argument of the first SGN function can be further expanded to give:

$$u_s(k)_n = \gamma \text{SGN} [(H^* - \hat{H}_n)^T X_n] \text{SGN} [x(n-k)] \quad (2.43)$$

By introducing the impulse response misalignment vector:

$$G_n = H^* - \hat{H}_n = \begin{bmatrix} g(0)_n \\ g(1)_n \\ \vdots \\ g(N-1)_n \end{bmatrix} \quad (2.44)$$

this can be written as:

$$u_g(k)_n = \gamma \text{SGN}[g(k)_n x(n-k) + \sum_{p \neq k} g(p)_n x(n-p)] \text{SGN}[x(n-k)] \quad (2.45)$$

In order to continue the analysis, it becomes necessary to make the limiting assumption that the input signal, $x(n)$, is white, Gaussian noise. Fortunately, most of the validity of the analysis is preserved since it is generally accepted that relative performance of echo cancellers with white Gaussian inputs is indicative of relative performance with speech inputs [5].

By assuming that convergence is slow, and thus that the misalignment vector can be approximated as being constant over many sampling instants, $U_g(k)_n$ can be viewed as a random process. This process is decomposed into a mean component, which tends to slowly shorten the misalignment vector, and a much larger random noise component which has no average effect on the convergence process.

The existence of a nonzero expected value for the tap weight correction is indicated by the fact that $x(n-k)$ is present in the arguments of both SGN functions in equation 2.45. Thus, a correlation exists between the arguments of the two SGN functions in the $g(k)_n$ direction which is masked, but not eliminated, by the distortions imposed.

To quantify this correlation, we assume that $g(k)_n$ and $x(n-k)$ are known, and view the argument of the first SGN function as random process having mean, $g(k)_n x(n-k)$ and variance equal to the power in the summation term. The process is Gaussian because it is a summation of Gaussian random variables ($g(p)_n x(n-p)$).

In the wider sense, $g(k)_n x(n-k)$ is itself a zero mean Gaussian process which is uncorrelated with the summation. Assuming that

the misalignment vector has many significant components, the variance of $g(k)_n x(n-k)$ will be small compared to that of the summation and we can make the approximation:

$$\left\langle \left[\sum_{p \neq k} g(p)_n x(n-p) \right]^2 \right\rangle \approx \left\langle \left[\sum_p g(p)_n x(n-p) \right]^2 \right\rangle = \sigma_e^2 \quad (2.46)$$

Here σ_e^2 is the variance of the error signal, which can be related to the input signal power variance, σ_x^2 , using the equation:

$$\sigma_e^2 = |G_n|^2 \sigma_x^2 \quad (2.47)$$

where $|G_n|$ is the length of the misalignment vector. Note that the effect of any additive noise, superimposed on the error signal, has been neglected here. The variance of such noise could easily be added to σ_e^2 to make the results more generally applicable.

In light of equations 2.46 and 2.47, the error signal, which forms the argument of the first SGN function in equation 2.45, under the condition that $g(k)_n x(n-k)$ is known, can be modelled as having a mean value of $g(k)_n x(n-k)$ and an approximate variance σ_e^2 . The resulting approximate pdf for $e(n)$, $f_{e|g,x}$, is illustrated in Figure 2.2. Here the product $g(k)_n x(n-k)$ is assumed to be positive, although this has no effect on the final results of the analysis. Hence the mode of the function is skewed slightly to the right.

The expected value of $\text{SGN}[e(n)]$, given $g(k)_n$ and $x(n-k)$, will be given by:

$$E \left\{ \text{SGN}[e(n)] \middle| g(k)_n x(n-k) \right\} = \int_{-\infty}^{\infty} \text{SGN}[e] f_{e|g,x}(e) de$$

Figure 2.2: Conditional pdf for $e(n)$

$$= \int_{e=0}^{\infty} f_e |g.x(e) de - \int_{e=-\infty}^0 f_e |g.x(e) de \quad (2.48)$$

where the vertical bar denotes conditioning. This is viewed as the difference between area B and area A in the diagram.

Letting:

$$\psi = g(k)_n \times (n-k) \quad (2.49)$$

equation 2.48 can be equivalently stated as:

$$\begin{aligned} E \left\{ \text{SGN}[e(n)] | \psi \right\} &= P(e(n) > 0 | \psi) - P(e(n) < 0 | \psi) \\ &= 2P(0 < e(n) < \psi) \end{aligned} \quad (2.50)$$

where $P(\cdot)$ denotes statistical probability.

Using the transformation:

$$Z = \frac{e(n) - \psi}{\sigma_e} \quad (2.51)$$

so that Z has the standard normal pdf:

$$f_z(z) = \frac{1}{\sqrt{2\pi}} \exp\left(-\frac{z^2}{2}\right) \quad (2.52)$$

this expectation becomes:

$$\begin{aligned} E \left\{ \text{SGN}[e(n)] \middle| \psi \right\} &= 2P\left(-\frac{\psi}{\sigma_e} < Z < 0\right) \\ &= 2P\left(0 < Z < \frac{\psi}{\sigma_e}\right) \end{aligned} \quad (2.53)$$

or:

$$E \left\{ \text{SGN}[e(n)] \middle| \psi \right\} = \frac{2}{\sqrt{2\pi}} \int_{-\frac{\psi}{\sigma_e}}^{\frac{\psi}{\sigma_e}} \exp\left(-\frac{z^2}{2}\right) dz \quad (2.54)$$

The integrand here can be expanded using a Taylor series to give:

$$\begin{aligned} E \left\{ \text{SGN}[e(n)] \middle| \psi \right\} &= \sqrt{\frac{2}{\pi}} \int_{-\frac{\psi}{\sigma_e}}^{\frac{\psi}{\sigma_e}} \left(1 - \frac{z^2}{2} + \frac{z^4}{8} - \dots\right) dz \\ &= \sqrt{\frac{2}{\pi}} \left(\frac{\psi}{\sigma_e} - \frac{1}{6} \left(\frac{\psi}{\sigma_e}\right)^3 + \frac{1}{40} \left(\frac{\psi}{\sigma_e}\right)^5 - \dots \right) \end{aligned} \quad (2.55)$$

By assuming that ψ is much smaller than σ_e , which is essentially the same premise on which 2.46 is based, all but the first term in equation 2.55 can be neglected. Hence:

$$E \left\{ \text{SGN}[e(n)] \middle| \psi \right\} \approx \sqrt{\frac{2}{\pi}} \frac{\psi}{\sigma_e} \quad (2.56)$$

Substituting from equations 2.47 and 2.49 we find:

$$E \left\{ \text{SGN}[e(n)] \middle| g(k)_n x(n-k) \right\} \approx \sqrt{\frac{2}{\pi}} \frac{g(k)_n x(n-k)}{\sqrt{G_n} \sigma_x} \quad (2.57)$$

Equation 2.57 provides the means by which we can calculate the final expected correction using:

$$\begin{aligned} & E \left\{ \gamma \text{SGN}[e(n)] \text{SGN}[x(n-k)] \middle| g(k)_n \right\} \\ &= E \left\{ \gamma \text{SGN}[x(n-k)] \middle| E \left\{ \text{SGN}[e(n)] \middle| g(k)_n x(n-k) \right\} \right\} \end{aligned} \quad (2.58)$$

Equation 2.58 follows from the well known statistical identity [17]:

$$E(P) = E \left\{ E \left\{ P \middle| Q \right\} \right\} \quad (2.59)$$

where both P and Q are continuous random variables.

Since $g(k)_n$ is assumed to be essentially constant for many sampling periods, the conditional expectation in equation 2.59 need only be evaluated over the domain of the zero mean, Gaussian input, $x(n-k)$ having pdf:

$$f_x(x) = \frac{1}{\sqrt{2\pi}\sigma_x} \exp\left(-\frac{1}{2}\left[\frac{x}{\sigma_x}\right]^2\right) \quad (2.60)$$

Hence the right side of equation 2.58 is given by:

$$E \left\{ \text{SGN}[x(n-k)] \cdot E \left\{ \text{SGN}[e(n)] \left| g(k)_n x(n-k) \right. \right\} \right\} =$$

$$\int_{-\infty}^{\infty} \gamma f_x(x) \text{SGN}[x] E \left\{ \text{SGN}[e(n)] \left| g(k)_n x(n-k) \right. \right\} dx \quad (2.61)$$

By making appropriate substitutions from equations 2.57 and 2.60, the readily achieved result is:

$$E \left\{ \gamma \text{SGN}[e(n)] \text{SGN}[x(n-k)] \left| g(k)_n \right. \right\} = \frac{2\gamma}{\pi} \frac{g(k)_n}{|G_n|} \quad (2.62)$$

This nontrivial result quantifies the average amount by which k^{th} component of the misalignment vector is expected to change during each iteration. Implicit in this entire analysis is the assumption that γ is small. An approximate difference equation can now be constructed to model the mean convergence process:

$$D_{n+1} = D_n \left(1 - \frac{2\gamma}{\pi |D_n|} \right) \quad (2.63)$$

where D_n is the expected value of G_n .

As stated in equation 2.47, the mean-square error is proportional to $|G_n|^2$. This implies that the parameter:

$$|D_n|^2 = D_n^T D_n \quad (2.64)$$

will be a good indicator of the mean-square error convergence process.

Multiplying both sides of 2.63 by D_{n+1}^T and simplifying gives:

$$|D_{n+1}|^2 = \left(|D_n| - \frac{2\gamma}{\pi} \right)^2 \quad (2.65)$$

By assuming an average convergence process which is continuous in time, this leads to:

$$|D(t)| = \sqrt{G_n^T G_n} \left| - \frac{2\gamma}{\pi} \frac{t}{T} \right| \quad (2.66)$$

where $|D(0)|$ has been set equal to the known initial misalignment vector length. This may be considered a valid approximate model for the mean convergence process as long as the length of the misalignment vector is much greater than that of the correction vectors.

If it is assumed that the residual echo is negligible once the length of the misalignment vector approaches that of the correction vectors, convergence time may be estimated by setting $|D(t)|$ to zero in equation 2.66. Thus the approximate convergence time is:

$$T_c = \frac{\pi \sqrt{G_n^T G_n} |_{t=0}}{2\gamma} \cdot T \quad (2.67)$$

The second parameter of major interest in evaluating the performance of the simplified algorithm is the degree of steady state echo cancellation it provides. In the above derivations it was assumed that the average convergence process occurs in the presence of a larger, zero mean random vector noise component. The effects of this component must be considered in modelling steady state properties.

Since the noise component of the adjustment vector is much larger than the mean, the length of the noise vector, defined as Q_n , can be assumed to be constant and equal to that of the entire adjustment vector:

$$|Q_n| = \left(\sum_{k=0}^{N-1} u_s^2(k)_n \right)^{\frac{1}{2}} \quad (2.68)$$

Substituting for $u_s(k)_n$ from equation 2.41 yields:

$$|Q_n| = N^{\frac{1}{2}} \gamma \quad (2.69)$$

The effect of this noise on the mean misalignment vector length can be modelled by first subtracting the adjustment vector, decomposed into the noise component, Q_n , and a mean component derived from equation 2.62, from the misalignment vector. Taking the mean-square magnitude of the result and assuming that Q_n is uncorrelated with G_n gives the iteration:

$$E \left\{ |G_{n+1}|^2 \right\} = E \left\{ \left(|G_n| - \frac{2\gamma}{\pi} \right)^2 + |Q_n|^2 \right\} \quad (2.70)$$

Substituting for $|Q_n|$ from equation 2.69 and substituting $|G_\infty|$ for $|G_n|$ and $|G_{n+1}|$ as will be the case when convergence is complete gives:

$$E \left\{ |G_\infty| \right\} = \frac{N \pi \gamma}{4} + \frac{\gamma}{\pi} \quad (2.71)$$

Equation 2.71 will approximately quantify the steady state length of the misalignment vector. Its accuracy and that of equations 2.66 and 2.67 will be verified via computer simulation in Chapter 3. Note that the second term on the right side will be negligible for transversal filters having more than a few taps.

2.5 Comparison of Simplified Algorithm with Gradient Algorithm

As described in the previous section, the mean-square residual error is proportional to the squared length of the misalignment vector for constant input power. That is, neglecting additive noise:

$$\sigma_e^2 = |G_n|^2 \sigma_x^2 \quad (2.47)$$

The Echo Return Loss Enhancement (ERLE), which is the amount by which the canceller attenuates the echo, may be defined as:

$$ERLE = 20 \log_{10} \frac{\sigma_y}{\sigma_e}$$

$$= 20 \log_{10} \frac{\sigma_x}{\sigma_e} \frac{\sigma_y}{\sigma_x} .$$

$$= 20 \log_{10} \frac{\sigma_x}{\sigma_e} - 20 \log_{10} \frac{\sigma_x}{\sigma_y} \quad (2.72)$$

The second term in this equation:

$$\text{ERL} = 20 \log_{10} \frac{\sigma_x}{\sigma_y} \quad (2.73)$$

represents the amount by which the echo entering the canceller is attenuated with respect to the input signal. It is thus referred to as the Echo Return Loss (ERL) of the 4-wire circuit. Typical hybrid coils in the telephone network, for example, have ERL with an approximately normal distribution. The mean of this distribution is between 11 dB and 15 dB with a standard deviation between 3 dB and 5 dB [2].

The VLSI echo canceller designed at Bell Laboratories employs an approximate version of the gradient algorithm for coefficient adaptation and offers approximately 27 dB of ERLE and a convergence time of between 300 ms and 500 ms [1]. These figures will be used as standards for comparison in the following analysis.

Consider the case where the system ERL is 10 dB. Solving equation 2.47 for $\frac{\sigma_x}{\sigma_e}$ gives:

$$\frac{\sigma_x}{\sigma_e} = |G_n|^{-1} \quad (2.74)$$

which, through substitution into equation 2.72, leads to:

$$\text{ERLE} = 20 \log_{10} |G_n|^{-1} - 10 \quad (2.75)$$

The limiting value for $|G_n|$ from equation 2.71 can be substituted into this equation and the value of γ required for the simplified algorithm to achieve 27 dB of ERLE, calculated (assuming $N=64$ taps). The result is:

$$\gamma = \left(\frac{4\pi}{N\pi^2 + 4} \right) \log_{10}^{-1} \left(\frac{-37}{20} \right) \quad (2.76)$$

$$= 2.79 \times 10^{-4}$$

This implies that a system capable of providing sufficiently small increments would require 13 bit digital words for coefficient storage. Furthermore, if such a canceller were placed in a 4-wire circuit with an ERL of 0 dB, the approximate convergence time from equation 2.67 (with $\sqrt{G_n^T G_n} \big|_{t=0} = 1$ and $T=125 \mu s$) would be 800 ms. This is significantly (≈ 2 times) slower than the commercial device.

This demonstrates the fact that, although it is possible to achieve comparable ERLE from a canceller which employs this simplified algorithm, it must be done at the expense of slower convergence. The tradeoff stems from the fact that the algorithm tends to reduce the misalignment vector to a fixed average length which is independent of its initial length. Therefore, if the initial length of the

misalignment vector is large (low ERL), ERLE can be very good, whereas if it is smaller, ERLE degrades unless the increment size is reduced.

2.6 Companded Coefficient Coding to Improve Simplified Algorithm Characteristics

The above shortcoming of the simplified algorithm could be skirted by decreasing the system increment size when the 4-wire ERL is high. This could be accomplished by making the increment size dependent on the magnitude of the error signal as suggested in [3]. Such an approach however, requires additional hardware to crudely quantize the error signal and provide for variable increment size.

A simpler alternative is to employ a companded code, such as the μ -255 scheme used in PCM systems [27], for coefficient storage and again, applying corrections only to the least significant bits. One of the inherent characteristics of such a code is that smaller inputs are stored with higher precision. Thus, assuming that higher 4-wire ERL implies a lower average amplitude impulse response, the average increment size used in the representation of such channels will be smaller. Hence available ERLE will remain more constant and the canceller will be better able to compete with commercial models [1,2].

The μ -law transfer function is pictured in Figure 2.3a) and clearly displays the ability of the code to represent lower analog inputs with higher precision. Another, perhaps more significant advantage of using companded codes for coefficient storage is that long, low level sections of the impulse response can be represented more accurately. As shown in Figure 2.3b), typical impulse responses encountered in the telephone network can have negligible amplitude over

- a) ψ -law transfer function showing higher precision for lower analog inputs

Impulse Response $b(t)$

Impulse Response $h(t)$

- b) Typical impulse responses found in telephone network with long low amplitude sections

Figure 2.3: Justification for Companded Coefficient Storage

3.

long time intervals either due to decay of the tail or flat delay if the canceller is located some distance from the reflection source. Since more of the samples in such responses occur near zero than do towards the top end of the dynamic range, better average storage precision (and hence better ERLE) can be achieved using a companded code than a linear one with the same number of bits. This factor becomes even more important when extremely long transversal filters are employed and misrepresentation of long idle sections can be a significant source of error.

The use of companded coding for filter coefficients has been suggested previously in [2], where it is recommended as a means by which convergence time may be decreased while maintaining high coefficient dynamic range. It is significant in fact, that because higher ERLE can be achieved with fewer bits using a companded code, less steps are required to cover a given coefficient register's full dynamic range. Thus, convergence time will be faster than it would be for a linear code with the same dynamic range.

2.6.1 Approximate Analysis of Simplified Algorithm with μ -law Coefficients

Analysis of the convergence properties of the simplified algorithm with companded coding is complicated by the fact that the increment size is different for different coefficient magnitudes. The increment size for the k^{th} nonzero tap weight (coding is linear near $\hat{h}(k)_n = 0$) is well approximated [27] by the equation:

$$\delta(k)_n = \psi |\hat{h}(k)_n| \quad (2.77)$$

where:

$$\psi = \frac{\ln(256)}{127} \quad (2.78)$$

This expression can directly replace the fixed increment, γ , in equation 2.62 to start the analysis. The equivalent of average difference equation 2.63 is then:

$$D_{n+1} = D_n - \frac{2\psi}{\pi |D_n|} \text{diag} \left| \begin{bmatrix} \hat{H}_n \end{bmatrix} \right| D_n \quad (2.79)$$

where:

$$\text{diag} \left| \begin{bmatrix} \hat{H}_n \end{bmatrix} \right| = \begin{bmatrix} |\hat{h}(0)_n| & 0 & 0 & \dots \\ 0 & |\hat{h}(1)_n| & & \\ 0 & & \ddots & \\ \vdots & & & \ddots \\ \vdots & & & & |\hat{h}(N-1)_n| \end{bmatrix} \quad (2.80)$$

Note that this is valid only once most of the coefficients have passed beyond the linear segment of the ψ -law transfer function near $\hat{h}(k)_n = 0$. This is assumed to be the case for all but a negligible portion of the total convergence time.

Following the methods used to derive equation 2.65 gives:

$$|D_{n+1}|^2 = |D_n|^2 - \frac{4\psi}{\pi |D_n|} \sum_{p=0}^{N-1} |\hat{h}(p)|_n^2 d(p)_n^2 + \frac{4\psi^2}{\pi^2} \sum_{p=0}^{N-1} \hat{h}(p)_n^2 \frac{d(p)_n^2}{|D_n|^2} \quad (2.81)$$

which cannot be solved in closed form. Therefore a simple expression for convergence time analogous to equation 2.67 cannot be derived. From arguments stated in Section 2.6, however, we know that convergence will be much faster than it would be for a linear code with the same precision as is found in the lowest segment of the ψ -law. Since the 8-bit ψ -law has approximately the precision of a 13-bit linear code in this region, this system will converge in a much shorter time than the 800 ns stated for the 13-bit system in Section 2.5.

Steady state cancellation at convergence can be estimated by adding the effects of algorithm noise as in the derivation of equation 2.70. In this case however, the noise vector is weighted by the estimated impulse response vector and the average noise power vector length, in analogy to equation 2.68 is:

$$|Q_n| = \left(\sum_{k=0}^{N-1} \psi^2 \hat{h}^2(k)_n \right)^{\frac{1}{2}} \quad (2.82)$$

Following the methods used to derive equation 2.71 gives:

$$E \left\{ \frac{4\mu}{\pi |G_\omega|} \sum_{p=0}^{N-1} |\hat{h}(p)_\omega| g(p)_\omega^2 \right\} = E \left\{ \frac{4\mu^2}{\pi^2} \sum_{p=0}^{N-1} \hat{h}(p)_\omega^2 \frac{g(p)_\omega^2}{|G_\omega|^2} + \mu^2 \sum_{k=0}^{N-1} \hat{h}(k)_\omega^2 \right\} \quad (2.83)$$

The ratio $\frac{g(p)_\omega^2}{|G_\omega|^2}$ must be less than unity for every value of p . Hence the second term will generally dominate the right side of this equation. This leads to the approximation:

$$E \left\{ \frac{4\mu}{\pi |G_\omega|} \sum_{p=0}^{N-1} |\hat{h}(p)_\omega| g(p)_\omega^2 \right\} \approx \sum_{k=0}^{N-1} \mu^2 h^2(k) \quad (2.84)$$

Here the steady state estimated impulse response samples, $\hat{h}(k)_\omega$, have been replaced by those of the unknown system, $h(k)$, on the assumption that the system identification process has been completed accurately.

Finally, by assuming that all tap weights act independently in their random variation after convergence, equation 2.84 can be decomposed into N -decoupled equations for $p=k$:

$$E \left\{ \frac{4\mu}{\pi |G_\omega|} |\hat{h}(p)_\omega| g(p)_\omega^2 \right\} \approx \mu^2 h^2(p), \quad p=0,1,2,\dots,N-1 \quad (2.85)$$

These equations can be manipulated to give:

$$E \left\{ \frac{g(p)_\omega^2}{|G_\omega|} \right\} = \frac{\pi \mu}{4} h(p), \quad p=0,1,2,\dots,N-1 \quad (2.86)$$

then added to form:

$$E \{ |G_{\infty}| \} = \frac{\sum_{p=0}^{N-1} |h(p)|}{4} \quad (2.87)$$

This gives the approximate length of the misalignment vector once the system has converged. The summation term in the numerator provides the ability for the misalignment vector to be made shorter as the 4-wire ERLE decreases, as described in Section 2.5.

The validity of equation 2.87 will be tested by computer simulation in Chapter 3.

2.7 Mid-Tread Quantization to Improve Steady State Convergence Properties

Practically speaking, misalignment noise results largely from random wandering of the filter coefficient estimates near their optimal values. Elimination of this source of error would theoretically leave only the ability of the digital registers to accurately represent the ideal tap weight values (coefficient quantization errors) to limit attainable ERLE.

A very simple method is suggested in [2] for reducing misalignment noise when using identification algorithms of the type described here. It involves enabling the adaptation process at the k th tap only when the related input sample, $x(n-k)$, and the error signal, $e(n)$, exceed the RMS input voltage by fixed ratios. This RMS

voltage can be approximated using simple rectified averaging as will be described in Chapter 5. Such a process may be viewed as mid-tread quantization of the input and error signals (i.e., neglecting samples having low magnitudes). Quantization according to the transfer functions shown in Figure 2.4 is proposed here. Although the justification described in [2] for such a modification involves decorrelation of adjacent input samples so that convergence with human speech input is improved, some other factors have been uncovered in this study.

Firstly since some taps will not be adjusted during each sampling instant, the expected length of the correction vector will decrease. This is statistically equivalent to reducing the magnitude of the "gain" factor, γ , in equation 2.62 (or equivalently μ if the μ -law quantization scheme is used). Hence the steady state length of the misalignment vector will decrease and ERLE will increase.

Secondly, for a given expected correction vector length, misalignment noise will be reduced because the correction vectors will match true gradient algorithm correction vectors more closely. This is due to the fact that each input and error sample can be represented by one of three (+1, 0, -1) possible values instead of two.

The analysis of the simplified algorithm with linear coefficient representations can quite easily be extended to include the effects of the mid-tread quantization schemes. The quantizing functions ϕ_x and ϕ_e will, of course, replace the SGN functions in this case. In place of equation 2.50 we can write

$$E \{ \phi_e \psi \} = P(e(n) > C_e \sigma_e \psi) - P(e(n) < -C_e \sigma_e \psi) \quad (2.88)$$

where C_e and C_x define the thresholds indicated in Figure 2.4.

a) Quantization transfer function for input signal

b) Quantization transfer function for error signal

Figure 2.4: Transfer Functions for Mid-Tread Quantization of Input and Error Signals

Using the transformation defined by equation 2.51, this maps into:

$$\begin{aligned} E \left\{ \phi_e \psi \right\} &= P(Z > C_e - \frac{\psi}{\sigma_e}) - P(Z < -C_e - \frac{\psi}{\sigma_e}) \\ &= P(Z > C_e - \frac{\psi}{\sigma_e}) - P(Z > C_e + \frac{\psi}{\sigma_e}) \end{aligned} \quad (2.89)$$

If $\frac{\psi}{\sigma_e}$ is again assumed to be small, equation 2.89 will be well approximated by:

$$E \left\{ \phi_e \psi \right\} \simeq 2 \frac{\psi}{\sigma_e} \left. \frac{\partial P(Z > \alpha)}{\partial \alpha} \right|_{\alpha=C_e} \quad (2.90)$$

Since:

$$P(Z > \alpha) = \frac{1}{\sqrt{2\pi}} \int_{\alpha}^{\infty} \exp \left(-\frac{z^2}{2} \right) dz \quad (2.91)$$

this simplifies to:

$$E \left\{ \phi_e \psi \right\} \simeq \sqrt{\frac{2}{\pi}} \frac{\psi}{\sigma_e} \exp \left(-\frac{C_e^2}{2} \right) \quad (2.92)$$

which differs from the equation 2.56 only by a constant factor.

Following the methods used in the derivation of equation 2.61 leads to:

$$\begin{aligned}
 E \left\{ \gamma \phi_x[x(n-k)] \phi_e[e(n)] g(k)_n \right\} &= \int_{-\infty}^{\infty} \gamma f_x(x) \phi_x(x) E \left\{ \phi_e \psi = \right. \\
 &\quad \left. g(k)_n x \right\} dx \\
 &= \frac{2\gamma}{\pi} \frac{g(k)_n}{|G_n|} \exp \left(-\frac{C_e^2}{2} - \frac{C_x^2}{2} \right) \quad (2.93)
 \end{aligned}$$

It follows from 2.93 that the addition of mid-tread quantizing slows down the convergence process by a factor of $\exp \left(-\frac{C_e^2}{2} - \frac{C_x^2}{2} \right)$.

Addition of mid-tread quantizing also has the effect of statistically reducing the noise component of the adjustment vector, given by equation 2.69. Hence, in this case:

$$E \left\{ Q_n^2 \right\} = N \gamma^2 P(|x(n-k)| > C_x \sigma_x \text{ and } |e(n)| > C_e \sigma_e) \quad (2.94)$$

Since the correlation between $x(n-k)$ and $e(n)$ is assumed to be very weak, this can be approximated by:

$$\begin{aligned}
E\{|Q_n|^2\} &\approx N\gamma^2 P(|x(n-k)| > C_x \sigma_x) P(|e(n)| > C_e \sigma_e) \\
&= N\gamma^2 P(|Z| > C_e) P(|Z| > C_x)
\end{aligned} \tag{2.95}$$

where $P(Z > \alpha)$ is defined by equation 2.91. By using the result from equation 2.93, the equivalent of equation 2.70 can be derived:

$$E\{|G_{n+1}|^2\} = E\left\{\left(|G_n| - \frac{2\gamma}{\pi} \exp\left(-\frac{C_e^2}{2} - \frac{C_x^2}{2}\right)\right)^2 + |Q_n|^2\right\} \tag{2.96}$$

Substituting for $E\{|Q_n|^2\}$ from 2.95 and again substituting $|G_\infty|$ for $|G_n|$ and $|G_{n+1}|$ leads to an expression for the final expected misalignment vector length:

$$\begin{aligned}
E\{|G_\infty|\} &= \frac{\gamma}{\pi} \exp\left(-\frac{C_e^2}{2} - \frac{C_x^2}{2}\right) \\
&\quad + \frac{N\pi\gamma}{4} \exp\left(\frac{C_e^2}{2} + \frac{C_x^2}{2}\right) P(|Z| > C_e) P(|Z| > C_x)
\end{aligned} \tag{2.97}$$

For long transversal filters, the first term in this expression will be negligible. Hence, comparison with equation 2.71 shows that the addition of mid-tread quantizations results in multiplication of the expected steady state misalignment vector length by a factor of approximately $\exp\left(\frac{C_e^2}{2} + \frac{C_x^2}{2}\right) P(|Z| > C_e) P(|Z| > C_x)$ (assuming that the transversal filter has many taps).

Substitution shows that this factor has a maximum value of unity at $C_x = C_e = 0$ and decreases monotonically as C_x and C_e are increased. Therefore, ERLE will be increased as the mid-tread thresholds are raised.

This benefit must be traded off with the increased convergence time inferred from equation 2.93 and will be limited by quantization errors due to finite coefficient register widths. The tradeoff between ERLE and convergence speed will be a major focus of the analysis by computer simulation presented in Chapter 3.

It is expected that similar advantages can be gained through the addition of mid-tread quantizations to the companded coefficient scheme. The benefit gained through input signal mid-treading will however, be somewhat masked by distortion of the correction vector's direction due to the μ -law coding. Such distortion is difficult to quantify since it is channel (impulse response vector) dependent.

The assertions made regarding the effects of mid-tread quantizations will be substantiated via computer simulation in Chapter 3.

2.8 Performance Advantage of Sampled Analog over Digital Architecture

The majority of reported echo canceller designs [1,2,7,19] use companded PCM input coding. The Bell Laboratories echo canceller for example, uses μ -law PCM at both the input and the echo ports ($x(n)$ and $y(n)$ respectively). It is well known that the standard μ -255 PCM code theoretically provides a constant signal-to-quantization noise ratio of approximately 38 dB [18]. (Practically speaking, about 33 dB to 35 dB

is a better estimate). Thus both the synthesized echo model and the quantized true echo will display this signal-to-noise ratio.

Since the two signal levels involved will be approximately equal, a composite noise floor approximately 35 dB below the input echo (or higher) will result from the subtraction at the cancellation node. This uncorrelated noise cannot be attenuated by the adaptive canceller. In addition, it will generally tend to disturb of the system identification process [5].

Therefore the theoretical maximum ERLE which can be achieved by a canceller of this type is 35 dB, assuming infinite coefficient resolution and an ideal system identification algorithm. In the canceller described in [1], other system limitations limit the expected ERLE to 27 dB.

In a sampled analog echo canceller of the type described in this thesis, no input signal quantization occurs. Hence the major factors limiting the attainable ERLE are coefficient quantization effects and identification algorithm nonidentities, assuming that the analog system's noise floor is negligible. This fact can lead to the design of high performing cancellers, even with significantly reduced coefficient register resolution.

2.9 Summary

This chapter presented a closed form model of the system identification process using algebraic sign correlation. In addition it proposed and mathematically justified methods by which the characteristics of such an algorithm can be improved to make its

performance more competitive with that of reported systems which use the superior gradient algorithm. The suggested modifications were:

- a) companded coefficient storage,
- b) mid-tread quantization of the input and error signals.

A mathematical rationalization for the proposal that sampled analog signal processing can result in improved echo canceller performance was also presented.

CHAPTER 3

ECHO CANCELLER COMPUTER SIMULATION

3.0 Introduction

In Chapter 2, the classical gradient algorithm for system identification was analyzed and compared to a simplified adaptation strategy which is better suited for integration into the system architecture described in Chapter 1. A boldly approximate closed form analysis of the simpler algorithm indicated that its performance is generally inferior to that of the gradient algorithm. Methods were then proposed for making its performance more competitive without significantly increasing hardware requirements.

In this chapter, the validity of the approximate mathematical analysis will be verified via a computer simulation. The merits of the proposed improvements for the simplified algorithm will then be evaluated using the simulation, in order that a strategy which is more competitive with the gradient algorithm can be contrived.

3.1 Transversal Filter and Channel Simulation

The system which the computer simulation must emulate is shown in Figure 3.1. A random input sequence $x(n)$, with an approximately Gaussian pdf was simulated by adding 12 approximately uniformly distributed random numbers as described in [21]. The component random numbers were generated by methods described in [3].

In addition to this generator, a second input generator was provided which put the Gaussian random numbers through a recursive

Figure 3.1: System Emulated by Computer Simulation

difference equation. The difference equation used was derived by performing an impulse invariant, continuous time to discrete time transformation [22] on a standard second order transfer function with 10 rad/sec (≈ 600 Hz) natural frequency and a damping factor of 0.1. This high Q filter was intended to correlate adjacent input samples, producing a semi-periodic result similar to that which might be observed for vowel sounds in human speech. The filter function was normalized so that it had unity power gain. The correlated input feature was included to test the claim made in [2] that mid-tread quantizations tend to improve convergence properties in the presence of such inputs.

The linear system used to produce the simulated echo, $y(n)$, had the sampled impulse response of a typical hybrid transformer given in [3]. In this way an environment simulating that which might be encountered at a 2-wire/4-wire interface in the telephone network was created.

A 64-tap adaptive transversal filter was simulated since this was the length employed in the laboratory model to be described in Chapter 5. Its output, $\hat{y}(n)$, was subtracted from that of the simulated echo to form the error signal, $e(n)$, during each sampling interval. This error signal was then used along with the 64 input samples stored in the filter to perform coefficient adaptation.

3.2 Adaptation Algorithms Simulated

Four tap weight adaptation algorithms were simulated. In each case every filter coefficient was adjusted once during each sampling period using the strategy:

$$\hat{h}(k)_0 = 0.$$

$$\hat{h}(k)_{n+1} = \hat{h}(k)_n + f(x(n-k), e(n)) \quad (3.1)$$

Here $f(x(n-k), e(n))$ is the tap weight correction function for the adaptation strategy being examined. The algorithms of interest are listed along with their related correction functions in Table 3.1. The nonlinear functions, ϕ_x and ϕ_e in the last entries are mid-tread quantization functions for the input samples and error signal respectively and can only take on values of 0 or ± 1 as described in Section 2.7. Power values for calculation of quantization thresholds were approximately calculated using the average of the past 64 squared input and error signal samples. Coefficient quantization in v-255 format was simulated as described in [18] for the last algorithm.

3.3 Program Input and Output

Input parameters for each run of the simulation includes first an algorithm code; 1, 2, 3 or 4, identifying in order, which of the four algorithms from Table 3.1 is to be employed. Next the value of the weighting constant, BETA (input value ignored for fourth algorithm) and a code identifying the type of input signal desired are required. The input signal code is set to 1 if a white Gaussian input is desired or 2 for the filtered noise input.

Output from the simulation includes misalignment vector length at various times during the convergence process, and an estimate of the Echo Return Loss Enhancement (ERLE), at the end of the simulation, calculated using the equation:

ALGORITHM	CORRECTION $f(x(n-k), e(n))$
1. Gradient Algorithm	$BETA * x(n-k) * e(n),$ BETA = an adjustable constant
2. Fixed Magnitude Correction Algorithm	$BETA * SGN [x(n-k) * e(n)],$ BETA = an adjustable constant
3. Fixed Magnitude Correction Algorithm With Mid-Tread Quantization	$BETA * \phi_x * \phi_e,$ BETA = an adjustable constant ϕ_x, ϕ_e are mid-tread quantizations detailed in Figure 2.4
4. Companded Storage Algorithm With Mid-Tread Quantization	$\psi * \phi_x * \phi_e,$ ψ = least significant possible adjustment of ψ -law code, ϕ_x, ϕ_e are mid-tread quantizations detailed in Figure 2.4

⊙ Approximations $\sigma_e^2 \simeq \sum_{i=0}^{N-1} e(n-i)^2 / N$ and $\sigma_x^2 \simeq \sum_{i=0}^{N-1} x(n-i)^2 / N$ are used in implementing ϕ_e and ϕ_x .

Table 3.1: Simulated Algorithms And Their Coefficient Corrections

$$ERLE \approx 10 \cdot \log_{10} \left(\frac{\sum_{p=0}^{N-1} y^2(n-p)}{\sum_{p=0}^{N-1} e^2(n-p)} \right) \quad (3.2)$$

This equation compares the average power of the error signal with the average power of the echo over the past N sampling instants to form an estimate, in decibels, of the amount by which the canceller attenuates the echo.

A listing of the FORTRAN program used to model the entire echo canceller is provided in Appendix A. The program was modified to list outputs after every 200 iterations for generation of Figures 3.4 and 3.5 (to be described below).

3.4 Results

Many simulation runs were performed for each adaptation algorithm so that their relative merits could be judged. The salient results are listed below.

3.4.1 Fixed Magnitude Correction Algorithm Results

Asymptotic approximations of misalignment vector length versus time for fixed correction sizes of .001 and .002 are illustrated using dashed lines in Figure 3.2. These curves were constructed using equation 2.66 for converging portions and equation 2.71 for the steady states. The initial length of the misalignment vector in each case is approximately 1.4, which is equal to the length of the channel impulse vector used, since all tap weight estimates are initially zeroed.

Figure 3.2: Misalignment Vector Length versus Time. This Figure Compares Asymptotic Approximations from Chapter 2 with Results Obtained from Computer Simulation with Linear Coefficient Coding

The solid curves plotted on the graph were generated using results from computer simulation of algorithm 2 from Table 3.1. Their proximity to the predicted mean curves supports the validity of the model derived in Section 2.4 and thus its underlying assumptions and the conclusions derived from it.

3.4.2 Results for Companded Coefficient Algorithm Without Mid-Tread Quantization

Results obtained from the computer simulation using approximate μ -law coefficient coding and without mid-tread quantization (mid-tread quantization thresholds zeroed) are plotted in Figure 3.3. Note that the convergence process is essentially complete within 1000 iterations (125 ms for an 8 kHz sampling rate).

Equation 2.87 predicts a steady state expected misalignment vector length of approximately 0.16 for this system. This agrees well with the average value of the last 10 simulation results which is 0.168, and supports the validity of the model derived in Section 2.6.1.

The steady state ERLE provided by the canceller here is approximately 20 dB which does not compete favourably with existing commercial cancellers [1,2]. Its relatively fast convergence speed however, implies that there is room for trading off convergence speed for improved steady state cancellation as described at the end of Section 2.7.

A simulation run performed with fixed increment adjustments, equal to those which would be used with a linear coefficient storage code having the same number of bits as the μ -law code (8 bits), showed convergence time which was similar to that of the μ -law scheme. The

Figure 3.3: Misalignment Vector Length versus Time from Computer Simulation with ν -law Coefficient Coding and without Mid-Tread Quantization

steady state ERLE was, however, approximately 9 dB poorer. This supports the use of a companded code over a linear one having the same number of bits.

3.4.3 Results of Adding Mid-Tread Quantization

Mid-tread quantization functions were added to both the linear (with $\beta = .001$) and companded versions of the simplified algorithm to test the assertions made in Section 2.7. In each case, centre clipping of $x(n-k)$ was first introduced with C_x (see Figure 2.4) set to 1.42 as suggested in [2]. Centre clipping of $e(n)$ was then added with C_e set to 0.5. This value of C_e was chosen experimentally so that the convergence time would not exceed the 10,000 iteration time period covered by the simulation when linear coefficient coding was simulated.

The results of these runs are plotted in Figures 3.4 and 3.5. The vertical scales are logarithmic so that differences in the steady state misalignment vector length can be clearly seen. Steady state ERLE is indicated for each run.

The ERLE values from Figure 3.4 are deceptively high. Recall that since fixed increments are used in this case, these values are indicative of channel independent residual echo. Thus, if the simulated 4-wire return loss dropped from the -6 dB level (impulse response has 6 dB of gain) used in the simulation, to a more realistic 10 dB, approximately 16 dB would be subtracted from each of these levels. As discussed in Section 2.5, this effect is reduced when μ -law coding is applied.

Table 3.2 compares steady state misalignment vector lengths and convergence times from the computer simulation results with results

Figure 3.4: Misalignment Vector Length versus Time from Computer Simulation with Linear Coefficient Coding showing Effects of Adding Mid-Tread Quantization

Figure 3.5: Misalignment Vector Length versus Time from Computer Simulation with ψ -law Coefficient Coding showing Effects of Adding Mid-Tread Quantization

Parameter	C_x	C_e	Equation(s) Required For Calculation	Calculated Value	Value from Computer Simulation
Steady State Misalignment Vector Length	0 1.42 1.42	0 0 0.5	2.71 2.97 2.97	.0503 .0223 .0152	.0506 .0217 .0174
Convergence Time (Iterations)	0 1.42 1.42	0 0 0.5	2.67 2.67, 2.93 (see text) 2.67, 2.93 (see text)	≈ 2200 ≈ 6000 ≈ 6800	≈ 2500 ≈ 6500 ≈ 7200

Table 3.2: Comparison of Results from Computer Simulation with
Calculated Predictions for Linear Coefficient Coding
($\beta = .001$) with Mid-Tread Quantization

predicted from equations derived in Chapter 2 for a system with linear coefficient coding. Each misalignment vector length from the simulation is actually the average of the last 10 output values. Convergence times were calculated using the slowing factor $\exp(-\frac{C_e^2}{2} - \frac{C_x^2}{2})$ described following the derivation of equation 2.93. The comparisons listed support the validity of approximate equations from Chapter 2 and, along with Figure 3.4, illustrates the tradeoff between steady state echo cancellation and convergence time which is characteristic of this scheme.

Table 3.3 lists computer simulation results, similar to those in Table 3.2, for a system with μ -law coefficient coding. These results in conjunction with Figure 3.4 illustrate that a tradeoff between steady state cancellation and convergence time is also apparent in this case although accurate mathematical predictions are difficult to derive.

The ERLE improvement due to input centre clipping is only 2.8 dB for the companded system, substantially less than the 10 dB observed for the system with linear coefficient coding. This is attributed to the distorting effect of the μ -law on both the magnitude and direction of the correction vectors.

The ERLE improvement due to error signal centre clipping is 3.6 dB for the linear coding case and 2.7 dB for the companded case. From these results it might be conjectured that this method of ERLE improvement is less sensitive to the distorting effect of the μ -law coding than the previous method.

Parameter	C_x	C_e	Value from Computer Simulation
Steady			
State	0	0	0.168
Misalignment	1.42	0	0.0934
Vector			
Length	1.42	0.5	0.0735
Convergence	0	0	≈ 1000
Time	1.42	0	≈ 2200
(Iterations)	1.42	0.5	≈ 2400

Table 3.3: Results of Computer Simulation for ψ -law Coefficient
Coding with Mid-Tread Quantization

3.4.4 Performance with Filtered Noise Input

Simulation runs like the ones listed above were also performed using the filtered input option. In each case the relative performance under varying operating conditions yielded results similar to those observed with the white noise input. These results are not in agreement with the claim made in [2] that mid-tread quantization functions of the type used here tend to decorrelate adjacent input sample and hence improve convergence characteristics for correlated inputs.

3.4.5 Potential for a Commercially Competitive Echo Canceller Design

Figure 3.6 shows the measured convergence curve of the Bell Laboratories VLSI echo canceller obtained from [1]. Superimposed on this graph is the convergence curve, generated by computer simulation, for a μ -law coded echo canceller with mid-tread quantization. With C_x and C_e set equal to 1.6 and 0.75 respectively this canceller competes with the VLSI canceller both in terms of convergence time and steady state echo return loss enhancement. The steady state ERLE generated from this particular run was approximately 29 dB.

It is therefore proposed that a canceller using this exceedingly simple identification algorithm with the architecture described in Chapter 1 can compete in the same marketplace as existing digital cancellers.

3.5 Conclusions

The results obtained from the above simulation runs support the accuracy of the mathematical models used in Chapter 2 in describing

Figure 3.6: Comparison of Convergence Characteristic of Mid-Tread Quantized ν -law Algorithm with that of the Bell Laboratories Cancellor [1]

the relative performance of systems having companded and linear coefficient coding schemes. They also confirm the effectiveness of mid-tread input and error signal quantization functions in improving steady state echo cancellation as predicted.

CHAPTER 4

EXISTING TECHNOLOGY FOR ANALOG SIGNAL PROCESSING

4.0 Introduction

The analyses presented in Chapters 1 and 2 have assumed the existence of an ideal signal processing structure which convolves a set of digital tap weights with analog input samples. A number of approaches aimed at realizing such a structure have been demonstrated [2,11,13,14,15,16] with varying degrees of success.

Since it is intended that the advantages of the mixed analog/digital scenario for echo canceller design be proven in a practical context, an overview of the technologies available for realization of such a processor will be an essential component of this thesis. This chapter is intended to provide such an overview as well as a description of the structure chosen for use in the laboratory model.

4.1 Convolution Processor Design Approaches

The convolution sum of products

$$\hat{y}(n) = \sum_{k=0}^{N-1} \hat{h}(k) x(n-k) \quad (4.1)$$

contains components related to each of the N past input signal samples. The convolution processor therefore must contain N analog storage locations; one corresponding to each of the components of the summation.

The fact that the sampling instant, n , appears in the argument of the input sequence but not the impulse response sequence implies a relative shifting of the two by one sample per sampling instant. This relative shifting operation can be equivalently realized by holding impulse response samples at fixed locations in the processor and moving analog input samples past them, or by holding past input samples in fixed locations and moving the impulse response samples.

4.1.1 Reported Architectures with Shifting Analog Samples

In the moving analog sample scheme, signal storage (weighted or unweighted) is realized using analog delay lines. Such structures have been most effectively realized using charge transfer techniques in the form of charge coupled devices (CCD's) or bucket-brigade devices (BBD's). These design approaches are illustrated in Figure 4.1.

In the classical CCD delay line, shown in Figure 4.1a), overlapping clock phases (ϕ_1 , ϕ_2 and ϕ_3) produce a moving potential well in which surface charge, representative of an input sample, is carried. Inherent in this structure is the lack of established circuit nodes at which measurement or adjustment of charge packets can be accomplished. For this reason modified electrode configurations (added sensing electrodes for example) complicate the basic design when convolution with digital coefficients is desired.

The early realization of the BBD illustrated in Figure 4.1b) has operating principles similar to those of the CCD except for one additional detail. Whereas all stored charge is lost if CCD clocks are disabled, it will be stored in the fixed capacitance between electrode and n -diffusion in the case of the BBD. Hence, non-overlapping, 2-phase

(a) Classical CCD Structure (Metal Gate)

(b) Classical BBD Structure (Metal Gate)

Figure 4.1: CCD and BBD Delay Lines

clocks can be used to direct charge flow. Note that the diffusion (*) forms a convenient circuit node for modifying or measuring stored charge. A more popular BBD design than that shown in Figure 4.1 is fabricated using a self aligning silicon gate process, but operates similarly to the one pictured.

Several convolvers which employ moving analog sample techniques have been described in recent literature. In the system reported in [13], M parallel CCD delay lines are used to realize a transversal filter with M-bit coefficient accuracy as shown in Figure 4.2a). Here binary weighting is accomplished at the input to each CCD. Sensing electrodes and circuitry are also included after each unit stage. A 1XN bit storage register, which stores one bit of the coefficient representation, is associated with each CCD. Placing a logical zero in one of the memory locations changes the charge transfer timing for the associated CCD cell so that its stored charge does not reach the sensing node while the output summer is sampling. A logical one, however, allows properly timed sensing and summing. This combination of binary input weighting for the CCD's, +1 or 0 multiplication at the sensing nodes and output summing is thus equivalent to multiplication of input samples by digital coefficients and summing.

Another approach, which is detailed in [14], is illustrated in Figure 4.2b). Here, all of the multiplications using the present input sample, which are required to calculate components of the next N filter output samples, are performed simultaneously using multiplying digital-to-analog converters (MDAC's). N-BBD delay lines of varying lengths then channel the products to the output summer in the appropriate order.

(a) Parallel CCD for Each Coefficient Bit Position as described in [13]

(b) Parallel BBD for Each Required Delay as described in [14]

Figure 4.2: Reported Moving Sample Convolvers

Both of the above architectures are capable of high speed signal processing (up to 1 MHz for the system described in [13]) because of their pipelined architectures. This capability however, is bought at the expense of excessive die size due to the inclusion of several delay lines with related control circuitry. Since echo cancellation for voice communication can be done effectively at an 8 kHz sampling rate, [1] the capability for such high speed processing is unnecessary.

The convolver described in [11] uses a single, multiplexed MDAC to effectively replace the array of MDAC's shown in Figure 4.2b). In this way it trades off speed to reduce circuit size and power dissipation. In addition it employs a unique scheme by which MDAC outputs can be easily injected at different positions along a single delay line, skirting the need for delay lines of various lengths. Since this particular structure is the one employed in the laboratory model echo canceller, a more detailed description of its operation will be saved for later sections in this chapter.

4.1.2 Reported Architectures with Moving Coefficients

Processor architectures based on shifting of the discrete impulse response generally store each input sample in a fixed location in a sample and hold (S&H) array for N sampling periods. Digital shift registers are then used to move the impulse response samples past the array.

In the system described in [16], for example, digital tap weights are shifted through a binary area-ratioed capacitor array as shown in Figure 4.3. This array links the weights to the stationary S&H sites and is the multiplying structure in the filter. The device

Figure 4.3: Moving Tap Weight Structure described in [16]

described in [15] operates in a similar manner, but multiplexes a single MDAC to do all of the related multiplications.

Processors of this type generally write the most recent input sample for the S&H array over the oldest one, which was sampled N periods earlier. The first impulse response sample is then forced to follow the location of the most recent input sample via the shifting process. This operation results in movement of the coefficients in a circular fashion with respect to the S&H array so that the array and the coefficients overlap in the same way every N sampling periods. Under such conditions, non-uniformities across the S&H array and the array/multiplexer interface result in a periodic noise component with a fundamental frequency of f_s/N . This is the mechanism which limits the dynamic range of such filters and is referred to as Fixed Pattern Noise (FPN).

As will be explained in the next section, dynamic range is of paramount importance in the design of a PTF to be used for echo cancellation. For this reason, the moving analog sample method of convolution may be desirable over the moving coefficient scheme because of its FPN immunity.

4.2 Importance Of Dynamic Range In Echo Canceller PTF's

The ability of an echo canceller to maintain good ERLE over a wide range of input and echo power levels will largely determine how competitive it is with existing systems. The Bell Laboratories echo canceller for example is able to maintain a minimum 22 dB of ERLE over a 20 dB input power range and 12 dB range of 4-wire return loss [1]. Thus the limiting noise floor of this system must be separated from the

maximum white noise signal level by at least the sum of these figures or 54 dB.

This fact can be clarified by referring the standard echo canceller characterization setup shown in Figure 4.4. The amount by which the power of $e(n)$ is attenuated with respect to $y(n)$ ($\propto \hat{y}(n)$) defines the ERLE of the canceller. If $y(n)$ is attenuated first 20 dB at A, then 12 dB at B with respect to the maximum canceller output, $\hat{y}(n)$ will be forced to come 32 dB closer to its noise floor. Although the noise floor for $\hat{y}(n)$ propagates through the summer, the signal output $e(n)$ is lower than $\hat{y}(n)$ by the ERLE of the canceller. Hence, if the sum of the above 32 dB and the ERLE which the system is capable of providing in the absence of noise, forces $e(n)$ to the noise floor, measured ERLE will degrade.

Furthermore, the simulated channel response in Figure 4.4 is dispersionless. Thus the dynamic range which must be specified here is the so called "dynamic range per tap" [15]; that is the dynamic range of the PTF with one tap weight at a maximum and the rest zeroed. Therefore, signal amplification over noise via the tap weight settings (impulse response power) cannot be exploited.

Dynamic range per tap reported for sampled analog PTF's in recent literature ranges up to about 50 dB [15] which approaches the 54 dB benchmark set by the digital version. The device described in [13], in contrast, provides only 33 dB and would not be competitive for echo cancellation.

4.3 PTF Chosen For Echo Canceller Laboratory Model

The PTF used for construction of the laboratory model was

Figure 4.4: Recommended Test Configuration for Characterizing ERLE

based on the unique BBD structure described in [11]. The BBD was supplied, on a chip, by its developers at Universiteit Leuven, Belgium. The system design for this chip was supervised by Professor M.A. Copeland of Carleton University while on sabbatical in Belgium.

A block diagram of a PTF built using this chip is shown in Figure 4.5. Stored digital coefficients are multiplied in reverse time order by each input sample. The multiplications are carried out by a single multiplexed MDAC. The resulting serial products are sequentially channelled into the appropriate stages of a 64 stage BBD via a row of dynamic amplifiers. A digital shift register is used to control the multiplexing of the MDAC output across the dynamic amplifiers which add charge to the BBD cells in proportion to these products. Each time all of the charge packets related to one input sample have been loaded, the contents of the BBD are advanced over one cell.

This parallel in - serial out approach to the convolution calculation is similar to the approach employed by the system in Figure 4.2b). It replaces the entire row of MDACs with a single multiplexed device and replaces N ($N=64$) delay lines of different lengths and an output summer with a single tapped delay line (BBD) having a summing node (dynamic amplifier) at each tap.

Only the portion of the block diagram enclosed by the rectangle was included on the supplied chip.

This particular PTF was chosen for the following reasons:

- 1) It had more taps than most readily available devices ($N=64$).
- 2) Its simplicity and low power dissipation (25 mW) made its design a strong candidate to be included in a future, fully integrated echo canceller.

Figure 4.5: Block Diagram of PTF used for Laboratory Model Echo Cancellation

- 3) Since the MDAC was supplied externally, a commercial companded MDAC could be used for experimentation.

4.3.1 Dynamic Amplifier Operation

Use of a dynamic amplifier for sampled data charge integration was first proposed in [12]. The circuit consists of a MOS transistor and a simple set of switches and saves power and chip area in comparison with static operational amplifiers. The use of a dynamic amplifier in a simple switched-capacitor integrator is illustrated in Figure 4.6.

The analog input signal is first sampled on ϕ_1 , placing the charge $C_1 V_1$ on the input capacitor. ϕ_2 and ϕ_3 (with ϕ_1 off) then allow the gate of Q_1 to be pulled above its threshold voltage, V_T , via capacitive coupling through C . Finally, only ϕ_3 and ϕ_4 are enabled so that node A begins to discharge from V_{dd} towards ground. Again, because of C , the gate voltage of Q_1 also moves towards ground until it reaches V_T and turns the transistor off.

Since the voltage across C_1 starts at V_1 and finishes at V_T , the charge transferred to C from C_1 through the above process is $-C_1 (V_1 - V_T)$. Therefore, if the input is biased around V_T , integration of charge on to C , in proportion to the input signal voltage, results. In order to create an operating range which is symmetrical about the biasing level, the threshold voltage of Q_1 is set to approximately half of V_{dd} .

4.3.2 Combining Dynamic Amplifiers With The Classical BBD

Realization of the parallel in-serial out convolution process described in Section 4.4 requires the ability to add or subtract well

Figure 4.6: Use of a Dynamic Amplifier in a Switched Capacitor Integrator

defined quantities of charge from each BBD cell. This is simply and effectively accomplished by combining each two-stage cell with a dynamic amplifier as shown in Figure 4.7, with the clock timing detailed in Figure 4.8.

The transistor of the second clock phase of the BBD is not clocked directly but rather switched on and off by ϕ_2 and ϕ_5 respectively. The first stage of the BBD is clocked by ϕ_1 and is no different from the standard structure.

Biased output products from the MDAC are clocked into successive cells of the circuit via multiplexing clocks, ϕ_{Mk} ($k = 1, 2, 3, \dots, 64$). The biased charge corresponding to the product of the most recent input sample and the k^{th} tap weight (tap weights in reverse order here) is thereby stored on the input capacitor for the k^{th} cell, C_{1k} . With the input charge stored on C_{1k} , ϕ_2 , ϕ_3 and ϕ_4 are sequenced in the same way described for the simple switched capacitor integrator, to sum the signal component ($(N-k) \times (n)$) of this charge into capacitor C_{2k} . The total charge which is transferred to C_{2k} by the end of ϕ_4 is the sum of the charge taken from C_{1k} on ϕ_2 through the standard BBD action and the new convolution component from the dynamic amplifier action. Finally ϕ_5 causes one side of C_{2k} to be pulled to V_{dd} so that this total charge may be transferred to the next cell when ϕ_1 goes high.

Figure 4.7: Combining Classical BBD Cell with a Dynamic Amplifier

Figure 4.8: Clocking for BBD with Dynamic Amplifiers

4.3.3 Synchronization of On and Off-Chip Functions

Clearly, proper operation of the PTF chip depends on the ability of external circuitry to provide each convolution component from the MDAC to the analog bus in synchronism with the related multiplexing clock, ϕ_{Mk} . The multiplexing clocks themselves are developed on-chip by the digital shift register shown in Figure 4.4. It is a two phase, 64-stage dynamic circuit and is clocked externally using the scheme detailed in Figure 4.9.

Just prior to the first multiplexing signal (t_0) a pulse is sent to the input of the shift register via the in-SR line. This pulse then propagates through one stage of the shift register for each positive pulse on either the ϕ_1 -SR or ϕ_2 -SR clock. Therefore, the output from each of the 64 shift register stages forms one of the multiplexing clocks directly.

In order to synchronize the products from the MDAC with the multiplexing clocks, the input signal to the PTF is sampled during ϕ_3 when none of the clocks are active, then held while multiplexing is taking place. The first tap weight is then directed to the digital port of the MDAC on the first ϕ_2 -SR pulse after the in-SR signal. Successive tap weights are directed to the MDAC for every low to high transition of either ϕ_1 -SR or ϕ_2 -SR thereafter until all 64 weights have been paired with the input sample.

A new sample is developed at the output of the PTF on each rising edge of the clock marked S. Since this edge occurs before the input multiplexing process is complete, the output generated during a given sampling period has no component resulting from the most recent input sample in the S&H.

Figure 4.9: PTF Dynamic Shift Register and I/O Clocks.

The clock marked R in Figure 4.8 resets the hold circuit at the output of the PTF and G_1 clocks bias charge into the input of the BBD. The inverse of ϕ_3 is also provided to the chip for internal clock feedthrough reduction purposes.

The pinouts of the filter chip are detailed in Appendix B.

4.4 Summary

An overview of available signal processing technology for realization of sampled analog input convolution with digital coefficients was presented in this chapter. The particular implementation which will be used in the construction of the laboratory model echo canceller was also described.

CHAPTER 5

LABORATORY MODEL ECHO CANCELLER DESIGN

5.0 Introduction

This chapter describes the design of the 64-tap experimental echo canceller, constructed to demonstrate both the implementation of the simplified identification algorithm as described in Chapter 2 and the advantages of the sampled analog architecture. A simplified block diagram approach will be used to describe the system. Detailed engineering schematics are included in Appendix C. The relationship between functional blocks and actual circuit components has been kept sufficiently exact for easy reference.

5.1 System Overview

A block diagram of the echo canceller is shown in Figure 5.1. It is designed to invoke the companded coefficient storage algorithm with mid-tread quantization for the reasons stated in Section 3.4.5. The PTF chip and MDAC combine to convolve stored coefficients from the Tap Weight RAM with the sampled input signal, $x(n)$, as described in Section 4.4. The MDAC itself provides the capability for linearizing companded coefficient storage codes.

Tap weight modifications are performed during each sampling instant for which the error signal sample, $e(n)$, exceeds an adaptive mid-tread quantization threshold. This decision is made by the ENABLE E block in the diagram. Furthermore, only coefficients with related input sample levels exceeding a second adaptive threshold are adjusted. The

Figure 5.1: Laboratory Model Echo Canceller Block Diagram

method used for determining the threshold values will be described in Section 5.5. The second decision is made by the ENABLE X block for each input sample as it enters the processor and is stored as a single bit (high level if the enable condition is satisfied) in the 64-stage ENABLE X SHIFT REGISTER. In this way, decisions related to all 64 of the past input samples used by the PTF chip can be accessed via register recirculation and logically AND'ed with the ENABLE E output to enable the Tap Weight Modifier.

Binary signals representing the algebraic signs of the 64 past input samples are stored in a similar manner in the SGN X SHIFT REGISTER for algorithm implementation. High logic levels are used to represent negative samples both for the hard nonlinearity feeding this shift register and the one operating on $e(n)$.

The direction in which each tap weight should be adjusted is defined by the algebraic sign of the related input signal times error signal product. This is equivalently realized via the EXCLUSIVE OR gate shown. By cyclically accessing the coefficient storage locations in RAM in synchronism with the contents of the two shift registers, the matching of coefficients and adaptation data necessary for the Tap Weight Modifier to increment, decrement or freeze coefficient values is achieved.

5.2 Tap Weight RAM

The 64 digital tap weights are stored in two Intel 2114 static RAM's. Two chips were required since each is capable of storing 4-bit parallel data while 8-bit coefficients are required. The capability to isolate the address and data inputs of these chips from driving logic

was included via TTL TRI-STATE buffers controlled by DIP switches. This feature was intended to facilitate tap weight control using an external microprocessor and was included as a circuit fault detection option. Its use was however, was never required.

5.3 Tap Weight Modifier

A simplified block diagram of the coefficient updating circuit is shown in Figure 5.2. Related clock timing is shown in Figure 5.3. The $\overline{WE}$ line allows the coefficient RAM to be read when it is high and written to when it is low. Counter, U15/16, is preset with the lower 7 bits of a coefficient from the RAM on the rising edge of the LOAD clock. The most significant bit of the coefficient code is the sign bit which cannot be modified simply via the up/down counter. Thus only the coefficient's absolute value is loaded into the counter.

Two logic signals are derived from the stored coefficient. The first signal, SATURATE, detects the condition where a coefficient's magnitude cannot be incremented due to overflow (all seven bits high) and is realized via U17. The second signal, ZERO, determines whether or not the coefficient has minimum possible magnitude (all seven bits low) and is generated by the counter itself. In addition an $\overline{UP/DOWN}$ signal is generated by U20A which determines whether the value in the counter should be incremented or decremented. As shown, the $\overline{UP/DOWN}$ signal is a function of both the direction of adjustment dictated by the identification algorithm and the present sign of the coefficient. It is given a high logic level if decrementing of the coefficient's absolute value is implied. Note that the compliment of this signal is used in the development of the SATURATE signal, to detect the condition where

Figure 5.2: Simplified Tap Weight Modifier Block Diagram

Figure 5.3: Clock Timing for Coefficient Updating Circuitry

maximum magnitude has been reached, although further incrementing is implied.

The UP/DOWN, SATURATE and ZERO signals along with the sign bit of the input coefficient are stored at the output of latch U52, starting on the falling edge of the LOAD clock. A combinational logic block, (U18-20) is then used to invert the sign bit if the input coefficient has zero magnitude, and decrementing is implied to produce the updated coefficient's sign bit. The stored SATURATE signal is used to disable the counter so that it does not overflow.

Gate U19B simply passes the UP/DOWN signal to the counter unless a zero crossing is signalled, in which case the counter is forced to increment. The combination of this and the sign bit inverting feature provides a smooth transition for coefficients passing through zero magnitude.

The rising edge of the ADJUST pulse clocks the counter via U49-51 if the ENABLE signal is low, thereby updating the magnitude of the coefficient. At the same time the updated sign bit is latched into flip-flop U3B and directed to the UPDATED COEFFICIENT BUS, with the new magnitude. The ENABLE signal is generally controlled by mid-tread quantization circuits (ENABLE E and ENABLE X) so that the coefficient can be passed unmodified if the related input or error signal level is too low. It can also be controlled by the coefficient clearing circuit; a feature which will be better explained in later sections.

The positive pulse on the write line allows the modified coefficient to be directed to the RAM data bus so that it can be stored.

Figure 5.4: Convolution Circuit Block Diagram

5.4 Convolution Circuitry

A block diagram of the circuit used to convolve the sampled analog input signal with digital coefficients is shown in Figure 5.4. As described in Section 4.3, each held input sample must be multiplied by all of the stored coefficients serially by the MDAC, then directed to the PTF chip. Unfortunately, the only μ -law MDAC which could be found (PMI DAC-76) would only accept positive analog input currents. Therefore, the input signal was full - wave rectified before being directed to the MDAC. The polarity of the output product was then corrected via an EXCLUSIVE-OR operation using the digital sign bit as shown.

The input magnitude and sign signals for the full wave rectifier are also directed to the mid-tread quantization and coefficient adjustment decision circuits respectively.

5.5 Mid-Tread Quantization Circuits (ENABLE E and ENABLE X)

The block diagram pictured in Figure 5.5 depicts the circuitry which effectively decides which input and error samples are sufficiently large to be considered useful for tap weight adaptation.

The rectified input signal, $|X|$ is made available by the convolution circuitry. Each rectified input sample is compared with an adaptive mid-tread threshold by U43C. The threshold is formed by averaging the rectified input signal with a lowpass filter and amplifying the result. This yields a voltage which is approximately proportional to the RMS level $\langle |X| \rangle = \sqrt{\frac{2}{\pi}} \sigma_X$ for a Gaussian input (for example). The output of U43C thereby logically realizes the quantization transfer function pictured in Figure 2.4a) with:

Figure 5.5: Mid-Tread Quantization Circuitry Block Diagram

$$C_x = G_1 \cdot \sqrt{\frac{2}{\pi}} \quad (5.1)$$

for a Gaussian input, where G_1 is the threshold gain defined by the setting of R_2 . This ENABLE X output must be stored with similar outputs related to the 64 past input samples as will be described in the next section. Only the proportionality constant would change in equation 5.1 in the presence of inputs which are not Gaussian.

Realization of the quantization transfer function for the error signal (θ_e = ENABLE E) as was defined in Figure 2.4b) is similar except that the error signal must first be generated then rectified via U42. The error signal is generated by subtracting the PTF output $\hat{y}(n)$, from the unknown system's response, $y(n)$ (echo). This signal also forms the output of the echo canceller.

The threshold value for the error signal quantization is proportional to the constant:

$$C_e = G_2 \sqrt{\frac{2}{\pi}} \quad (5.2)$$

where G_2 is the gain value defined by the setting of R_1 .

5.6 ENABLE E and ENABLE X Shift Registers

A block diagram of the circuit used to store and access the past 64 SGN X signals, to be used during coefficient updating is shown in Figure 5.6.

The 64-stage shift register itself has a MODE input which permits recirculation of stored data in synchronism with the CLK input

Figure 5.6: SGN X Shift Register Block Diagram

when supplied with a high logic level. This mode of operation is used for reading the register's contents. Supplying the MODE input with a low logic level allows a new sample to be clocked into the first stage and all other stored values to be shifted one position. In this mode, the value originally stored in the last stage is lost.

As shown in the timing diagram in Figure 5.7, clock $\overline{\phi}_5$, which feeds the MODE input, is low while the CLK line receives a single positive pulse. This allows the SGN X logic level stored by flip-flop U39A to be clocked into the shift register. The flip-flop acts as a unit delay element for the SGN X signal coming from the convolution circuitry, due to the relative timing of the input CLK pulse and S. This compensates for the inability of the PTF to generate an output component related to the most recent input sample. (If the PTF output does not contain information related to the most recent sample, then no component of the updating process should be related to that sample).

During the time that $\overline{\phi}_5$ is high and the shift register is in the recirculating mode, 64 positive logic pulses are sent to the CLK input so that the stored data can be read serially. The positioning of data in the shift register is identical before and after this pulse train.

EXCLUSIVE-OR gate U20C logically determines the implied direction of tap weight updating from the shift register's output and the SGN E signal. The ENABLE X shift register functions in a similar fashion to the SGN X circuit. The CMOS shift registers used in these circuits were supplied with +12 volts so that they operated with sufficient speed. Up and down level shifts for interfacing to related TTL circuits were performed using open-collector TTL buffers and bipolar comparators respectively.

Figure 5.7: Timing Diagram For ENABLE E and ENABLE X Shift Registers

5.7 Timing Generation

The master clock frequency for the echo canceller is 6.0 MHz. A simple TTL circuit was used to derive the adaptation circuitry clocks shown in Figure 5.8. The ϕ_c clock, which runs in synchronism with $\overline{WE}$ during adaptation is used to synchronize the PTF related circuitry with the coefficient adaptation circuitry.

As shown in Figure 5.8, ϕ_c is used to clock a synchronous 7-bit counter which cyclically addresses 128 bytes of stored data in an Intel 2716 EPROM. The contents of the EPROM are sampled data representations of eight of the PTF clocks detailed in Section 4.3 (ϕ_1-G_1 , ϕ_2 , ϕ_3-R , ϕ_4 , ϕ_5 , ϕ_1-SR , $in-SR$ and S). The two remaining PTF clocks, ϕ_2-SR and $\overline{\phi_3}$, are generated by inverting ϕ_1-SR and ϕ_3 respectively. The PTF functions controlled by these clocks were detailed in Chapter 4. Clock $\overline{\phi_c}$ is used to trigger latching of the output data from the EPROM so that spurious transitions which occur during access periods do not affect the clocks.

Since ϕ_2 has a frequency of 1 MHz, and the 128 stored bytes in the EPROM represent the clocking sequence for a single PTF sampling period, the system's sampling frequency is approximately 7.81 kHz. This is slightly lower than the 8 kHz telephony standard but is acceptable for experimental purposes.

During the first 64 periods of the ϕ_c clock, the dynamic amplifiers in the PTF chip are being loaded. Since this implies that the filter coefficients must be accessed, no tap weight adaptation is permitted during this time interval. Hence the updating clocks shown in Figure 5.3 are only enabled when the most significant bit of the EPROM address counter is high (the last 64 periods of ϕ_c in that sampling period). Since one period of the sequence detailed in Figure 5.3 occurs

Figure 5.8: PTF Timing Generator Block Diagram

for every period of ϕ_c , the adjustment of all 64 tap weights is permitted during the last 64 periods.

The six least significant bits of the EPROM address counter, are used to address the coefficient RAM chips. Thus all of the 64 coefficient storage locations are accessed twice per sampling period; once for dynamic amplifier loading and once for coefficient updating. In addition, the 64 shift register CLK pulses shown in Figure 5.7 which occur during the second half of the sampling period are synchronized with $\overline{\phi_c}$. This guarantees that $SGN\ X$ and $ENABLE\ X$ signals are accessed at the same time as the related tap weights for adaptation.

The clocking voltages required for the NMOS PTF chip are higher than those available from the TTL timing circuits (see Appendix B). Therefore, TTL buffers with open-collector outputs were required to perform level shifts for most signals. The exceptions were ϕ_3 and $\overline{\phi_3}$ which required -5 Volt low levels as well as +12 Volt high levels. Bipolar comparators (LM339) supplied with these voltages were used to satisfy such requirements.

5.8 Coefficient Clearing

It is desirable to start the echo canceller convergence process with all coefficients set to zero. In this way, initial 4-wire return loss degradation due to added echo from a nonzero PTF transfer function can be avoided.

The ability to zero the digital tap weights was provided indirectly using the existing adaptation circuitry. A DIP switch was used to control a simple set of gates which enabled the following functions:

- 1) Forced the ENABLE line to the updating counter in the Tap Weight Modifier (Figure 5.2) low so that the mid-tread quantization features could not prevent coefficient adjustment.
- 2) Forced the SGN X input to the SGN X Shift Register (Figure 5.6) high, thereby driving the related input of U20C high independent of input sample polarity.
- 3) Directed the input coefficients sign bit to the other input of U20C.

With one input to EXCLUSIVE-OR gate U20C forced high, its output is simply an inverted version of the other input; the coefficient sign bit. Since this output signal is used by the Tap Weight Modifier to determine the direction of coefficient correction, negative input coefficients are forced to be adjusted in the positive direction and positive coefficients are forced to be adjusted in the negative direction. Hence all tap weights are forced virtually to zero except for oscillation in the least significant bit positions. The effects of this oscillation are totally masked by the noise floor of the PTF.

CHAPTER 6

RESULTS

6.0 Introduction

This chapter presents experimental results obtained from the laboratory model echo canceller. Some attention has been focussed on producing results which could be compared to those obtained from literature describing existing digital cancellers available commercially.

6.1.1 Echo Return Loss Enhancement Test procedure

The ERLE test apparatus pictured in Figure 6.1 was designed to emulate standard test set-ups described in [1] and [2].

A white noise input, bandlimited at 3.4 kHz, was generated by combining a pseudo-random noise generator chip with a Northern Telecom antialiasing filter module. The echo itself is assumed to be an attenuated version of the input signal. Residual echo ($e(t)$) is measured using a C-message weighted noise meter.

Residual echo power is measured first with all filter coefficients zeroed, then after the canceller has been allowed to converge for approximately 1 second. The difference between these two measurements, in dB, is the ERLE provided by the canceller. Note that 15 dB of gain was added at the output of the PTF so that the range of the tap weights would not be exceeded for the return loss test values recommended in the literature (difference between input and echo signal power).

Figure 6.1: Test Configuration for Measuring Laboratory Model ERLE

The delay in the echo path was introduced to compensate for the unit delay inherent in the PTF design (see Section 4.4.3).

6.1.2 Echo Return Loss Enhancement Test Results

Measured ERLE with 6 dB of channel return loss as a function of input power is plotted in Figure 6.2. Also pictured is the equivalent curve for a canceller marketed by COMSAT [2] which has similar digital coefficient representation and a similar adaptation strategy but uses a companded PCM code to store input samples.

The superior performance of the experimental canceller in terms of ERLE over the upper 20 dB of input signal range supports the argument that improved performance can be achieved by replacing digital input signal representations with analog storage.

Values of C_x and C_e were set to 1.6 and 0.75 respectively, similar to the canceller simulated in Section 3.4.5 for this experiment.

Degradation of the canceller's performance below the upper 10 dB of input signal range is due to the noise floor of the PTF. Since the power at the cancelled output clearly cannot be lowered below the system noise floor, ERLE drops in proportion to input signal power below this range.

These measurements imply a usable dynamic range per tap of approximately 40 dB for the PTF, by the reasoning described in Section 4.3. This is approximately 19 dB lower than the dynamic range reported by the designers of the PTF chip [23]. The discrepancy is attributed to two factors:

- 1) Due to the low gain transfer function used (recall that $[\text{PTF power gain}] = \sum \hat{h}_1^2$), the maximum usable signal

Figure 6.2: Comparison of ERLE Provided by Experimental Cancellor with that Provided by the COMSAT Cancellor [2]

level was limited by the PTF input circuit rather than the output source follower as reported in [23]. Hence the maximum achievable output signal level was only 0.6 volts peak-to-peak compared with the 3.35 volts reported. The input signal was limited to approximately 4 volts peak-to-peak by the full wave rectifier MDAC combination. The dynamic range lost here is approximately 15 dB.

- 2) The white noise input signal used has a peak-to-RMS ratio which exceeds that of a sinusoidal input by approximately 6 dB. (Maximum sinusoidal input is generally used as a reference to dynamic range measurements.) Hence about 6 dB of top end dynamic range is lost due to the white noise input. (Total dynamic range loss is $15 \text{ dB} + 6 \text{ dB} \approx 21 \text{ dB}$).

The transfer function used here had power gain which is typical of that which might be encountered in telephone network applications [2]. Certainly, unity power gain could never be exceeded in systems involving passive hybrids. Hence it would be practical to increase the size of the dynamic amplifiers' input capacitors to increase the signal gain provided by the PTF. Since the analysis presented in [23] shows that the noise floor is dominated by BBD charge transfer effects, charging these capacitors would not significantly affect the noise measurement. Thus dynamic range would increase.

The limitation imposed by the rectifier/MDAC combination was identified following completion of the characteristics described in this chapter. This limitation could have been eliminated had some of the input circuitry been redesigned. (This is independent of the PTF chip

itself.) Such a modification would have provided between 6 dB and 8 dB of additional dynamic range, and might yield an ERLE characteristic similar to that traced by the dashed line in Figure 6.2. The improvement assumed for construction of the curve is 6 dB.

The echo canceller's performance also exceeded that reported for the Bell Laboratories VLSI canceller by between 1 dB and 3 dB over the upper 10 dB of the input signal power range [1]. The Bell Laboratories canceller combines a companded PCM input code with much more precise (16 bits as described in [20] is assumed) coefficient representation than the experimental canceller. This result is therefore supportive of the conjecture that the benefits derived from unquantized input sample storage can be used to trade off coefficient register width.

It should be noted that the VLSI canceller is capable of maintaining 22 dB of ERLE with input signal and channel attenuations of 20 and 12 dB respectively (total echo attenuation of 32 dB). Such performance could not be achieved by the experimental canceller due, again, to the dynamic range limitation.

6.2.1 Convergence Time Test Procedure

Echo canceller convergence time was estimated by placing a storage oscilloscope at the output ($a(t)$) of the canceller and triggering its sweep at the beginning of the adaptation process. An example of the type of stored trace generated using this procedure is shown in Figure 6.3. The canceller convergence time is approximated as the time required for the output (residual echo) to decay to a steady state.

Figure 6.3: Storage Oscilloscope Trace Showing Decay of Residual Error
versus Time

Vertical Sensitivity: 300 mV/div

Horizontal Sweep Rate: 20 ms/div

6.2.2 Convergence Time Test Results

The trace shown in Figure 6.3 was measured using the test apparatus described for the ERLE characterization. A convergence time of approximately 100 ms is observed under these conditions.

It must be pointed out that, although this type of test (using a nondispersive echo model) is standard for echo canceller characterization [1,2], it is not necessarily a good indicator of the typical expected convergence properties of the canceller. Since the misalignment vector in a nondispersive (non-filtered) environment starts with only one significant nonzero component, the error signal will be related to a single filter tap throughout most of the convergence process. Hence almost all of the corrections performed on this tap will be in the correct direction and a converged state will be obtained very quickly.

In order to demonstrate this fact, convergence time was measured with the echo channel model in Figure 6.1 replaced by a Kron-hite¹ adjustable bandpass filter with corner frequencies set to 300 Hz and 380 Hz. This particular filter function was chosen because the significant portion of its impulse response was dispersed over the full 8 ms length of the PTF as shown in Figure 6.4.

In this case, the measured convergence time was approximately 450 ms which is more in line with the value obtained from the computer simulation in Section 3.8.

Again such convergence times compete well with those specified for existing adaptive cancellers on the North American market [1,2].

¹ Adjustable filter manufactured by Kron-hite Company, Cambridge, Mass., U.S.A., Model 310-AB.

Figure 6.4: Impulse Response of Filter used to Test Convergence
Speed for a Dispersive Channel

Top Trace - 5V input pulse

Bottom Trace -

Vertical Sensitivity: 50 mV/div

Horizontal Sweep Rate: 1.0 ms/div

6.3 Steady State Performance in the Time Domain (IIR Channel)

In order to test the echo canceller's ability to identify a more complex echo channel response than the flat attenuation model used in the ERLE characterization, the converged response with an IIR model was examined. As in the previous section the Kron-hite adjustable bandpass filter (second order) was used as the unknown system to be identified. Several combinations of corner frequency settings were used in evaluating the canceller's performance.

As an example, the impulse response of the Kron-hite filter with corner frequencies set at 300 Hz and 600 Hz is pictured in Figure 6.5a). Figure 6.5b) shows the impulse response of the PTF in the converged echo canceller with coefficients frozen (adaptation inhibited). The strong resemblance of the two responses is indicative of the canceller's ability to identify the dispersive system.

The ERLE measured in this more demanding environment degraded to approximately 26 dB, compared to the 31 dB observed in the nondispersive case, since more coefficients were forced into low precision regions of the μ -law code. The outputs from the Kron-hite filter and the converged PTF are compared with a 3.4 kHz bandlimited white noise input in Figure 6.6 to point out close correspondence between the true response and the synthesized approximation.

The degradation in ERLE with increased impulse response dispersion is consistent with the performance predicted by equation 2.92 ($\sum |h(p)|$ becomes large).

6.4 Effect Of Eliminating Mid-Tread Quantizations

In order to confirm the effectiveness of the mid-tread

a) Impulse response of IIR system

b) Converged PTF response

Figure 6.5: Comparison of IIR System Impulse Response with Converged PTF Response

Top Traces -
 Vertical Sensitivity: 220 mV/div
 Horizontal Sweep Rate: 0.5 ms/div
 Bottom Traces - 5V input pulse

Figure 6.6: Comparison of True System Response (top trace) with Synthesized Response (bottom trace) with Bandlimited Noise Input

Vertical Sensitivity: 500 mV/div

Horizontal Sweep Rate: 5 ms/div

quantization scheme, the experiment described in the previous section was repeated with the mid-tread quantization features removed ($C_x = C_e = 0$). The resulting PTF impulse response is shown in Figure 6.7. Comparison of this response with that shown in Figure 6.5b) confirms that the effectiveness of the identification algorithm has been degraded. The ERLE provided in this case dropped to about 18 dB.

6.5 Steady State Performance in the Frequency Domain

In order to investigate steady state convergence properties in the frequency domain, two extreme channel responses were simulated. The first was a flat 6 dB attenuation and the second was a narrow, fourth order Butterworth bandpass response realized via a second Kron-hite adjustable filter. The corner frequencies of the bandpass filter were 400 Hz and 900 Hz.

Figure 6.8 compares the transfer function between the echo and the input for the flat channel to the corresponding residual error transfer function. The slow drop of the echo spectrum below the -6 dB low frequency value is the result of $\frac{\sin x}{x}$ roll-off produced by the S&H action. Clearly the residual error feedthrough is attenuated with respect to the echo by more than 30 dB as was determined in the ERLE characterization. Furthermore the residual error spectrum is fairly flat, confirming the approximate white frequency characteristic of the misalignment noise.

The echo and residual error transfer functions for the bandpass channel are compared in Figure 6.9. Here the residual error characteristic is substantially more erratic than that observed in the pre-

Figure 6.7: Impulse Response of Converged PTF without Mid-Tread
Quantization

Top Trace -

Vertical Sensitivity: 200 mV/div

Horizontal Sweep Rate: .5 ms/div

Bottom Trace - 5V input pulse

Figure 6.8: Echo and Residual Error Transfer Functions with Flat Channel

Figure 6.9: Echo and Residual Error Transfer Functions with Bandpass Channel

vious case due to the increased complexity of the identified channel and the fact that the different coefficients are represented with widely distributed precision because of their companded digital representations.

6.6 Confirmation of Misalignment Limited ERLE

Since the echo canceller incurs no residual error due to input (or error) signal quantization effects, the residual error signal in the ERLE characterization is primarily the result of coefficient misalignment for high echo levels (to 10 dB in Figure 6.2). This fact was confirmed by freezing the coefficients in the converged state for the flat channel, then carefully adjusting the channel gain to minimize the error signal power. Since only a single tap is represented with low precision for such a channel (the rest are in the least significant segment of the companded code), this process effectively eliminates the dominant source of misalignment noise.

As displayed in Figure 6.10 approximately 40 dB of ERLE could be achieved in this manner. This figure exceeds even the theoretical capability limits of echo cancellers based on companded PCM by about 5 dB. This further supports the argument in favour of analog signal processing since this level of ERLE could be achieved with the use of a better identification algorithm.

Shown also in Figure 6.10 is the error signal spectrum with the input signal removed which is in fact dominated by the PTF noise floor. The reason that the residual error in signal could not be reduced down to this noise floor can be explained by examining the system's response to a 1000 Hz sinusoid. The spectrum of the PTF output

Figure 6.10: Echo and Residual Error Transfer Functions after Manual Gain Optimization Compared to Circuit Noise Floor

with such an input is shown in Figure 6.11. Evident here are second and third harmonic distortion components. Since these distortion components are the result of system nonlinearity, they cannot be correlated with the input signal and cancelled. Hence the residual error spectrum contains these components even though the fundamental is cancelled, almost to the level of the noise floor. This is illustrated in Figure 6.12.

The nonlinear distortion components observed in this experiment are attributed to the input signal rectifier's nonideal characteristic. Confirmation of this by direct measurement was not possible however due to the masking effect of the large harmonic components present in the ideally rectified sinusoid.

Figure 6.11: PTF Output with ≈ 1000 Hz Sinusoidal Input showing Harmonic Distortion
(Impulse transfer function)

Figure 6.12: Residual Error with ≈ 1000 Hz Sinusoidal Input Displaying Uncancelled Harmonic Components
(Impulse transfer function)

The results obtained from the laboratory model are consistent with the performance predictions from the computer simulation and the mathematics presented in Chapter 2, both in terms of convergence time and steady state echo cancellation. Limitations on the amount of ERLE achievable due circuit noise and nonlinear distortion were also identified through this exercise. Such effects must be minimized to truly realize the full advantages of the analog signal processing approach.

The laboratory model's performance was generally quite high and supported the viability of echo cancellation via analog signal processing.

CHAPTER 7

CONCLUSIONS AND RECOMMENDATIONS

7.0 Summary

Arguments supporting the use of a mixed analog/digital architecture for echo canceller design were presented in this thesis. Attention was focussed on designing a system which exhibits performance competitive with that of existing digital cancellers but can be realized using relatively simple hardware. The major proposed vehicles for reduction of hardware complexity were the elimination of the need for A/D converters and digital signal storage registers due to sampled analog signal processing, and the ability to trade off identification algorithm precision with performance improvements gained through the elimination of input signal quantization errors.

A detailed mathematical analysis exploring methods for simplifying the classical gradient method of tap weight adaptation along with a supporting computer simulation led to the design and characterization of a 64 stage, high performance laboratory model echo canceller which illustrates these principles.

7.1 Recommendations Concerning Future Work

Some of the findings presented in this thesis have indicated the need for further research in the areas described below.

7.1.1 Signal Processing Dynamic Range

One of the major limitations of the echo canceller constructed

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was its dynamic range. This problem was attributed both to dynamic range of the PTF chip itself and a loss in top end dynamic range due to the design of the input signal rectifier. It is recommended that further research be directed towards developing analog signal processing structures with the wide dynamic range (> 54 dB per tap) required for echo cancellation. Devices having 128 or more stages and exhibiting such a dynamic range would truly have a decided advantage over equivalent digital circuits used in commercial echo cancellers.

7.1.2 Echo Canceller Integration

An echo canceller of the type described is well suited to integration on to a single IC. The possibility of including such a canceller as part of a larger system, such as a "handsfree telephone" [26], telephone subscriber line interface or bidirectional amplifier on a single chip has strong product development implications.

The PTF used in the construction of the laboratory model can be fabricated using a simple and very general technology. Other alternative sampled analog convolvers also exist as described in Chapter 4.

Integration of a companded MDAC on the same chip would be straightforward using a switched capacitor design approach as described in [15]. Random logic and clock generation circuitry is well suited to realization via PLA's or other general logic structures. The remaining correlation and processing circuits are also well suited to integration using switched capacitor techniques.

The operating frequency of the MDAC is a primary consideration in the design of an integrated PTF for an echo canceller. Since a

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multiplexed MDAC must operate at the filter's superfrequency to perform the convolution operation, some architectural pipelining may be required if echo canceller tail capability (PTF length) is increased.

Preliminary design calculations have indicated that the functional blocks for a 128-tap canceller of this type would occupy approximately 52,000 square mils of IC area assuming a 5 micron NMOS process. This figure is broken down in Appendix D and represents an area approximately 50% smaller than that occupied by the Bell Laboratories chip. Power dissipation should be reduced at least proportionately.

7.1.3 Echo Cancellation for Digital Signals

Recently, the use of echo cancellers has been proposed for use in achieving full-duplex digital communication over 2-wire telephone subscriber lines [24], [25]. This application requires much higher ERLE (60-70 dB) than is available from existing voiceband echo cancellers due to the necessity for cancelling "sidetone", which is typically much stronger than the desired signal from the far end. It has been proposed that sampled analog signal processing techniques might be a viable alternative to extremely wide digital storage registers in such applications.

7.1.4 Optimized Coefficient Storage Code

The μ -255 coefficient storage code used in the laboratory model canceller was responsible for fairly significant ERLE degradation for highly dispersive echo paths. This effect could be reduced by using a more gentle companding law for coefficient storage. This would

sacrifice some excess impulse response dynamic range for increased top-end precision. The μ -255 companding law was used in this exercise only, because of the availability of a suitable MDAC in discrete form and is by no means an optimal choice.

7.2 Conclusions

The potential advantages of analog signal processing for echo cancellation both in terms of hardware simplification and system performance have been demonstrated through this work. The results of this study could lead to the design of an echo canceller capable of being integrated as part of a larger system on a single IC.

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APPENDIX A

ECHO CANCELLER COMPUTER
SIMULATION


```

C      GENERATE NEW INPUT SAMPLE.
C
C      X(1)=XNEW(ISEED,REG,IIP)
C
C      GENERATE ECHO
C
C      Y=ECHO(X,H,NTAP)
C      YSTO(1)=Y
C
C      DO CONVOLUTION
C
C      YHAT=0.
C      DO 1030 J=1,NTAP
C      YHAT=YHAT+X(J)*HHAT(J)
1030  CONTINUE
C      ERROR=Y-YHAT
C      ERRSTO(1)=ERROR
C
C      UPDATE TAP WEIGHTS
C
C      CALL UPDATE(HHAT,NTAP,X,ERROR,BETA,IALG,ERRSTO)
1040  CONTINUE
C
C      PERFORMANCE MEASUREMENT
C      MISALIGNMENT VECTOR LENGTH:
C
C      ERVECT=0.
C      DO 1050 I=1,NTAP
C      ERVECT=ERVECT+(H(I)-HHAT(I))**2
1050  CONTINUE
C      ERVECT=SQRT(ERVECT)
C      WRITE (8,9010) NSTOP,ERVECT
C      NSTART=NSTOP+1
1060  CONTINUE
C
C      ERLE CALCULATION
C
C      SUM1=0.
C      SUM2=0.
C      DO 1070 I=1,NTAP
C      SUM1=SUM1+ERRSTO(I)**2
C      SUM2=SUM2+YSTO(I)**2
1070  CONTINUE
C      ERLE=10*ALOG10(SUM2/SUM1)
C      WRITE (8,9020) ERLE
C      PRINT*,HHAT
C      GOTO 1000
9000  FORMAT(//X,"ITERATIONS",15X,"ERROR MEAN SQ.")
9010  FORMAT(X,I5,20X,1E12.4)
9020  FORMAT(//X,"FINAL ERLE =",1E12.4,2X,"DB."//)
C      END
C
C      DIGITAL FILTER PRODUCING ECHO:

```

```

C
      REAL FUNCTION ECHO(X,H,NTAP)
      REAL
1       H(64),
2       X(64)
      TEMP=0.
      DO 1000 I=1,NTAP
          TEMP=TEMP+X(I)*H(I)
1000    CONTINUE
      ECHO=TEMP
      RETURN
      END

C
C
C       TAP WEIGHT CORRECTOR
C
      SUBROUTINE UPDATE(HHAT,NTAP,X,ERROR,BETA,IALG,ERRSTO)
      REAL
1       ERRSTO(64),
2       HHAT(64),
3       X(64)
      GOTO(1000,1020,1040,1070),IALG

C
C       ALGORITHM 1: STANDARD GRADIENT ADAPTATION
C
1000    DO 1010 I=1,NTAP
          HHAT(I)=HHAT(I)+BETA*ERROR*X(I)
1010    CONTINUE
      RETURN

C
C       ALGORITHM 2: FIXED MAGNITUDE CORRECTIONS
C
1020    DO 1030 I=1,NTAP
          DEL=ERROR*X(I)
          SIGN=-1.
          IF (DEL.GE.0.) SIGN=1.
          HHAT(I)=HHAT(I)+BETA*SIGN
1030    CONTINUE
      RETURN

C
C       ALGORITHM 3: FIXED MAGNITUDE CORRECTIONS WITH MID-TREAD
C               QUANTIZATIONS
C
1040    XRMS=0.
      DO 1050 I=1,NTAP
          XRMS=XRMS+X(I)**2
1050    CONTINUE
      XRMS=SQRT(XRMS/NTAP)
      EMIN=XRMS*1.E-8
      EMAG=ABS(ERROR)
      IF (EMAG.LE.EMIN) RETURN
      DO 1060 I=1,NTAP
          XMIN=.63*XRMS
          XMAG=ABS(X(I))

```

```

      DEL=ERROR*X(I)
      SIGN=-1.
      IF (DEL.GE.0.) SIGN=1.
      BETAP=BETA
C     IF(HHAT(I).GT.,3) BETAP=5*BETA
      IF (XMAG.GT.XMIN) HHAT(I)=HHAT(I)+BETAP*SIGN
1060  CONTINUE
      RETURN
C
C
C     ALGORITHM 4: U-LAW COEFFICIENT ADAPTATION
C
1070  XRMS=0.
      ERMS=0.
      DO 1080 I=1,NTAP
        XRMS=XRMS+X(I)**2
        ERMS=ERMS+ERRSTO(I)**2
1080  CONTINUE
      XRMS=SQRT(XRMS/NTAP)
      ERMS=SQRT(ERMS/NTAP)
      EMIN=1.46*ERMS/XRMS
      EMIN=EMIN*2.8141
      IF (ERMS.GE..28) EMIN=1E-8
      EMAG=ABS(ERROR)
      IF (EMAG.LE.EMIN) RETURN
      DO 1170 I=1,NTAP
        XMIN=1.42*XRMS
        XMAG=ABS(X(I))
        IF (XMAG.LT.XMIN) GOTO 1170
        DEL=ERROR*X(I)
        ISIGN=-1
        IF (DEL.GT.0.) ISIGN=1
        HMAG=ABS(HHAT(I)*3832.)
C
C     U-LAW CORRECTOR
C
      IF (HMAG.GE.16) GOTO 1090
      HHAT(I)=HHAT(I)+FLOAT(ISIGN)/3832.
      GOTO 1170
1090  IF (HMAG.GE.47) GOTO 1100
      HHAT(I)=HHAT(I)+2*FLOAT(ISIGN)/3832.
      GOTO 1170
1100  IF (HMAG.GE.108) GOTO 1110
      HHAT(I)=HHAT(I)+4*FLOAT(ISIGN)/3832.
      GOTO 1170
1110  IF (HMAG.GE.229) GOTO 1120
      HHAT(I)=HHAT(I)+8*FLOAT(ISIGN)/3832.
      GOTO 1170
1120  IF (HMAG.GE.470) GOTO 1130
      HHAT(I)=HHAT(I)+16*FLOAT(ISIGN)/3832.
      GOTO 1170
1130  IF (HMAG.GE.951) GOTO 1140
      HHAT(I)=HHAT(I)+32*FLOAT(ISIGN)/3832.
      GOTO 1170

```

```

1140     IF (HMAG.GE.1912)GOTO 1150
        HHAT(I)=HHAT(I)+64*FLOAT(ISIGN)/3832.
        GOTO 1170
1150     IF (HMAG.GE.3832)GOTO 1160
        HHAT(I)=HHAT(I)+128*FLOAT(ISIGN)/3832.
        GOTO 1170
1160     HHAT(I)=1.
1170     CONTINUE
        RETURN
        END

C
C
C     RANDOM INPUT GENERATOR
C
      REAL FUNCTION XNEW(ISEED,REG,IIP)
      REAL
1      REG(64)
      TEMP=0.
      DO 1000 I=1,12
        ISEED=ISEED*65539
        TEMP=TEMP+2*ISEED*2.328306436538696D-10/16
1000    CONTINUE
      XNEW=TEMP/2.

C
C     RANDOM NUMBERS HAVE ZERO MEAN, UNIT VARIANCE
C
      IF (IIP.EQ.1) RETURN
      Y=.557*REG(1)-.779*REG(2)+.837*REG(3)
      REG(2)=REG(1)
      REG(1)=Y
      REG(3)=TEMP/SQRT(2.)
      XNEW=Y
      RETURN
      END

```

APPENDIX B

PTF PINOUT DESCRIPTION

DIP - 24 PINS

PIN NUMBER	SYMBOL	COMMENTS
1	SUB	substrate - held at -5 volts
2	ϕ_4	high = 12 volts, low = 0 volts
3	ϕ_3	high = 12 volts, low = -5 volts
4	in-SR	high = 12 volts, low = 0 volts
5	V_{SS}	low supply = 0 volts
6	ϕ_2 -SR	
7	ϕ_1 -SR	high = 12 volts, low = 0 volts
8	no connection	
9	V_J	adjustable offset balancing voltage ≈ 5 volts
10	no connection	
11	V_{in}	analog input
12	ϕ_3	high = 12 volts, low = 5 volts
13	V_I	analog ground = 5 volts
14	V_{OUT}	analog output
15	S	high = 12 volts, low = 0 volts
16	R	
17	V_{RES}	reset voltage for last BBD capacitor = 10 volts
18	ϕ_2	high = 12 volts, low = 0 volts
19	V_{DD}	high supply = 10 volts

20	ϕ_5	high = 12 volts, low = 0 volts
21	no connection	
22	ϕ_1	high = 12 volts, low = 0 volts
23	D_{in}	first BBD input = 0 volts
24	G_1	identical to ϕ_1

APPENDIX C

ENGINEERING SCHEMATICS OF THE
LABORATORY MODEL ECHO CANCELLER

POWER SUPPLIES

SHEET 1 - ADAPTATION CLOCK CIRCUITRY

SHEET 2 : PTF TIMING CIRCUIT

SHEET 4 : TAP WEIGHT RAM

APPENDIX D

PRELIMINARY AREA ESTIMATE FOR A SAMPLED ANALOG ECHO CANCELLER IC

In order to make an approximate comparison with the Bell Laboratories echo canceller in terms of chip area, most of the data shown below is based on figures found in [1]. The length of the canceller has also been extended to 128 taps and a 5 micron NMOS process has been assumed for the same reason.

<u>Circuit Block</u>	<u>Area Required</u> (mils ²)
* Companded MDAC	3,200
128 x 8 - Bit RAM	7,987
* 20 OP AMPS	2,440
Transversal Filter [11]	18,352
300-600 Random Gates	<u>20,000</u>
	51,979 mils ²

* Estimate obtained through Northern Telecom Inc., Silicon Division.

It is noted that the above figures do not allow for the inclusion of a doubletalk detector or a centre clipper which are both provided on the Bell Laboratories IC. These are very simple functional blocks however and are assumed to occupy negligible area.

Note also that, in analog applications, the Bell Laboratories IC must operate with two A/D and two D/A converters.

END

0	6	H	0	9	H	8	4
---	---	---	---	---	---	---	---

FIN