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CONTINUOUS-TIME FILTERS USING
OPEN LOOP TUNABLE TRANSCONDUCTANCE AMPLIFIERS

by

Calvin Plett

A thesis submitted to the Faculty of Graduate
Studies and Research in partial fulfillment
of the requirements for the degree of

Master of Engineering

Department of Electronics
Faculty of Engineering
Carleton University
Ottawa, Canada
August 1986

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The undersigned recommend to the faculty of Graduate Studies
and Research the acceptance of the thesis:

"Continuous-Time Filters using Open Loop
Tunable Transconductance Amplifiers"

submitted by Calvin Plett in partial fulfillment of the
requirements for the degree of Master of Engineering.

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ABSTRACT

This thesis reports on work on high-frequency continuous time filters which used tunable transconductance amplifiers. The use of opamps allowed for high output impedance and easy interconnection of integrators. Both single-ended and double-ended biquad filters, have been realized in CMOS. High Q zeros and close relative spacing of poles and zeros were used to achieve a fast transition from passband to stopband.

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LIST OF SYMBOLS AND TERMS

AC	Alternating Current
BNR	Bell Northern Research
GMC	Canadian Microelectronics Corporation
CMOS	Complementary Metal Oxide Semiconductor
CMOS1B	Northern Telecom CMOS process, with 5um minimum line width.
CMOS3	Northern Telecom CMOS process, with 3um minimum line width
DC	Direct Current
DE	double ended -an opamp or OTA integrator which has a positive and a negative output
DRC	design rule check
EPROM	Erasable Programmable Read Only Memory
IC	Integrated Circuit
LAYED	Layout Editor
NT	Northern Telecom
opamp	operational amplifier
OTA	operational transconductance amplifier
phase margin	-the phase difference between the output phase and 180 degrees, measured at the UGBW in an open loop amplifier or OTA. This is a measure of stability.
PHLED	Physical Layout Editor
PSRR	Power Supply Rejection Ratio

LIST OF SYMBOLS AND TERMS (continued)

SCAMPER circuit simulator

SE single ended - an opamp or OTA integrator which has a positive output only

SPICE circuit simulator

μm micron

μA microampere

UGBW unity gain band width, the frequency at which the gain goes to unity or 0dB.

VCF Voltage Controlled Filter

VCO Voltage Controlled Oscillator

V_{DS} voltage from drain to source

V_{GS} voltage from gate to source

V_{i} input voltage

V_{o} output voltage

V_{T} Threshold Voltage

CHAPTER 1 INTRODUCTION

1.1 THESIS OBJECTIVE

The objective of this thesis is to explore the use of wideband CMOS opamp design techniques in the realization of open loop transconductance filters. Emphasis will be on the biquad filter which will include a zero in its transfer function. The use of EPROMs in pretuning the filter parameters will also be explored. Other means of tuning the filter parameters will not be considered in detail.

1.2 THESIS MOTIVATION

In the past, open loop transconductance filters have been realized using differential pairs. This did not allow DC coupling and required level shifting. Also, performance was dependent on the parasitics of the input stage. Use of a wideband CMOS opamp eliminates problems with DC coupling and level shifting. As well, parasitics are well understood for the CMOS opamp, so that standard circuit design techniques can be used to improve the performance of the filter.

In many applications such as for anti-alias filters, a fast transition from the pass band to the stop band is required. In switched capacitor filters this has been achieved by using biquad filters with zeros in the transfer function. In the past, implementation of zeros in continuous filters has not received a lot of attention, though the possibility has been mentioned. In this thesis, high rolloff filters will be studied through the use of closely spaced poles and zeros.

Most of the continuous time filters discussed in the past have used a phase-locked loop tuning circuit. This requires the use of voltage-controlled oscillators or voltage-controlled filters, phase detectors and loop filters with long time constants. This represents a large amount of circuitry. In this thesis an alternative is presented where the circuit is pretuned using relatively simple circuitry consisting of EPROMs.

1.3 BACKGROUND OF MONOLITHIC FILTERS

The background of monolithic filters will be presented with the integrator used as an example. Various forms of the integrator are seen in Figure 1.1 and will be discussed as a means of developing understanding of the particular integrator used in this thesis, the open loop transconductance integrator.

1.3.1 DISCRETE FILTERS

Figure 1.1a shows the well known discrete continuous time integrator which uses a capacitor, a resistor and an integrated operational amplifier (opamp). Precision of the time constant, RC , is obtained by the use of precise discrete components. The main requirements of the opamp are that it have a high gain and low noise at the frequencies of interest. With the increase in the complexity of integrated circuits, it became desirable to have complete filters on the integrator circuit. High quality capacitors with low voltage dependence could be integrated

a) Discrete Integrator

b) Switched Capacitor Integrator

c) Transistor in Linear mode

d) open loop OTA Integrator

e) Differential Pair Integrator

Figure 1.1 Integrator Options

but large-valued resistors required large areas and showed a strong voltage dependence, and led to widely varying time constants. This started the search for an alternative device or circuit technique that would perform the same function as the resistor without its problems.

Some of the resulting techniques were the switched-capacitor filter [1] and the transconductance filter [2]. These methods solved some of the problems associated with integrated resistors but they, in turn, created other problems.

1.3.2 SWITCHED-CAPACITOR FILTERS

Figure 1.1b shows a version of the switched-capacitor integrator. The capacitor, C_R , is switched between the input voltage and the virtual ground of the opamp. A charge flows in proportion to the voltage difference. This amount of charge flows in every clock period T . Averaged over a number of cycles, this is equivalent to the flow of current through a resistor. The value of the equivalent resistor is given by T/C_R . Thus the discrete time constant RC is equivalent to the switched-capacitor time constant of TC/C_R . The capacitor ratio can be very precise, in spite of poor absolute precision, leading to accurate time constants without the necessity of trimming.

However, switched-capacitor filtering is not without its drawbacks. Since the switched-capacitor filter is inherently a sampled data system, mixing occurs between the input frequency and the clock frequency. Any input frequency higher than half the clock frequency will appear in the baseband at the output. This effect, called alias-

ing, must be avoided by preceding the sampling device with a continuous-time anti-alias filter.

Switched-capacitor filters are limited in their high frequency capabilities. The opamps in a switched-capacitor circuit must settle close to their final value in the clock period. Thus the opamps will typically have a unity gain bandwidth (UGBW) much higher than the frequency of the clock. In addition, only if the clock frequency is well beyond the filtering frequency of interest, can the idea of a resistor equivalent be used.

The switched-capacitor filter requires considerable area to realize the clock driver, (typically of up to four phases), the switches, capacitors, interconnections, and the anti-alias filter. As well, the presence of a clock in the system can cause noise which is picked up in other parts of the circuit. Clock signals can be injected through the switches into the filter circuit where they result in clock feedthrough noise. This can be limited but not prevented by careful design of matched complementary switches. Residual noise can often be tolerated since the clock frequency is higher than the filter cut-off frequency.

1.3.3 CONTINUOUS TIME INTEGRATORS

The continuous filter has a number of advantages over the sampled data filter. It does not require an anti-alias filter. Problems such as clock feedthrough or clock noise are eliminated. There is the potential of operation at higher frequencies since settling time in a

clock period is no longer of concern. There are some disadvantages however. Unlike the switched-capacitor, the devices or circuits used in place of the resistor are often nonlinear or voltage dependent. This requires additional circuitry to minimize these effects. The equivalent resistance value is no longer matched to the capacitors and hence elaborate tuning schemes must be used if precision is required. These disadvantages are very important and have been the main reason for the continued success of switched-capacitor filters in monolithic integrated circuits.

1.3.3.1 TRANSISTOR AS A RESISTOR

The simplest device to use as a resistor is the MOS transistor in the linear region as shown in the circuit in Figure 1.1c. The transistor is equivalent to a resistor over a small voltage input region only. It is therefore necessary to take steps to expand the range and improve linearity. Tsividis [3] reported on such a device where linearity was improved by use of a differential arrangement. This was used in the voice band, but later studies, [4] showed the possibility of extending this up to higher frequencies. The time constant of the integrator is tuned by adjusting the gate voltage of the transistor. This gate voltage is derived typically from a phase-locked loop tuning circuit. One of the reported tuning strategies was to use two identical transistors as resistors and to alternately switch them between the actual circuit and a tuning circuit [5]. Thus there was always a complete circuit except during the switching transients and this was

referred to by the author as "essentially" continuous.

1.3.3.2 OPEN LOOP TRANSCONDUCTANCE FILTERING

A transconductance device is one where the output current is proportional to the input voltage. This is another name for a voltage controlled current source. The most fundamental of such devices is the MOS transistor, where the input is the gate voltage and the output is the drain or source current. This simple device displays the same problems as the MOS resistor, that is, a small linear operating range. In addition, the output resistance is too low for a good current source. More elaborate circuits can be used to overcome such problems. These circuits in their more complex forms are often called operational transconductance amplifiers or OTAs due to their resemblance to the standard opamp.

Figure 1.1d shows the basic integrator based on the OTA. The symbol shown for the OTA illustrates the fact that the OTA differs from the opamp mainly in that it has a different output stage. The OTA feeds a current proportional to the input voltage into the integrating capacitor. This is the same function performed by the resistor in the discrete integrator. For the discrete integrator of Figure 1.1a, the output voltage V_o is related to the input voltage V_i , by:

$$V_o = i/sC = V_i/sCR \quad (1.1)$$

For the OTA based integrator of Figure 1.1d, the corresponding equation is:

$$V_o = i/sC = g_m V_i/sC \quad (1.2)$$

Thus, the two circuits have identical performance if the transconductance g_m of the OTA integrator is made equal to $1/R$ of the discrete integrator. By setting the output voltage equal to the input voltage, the unity gain bandwidth of the two integrators can be seen to be:

$$UGBW = 1/RC \text{ and } g_m/C \text{ respectively} \quad (1.3)$$

The term $1/RC$ or g_m/C usually corresponds to the pole frequency of a filter using this integrator. That is, the filter pole frequency is usually equal to the unity gain bandwidth of the integrator.

The diagram and equations point out one of the differences between the discrete integrator and the OTA integrator. In the discrete integrator, the UGBW of the opamp in open loop is required to be much higher than the UGBW of the integrator since in closed loop the opamp input must be maintained at virtual ground. In the OTA case, the UGBW of the filter and of the OTA itself are the same. The OTA filter is thus generally capable of operating at higher frequencies. There is a reservation, however. High frequency operation in the opamps and OTA integrators is limited to a different extent by the phase shift due to the parasitic pole (second, non dominant pole related to parasitic,

capacitance). The opamp can have a UGBW close to the parasitic pole while the OTA must have a UGBW sufficiently lower to avoid phase shift due to the parasitic pole. Thus the opamp, as used in the discrete integrator, can have a higher open loop UGBW than that of the OTA integrator.

In the transconductance filter, the pole frequency is determined by the ratio of the transconductance to the capacitance. Thus the ratio of these values is very important in determining the accuracy and reproducibility of the filter functions. This ratio does not track in integrated circuit technology so tuning is required. The transconductance can be tuned by control of the current through the input transistors of the OTA. The capability of tuning is important in the design of general purpose filters which can be tuned over a range of frequencies.

The actual design of an on chip tuning circuit can be quite complex. In the past this has been done by designing a voltage-controlled oscillator (VCO) or a voltage-controlled filter (VCF) using the same integrators as were used for the actual filter. A phase-locked loop could be used to tune the filter by comparing the output of the VCO or the VCF to an externally supplied reference signal.

In 1978 Tan and Gray [6] reported on transconductance filtering which used a phase-locked loop tuning method. Since then, numerous papers have been written which describe transconductance filtering and present various designs of transconductance amplifiers. One of the

most fundamental designs for the transconductance amplifier is the differential pair [7], as shown in Figure 1.1e. This allows designs with a low number of transistors. This is attractive for limiting the parasitics that reduce the high frequency operation potential. However this design can achieve only moderate DC gains, requires level-shifting and presents inter-stage coupling problems.

Significant work has been done, in the past, on the applications of transconductance amplifiers. Geiger et al. in a 1985 paper, [8], provided a detailed discussion and bibliography of such work. In the past, filter designs have often been based on ladder filters [7]. Ladder filters are favored due to the low sensitivities to component variations. Biquad filters on the other hand are of interest since they can be realized directly with the OTA as the integrator, they have been used extensively and studied in the past in the context of switched capacitor filters and they allow independent control of various parameters such as Q, gains, pole frequencies etc. Biquad filters have been studied in the context of high Q multiple pole filters. One of the big problems with this design is that of Q enhancement due to the use of non ideal integrators. The implementation of biquad filters which include zeros in the transfer function have been mentioned in the past but one of the first reported realizations occurred in [9], where it was reported that the Q of zeros was decreased with non ideal integrators.

1.4 Thesis Format

The thesis is on a study of open loop transconductance filtering and tuning considerations. Chapter 1 is the introduction to the thesis. It provides the objective and the motivation for the thesis as well as a discussion of background material. In Chapter 2, the use of the folded cascode opamp as the transconductance amplifier will be justified and details of the design will be given. Both single ended and double ended designs will be discussed. In Chapter 3 these amplifiers will be interconnected to form biquad filters. Simulations and measurements will be discussed in Chapter 4. In Chapter 5, filter tuning will be discussed. After the general discussion, design, simulation and measurement of EPROM-based pretuning circuits will be presented. In Chapter 7, conclusions will be drawn.

CHAPTER 2 OPAMP AND INTEGRATOR DESIGN FOR OTA FILTERS

2.1 INTRODUCTION

The design of opamps and integrators is important in determining OTA filter behaviour. As discussed in Chapter 1, the fundamental part of the biquad, the integrator, should be as ideal as possible. An ideal integrator has a gain which decreases at 20 dB per decade and the phase is at -90 degrees. Any deviation from the ideal will be first seen as a phase shift which causes serious degradation in the filter performance. This implies as design objectives for the integrator, a high DC gain and parasitic poles occurring at relatively high frequencies. The opamps, as distinct from the OTA integrators, will be used mainly as buffers between filter stages and as output pad drivers. To operate well as buffers, they should have significant gain at the frequencies of interest. This implies that their UGBW should be much higher than that of the integrators. As output drivers they should provide sufficient current to drive external loads. Other parameters of interest to both the integrators and the opamps are noise, power supply rejection, common mode range, linearity, layout area and power consumption.

In this thesis, the terms opamp, integrator and OTA may be confused since all are based on the folded cascode opamp. Whenever the distinction is required, the integrator, or OTA integrator will refer to a folded cascode opamp that has been modified to operate specifically as an integrator in a filter context. The term buffer opamp will be used only when discussing a folded cascode opamp that has

been designed to have a high unity gain bandwidth, since its main function is as a buffer between filter stages. Often the distinction is not required, or the meaning is obvious, and the terms OTA or opamp will be used.

2.2 OTA INTEGRATOR SELECTION

There are a number of reasons why the OTA integrator using the folded cascode opamp was selected instead of a simpler choice such as the differential pair. First, the opamp does not have the level shift problems that the basic differential pair does. It can be designed to have a nominal output voltage at zero volts, that is, with no offset. Second, the addition of the output stage increases the output impedance and increases the DC gain. This allows the low frequency pole to be at a frequency much lower than the frequency of interest. As well, with the folded cascode opamp, the parasitic poles are well understood so known design techniques can be used to push the high frequency parasitics to as high a frequency as possible. A finite DC gain will cause a phase lead at low frequencies while the parasitic poles cause a phase lag at high frequencies. Ideally these should be far enough apart to provide a wide region where the phase is at 90 degrees. Since in practice a wide region is not obtainable, the design can deliberately trade off the two effects to obtain 90 degrees at the frequency of interest. Finally, with the use of the opamp, both double-ended and single-ended filters are possible. The double-ended filters and opamps have both a positive and negative output while the single-ended filters and opamps have only the positive output. All opamps have both a positive and

negative input.

The folded cascode opamp shown in Figure 2.1 is a good choice for use as a high frequency transconductance amplifier. It is basically a single pole design which allows it to operate at high frequencies. The dominant pole is provided by a capacitor at the output, which can also be used as the integrating capacitor. This amplifier has a high impedance current output which is proportional to the input voltage as is required for design of the integrator.

2.3 FOLDED CASCODE OPAMP CIRCUIT DESCRIPTION

The folded cascode amplifier is shown in Figure 2.1 as eleven transistors and two blocks. The bias block provides biases to some of the current sources and cascode transistors and will be described later. The other block contains an offset correction circuit for the single-ended amplifier or a common-mode correction circuit for the double-ended amplifier. This block is the main difference between the single-ended and the double-ended amplifiers and its details will be examined later. The rest of the circuit is common to all amplifiers and will be discussed in this section.

Figure 2.2 shows a simplified schematic of the single-ended amplifier where some of the transistors have been replaced by equivalent current sources. Nominal currents for the case where there is no differential input voltage are also shown. Transistors M1 and M2 form

the input differential pair. M3 is the current source for the input pair. This current of $2I$ is nominally split equally so that a current of I goes through each of the input transistors. The current through these devices is 'folded' over into the output stage which consists of M4 through M11. M4 and M5 act as current sources of value $2I$ each as set by the bias circuit. Of this current, I goes through an input transistor, leaving a current of I for the output stage. The output common mode or offset block measures one or both of the output voltages and sets the current sources M10 and M11 to keep the outputs at zero volts. Thus, the current in the output stage is nominally balanced so that if there is no differential input voltage, the outputs are at zero volts with no output current. Transistors M6, M7, M8 and M9 are the cascode transistors which act as buffers to increase the output impedance of the opamp. The bias circuit is required to keep these transistors operating in their saturated region.

When a differential input voltage V_i is applied, as shown in Figure 2.3 for the single-ended amplifier, and Figure 2.4 for the double-ended amplifier, currents in M1 and M2 are no longer equal. Each of the input transistors will have half of the input voltage across it so the current will be $g_m V_i / 2$ away from the nominal current of I . This will be added to the nominal cascode current on one side and subtracted from the other. The effect of these currents on the output current flowing into the integrating capacitor depends on the output feedback circuit. In the single-ended case, the feedback holds the negative

Figure 2.3 The Single-Ended Opamp with Differential Input

Figure 2.4 The Double-Ended Opamp with Differential Input

output to ground by balancing the current on that side. This has the effect of doubling the current on the other side so the output current is $g_m V_i$. In the double-ended case, the feedback keeps the sum of the two outputs at ground so if the change of currents is balanced, the feedback does not make any change. Thus the output current is $g_m V_i / 2$. Therefore, with the same input transistors and the same transconductance, the current at each output of the differential OTA is half of the output current for the single-ended OTA.

2.4 DESIGN OF OPAMPS AND OTA INTEGRATORS

The initial goal was to design a filter at 455 kHz that would include a zero in the design. Thus an OTA integrator had to be designed with a UGBW at 455 kHz. For the buffer opamps, a decision was made to use the same basic structure, but with changes made to the input pair and to the integrating or compensation capacitor. Thus for the OTA integrator the g_m is minimized while the output capacitor is made as large as possible. For the buffer opamp, the g_m of the input pair is made as large as possible while the output capacitance is made as small as possible while still retaining a safe phase margin.

The required corner frequency can be achieved by a combination of input sizes and bias current. This choice will involve a tradeoff between the need for a wide common-mode operating range, and linearity. Small input devices allow a wide linear differential input swing while larger input devices (and lower bias current) will allow a wider common-mode range. These factors will be examined in the following sec-

tions.

2.4.1 DESIGN PROCEDURE

The OTA integrators and buffer opamps can be roughly designed by use of the simple square law transistor equations. Fine tuning would have to follow and would involve the use of simulations and measurements.

The basic square law equation for a MOS transistor in saturation is:

$$i_d = \frac{k_p}{2} \left(\frac{W}{L}\right) (V_{gs} - V_T)^2 \quad (2.1)$$

Where k_p is a transistor parameter that takes into account the mobility, the dielectric constant and the oxide thickness. By taking the derivative of this equation with respect to V_{gs} , the transconductance can be found to be:

$$g_m = \frac{d(i_d)}{d(V_{gs})} = k_p \left(\frac{W}{L}\right) (V_{gs} - V_T) = (2k_p \left(\frac{W}{L}\right) i_d)^{1/2} \quad (2.2)$$

The required size of g_m can be determined from the required corner frequency and the size of the integrating capacitor by use of the following relation as derived in Chapter 1.

$$\omega_c = \frac{g_m}{C} \quad (2.3)$$

The square law relations can be used to estimate cutoff voltage, common-mode range and linearity. The differential pair shown in Figure 2.5, can be described by the currents i_1 and i_2 through the input

Figure 2.5 The Differential Pair

transistors as a function of input voltages, V_1 and V_2 , and the common source voltage, V_S , by use of (2.1). The sum of these currents must equal the bias current I_B through M3. These equations are:

$$i_1 = k (V_1 - V_S - V_T)^2 \quad (2.4)$$

$$i_2 = k (V_2 - V_S - V_T)^2 \quad (2.5)$$

$$i_1 + i_2 = I_B \quad (2.6)$$

where:

$$k = (k_p/2) (W/L) \quad (2.7)$$

These equations can be combined to eliminate V_S and i_2 to give the basic square law equation describing the differential pair:

$$(k)^{1/2} (V_1 - V_2) = (i_1)^{1/2} - (I_B - i_1)^{1/2} \quad (2.8)$$

2.4.2 CUTOFF OF INPUT TRANSISTOR

An input transistor will be cutoff when the opposite transistor takes all of the bias current. By setting i_1 equal to I_B or to zero, in eq. 2.8, the following conditions result:

$$(V_1 - V_2) = \pm (I_B/2k)^{1/2} \quad (2.9)$$

Thus, to allow a maximum swing before cutoff, I_B should be high and the transistor size or k should be small. By changing both I_B and k , the cutoff voltage can be increased while keeping the g_m constant.

2.4.3 INPUT COMMON-MODE RANGE

Common-mode voltage is defined as the average of two voltages while differential voltage is the difference between two voltages. Common-mode range is a measure of how far the average of the two input voltages can differ from zero volts without seriously affecting the OTA performance. The worst case is when the two inputs swing negative since this will bring the current source transistor M_3 out of saturation. The

point at which this happens is when the common source voltage V_S swings down to a threshold voltage below the gate voltage, (V_{B4}) of $M3$. By setting V_S equal to $(V_{B4} - V_T)$ and using (2.8) the following results:

$$V_{in} = V_{B4} + (I_B/2k)^{1/2} \quad (2.10)$$

This shows that at low current, the input voltage equals the bias voltage since at cutoff the source is just one threshold below the bias voltage. At any finite current, the second term in (2.10) gives the additional voltage required to pass that current. This shows that V_{B4} should be low, which may require bias transistors with large (W/L) . Once V_{B4} is set then this limit can be approached by using large input devices at low current such that the operating voltage across these transistors is small. This is the opposite requirement to that for maximum differential input range as seen in the previous section.

It should be noted that (2.10) does not give a hard limit. After the limit point, the current source goes out of saturation and the bias current will no longer be constant. This causes the transconductance of the input stage to decrease. It is possible by increasing the bias voltage, V_{B4} , to offset this decrease in transconductance. However, a feedback tuning circuit will not make this correction since most tuning circuits operate on a separate reference filter which will not experience the same common-mode voltage.

2.4.4 LINEARITY

Linearity was not studied in detail except for the effect of the device size of the input stage. The frequency response requirements often call for small devices in the input stage for which linearity can be obtained over a wide swing of input voltage. This is in general not true for an opamp since for this case the input stage must be as large as possible to achieve maximum gain.

Equation 2.8 describes the nonlinear relation between currents and voltages of a differential pair. To simplify the equations another variable X is defined. Since the current i_1 is nominally half of the bias current I_B :

$$i_1 = I_B/2 (1 + X) \quad (2.11)$$

or:

$$X = (2i_1 - I_B)/I_B \quad (2.12)$$

X now represents the difference in current from the nominal. Since i_1 swings from 0 to I_B , X can vary from -1 to +1 and is nominally equal to 0. Equation 2.8 then becomes:

$$(2k/I_B)^{1/2} (V_1 - V_2) = (1+X)^{1/2} - (1-X)^{1/2} \quad (2.13)$$

The two right-hand terms can be expanded using the binomial expansion. In the process the even powers cancel out and the expression becomes:

$$(2k/I_B)^{1/2} (V_1 - V_2) = X + 1/8 X^3 + 7/128 X^5 \dots \quad (2.14)$$

This gives us the input voltage as a function of the current. The series can be inverted to solve for the current. To simplify, express the input voltage drive Y as follows:

$$Y = (2k/I_B)^{1/2} (V_1 - V_2) \quad (2.15)$$

The expression can then be written in terms of a series in Y:

$$X = Y - 1/8 Y^3 - 25/512 Y^5 \dots \quad (2.16)$$

This can be expressed in terms of g_m using (2.2) as:

$$i_1 = \frac{I_B}{2} + \frac{g_m}{2} (V_1 - V_2) X$$

$$\left[1 - \frac{1}{8} \left(\frac{2k}{I_B} \right) (V_1 - V_2)^2 - \frac{25}{512} \left(\frac{2k}{I_B} \right)^2 (V_1 - V_2)^4 \right] \quad (2.17)$$

This shows the third and fifth order nonlinearity terms in proportion to the fundamental. To make the linear term dominate, the input device should be small. This also increases the cutoff voltage as seen from (2.9). At the cutoff voltage the third harmonic will be 25% of the fundamental and the fifth will be about 20%. In this extreme case, a large number of the higher order nonlinearities are also important. At half of the cutoff voltage, the third and fifth order terms are down to

about 6% and 1% respectively.

This analysis has shown that it may be possible to design the input differential stage to have the desired linearity and cutoff by using appropriate input stage size and current. However, frequently a tradeoff will be involved since the size of the input devices may be constrained by requirement of a particular corner frequency (2.3) or common-mode voltage range (2.10).

2.4.5 SINGLE-ENDED OFFSET CORRECTION AND BIAS CIRCUITS

An offset correction circuit is required in the single-ended folded cascode amplifier to ensure that under steady state conditions the output is at zero volts when the inputs are at zero volts. The main reason for requiring the offset circuit is that the input stage current is fed directly into the output stage. The input current, which is used to tune the UGBW, can be varied over a large range. The offset circuit should be capable of keeping the output close to zero volts in spite of varying currents, nonideal design, process variations and temperature changes.

Figure 2.6 shows the offset correction circuit for the single ended OTA. Transistors M12 and M13 form a feedback loop which measures the voltage at the negative output and controls the current source, M10 and M11 to keep the output voltage nominally at zero volts.

The capability of providing a low offset over the range of tuning currents depends largely on the design of the bias circuit. In the

basic bias circuit of Figure 2.7, the cascode string bias I_{CASC} sets up the currents I_4 and I_5 through M_4 and M_5 in Figure 2.6, separately from the tuning current I_B . The feedback circuit adjusts the current through M_{10} and M_{11} to be equal to $(I_4 - I_B/2)$, to obtain a balance. Thus the current I_{10} will decrease in direct proportion to an increase in input bias current. When I_B reaches $2I_4$, the output string current will fall to zero and the circuit will cease to work. Even before this point, the feedback loop will not be able to keep the negative output at exactly zero volts due to the low loop gain. The output voltage and the gate voltage of M_{10} and M_{11} are relatively the same, being separated by a source follower. Thus a change in current requires a change in the gate voltage and hence in the output voltage.

Figure 2.8 shows an improved bias circuit where the cascode string biases are related to the input stage bias. In this case, the current through M_4 and M_5 is equal to I_B and the feedback loop is required to keep I_{10} at $I_B/2$. This means that cut off will not occur in the output stage. The feedback loop gain is the same as before so output variations will still occur as the bias current changes. What is required is a circuit where the feedback loop is also referenced to the bias circuit so that at any bias current, the output can nominally remain at zero volts. An example of such a circuit will be shown for the double-ended opamp and OTA integrator.

Figure 2.8 Improved Bias Circuit.

The improved bias circuit is more complicated than the basic bias circuit of Figure 2.7. This is largely because it was designed as a wide swing bias circuit [10]. This circuit is designed to bias the current source transistors M4, M5, M10 and M11 of Figure 2.6 closer to the edge of saturation, allowing the output to swing closer to the power supply voltage without loss of gain. This is required for opamps with reduced power supply voltages.

2.4.6 DOUBLE-ENDED COMMON-MODE CIRCUIT

Double-ended opamps and OTA integrators require both a positive and a negative output which together do not have any common-mode voltage. That is, the output voltage swing should be purely differential with the average at zero volts. The differential output voltage is the result of the output current which is defined by the differential input voltage. The common-mode output voltage, however, is indeterminate so a circuit is required to ensure it remains at zero volts.

The design of a common-mode suppression circuit is one of the most important aspects of double-ended amplifier design and has received a lot of attention in the literature. Most of the reported designs involve some compromises. The common-mode circuit must be linear and be able to operate over a large output voltage range. A lack of linearity often causes large differential signals to be partially converted into common-mode signals, that is, the swings on the two output sides are not equal. Limited operating range or imbalance in the common-mode circuit can cause the output swing to be limited in one

direction. The common-mode circuit can potentially add power supply noise or other noise to the outputs of the amplifier so this must be considered as part of the design. Common-mode loop stability is another important consideration which has not been extensively explored in the literature.

This section will deal with some alternative designs of a common mode circuit with emphasis on loop stability, linearity and noise rejection. The results of this analysis could also be applied to the single-ended case and other areas of circuit design in general.

Figure 2.9 shows the double-ended opamp with blocks shown for the bias circuit and the common-mode circuit. This amplifier is the same as the single-ended circuit as was shown in Figure 2.1 except for the common-mode circuit, and the load connection. A capacitor from each output to ground, as shown, provides a common-mode load of value C . It also provides an equivalent differential load of value $C/2$ since the capacitors are in series for difference mode signals. Note that a capacitor connected directly between the two outputs would not provide a common-mode load. The offset circuit as used in the single-ended amplifier kept the negative output at ground so it obviously cannot be used in the double-ended case.

Figure 2.10 shows a block diagram of a circuit which expands on some of the details of the common-mode block of Figure 2.9. This cir-

Figure 2.9 Double-Ended Folded Cascode Opamp

Figure 2.10 Block Diagram of Common-Mode Suppression Circuit

circuit sums the two output voltages, compares it to zero volts then uses a filtered and level shifted version of this error voltage to control the current sources in the output stage. Level shift is required since the current source input is not nominally at zero volts when the outputs are both at zero volts. The type of loop filter and the gain are designed to achieve maximum common-mode suppression while maintaining stability. The need for linearity and operating range applies mainly to the summing circuit since it must deal directly with the output voltages. The rest of the circuit deals only with the error voltage which is nominally at zero volts. Some methods of summing will now be considered.

2.4.6.1 SUMMING OUTPUT VOLTAGES WITH RESISTORS

One possible summing circuit is simply two equal-valued resistors connected in series between the two outputs. The midpoint of the two resistors will be at zero volts only if the sum of the outputs is zero volts. This can be followed by an amplifier which can be nonlinear since it is behind the summing point, in the forward loop. The problem has been and still is how to realize the resistors in an integrated circuit such that they are linear over a wide voltage swing and do not load the high impedance output of the amplifier.

2.4.6.2 SUMMING OUTPUT VOLTAGES WITH TRANSISTORS

Another possible summing circuit sums the two output voltages using transistors. Over a narrow range, the output current of the transistors is proportional to the input voltage so two transistors can

be used to derive a current proportional to the sum of the output voltages. This has the advantage that the output is not loaded by the sensing device. This technique, however, is linear over a small range only. Linearity can be extended by a variety of techniques including the use of cross coupled small transconductance differential pairs for measuring the output voltage. An example is shown in Figure 2.11 [9]. A small size helps to increase the linear range as well as to decrease the gain around the common-mode loop for stability reasons. This method, while linear over a fairly wide range, cannot achieve rail to rail operation. The limiting effect occurs when an output swings far enough to cut off one of the transistors in the sensing differential pair so that further output swing does not result in a change of current. The feedback action around the common mode loop indicates that this output has stopped moving and the current is adjusted to prevent the other side from approaching the rail further. A more complicated circuit would be required to achieve a further swing. With many of the circuits using a sensing transistor, there is gain in two locations around the common-mode loop. If both gains are of the same order and rolled off by similar capacitance then the loop will be unstable. This stability problem and some solutions will be discussed later.

Transistors can also be used as resistors in the linear region. This can avoid some of the stability problems but linearity and operating range are still limited.

2.4.6.3 SUMMING OUTPUT VOLTAGES WITH SWITCHED-CAPACITORS

The approach which was used in this design was to use switched capacitors as shown in Figure 2.12 to perform the summing action in the common-mode loop of Figure 2.10. As well, capacitors are shown for instantaneous summing. This circuit should allow linear operation over a wide range since the switches are passive and potentially able to operate close to the rails. Since the midpoint of the two switched-capacitor resistors remains close to 0 volts, the rest of the common mode circuitry will operate over a wide range of output voltages. To limit the loading on the output, the switched-capacitor resistors should be as large as possible. This dictates the use of small capacitors in combination with a low switching frequency. To prevent the two outputs from being unbalanced, small capacitors must be carefully designed for matching. The two capacitors should have the same shape and should be equally affected by parasitic capacitance. A low clock frequency can result in clock feedthrough within the bandwidth of the opamp or OTA. Since the required resistance is high, switches can be of minimum size resulting in small overlap capacitance and low injected clock signal. Using switches with equal size p and n channel transistors and using complementary clocks will also cancel some of the injected signal.

2.4.6.4 ANALYSIS OF COMMON-MODE CIRCUIT

To evaluate the effects of the common-mode loop on the clock noise, power supply noise and stability, consider Figure 2.13 which shows a control type block diagram of the common-mode feedback loop. The blocks and nodes will be compared to the previous block diagram of the common-mode loop, Figure 2.10 and to the specific common-mode circuit as used in this thesis, Figure 2.12.

The blocks in Figure 2.13 are labelled as A, G and H. A represents the gain of the common-mode loop amplifier in Figure 2.10 and consists of a differential pair and two diode connected loads in Figure 2.12. The sum of the output of this block and V_{SS} noise (labelled as V_g) appear as the input to block G. In Figure 2.12, block G represents the gain of the current source transistors M10 and M11 and the cascode buffers M8 and M9 with an output V_o . The output is loaded by capacitor C and the output resistance R. H is the transfer function from the output to the input of the common-mode differential amplifier. This is the switched-capacitor network and the parallel capacitors C_f of figure 2.12. The output of block H and the clock noise are summed to form the voltage e_1 at the input of block A, to complete the loop. This summing action takes place at the input of the common-mode differential amplifier in Figure 2.12.

The clock noise V_c is derived from the clock signal by a capacitive divider as shown. C_i represents the equivalent overlap capacitance

Figure 2.13 Control Block Diagram of Common-Mode Loop

of the switches. C_f , the total capacitance to ground from the node labelled with V_c , serves to attenuate the amplitude of the clock noise V_c . As will be described later, this attenuation is provided by the capacitor, also labelled C_f in Figure 2.12, which is connected between the output and the input to the common-mode difference amplifier.

The blocks of Figure 2.13 will now be described in more detail. Equations will be derived and used to discuss the loop performance.

The block H consists of the switched-capacitor resistor and the parallel capacitor. Since this analysis is concerned with the instantaneous feedback loop, only the capacitive part of Figure 2.12 is pertinent. That is, the switched-capacitor path is never complete for this particular implementation. This leaves block H as a purely capacitive divider consisting of the capacitor C_f and the input capacitance to the common-mode amplifier. Thus, since C_f is relatively large, H represents a real number nominally equal to one.

G represents the gain from the gates of the current source transistors M_{10} and M_{11} to the output. The block G is thus modelled as a current source with transconductance g_m feeding into the output common-mode load (a capacitor in parallel with a resistor). The gain of this block is given by:

$$G = - \frac{g_m R}{1 + sCR} \quad (2.18)$$

In Figure 2.13, A represents the gain of the common-mode ampli-

CHAPTER 3 · BIQUAD DESIGN

3.1 INTRODUCTION

In Chapter 2 the design of opamps and transconductance integrators were discussed. In this chapter they will be combined to form biquad filters. First the biquad using discrete resistors, capacitors and opamps will be examined and then extended to the transconductance based biquad filter.

3.2 DISCRETE BIQUAD

Figure 3.1 shows the standard discrete biquad which uses resistors and capacitors to realise the various filter parameters. The transfer function of the filter is:

$$\frac{V_0}{V_I} = \frac{C_5}{C_2} \frac{s^2 + \frac{1}{R_1 R_2 C_1 C_5}}{s^2 + s \frac{1}{R_3 C_2} + \frac{1}{R_2 R_4 C_1 C_2}} \quad (3.1)$$

The parameters of interest are the pole and zero frequencies, the Q of the pole, the Q of the zero and the gain of the system. These parameters can be extracted by comparing the system equation to the standard second order equation:

$$s^2 + s \frac{\omega_0}{Q} + \omega_0^2 = 0 \quad (3.2)$$

where ω_0 is the frequency in radians per second of the pole or of the

result in expressions for power supply noise and clock noise. The closed loop transfer function of the general block diagram, Figure 2.10 is:

$$V_o = \frac{GAV_c + GV_s}{1 - GAH} \quad (2.21)$$

This can be solved for the specific circuit in Figure 2.12 by substituting equations 2.18 and 2.19 into 2.21. The overall closed loop transfer function becomes:

$$V_o = - \frac{g_m R A_0 V_c + g_m R V_s (1 + sT_0)}{s^2 (CR T_0) + s (CR + T_0) + 1 + g_m R A_0 H} \quad (2.22)$$

Since $g_m R$ corresponds to the DC gain A_1 in Figure 2.13 and CR corresponds to the time constant T_1 , the following equation can be written:

$$V_o = - \frac{\frac{A_1 A_0}{T_1 T_0} V_c + \frac{A_1}{T_1} \left(s + \frac{1}{T_0}\right) V_s}{s^2 + s \left(\frac{1}{T_1} + \frac{1}{T_0}\right) + \frac{1 + A_1 A_0 H}{T_1 T_0}} \quad (2.23)$$

This is an equation of a second order low pass filter to clock noise V_c with a zero in the path of the power supply noise V_s . Figure 2.14 shows the frequency response of a low pass filter. From (2.20), the zero order term in the denominator is the square of the unity gain bandwidth (if the 1 is ignored) of the open loop.

Figure 2.14 Low Pass Response of Common-Mode Circuit

Thus as seen in Figure 2.14, there is a low frequency gain for clock noise and power supply noise, with rolloff (and peaking if the Q is greater than 1) beginning at the unity gain bandwidth. Thus even if the low frequency gain is low, a high Q in the common-mode loop could cause excessive noise at the frequency of its unity gain bandwidth. It can be shown that the Q of the loop can be reduced by separating the two time constants, that is, by making one of the two poles dominant as was previously shown to be required for loop stability. The amount of pole separation required for stability is usually sufficient to result in a loop Q that is smaller than one. A simple example will demonstrate the effect on the Q of separating the poles. If the overall DC loop gain is 100 and the two time constants are the same, then the Q will be 5. This would result in the clock feedthrough being increased by a factor of 5 at the UGBW frequency. If, however, the ratio of the two time constants is increased to 25, the Q in this example would be reduced to about one. Therefore the dominant pole which is required for stability is also useful for suppression of peaking of the clock feedthrough and power supply noise.

For power supply noise, in (2.23), the term in V_s has a zero associated with it. However, this will normally occur at a high enough frequency to be of no importance. This is the case since the zero frequency is equal to the non dominant pole frequency which is at or beyond the loop UGBW.

Since it has been shown that the Q of the common-mode loop is low and the zero is of no importance, the worst case power supply noise

and clock noise can be expressed as the low frequency terms of (2.23) as follows:

$$V_O = -V_C/H - V_S/A_OH \quad (2.24)$$

The above equation shows V_O related to the power supply and clock noise by the respective feedback terms of $1/A_OH$ and $1/H$. A_O is the gain of the cascode current sources from the gates of M10 and M11 to the output. H is the gain from the output to the common-mode loop amplifier, ie. the common-mode gain of the summing circuit. Clearly both terms A_O and H must be as high as possible to reduce power supply and clock feedthrough noise. Since H is obtained from a passive network in this case, it can be as high as unity as was described in a previous section. H could be made to have a gain, as in the case of Figure 2.11, but this involves the use of transistors at the output with consequent nonlinearity and limited range.

Since H is equal to or less than 1, clock noise must be reduced by other means. As discussed in the beginning of the section, the clock input capacitance, (C_i of Figure 2.13) must be minimized. In addition, the capacitance C_f should be maximized. A capacitance cannot be put to ground from the input of the common-mode difference amplifier since this would decrease the feedback parameter H . The capacitors from the OTA output to the summing amplifier input also provides attenuation to the clock input and can be increased without changing H . These capacitors also contribute to the OTA differential load which limits how much they can be increased.

For power supply noise (V_s) the equation shows the need to keep both H and A_0 large. The size of A_0 will often be limited by the requirement for stability which is determined by the overall loop gain and the frequency ratio of the poles. The maximum frequency ratio of the poles is limited by the maximum allowed size of the output common mode capacitance and the minimum output common-mode resistance. This limits the overall loop gain and hence limits the value of the gain A_0 .

Thus it can be seen that most of the parameters in the common mode loop are interdependent and often a compromise has to be made in achieving acceptable performance. For example a high loop gain will keep the common-mode component of the output voltage low and will decrease the power supply noise but will decrease the stability. The use of switched-capacitors potentially adds clock noise and extra circuit complexity but removes the nonlinearities and limited range problems of transistor summing circuits. The arrangement of output loading capacitors involves another tradeoff. By connecting capacitors from each side to ground instead of using differentially connected capacitance, stability, common-mode cancellation and power supply rejection are improved. However, differentially connected capacitors require less total capacitance.

The rationale for the choice of the circuit of Figure 2.12 is now given. A low gain common-mode amplifier was chosen to ensure common-mode loop stability. This was achieved by having the load transistors diode connected. By having the current through the diode loads

derived from the bias circuit, the nominal output offset is low for any bias current. Linearity over a wide voltage range was achieved in the summing circuit by the use of switched-capacitor resistors. The resulting clock feedthrough noise was kept low by (i) minimizing the switch size, (ii) using complementary clocks, (iii) using a summing circuit with an instantaneous gain close to unity and (iv) using as large a value as possible for the capacitor in parallel with the summing circuit. The alternative choice of connecting a capacitor from the input of the common mode amplifier to ground was not used since this would decrease the instantaneous gain of the summing circuit.

The design of a high gain common-mode loop was initially considered. This used mirror connected loads in the common-mode amplifier of Figure 2.12. Simulations indicated that this circuit had significantly better power supply rejection than that for the low gain circuit. However, this circuit was abandoned due to its marginal common-mode loop stability.

2.4.7 OTHER APPLICATIONS OF THE COMMON-MODE CIRCUIT

Some of the circuit techniques shown in Figure 2.12 could be applied to some of the other designs previously discussed. One of the problems with the cross coupled transistor sensing circuit of Figure 2.11, was the instability due to high loop gain. This could easily be decreased by using the diode connected loads. This could make the circuit useful if its limited range could be tolerated. Another potential use of the common-mode circuit is in the single-ended amplifier

where the common-mode circuit could be used directly with the exception that only one output would be connected to the summing amplifier. This would force the output to be at ground as required. Balanced outputs are not required and due to the grounded output, operating range would not be of concern. Thus, in this application, the switched-capacitor summing network could be replaced with a transistor. This would be an improvement over the previously discussed offset circuit in that it would allow some increase in gain and would provide an offset circuit that tracks the bias current.

2.5 SUMMARY

In this chapter, the reasons for using a folded cascode amplifier as an OTA and the design of such an amplifier has been discussed. The input stage was studied in detail to derive equations describing the cutoff voltage, the common-mode range and the linearity as a function of the transistor size and bias current. It was concluded that linearity and cutoff voltage could be improved by decreasing the size of the input devices, but at the expense of the common-mode range.

For the single-ended amplifier, an offset correction circuit was shown to be necessary to keep the output at zero volts over a wide range of tuning currents. It was shown how the tuning range could be increased by deriving all bias voltages from a single tuning current.

For the double-ended amplifier, common-mode cancellation circuits were discussed. Many designs have problems with non linearity,

limited range or instability. The design used in this thesis to overcome these problems was based on a switched-capacitor summing circuit. This was discussed in terms of a control circuit. Expressions for loop gain, stability, clock noise and power supply noise were derived. A design was shown where the output voltage remained nominally at zero volts for any tuning current. This circuit could also be used as a further improvement to the single-ended amplifier.

CHAPTER 3 - BIQUAD DESIGN

3.1 INTRODUCTION

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The parameters of interest are the pole and zero frequencies, the Q of the pole, the Q of the zero and the gain of the system. These parameters can be extracted by comparing the system equation to the standard second order equation:

$$s^2 + s \frac{\omega_0}{Q} + \omega_0^2 = 0 \quad (3.2)$$

where ω_0 is the frequency in radians per second of the pole or of the

zero. Thus the parameters can be expressed as follows:

$$\omega_z = \frac{1}{(R_1 R_2 C_1 C_5)^{1/2}} \quad (3.3)$$

$$\omega_p = \frac{1}{(R_2 R_4 C_1 C_2)^{1/2}} \quad (3.4)$$

$$Q_p = \frac{R_3 C_2}{(R_2 R_4 C_1 C_2)^{1/2}} \quad (3.5)$$

$$Q_z = \text{infinity} \quad (3.6)$$

$$\text{GAIN}_{\text{DC}} = \frac{R_4}{R_1} \quad (3.7)$$

$$\text{GAIN}_{\text{HF}} = \frac{C_5}{C_2} \quad (3.8)$$

Figure 3.1 The Discrete Biquad Filter

Of course it must be realized that these expressions are valid for ideal components and in real life some of these parameters will not be achieved. In theory the Q of the zero is infinite meaning there will be a total cancellation of the signal at the zero frequency. This can be seen by noting that in the numerator of equation 3.1 there is no term in s . In practice any phase shift due to parasitics will cause the Q to be finite. The same problem occurs when trying to achieve a pole with a high Q . These effects will be studied in more depth in the section on transconductance biquads.

It is also important to note that the filter parameters are not all independent. For example, the ratio of zero frequency to pole frequency is equal to the ratio of DC gain to high frequency gain. Thus, if the pole and zero frequency are set then only one of the gains can be set independently. The Q of the pole can still be set with R_3 .

3.3 SINGLE-ENDED TRANSCONDUCTANCE BIQUAD DESIGN

The transconductance equivalent of the continuous biquad can be realized in its most general form by replacing each resistor with an OTA. The result is the filter of Figure 3.2a with a corresponding transfer function. It is however possible to realize simpler (but less flexible) versions of the biquad filter. Simplifications can be realized by using both positive and negative inputs of the OTA to realize the equivalent of two resistors with the same differential pair. Some examples are shown in Figures 3.2b and 3.2c. Note that in each case some degree of flexibility appears to have been given up. In the trans-

fer function for the filter using two OTAs, the Q can no longer be tuned independently. It would be possible to tune the Q with g_{m2} but then corrections would have to be made with g_{m1} to prevent the pole and zero frequencies from changing. In the biquad using three OTAs, seen in Figure 3.2c, the addition of OTA3 has allowed the Q to be tuned independently. The equation indicates that for both of these biquads the zero and pole both occur at the same frequency. This however can be remedied by splitting the capacitor C_2 as shown in Figure 3.2d, with the resulting transfer function:

$$V_o = \frac{C_5}{C_2 + C_5} \frac{s^2 + \frac{g_{m1}g_{m2}}{C_1C_5}}{s^2 + s \frac{g_{m3}}{C_2 + C_5} + \frac{g_{m1}g_{m2}}{C_1(C_2 + C_5)}} \quad (3.9)$$

The equation shows the pole to zero frequency as the capacitor ratio $C_5/(C_2+C_5)$. This means that the spacing can be very accurately determined. However there is still a loss of flexibility in that the zero frequency is constrained to be above the pole frequency. This constraint can be removed by returning to the original general form of the filter as shown in Figure 3.2a. The filter using four OTAs does not actually need to have twice the number of components contained by the

filter using two OTAs. Since OTA2 and OTA3 feed current into the same integrating capacitor, it is possible to use two input differential pairs feeding current into a single output stage. Thus going from the filters using two OTAs to filters using four OTAs is a matter of adding two input differential pairs and their current source transistors. Of course it is necessary to design the output stage in such a way that it can handle the combined DC current of the two input stages.

3.3.1 INCLUSION OF FINITE GAIN AND PARASITIC POLES

The transfer functions were generated by modelling the OTA as an ideal voltage controlled current source. This results in a perfect cancellation at the zero frequency and an infinite Q. However, practical OTAs have finite gains as well as parasitic poles which add extra terms to the transfer functions. In particular, these effects reduce the Q of the zeros as shown in the following analysis.

The finite DC gain can be included without increasing the order of the transfer function by adding an equivalent resistor from each output to ground. This will cause the DC gain to be $g_m R$ rather than infinity. Addition of parasitic poles will increase the order of the transfer function equation to a fourth order. Instead of adding an extra pole to the OTA model and solving the resultant 4 by 4 matrix equation, a transfer function can be derived without the parasitics, then each occurrence of g_{m1} and g_{m2} can be replaced by a term which includes the parasitic pole. The transfer function, including the finite DC gain, but not the parasitics, is:

$$V_o = \frac{C_5}{C_2 + C_5} \frac{s^2 + \frac{s}{R_1 C_1} + \frac{g_{m1} g_{m2}}{C_1 C_5}}{s^2 + s \left(\frac{g_{m3} + 1/R_2}{C_2 + C_5} + \frac{1}{R_1 C_1} \right) + \frac{g_{m1} g_{m2} + 1/R_1 (g_{m3} + 1/R_2)}{C_1 (C_2 + C_5)}} \quad (3.9)$$

The zero order term in s in the numerator is equal to $(\omega_z)^2$, the square of the zero frequency. If now both of g_{m1} and g_{m2} are divided by the term $(1+sT)$ and s is replaced by $j\omega_z$ the numerator of the equation becomes, at ω_z :

$$(\omega_z)^2 \left[\frac{-2j\omega_z T + (\omega_z T)^2}{(1 + sT)^2} + \frac{j}{\omega_z R_1 C_1} \right] \quad (3.10)$$

This expression can be simplified by noting that the parasitic pole frequency is much higher than the zero frequency and therefore the term $\omega_z T$ is much less than 1. Thus the second term in the expression is much smaller than the first and can be ignored. Likewise, at the zero frequency, $(1+sT)$ is nearly equal to 1 and so can be ignored as well. The resulting simplified form of (3.10) can be compared to the general equation (3.2) to derive an expression for Q . Then the final expression is:

$$\frac{1}{Q_z} = \frac{1}{\omega_z R_1 C_1} - 2T\omega_z = \frac{\omega_{LF \text{ pole}}}{\omega_z} - \frac{2\omega_z}{\omega_{par \text{ pole}}} \quad (3.11)$$

This expression shows how the Q of the zero is affected by the

low frequency pole of the first OTA and the parasitic poles. This shows that it is possible to balance the phase lead due to the low frequency pole with the phase lag due to the parasitic poles to obtain high Q zeros. It is interesting to note that only one of the dominant poles appears in the expression. This means that the parasitic poles must be twice as far from the zero frequency as the zero frequency is from the dominant pole. In this way, each will contribute roughly half of the phase shift required to match the phase due to the dominant pole. The parasitic pole frequency is limited so it may be necessary to increase the frequency of the dominant pole and hence to decrease the DC gain. This does not affect the filter DC gain much if it is designed to have unity gain at DC. The DC gain error can be shown to be equal the inverse of the integrator gain at DC multiplied by the ratio of g_{m3} to g_{m2} . This ratio will usually be much less than 1 since it represents the inverse of the Q of the pole. As an example, a low DC gain of 20 per integrator when combined with a pole with a Q of 5 would result in a filter DC gain error of only 1%.

In a biquad filter, the effectiveness of the zero in producing a notch is reduced by a nearby pole. The actual gain at this frequency can be found by substituting $s = j\omega_z$ into the standard form for a biquad filter with the result:

$$\frac{V_o}{V_i} = \frac{Q_p/Q_z}{r - jQ_p(1-r^2)} \quad (3.12)$$

Where r is the ratio between the frequencies of the zeros and the poles. This equation shows that if the poles and zeros are closely

spaced then the gain at the frequency of the zero will be the ratio of the Q of the pole to the Q of the zero. In this case, if the Q of the pole has a fixed value, the gain at the zero frequency can be used directly as an indication of the Q of the zero.

3.4 DOUBLE-ENDED TRANSCONDUCTANCE BIQUAD DESIGN

It is often desirable to use differential filters for reasons of power supply rejection, cancellation of even harmonics or noise rejection.

In double-ended filters, double-ended amplifiers with well balanced outputs as developed in Chapter 2 are used. The capacitors must present the same load to both outputs. Since most capacitors in integrated circuit technology are not balanced, they cannot simply be connected between the two outputs but must be split into two capacitors in parallel or series.

For differential filters, each OTA is used in the balanced sense so it is no longer possible to use both inputs to realize separate resistors as was done in simplifying Figure 3.2a to 3.2b. Thus it is necessary to implement the biquad in the general form. Such a realization is shown in Figure 3.3. Each of the OTAs of the single-ended filter has been replaced by a double-ended OTA. The integrating capacitors have been shown from the outputs to ground. Capacitors to ground are required for common-mode loop stability and noise performance, as discussed in Chapter 2, though it is possible to reduce the total area

Figure 3.3 Double-Ended OTA Based Biquad Filter

of the integrated capacitors by connecting part of the capacitance differentially.

The transfer function of the filter can be found by applying the equation for the double-ended OTA as shown in Chapter 2:

$$i_o = g_m \left(\frac{V_+ + V_-}{2} \right) \quad (3.10)$$

where g_m is the transconductance of each input transistor. Note that in the single ended case, the output current was twice as large because of the current doubling action of the offset circuit. By applying this equation and assuming that the negative outputs are exactly the inverse of the positive outputs, the following transfer function results:

$$V_o = \frac{C_5}{C_2 + C_5} \frac{s^2 + \frac{g_{m1}g_{m2}}{C_1C_5}}{s^2 + s \frac{g_{m3}}{C_2 + C_5} + \frac{g_{m4}g_{m2}}{C_1(C_2 + C_5)}} \quad (3.11)$$

It can be seen that this equation is the same as that for the single ended filter. However as noted above, the output current is halved and the voltage from each output to ground is halved. In addition the total capacitance is doubled.

3.5 SUMMARY

In this chapter biquad filters have been discussed, in particular, biquads that include a zero in the transfer function. The biquad using discrete resistors and capacitors was first examined and expressions derived for the pole and zero frequencies, the Q and the gains.

The single-ended OTA based biquad was derived by replacing each discrete integrator with an OTA integrator. A circuit was shown where a zero could be implemented. The transfer function indicated that the ratio of the pole to zero frequency was determined by a capacitor ratio which can be very precise. The quality of the zero depends on the phase of the integrator. Finite DC gain and parasitic poles have opposite effects on the phase shift so can be designed to balance and to allow a high Q design. It was shown that if the pole frequency and zero frequency are nearly the same, the gain at the zero frequency is equal to the ratio of the Q of the pole to the Q of the zero.

The double-ended biquad filter required four OTAs. It was shown that if the integrating capacitors were connected to ground, then the total capacitance would be twice that for the single-ended OTA based biquad. The use of differential capacitors could reduce the total amount of capacitance but at the expense of power supply rejection and clock noise.

CHAPTER 4. SIMULATIONS AND MEASUREMENTS

4.1 INTRODUCTION

In previous chapters, designs and design equations have been presented for transconductance amplifiers, integrators and biquad filters. Based on these theoretical considerations, a total of four test chips were designed. Two different CMOS processes were used. In this chapter, simulation and measurement of these devices will be presented and compared to theory and to the design objectives. This will include a description of the technologies. As well the tools used for layout, simulation and measurement will be discussed.

4.2 TEST CHIP CONTENTS AND TECHNOLOGY

Of the four test chips, the first two were fabricated in the Northern Telecom (NT) 5um process, CMOS1B, while the last two were designed using the NT 3um process, CMOS3. Some implications of the different processes will be seen in section 4.4. The first three test chips were submitted to the Canadian Microelectronics Corporation (CMC) for fabrication while the last one was part of a test chip to be fabricated directly by NT. The first chip included single-ended opamps and single-ended transconductance biquad filters. The first chip had a number of design rule violations, an error in the bias circuit design and missing connection to the output buffer. In spite of the errors, some measurements were still possible. The second chip corrected all the errors of the first chip. The third and fourth test chips, designed in the CMOS3 process, included both single-ended and double-ended

opamps and biquad filters. Also included was an EPROM based circuit to be used for tuning purposes, as will be discussed in Chapter 5. Figure 4.1 shows a photomicrograph of the first chip.

4.3 LAYOUT AND VERIFICATION TOOLS

Layout of the CMOS1B design was carried out using the Metheus work station at Carleton University, using the physical layout editor (PHLED). Simulations were performed using Spice and CMC provided parameters. The rule checker was not available for the first test chip so it was not error free. This caused some problems with the measurement. Later designs were all checked before fabrication.

The layout of the CMOS3 design was done partially at Carleton using PHLED, and partially at Northern Telecom using their layout editor (LAYED). This was basically the same design as the 5um versions but modified for the 3um process. This involved extensive simulation to account for the differences in parameters as well as for the reduced operating voltage of ± 2.5 volts as compared to the previous ± 5 volts. Circuit improvements were also found to be necessary for correct operation of the bias circuit. In addition, a double-ended version was also designed. Simulations were done with Spice level 2 at Carleton and with the BNR-designed simulator, Scamper, at Northern Telecom.

4.4 MEASUREMENT TOOLS

All of the measurements were done on dual inline packages thus no use was made of special test apparatus like wafer probers. This

Figure 4.1 Photomicrograph of the First Test Chip in CMOS1B.

allowed measurements to be made with simple tools like signal generators, oscilloscopes, spectrum analyzers and multi-meters. However in some cases this was a limiting factor where probes added too much capacitance to output drivers and thus prevented measurements of unity gain bandwidth. No measurements have yet been performed on the 3 μ m opamps and filters as they are still in fabrication. For these devices, only simulation results will be presented.

4.5 SIMULATION PARAMETERS

Table 4.1 highlights some of the differences in simulation parameters between CMOS1B and CMOS3, as supplied by the Canadian Microelectronics Corporation [12]. Inspection of the parameters indicates several advantages of CMOS3. The reduction of feature size from 5 μ m to 3 μ m will allow for more compact designs. CMOS3 will be able to operate at higher frequencies since the transconductance and currents are increased due to decrease in oxide thickness, higher mobility and lower thresholds. In addition, parasitic capacitances will be reduced due to the smaller feature size. However, the decrease in oxide thickness forces a reduction in operating voltage to prevent breakdown.

The design rules for CMOS3 were intended to be compatible with CMOS1B. This would allow the use of a scaled version of the CMOS1B design for CMOS3. However in analog design the parameter changes do not allow a direct scale. Due to the reduction in oxide thickness, the reduction in threshold voltage and the increase in mobility, a transistor in CMOS3 with the same (W/L) as one in CMOS1B would have signifi-

	CMOS1B	CMOS3	UNITS
Minimum Dimension	5	3	um
Oxide Thickness	.085	.050	um
Electron Mobility	750	775	cm ² /Vs
Hole Mobility	240	250	cm ² /Vs
n Transistor Constant k_p	30	50	uA/V ²
p Transistor Constant k_p	9.5	16	uA/V ²
n Threshold Voltage V_{T0}	0.9	0.7	V
p Threshold Voltage V_{T0}	-0.9	-0.8	V
Analog Rail V_{DD}	5	2.5	V
Analog Rail V_{SS}	-5	-2.5	V

TABLE 4.1 Simulation Parameters for CMOS1B and CMOS3 as supplied by CMC.

cantly more current and a higher transconductance. In addition, the change of operating voltage from ± 5 volts to ± 2.5 volts means that the bias circuits must be redesigned. To achieve a sufficient output swing with the reduced operating voltage requires that special attention be paid to the design of a wide output swing bias circuit [10].

In the following sections, an example curve is usually shown for each type of simulation to show the behavior of the circuit. Due to the scale used on these diagrams, precise values cannot be determined from them. The tabulated values have been obtained from expansions of similar curves.

4.6 SIMULATION AND MEASUREMENT OF OPAMPS AND OTA INTEGRATORS

Figure 4.2 shows the single-ended opamp which was realized in CMOS1B and in CMOS3. The OTA integrators use the same design as the opamps except for a smaller device sizes in the input stage and larger integrating capacitors at the output. Figure 4.3 shows the bias circuit which was used for the CMOS1B design and the improved bias circuit which was used for the CMOS3 design. Note that the bias current of the CMOS3 opamps is equal to the bias circuit input current I_1 multiplied by 4 due to the ratio of 4 in the mirroring circuit. Figure 4.4 shows the double-ended opamp which was realized in the CMOS3 process. The design is the same as for the single-ended opamp except for the replacement of the offset cancellation circuitry with the common mode circuitry.

4.6.1 DC BEHAVIOR

Figure 4.5 shows a simulation of the DC transfer function of the 5um OTA integrator at a bias current of 40uA. The nonsymmetrical shape of the currents through the input transistors occurs because the input voltage was applied from one side to ground. Thus as the input voltage increases, the source voltage also increases which causes an increase in current due to the finite output impedance of the current source. The current through the input transistors allows an estimate of transconductance, cutoff and linearity. Transconductance is the ratio of the change of output current with the change in the input voltage. In the linear region, with a single-ended input, the source voltage change is

Figure 4.2 The Single-Ended Opamp

Figure 4.3 The Bias Circuits

Figure 4.4 The Double-Ended Opamp

Figure 4.5 DC Transfer Function of 5um Single-Ended OTA (Simulation)

half of the gate voltage change. Thus transconductance of the input transistor is twice the slope of the current versus the input voltage curve. This is about $34\mu\text{A/V}$. Cutoff, where the current in one of the transistors falls to zero, occurs at about 1.8V. Linearity can be seen by comparing a straight line with the actual line and noting the difference. A rough estimate from the curve shows that linearity is about 10% in error at just over 1V (in the negative direction). The slope of the output voltage curve is the DC gain and is 157 in this case. The negative output is also shown. The slope of this curve is a measure of the performance of the offset circuit. For the CMOS1B OTA the gain to the negative output is about 0.3. Table 4.2 compares the DC behavior of the opamps and integrators to the simple theoretical equations of Chapter 2. The transconductance g_m has been calculated from (2.2) and cutoff has been calculated from (2.9). The entry in the table for simulated cutoff represents the input voltage required to reduce the current by 90%.

The most notable difference between the OTA integrator and the opamps is the much lower transconductance and voltage gain due to the reduced device size of the input pair. This allows the OTA integrator to operate linearly over a much wider input voltage range. The simple square law theory is seen to give a good estimate of operating performance. This was especially useful in designing the CMOS3 circuit with nearly the same cutoff voltage as for the CMOS1B design.

The DC gain of the single-ended CMOS3 design can be seen from Table 4.2 to be about twice as high as for the double-ended design.

		I_1	g_m		DC GAIN	cutoff		other
		(μA)	($\mu A/V$)		(V/V)	(V)		
			theor	sim	sim	theor	sim	conditions
CMOS1B	OPAMPS	40	279	190	1025	.143	0.19	$I_{CASC} = 25\mu A$
	OTA	40	34.9	30.2	157	1.14	1.45	$I_{CASC} = 25\mu A$
CMOS3	OPAMPS	100	506	520	866	.198	.20	for CMOS3, $I_{BIAS} = 4I_1$ nominally
	SE OTA	100	105	104	193	0.95	0.9	
CMOS3	OPAMPS	100	506	451	450	.198	.20	nominally
	DE OTA	100	105	102	99	0.95	.97	

Table 4.2 DC Behavior of Opamps and OTA Integrators. Theoretical g_m from eq 2.2, cutoff from eq. 2.9 simulated cutoff: to 90%

The reason for this difference is that the switched-capacitor resistor is loading the output at DC.

4.6.2 DC LEVELS WHEN TUNING

Figures 4.6 and 4.7 show the DC current and voltage variations for the opamps of Figures 4.2 and 4.4 when the bias current is varied. These curves will be used to discuss the tuning range, and output voltage offset. The variations are due largely to the choice of bias circuit (Figure 4.3) and the configuration of the output offset or common mode feedback circuit.

Figure 4.6 shows the current variations in the single-ended OTA of Figure 4.2 as realized in both the CMOS1B and the CMOS3 process. Currents are shown through transistor M1 in the input stage as $I(M1)$

and through the cascode chain as $I(M10)$. As seen in Figure 4.6, the OTA in the CMOS3 process was designed to operate at higher currents than the OTA in the CMOS1B process. The relationship of the input stage current to the cascode chain current is different for the two designs due to the use of different bias circuits. The simple bias circuit was used in the design in the CMOS1B process. The result is that the cascode current decreases as the bias current increases. This limits the tuning range. The CMOS3 design used the improved bias circuit where the cascode chain is tuned in proportion to the input current, and the cascode current is seen to follow the input stage current. In this case the current range limitation occurs when some of the transistors leave the saturated region of operation.

Note that the current $I(M1)$ is nominally related to the bias circuit input current I_1 by a factor of $1/2$ for the design in the CMOS1B process and by a factor of 2 in the CMOS3 process. This is due to the difference in the current mirror ratio in the two bias circuits.

Figure 4.7 shows the output voltage of the three types of OTA integrators (CMOS1B single-ended, CMOS3 single and double-ended) in response to the variations of the tuning current. The output voltage variations in this figure can be discussed in relation to the design of the offset circuit and the common mode circuit of Figures 4.2 and 4.4. Both of the single-ended designs show a large variation in output voltage, due to the low gain of the offset circuit. The difference in

Figure 4.6 Current Changes with Variations of Tuning Current

Figure 4.7 Voltage Changes with Variations of Tuning Current

the bias circuits accounts for the improvement from 0.85V in the CMOS1B design to 0.65V in the design in the CMOS3 process. The CMOS3 double-ended OTA shows a 0.1V variation in output voltage. This large improvement occurs because the common mode loop is referenced to the bias circuit.

The discussions show the advantages of the improved bias circuit of the CMOS3 designs in allowing a large tuning range. They also show the benefits of the common-mode loop of the double-ended design in reducing the output voltage variations when the bias current is varied. It should be possible to use similar circuit techniques to improve the offset circuit of the single-ended OTA integrators..

4.6.3 FREQUENCY RESPONSE

Figures 4.8 and 4.9 show the frequency response of the buffer opamps at the nominal bias currents. This shows a UGBW of 18MHz for the opamp in the CMOS1B process and 41MHz for the CMOS3 process. Measurement results for the first test chip in CMOS1B showed a much lower UGBW due to the capacitance of the pads, the capacitance of the probes and the requirement to operate at a lower bias current due to an error in the bias circuit.

Figures 4.10 and 4.11 show the frequency response of the OTA integrators at various bias currents. The results obtained from expanded versions of these figures are summarized in Table 4.3. It is noted that the UGBW increases for increasing bias current in proportion to

Figure 4.8 Frequency Response of Single-Ended Buffer Opamp CMOS1B

Figure 4.9 Frequency Response of Single-Ended Buffer Opamp CMOS3

Figure 4.10 Frequency Response of Single-Ended OTA Integrator CMOS1B with Simple Bias Circuit

Figure 4.11 Frequency Response of Single-Ended OTA Integrator CMOS3 with Improved Bias Circuit

	I_1 (μA)	DC GAIN (dB) sim	UGBW sim	PHASE AT UGBW (degrees)	other conditions	
CMOS1B	OPAMP	40	60.2	17.2 MHz	-135	$I_{CASC} = 25\mu A$
	OTA	5	33.8	180 kHz	-89.1	$I_{CASC} = 25\mu A$
	OTA	40	44.1	463 kHz	-90.5	$I_{CASC} = 25\mu A$
	OTA	80	50.4	620 kHz	-91.5	$I_{CASC} = 25\mu A$
CMOS3	OPAMPS	25	58.5	41.6 MHz	-122	
	OTA	0.2	59.0	200 kHz	-90.63	
	OTA	1	57.3	382 kHz	-90.65	
	OTA	5	53.0	777 kHz	-90.61	
	OTA	25	45.9	1.60 MHz	-90.45	
	OTA	100	42.0	2.63 MHz	-90.60	

TABLE 4.3 Frequency Response of Buffer Opamps and OTA Integrators

the square root of the current. With the cascode current related to the input current, as in the OTA integrators in the CMOS3 process, the DC gain is expected to decrease as the bias current increases. This is because as the g_m of the input pair increases, the output resistance decreases by a larger amount. Thus the DC gain, which is equal to the product of the g_m and the output resistance, decreases. For this reason, the phase curves of Figure 4.11 also move to higher frequencies as the bias current is increased, and the phase at the UGBW frequency is nearly independent of frequency. This is seen in Table 4.3. The OTA integrators in the CMOS1B process, however, use a fixed cascode bias. As the bias current is increased, the cascode current actually decreases as was seen in Figure 4.6. For this reason, in Figure 4.10, the DC gain increases and the phase curves move to lower frequencies with

increasing bias current. Thus the phase at the UGBW frequency shows large variations over the tuning range as is shown in Table 4.3.

Some further attempts were made to improve the performance of the OTA integrators. It was found to be possible to increase the DC gain by increasing the length of the output transistors. However, the added size also caused an increase in parasitic capacitance which lowered the frequency of the parasitic poles. Thus the increase in DC gain was at the expense of bandwidth. The phase for the CMOS3 OTA integrators of about -90.6 degrees indicates that the parasitic pole is relatively too close to the UGBW with respect to the dominant pole. Thus, a reduction of DC gain is required to bring the phase closer to -90 degrees. For this reason, all cascode transistors were left at the minimum length.

4.6.4 COMMON MODE LOOP STABILITY

As discussed in section 2.4.5, stability is an important part of the design of the common mode loop. One of the two gain stages in the common mode loop, the current source (M10 and M11 in figure 4.4) is fixed by the differential requirements. Thus the design of the second gain stage, which is the differential measuring amplifier, will determine the stability of the loop. The current source stage was determined by simulation to have a gain of about 53dB and a UGBW at about 15MHz. The common mode measuring amplifier is constrained to have a low gain to keep the UGBW below the frequency of the parasitic poles, which occur at about 40MHz. The amplifier which is used in this design has a

low gain - due to its diode-connected load, as shown in Figure 4.4. The gain is half of the ratio of the input pair transconductance to the load transconductance. With p-channel input transistors and n-channel loads, it is difficult to achieve a gain higher than unity with typical size transistors. Figure 4.12 shows the stability analysis of the common mode loop. The gain of the common mode difference amplifier is seen to be -3.4 dB. This results in a loop UGBW of 11.2 MHz with a phase margin of 75 degrees. A somewhat higher common mode loop gain could be useful to improve the power supply rejection, and would still provide adequate stability. It would be possible to increase the size of the input transistors, but to double the gain requires an increase in (W/L) by a factor of four. Another alternative would be to use an n channel differential stage with p channel loads. This could increase the gain significantly if desired, but would require a change of polarity in the feedback loop.

4.6.5 POWER SUPPLY REJECTION

Table 4.4 shows the simulation results for the power supply rejection at low frequencies and at the UGBW. A resistor was connected from the input of the bias circuit to ground to provide the bias current. Other methods of deriving the bias current are available and will affect the PSRR. For example, the resistor could be connected to the power rail or a current source could provide the current. (With a resistor to V_{DD} , in general, the V_{DD} rejection is degraded and the V_{SS} noise rejection is improved.)

Figure 4.12 Stability Analysis of Common-Mode Loop. Open Loop Magnitude and Phase Analysis.

			V _{DD} REJECTION		V _{SS} REJECTION	
			DC	at UGBW	DC	at UGBW
CMOS1B	OTA	SE	53.3	69.5	29.3	58.1
CMOS1B	OPAMP	SE	54.7	58.3	38.6	44.4
CMOS3	OTA	SE	26.3	64.3	11.7	50.5
CMOS3	OPAMP	SE	24.4	49.4	11.1	36.2
CMOS3	OTA	DE	44.6	47.1	34.2	29.2
CMOS3	OPAMP	DE	41.1	42.7	38.1	31.8

Table 4.4 Power Supply Rejection in dB of Opamps and OTA Integrators.
SE is single-ended. DE is double-ended output with rejection from each output.

The single-ended amplifiers were designed without much consideration to power supply rejection, and this is reflected, in particular, in the CMOS3 SE columns of Table 4.4. However, the behavior is surprisingly much better at the UGBW frequency, because the capacitor from the output to ground improves the power supply rejection at these frequencies. The size of the output capacitor for the OTA integrator is five times the size of the buffer opamp output capacitor. For this reason, the OTA shows a power supply rejection at the unity gain bandwidth that is better than that of the corresponding buffer opamp by a factor of about five (or 14 dB). The V_{SS} rejection is worse than the V_{DD} rejection, probably related to the design of the offset circuit. More work needs to be done on power supply rejection for the single-ended amplifiers.

For the double-ended buffer opamp and OTA integrators, the common mode cancellation circuit was designed with power supply rejection as one of the considerations. This resulted in a reasonably flat and acceptable power supply rejection. The OTA in general does not show any improvement over the opamp since the common mode capacitive load was the same in both of the designs. The additional capacitance of the OTA was placed differentially between the two outputs. Further improvements could be made by increasing the gain of the common mode loop by increasing the size of the differential transistors, or by modifying the circuit so that n channel input devices are used. This circuit could also be used for the single-ended amplifiers in a slightly modified form.

4.6.6 CLOCK FEEDTHROUGH

Clock feedthrough is of concern in the double-ended amplifier and integrator since the common mode feedback uses a switched-capacitor network. Figure 4.13 shows a time domain analysis showing the clock feedthrough of the OTA integrator. A four phase clock at 5 MHz with 5 ns rise and fall times was used in the simulations. The required initial conditions were found by simulating the OTA using the continuous equivalent of the switched-capacitor common mode circuit. The steady state values used were 0V at the inputs and 68.4mV at the outputs and at the input of the common mode differential amplifier. The bias circuit was also replaced by constant voltage sources to speed up the simulation. The initial transient appears to last about 2 μ s; then a steady state is reached. If the initial conditions are further from the

Figure 4.13 Clock Feedthrough of Differential OTA Integrator

steady state, the output takes a long time to settle, in fact longer than would be predicted by the continuous equivalent time constant of τ_{eq} . This shows the importance of starting with values as close to the steady state as possible. In the steady state, the output is seen to repeat itself at the clock rate. The peak to peak swing on the output is simulated to be 8.8mV, which is equivalent to a few millivolts RMS.

The clock feedthrough noise at the output is expected to be different for the different phases of the clock. On the edge of phase one, the output voltage changes suddenly since noise is injected capacitively into the output. On the edge of phase two, the output voltage changes more slowly, due to the limited frequency response of the common mode loop.

From equation 2.24, since the feedback factor H has been limited to unity, the clock noise can be reduced by decreasing the equivalent clock input, V_c , which is determined by the capacitive divider formed by the net overlap capacitance, C_i , and the capacitor it feeds into, C_f . C_i has been minimized by using minimum size transistors for the switches. C_f could be increased, but this also increases the differential load on the opamp so an equivalent amount would have to be removed from the outputs to ground.

Clock noise at the output would limit the dynamic range at that frequency. However, for a low pass or bandpass filter operating in the 1 to 2MHz region, the clock feedthrough is out of band and should not cause problems. Common mode signals at more than half the sampling rate

will cause the common mode cancellation to be incorrect. However, as long as the output signal is purely differential then aliasing should not occur even at frequencies close to the sampling frequency. More work is still needed on the combined effects of a desired output signal and the clock feedthrough. It is possible that the effect will produce clock feedthrough at higher amplitude than for steady state. The simulated response relies on accurate models of transistor parasitics. Measurement is obviously needed to arrive at actual values of clock feedthrough under various conditions.

4.7 SIMULATIONS AND MEASUREMENTS OF BIQUAD FILTERS

Figures 4.14 and 4.15 show the single-ended and double-ended OTA based biquad filters as discussed in Chapter 3. The nominal pole frequencies were chosen at 455kHz for CMOS1B and 1.6MHz for CMOS3. The ratio of the integrating capacitors and feedforward capacitors were chosen to result in a zero to pole frequency ratio of 1.05 as discussed in section 3.3. OTA1 and OTA4 were realized as one OTA in the single-ended filter and as two differential pairs feeding into the same cascode stage in the double-ended filter. OTA2 and OTA3 were realized in both the single-ended and double-ended filters as two differential pairs connected to the output cascode stage, with relative sizes and currents selected to realize a Q of about 5.

Measurements have been made on the CMOS1B filters and will be compared to simulation results. The CMOS3 devices were not fabricated in time to allow measurements for this thesis so only simulation re-

Figure 4.14 The Single-Ended OTA Based Biquad Filter

Figure 4.15 The Double-Ended OTA Based Biquad Filter

sults will be presented.

4.7.1 FREQUENCY RESPONSE

Figure 4.16 shows the frequency response of the CMOS1B OTA based biquad filter at several bias currents. Both simulations and experimental results are shown with good agreement. The response is that of a low pass with a notch at the zero frequency. Since the pole and zero are closely spaced, the notch depth can be used as an indication of the Q of the zero as discussed in section 3.3.1. As bias current increases, the notch frequency also increases. The figure indicates that the notch depth is maximum for an input current of about 20uA where the phase of the integrators is closest to 90 degrees as shown in Table 4.3. Figure 4.17 and 4.18 show the measured notch depth and notch frequency versus bias current for the first and second test chips in CMOS1B. In both figures, the notch frequency increases as the square root of the bias current as would be expected from (2.2). In the first test chip (Figure 4.17), the anomalous behavior at high bias current is due to bias problems which were corrected in later designs. In both figures there is an optimum bias current to obtain the deepest notch. It was shown in the second test chip that the optimum bias current depended on the choice of the cascode current and in particular if the cascode current was increased, the optimum bias current could be increased. The explanation as given in Chapter 2 is that at higher cascode current, the DC gain drops and the dominant pole moves to a higher frequency. Thus the phase lead it provides is increased and can balance a larger phase lag as would occur at higher frequencies.

2

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MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS
STANDARD REFERENCE MATERIAL 1010a
(ANSI and ISO TEST CHART No. 2)

CHAPTER 5 TUNING CONSIDERATIONS

5.1 INTRODUCTION

There are many reasons why tuning considerations are important. Because of variations in parameters, the actual frequency of operation could be quite different from the desired frequency. The main transistor parameters that are variable from wafer to wafer are the transconductance and the threshold voltage. In addition, capacitor values are likely to vary from one wafer to the next. Frequency change with time can be caused, in the short term, by temperature changes and over the long term, by aging or repeated stress. A well designed tuning circuit must ensure that the filter continues to operate at the right frequency in spite of all of these factors.

In this chapter, several methods of tuning are examined. The first is called continuous tune, where the performance of the filter, or of a similar master filter is continuously compared to the ideal performance and corrections are made. This allows the filter to track variations in processing as well as variations in time such as drift and temperature change. The second method is called pretuning. In this case, the filter is tuned once to compensate for processing variations. Other variations must be minimized through circuit techniques. It is also possible to use some combination of continuous tune and pretune to benefit from the advantages that each of them can offer.

Figure 4.17 Measured Notch Frequency and Notch Depth versus Bias Current for First CMOS1B Submission

Figure 4.18 Measured Notch Frequency and Notch Depth versus Bias Current for Second CMOS1B Submission

Figure 4.19 shows the simulated frequency response of the CMOS3 OTA based biquad filter. With input currents from 0.1uA to 100uA the notch frequency is seen to vary from 160kHz to 2.6MHz. The notch depth for this range of bias currents is nearly constant at -19dB.

The capability of obtaining a notch which is tunable over a large frequency range and has a nearly constant depth over this range is in large part due to the improved bias circuit. With the cascode current proportional to the bias current, the integrators are capable of operating at very low and to moderately high bias currents. The high current operation is limited by the voltage required to keep the transistors in saturation. Well before the current of 100uA, some of the transistors are no longer in saturation which explains why for the high currents the frequency is smaller than expected, and the Q of the zero is beginning to degrade. For a current change of 1000 times, the expected frequency change would be 31 times, instead of the observed change of 16 times. Because the integrator had a nearly constant phase over the range of bias currents, the notch depth was expected to be nearly constant. The phase was different from the ideal by about 0.6 degrees at the pole frequency. The expected notch depth is roughly equal to the sine of twice the phase error times the Q of the pole. At 0.6 degrees this is equal to 19.6 dB.

This shows the success of the bias circuit in allowing operation over a very wide range. It also demonstrates the need for the integrators to have a phase of 90 degrees at the UGBW.

Figure 4.19 Frequency Response of CMOS3 Biquad Filter with improved Bias Circuit

4.8 SUMMARY

In this chapter, four designs of the OTA based biquad filters were simulated and the results were compared to measurements. The design environment was briefly described and the technology and its influence on the design was discussed.

Simulation results were first shown for the opamps and integrators. This included DC response, frequency response and power supply rejection. The redesign of the bias circuit for the last two design test chips was shown to be beneficial in allowing an increased frequency range of operation. In the double-ended OTA, the design of the common mode circuit was shown to provide lower offset than for the single-ended OTAs. A similar design could be used to improve the performance of the offset circuits. It was also shown for the double-ended design that power supply noise could be reduced. In the single-ended circuits, power supply noise though simulated, was not part of the design criteria.

Frequency response curves were shown for the various biquad filters. The first two test chips had experimental curves while the last two relied on simulation only. The frequency response showed a notch at the zero frequency with the notch frequency tunable with the bias current over a range of 2 octaves for the first two test chips and over a range of 4 octaves for the last two test chips. It was seen that the quality of the zero corresponded well to the phase of the integrators at the unity gain bandwidth frequency.

CHAPTER 5 TUNING CONSIDERATIONS

5.1 INTRODUCTION

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In this chapter, several methods of tuning are examined. The first is called continuous tune, where the performance of the filter, or of a similar master filter is continuously compared to the ideal performance and corrections are made. This allows the filter to track variations in processing as well as variations in time such as drift and temperature change. The second method is called pretuning. In this case, the filter is tuned once to compensate for processing variations. Other variations must be minimized through circuit techniques. It is also possible to use some combination of continuous tune and pretune to benefit from the advantages that each of them can offer.

5.2 CONTINUOUS TUNING

In the past, most of the tuning considerations were directed at continuous tuning. One popular method was to use a phase-locked loop circuit as shown in Figure 5.1. The VCO is built with the same integrators as used for the filter, with a desired oscillating frequency equal to the filter pole frequency. A phase detector compares the VCO frequency to an externally supplied reference frequency and adjusts the tuning voltage to keep the two frequencies locked. This implies that the filter must be well matched to the VCO. However, large signals are present in a simple VCO, while small signals occur in the filter. For this reason, with the same bias current, the transconductance of the input transistors of the VCO is lower on the average than that for the filter. The result is that the tuning voltage which produces the correct VCO frequency will produce a filter pole frequency that is too high. Thus, in addition to the need to match components, additional circuitry may be required to match or restrain the signal amplitude. An alternative that has been employed is to use a voltage-controlled filter instead of the voltage-controlled oscillator. The second order filter is designed such that at the pole frequency, the phase at the output is at 90 degrees with respect to the input. A phase detector compares the phase of the output signal to the reference input. If the filter pole frequency is not equal to the input reference frequency then the phase difference will not be 90 degrees, and corrections will be made to the tuning voltage. This tuning voltage also tunes the actual filter so it can be considered as the slave filter,

a) PLL using VCO

b) PLL using VCF

Figure 5.1 Tuning Circuit using a Phase Locked Loop. The circuit uses a voltage controlled oscillator or a voltage controlled filter.

while the reference filter can be called the master filter. The main requirement is that the master and slave filters be carefully matched.

One design used components which were switched between a tuning circuit and the actual filter. This meant that the components which were being individually tuned were also used in the real circuit [5]. This was reported to lead to better matching between the master and slave filters.

5.2.1 CONTINUOUS TUNE REQUIREMENTS

A feedback circuit ensures that the bias levels are correct for the master filter. The same bias levels are applied to the slave filter. To ensure that the slave filter has the correct frequency response, the master and slave circuits must be carefully matched. In addition, considerable circuitry is required, such as the master filter, the phase detector, and probably a low-pass loop filter with a long time constant. As well, there is the need for an externally supplied reference signal.

5.2.2 BENEFITS OF CONTINUOUS TUNING

In a carefully designed circuit, continuous tuning is capable of eliminating circuit variations due to processing variations. Variations due to temperature changes, drift or aging can also be eliminated.

5.3 PRETUNING

With pretuning, the filter is tuned once and then is operated in an open loop fashion. Some of the available methods for pretuning are the use of trim resistors, fusible links or EPROMs. The resistors can, for example, be laser trimmed to adjust the bias current. Fuses can be blown to alter circuits that adjust the tuning voltage. EPROMs can be used to design a programmable current source. EPROM pretuning has been studied in some detail and will be discussed in a later section.

5.3.1 PRETUNE REQUIREMENTS

Pretuning must be capable of correcting for process variations. Obviously it will not be capable of tuning parameters that change with time so design techniques must be used which minimize these effects.

5.3.2 BENEFITS OF PRETUNING

While there are obvious disadvantages of pretuning, such as open loop operation with no method of following temperature change, there are also some benefits. Pretuning can account for processing variations without the requirement to match a slave and a master filter. The circuit complexity can be greatly reduced since the feedback elements need not be present. To compensate for the inability to track temperature variations, circuits must be designed so that they have a low temperature sensitivity.

5.3.3 EPROM PRETUNING

EPROM pretuning was studied in some detail to evaluate its potential for use with the transconductance biquad filter. A combination of two different approaches was used. Digital EPROM pretuning could be used to select current sources with binary weighting while analog EPROM pretuning allows any value of current to be used. Thus the digital EPROM could be programmed to take care of the most significant bits of the current while the analog EPROM takes care of the remainder. Digital EPROMs are not sensitive to temperature since they act as switches only, but the current sources they select must be designed to be temperature insensitive. Temperature affects in the analog EPROM are minimized by reducing the range of currents it handles.

5.3.3.1 ANALOG EPROM PRETUNING

Figure 5.2 shows an analog EPROM circuit. The threshold of the EPROM transistor can be tuned in an analog sense to obtain the desired current, which is then mirrored into the bias circuit. This programming is preferably done with UV light. This method of programming is preferable since, unlike high voltage programming, the circuit can remain connected during the programming sequence. The tuning procedure is further discussed in section 5.3.3.3.

5.3.3.2 DIGITAL EPROM PRETUNING

Figure 5.3 shows the setup of a digital EPROM pretuning circuit. Each EPROM transistor forms half of a differential pair with a regular transistor as the other half. The current sources of consecutive differential pairs have binary weighting. The gates of the regular transistor are connected to a reference voltage, typically zero volts during operation. The gates of the EPROM transistors are connected to program points which are kept at V_{DD} during operation. If the EPROM threshold is low, all of the current flows through the EPROM from V_{DD} and if the threshold is high, the current flows through the regular transistor and forms part of the bias current. Thus, by selectively programming the EPROM thresholds, it is possible to select any combination of the weighted current sources to form the bias current. It is important to keep the operating voltages the same for each of the differential pairs and current sources to avoid inexact multiples of the input current due to variations in body effects and output resistance. The current sources and differential transistors can be designed as binary multiples of a unit cell.

5.3.3.3 EPROM TUNING SEQUENCE

This section will describe the required steps in tuning EPROM current sources to obtain the correct filter response.

The initial step is to determine the required combination of binary current sources. This is done by sequentially selecting all the possible current levels, while observing the required filter parameter such as the notch frequency. To select a particular current source, the EPROM is turned off by setting the program pin low while the reference level is at zero volts. Similarly, to deselect a current source, the program level is brought high while the reference level is at 0V (or at V_{SS} if required).

After determining which current sources should be selected, the next step is to actually program the EPROMs in the required directions. For current sources that should be selected, the program pin is brought high while the reference pin is brought to V_{SS} . This causes all the current to flow through the EPROM, (the opposite of what is required in actual operation later). For current sources which are not to be selected, the program pins are left low so no current flows through the EPROM. Then the EPROMs are exposed to UV light. Thresholds program high if there is current flowing through the device while the thresholds decrease if there is no current. The decrease in threshold value corresponds to the conventional erase. Note that for the thresholds programmed high, the reference level is at V_{SS} which ensures that after programming when the reference level is returned to 0 volts, the EPROM

will definitely be off. If an analog EPROM is present, it should not have current flowing through it during the digital EPROM tuning process. This is to prevent its threshold from increasing. The analog EPROM is tuned after the digital EPROM tune without any change to the voltage levels on the program pins. This prevents the thresholds of the digital EPROMs from shifting while the analog EPROM is being programmed. Note that this implies that filter parameter measurements are not possible during analog tuning if there are digital EPROMs present. In this case, some method of tuning with pulses of UV light and doing a measurement in between would have to be used.

The final step after programming is completed is to connect the EPROM circuitry for actual operation. This requires that the program pins are all connected to V_{DD} and the reference pins are connected to zero volts.

5.4 COMBINATION OF PRETUNING AND CONTINUOUS TUNING

It is possible with some combination of continuous tuning and pretuning to obtain some of the benefits of both methods. The pretuning could be designed to account for process variations while a continuous tuning circuit would account for the later variations with time. It is possible that by removing the largest variations due to the processing, the design of the continuous tuning network could be simplified.

5.5 SIMULATIONS AND MEASUREMENT

All of the experimental work on EPROM pretuning was done on EPROM cells as previously integrated in the CMOS3 process. These were wired together to form the circuits as discussed before and measurements were made on programming characteristics, charge retention, temperature effects etc. A circuit is presently in fabrication which combines the biquad filters and analog and digital EPROM pretuning circuits on the same chip.

Simulations are difficult to perform since most simulators do not allow perfectly floating capacitors such as are required for EPROMs which should retain their charge for years. In simulations, the capacitors had time constants of the order of seconds. Without modification, some simulations of fast events such as threshold measurements and selection of currents in digital EPROMs were possible. Since no model for the EPROM was available, a regular transistor and capacitor were combined and the initial voltage on the capacitor adjusted until the apparent threshold of the overall transistor matched that of the EPROM obtained experimentally. A standard method for measuring threshold is to apply a voltage ramp at the gate and to measure the drain current. With a low drain voltage, typically 0.1V, a plot of current versus gate voltage is roughly linear, and indicates the threshold voltage. Measurements of erased EPROMS showed a voltage intercept of about 1.8V. Figure 5.4 shows a ~~simulation~~ of drain current versus applied gate voltage with an initial voltages on the capacitor of -1V.

Figure 5.4 EPROM Threshold Simulation

These simulation models of the EPROMs for both low and high threshold (or any intermediate threshold) can be used for more complete simulations. Figure 5.5 shows one example of a simulation where each possible current level in a digital EPROM circuit is consecutively selected. This shows that all levels are exact multiples of the basic bias current of 8.4uA.

Figure 5.6 shows the programming behaviour of an analog EPROM under UV light. Initially with a low threshold, the current is set to 45uA by selection of the resistor value. With current flowing and the UV light on, the threshold increases and after 2 minutes the current has decreased to 24uA. At this time the UV light is turned off and the current remains constant until the UV light is turned back on again. In measurements over longer periods of time, no observable change of current was found for a period of two weeks. Long term tests of the charge retention have not been carried out yet.

Instead of observing the current as the tuning process takes place, it is possible to use the filter performance as a tuning criterion. For example, a spectrum analyser could be used to observe the notch frequency as UV light is applied. Pulsed UV light could be used to slow down the rate of change as the correct frequency is approached.

Figure 5.5 Simulation of Digital EPROM Selection. Initially all current sources are selected for a total current of seven times the basic current.

Figure 5.7 shows the temperature effects on the current through an analog EPROM. The temperatures was varied from 25 degrees C to 125 degrees C and the change of current was observed. The nominal current was set at a number of different levels by changes to the resistor and by partial programming. Two parameters are known to be directly affected by temperature. The threshold decreases in direct proportion to the temperature increase, and hence the current increases. The mobility varies as $T^{-3/2}$ which results in a decrease of current as the temperature increases. The threshold effect is expected to be dominant when operating just above the threshold as occurs for low currents. The changing of threshold will have very little effect on current at high current levels where the mobility effect is expected to dominate. This was observed experimentally with a positive temperature coefficient at 6uA and a negative temperature coefficient at 60uA. In between it is possible, in principle, to have the two effects compensate each other. This was observed in the 15uA region. An analog EPROM designed to operate with a nominal current in this region should have a low temperature sensitivity even though exact temperature compensation can not be expected.

Figure 5.6 Programming of Analog EPROM with UV light

Figure 5.7 Temperature Effects of Analog EPROM

5.6 DISCUSSION AND SUMMARY

In this chapter, the role which EPROM pretuning might have in providing the bias current for the biquad filter, has been discussed. While continuous tuning has clear advantages in being able to compensate for any disturbance, it requires complex circuitry. EPROM pretuning, including digital EPROMs for selections of temperature insensitive current sources and analog EPROMs optimized for minimum temperature coefficient, could be used to correct for the effects of processing variations. This may be adequate in non-critical applications. In other applications it may lead to a simpler design of a continuous feedback circuit. A more complete study of long term stability is still needed to determine the suitability of the analog EPROM.

CHAPTER 6 CONCLUSIONS AND RECOMMENDATIONS

6.1 SUMMARY AND CONCLUSIONS

The objective of this thesis was to study the implementation of transconductance filters making use of wideband CMOS opamps. In Chapter 1, three areas for research were identified that had not received a lot of attention in the past. First was the adaptation of high frequency CMOS opamps to realize the integrator as compared to the past use of simpler devices such as differential pairs. The second research topic was the use of biquad filter topologies which made use of closely spaced poles and zeros in order to obtain a fast transition from pass-band to stopband. The final area of research was a study of filter pretuning in particular with analog and digital EPROMs.

In Chapter 2 the folded cascode opamp was studied. A simple model was used to describe the input differential pair in terms of cutoff voltage, common-mode range and linearity. It was shown that cutoff voltage and linearity could be improved by using small input devices; however this would tend to limit the common-mode range. The use of small input devices is possible in this application while it is not possible in general purpose opamp design. The transconductance of these amplifiers can be tuned by varying the bias current to the input pair. Since the tuning range is large, circuits were needed to keep the output at zero volts. In the single-ended opamp the offset circuit keeps the negative output close to ground. In the double-ended opamp, a common-mode correction circuit keeps the sum of the two outputs, ie.

the common-mode voltage, close to ground. An outstanding problem in previous work with the common-mode circuit has been its linearity and range of operation. A switched-capacitor summing circuit was proposed as a solution to these problems in this thesis. The implementation of such a circuit was studied to show that the problems of clock noise, stability and power supply rejection could be dealt with. It was found necessary to have the load capacitance connected to ground instead of differentially. In general, common-mode loop stability has been studied deeply in this thesis; there is little literature on this problem.

The design of the bias circuit was also shown to be important. The basic bias circuit had the input stage and the cascode stage tuned separately. This resulted in the current in the cascode stage being reduced to zero for large bias currents. The improved bias circuit tuned both stages in unison and so required only one current input and could operate over a much larger input current range. For both of these circuits, the offset adjust circuit was not related to tuning current so fairly large offsets were expected at the output. As part of the double-ended opamp, the common-mode feedback circuit was designed to be referenced to the bias current so low offset was expected over the complete tuning range. It was suggested that this circuit could be adapted to improve the single-ended circuits.

In Chapter 3 the design of the biquad filter was considered. It was shown how the open loop transconductance biquad filter could be derived from the discrete biquad filter. Simplifications could be made by combining resistors or by using more than one input stages feeding

into a single cascode stage. In this way the different topologies used from two to four input stages, two cascode stages and three capacitors to realize the biquad filter. A zero was included in the transfer function by capacitively coupling the input to the output. It was shown that the ratio of the zero frequency to the pole frequency was determined by a capacitor ratio. Thus, the pole and zero could be very closely spaced to provide fast transitions. This frequency ratio would remain the same over the tuning range or process variations.

It was shown that with careful design, the effects of the DC gain and the parasitic poles can counterbalance and a high quality zero can be obtained. The double-ended biquad filter was shown to use twice the total capacitance of the single-ended design if the capacitance is connected to ground.

Four test chips were designed and simulations of their performance were discussed in Chapter 4. Some measurements have been made on the first two designs. Measurements and simulations verified the theory of Chapters 2 and 3. The improved bias circuit allowed the last two designs to be tuned over 4 octaves in frequency while the first two could be tuned over 2 octaves. Over this range of tuning current, the range of output offset voltage was 850mV for the basic bias circuit and 650mV for the improved bias circuit. For the double-ended amplifiers with the further improvement in the bias circuit this voltage was decreased to about 100mV. Some further improvements seemed possible.

The filters were designed to have a pole frequency of 455kHz for

the first two test chips and 1.6 MHz for the last two test chips. The ratio of zero frequency to the pole frequency was designed to be 1.05. Measurements on the first two test chips verified that the simulations were correct. The depth of the notch was related to the phase of the integrators at the notch frequency, with a phase of 90 degrees producing the deepest notch. The circuits using the improved bias circuit showed a nearly constant phase and notch depth over the tuning range.

Simulations of the double-ended circuit showed that clock noise in steady state would be about 8mV peak to peak.

In Chapter 5, tuning options were discussed with emphasis on ~~A~~ EPROM pretuning. With pretuning, tuning is done once and then the system operates open loop. Thus it can account for process variations but must rely on circuit design techniques to minimize change due to temperature, drift and aging. The advantage of such a system is that it is simple compared to the continuous feedback option. In Chapter 5, a design was shown for the digital EPROM which selected weighted current sources, to make up the bias current. An analog EPROM could then be programmed to provide any level of current, typically between the bits of the digital EPROM. Programming of the EPROMs could be performed in circuit with the use of UV light which was verified experimentally. The temperature dependance of the current in a diode connected EPROM was measured in the range from 25 to 125 degrees C. For an increase in temperature, both the threshold and the mobility decreased. At low currents, the threshold change was dominant and the current increased

with increased temperature. At higher currents, the mobility change was dominant and the current decreased as temperature increased. It was shown that at an intermediate current, these effects balanced and that an EPROM designed for a nominal current in this region was temperature insensitive. It was concluded that pretune could be successful in compensating for the effects of process variations and could be designed to have a low temperature sensitivity. In more critical applications, a combination of continuous tune and pretune could simplify the design of the feedback circuitry.

6.2 RECOMMENDATIONS FOR FURTHER WORK

Measurements on the first two test chips agreed fairly well with simulations. The last two test chips are still in fabrication and should be studied when available. This is especially important for the double-ended amplifier which had a few features that are difficult to simulate. The switched-capacitor common-mode feedback circuit was difficult to simulate since it relies on accurate models of transistors when dealing with fast transients. Any frequency domain simulations are difficult to make due to the switches. Sinusoidal inputs can be applied and the outputs simulated in the time domain but this requires a lot of computing time. The other alternative which was used in this work was to replace the switched-capacitor with its resistor equivalent and simulate the resultant continuous circuit. This will not give the correct result in the region of the clock frequency and will hide problems such as aliasing and clock feedthrough, but is appropriate for studying general behavior. Other areas where simulations may be inadequate are

in differential power supply rejection and noise.

Work should continue on the topic of extending the wideband CMOS opamps and integrators to higher frequencies. This may be possible to some extent with increased device size to allow higher currents. This will also increase the parasitics so a tradeoff is involved if this approach is to be pursued. It was suggested that lower DC gain would help to offset the high frequency parasitics. Another area that could be studied is the deliberate introduction of phase delays in certain paths to balance the delays due to the parasitic poles.

In the EPROM pretune circuit, temperature dependence has been studied, but the combined behavior of the tuning circuit and the filter has not been studied. Constant notch frequency rather than constant bias current with a change in temperature should be the objective. Another topic that should be studied is the long term stability of the EPROM threshold.

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