A 24GHz Fully Differential Transmit PLL
in a 0.13 μ m Process

by
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Abstract

In this thesis the design of a 24GHz fully differential transmit phase locked loop (PLL) is reported. The circuits are implemented in a 0.13 μ m process.

This transmit PLL consists of a voltage-controlled oscillator (VCO), a phase frequency detector (PFD), a charge pump (CP) and a down-conversion mixer, as well as an on-chip loop filter. All the blocks are fully differential.

The differentially tuned VCO is constructed using a complementary negative g_m structure. The varactors in the VCO are implemented using accumulation MOS (AMOS) varactors to obtain higher Q and relatively large tuning range. The measured free running output frequency is 21.5GHz and the VCO gain is 588MHz/V.

The down-conversion mixer is implemented using a conventional Gilbert Cell topology. The most challenging part of this design was the high frequency single-ended to differential converter, which is utilized to convert the single-ended off chip LO signal into a balanced differential signal. After much research, a two stage differential pair used as a converter was found to be the best choice.

The PFD is constructed using current mode logic (CML) cells and the CP is driven by rail-to-rail signals. The frequency response was the major concern in the PFD and CP design. A CP with cascaded current sources is found to provide improved speed and current matching.

The measurement results showed the VCO and mixer work properly but the PFD and CP part fails due to a short circuit existing in the circuit which was caused by careless layout. This failure could be fixed by a laser cut.

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Abbreviations

PLL	Phase Locked Loop
BJT	Bipolar Junction Transistors
CML	Current Mode Logic
MIM	Metal Insulator Metal
PCB	Printed Circuit Board
RFIC	Radio Frequency Integrated Circuits
VCO	Voltage Controlled Oscillator
PFD	Phase Frequency Detector
CP	Charge Pump
AMOS	Accumulation Metal Oxide Semiconductor
FET	Field Effect Transistor
LO	Local Oscillation
BPF	Bandpass filter
LPF	Lowpass filter
HPF	Highpass filter
LVS	Layout versus schematic
DRC	Design rule check

Chapter 1 Introduction

1.1 Motivation for this Work

With each passing year more applications for wireless technology are appearing. Cell phones, WLAN, GPS, RFID tags, and medical sensors are just some examples of wireless technology, which are becoming commonplace in everyday life. With the introduction of all these new devices, the spectrum is becoming increasingly crowded. Thus cost effective wireless devices that work at higher frequencies are needed. Above the 5GHz band, there is another unlicensed band at 24GHz. Recently, more and more research has been done to investigate whether modern CMOS technology can be used to implement radios in this frequency band. Fortunately, CMOS technology has now progressed to the state where implementing such radios has become feasible.

In a wireless transceiver, the transmitter design often focuses on how to obtain high power efficiency within the linearity tolerance. Often, the transmitter has less possible architecture forms than the receiver has. A common architecture for the transmitter design is the transmit phase locked loop (PLL), which is also called an offset PLL. Compared with other architectures such as a direct conversion or a two-step conversion, the transmit PLL does not require an expensive bandpass filter (BPF) which is hard to implement on-chip. The transmit PLL architecture has already been widely used in GSM transmitter designs.

1.2 Contribution

This work contributes to the design of a very high frequency transmit PLL for future application. Specifically, in this work, a 24GHz VCO is integrated in a PLL and a fully differential architecture is implemented. In recent literatures, high frequency LC VCOs are widely investigated. However, these VCOs are not implemented in closed loops but free running. On the other hand, synthesizers in fully differential structure become more and

more attractive with the development of CMOS technology but the VCO frequency is not as high as 24GHz. In this thesis, the high frequency VCO is implemented in a fully differential closed loop which becomes challenging and attractive. In addition, the 400MHz phase/frequency detector (PFD) comparison frequency is among the highest one in recent papers.

In this work, specifications for each block in this PLL are defined and this PLL circuit was designed and fabricated. Based on measurement results, the high frequency VCO and mixer work properly. The VCO and mixer results are close to the specifications. Through this work, it is shown a high frequency PLL in fully differential structure is possible to be designed and implemented in this 0.13 μ m process.

1.3 Thesis Overview

This thesis is organized as follows. First the background of the transmit PLL is introduced in Chapter 2. A system level design procedure and simulation results are introduced in Chapter 3. This system level design is implemented in VerilogA code and a behavioral level simulation is performed to show the transmit concept can work properly. In the following Chapters, all blocks required are introduced. The PFD, CP, VCO and mixer circuit design are discussed in Chapter 4 to Chapter 7 respectively. Finally, the chip layout, post layout simulation results and measurement results are presented in Chapter 8. Chapter 9 is the conclusion of this thesis.

Chapter 2 Background

2.1 Signal Modulation Scheme

In wireless communications, the transmitted waveform is usually a high-frequency carrier modulated by the original signal due to the limited antenna size [1]. The original signal, such as video, sound, or a DSP signal, is defined as the baseband signal. Signal modulation is the process of converting the baseband signal to a passband signal, which can be transmitted.

Modulation can be either analog or digital. Modulation can transmit information by varying either the amplitude or the phase and frequency of the carrier. Recently, digital modulation has become more popular. Some common types of digital modulation are amplitude shift keying (ASK), phase shift keying (PSK), and frequency shift keying (FSK). In modern wireless communications, PSK and FSK have much wider usage because they are less sensitive to amplitude noise [1].

In general, a modulated signal can be defined as:

$$x(t) = A(t) \cos[\omega_c t + \phi(t)] \quad (1)$$

where $A(t)$ and $\phi(t)$ are general functions of time. If $\phi(t)$ is kept constant and never varies with time, and $A(t)$ is a function of time, the modulated signal $x(t)$ is called a variable envelope signal. However, if $A(t)$ is kept constant but $\phi(t)$ is a function of time, the modulated signal $x(t)$ is a constant envelope signal. In this case, the information is stored only in the phase or the frequency of the waveform. A typical constant envelope modulation is Gaussian minimum shift keying (GMSK) that is widely applied in many standards such as GSM, DECT, and HIPERLAN cellular systems [2][3].

If a constant envelope modulation is used, the transmitter system has a much lower linearity requirement on a power amplifier (PA), and a non-linear PA can be selected to get high power efficiency. The signal modulation scheme is critical to the transmitter selection. The design of the transmitter depends on which modulation scheme is selected. [2][3][4][5].

2.2 Transmitter Architecture

In a modern wireless transceiver, the RF transmitter modulates the base band signal, up-converts and amplifies the RF signal for transmission. Compared with the receiver, in the transceiver there are fewer architectural choices. In general, the transmitter architecture can be identified as a direct-conversion transmitter, two-step transmitter or a transmit Phase Locked Loop (PLL) [1][2].

In an RF transmitter, when the local oscillation (LO) frequency equals the transmitted carrier frequency, this transmitter is called a direct-conversion transmitter. This type of transmitter suffers from a critical drawback: the LO signal will be directly disturbed by the output from the power amplifier due to the fact that the PA output spectrum is close to the LO frequency. When the output signal from the PA is strong, the corruption is more severe. This phenomenon is widely known as “injection pulling” [1].

In order to remove the “injection pulling”, a two-step transmitter architecture can be implemented. The basic idea is to up-convert the baseband signal in two steps (or even more steps) so that the PA output spectrum is far away from the LO signal frequency. However, in this architecture, a band-pass filter (BPF) must be placed before the PA stage to remove all unwanted harmonics. The required rejection factor normally is very large (up to 50 to 60dB) [1]. Since the center frequency of this BPF is very high, this BPF is also called an RF filter. Normally this RF filter is hard to integrate on chip and it is expensive.

To eliminate the RF filter, a special transmitter architecture can be selected. This kind of transmitter has a PLL structure so it is called a transmit PLL or offset PLL architecture. The block diagram of this transmit PLL architecture is shown in Figure 1.

Figure 1. Transmitter PLL architecture block diagram.

The main difference between the transmit PLL and a normal synthesizer is the transmit PLL has a down-conversion mixer placed in the return path instead of a frequency divider in a synthesizer. This down conversion mixer has a fixed frequency input signal called RF LO as shown in Figure 1. The output signal from the transmit VCO (Tx VCO) is sent into this mixer. The desired output frequency tones from the mixer are at frequency of $f_{VCO} \pm f_{LO}$, where f_{VCO} is the frequency of the Tx VCO output signal and f_{LO} is the RF LO frequency. If a lowpass filter is implemented after the mixer to remove the high frequency component, the output from the mixer contains only the $f_{VCO} - f_{LO}$ component. This signal is sent into one port of the phase/frequency detector (PFD).

The input signals in Figure 1 are baseband I and Q signals. They are translated to a fixed intermediate frequency (IF) signal first. This IF signal is sent into the other port of the PFD. The PFD performs the task of comparing the IF signal and the mixer output signal. If the phases or frequencies of these two signals are not in alignment, the PFD will gener-

ate either an UP or DOWN signal to send to the charge pump (CP). The CP will then push charge onto the loop filter or pull charge back off the loop filter respectively. As a result, the voltage on the loop filter will change and cause the Tx VCO to either increase or decrease its output frequency. Since the RF LO signal frequency is fixed, the output signal frequency from the down-convert mixer will also become higher or lower. Through this mechanism, the phases and frequencies of the IF signal and the output from mixer will eventually be in alignment. After this occurs the transmit PLL is said to be in lock.

Even in the locked state, the PFD will not stop comparing the phase/frequency difference between the IF and the feedback signals. Whenever the IF signal frequency changes, the PFD and CP will sense the change and control the Tx-VCO such that the Tx-VCO output signal is frequency modulated with the original IF signal. Through these steps, if the bandwidth of the PLL is selected properly and the IF signal frequency does not change too rapidly, the frequency modulation of the IF signal will be faithfully reproduced at the Tx VCO output [2][3][4].

Compared with the divider in the synthesizer, a down-conversion mixer in the return path as shown in Figure 1 can reduce transmit PLL settling time dramatically. If it is assumed a transmit PLL has a divider with division ratio N in the return path, the frequency of the IF signal is f_{IF} and the output frequency from the VCO is still f_{VCO} , then the f_{VCO} and f_{IF} have to satisfy the condition as shown in equation (2) to get the transmit PLL locked.

$$f_{VCO} = N * f_{IF} \quad (2)$$

If f_{IF} changes by Δf , f_{VCO} has to change by $N * \Delta f$. Once this happens the transmit PLL will be in lock again.

However, if a down-conversion mixer with a fixed f_{LO} is implemented in the return path, as long as the condition shown in equation (3) is satisfied, the transmit PLL is in lock.

$$f_{VCO} - f_{LO} = f_{IF} \quad (3)$$

As a result, if f_{IF} changes by Δf , f_{VCO} only needs to change by the same amount Δf and the transmit PLL will be in lock again. Therefore, in theory the transmit PLL has a shorter transient time to achieve lock [2]. The most attractive characteristic of this transmit PLL architecture is that all unwanted high-order harmonics will be absorbed by the loop filter. These high-order harmonics are generated during the frequency translation process and there is no way to avoid generating them. In this architecture, an expensive RF BPF mentioned in the two-step architecture before is not required.

2.3 Phase Locked Loop

The transmit PLL has almost all the blocks a conventional synthesizer would have except that it has a down conversion mixer instead of a divider. This down conversion mixer performs the task of down converting the high frequency output spectrum to the IF frequency but has nothing to do on the phase. As a result, this mixer cannot be simply regarded as an integer divider with division ratio N . Nevertheless, to make analysis simple, the transmit PLL is still assumed to be a normal PLL at beginning.

There is much literature on the analysis of a PLL system. In general, a PLL system is a non-linear system so it is difficult to express its behavior mathematically. However, if all blocks are replaced by their linear models, the PLL will become a linear system. The linear model of a PLL system is shown in Figure 2.

Figure 2. Linear model of a PLL.

In Figure 2, the PFD and CP work as a subtractor with gain represented as K_{PHASE} , the loop filter has transfer function $H(s)$, and the VCO has gain K_{VCO} . The overall transfer function is shown in equation (4).

$$\frac{\phi_{\text{OUT}}}{\phi_{\text{in}}} = \frac{\frac{K_{\text{PHASE}} K_{\text{VCO}} H(s)}{s}}{1 + \frac{K_{\text{PHASE}} K_{\text{VCO}} H(s)}{Ns}} \quad (4)$$

In a charge pump based PLL, the K_{PHASE} can be expressed as shown in equation (5) [6].

$$K_{\text{PHASE}} = \frac{I_{\text{CP}}}{2\pi} \quad (5)$$

where I_{CP} is the charge pump output current.

The transient response of a PLL is a nonlinear phenomenon but in general the loop dynamics depend on the loop filter parameters. Figure 3 shows a widely used loop filter, which is a second-order passive lowpass filter.

Figure 3. A typical second-order loop filter.

In Figure 3, C_2 is used to eliminate the high frequency noise and it is normally much smaller than C_1 , roughly one to tenth of C_1 . Therefore, to calculate the loop filter transfer function, C_2 may be ignored. The input is the current i_{cp} from the charge pump and the output is the voltage, V_{CNTL} , developed on the loop filter. Therefore, the transfer function of this loop filter can be expressed in equation (6).

$$H(s) = R + \frac{1}{sC_1} \quad (6)$$

Using equations (5) and (6) to replace the K_{PHASE} and $H(s)$ in equation (4), the closed loop transfer function becomes:

$$\frac{\phi_{OUT}}{\phi_{in}} = \frac{\frac{K_{PHASE} K_{VCO} H(s)}{Ns}}{1 + \frac{K_{PHASE} K_{VCO} H(s)}{Ns}} = \frac{\frac{I_{CP} K_{VCO}}{2\pi * NC_1} (RC_1 s + 1)}{s^2 + \frac{I_{CP} K_{VCO}}{2\pi * N} R_1 s + \frac{I_{CP} K_{VCO}}{2\pi * NC_1}} \quad (7)$$

This transfer function is a second-order function and has a lowpass characteristic. Inspection of the lowpass characteristic reveals that the loop can track the input phase modulation within the loop bandwidth and fails to track the phase modulation that is out of the

loop bandwidth [7]. Normally the loop bandwidth is defined by the 3dB bandwidth of the loop. It is shown in equation (8) [6].

$$\omega_{3dB} = \omega_n \sqrt{1 + 2\zeta^2 + \sqrt{4\zeta^4 + 4\zeta^2 + 2}} \quad (8)$$

where ζ is the damping factor of this transfer function. The natural frequency of this transfer function can be found as

$$\omega_n = \sqrt{\frac{I_{CP} K_{VCO}}{2\pi * NC_1}} \quad (9)$$

The damping factor can be found as

$$\zeta = \frac{R}{2} \sqrt{\frac{I_{CP} K_{VCO} C_1}{2\pi * N}} \quad (10)$$

In a feedback system, the stability of the loop must be taken into consideration during the design process. To maintain a stable loop, the phase margin must be set properly. Normally the phase margin should be kept larger than 60° to maintain a stable loop and a relatively flat gain peaking [8][7].

2.4 Phase Noise

Phase noise is an important criterion to measure PLL performance in a wireless communications system. In a PLL system, all blocks will contribute noise to affect the whole PLL phase noise performance. In general, the noise from different blocks can be divided into two types. One is the VCO phase noise. The other is the noise from the rest of the blocks [6][7][8].

The transfer function of the output noise due to the VCO noise can be shown as:

$$\frac{\varphi_{noise,out}}{\varphi_{noise,VCO}} = \frac{s}{s + \frac{K_{PHASE} K_{VCO} H(s)}{N}} = \frac{s^2}{s^2 + \frac{I_{CP} K_{VCO}}{2\pi * N} Rs + \frac{I_{CP} K_{VCO}}{2\pi * NC_1}} \quad (11)$$

This transfer function has a highpass characteristic. The VCO raw noise will be suppressed by the loop below the loop bandwidth. However, the VCO noise is the major noise source of out-of-band noise for the whole PLL loop [6].

Besides the VCO noise, the other noise sources all have an impact on the PLL phase noise. These noise sources include the phase/frequency detector, charge pump, loop filter and divider (or down-conversion mixer). The output noise due to these noise sources can be input referred and have a transfer function given as equation (12) [6].

$$\frac{\varphi_{noise,out}}{\varphi_{noise,other}} = \frac{K_{PHASE} K_{VCO} H(s)}{s + \frac{K_{PHASE} K_{VCO} H(s)}{N}} = \frac{\frac{I_{CP} K_{VCO}}{2\pi * C_1} (1 + RC_1 s)}{s^2 + \frac{I_{CP} K_{VCO}}{2\pi * N} Rs + \frac{I_{CP} K_{VCO}}{2\pi * NC_1}} \quad (12)$$

Equation (12) is a lowpass transfer function. The input referred noise will be suppressed by the loop beyond the loop bandwidth [6][7][8].

From a noise point of view, if the loop bandwidth is selected properly, the output phase noise may be optimized. Theoretically the optimized bandwidth should be the cross-point of the VCO noise and other noise profiles as shown in Figure 4.

Figure 4. Optimized loop bandwidth from a noise point view.

However, the loop bandwidth also determines the loop dynamics. Therefore, the loop bandwidth selection should be a compromise between noise and other factors such as settling time and locking range. Nevertheless, to reduce the phase noise, a proper loop bandwidth is very critical.

Chapter 3 SYSTEM LEVEL DESIGN

This chapter is intended to describe the system level design process of this transmit PLL. The system level design process includes setting the specifications for each block and determining the loop filter components. A behavioral level simulation has been performed to verify this transmit PLL works properly.

3.1 Design Specifications

This transmit PLL is implemented in a $0.13\mu\text{m}$ CMOS process. This process has eight layers of metal. The nominal supply voltage for a regular transistor is 1.2V but can be increased to 1.5V. The threshold voltages for PFET and NFET are all close to 0.3V. To leave enough headroom for the VCO and the charge pump design, in this design the supply voltage is set to be 1.5V.

Today for the 2.5GHz synthesizer, the comparison frequency is normally chosen to be twenty to forty mega hertz. Since in this work, the VCO has a 24GHz nominal output frequency, the nominal IF frequency is selected to be 400MHz which is also ten times the normal IF frequency in the 2.5GHz synthesizer. The division ratio N between the RF output frequency and the IF frequency is 60. This circuit should be able to accommodate an IF frequency anywhere between DC to two times the nominal frequency which is 800MHz. However, when the IF frequency is higher than 500MHz, the PFD has no capability to handle such high frequency input. Nevertheless, this transmit PLL is not a broadband system, 500MHz bandwidth is large enough to cover the IF range required. Consequently, the IF frequency is chose to be varied from DC to 500MHz.

Within this range, the transmit PLL should have capability to track the IF signal frequency changes. Therefore, the VCO output must cover the range from 23.6GHz to 24.1GHz if the local oscillation (LO) signal to the mixer is set to 23.6GHz. However, if other issues, such as process variations and temperature variations, are taken into consid-

eration, the VCO output range should be at least ten percentages larger than the required range. In this design, the VCO output is expected to be from 23.6GHz to 24.15GHz to grantee the required tuning range can be fully covered unconditionally.

The loop bandwidth setting is essential to this transmit PLL. To set an appropriate bandwidth, loop stability, tracking time, and noise performance should be taken into consideration. To have a stable loop, the loop bandwidth cannot be set too large. Normally the ratio between loop bandwidth and the comparison frequency is less than one to ten to keep the system stable [5][8]. On the other hand, the loop bandwidth cannot be set too tight. Otherwise the loop tracking time may become very long. More essentially, the loop bandwidth must be larger than the bandwidth of the modulated signal to allow all high-order frequency components to pass the loop filter. Besides, the bandwidth selection should also depend on the noise profiles of the components in the loop as mentioned in section 2.4. Therefore, the loop bandwidth is set considering a number of compromises. However, in this design, the loop bandwidth is set to be 1MHz as a conventional number. The noise profiles are not taken into consideration for this bandwidth.

Since the supply voltage for this design is 1.5V, a reasonable estimation of the CP output voltage range is from 0.25V to 1.25V. This voltage range is also the available VCO tuning voltage range. Therefore, the VCO gain K_{VCO} will be approximately:

$$K_{VCO} \approx \frac{24.15 - 23.6}{1.25 - 0.25} = 550 \text{MHz/V} \quad (13)$$

Another important design specification is the charge pump current I_{CP} . Typically this current could be from 500 μ A to 2mA [6]. In this design, the I_{CP} is set to be 500 μ A to save power. After the CP current is selected, the PFD gain K_{phase} is:

$$K_{phase} = \frac{I_{CP}}{2\pi} = \frac{500\mu A}{2\pi} = 0.08mA / rad \quad (14)$$

The design specifications of this transmit PLL are listed in Table 1.

Table 1: Summary of design specifications

Parameter	Value
Supply Voltage (V)	1.5
LO frequency (GHz)	23.6
IF frequency (MHz)	0~500
VCO output range (GHz)	23.6~24.1
VCO gain (MHz/V)	550
Charge pump current (mA)	0.5
PFD/CP gain (mA/Hz)	0.5
Loop bandwidth (MHz)	1
Phase noise (dBc/Hz)	As low as possible

3.2 Loop filter design

In a PLL design, the general loop dynamics are controlled by the loop filter components. In this work, the loop filter is a second order passive lowpass filter.

The closed loop transfer function can be represented by equation (7) in section 2.3. It is a lowpass function. The important parameters in this transfer function are the damping factor ζ and the nature frequency ω_n . To get a flat response curve on the lowpass transfer function, the damping factor ζ is normally set to be 0.707. The gain peaking in decibels for the lowpass close loop transfer function can be found in equation (15) [7]:

$$peaking = 10\log \frac{8\zeta^4}{8\zeta^4 - 4\zeta^2 - 1 + \sqrt{8\zeta^2 + 1}} = 2dB \quad (15)$$

By setting the damping factor as 0.707, the phase margin (PM) can be found as 65.6° , which implies the PLL is stable [7].

Since the loop bandwidth ω_{3dB} is set to be 1MHz in this Transmit PLL, the natural frequency ω_n can be found through equation (8) in section 2.3.

$$\begin{aligned}\omega_{3dB} &= \omega_n \sqrt{1 + 2\zeta^2 + \sqrt{4\zeta^4 + 4\zeta^2 + 2}} = 2\pi \times 1M \\ \omega_n &= \frac{\omega_{3dB}}{2.1052} = \frac{2\pi \times 1M}{2.1052} = 2.9846 \times 10^6 \text{ rad/s}\end{aligned}\tag{16}$$

The relationship between the natural frequency and the loop filter capacitor C_1 can be found in equation (9) in section 2.3. Therefore, the value of C_1 is given in equation (17).

$$C_1 = \frac{I_{CP} K_{VCO}}{2\pi * N \omega_n^2} = \frac{0.5 \times 10^{-3} \times 2\pi \times 555 \times 10^6}{2\pi \times 60 \times (2.9846 \times 10^6)^2} = 447 \text{ pF}\tag{17}$$

Afterwards, the resistor R can be found according to equation (10).

$$\begin{aligned}\zeta &= \frac{R}{2} \sqrt{\frac{I_{CP} K_{VCO} C_1}{2\pi * N}} \\ R &= \frac{2\zeta}{\sqrt{\frac{I_{CP} K_{VCO} C_1}{2\pi * N}}} = 1.03 \text{ K}\Omega\end{aligned}\tag{18}$$

Normally the value of C_2 is chosen to be roughly one tenth of the value of C_1 to reduce higher order harmonics. However, when the value of the resistor R is high, the series impedance of R and the C_1 is comparable to the impedance of C_2 at the natural frequency ω_n , the value of C_2 must be decreased [6]. In this design, the impedance of C_2 is 7.33K Ω at 400MHz if C_2 is only one tenth of the C_1 . Compared with the series resistance of R and

C_1 , this value is not large enough. Therefore, C_2 must be smaller than one tenth of C_1 . In this design, C_2 is selected to be one twentieth of C_1 , which is 22.4pF.

The VCO uses differential tuning and the charge pump also has differential outputs. Therefore, the loop filter could be fully differential as well. The above calculation values for R , C_1 and C_2 are all based on a single-ended loop filter, which is shown in Figure 5 (a). To have an equivalent differential loop filter, C_2 can be split and tied explicitly to ground as shown in Figure 5 (b) [6]. Therefore, from a differential point of view, this differential loop filter still has an equivalent transfer function to the single-ended counterpart.

Figure 5. Second order loop filters (a) Single-ended; (b) Differential.

The values of the components in this differential loop filter are listed in Table 2.

Table 2: Differential loop filter components

Components	Value
$R/2$	500Ω
$R/2$	500Ω
C_1	447pF
$2C_2$	44.8pF
$2C_2$	44.8pF

After all components are determined, the transfer function of this transmit PLL can be plotted as shown in Figure 6. The Matlab scripts are list in Appendix B.

Figure 6. Closed loop transfer function plot.

From Figure 6, the 3dB loop bandwidth is 1MHz as expected. The peaking is 2dB higher than the DC gain.

3.3 Behavioral Level Simulation Results

After the components in the loop filter are determined, the next step is to run a behavioral level simulation to verify a transmit PLL with the parameters obtained in the above sections is feasible.

The completed transmit PLL block diagram is shown in Figure 7. To perform a behavioral level simulation, some behavioral modules must be developed first. These blocks include a differentially tuned VCO, a differential CP, a mixer and a PFD.

Figure 7. Completed differential transmit PLL block diagram.

The scripts widely used for system level simulation are Matlab, VerilogA, and AHDL. VerilogA and AHDL can be integrated into Cadence Spectre and run with Cadence analog environment. In this design, all behavioral modules are constructed with VerilogA script. The scripts for these modules are listed in Appendix A.

The test bench for this transmit PLL is shown in Figure 8.

Figure 8. Test bench for the behavior mode simulation.

In this test bench, the CP output current is $500\mu\text{A}$. The VCO has nominal output frequency of 24GHz and has a gain of $K_{\text{VCO}} = 550\text{MHz/V}$. The LO frequency for the mixer is 23.6GHz . Since the mixer in behavioral mode will generate two tones, which are at frequencies of $f_{\text{VCO}} \pm f_{\text{LO}}$, a lowpass filter is required to remove the high side band tone. This lowpass filter has corner frequency at 700MHz . The output waveform from this lowpass filter will be sent into the PFD and compared with the IF signal.

In this simulation, the frequency step size Δf is randomly selected to be 30MHz . Since the IF nominal frequency is 400MHz , to have a 30MHz step size, the IF frequency can be selected to be either 370MHz or 430MHz . In this simulation, the IF frequency is set to be 430MHz .

When this IF signal and the mixer out signal are sent into the PFD, the PFD will generate either an UP or a DN signal according which signal is ahead in phase.

The control line voltages simulation results are shown in Figure 9.

Figure 9. Behavioral level simulation of the differential control line voltage

In steady state, the differential voltage between the two control lines is 0.54V. Since the K_{VCO} is 550MHz/V, the VCO output frequency f_{VCO} is:

$$\begin{aligned} f_{VCO} &= 24GHz + K_{VCO}V_{tuning} \\ &= 24GHz + 550MHz/V \times 0.54V \approx 24.03GHz \end{aligned} \quad (19)$$

Since the input IF frequency is set to be 430MHz. The LO frequency is 23.6GHz. When this transmit PLL is in lock, the VCO output frequency f_{VCO} is expected to be

$$f_{VCO} = f_{LO} + f_{IF} = 23.6GHz + 0.43GHz = 24.03GHz \quad (20)$$

This number agrees with the result obtained in equation (19).

To Verify the VCO output frequency is 24.03GHz, a discrete Fourier transform (DFT) of the output transient waveform was calculated. The resolution window is set to be 1MHz,

the sampling time is 1uS after the PLL is stable, and the sampling points are 8192. The result is shown in Figure 10.

Figure 10. VCO output spectrum.

Figure 10 shows that the VCO output frequency is exactly 24.03GHz as expected. The DFT calculation result verifies the behavior mode PLL works properly. This PLL also works properly for different frequency step sizes.

3.4 Conclusions

In this chapter, the design specifications are defined for each transistor level block. The components of the loop filter are determined to set the PLL dynamics properly. Afterwards, the behavioral modules for this transmit PLL are developed in VerilogA script. A behavioral level simulation was run to verify that the transmit PLL works properly.

Chapter 4 PFD DESIGN

In this chapter the design procedure for the PFD and a single-ended to differential converter will be presented. A PFD in a PLL system is used to produce voltage signals proportional in width to the input phase difference. The voltage signals generated will drive the CP. In this transmit PLL, one input of the PFD is fed by the output from the down-conversion mixer. Another input is fed by an IF signal which is generated externally from a signal generator. The PFD is implemented in a current mode logic (CML) structure.

4.1 Current Model Logic Cell

In modern logic circuit design, CMOS rail-to-rail logic is the most widely used type of logic for sequential circuit design. However, in high-speed logic circuit design, CML circuits are used much more often. Compared with CMOS rail-to-rail circuits, the CML circuitry is faster because the CMOS rail-to-rail has input and output swings at a rail-to-rail level but CML requires much less voltage swing. At high frequencies, the CML consumes less power than the CMOS rail-to-rail logic does. The CML circuits also have differential input and output signals. Therefore, the CML has better power supply and substrate noise rejection than CMOS rail-to-rail logic [6]. In this thesis, all blocks will be fully differential so CML is a good choice for the PFD design.

A simple CMOS CML block is a differential pair as shown in Figure 11.

Figure 11. A simple differential pair and output current.

When the absolute value of the differential input voltage V_{in} is larger than $\sqrt{\frac{2I_{SS}}{\mu_n C_{ox} \left(\frac{W}{L}\right)}}$,

the bias current I_{SS} will all flow through one transistor, the other transistor will shut off and conduct no current. Therefore, the single-ended output voltage is equal to $V_{DD} - I_{SS}R_D$, which can be defined as logic “0”. The other side output voltage is V_{DD} due to the fact that no current is flowing. This output can be defined as logic “1”.

In a bipolar process, the differential input voltage is normally from 100mV to 200mV to fully switch the differential pair transistors, but in a CMOS process, the differential input voltage has to be at least 200mV [6]. In the 0.13 μ m process used in this work, the differential voltage has to be no less than 300mV to fully switch the CML circuitry for reasonably sized transistors.

It is possible to combine more inputs in one CML stage to generate logic functions, such as AND, OR, and XOR. To have such logic gates implemented in CML, two or more differential pairs will be stacked. A simple NOR gate in CML is shown in Figure 12 [6]:

Figure 12. A NOR gate in CML logic.

In Figure 12, the differential input pairs with inputs labeled as logic “A” and “B” are stacked. If the inputs A and B all have a voltage swing from V_{DD} to $V_{DD} - I_{SS}R_L$, and since the DC bias point of M_1 and M_2 is lower than M_3 and M_4 , therefore M_1 and M_2 cannot be fully switched like M_3 and M_4 are. To properly switch the differential pairs M_1 and M_2 , a DC level shift circuit must be applied to shift the common mode voltage of input A down to a level so that the differential pair M_1 and M_2 can be switched properly. A simple level shift circuit is a source follower as shown in Figure 13.

Figure 13. A source follower works as a level shift.

If M_1 and the current source M_2 are sized properly, then ignoring the body effect of M_2 the voltage gain can be expressed as:

$$A_V = \frac{g_{m1}r_{O2}}{1 + g_{m1}r_{O2}} \approx 1 \quad (21)$$

where r_{O2} is the output impedance of the current source transistor M_2 . Thus, the output can have almost the same voltage swing as the input but the DC level at the output node is lower than the input node by at least one threshold voltage.

4.2 PFD Design Procedure

4.2.1 PFD working theory

In this thesis, the PFD designed is a tri-state PFD as shown in Figure 14 [6].

Figure 14. A tri-state PFD block diagram.

This PFD consists of two resetable D-flip-flops and one AND gate. The inputs of the D-flip-flops are always tied to logic “1”. The IF and mixer output signals are used as clock signals to control the D flip-flops. Examples of the input and output waveforms for this PFD are shown in Figure 15.

Figure 15. The PFD input and output waveforms.

In this PFD, if the rising edge of the IF signal comes first, since the input of the upper D Flip-flop is tied to logic “1”, the output signal “UP” from this D flip-flop will be “1”. This “1” output will be held until the first rising edge of the mixer output signal. When the rising edge of the mixer output signal arrives, the lower D flip-flop will sample the input which is always “1”, the output signal “DN” from this D flip-flop will then go high. Since both “UP” and “DN” become active at this point, the “reset” signal from the AND gate will become “1”, and both D flip-flops will be reset immediately. It depends on whether the IF signal or the mixer output signal comes first as to whether the “UP” or “DN” signal will be active and drive the charge pump. In reality, all logic gates have delays and will not respond fast enough to get the “ideal” waveforms shown in Figure 15. Sometimes a small variance between the IF and the Mixer output signal cannot be detected. This phenomenon is known as “dead zone” [6]. To eliminate the dead zone in the PFD, the AND gate should have enough delay time to detect small phase variances. In this work, the AND gate delay is long enough to remove the dead zone so no extra delay cell is required.

The D flip-flop can be implemented using four NOR gates as shown in Figure 16 [6][7].

Figure 16. A positive edge triggered D flip-flop.

This D flip-flop is a positive edge triggered D flip-flop and it has a hidden “high” input so no extra D input pin is required for this flip-flop [6].

4.2.2 Transistor Level Design

The PFD consists of one AND gate and two D flip-flops. Each D flip-flop is composed of four NOR gates. The AND gate has a similar structure as the NOR gate but different input positions. The AND gate and NOR gate presented in this design are shown in Figure 17.

Figure 17. Logic gates in CML (a) NOR gate, (b) AND gate.

In this process, to fully switch the differential pairs, the input and corresponding output voltage swing have to be no less than 300mV. However, since the operating frequency is around 400-500MHz, and when parasitic capacitance is taken into consideration, the voltage swing should be larger to guarantee each CML stage will be fully switched. In practice the voltage swing was selected to be 500mV. The bias current I_{SS} is selected to be

500 μ A and it is provided by the current source transistor M_6 . This current source transistor M_6 should have a large output impedance to have good common mode rejection performance. For a single current source transistor, the output impedance r_o depends on the transistor's channel length. The relationship between channel length L and the output impedance r_o is given by:

$$r_o = \frac{1}{\lambda I_{DS}} \text{ and } \lambda \propto \frac{1}{L} \quad (22)$$

Therefore, to get high output impedance, the channel length L should be large [7]. On the other hand, the switching transistors, from M_1 to M_5 , use the shortest length allowed by the technology to provide a fastest switching.

Another block that is in the PFD design is the level shift as mentioned in section 4.1. Similarly, the current source transistor is long to provide large output impedance, and the source follower M_1 is designed using a minimum length transistor for best frequency response.

The final values of the components used for the PFD are listed in Table 3.

Table 3: PFD components value

AND gate & NOR gate	Transistor		Width (μm)	Length (μm)	# of fingers
		M ₁	3.25	0.12	4
		M ₂	3.25	0.12	4
		M ₃	3.25	0.12	4
		M ₄	3.25	0.12	4
		M ₅	3.25	0.12	4
		M ₆	5	1.5	15
	Resistor	R _L	Value(Ω)		
			1K		
	Bias voltage	V _{REF}	Value (V)		
			0.4		
Level shift	Transistor		Width (μm)	Length (μm)	# of fingers
		M ₁	5	0.12	3
		M ₂	5	2	2
	Bias voltage	V _{REF}	Value (V)		
			0.65		

4.3 Single-ended to Differential converter

In this work, the IF signal is obtained from a signal generator. The signal generator can only generate a single-ended sinusoid signal. A single-ended to differential converter is required to convert the single-ended signal into a differential one. This converter is normally an off-chip balun. In this thesis, an on-chip converter is designed and placed before the PFD to perform this task.

The single-ended to differential converter block is shown in Figure 18.

If the V_{in} is large enough that half V_{in} can fully switch the differential pairs, both side outputs will swing from $V_{CC} - I_{SS}R_L$ to V_{CC} . Thus, the single-ended signal is converted into a differential one. This converter works properly for a low frequency input such as 400MHz but will be ineffective at higher frequencies such as 23.6GHz.

Table 4: Single-ended to differential converter block components value

Transistor		Width (μm)	Length (μm)	# of fingers
	M_1	1	0.15	8
	M_2	1	0.15	8
	M_3	8	2	20
Resistor		Value(Ω)		
	R_L	500		
	R_{bias}	15K		
Bias voltage		Value (V)		
	V_{ref}	0.45		
	V_{bias}	1.1		
Capacitor	C_C	Value (pF)		
		5		

4.4 PFD Simulation Results

The PFD and the single-ended to differential blocks simulation results are shown in Figure 19.

Figure 19. PFD simulation results.

In Figure 19, the “Mixer differential input” signal is a 350MHz differential signal from the mixer output. The “IF input” is a differential signal generated from the single-ended to differential converter. This signal is a 400MHz frequency signal.

The “ V_{dn} ” and “ V_{up} ” signals are the DN and UP signals generated by the PFD block respectively. The “ V_{dn} ” signal becomes high when the “Mixer differential input” signal arrives till the “IF input” signal is active. This result agrees with the waveform shown in Figure 15.

In this CML circuitry, the time delay between the “Mixer differential input” signal and the “ V_{dn} ” signal is 216.8ps through simulation.

The total current consumption in this simulation is 20.3mA.

Chapter 5 Charge Pump

In a PLL system, the function of the CP is to place charge onto the loop filter or remove charge from the loop filter according to whether the input signal generated from the PFD is an UP or DN pulse [6]. In other words, the CP converts a voltage into a current. The critical criteria to measure the performance of a charge pump are speed, current matching and output noise. The charge pump designed in this work is designed to be driven by rail-to-rail input signals, but the output voltages from the PFD are CML level signals. Thus, a CML to rail-to-rail converter block must be inserted between the PFD and CP to convert the CML level signals to rail-to-rail level signals. In this chapter, the design procedure for the differential CP and the CML to rail-to-rail block will be presented.

5.1 Differential Charge Pump Working Theory

A CP is a pair of current sources which are controlled by two switches. A differential CP has two pairs of current sources controlled by four switches. The switches will be on or off corresponding to the UP or DN signal received from the PFD. A differential CP and a differential loop filter are shown in Figure 20.

Figure 20. (a) A differential charge pump; (b) A differential loop filter.

In the differential CP, the upper current sources, I_{CP1} and I_{CP2} , always send out current through the I_{OUT+} or I_{OUT-} terminal respectively to the loop filter. The lower position current sources, I_{CP3} and I_{CP4} will only sink current from the loop filter. When the UP signal is active, the current sources I_{CP1} and I_{CP4} are tuned on. The current i_{UP} will leave I_{OUT+} and come back to I_{OUT-} through the loop filter. A pair of differential voltages, V_{CNTL_P} and V_{CNTL_N} , will be developed on the loop filter to control the differentially tuned VCO. Alternatively, when the DN signal is high, current will leave I_{OUT-} and come back to I_{OUT+} . Thus, the differential voltage on the loop filter will be changed.

The differential CP has many advantages over the single-ended CP. Firstly, the switch mismatches between NMOS transistors and PMOS transistors become less critical. In a differential CP, both the UP and DN signal will switch a PMOS current source and NMOS current source, but in a single-ended CP normally the UP signal switches the PMOS transistor and the DN signal switches the NMOS transistor. Another important point is the differential CP can generate double the tuning voltage compared to the single-ended CP. In addition, the differential CP is less sensitive to leakage current, and the differential CP has better immunity to the common mode noise such as supply, ground and the substrate noise. However, a differential CP has to pay a penalty of increased power consumption, more output noise and it requires a CMFB circuit [9].

5.2 Charge Pump Design Procedure

5.2.1 Design Consideration

In a CMOS process, the current sources I_{CP1} and I_{CP2} in Figure 20 are normally constructed with PMOS transistors and I_{CP3} and I_{CP4} are constructed with NMOS transistors. In the CP design, an important design issue is the pumping out current and the pumping in current should be matched. Even if a PLL is in a locked state, the PFD will still generate very narrow UP and DN pulses at the reference frequency. These UP and DN pulses will still cause the CP to produce up and down currents. In an ideal case, these two cur-

rent are perfectly matched and will be canceled out by each other. However, if a current mismatch exists, some charge will be transferred to the loop filter and the voltage on the loop filter will be changed and causes the VCO output frequency to change. The feedback in the loop will capture the change and force the voltage to return to the right value. This process will cause spikes in the output spectrum, which are known as “reference spurs”. Larger amounts of mismatch will lead to stronger spurs [6]. Another severe problem due to the current mismatch is the phase offset. The phases of reference and input signal will not be in alignment and have an offset. The amount of the phase offset ϕ_{offset} is shown in the following equation [9]:

$$|\phi_{\text{offset}}| = 2\pi \cdot \frac{\Delta t_{\text{ON}}}{T_{\text{ref}}} \cdot \left(\frac{I_{\text{CP}} + \Delta i}{I_{\text{CP}}} - 1 \right) = 2\pi \cdot \frac{\Delta t_{\text{ON}}}{T_{\text{ref}}} \cdot \frac{\Delta i}{I_{\text{CP}}} \quad (24)$$

where T_{ref} is the reference signal period, Δt_{ON} is the turn-on time of the PFD, and Δi is the current mismatch. Therefore, in the CP design, current matching is the most important issue to be considered.

The second issue in the CP design is speed. The switches in the CP are controlled by either UP or DN pulses from the PFD. Assume the CP receives an UP signal, it has to respond fast enough to generate current I_{CP} before the DN pulse comes. Otherwise, the voltage presented on the loop filter will not track the phase difference. In this thesis, the input frequency to the PFD will be around 400MHz. Therefore, the output signal from the PFD will be around 400MHz as well. Therefore, the CP designed must have the capability to respond to these high frequency inputs.

The third issue is the output voltage range of the CP. The CP is constructed using current source transistors and switch transistors. For the current source transistors, there exist minimum output voltages, which are the saturation voltages of those transistors. For an NMOS transistor, the minimum output voltage is $V_{\text{DS,SAT}}$ and for a PMOS, the maximum

output voltage is $V_{DD}-V_{DS,SAT}$. This CP output voltage range is one factor that determines the VCO tuning range so it is expected to be as large as possible.

The last important factor in the CP design is the output noise. The charge pump is one of the in-band noise contributors so the CP's output noise is expected to be low. In a CMOS process, the major noise sources are $1/f$ noise and channel noise [8]. They are all associated with the output current I_{CP} . The relationship between the input referred noise $\theta(f)$ from a CP and the output current can be found as follows [6]:

$$\theta(f) = 2\pi \sqrt{\left[\frac{2K\mu}{L^2 f I_{CP}} + 4KT \left(\frac{2}{3} \right) \sqrt{\frac{2\mu C_{ox} W}{I_{CP}^3 L}} \right] \left(\frac{t_{CP}}{T_0} \right)} \quad (25)$$

where K is a constant of proportionality which is process dependent, W and L are the width and length of the current source transistors respectively, f is the input frequency, I_{CP} is the output current, t_{CP} is the time when two current sources are on for each period, and T_0 is the period. This input referred noise $\theta(f)$ will be suppressed by the lowpass transfer function. To achieve low output noise, the CP current should be large [6].

In a CP design the leakage current is also very important. It will also cause reference spurs [9]. To reduce the leakage current, the transistors are expected to be strongly shut off. Thus, the switch control voltages are expected to be rail-to-rail signals. Another important issue in a CP design is charge sharing. It may also cause reference spurs. Normally charge sharing effects can be reduced by setting the switch voltages carefully [6]. In this design, the charge sharing effect is not taken into consideration.

5.2.2 Design Procedure

The PMOS and NMOS transistors have output current I_{DS} when they are used as current sources. However, due to the channel modulation, the I_{DS} in saturation can be approximately given by equation (26) [8].

$$I_{DS} = \frac{1}{2} \mu_n C_{OX} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \quad (26)$$

Therefore, the I_{DS} is not only controlled by V_{GS} but also by V_{DS} . The output resistance of a transistor can be found as:

$$r_O = \frac{1}{\lambda I_{DS}} \text{ and } \lambda \propto \frac{1}{L} \quad (27)$$

However, the output current of a CP is expected to stay constant to reduce current mismatches no matter how the output voltage changes. The channel modulation has to be kept small so the r_O can be large. Therefore, the channel length L has to be long.

In addition, the saturation voltage $V_{DS,sat}$ can also be written as:

$$V_{DS,sat} = \sqrt{\frac{2I_{DS}}{\mu_n C_{OX}}} \left(\frac{L}{W} \right) \quad (28)$$

In order to have a low $V_{DS,sat}$ so that the output voltage range can be large, the L/W ratio has to be kept small. Therefore, if the L has to be large to get high output impedance, the W has to be large too to get small L/W ratio.

However, when the L and W are large, the gate and junction capacitance become large too. If the switch frequency is high, the speed performance of the CP becomes worse. Therefore, in this high-speed CP design, the key point is how to find a balance point between current mismatch, output voltage range, and speed.

After some comparison, the best approach is to use a cascaded structure as shown in Figure 21.

Figure 21. A cascaded structure.

From Figure 21, the output resistance can be obtained:

$$r_{out} = r_{o2} + r_{o3} + g_{m2}r_{o2}r_{o3} \quad (29)$$

where r_{o2} and r_{o3} are the output resistance of M_2 and M_3 respectively, and g_{m2} is the conductance of M_2 [8]. A cascaded transistor structure has much larger output impedance than a single transistor at the price of lower output voltage range. However, the size of M_2 and M_3 can be small so the total parasitic capacitance will be small. The speed performance of a cascaded structure CP will be better than a single transistor with same output impedance. To increase the output voltage range, the M_2 gate voltage V_{bias} can be adjusted [8].

The differential CP designed is shown in Figure 22.

Figure 22. A differential CP.

The differential CP has four cascaded current sources. Two pairs of CMOS switch transistors, M_5, M_6 and M_{12}, M_{13} , consist of the two UP switches. Similarly, M_3, M_4 and M_{14}, M_{15} , consist of the two DN switches. These switches are all controlled by rail-to-rail signals. The output current of this CP is $500\mu A$.

The sizes of all transistors can be found in Table 5.

Table 5: CP transistor size

Transistor	W(μm)	L(μm)	# of fingers
M_1	3.76	1.5	5
M_2	3.76	1.5	5
M_3	1.5	0.12	1
M_4	1.5	0.12	1
M_5	7.5	0.12	2
M_6	7.5	0.12	2
M_7	6.2	0.12	5
M_8	6.2	0.12	5
M_9	1.2	0.12	5
M_{10}	1.2	0.12	5
M_{11}	5	0.12	5
M_{12}	1.5	0.12	1
M_{13}	1.5	0.12	1
M_{14}	7.5	0.12	2
M_{15}	7.5	0.12	2
M_{16}	6.2	0.12	5
M_{17}	6.2	0.12	5
M_{18}	1.2	0.12	5
M_{19}	1.2	0.12	5

Before this version CP, a CML level input signal driven CP was developed first. Through simulation, there was still a certain amount leakage current existing when the CP was off. This is due to the CMOS switches cannot be fully on and off if driven by a CML level signal. To reduce the leakage current when the CP is off, the transistors are expected to be fully off. The CMOS switch voltages are operated at a rail-to-rail level. However, since the PFD is constructed in CML cells for differential structure and high speed performance, the output signal from the PFD is a CML level output. Therefore, a CML to rail-to-rail converter block is required between the PFD and CP. This block is expected to have a CML level input and a rail-to-rail output.

In this work, the converter used is similar to the circuit presented in [10]. The schematic of this converter is shown in Figure 23.

Table 6: CML to rail-to-rail converter transistor size

Table 6: CML to rail-to-rail converter transistor size

Simulation results show it can also work properly at 400MHz in this 0.13 μ m process.

Ideally when the CP is off, there is no current flowing through loop filter so the voltages on the loop filter can be kept constant. However, in reality, due to some unavoidable factors, such as leakage current, temperature, or current mismatches, the voltages on the loop filter will drift. Both of them will either go up or go down. Eventually either the NMOS or PMOS transistors will leave the saturation region and enter the linear region. Therefore a CMFB circuit is required to prevent this from happening.

Normally a CMFB circuit is designed to compare the common mode voltage with a reference voltage and use the difference of those two voltages to adjust the output current and therefore control the common mode voltage. The difficulty in this design is that in a locked state, the CP does not generate current so it is hard to control the common mode voltage through controlling the CP's current.

An alternate method is to design a separated CMFB block placed in the loop filter. When either side voltage of the loop filter drifts, this CMFB will charge or discharge the loop filter to pull this side voltage back to the right value. This idea is found in [11] and the circuitry is shown in Figure 24.

Figure 24. CMFB block circuit.

When the differential voltage $V_{\text{CNTL_P}}$ and $V_{\text{CNTL_N}}$ both go up, the NMOS transistors in the circuit will discharge the control lines so both $V_{\text{CNTL_P}}$ and $V_{\text{CNTL_N}}$ will drop. When $V_{\text{CNTL_P}}$ and $V_{\text{CNTL_N}}$ both go down, the PMOS transistors will charge the control lines so $V_{\text{CNTL_P}}$ and $V_{\text{CNTL_N}}$ will rise. Through this mechanism, the CMFB can set the common mode voltage and prevent the common mode voltage of $V_{\text{CNTL_P}}$ and $V_{\text{CNTL_N}}$ from drifting. The detailed transistor sizes for this CMFB block can be found in Table 7.

Table 7: CMFB transistor size

Transistor	W(μm)	L(μm)	# of fingers
M_1	0.5	0.12	1
M_2	0.5	0.12	1
M_3	1	0.12	1
M_4	1	0.12	1
M_5	2	0.12	10
M_6	2	0.12	10
M_7	2	0.12	10
M_8	1	0.12	50
M_9	1	0.12	50
M_{10}	1	0.12	50

5.3 Simulation Results

In this section, the simulation results associated with the CP and the CMFB are presented. The first plot is the output current from this differential CP versus the output voltage. It is shown in Figure 25.

Figure 25. NMOS and PMOS DC sweep output current versus voltage.

From Figure 25, when the output voltage is greater than 0.5V and less than 1V, the output current from NMOS and PMOS current source is almost matched. Therefore, the effective output voltage range is from 0.5V to 1V. However, since this CP is a differential CP the output range can be doubled. From a differential point view, the effective output voltage range is from -0.5V to 0.5V.

The above results are obtained based on a DC simulation. The speed performance of this CP can be obtained from a transient simulation. To better illustrate that the cascaded structure of the CP has better speed performance, an $L=1\mu\text{m}$ single current source is used to compare the output current of the two designs. The width of this single current source is set to a certain value so that the single current source has similar saturation voltage $V_{DS,sat}$. The simulation result is shown in Figure 26.

Figure 26. Transient output current simulation results (a) Cascaded structure (b) L=1 μ m single transistor, input is a 400MHz rail-to-rail signal.

From Figure 26, it is obvious the cascaded structure is faster than a long transistor.

The CML to rail-to-rail block simulation is shown in Figure 27.

Figure 27. CML to rail-to-rail block simulation results.

From Figure 27, the CML level input signal can successfully be converted into a rail-to-rail output. There is a certain delay between the input and the output, but since both the UP and DN signal paths have the same delay, this delay will not affect the CP performance severely.

Chapter 6 VCO

The core of a PLL system is a voltage-controlled oscillator (VCO). A VCO is an electronic oscillator whose output frequency can be controlled by a control voltage. In most cases, the control voltage used is the voltage present on the PLL loop filter.

Most VCOs can be divided into two categories. One is inductor based VCOs called LC-VCOs and the other is non-inductor based VCOs, such as ring VCOs. In general, an LC-VCO has better phase noise performance but at the cost of larger layout area due to the large area of the inductor [6]. Nevertheless, LC-VCOs are widely used in most wireless applications where phase noise performance is critical to the system's operation.

6.1 VCO Theory and Analysis

6.1.1 VCO Topology

A Colpitts VCO and a negative G_m VCO are two types of LC-VCOs commonly used. Today the negative G_m VCO structure is becoming more and more popular because of its simple structure and a relatively low gain requirement to sustain oscillations [12].

The basic working theory for a negative G_m VCO is to use one or two pair(s) of cross-coupled transistors to compensate for the loss in LC tank to maintain the oscillation. According to the different type of transistors used in the VCO, a negative G_m VCO can be identified as PMOS, NMOS or a complementary VCO as shown in Figure 28.

Figure 28. Negative G_m VCO topologies: (a) PMOS VCO, (b) NMOS VCO, and (c) Complementary VCO.

Much research has been done to compare the phase noise performance of the three topologies shown in Figure 28 recently. A common conclusion drawn is that the NMOS VCO has the worst phase noise performance due to the higher $1/f$ noise in NMOS transistors [6][13]. The PMOS VCO is said to have better phase noise performance because this type VCO has less active devices than the complementary VCO does and less active devices mean less noise [6]. Some other articles claim that the complementary VCO has better phase noise because it can enhance the symmetry of the output waveform and the symmetry of the VCO output can effectively suppress the up-conversion noise from the current source transistor [14][15].

To determine the VCO topology, except for the phase noise performance, the DC bias condition for varactors is also an important factor. In this $0.13\mu\text{m}$ process, available varactors are PN junction diode varactors and accumulation MOS (AMOS) varactors. The tuning voltage for the diode varactor is from 0V to -3V. The AMOS varactor has an

available tuning voltage V_{GD} from -0.5V to 1V. In this thesis, the AMOS varactors are selected due to their relatively higher Q and larger tuning range [6][14]. The tuning voltage from the loop filter is positive and connected to the drain of the AMOS varactor. To get a negative V_{GD} , the gate of the AMOS varactor must be biased at a certain voltage. It is easy to bias the AMOS varactor in the complementary topology because the NMOS switch transistors will provide the DC point required. However, in a PMOS only topology, a special arrangement is required to bias the AMOS varactor. Normally a decoupling capacitor can be used to isolate the AMOS varactor as shown in Figure 29.

Figure 29. Bias AMOS varactors.

However, the bias resistor R_{bias} must be large to block the AC current. The white noise of these two large resistors will directly be upconverted into the VCO phase noise, which should always be avoided. Another approach is to use a diode connected transistor to set DC point as shown in Figure 30.

Based upon the above considerations, a complementary structure is selected for this design.

The VCO in this work uses differential tuning. Differential tuning means the control voltages are differential signals. In a more conventional design as shown in Figure 28, the tuning voltage V_{CNTL} is a ground-referenced voltage used to tune the varactors. Any noise presented at this node can be converted to phase noise. To reduce this noise, a differential tuning topology can be implemented. A differentially tuned complementary VCO topology is shown in Figure 31.

Figure 31 Differential tuned negative G_m VCO.

In Figure 31, NFETs M_1 and M_2 and PFETs M_3 and M_4 are cross-coupled to provide a negative resistance to compensate for the loss in the resonator. The resonator consists of the inductor L and varactors C_{VAR} that determine the operating frequency. The varactors are controlled by the voltage difference between V_{cntl_p} and V_{cntl_n} .

6.1.2 RF Tank

In an LC-VCO, the core is the LC based RF resonator commonly called a “tank”. An ideal RF tank will present infinite impedance at the resonant frequency and a low impedance at harmonics. In an LC-VCO, the RF tank will attenuate all other frequency components and leave the resonant frequency component. This frequency component is the VCO fundamental output. Without the consideration of the parasitic capacitance, the fundamental output from an LC-VCO is given by:

$$\omega_o = \frac{1}{\sqrt{LC}} \quad (30)$$

where L and C are the inductor and capacitor in the RF tank respectively. Since parasitic capacitance is always present, the actual output frequency will be lower than ω_o . Nevertheless, equation (30) can predict the VCO output frequency relatively precisely [12].

In an LC tank, the on-chip inductor loss is usually the main loss. The key to the design of a low-phase-noise LC VCO is the design of a high quality LC tank [17][18]. However, at high frequency such as 24GHz, the varactor loss also becomes significant. The varactor Q will be lower. Therefore, the total LC tank loss is composed of the inductor loss and the varactor loss. Nevertheless, to design a high performance VCO can start from designing a high quality on-chip inductor.

To have a high quality on-chip inductor is always a big challenge in modern process technology due to unavoidable on-chip losses. These losses include parasitic capacitance, metal series resistance, and substrate losses. Moreover, the inductor loss will increase with the operating frequency because of the skin effect and proximity effect [12][18]. To describe the quality of an inductor, a quality factor, or Q, can be defined as

$$Q = \frac{|\text{Im}ng(Z_{ind})|}{|\text{Re}(Z_{ind})|} = \frac{\omega L_s}{R_s} \quad (31)$$

where Z_{ind} is the impedance of the inductor, R_s is the series loss, and L_s is the effective inductance [12]. The series loss R_s and inductance L_s can be converted to parallel resistance R_p and parallel inductance L_p as:

$$\begin{aligned} R_p &= R_s (1 + Q^2) \\ L_p &= L_s \left(\frac{Q^2}{1 + Q^2} \right) \approx L_s \end{aligned} \quad (32)$$

Therefore, the quality factor Q can be rewritten as

$$Q = \frac{R_p}{\omega L_p} \quad (33)$$

A more conventional method to define Q through simulation is shown in equation (34).

$$Q = -\frac{\text{Im}ng(Y_{11})}{\text{Re}(Y_{11})} \quad (34)$$

where Y_{11} is the Y parameter in a one-port SP simulation. From equation (3) and (4), to obtain a high Q inductor, the inductor series loss has to be small. A simple method can be used to estimate the loss in an inductor is shown in equation (35) [18].

$$R_s = \frac{2}{G_{SUB} L W} \quad (35)$$

In equation (35), L is the total length of an inductor, W is the metal width, and G_{SUB} is the conductance per unit area of the substrate. From equation (35), the easiest way to reduce R_s is to increase the metal width of the inductor at the price of reduction the effective inductance. In [18], a simple equation can be used to calculate the on-chip inductance. This equation is shown in equation (36).

$$L_s = \beta d_{out}^{\alpha_1} W^{\alpha_2} d^{\alpha_3} n^{\alpha_4} S^{\alpha_5} \quad (36)$$

where d_{out} is the outer length, W is the metal width, d is the average inductor length, n is the number of turns, and S is the metal spacing. Parameter β , α_1 , α_2 , α_3 , α_4 , and α_5 are process dependent but α_1 , α_2 , and α_5 are negative numbers. From equation (36), L_s is inversely proportional to W . Therefore, increasing W can reduce R_s but reduce the effective inductance simultaneously.

There are two conflicting points of view for the selection of an inductor for a low-phase-noise LC-VCO [18]. Some papers suggest selecting the inductor to be as large as possible without entering into the self-resonance region to get large output voltage swings [12][16]. However, from equation (35), the inductor series loss R_s is proportional to the effective inductance. When an inductor is selected to be as large as possible, the R_s also becomes high.

Another suggestion is that the selected inductor should be a balanced result between inductor size and inductor loss [18]. In other words, the Q should be at its peak at the operating frequency, which means the ratio between the effective inductance and loss R_s must be the highest.

After some comparisons, in this design, the inductor is selected following the second rule. The peak Q of the inductor is at 24GHz.

To make an oscillator tunable, a varactor is required in the LC tank. A varactor is a device whose capacitance can be varied with the control voltage. The output frequency f_0 of a VCO is given by equation (37).

$$f_0 = \frac{1}{2\pi\sqrt{L(C_{\text{var}} + C_{\text{fixed}})}} \quad (37)$$

where L is the inductor in the RF tank, C_{var} is the varactor capacitance and C_{fixed} is the parasitic capacitance and the fixed capacitors in the RF tank if required. The output frequency f_0 will change when C_{var} changes.

In this process, there are two types of varactors that can be selected. One is a PN junction varactor and the other is a MOS varactor. In this thesis, the MOS varactor is selected because it has relatively higher Q and a relatively large tuning range [6][14][20].

The MOS varactor is an NFET transistor in an N-well with N+ source and drains shorted together [20][21]. The total capacitance depends on the voltage difference between the gate and the source-drain. The MOS varactor cross section can be shown in Figure 32.

Figure 32. MOS varactor cross section.

A MOS varactor operates in three regions [21].

Accumulation region:

When the gate voltage V_G is positive, the majority carrier, n- in this case, is attracted to the surface of the N well to form a conduction plane, the MOS varactor is operated in the accumulation region. The total capacitance is approximately equal to the gate-oxide capacitance C_{ox} .

Depletion region:

When V_G goes from positive to negative, some minority carriers (holes) are attracted to the surface of the N well. These holes neutralize the electrons to form a depletion layer. This layer has capacitance C_{dep} . When V_G goes further negative, more holes are attracted to the surface of the N well, and consequently, the depletion layer increases and C_{dep} also increases. The total capacitance of the MOS varactor is approximately equal to $C_{var}=C_{ox}$ in series with C_{dep} , which is voltage dependant and can be controlled by varying the gate to drain/source voltage.

Inversion region:

When V_G goes to a certain negative voltage, a layer of holes is accumulated under the surface of the N well. This MOS varactor is operated in the inversion region. In this region, further reduction of V_G cannot increase the depletion region. The total capacitance is then a constant value which equals to C_{ox} in series with C_{fixed} . The models for MOS varactor in the three regions are shown in Figure 33.

Figure 33 MOS varactor models: (a) Accumulation region; (b) Depletion region; (c) Inversion region.

One important characteristic for a MOS varactor is its quality factor, Q . The Q for MOS varactor can be defined as:

$$Q = \frac{1}{\omega C R_s} \quad (38)$$

where R_s is the series parasitic resistance which includes the channel resistance R_{ch} and gate resistance R_G . The R_G is negligible if double-side gate and multiple fingers are employed and therefore the channel resistance R_{ch} is the dominant factor for R_s [21]. Therefore, to have a high Q varactor, the channel length has to be kept to the smallest length allowed by the technology for best Q and a multiple finger structure should be employed.

In a VCO design, the control line noise affects the VCO's phase noise through the varactor's C-V characterization. In other words, a small ΔV on the control line will cause a variation, ΔC , in the varactor, and this will cause the output frequency to be changed. The phase noise due to the control line noise ΔV is given by equation (39) [6].

$$PN = \left(\frac{\Delta V K_{vco}}{2\Delta\omega} \right)^2 \quad (39)$$

where K_{VCO} is the VCO gain and $\Delta\omega$ is the frequency offset. To reduce this noise up-conversion, a bank-switching technique is normally implemented to reduce the VCO gain K_{VCO} [6][16]. In this thesis, a differential tuning technique is implemented to reject this common-mode noise. The differential tuning varactors are shown in Figure 34.

Figure 34. Differential tuning varactors.

In Figure 34, the output nodes, out_p and out_n are common mode voltages. When V_{ctrl_n} goes down and V_{ctrl_p} goes up, both the C_{var+} and C_{var-} increases due to the increasing V_{GS} , and the total capacitance increases. When V_{ctrl_n} goes up and V_{ctrl_p} go down, the total capacitance decreases. If V_{ctrl_n} and V_{ctrl_p} both go up, the C_{VAR+} will increase because the V_{GS} increases, and C_{VAR-} will decrease because the V_{GS} decreases and the total capacitance does not change. The C-V characteristic for C_{var+} and C_{var-} can be seen in Figure 35 [6].

Figure 35. Capacitance versus differential tuning voltage

6.1.3 Oscillation Startup Condition

To analyze the start up condition for a complementary VCO in Figure 28, a small signal model for the cross-coupled NFETs M_1 and M_2 can be shown in Figure 36.

Figure 36. Small-signal model for the cross-coupled NMOS pair

The NMOS transistors are replaced by their equivalent T-models [22]. R_{S1} and R_{S2} are equal to $1/g_{m1}$ and $1/g_{m2}$. If the transistors are matched properly, then $g_{m1} = g_{m2}$ and $R_{S1} = R_{S2}$. V_{in} can be written as

$$V_{in} = (i_{in} + g_m V_{in}) \times \frac{2}{g_m} = 2V_{in} + \frac{2}{g_m} i_{in} \quad (40)$$

Therefore, the output resistance R_{in} can be found in equation (41).

$$R_{in} = \frac{V_{in}}{i_{in}} = -\frac{2}{g_m} \quad (41)$$

The cross-coupled PMOS transistors are similar to the NMOS counterpart and they provide another $-2/g_m$, if PMOS transistors and NMOS transistors are g_m matched. The total output impedance for the cross-coupled transistor pairs is $-4/g_m$.

In order to get a sustained oscillation, this output impedance has to cancel out the losses in the RF resonator, which can be modeled as a resistor R_p in parallel with the pure LC resonator. Therefore, a necessary start up condition for an oscillation is

$$g_m \geq \frac{4}{R_p} \quad (42)$$

6.1.4 Oscillation Output Amplitude

When the oscillation startup condition is met, the oscillation amplitude will increase. However, the oscillation amplitude will not increase indefinitely. Nonlinear effects in the transistors will limit the amplitude to some finite value and the oscillation will enter into a stable state.

In the stable state, if the cross-coupled transistors are ideally switched, the complementary topology VCO can be modeled as a current source in parallel with an R-L-C tank as shown in Figure 37 [15].

Figure 37. Complementary VCO equivalent circuit.

$I(t)$ in Figure 37 is the current steering from I_{bias} to $-I_{bias}$ for the complementary VCO. Here I_{bias} is the bias current for the VCO. R_p is to model the losses in the LC resonator. At the oscillation frequency, the admittance of inductor L and capacitor C cancel out each other. The output voltage V_{tank} is approximately equal to $R_p I(t)$. If the differential pair transistors are ideally switched, the current flowing through transistors is a series of pulses. Due to the existence of the LC tank, all other harmonics are absorbed except the fundamental component. The fundamental current component for PMOS or NMOS only VCOs is $i_{fund} = \frac{2}{\pi} I_{bias}$ [15], but for a complementary structure VCO, $i_{fund} = \frac{4}{\pi} I_{bias}$. Therefore, the tank voltage V_{amp} is approximately given by equation (43).

$$V_{amp} = \frac{4}{\pi} I_{bias} R_p \quad (43)$$

6.1.5 VCO Phase Noise

In a PLL system, the major out-of-band phase noise comes from the VCO's phase noise [6]. Thus, the phase noise performance for a VCO is highly critical.

In steady state, the output signal V_{osc} from VCO can be represented as:

$$V_{osc} = A \cos(\omega t + \varphi_n(t)) \quad (44)$$

where $\varphi_n(t)$ is the phase noise. In the frequency domain, the spectrum exhibits “skirts” around the center frequency [12][16].

The noise sources in the VCO can be divided into two groups. One is the intrinsic noise sources and another is the extrinsic noise sources. The intrinsic noise sources are those existing in the VCO internal circuits. The extrinsic noise, such as supply noise, substrate noise and control line noise are coupled from the outside world to the VCO.

Intrinsic noise sources:

The major intrinsic noise sources in the VCO are transistor noise and RF tank noise. They can be modeled as in Figure 38 [15].

Figure 38 VCO with noise sources

In Figure 38, the V_n is the effective noise source to represent the noise from RF tank losses. As described before, the RF tank losses can be modeled by a parallel resistor R_p . The noise spectrum density can be written as in equation (45) [15].

$$\frac{\overline{i_n^2}}{\Delta f} = \frac{4KT}{R_p} \quad (45)$$

The two pairs of switching transistors in the VCO also contribute noise. In CMOS transistors, the main noise sources are $1/f$ noise and channel noise [7]. The total differential noise power summarized in [15] can be written as:

$$\overline{i_n^2} = \frac{1}{4}(i_{n1}^2 + i_{n2}^2 + i_{p3}^2 + i_{p4}^2) = \frac{1}{2}(i_n^2 + i_p^2) \quad (46)$$

The noise density can be written as ($1/f$ noise is not included):

$$\frac{\overline{i_n^2}}{\Delta f} = 4KT\gamma\mu C_{ox} \frac{W}{L}(V_{GS} - V_T) \quad (47)$$

where γ is a process dependent number and in short channel it is between 2 and 3.

The noise source due to the RF tank losses is unavoidable, however it can be reduced by properly selecting the inductor and varactor in the RF tank as described in section 6.1.2.

The noise in the two pairs of switching transistors is also critical to the VCO phase noise. Since the channel noise of a transistor is proportional to the current, the channel noise is hard to reduce if the current has to maintain a certain level. The $1/f$ noise can be reduced by increasing the transistor's length and width.

In addition, the current source noise up-conversion is a major contributor to the total phase noise. An inductor in series in the current path is an effective way to reduce the noise up-conversion but at the price of large area. Another method is to place a large capacitor in parallel with the current source. The purpose of this capacitor is not only to reduce the channel noise from the current source transistor but also to provide an alternative current path so that the current is flowing through transistors in a class-C manner. The switching transistors are off most of the time, and conduct for only a small percentage of a whole period [15][27]. In this thesis, the operating frequency is so high that the

current source transistor's parasitic capacitance is large enough to shape the current so no extra capacitor is required.

Since the current source noise is up-converted into close-in phase noise through the VCO's mixer action, the even-order components must be suppressed as much as possible. Therefore the single-end output waveform has to be symmetric to reduce the even order components. This is a reason why some people believe a complementary VCO topology VCO provides better phase noise performance because the complementary VCO can enhance the symmetry of the output waveform [15].

To get a symmetric output waveform, the transconductance, g_m , of the NMOS and PMOS transistors have to be matched. This can be done by carefully sizing the NFETs and PFETs so that the absolute saturation voltages, $|V_{GS}-V_T|$, are equal.

Extrinsic noise sources:

The extrinsic noise sources include supply noise, substrate noise and control line noise. To reduce supply noise and substrate noise is not included in this thesis but in general a large filter and, isolation ring protection and careful layout are required. Differential tuning is implemented to suppress the control line noise as described in section 6.1.1.

6.1.6 VCO Amplitude and Bias Current Optimization

The VCO's phase noise can be calculated through Leeson's equation. One form of Leeson's equation is shown in equation (48) [11].

$$PN = \left[\frac{\omega_o}{2Q\Delta\omega} \right]^2 \left(\frac{FkT}{2P_s} \right) \quad (48)$$

where ω_0 is the center frequency of the oscillation, Q is the quality factor of RF tank, $\Delta\omega$ is the offset frequency, F is the excess noise factor for losses other than the RF tank, k is Boltzmann's constant, T is the absolute temperature, and P_S is the output power.

From equation (48), to get low phase noise, the amplitude and the RF tank Q has to be large. Normally, a VCO can be identified as working in either a current limited region or a voltage limited region [15]. In a current limited region, increasing the bias current can increase the output amplitude. In a voltage limited region, the output amplitude is limited by the supply voltage so any further increase in the current will not lead to any increase of the output amplitude but will increase the noise. The optimal amplitude and bias current for the best phase noise is the crossover point between the current limited region and the voltage limited region as shown in Figure 39.

Figure 39 Optimization point for a low phase noise VCO

6.2 VCO Design procedure

6.2.1 Inductor Selection

In this CMOS process, there are two kinds of inductors available. One is a single-ended spiral structure and the other is center-taped differential spiral structure. In general, for a

differential structure VCO, a differential inductor is preferred since it has a good symmetric structure and higher Q compared with two identical single-ended inductors connected back-to-back [12].

In this design kit, the smallest differential inductor is 500pH. To generate a 24GHz output signal, the total capacitance in this VCO has to be:

$$C_{total} = \frac{1}{\omega^2 L} = 88 fF \quad (49)$$

This value is too small to tolerate the parasitic capacitance in the circuit. Therefore, a single-ended inductor has to be selected even though it is not symmetric.

After comparison in simulation, the parameters for the inductor were chosen as shown in Table 8.

Table 8. Inductor parameters

Parameter	Value
Out Dimension	110 μm
Metal Width	5 μm
Number of turns	1
Underpass Width	15 μm
Space	5 μm

The simulation results for this inductor are shown in Figure 40.

Figure 40 Inductor value and Q value versus frequency.

From Figure 40, the inductor is 280pH and has peak Q around 20.7 at 24GHz. The self-resonance frequency is far above the operating frequency. Therefore this inductor is safe to be operated at 24GHz. The parallel resistor R_p can be found in equation (50).

$$R_p = \omega L_p Q = 2\pi \times 24G \times 280p \times 20.7 = 874\Omega \quad (50)$$

6.2.2 Varactor Selection

In this thesis, the nominal RF output frequency is 24GHz and the IF signal frequency is 400MHz. Assuming that the IF signal frequency could be as low as DC and as high as 800MHz, the RF output must cover from 24.4GHz to 23.6GHz if the LO frequency is 23.6GHz as defined in section 3.1.

Since the inductor is 280pH, the nominal C_{total} in the RF tank can be calculated as:

$$C_{total} = \frac{1}{\omega^2 L} = \frac{1}{(2\pi \times 24G)^2 (280p)} = 157 fF \quad (51)$$

To cover the output range from 23.6GHz to 24.4GHz, the C_{max} is 162fF and C_{min} is 151fF. ΔC is around 11fF.

Assuming the overdrive voltage for the charge pump transistor is 0.25V, the positive control voltage can vary from 0.25V to 1.25V. Simultaneously, the negative terminal can vary from 1.25V to 0.25V. Therefore, the possible differential tuning voltage is from -1V to 1V. The slope of varactors is $K_{var} = \Delta C / \Delta V = 5.5fF/V$.

As described in section 6.1.2, the accumulation MOS varactors were selected in this VCO design. The parameters for the varactors in this design are shown in Table 9.

Table 9. Varactor parameters

Parameter	Value
RX (active region) width	1 μ m
PC (poly gate) length	0.24 μ m
Number of gates	5
RX Repetition	5
Multiplicity	1

The simulation results for the varactors versus different tuning voltages are shown in Figure 41.

Figure 41 Varactor versus tuning voltage

From Figure 41, when the tuning voltage changes from -1V to +1V, the total varactors change from 45fF to 60fF. The $\Delta C=15\text{fF}$. It is large enough to cover the range required. From design menu, a single AMOS varactor has available tuning range from -1 to +0.5V, the possible differential tuning range is from -1.5V to +1.5V. As a result, the -1V to +1V tuning voltage is located within the linear tuning range.

6.2.3 Transistor Size

The supply voltage for this VCO is 1.5V. The current source transistors take 0.3V as the minimum output voltage. The maximum output swing is from 0~1.2V. Therefore, the DC biasing point for this VCO output node is set to be 0.6V.

Since in this $0.13\mu\text{m}$ technology, the μ_n is approximately three times larger than μ_p [12], the PMOS transistors are sized almost three times wider than the NMOS transistors to get

g_m matching. The lengths of all transistors are set to 120nm, which is the minimum length this technology allows. By setting the minimum length the transistors can be switched fast. In addition, by keeping the transistors short, the tuning range of VCO could become larger.

In this thesis the VCO will drive a mixer and will be connected to a spectrum analyzer. The current in this VCO will be relatively large. In this design, the VCO draws 2mA of bias current. The size of the switching transistors is shown in Table 10.

Table 10 Switching transistors size

Parameter	Value
PMOS width	6 μ m*7
PMOS length	0.12 μ m
NMOS width	2 μ m*7
NMOS length	0.12 μ m

The current source transistor has to be long enough to have large output impedance. In addition, a long and wide device will have less 1/f noise [5][7]. Since the headroom for the current source transistor is only 0.3V, the width of this transistor has to be large. The diode-connected transistor for this current mirror is sized to have a 1:1 ratio to have less noise multiplication at the price of more power consumption [14].

The actual size for the current mirror transistors is shown in Table 11.

Table 11 Current mirror transistors sizes

Parameter	Value
PMOS width	16 μ m*40
PMOS length	1 μ m

6.2.4 Output Buffer Design

The main purpose of a VCO buffer is to provide isolation between the VCO core and the outside circuitry it must drive. A commonly used buffer is a source follower but it is not

used in this thesis due to the large parasitic capacitance of the current source as shown in Figure 42.

Figure 42. A source follower as a VCO output buffer.

At 24GHz, this parasitic capacitor C_{para} will shunt the current source to ground. Consequently, the output voltage swing cannot follow the input swing.

To solve this problem, a differential input topology buffer is selected instead of single-ended buffer like the source follower. The differential buffer can be a CML buffer or a push-pull buffer. In this thesis, a CML buffer is chosen because the CML output swing can directly match the mixer input without the need for a voltage divider. The CML buffer is shown in Figure 43.

Figure 43 A CML buffer for the VCO.

Because the VCO has to have the capability to drive the mixer and a test probe, a large current is required in this VCO buffer stage. In this design, the bias current is designed to be 5mA.

6.3 Simulation Results

The output frequency versus differential control voltage can be seen in Figure 44.

Figure 44. Output frequency versus differential control voltage.

From Figure 44, the K_{VCO} is around 500MHz/V. It is enough to cover the overall band required. There is a small frequency variation between the differential output frequencies when the differential voltage is 0.3V. This frequency variation is most likely caused simulation method. The plot in Figure 44 is obtained through a transient simulation. To get more precise results, a periodic steady state (PSS) simulation should be applied on the VCO's output voltages to get the fundamental tone frequency.

The phase noise performance of this VCO can be seen in Figure 45.

Figure 45. Phase noise simulation result.

In this transmit PLL system, the bandwidth is designed to be 1MHz. At 1MHz offset, the phase noise is simulated to be -104.7dB/Hz.

Chapter 7 Mixer

A mixer is a circuit that converts an input signal from one frequency to another frequency [12][16]. According to the input and output frequency, the mixer can be identified as an up-conversion mixer or a down-conversion mixer. The purpose of a down-conversion mixer is to convert a high frequency input spectrum into a low frequency output spectrum. In this thesis, the mixer is placed in the feedback path in the transmit PLL to down convert the output from the VCO to a low frequency signal and send this signal to the PFD.

7.1 Mixer Working Theory

Today the most common mixer topology is the double balanced mixer, which is also called a Gilbert Cell Mixer. The double balanced topology is composed of two single balanced configurations. The advantage of the double balanced mixer over the single balanced mixer is that the double balanced mixer has better immunity to the LO leakage, which is also called LO feed-through [16].

A common Gilbert Cell mixer is shown in Figure 46.

Figure 46. A Gilbert Cell mixer.

In Figure 46, the lower differential pair M_1 and M_2 is driven by a differential signal, which is the RF input signal. The upper quad transistors, from M_3 to M_6 are switched by the LO signal. If the input is V_{IN} and the output is V_{OUT} , the conversion gain of the mixer can be found as:

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{2}{\pi} g_{m1} R_L \quad (52)$$

where g_{m1} is the transconductance of the lower differential pair transistors [5][11].

However, in this thesis, the RF signal is not a small signal received from a low noise amplifier (LNA). It is the feedback signal from VCO output and is a large signal. Fast frequency response is the main concern of this mixer. To get a fast frequency response and

the maximum output swing, both the upper quad and lower differential transistors are all fully switched. Ideally the output voltage swing $V_{\text{swing}} = I_{\text{bias}}R_L$. However, since the RF and LO frequencies are very high, the parasitic capacitance in the mixer circuit will make the voltage swing smaller than this simple estimation.

The capacitor C_C in parallel with R_L implements a RC low-pass filter with corner frequency f_C to select the desired IF band frequency signal from the mixer output signal. The corner frequency f_C can be found as:

$$f_C = \frac{1}{2\pi C_C R_L} \quad (53)$$

7.2 Design Procedure

7.2.1 DC Biasing

In this transmit PLL the supply voltage is 1.5V. The bias current I_{bias} is selected to be 1mA. The output swing is expected to be 500mV. Therefore, the load resistor is set to be $R_L = 500 \Omega$. The output frequency is expected to be from DC to 600MHz. The lowpass filter has a corner frequency no less than 700MHz. Thus, the C_C can be found as:

$$C_C = \frac{1}{2\pi R_L f_C} = \frac{1}{2\pi(500)(700M)} = 455 \text{ fF} \quad (54)$$

The current source requires at least 0.3V headroom. If all the transistors are ideally switched, the output should be 0.5V. Thus, for a 1.5V supply voltage, there is 0.7V headroom left for the upper quad and lower differential pair transistors.

The switching transistors should be sized properly to make the switching more abrupt and to reduce the time when two transistors are turned on simultaneously. For a given bias

current, the switching transistors could be sized with a large width so that the V_{GS} can be set only a little higher than the threshold voltage V_{TH} [1]. However, in this work, since the input frequency is extremely high, the switching transistors cannot be made too wide since the large gate capacitance will shunt the input signal.

The mixer schematic with bias information is shown in Figure 47 and the final size of the transistors is listed in Table 12.

Figure 47. Gilbert cell mixer.

Table 12: Inductor Dimensions

		Width (μm)	Length (μm)	# of fingers
Transistor	M_1	1.5	0.15	30
	M_2	1.5	0.15	30
	M_3	1	0.15	10
	M_4	1	0.15	10
	M_5	1	0.15	10
	M_6	1	0.15	10
	M_7	10	1	5
	M_8	10	1	5
Resistor		Value(Ω)		
	R_L	500		
	$R_{LO \text{ bias}}$	10K		
	R_{bias}	10K		
Capacitor		Value (F)		
	C_L	455f		
	C_C	1p		
	C_f	0		
Bias voltage		Value (V)		
	$V_{RF \text{ bias}}$	0.8		
	$V_{LO \text{ bias}}$	1.2		

7.2.2 Output Buffer

The purpose of the mixer output buffer is to isolate the Gilbert cell mixer and outside circuitry. In addition, a good output buffer can further suppress the high-order harmonics generated to smooth the output waveform. In this design, the mixer output signal is sent into one port of the CML based PFD to compare with the reference signal. Based on the above analysis, a CML buffer is appropriate for this design. The advantage of this CML buffer is that it is easily implemented and easily interfaced with the PFD. No extra bias circuitry is required between the mixer and the PFD. However, the output from the mixer must be strong enough to drive a spectrum analyzer through test pads, and therefore the CML buffer requires a large bias current. The CML buffer is shown in Figure 48.

Figure 48. Mixer output buffer.

The size of the buffer components is listed in Table 13.

Table 13: Mixer output buffer components value.

Transistor		Width (μm)	Length (μm)	# of fingers
	M ₁	1	0.15	8
	M ₂	1	0.15	8
	M ₃	8	2	20
Resistor		Value (Ω)		
	R _L	500		
	R _{bias}	15K		
Capacitor		Value (pF)		
	C _C	5		
Bias voltage		Value (V)		
	V _{bias}	1.1		

7.2.3 Single-ended to Differential Converter

Similar to the PFD described in section 4.3, the LO signal is from a signal generator and it is a single-ended signal. To properly switch the mixer, a single-ended to differential converter is required to convert this single-ended signal into a differential form. Since the

LO signal is around 23.6GHz, it is difficult to find an off-chip balun to perform this task. Therefore it is necessary to design an on-chip single-ended to differential converter.

The simplest way to build such a converter is to use a differential pair with one input AC grounded as shown in Figure 49. As described in section 4.3, if a single-ended signal V_{in} is applied to a differential pair, it can be viewed as two signals which have the common mode part $V_{in}/2$ and differential mode $\pm V_{in}/2$. Therefore, the differential mode gain is still $g_m R_L$ as shown in equation (23). The g_m and the R_L are the transconductance and the load resistor of the differential pair, M_1 and M_2 in Figure 49, respectively. The common-mode gain is

$$A_{V,comm} = \frac{g_m R_L}{1 + g_m R_{SS}} \quad (55)$$

where R_{SS} is the impedance of the current source transistor, M_3 . However, when the input frequency is very high, the parasitic capacitance C_p of the current source M_3 will shunt the node P to ground. The R_{SS} becomes very small. The common mode is close to $g_m R_L$. Consequently, the common mode rejection ratio (CMRR) becomes much worse. The output signal will not be a pair of differential signals as expected.

Figure 49. The high-frequency single-ended to differential converter.

To solve the CMRR problem, the impedance at node P must be increased. There are three ways to increase the current source impedance as shown in Figure 50.

Figure 50. Possible ways to improve CMRR (A) inductor (B) cascaded (C) resistor as source degeneration.

In Figure 50, the first approach is to use an inductor to increase the impedance. This method is simple and easy to implement. However, the problem is the inductor takes large chip area, which is limited in this design. The other way is to use a cascaded current mirror structure. The output impedance of the current mirror can be found as $r_{o3} + r_{o4} + g_{m3}r_{o3}r_{o4}$ [16]. This method can effectively reduce the parasitic capacitance if M_3 and M_4 are selected to be small. An alternative way is to use a resistor R_S as source degeneration. The output impedance is approximately $g_{m3}r_{o3}R_S$ [16]. This method can also reduce the parasitic capacitance since the M_3 can be a small transistor. The drawback of these two methods is they both require more headroom. However, since the supply voltage is 1.5V, it is not difficult to implement the cascaded current source or source degeneration. The simulation results show both methods can work properly. In this design, the resistive source degeneration method is selected. To get a more balanced output, two stages of differential pairs are used as shown in Figure 51.

Figure 51. Two-stages of differential pairs as single-ended to differential converter.

The transistor dimension and resistor values are listed in Table 14.

Table 14. High-frequency single-ended to differential converter components value.

		Width (μm)	Length (μm)	# of fingers
Transistor	M_1	1	0.12	15
	M_2	1	0.12	15
	M_3	2	0.12	25
	M_4	1	0.12	15
	M_5	1	0.12	15
	M_6	3.2	0.12	25
Resistor		Value (Ω)		
	R_{L1}	200		
	R_{L2}	150		
	R_{S1}	45		
	R_{S2}	50		
Bias voltage	V_{REF}	Value (V)		
		0.8		

7.3 Simulation Results

To simulate the down-conversion mixer and the high frequency single-ended to differential converter, a single-ended 23.6GHz signal is used as the LO input signal and a differential signal at 24GHz is sent into the mixer as the IF signal. The output from the single-ended to differential converter is shown in Figure 52.

Figure 52. Single-ended to differential converter simulation result.

From Figure 52 it can be seen the output signal is not a perfectly balanced differential signal. However, the lowest differential peak-to-peak amplitude is 290mV, which is sufficient to switch the mixer quad transistors.

The output signal from the down-conversion mixer in time domain is shown in Figure 53.

Figure 53. Down-conversion mixer output waveform.

The output signal is an 800mV peak-to-peak differential signal. The swing is less than the theoretical value, which is $2I_{bias}R_L = 1V$. The reason is at a high frequency such as 24GHz, the parasitic capacitance becomes more significant than at low frequencies. Therefore, the differential output swing will be less than $2I_{bias}R_L$.

The output waveform has some high frequency ripples that are caused by the 23.6GHz LO feed-through. Although differential structure is chosen, the LO feed-through cannot be eliminated completely. In addition, the RC filter is first order and only has -20dB/dec roll off, so the LO feed-through is presented at the output.

To further analyze the high-order noise, a DFT calculation is performed on the output waveform. The result is shown in Figure 54.

Figure 54. Down-conversion mixer output spectrum.

The fundamental component of the output is 400MHz which is as expected. The third order harmonic is 32.1dB lower than the fundamental. The high-order components are further suppressed by the lowpass filter in the mixer.

Chapter 8 Layout and Measurement Results

In this chapter, the chip layout and test PCB layout are introduced followed by the measurement results. Unfortunately this transmit PLL only works partially. A failure analysis is included in this chapter.

8.1 Layout

The top-level layout is shown in Figure 55.

Figure 55. Top layout.

The total die area is $985 \times 980 \mu\text{m}^2$. This chip has two RF input pads and four RF output pads. One RF input pad is used for the 23.6GHz LO input and the other input pad is oc-

cupied by the 400MHz IF input. Two RF output pads are used for the VCO differential outputs and another two are reserved for the mixer differential outputs. In addition, there are two pads at the top used to monitor the differential control voltages developed on the differential loop filter.

The supply and ground for the high-frequency part of the circuit, including the VCO and the mixer, has two dedicated pads which are called V_{cc_rf} and V_{ss_rf} . The other blocks have a supply and ground called $V_{dd_digital}$ and $V_{ss_digital}$. By doing this, it is possible to test the high-frequency or low-frequency part of the circuit independently. In addition, the noise coupling from the supply trace can be reduced.

This 0.13 μ m process requires a large antenna diode to pass the antenna check. However, a large antenna diode means large parasitic capacitance. The antenna diode at the VCO output significantly reduces the VCO output swing. In addition, at such a high frequency, the wire trace presents transmission line effects, and the output frequency becomes lower than 24GHz. To reduce these parasitic effects, the trace between the VCO and the mixer should be kept as short as possible and the layout should be kept compact.

8.2 Post-layout Simulation Results

After the layout passed the design rule check (DRC) and the layout versus schematic (LVS) check, a post-layout simulation was performed to check how much the parasitics affect the results. The first step was to check the VCO output frequency. The free running VCO post-layout simulation result shows the output frequency was 22.5GHz, which was lower than 24GHz. In a future submission, the VCO circuit should be modified to reduce the parasitic transmission line effects to center the output frequency. That is not an easy job because the inductor models in this 0.13 μ m process have an upper frequency limit at only 20GHz. Besides, the inductor in use is already close to the minimum one in the process library. To further increase the output frequency, another possible approach is to reduce the varactor size but this will reduce the VCO tuning range. One could also re-

duce the switching transistors' size to reduce the parasitic capacitance but this will reduce their g_m . Therefore it will take time to modify the output frequency.

Unfortunately the VCO simulation results were only obtained close to the tape out time. There was not sufficient time to increase the free-running VCO output frequency. This problem was left for the next version of the design in a future tapeout.

Since the free running VCO output frequency is 22.5GHz, the LO frequency can be set to be 22.1GHz. The IF signal frequency is set to be 430MHz which is same as the step size shown in behavior mode simulation. The post-layout simulation results of the control line voltages are shown in Figure 56.

Figure 56. Control line voltage simulation results.

The differential control voltages in Figure 56 show the transmit PLL is in a locked state after 200ns. However there are still some high-order harmonics on the control lines,

which should be theoretically absorbed by the lowpass loop filter. The reason is the metal-insulator-metal (MIM) capacitor in the loop filter is not an ideal capacitor. The biggest MIM capacitor is around 430pF so the trace is relatively long. Through simulation, the MIM capacitor has self-resonance frequency of only 1.52GHz but this VCO has output frequency at 22.5GHz. Therefore the MIM capacitor cannot further remove the high-order harmonics completely. The characteristic of the MIM capacitor in the loop filter is shown in Figure 57.

Figure 57. MIM capacitor characteristics.

The total current drawn from the supply is 45.6mA. The VCO and mixer take 22mA and the other blocks take 23.6mA.

8.3 Measurement Results

8.3.1 PCB

This design is fabricated by CMC and MOSIS. To test this chip, a printed circuit board (PCB) is designed with ORCAD. This PCB is shown in Figure 58.

Figure 58. PCB for the test chip.

This PCB is a four-layer high-frequency PCB constructed with FR4 material. FR4 is quite lossy at 24GHz. A better high-frequency material is RO18 but it is much more ex-

pensive and requires longer time to be delivered from the manufactory. Thus, FR4 is still selected in this work.

The loose die is surface mounted on this PCB. The on-chip pads are connected to the PCB pads through bond wires. To reduce the bond wire effect, which is roughly 1nH/mm, the VCO output pads are put close to the PCB pads.

The test setup in the lab is shown in Figure 59.

Figure 59. Test setup.

8.3.2 VCO and Mixer measurement results

To test this Transmit PLL, the first step is to find the VCO output frequency. To eliminate other parasitic effects, a good approach is to measure the VCO output using high

frequency wafer probe. In this measurement, a three-pin probe was used. The free running VCO output was measured with a 40GHz spectrum analyzer. This bandwidth of this spectrum analyzer is set to be 30KHz. The output spectrum is shown in Figure 60.

Figure 60. Free running VCO output spectrum.

The VCO output is at 21.51GHz, which is 1GHz lower than the post-layout simulation result. This is due to the fact that the trace parasitic is not totally extracted in the simulation. The VCO output power is low due to the parasitic capacitance, trace inductance in the circuit, as well as the cable loss and other loss in the test equipment.

The VCO tuning range can be measured by applying two control voltages directly on the V_{CNTL_P} and V_{CNTL_N} pads and measuring the output tone. The measurement result is plotted in Figure 61.

Figure 61. VCO tuning range measurement results.

This differential VCO can be tuned from 21.15GHz to 22.05GHz. The VCO gain is

$$K_{vco} = \frac{22.05\text{GHz} - 21.15\text{GHz}}{0.7 - (-1)} = 588.24\text{MHz/V} \quad (56)$$

This measurement result is very close to the 555MHz/V simulation result.

When the VCO output frequency and tuning range are known, it is possible to measure the mixer output frequency if a proper LO signal is applied. When a 21.1GHz LO signal with 10dBm amplitude is input into the mixer, the output frequency from the mixer can be plotted as shown in Figure 62.

Figure 62. Mixer output measurement results.

The red line is the actual measurement results and the blue line is the theoretical results obtained by subtracting the LO frequency from the VCO output frequency. Obviously the actual mixer output is very close to the theoretical value.

The VCO and mixer draw 21mA of current, which is close to the 22mA simulation result.

8.3.3 Full Loop PLL measurement results

To check whether the transmit PLL is in lock or not, the mixer output frequency was measured. If the transmit PLL is in lock, the mixer output frequency should be exactly equal to the IF input frequency.

Unfortunately, this transmit PLL measurement shows the transmit PLL can achieve lock within only a very narrow range. The measurement result is reported in the Table 15.

Table 15. transmit PLL measurement results

f_{LO} (GHz)	f_{IF} (MHz)	V_{CNTL_P} (V)	V_{CNTL_N} (V)
20.5	381	0.132	1.364
20.5	390	0.163	1.332
20.5	393	0.130	1.320
20.5	395	0.176	1.318
20.5	400	0.194	1.291

From Table 15, it can be seen when the IF frequency varies from 381MHz to 400MHz, the transmit PLL can lock. Beyond this range, the transmit PLL loses lock but can enter into a steady state. The output frequency will try to follow the IF frequency but there is always a certain offset between the mixer output and the IF signal. This offset is not fixed and will vary with the VCO output frequency.

The PFD and CP blocks drew current of 206mA but simulation showed the current should be only 23.6mA. This large current implies either a short circuit exists in the circuit or a PN junction diode has turned on when the power is on. If this large current is caused by a PN junction diode, when the supply voltage becomes lower than some certain value, such as 0.7V, this large current will disappear. However, in this work, when the supply voltage was adjusted from 0.3V to 2V, the current still existed. The results are reported in Table 16.

Table 16. PFD/CP supply voltage and current measurement results.

Voltage (V)	Current (mA)
0.3	41.0
0.5	50.0
1.2	173
1.5	206
1.8	245
2.0	279

From Table 16, the relationship between voltage and current is almost linear. The resistance is approximately 7Ω . In this case, a short circuit in the circuitry is highly suspected and the 7Ω resistance is most likely the wire resistance.

The short circuit may be caused by schematic design, layout design, PCB design or process mistakes. However, the top-level circuit has passed schematic simulation and post-layout simulation so the chance for schematic short or layout short is very small. However, after post-layout simulation, some components were added to meet the manufacturers' requirement. These components include ESD diodes, clamps, and a chip ring. The ESD diodes and clamps are chosen from the process library directly and used in both high frequency and low frequency input and output pins. Since the high-frequency part works properly, the ESD diodes and clamps for the low-frequency circuitry are also expected to work properly. The last component is the chip ring, which is also chosen from the process library. Before the chip ring was added, the top-level layout connectivity of the low-frequency supply, $V_{dd_digital}$, and ground, $V_{ss_digital}$, is shown in Figure 63 and Figure 64 respectively.

Figure 63. Connectivity of $V_{dd_digital}$ without chip ring.

Figure 64. Connectivity of $V_{ss_digital}$ without chip ring.

From Figure 63 and Figure 64, $V_{dd_digital}$ and $V_{ss_digital}$ are separated properly. However, after the chip ring is added, the connectivity of $V_{dd_digital}$ and $V_{ss_digital}$ is shown in Figure 65.

Figure 65. Connectivity of $V_{dd_digital}$ and $V_{ss_digital}$ with chip ring.

From Figure 65, $V_{dd_digital}$ and $V_{ss_digital}$ are shorted. The problem is in the top ring, which is connected to $V_{dd_digital}$ by mistake as shown in Figure 66.

Figure 66. $V_{dd_digital}$ is connected to chip ring by mistakes.

The top ring is normally connected to ground. Therefore, $V_{dd_digital}$ and $V_{ss_digital}$ are shorted together. Since the short circuit exists, the low-frequency part does not work properly.

Chapter 9 Conclusions

This work has implemented a high-frequency transmit PLL in a 0.13 μ m process. This transmit PLL has fully differential architecture. Through simulation, this work has demonstrated that this transmit PLL with 24GHz output frequency and 400MHz comparison frequency is possible.

This work has been manufactured and tested. Unfortunately, due to the careless layout problem, a short circuit exists in this work. Only partial of this work can work properly. The measurement results of the high frequency part circuit, including VCO and mixer blocks, are close to the design specifications. Therefore, this 0.13 μ m process is reliable, and because the post-layout simulation results are correct, this work should work properly if this short circuit can be fixed in next tape-out.

9.1 Future work

Future work involves fixing this failure. A laser cut can be used to cut the short between chip ring and $V_{dd_digital}$. The next step is to test the full chip to see whether it can lock over the whole tuning region required. If this transmit PLL can get lock properly, the total current consumption should be reduced to save power. Another issue is the VCO output buffer. To properly measure the performance of this transmit PLL, such as phase noise, one or more large buffers are required to amplify the VCO output

Further work could also involve a PA design at 24GHz to finish this Transmit PLL.

Appendix A

Differential VCO

```
`include "discipline.h"
`include "constants.h"
`define PI 3.14159265358979323846264338327950288419716939937511

module diff_vco (vin_p,vin_n, vout_p, vout_n);
input vin_p,vin_n;
output vout_p, vout_n;
electrical vin_p,vin_n, vout_p,vout_n;
parameter real amp = 1;
parameter real center_freq = 5G;
parameter real vco_gain = 150M;

real wc; // center freq in rad/s
real phase_lin; // wc*time component of phase
real phase_nonlin; // the idt(k*f(t)) of phase
integer num_cycles; // number of cycles in linear phase component
real inst_freq; // instantaneous frequency

analog begin
  @ ( initial_step ) begin
    wc = 2 * `PI * center_freq;
  end

  phase_lin = wc * $abstime;
  num_cycles = phase_lin / (2*`PI);
  phase_lin = phase_lin - num_cycles * 2 * `PI;

  phase_nonlin = 2 * `PI * vco_gain * idt ( (V(vin_p)-V(vin_n)), 0);

  V(vout_p) < amp * sin (phase_lin phase_nonlin);
  V(vout_n) < (-1)*amp * sin (phase_lin phase_nonlin);
  //
  // ensure that modulator output recalculated soon.
  //
  inst_freq = center_freq vco_gain * (V(vin_p)-V(vin_n));
  $bound_step (0.04 / inst_freq);
end
endmodule
```

Phase-Frequency Detector

```
`include "discipline.h"
`include "constants.h"
`define behind 0
`define same 1
`define ahead 2

module diff_freq_ph_detector(vin_if_p,vin_if_n, vin_lo_p,vin_lo_n, sigout_inc, sigout_dec);
input vin_if_p,vin_if_n, vin_lo_p,vin_lo_n;
output sigout_inc, sigout_dec;
electrical vin_if_p,vin_if_n, vin_lo_p,vin_lo_n, sigout_inc, sigout_dec;
parameter real vlogic_high = 1;
parameter real vlogic_low = -1;
parameter real vtrans = 0;
```

Appendix A

```
parameter real tdel = 0 from [0:inf];
parameter real trise = 1p from (0:inf);
parameter real tfall = 1p from (0:inf);

integer tpos_on_if, tpos_on_lo; // flags for transitions on the inputs

real sigout_inc_val, sigout_dec_val;

integer state;

analog begin
  @ ( initial_step ) begin
    sigout_inc_val = 0;
    sigout_dec_val = 0;
    state = `same;
  end

  tpos_on_if = 0;
  @ ( cross(V(vin_if_p) - vtrans, +1) )
    tpos_on_if = 1;

  tpos_on_lo = 0;
  @ ( cross(V(vin_lo_p) - vtrans, +1) )
    tpos_on_lo = 1;

  if (tpos_on_if && tpos_on_lo) begin
    state = `same;
  end else if (tpos_on_if) begin
    if (state == `behind) begin
      state = `same;
    end else if (state == `same) begin
      state = `ahead;
    end
  end else if (tpos_on_lo) begin
    if (state == `ahead) begin
      state = `same;
    end else if (state == `same) begin
      state = `behind;
    end
  end

  if (tpos_on_if || tpos_on_lo) begin
    if (state == `ahead) begin
      sigout_inc_val = vlogic_high;
      sigout_dec_val = vlogic_low;
    end else if (state == `same) begin
      sigout_inc_val = vlogic_low;
      sigout_dec_val = vlogic_low;
    end else if (state == `behind) begin
      sigout_inc_val = vlogic_low;
      sigout_dec_val = vlogic_high;
    end
  end

  V(sigout_inc) <+ transition(sigout_inc_val, tdel, trise, tfall);
  V(sigout_dec) <+ transition(sigout_dec_val, tdel, trise, tfall);
end
endmodule
```

Differential Charge-pump

Appendix A

```
`include "discipline.h"
`include "constants.h"

module diff_charge_pump(siginc, sigdec, vout_p, vout_n, vsrc);
input siginc, sigdec;
inout vout_p, vout_n, vsrc;
electrical siginc, sigdec, vout_p, vout_n, vsrc;
parameter real iamp=0.5m from [0:inf];
parameter real vtrans = 0;
parameter real tdel=0 from [0:inf];
parameter real trise=1n from (0:inf);
parameter real tfall=1n from (0:inf);

real iout_val;
analog function real i_mult;
input inc;
input dec;
input vtrans;
real inc;
real dec;
real vtrans;

integer inc_high;
integer dec_high;

begin
inc_high = inc > vtrans;
dec_high = dec > vtrans;
i_mult = 0.0;
if (inc_high == dec_high) begin
i_mult = 0.0;
end else if (inc_high) begin
i_mult = 1.0;
end else if (dec_high) begin
i_mult = -1.0;
end
end
endfunction

analog begin
@ ( initial_step ) begin
iout_val = iamp*i_mult(V(siginc), V(sigdec), vtrans);
end

@ (cross(V(siginc) - vtrans, 0)) begin
iout_val = iamp*i_mult(V(siginc), V(sigdec), vtrans);
end
@ (cross(V(sigdec) - vtrans, 0)) begin
iout_val = iamp*i_mult(V(siginc), V(sigdec), vtrans);
end

I(vsrc, vout_p) <+ transition(iout_val, tdel, trise, tfall);
I(vsrc, vout_n) <+ (-1)*transition(iout_val, tdel, trise, tfall);
end
endmodule
```

Appendix B

% Main PLL calculation script

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% lowpass filter transfer function: Kvco/s
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
clear;
fstart=10e3;   % starting at 10kHz
fstep=10e3;    % freq step is 10kHz
fstop=10e6;    % stop freq is 10MHz

f=fstart:fstep:fstop; % generate frequency vector
w=2*pi*f;
w_high=2*pi*fstop;
w_low=2*pi*fstart;

R = 1E+3;
C1 = 447E-12;
C2 = 44.8E-12
%LPF = my_lpf (R2,R3,C1,C2,C3, w)
LPF = my_2nd_order_lpf (R, C1, C2, w)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% VCO transfer function: Kvco/s
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Kvco= 555e+6;
VCO = my_vco (Kvco, w);

% =====
% Divider
% =====
N = 60;
Cdiv = 1 / N;

% =====
% PFD/CP gain: Kpfd=1/2pi
% =====
lcp = 0.5E-3;
Kpfd = lcp/(2*pi)

% =====
% Forward Loop Gain
% =====

FG = Kpfd.*LPF.*VCO;
% figure (1)
% semilogx(f,20*log10(abs(FG)));
% grid on;
% title('Forward Gain transfer function plot');
% xlabel ('Frequency (Hz)')
% ylabel ('FG(s) dB')
% grid on;
% AXIS fill
% bode (FG, {w_low, w_high})

% =====
% Closed Loop T
% =====
% Loop gain = Forward gain/N
LG = FG*Cdiv
% figure (1)
% bode (LG, {w_start, w_stop})
```

```
% margin(LG)
% title('Loop Gain transfer function, check stability');
% xlabel('Frequency (Hz)')
% ylabel('H(s) dB')
% grid on;

% System transfer function =F.G/1+L.G
sys_tf = FG./(1+LG);
%sys_tf = FG/(1+LG)
%figure(2)
%bode(sys_tf, {w_start, w_stop})
%grid on;
semilogx(f,20*log10(abs(sys_tf)));
% grid on;
title('System Transfer Function Plot, from Vin to Vout');
xlabel('Frequency (Hz)')
ylabel('Transfer function H(s) dB')
grid on;
% AXIS fill

function [VCO] = my_vco(Kvco, w)
%hold off

% =====
% VCO Circuit Kvco*2pi/s
% =====

% Kvco needs time 2pi because s=2*pi*f
% num_VCO= 2*pi*Kvco;
% den_VCO= [1 0];
% vco=tf(num_VCO, den_VCO);
% vco=zpk(vco)
% figure(2)
% bode(vco, {w_low, w_high})
% grid on;
% [Gm,Pm,Wcg,Wcp]=margin(vco)
VCO = (2*pi*Kvco)/(j*w);

function [LPF] = my_2nd_order_lpf(R,C1,C2,w)
%hold off

% =====
% Loop Filter Circuit
% =====
% I(s)
% -----
%      |      |      +
%      |      |      |
%      <      |      |
%      >      |      |
%      R <      ----- C2
%      >      |      |
%      <      |      |
%      >      |      |
%      |      |      |
%      |      |      |
%      |      |      |
%      C1 ----- |
%      ----- |
%      |      |      8
%      |      |      -
% -----
```

Appendix B

```
% Third Order Loop Filter
% =====

% =====
% branch1: R2 in series with C2, (1)tf method (2) array method
% =====
% (1) tf method
% num_branch1 = [R2*C2 1];
% den_branch1 = [C2 0];
% branch1 = tf(num_branch1, den_branch1);

% (2) Array method
br1 = R + 1./(j*w*C1);
br2 = 1./(j*w*C2);

% =====
% LPF transfer function
% =====

% LPF=(1/(1/branch1+1/branch2+1/branch3))*vdiv
% %Zero, Pole, K model
% lpf=zpk(LPF)
LPF=1./((1./br1)+(1./br2));
```


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