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**LA THÈSE A ÉTÉ
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FEASIBILITY STUDY OF A CCD LINEAR
IMAGE PROCESSOR

by

Richard A. Bourassa, B. Eng.

A thesis submitted to the Faculty of Graduate
Studies and Research in partial fulfillment
of the requirements for the degree of

Master of Engineering

Department of Electronics
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Ottawa, Canada
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August, 1979

ABSTRACT

The feasibility of a novel approach in image processing, based on modulating the integration time of a CCD linear image sensor, is studied in this thesis. By combining the optical properties of CCD photoelements with the electrical properties of CCD shift registers, it is possible to design a general purpose image processor. The fundamental mechanism of discrete summations, basic to most image processing algorithms, lends itself to an easy implementation in CCD imagers, using their inherent shift-and-add capability. Coefficients required for a specific processing algorithm modulate the photoelements integration time by controlling the CCD driving clock waveforms.

Experimental results indicate that the integration time modulation approach in CCD image processing is feasible. It is verified by successful implementation of image processing algorithms such as edge detection, convolution and Discrete Fourier Transform. Practical applications are numerous in both military and industrial environments.

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TABLE CONTENTS

	<u>PAGE</u>
CHAPTER 1. INTRODUCTION	1
1.1 Introduction	1
1.2 Related works	1
1.3 Thesis objectives	2
1.4 Thesis format	3
CHAPTER 2. REVIEW OF THE OPTO-ELECTRICAL PROPERTIES OF A LINEAR CCD IMAGE SENSOR	4
2.1 Introduction	4
2.2 Operation of a CCD imager	4
2.3 Operating parameters and limitations of a CCD imager	6
2.3.1 Photogeneration process	6
2.3.2 Transmittance of light	8
2.3.3 Transfer inefficiency	8
2.3.4 Dark current	9
2.3.5 Noise	11
2.4 Inherent processing capability of a CCD imager	12
CHAPTER 3. DESIGN OF A CCD IMAGE PROCESSOR	20
3.1 Introduction	20
3.2 General description	20
3.3 Imaging section -- Description of device	22
3.4 Control circuitry	25
3.4.1 Discussion on CCD clocks	25
3.4.2 Implementation	33
3.5 Postprocessing circuitry	43
3.5.1 Analog circuit	43
3.5.2 Digital data collection system	45
CHAPTER 4. EXPERIMENTAL RESULTS	49
4.1 Introduction	49
4.2 Preliminary experiments	49
4.3 Some limitations of the CCD image processor	61
4.3.1 Noise sources and transfer inefficiencies	61
4.3.2 Distortion effect	63
4.4 Experiments	66
4.4.1 Fluid level indicator	69
4.4.2 Bar code reader	72
4.4.3 Frequency analysis of an image	74

	<u>PAGE</u>
CHAPTER 5. CONCLUSIONS	87
5.1 Summary and conclusions	87
5.2 Suggestions for future work	88
REFERENCES	91
APPENDIX A CIRCUIT DIAGRAM OF THE CCD IMAGE PROCESSER	93
APPENDIX B CCD 110F SPECIFICATION SHEETS	96
APPENDIX C INTEL PROMPT 48 SPECIFICATION SHEETS	102
APPENDIX D EXAMPLES OF TAP WEIGHT GENERATION PROGRAM	110
APPENDIX E DATA COLLECTION SYSTEM SOFTWARE CONTROL	117
APPENDIX F DFT COEFFICIENTS CALCULATION	122
APPENDIX G COMPUTATION OF A COSINE TRANSFORM ON SIGMA-9 COMPUTER	124
APPENDIX H COMPUTATION OF INVERSE DFT ON SIGMA-9 COMPUTER	126

LIST OF FIGURES

<u>FIGURE NO.</u>		<u>PAGE</u>
2.1 a,b	Schematic of CCD in imaging and processing modes of operation	15
2.2	Operation of the CCD image processor	17
3.1	Block diagram of image processor	21
3.2	Block diagram of CCD 110F	24
3.3	Typical test patterns for preliminary experiments	26
3.4	Optical set-up	27
3.5	Timing sequence of CCD clock waveforms for the camera mode of operation	31
3.6	Timing sequence for image processing applications	34
3.7	Block diagram of the control circuit	35
3.8	Clock cycle generation example	38
3.9	Interface circuit (TTL to MOS levels) for clocks ϕ_1 and ϕ_2	41
3.10	Picture of ϕ_1 and ϕ_2	42
3.11	Circuit diagram of analog output recovery circuit	49
3.12	Block diagram of data collection system	46
4.1	Camera mode example	50
4.2 a,b,c	Convolution of two rectangles	53,54
4.3	Convolution example	55
4.4	Convolution example	56
4.5	A possible set of coefficients for edge detection	58
4.6 a,b	Edge detection: tap weight pattern and results	59
4.7	Edge detection of a rectangle with different tap weight patterns	60
4.8	Convolution of two rectangles: inputs	64

<u>FIGURE NO.</u>		<u>PAGE</u>
4.9	Convolution of two rectangles: theoretical and experimental outputs	65
4.10	Output correction methods for the CCD 110F	67
4.11	Output signal of a convolution	68
4.12	Fluid level indicator	71
4.13	Experimental one: DFT of a single rectangle image Image	78
4.14	Experiment one: DFT of a single rectangle image Computer simulation results	79
4.15	Experiment one: DFT of a single rectangle image Experimental results	80
4.16	Experiment two: DFT of two rectangles Image	82
4.17	Experiment two: DFT of two rectangles Computer simulation results	83
4.18	Experiment two: DFT of two rectangles Experimental results	84

LIST OF TABLES

<u>TABLE NO.</u>		<u>PAGE</u>
3.1	CCD 110F driving clock waveforms	29
3.2	CCD 110F voltage supplies	30
4.1	Experiment one: DFT of a single rectangle image. Comparison of a computer simulation and experimental results	81
4.2	Experiment two: DFT of two rectangles Comparison of computer simulation and experimental results	85

LIST OF SYMBOLS AND ABBREVIATIONS

a_j	: Incident photon flux of photoelement j
b	: Number of bits
BCCD	: Buried channel charge coupled device
c	: Speed of light
CCD	: Charge coupled device
C_{eff}	: Effective storage capacitance per unit area of a potential well
$\cos$	: Cosine
CPU	: Central processing unit
CRT	: Cathode ray tube
CZT	: Chirp-Z-Transform
dB	: Decibel
DFT	: Discrete Fourier Transform
DMA	: Direct memory access
E_g	: Energy gap between the states that contribute to thermal generation and conduction band
FFT	: Fast Fourier Transform
Fig.	: Figure
FIR	: Finite Impulse Response
FPN	: Fixed pattern noise
FZ	: Fat zero
$f(t), g(t)$	: Continuous time fonction
$f(k), g(k), x(m)$	: Discrete time fonction
h	: Planck's constant
HEX	: Hexadecimal

I_o	: Incident light intensity
I/o	: Input/output
J_d	: Dark current density
k	: Boltzmann's constant
kHz	: Kiloherzt
°K	: Kelvin degrees
L	: Thickness of the semiconductor
LED	: Light emitting diode
L_n	: Diffusion length
Log ₁₀	: Base 10 logarithm
MHz	: Megahertz
MOS	: Metal oxide semiconductor
msec.	: Millisecond
N	: Total number of effective photoelements Total number of image samples Total number of frequency components
N_A	: Substrate doping density
P_n	: Charge packet amplitude after n transfers
P_o	: Initial charge packet amplitude
q	: Electronic charge
$Q_s(t)$	: Charge density
RAM	: Random access memory
SCCD	: Surface channel charge coupled device
S_1	: Silicon
S_1O_2	: Silicon dioxide
SNR	: Signal-to-noise ratio

SZ : Slim zero

t : Time

T : Temperature in °K

T_i : Integration time of clock cycle i

T_s : Storage time of a CCD

TTL : Transistor-transistor logic

UPI : Universal Product Code

v : Volts

V_i : Output voltage corresponding to photoelement i

w : Watts
Depletion layer width

$y(n), Y(n)$: Frequency components

1-D : One-dimensional

2-D : Two-dimensional

α : Absorption coefficient in silicon

ΔV : Voltage difference

ϵ : Transfer inefficiency

ϵ_s : Dielectric constant of the silicon

λ : Wavelength of light

μsec : Microsecond

π : 3.1416

σ_e^2 : Probability distribution variance of quantization

$\tau(\lambda)$: Transmittance through the gate electrode structure of a CCD imaging cell

ϕ_p : Photosite control clock waveform (theoretical)

ϕ_R : Reset clock waveform

ϕ_s : Sampling clock waveform

$\phi_{XA}, \phi_{XB}, \phi_T$: Transfer gate clock waveform

$\phi_{1A}, \phi_{1B}, \phi_1$,

$\phi_{2A}, \phi_{2B}, \phi_2$: Shift register clock waveform

CHAPTER 1

INTRODUCTION

1.1 Introduction

Charge coupled devices (CCD's) have been used successfully to store and delay electrical signal samples in both digital and analog forms. A properly designed CCD can also be used to convert an optical image into an electrical signal. By combining these two properties of the CCD, an image processor may be designed to perform various processing operations on the image, providing a cost-effective alternative to other digital image processors. Based on a CCD linear imager, a simplified version of the image processor has been constructed and characterized to demonstrate the feasibility of such an approach.

1.2 Related works

Charge coupled devices, since their invention by Boyle and Smith [1] in 1969, have been applied to many areas of technology: image sensing, signal processing and data storage. Their advantages and limitations are well understood [2,3,4].

An electro-optical signal processing system using an image sensing CCD as the central element had been reported to implement convolvers [5], Finite Impulse Response (FIR) transversal filters [6,7,8], etc. In this approach, an analog signal is used to modulate a Light Emitting Diode (LED) that illuminates the charge coupled device. The amount of light which is allowed to reach a given CCD storage potential well is controlled by a photographic mask placed between the CCD and the LED. The mask embodies tap weights defining the filter used in the application.

Image processing can be done using a similar approach. The

input signal (image) is focussed onto a CCD image sensor and tap weights defining the type of processing to be done are either fed to the LED [6,7,8] or to the device itself. The former approach has been proven successful but has some inherent disadvantages: the image (e.g., photographic negative) has to be placed between the CCD and a light source and continuous control of the light source is required, which is only suitable for photographic negative processing.

The use of tap weights to modulate the CCD driving clock pulse period that controls the charge gathering capability of the device under fixed illumination is the alternate image processing approach utilized in this thesis. Clock waveforms which are needed to operate the CCD are generated by hardware circuitry according to a set of predefined tap weights. A microprocessor is programmed to generate the required tap weights for various signal processing applications. Versatility is the main advantage of this approach: the system can be used to process any properly focussed image as well as photographic negatives.

1.3 Thesis objectives

The first objective of this thesis is to demonstrate the feasibility of a CCD linear image processor using integration time modulation. Experimental results reported in this study are positive. Various experiments in one-dimensional image processing applications are also reported; they include a fluid level indicator, a bar code reader and a data transformer. The applicability of this image processor is limited not so much by the CCD's inherent limitations but rather by the optical system used to focus the image onto the device. Further work can be done in that area to improve overall performance. Extension of this image processing approach for two-dimensional images is expected to find many applications.

1.4 Thesis format

Chapter 2 consists of two theoretical parts: (1) a summary of the main physical properties of CCD's and their limitations, and (2) a brief review of how signal processing can be done using a CCD imager. Chapter 3 is a description of the system designed for doing image processing. Guidelines such as versatility in the type of processing to be done were considered. In chapter 4, experimental results are reported. They include preliminary experiments, measurements of important limitations discussed in chapter 2, and some applications. Finally, the conclusions and recommendations for future work are presented in chapter 5.

CHAPTER 2

REVIEW OF THE OPTO-ELECTRICAL PROPERTIES OF A LINEAR CCD IMAGE SENSOR

2.1 Introduction

The central element in the proposed image processing system is a CCD image sensor. It is important to appreciate the operation and limitations of the image sensor in light of the proposed image processing system. In this chapter a brief description of the various parameters that govern the operation of a CCD imager is included. Also discussed are some fundamental signal processing concepts that are relevant to the proposed system. Discussions here are made in the context of a Fairchild CCD 110F imager*, however the system is not restrictive to any particular CCD architecture.

2.2 Operation of a CCD imager

In a charge coupled device linear image sensor, light photons representing an image are absorbed by the photoelements and charges are created by hole-electron pair production. Minority charge carriers (electrons for n-channel devices) are collected under photogates and form charge packets. After a prescribed time of light integration, charge packets are gated onto the analog shift registers, which are located on both sides of the imaging array, to be serially shifted to the output circuit. The CCD essentially handles the information in the form of charge packets using a series of closely spaced metal-oxide-semiconductor (MOS) capacitors for its shift registers.

* Fairchild Semiconductor Components Group, 464 Ellis Street, Mountain View, Ca. 94042

Charge generation is controlled by the incident light intensity and the integration time or time during which photoelements are exposed to light. To estimate the total photogenerated charge over a given integration time, a convenient approach is to solve the one-dimensional steady state continuity equation separately for the depletion and neutral regions in the semiconductor substrate. By applying the proper boundary conditions, the charge density Q_s was found to be given by the expression: [9]

$$Q_s(t) = \frac{q I_0 \tau(\lambda) t \lambda}{hc} \left\{ (1 - e^{-\alpha w}) + \frac{\alpha L_n^2}{(\alpha^2 L_n^2 - 1)} \left[\alpha e^{-\alpha w} + \frac{e^{-\alpha L} e^{-\alpha w} \cosh\left(\frac{L-w}{L_n}\right)}{L_n \sinh\left(\frac{L-w}{L_n}\right)} \right] \right\} \quad (2.1)$$

where:

w : depletion layer width

t : integration time (in seconds)

I_0 : incident light intensity at the silicon surface (watt/cm²)

$\tau(\lambda)$: transmittance through the gate electrode structure of a CCD imaging cell

λ : wavelength of light (cm)

q : electronic charge: 1.6×10^{-19} C

h : Planck's constant: 6.6×10^{-34} J·sec

c : velocity of light: 3×10^{10} cm/sec

α : wavelength dependent absorption coefficient in silicon (cm⁻¹)

L : thickness of the semiconductor (cm)

L_n : diffusion length

Equation (2.1) can be simplified by assuming that the substrate thickness is large and is greater than the diffusion length. This

assumption may be good in devices where $L > 200$ microns and L_n lies between 50 and 125 microns for doping densities in the range of 1 to 4 Ωcm . The simplified expression is: [9]

$$Q_s(t) = \frac{qI_o \tau(\lambda) t \lambda}{hc} \left[1 - e^{-\alpha w} + \frac{\alpha L_n}{\alpha L_n + 1} e^{-\alpha w} \right] \quad (2.2)$$

2.3 Operating parameters and limitations of a CCD imager

A CCD image sensor has inherent limitations in the photon to charge conversion process, charge transport process and the final charge to voltage conversion process. Some of these limitations, like the various noise sources and dark current, limit the dynamic range of a CCD imager and therefore will have identical effects on the performance of the image processor. Other limitations, like the variation of light transmittance along the photoelements and transfer inefficiency, cause degradation of the quality of the image reproduced by a CCD imager. In terms of image processing, this means that an image slightly different from the one focussed onto the device will be processed by the CCD image processor. The above limitations arise from technology limitations of a charge coupled device and have been treated extensively in the literature [2,10,11,12]. Following is a brief description of the few important parameters that affect the operation of a CCD imager used as an image processor.

2.3.1 Photogeneration process

Referring to equation (2.2), it is noticed that the nonlinearity arising in the relationship between charge density and the incident light intensity is through the dependence of Q_s on the depletion layer width,

which changes with the surface potential ϕ_s : [9]

$$w = \sqrt{\frac{2\epsilon_s}{qN_A} \phi_s} \quad (2.3)$$

where:

ϵ_s : dielectric constant of the silicon (Farad/cm)

N_A : substrate doping density (cm^{-3})

The dependence of Q_s on w is generally weak so that the relation between the photogenerated charge density and the product $I_0 \cdot t$ is almost linear. However, there is still a small image distortion introduced in the photogeneration process because of this non-linear relationship.

Another limiting factor related to the photogeneration process is the blooming of image. Blooming is an apparent increase in the size of an image of a bright object under overload conditions. In the CCD, excess carriers from a localized overloaded photoelement can either diffuse through the bulk to neighbouring potential wells, or diffuse into the transfer channels of the read out CCD shift registers, producing an enlarged image in the display. Blooming can be suppressed by the use of overflow drains or potential barriers for the storage wells [2].

As said previously, the photogeneration process is essentially a transformation of an optical image into a set of charge packets that contain most of the information about the image. The minimum feature size of an image that can be transformed, and later recovered, is limited by the spatial resolution of the CCD. Spatial resolution is determined by the element-to-element spacing of photoelements.

2.3.2 Transmittance of light

For a front side illuminated device, incoming light photons have to pass through three layers of material before reaching the single crystal silicon surface of the photoelement. These layers usually consist of one of silicon dioxide for scratch protection and surface passivation, one of polysilicon for the conductive gate structure and one of silicon dioxide for gate insulation. They have different indices of refraction. The interface between each layer gives rise to multiple reflections, causing wavelength dependent interferences. These interferences affect the photogeneration process, as seen from equation (2.2), through a complex relationship between λ , $\alpha(\lambda)$ and Q_s . Peaks and valleys in the transmission spectrum were observed and reported in the literature [2,9]. According to manufacturer's specifications [16], the transmittance of the CCD 110F across the visible spectrum is satisfactory for the purpose of this thesis.

Transmittance of light is also affected by the absorption in the polysilicon gate layer. Transparent gate electrode materials with high conductance, such as tin oxide, were reported to produce better spectral response than polysilicon [13].

2.3.3 Transfer inefficiency

Incomplete charge transfer in a CCD serial shift register can result in an overall degradation of the signal. Extensive studies in this field have been undertaken for both surface channel CCD's (SCCD's) [3] and buried channel CCD's (BCCD's) [14,15].

The transfer loss or transfer inefficiency ϵ is expressed in terms of the charge fraction not transferred in a single shift operation and is a fixed value for a given CCD. Values of $\epsilon < 1 \times 10^{-5}$ may be

obtained for BCCD's [10,16]. The total number of shifts, n , that can be made on a charge packet depends on ϵ . If P_0 is the initial charge packet amplitude, its new value after n transfers is given by: [4,17]

$$P_n = P_0 (1 - \epsilon)^n \quad (2.4a)$$

$$\approx P_0 (1 - n\epsilon) \text{ for small } \epsilon \text{ and } n\epsilon \ll 1 \quad (2.4b)$$

When clocked appropriately, the dominant transfer loss mechanism is from trapping of carriers in energy states in the band gap region of the semiconductor. By comparison, trapping at Si-SiO₂ interface is more pronounced than in bulk semiconductor. As a result, the surface channel device suffers a higher transfer inefficiency than its buried channel counterpart because interface states do not interfere directly with signal charges travelling in a channel buried in the semiconductor substrate.

In SCCD's, propagation of a constant background charge level through the device can serve to keep most of these trapping states occupied, hence increasing the transfer efficiency at the expense of lower charge handling capability. This constant signal or "fat zero" (FZ) is of the order of 10-25% of a full potential well [3,15,17]. Propagation of a small bias or "slim zero" (SZ) of the order of 1% of a full well can almost eliminate the bulk trapping effect in BCCD's [2,3].

In general, if the CCD imager is operated properly, transfer inefficiency may be kept to a reasonably low level. When the device is used in an image processing configuration, additional limitations due to transfer inefficiency may affect the overall system performance. They will be discussed in section 2.4.

2.3.4 Dark current

Dark current or thermal charge generation [3] is not spatially

uniform across the device because of many factors: defects in the silicon substrate and the Si-SiO₂ interface, non-uniform impurity distribution, etc. A "fixed pattern noise" (FPN) is observed at the output when the CCD is operated in the dark without an input image. Charge packets clocked out are mainly due to dark current and form a fixed pattern corresponding to the physical location of the localized dark current sources. Although the average dark current level is usually quite low for most charge coupled devices, high localized dark current levels or dark level non-uniformities are often high enough to affect the dynamic range of the device.

Thermal generation at the Si-SiO₂ interface, thermal generation in the depletion region and thermal generation in the neutral bulk within a diffusion length of the depletion region are the three major sources of dark current. The increase of dark current with integration time limits the storage time T_s of the device, which is defined as being the time required for the dark current charge to fill a potential well and which is given by: [14]

$$T_s \approx \frac{C_{eff} \Delta V}{J_d} \quad (2.5)$$

where:

C_{eff} : effective storage capacitance per unit area of the well

J_d : dark current density

ΔV : height of the barrier isolating the storage wells.

T_s typically lies between 0.1 and 10 seconds. It is an important limitation in CCD memories but not so much in most imagers where charges are integrated and clocked out at a relatively fast rate.

Dark current is also strongly dependent on temperature as seen from relation (2.6): [14]

$$J_d \propto \exp(-E_g/2kT) \quad (2.6)$$

where:

E_g : energy gap between the states that contribute to thermal generation and conduction band

k : Boltzmann's constant = 1.38×10^{-23} J/°K

T : temperature in °K

Cooling the device will greatly reduce the average dark current level but dark current level non-uniformity still remains an important limiting factor.

2.3.5 Noise

Noise sources are an important limitation in low light level applications. Like dark current level non-uniformity, they limit the dynamic range of the charge coupled device. A BCCD imager has many sources of noise among which are photon induced shot noise, background charge generation noise, transfer noise, reset noise and noise due to charge trapping states. Following is a brief description of these main noise sources. A more elaborate discussion can be found in [2].

In general, the emission of photons from any source is a random, stochastic, Poisson distributed process [14]. Consequently, the number of photons collected in a potential well in time t is therefore a random variable, and its standard deviation is the photon shot noise. It is equal to the square root of the average number of carriers in a charge packet and therefore becomes an important noise source for high level signal charge.

Dark current noise is essentially a fluctuation in the average amount of thermally generated charges. It is a very small noise source

considering the fact that the average dark current level itself is usually very low. Transfer noise, being a fluctuation in the amount of carriers left behind after each transfer, is very low in BCCD's. Noise associated with trapping effects is a fluctuation in the number of charges trapped and released by the charge trapping states and is frequency dependent. The few discrete energy levels containing trapping states in the substrate give rise to specific discrete re-emission time constants. Trapping noise then depends on the relation between these time constants and the time between successive transfers in the CCD shift registers. It is maximum for transfer times equal to the re-emission time constants most encountered in bulk trapping states but, because it involves a limited number of charges, it remains quite a small noise source as compared to other ones like photon induced shot noise.

Reset noise is mainly thermal noise of the MOS channel between the reset amplifier drain and the diffusion region and can be classified as being an RC type noise between the channel resistance and the diffusion region capacitance. Double correlated sampling at the output can minimize it [2,12,14]. Some CCD's, like the one used in this work, use a technique similar to double correlated sampling. Two diffusion regions are cyclically preset to a reference potential and charges coming out of the analog shift registers are sent to one of them. Each diffusion region is connected to a MOS amplifier gate so that one output voltage is at reference level and the other one is at reference plus signal level. Subtracting the two outputs will suppress reset noise, which appears as common mode signal to both diffusions.

2.4 Inherent processing capability of a CCD imager

What have been described so far are the basic operation of a

CCD imager and some of its important limitations. A CCD imager has another inherent capability not yet discussed: it can provide linear processing of an image without any modification of the existing internal structure.

Fundamental to signal processing theory, for time varying signals, is the action of convolution in which two signals are multiplied in a specific order and yield a unique output. Equation (2.7) describes the convolution of two functions $f_1(t)$ and $f_2(t)$.

$$g(t) = \int_{-\infty}^{\infty} f_1(t-\alpha) f_2(\alpha) d\alpha \quad (2.7)$$

For discrete time varying functions, one of them can be replaced by a series of coefficients or tap weights, i.e. a "fixed" function, and the other one allowed to vary, i.e. a time sampled continuous function. For a causal case (the convolution product is zero for negative times) and a limited sequence, equation (2.7) can be replaced in the discrete case by:

$$g(n) = \sum_{k=1}^N f_1(k) f_2(n-k) \quad (2.8)$$

where N is the number of samples taken.

These equations apply to time varying signals. However, the CCD linear image processor utilized in this thesis was built to look at and process steady images or at least slow moving ones. Therefore, images to be processed are not time dependent. CCD imagers, however, inherently transform space varying images in time varying electrical signals that reflect the spatial content of the image. To analyse or process an image with the CCD linear image processor, time domain convolution functions can therefore be used on the time dependent counterpart of the image. The

same applies to other functions defined in the time domain and to time to frequency transform functions. The spatial frequency content of a steady image can therefore be obtained using Discrete Fourier Transform algorithms on the time varying representation of the image in the CCD.

Thus, the fundamental mechanism of discrete convolution whereby samples are multiplied two by two and added to other products to yield a single output, basic to signal processing theory, can be successfully implemented in a CCD imager using its inherent shift-and-add capability. The optical input signal is easily convolved with a series of coefficients that control the charge gathering process of the CCD photoelements by controlling the incident light or, in this case, the integration time.

The image, illuminated by a constant light source, is divided in 256 parts when it reaches the 256 photosites and becomes a sampled analog function. Accumulated charges are then transferred in analog shift registers to be eventually clocked out using one of the two possible modes of operation: camera mode or processing mode. In the former one, charges in the shift registers are all clocked out before other charges can be transferred from the photosites to the shift registers. CCD clocks are controlled by a set of identical tap weights defining a unique integration time for all photosites. The image is reproduced at the output without any change or distortion. This is the usual mode of operation of a CCD imager (Fig. 2.1a).

In the processing mode (Fig. 2.1b), charges in the shift register are shifted one stage and then added to other charges coming from photosites. This inherent shift-and-add process lends itself to an easy implementation of discrete convolution and other signal processing schemes. For any processing application, CCD driving clock waveforms are modulated by a

Fig. 2.1a Schematic of CCD in camera mode operation. In the camera mode, charges are integrated once (according to tap weight x_i) and transferred from photosites a_j 's into delay elements D_j 's. They are all clocked out before other charge packets are dumped into delay elements via the closing of switches S_1 to S_{128} every 128th clock cycle.

Fig. 2.1b Schematic diagram of CCD in processing mode of operation. In the processing mode, a shift-and-add process takes place in shift registers. At each delay element D_j , a new charge packet $a_j x_i$ is added to what was previously there.

set of weights related to the processing function. This process is illustrated by the model of Fig. 2.2. For simplicity, only four CCD delay elements are considered. a_1 , a_2 , a_3 , and a_4 represent the total incident photon flux of photoelements 1, 2, 3 and 4 respectively. T_i is the integration time of clock cycle i and is determined by tap weight x_i . The total number of charge carriers generated in photoelement j during clock cycle i is proportional to $a_j T_i$, the product of the total incident photon flux and of the integration time. Without loss of generality, a unity generation rate and a 100% photon-charge carrier conversion efficiency are assumed. The product $a_j T_i$ now represents the total number of photo-generated charges collected by the photoelement during the time interval T_i .

After charge packet $a_j T_i$ has been formed, it is transferred to delay element j and then shifted right to delay element $j + 1$ during clock cycle $i + 1$. During this same clock cycle, other charges are generated in photoelement $j + 1$ and later on transferred to delay element $j + 1$ and added to charges previously there. The total charge in delay element $j + 1$ after clock cycle $i + 1$ is thus $a_j T_i + a_{j+1} T_{i+1}$. It is shifted right again to delay element $j + 2$ and the process goes on until total charge packets are shifted out of the registers. For example, the output at the fifth clock cycle in Fig. 2.2 is:

$$y(5) = a_4 T_4 + a_3 T_3 + a_2 T_2 + a_1 T_1 \quad (2.9)$$

The CCD is assumed to have ideal characteristics in this discussion. In practice, when dark current, noise and transfer inefficiency are being considered, the effective dynamic range of the device is reduced. Tap weights can however be modified to compensate some of these effects [12].

Fig. 2.2. Operation of the CCD image processor. The inherent shift-and-add process of the CCD imager lends itself to an easy implementation of signal processing techniques using charge coupled devices. The shift-and-add process is illustrated by two sets of arrows. The vertical ones show the transfer of charge packets from photoelements to delay elements and the implied summation in the delay elements with the previous contents. The oblique arrows show the shifting occurring in the shift registers at each clock cycle.

Device limitations are not the only ones to affect the processing capability of the system. Some errors in the coefficients of the desired transformation are introduced by quantization of the coefficients in a limited number of digital bits (b). In the present system, coefficient quantization in $b = 8$ digital bits provides a quantization step size of 2^{-8} . The coefficients are all rounded off to the integral multiple of the above step size, i.e. they take any of 256 possible values. The errors introduced by this process lie within $\pm$ one-half of the least significant bit, or ± 0.4 microseconds in integration times, corresponding to a highest clock frequency of 1.2 MHz. The probability distribution of this error has a variance of: [20]

$$\sigma_e^2 = \frac{2^{-2b}}{12} \quad (2.10)$$

and a signal-to-noise ratio can be defined as: [20]

$$\text{SNR} = 10 \log_{10}(R/\sigma_e^2) \quad (2.11)$$

where

$$R = \frac{\left(\sum_{n=1}^N a_n \right)^2}{\sum_{n=1}^N (a_n)^2} \quad (2.12)$$

and $\{a_n\}$ represents the image samples. It is real and positive for all values of n . For more than one non-zero image sample in $\{a_n\}$, R varies from a minimum of 1 to a maximum of N and the SNR has a minimum value of $1/\sigma_e^2$ or, more specifically: [20]

$$\text{SNR} \geq (6.02b + 10.79) \text{ dB} \quad (2.13)$$

The SNR thus increases by 6 dB for each bit added in the quantization process and, when using 8 bit coefficients, is equal or better than 59 dB. Thus, the commercially available 8 bit word memory systems or microprocessors provide adequate SNR for most processing applications.

Another small error source associated with the coefficients is the finite fall and rise times of the clock waveform pulses. Typical rise and fall times measured at 1.2 MHz clock frequency give 40 and 10 nanoseconds, respectively. These transition times are very small when compared to the coefficient defined integration time cycles (minimum of 1.7 microseconds) and therefore have little effect on the processor's performance.

In general, most signal processing algorithms require both positive and negative tap weight coefficients lying between +1 and -1. The negative coefficients are handled by scaling and the application of an offset so that, prior to quantization, all coefficients lie between +1 and 0. As such, the conversion also reduces the output dynamic range by 6 dB. The fixed offset so generated can finally be removed at the output of the CCD.

CHAPTER 3

DESIGN OF A CCD IMAGE PROCESSOR

3.1 Introduction

A CCD image processor using the integration time modulation technique has been built to demonstrate the feasibility of this new approach in image processing. Integration time modulation is particularly suited for image processing but it imposes special design considerations on the system. Other considerations come from the fact that the experimental CCD image processor should be able to perform various types of signal processing on the image and that some of the system parameters, like the clock waveforms, should be easily modifiable for testing purposes.

This chapter describes the actual design of a CCD image processor using integration time modulation.

3.2 General description

The image processor is made of three main sections: 1) a control circuit generating the various clock waveforms needed to operate the CCD; 2) an imaging section including a CCD imager and its associated optics; 3) a postprocessing section to provide analog and digital outputs.

The processor block diagram is shown in Fig. 3.1. As discussed in chapter 2, digital coefficients or tap weights are needed to perform any kind of processing on a signal. One complete set, defining one processing application, is stored in a Random Access Memory (RAM) and coefficients are sequentially sent to a clock generation circuit. These 8-bit coefficients thus control the imager integration time by controlling the CCD clock waveforms.

Most CCD linear image sensors would be suitable to demonstrate

Fig. 3.1. Block diagram of image processor.

the feasibility of a clock controlled CCD linear image processor. However, charge coupled devices vary widely in their internal structure, e.g., 2-phase versus 3-phase electrode structure, so that many types of CCD's require particular sets of clock waveforms and are not directly interchangeable. For convenience, it was then decided to use the same device, a Fairchild's CCD 110F linear image sensor, for all experiments and to build a clock generation circuit suited to this device.

The CCD is the central element of the image processor. Its 256 separate photoelements transform the incoming optical signal into charge packets that are shifted and added according to the device clock waveforms. Image processing is thus done in the device by controlling the charge gathering process via charge integration time modulation. Image sensing capability of the photoelements and shift-and-add capability of the shift registers are the main features that, when combined, permit images to be processed in the device.

Digital and analog postprocessing circuitry are included in the system for further processing of the time dependent representation of the image. A sample-and-hold circuit first samples the CCD output signal during valid time intervals and holds the data for a complete clock cycle. More analog circuitry may be used for further processing, e.g., amplification, filtering, peak detection. Digital circuitry is also provided to convert the output samples into digital (8-bit) words for storage, further processing or interfacing with digital computer systems.

3.3 Imaging section - Description of device

The choice of a unique imaging device for all experiments simplifies the design of the image processing system, especially the clock generation circuit. The CCD 110F is first described in this section along

with the control clock requirements and the optical arrangement. The support circuitry, for clock generation and output recovery, will be described in subsequent sections.

The Fairchild CCD 110F linear image sensor can be divided into four main parts: 256 image sensing elements, two transfer gates, two analog shift registers and an output unit [16]. A block diagram of the device is given in Fig. 3.2. The sensor elements, numbered a_1 to a_{256} in the figure, are covered by a polysilicon photogate (about 3000 Å thick) and are separated by diffused channel stops. Light photons pass through the photogate and are absorbed in the single crystal silicon. Charge carriers are created by hole-electron pair production and accumulated in the image sensor elements.

The amount of charge so created depends on, among other things, the integration time and the incident light intensity. After some time, accumulated charge packets are transferred out, via transfer gates, to the CCD shift registers. Alternate packets are transferred to the A and B registers. Each CCD register, shielded from light by a layer of aluminum, moves the picture elements, often called "pels" or "pixels", serially from the sensor elements to the output stage.

Each register is 130 bits long, of which only the first 128 can directly receive charge packets from the image sensor elements. The last two bits are used to allow charges from the shift registers to merge smoothly into a single channel before reaching the output stage.

A precharged diode or floating diffusion, connected to the gate of an on-chip MOS amplifier, senses signal charges, and the amplifier output voltage becomes proportional to the charge packet and the reference potential. A compensation circuit in the CCD 110F reduces reset noise.

Fig. 3.2. Block diagram of CCD 110F. Incident light is absorbed in photoelements, a_1 to a_{256} , and generates charges. Collected charges are then transferred to two shift registers, A and B, via two transfer gates, T1 and T2. Charge packets are then serially clocked out to the output stage where they are converted into voltage.

by providing a second output voltage, proportional to the reference potential so that the difference of the two outputs is the net signal with greatly suppressed reset noise. For practical reasons, the compensation circuit was not used in any experiments: the required extra peripheral circuitry to recover the signal by subtracting one CCD output signal from the other is complex, and, not much is gained from reducing reset noise if other system components, like the optical arrangement, are determining factors in the image processor performance.

The CCD 110F is a linear image sensor. Being so, it can only be used to process one-dimensional (1-D) images. For practical considerations, 2-D photographic negatives, which are illuminated with a controllable light source, were used as objects. To simulate a 1-D situation, image patterns were designed in such a way that they would vary along an axis parallel to the CCD photoelements distribution axis. Some typical test patterns are shown in Fig. 3.3.

An optical system is required to focus the object onto the imaging device. A satisfactory light source can be constructed with a common light bulb and some focussing lenses. The optical arrangement is shown in Fig. 3.4.

3.4 Control circuitry

3.4.1 Discussion on CCD clocks

In the CCD image processor, signal processing is done by controlling the charge gathering process in the image sensors. This is done by controlling the CCD clock voltage waveforms. They are generated by digital TTL circuitry ("clock generation circuit" in Fig. 3.1), according to a set of tap weights stored in a RAM. To complement the control circuitry, a microcomputer is used to generate the various sets

Figure 3.3. Typical test patterns for preliminary experiments
(shown in actual size).

Fig. 3.4. Optical Setup

of tap weights needed for different processing applications. Tables 3.1 and 3.2 contain a description of clocks and voltages needed to operate the CCD 110F.

The standard operation of the device requires eight different clock waveforms. There is one clock for each transfer gate and one set of complementary clocks for each shift register; they respectively correspond to ϕ_{XA} and ϕ_{XB} , ϕ_{1A} , ϕ_{1B} , ϕ_{2A} and ϕ_{2B} in Table 3.1. Since the two CCD registers in the device are time-division multiplexed, only one reset (ϕ_R) and one sampling (ϕ_S) clocks are required. They must, however, be operated at twice the frequency of the shift register clocks.

To reduce the complexity of the control circuitry, the outputs from two adjacent cells were combined by operating clocks ϕ_R and ϕ_S at one half the normal operating frequency. In other words, the number of effective photoelements is reduced from 256 to 128 and the number of CCD clock waveforms is reduced from 8 to 5, ϕ_{XA} being identical to ϕ_{XB} and ϕ_{2A} , ϕ_{2B} being identical to the set ϕ_{1A} , ϕ_{1B} . The clocking sequence for normal imaging mode using this modification is shown in Fig. 3.5. In the following discussion, the subscripts A and B are dropped for simplicity.

Clocks ϕ_1 and ϕ_2 have to be exactly complementary to facilitate efficient charge transfer in the shift registers. When ϕ_1 is high, no shifting takes place, the output diffusion can be reset and charges can be transferred from the photosites to the shift registers. When ϕ_2 is high, charge packets in the registers are shifted one step towards the output stage. The output diffusion region is reset when ϕ_R is high and the output waveform becomes valid when ϕ_R comes back to the low state. The charge to voltage conversion is initiated by the falling edge of ϕ_R .

In the camera mode of operation (Fig. 3.5), transfer gate clock

<u>CLOCK</u>	<u>DESCRIPTION</u>	<u>PULSE DURATION</u>	<u>PULSE AMPLITUDE</u>
$\phi_{1A} = \phi_{1B} = \phi_1$ $\phi_{2A} = \phi_{2B} = \phi_2$	Complementary clocks for the two phase analogue shift registers to carry charge from the input to the output end.	.95 μ sec	10V
ϕ_R	Reset clock to periodically reset the floating diffusion at the end of the CCD registers. Its leading edge terminates the charge to voltage conversion.	.6 μ sec	10V
$\phi_{XA} = \phi_{XB} = \phi_T$	Transfer gate clock to transfer charge from the photosites to both shift registers	.6 μ sec	10V
ϕ_S	Sampling clock used at the output of the CCD to sample information at the proper time.	.5 μ sec	10V

Table 3.1. CCD 110F driving clock waveforms [16].

<u>VOLTAGE SUPPLY</u>	<u>DESCRIPTION</u>	<u>TYPICAL VALUE (VOLTS)</u>
V_{OD}	Drain voltage of the output source follower transistor	+15V
V_{RD}	Reset diffusion voltage to precharge the floating diffusion during the ON time of the ϕ_R clock	+15V
V_{OG}	Voltage of the last transfer electrode of the shift registers. It aids the flow of charge to the charge sensing stage	+6V
V_{PG}	Bias voltage of the photogate to bias the imaging cells in deep depletion	+9.5V

Table 3.2. CCD 110F voltage supplies [16].

Fig. 3.5. Timing sequence of CCD clock waveforms for the camera mode of operation. It illustrates the five clocks needed to operate the CCD 110F when 128 "effective" photoelements are used. Transfer gate clock Φ_T , comes ON every 128th Φ_1 clock pulse, allowing a complete frame to be clocked out before other charge packets are transferred to the shift registers. All clock cycle periods are identical.

waveform (ϕ_T) goes high every 128th ϕ_1 clock pulse. In other words, the frequency of occurrence of ϕ_T is 128 times slower than the frequency of occurrence of all other clock waveforms: ϕ_1 , ϕ_2 , ϕ_R and ϕ_S . Therefore, to reproduce an image at the output of the CCD, charges are transferred once from the photoelements to the shift registers (when ϕ_T is high) and all clocked out before other charges are transferred to the registers. Because there are 128 effective photoelements, it takes 128 clock cycles to clock a frame out. In this discussion, a clock cycle refers to a sequence of ϕ_1 , ϕ_2 , ϕ_R and ϕ_S clock pulses and a frame refers to the image recorded in the CCD photoelements.

To summarize the imaging mode of operation, first, photoelements collect charges during a predetermined amount of time. Clock waveform ϕ_T then goes high and charges are transferred from photoelements to CCD shift registers delay elements. Clock ϕ_1 is high during this transfer time and so is ϕ_R , to reset the output diffusion region. Then ϕ_2 goes high to shift charge packets one stage towards the CCD output. During this time, ϕ_S goes high to sample the CCD output voltage (proportional to the charge packet just shifted out of the CCD). Clocks ϕ_1 , ϕ_R , ϕ_2 and ϕ_S follow the same sequence 127 more times before clock waveform ϕ_T goes high again to transfer a new frame in the CCD delay elements.

In imaging applications, special care has to be taken in order not to saturate the CCD output because of the long integration times. Intensity of the incident light or clock cycle length can be easily controlled to avoid saturation. The latter method is implemented using software techniques in the digital controller of the control subcircuit to control the occurrence of clock pulses.

The timing sequence for the processing mode of operation is shown

in Fig. 3.6. The shift-and-add capability of the CCD is needed to perform discrete summations, essential to most image processing applications. To make use of this shift-and-add capability, the transfer gate clock waveform is operated at the same frequency as the other CCD driving clocks. It is in fact identical to the reset clock waveform, ϕ_R . Therefore, every time ϕ_1 goes high, ϕ_T also goes high so that accumulated charges in the photoelements are transferred to the shift registers delay elements and added to their previous content. After, ϕ_2 goes high and charge packets are shifted to the next delay element, towards the output stage. Reset clock ϕ_R and sampling clock ϕ_S follow the same cycle as in the camera mode of operation: ϕ_R goes high when ϕ_1 is high and ϕ_S goes high when ϕ_2 is high.

3.4.2 Implementation

A block diagram of the control subcircuit is shown in Fig. 3.7. A clock generation circuit, a digital memory and a microprocessor are the main elements. The microcomputer system is used to generate sets of coefficients or tap weights defining the type of processing to be done. They are sent to random access memories for temporary storage. The two 5.2×4 bits RAM devices are capable of storing 512 8-bit words.

In a continuous operation, each coefficient is sent one at a time from the RAMs to some TTL circuitry that generates all CCD control clocks. A $\div 256$ counter is first loaded with the 8-bit word and counts up to "FF" in hexadecimal notation. Its "carry" line goes high at the count of "FF" and sends a trigger pulse to a monostable multivibrator that generates the first clock pulse: ϕ_S . Then a series of monostable multivibrators are used to generate the various clock pulses and delays between them. The charge gathering process in the photoelements is thus controlled by the

Fig. 3.6. Timing sequence for image processing applications. Contrary to the camera mode, ϕ_T comes ON at every clock cycle for processing applications. Clock waveforms ϕ_R and ϕ_T are identical. Clock cycle periods may vary from 1.67 μsec to 206.5 μsec . Pulse widths for ϕ_1 , ϕ_R , ϕ_T and ϕ_3 are the same as in Fig. 3.5.

Fig. 3.7. Block diagram of the control circuit.

tap weights, a large coefficient meaning a small integration time.

The last multivibrator allows the process to repeat itself by controlling the "load" line of the $\div 256$ counter. When all clocks have been generated, that line goes high and the counter gets a new tap weight from the RAM. The same pulse also goes to the "clock" input of a $\div 512$ counter, of which the output lines determine the location in the RAM of the next coefficient to be fetched. In some applications, 512 coefficients are needed and the $\div 512$ counter counts from "000" to "1FF" (HEX). In other applications, only 128 coefficients are needed and the counter goes from "000" to "07F" (HEX).

Another counter, a $\div 128$ one, is needed to generate ϕ_T for imaging applications. It counts the ϕ_1 clock pulses and sends a trigger pulse to a monostable multivibrator every 128th ϕ_1 pulse.

The master clock that operates the $\div 256$ counter is variable but 1.2 MHz was chosen as a convenient frequency for all experiments. The maximum integration time is determined by the maximum count of the $\div 256$ counter: from "00" to "FF". It is of the order of 0.2 milliseconds.

The minimum integration time should theoretically be 0 seconds. However, enough time should be given to the hardware circuit to generate the various clocks before the next tap weight is fed into the $\div 256$ counter. Moreover, the "load" line of the $\div 256$ counter is synchronized with its clock input so that a new tap weight can be entered only on the positive edge of the master clock pulse. Therefore, the minimum integration time is determined by the time required to generate all CCD driving clocks and should be an integral multiple of the master clock cycle time (i.e.: until a new tap weight is entered into the counter). For this setup, it is about 1.67 microseconds (or 2 master clock cycles) and "FF" is the

corresponding coefficient fed to the inputs of the $\div 256$ counter. It should be mentioned that the minimum integration time is not restricted to this value: it can correspond to any integral multiple of the master clock cycle time, which can also be modified.

If the illumination is constant (in time) for all photosites, the minimum integration time would allow a "fat zero" to be propagated through the device. The small offset so created at the CCD output reduces a little the dynamic range of the system.

To illustrate the clock generation process, two examples are given. First, Fig. 3.5 shows the timing sequence for the camera mode of operation. Tap weights are all the same, producing clock waveforms that go high at regular intervals as shown in Fig. 3.8a. The integration time is the same for all 128 clock cycles of a frame so that the optical input is in fact multiplied by a constant factor in the photoelements and a reproduction of the image is obtained at the output.

Fig. 3.8b is an example of the processing mode. In this case, a convolution between the image (rectangle) and a set of tap weights simulating a second rectangle is made. The tap weight rectangle is produced by a few long clock cycles, the other ones being short and representing the bias level. Typical values are "CF" for the bias and "00" for the long cycles. The detailed timing sequence of a clock cycle was shown in Fig. 3.6.

The clock generation circuit makes use of the coefficients to generate the CCD control clocks. A PROMPT 48 microcomputer system made by INTEL CO*, is used to generate these coefficients. It introduces versatility in the system in the sense that the RAM content can be easily modified by the microprocessor. Specification sheets of the PROMPT 48 are given in Appendix C. For each application, e.g., camera mode, edge

* Intel Co, 3065 Bowers Avenue, Santa Clara, Ca, 95051

(a)

(b)

Fig. 3.8. Clock cycle generation examples.

In the camera mode (a), all clock cycles have an identical period. The image is offset by a constant bias.

In the convolution example (b), short cycles define a bias level while five long cycles define a rectangle of length $5 \times T_2$ in time. The frame is therefore made of two different clock cycles, of length T_1 and T_2 .

detection, convolution, etc. .. a machine language program is written and stored in the microcomputer internal memory. When executing one of these programs, the microprocessor sends the appropriate tap weights serially to the proper locations in the external RAM, via some input-output (I/O) ports. An example of such a program and the corresponding flow diagram are given in Appendix D.

Although the PROMPT 48 has 1K byte of internal RAM, there is a need for some external memory to meet the system speed requirements. As previously mentioned, the minimum integration time should be close to 0 seconds: a "fat zero" level propagated through the CCD is good but the larger it is, the smaller the dynamic range is. Also image processing should be done as fast as possible, eliminating the possibility of having a time delay between each clock cycle. The clock generation circuit has thus to fetch a new tap weight every 1.67 microseconds (minimum integration time). On the other hand, the PROMPT 48 has a basic machine cycle time of 5 microseconds (2 microseconds for the newer version). It takes one or two machine cycles to execute an instruction and it takes many instructions to send one word of data to the external circuit. It is obviously too slow to meet the speed requirements of the clock generation circuit. Some microcomputer manufacturers have solved the problem by creating a Direct Memory Access facility to speed up transfer of data between the microcomputer and the external circuit. Unfortunately, the PROMPT 48 does not have DMA capability.

Because of economical constraints and because of ~~the~~ general versatility of the PROMPT 48, it was decided to use it and to solve the speed problem by adding an extra RAM, external to the basic microcomputer system. Its access time being less than 0.5 microseconds, it meets the

clock generation circuit requirements. In a first, non critical step, the RAM is filled by the PROMPT 48 at a "slow" speed; no processing is done during this time. In a second step, the RAM sends its data to the hardware circuit at a fast rate for image processing while the micro-computer is disabled.

The external memory can be addressed by the microcomputer or by the hardware circuit ($\div 512$ counter) and it can send its data to the hardware circuit ($\div 256$ counter) or get it from the microprocessor. The read/write line of the RAM is controlled by the PROMPT 48. However some tri-state buffers are needed to control the access to the RAM address lines. They are microprocessor controlled too. First, the PROMPT 48 puts the RAM in a "write" mode and sends data into it, controlling its address lines. Then, it puts the RAM in a "read" mode and gives control of the address lines to the hardware circuit by putting itself in a "passive" or disabled mode and remains in this mode until an interrupt signal is issued through one of the entries of the microcomputer periphery (broken lines in Fig. 3.7).

As it can be seen, the use of a microcomputer in the control subcircuit makes the system versatile: the image can be processed in many different ways under user control.

The Fairchild CCD operates at MOS levels: 0 volts for the low level and +10 to +12 volts for the high level. Standard LH 0026 MOS drivers were used to pull TTL levels clock waveforms ϕ_S , ϕ_T and ϕ_R to MOS levels. However, due to the criss-crossing nature of ϕ_1 and ϕ_2 that must be maintained, a special interface circuit was used for these two clocks [9]. The circuit diagram is shown in Fig. 3.9 and a picture of these two clocks is shown in Fig. 3.10.

Fig. 3.9. Interface circuit (TTL to MOS LEVEL) for clocks ϕ_1 and ϕ_2 .

Fig. 3.10. Picture of ϕ_1 and ϕ_2 . This picture shows the criss-crossing nature of complementary clocks ϕ_1 and ϕ_2 .

Horizontal Scale: 0.5 μ sec/division

Vertical Scale: 5 volts/division

Top Trace: ϕ_2

Bottom Trace: ϕ_1

3.5 Postprocessing circuitry

The last stage of the experimental setup is the postprocessing circuit. Its main purpose is to arrange the output into a convenient form, e.g., a digital output, a hard copy printout, etc ... This stage can be divided into two parts. First an analog circuit, essential for easy visual display, is described. Second, a digital data collection system for performing sophisticated postprocessing such as in the Discrete Fourier Transform experiments, is described.

3.5.1 Analog circuit

The analog circuit is a very flexible one. It can be modified according to one's intentions and to the application. This is why it is divided in many small blocks of which some are essential to all processing applications. The circuit diagram of this analog output recovery circuit is shown in Fig. 3.11.

The first and second blocks form a sample-and-hold circuit. Every time the sampling clock ϕ_s goes high, a sample is taken and held until another one is taken, i.e., for a complete clock cycle.

The next blocks are filters and amplifiers. The CCD output signal being of the order of 150 millivolts, it is convenient to amplify it before doing any further processing. The use of filters depends upon the application and the type of image. In general, filtering any high frequency noise means smoothing all edges in the signal. There is, therefore, a trade off to be made between clear signals and sharp edges. For example, in the camera mode, the output signal-to-noise ratio (SNR) is usually very good. It is then better to take advantage of the unfiltered sharp picture (sharp edges). In this case, the output is directly taken after the amplification stage (output A in Fig. 3.11). However, when doing an edge

Fig. 3.11. Circuit diagram of analog output recovery circuit. The analog output can be taken at different places in the circuit (A, B or C), depending on the application.

detection, the output signal is weak and so is the SNR. It is mainly due to the small integration time difference between "bias" tap weights and the other ones (more explanations are given in Chapter 4). For this situation, it is better to filter out the high frequency noise components resulting in smoothed edges. The output (B) is then taken after the filtering stages: one high pass to eliminate 60 Hz pick up and one low pass, for high frequencies noise suppression.

A comparator circuit is included in the postprocessing circuitry. It is particularly useful for edge detection applications where the single bit digital output of the comparator indicates quite accurately the edges of the image. A more sophisticated analog-to-digital conversion circuit can also be used and is discussed in the next section.

3.5.2 Digital data collection system

This circuit is very useful when further processing has to be done on the signal or simply for data storage. The data collection system basically converts an analog signal into an 8-bit digital signal, compatible for interfacing with computers or mass storage devices. It is more complex but more powerful than the simple comparator.

The data collection system block diagram is illustrated in Fig. 3.12. A Gould Storage Oscilloscope, model OS4000 [18], is used to digitize and store the output signal. An INTEL SDK-85 microcomputer system [19] interfaces the stored data to a teletype.

The Gould scope has two channels and a total storage capacity of 512 8-bit words. When both channels are used, one contains the output signal and the other one a marker indicating the start of a frame, so that 256 samples of each signal are taken. The analog samples are first transformed in an offset binary coded signal by the scope and then stored.

Fig. 3.12. Block diagram of data collection system

In a second step, the SDK-85 changes the signal into a decimal one, a form that lends itself better to data manipulation: graphs, calculations, computer interfacing, etc. ...

When the scope has stored all samples, it sends an interrupt pulse to the microprocessor CPU. After having acknowledged the interrupt, the SDK-85 starts the binary to decimal conversion and stores the samples in some external RAM. A "Display Memory" command to the SDK-85 monitor routine sends the RAM content to a teletype to get a hard copy of the digital output signal. A flow diagram and a program listing can be found in Appendix E.

Finally, a multiplexing circuit is needed between the processor and the Gould scope, the latter having two sets of eight output lines, one for each channel, and the former having only eight input lines.

As it can be seen, the image processing system contains two different microcomputers: a PROMPT 48 in the control circuitry and an SDK-85 in the data collection system. This apparent inefficient use of microcomputers can be explained by some constraints of the system and of the microcomputers themselves. First, the PROMPT 48 internal RAM is almost all occupied by various tap weight generation programs. The external RAM contains tap weights needed to generate all CCD clock waveforms for a particular application and the only two available I/O ports connect the microprocessor to this external RAM. If the PROMPT 48 were to be used for data collection purposes, it would have to be on a time sharing basis between the control and data collection circuits. The image could however be processed only once since the stored tap weights would be lost when the digital output samples were written in the internal RAM, assuming the PROMPT 48 internal RAM is used to store tap weight generation programs

only. This approach is good in some applications but in others, like surveillance, or in an experimental system, continuous processing of the image is preferable. A second microcomputer is then needed unless a larger, more powerful one is used to replace both the PROMPT 48 and the SDK-85 (a new version of the PROMPT 48 with increased RAM space, for example). The first solution was used for economical reasons. In summary, the CCD image processor is not restricted to the use of any particular microcomputer. Two microcomputers, a PROMPT 48 and a SDK-85, were used for simplicity in this system: the former in the control subcircuit and the latter in the digital postprocessing circuit.

P

CHAPTER 4

EXPERIMENTAL RESULTS

4.1 Introduction

The results of basic experiments like reproduction of the image, convolution and edge detection are reported in this chapter. The main objective is to demonstrate the feasibility of the integration time modulation technique in a CCD linear image processing system. Main sources of noise, dark current and transfer inefficiencies in the system are also analysed.

Applications of the CCD linear image processor to many practical situations are finally discussed. They include single parameter monitoring applications like a fluid level indicator or a wire thickness controller, bar code reading/decoding applications and frequency spectrum related applications.

4.2 Preliminary experiments

When operating in the camera mode, the CCD reproduces accurately the optical input at the output. The total time required to clock a complete frame or image out of the shift registers is 128 times the basic clock cycle time. The cycle time is constant for all clock cycles and has to be short enough to keep the photosites from saturating given a constant incident light intensity. Optimum values for a clock cycle range between 16 and 52 μsec and it therefore takes between 2 and 6.7 msec to clock a frame out.

Fig. 4.1 is a picture of the processor output signal (output A - in Fig. 3.11) when it is operating in the camera mode. The image is a transparent bar on a dark background. The incident light goes through

Fig. 4.1. Camera mode example. In this mode of operation, the image is reproduced at the output. All tap weights have the same value so that the optical signal is multiplied by a constant bias in the CCD. The image is a single transparent bar on an opaque background.

vertical scale: 2 volts/division
horizontal scale: external mode (see section 4.3.2)
length of frame: 6.78 msec
tap weights: "C0" (in hexadecimal)

the transparent portion of the image and generates charges in about ten photoelements of the CCD. The picture shows a complete frame, i.e. 128 image samples.

Ideally, the output should be of a binary form: all 128 samples should be at low or high state to represent dark or transparent portions of the image. In practice however, the output signal is blurred. Small portions of the incident light travel in a direction not perpendicular to the silicon frontal surface of the CCD and hit adjacent photoelements that should not normally receive light. Blurring and, to a lesser extent, transfer inefficiency, are the main reasons for having intermediate potential levels at the CCD output. The small ripples that can be seen on the top part of the rectangle of Fig. 4.1 are due mainly to non uniform incident light intensity, optical input shot noise and dark level non uniformities.

The relatively poor optical set up is a major error source in this experiment and all the other ones.

Hexadecimal tap weight coefficients used in all image processing applications lie between 00 and FF. They are normalized so that FF represents the lowest level (0.0) and 00 the highest level or (1.0). FF is then equivalent to the minimum integration time and 00 to the maximum one. Coefficients used to produce the image of Fig. 4.1 are all "CO" in hexadecimal. The integration time for each cycle is then:

$$64 \times 0.8 + 1.67 = 52.9 \text{ } \mu\text{sec} \quad (4.1)$$

where 64 is the count from "CO" to "FF", 0.8 μsec is the master clock period and the unit increment in discrete integration time, and 1.67 μsec is the time required for the generation of all clock pulses of a cycle. Being determined by the coefficients, the integration time can easily be

modified.⁴ Too much integration time can saturate the output and not enough can give a poor SNR. An optimum range of integration time exists between these extremes and 52.9 μ sec is in this range.

In the next preliminary experiment, the CCD is used as a convolver. The transparent bar of the previous example is convolved with a series of tap weights simulating another rectangle. A few long clock cycles determine the size (length in time domain) of the rectangle and all others are kept very short and produce a small bias level at the output.

Figure 4.2 illustrates the convolution product of the optical signal (transparent bar) with various sets of coefficients simulating rectangles of different sizes. From visual inspection, the best match is obtained in Fig. 4.2b (the convolution product is closest to a triangle). In this case 12 long clock cycles of 206.5 μ sec each, defined by tap weights of value "00" (hex), determine a rectangle 1.85 msec long in the time domain.

The next figures are the results of other convolution experiments. In Fig. 4.3, a rectangular image is convolved with a set of tap weights defining two identical strings of 12 long clock cycles. The result of the convolution is a good match between the electrical and optical input signals. Fig. 4.4 illustrates the convolution product of an image made of two transparent bars with a set of tap weights defining a single rectangle. From the output, it can be noticed that the electrical signal (21 long clock cycles of 206.5 μ sec each) matches the large rectangle better than the small one. These examples demonstrate that the best match of a simple image is easily found with the CCD linear image processor used as a convolver.

Another practical application of the CCD image processor is in contour extraction of an object. It often gives enough information to

Vertical scale:
5 volts/division

Horizontal scale:
external mode

length of frame:
6.5 msec

tap weights:
4 of value "00"
124 of value "CF"

(a)

Fig. 4.2. Convolution of two rectangles.

The image, a transparent bar on an opaque background, is convolved with simulated rectangles of various lengths. A best match is obtained when the convolution product is a triangle of base $2l$, l being the rectangle's length, as in Fig. 4.2b.

Fig. 4.2a illustrates the case where the simulated rectangle is smaller than the optical one and

Fig. 4.2c illustrates the opposite case.

Vertical scale:
5 volts/division

Horizontal scale:
external mode

length of frame:
7 msec

tap weights:
12 of value "00"
116 of value "CF"

(b)

Vertical scale:
5 volts/division

Horizontal scale:
external mode

length of frame:
8.6 msec

tap weights:
21 of value "00"
107 of value "CF"

(c)

Fig. 4.3. Convolution example.

In this example, the optical signal is a rectangular bar and is convolved with a set of coefficients defining two rectangles of the same size. Each one is defined by 12 clock cycles of 206.5 μ sec each. The bias level is set by tap weights of value "CF" (hex).

Vertical scale: 2 volts/division

horizontal scale: external mode

length of frame: 9.1 msec

tap weights: 24 of value "00"

104 of value "CF"

Fig. 4.4. Convolution example.

Two rectangular bars (top trace) are convolved with a set of coefficients defining a single rectangle. 21 long clock cycles of 206.5 μ sec are used to do so. The bias level is defined by tap weights of value "EE" for the top trace and "CF" for the bottom one.

Vertical scale: 5 volts/division

horizontal scale: external mode

length of frame: 1.7 msec for the top trace (camera mode)

8.4 msec for the bottom trace (convolution)

classify or recognize an object and is easily implemented. It is very useful in surveillance applications. In one-dimensional cases, edge detection can be performed by various methods among which double differentiation of the image is often used [20].

For discrete time signals, the second derivative can be approximated by $a(n) - 2a(n-1) + a(n-2)$ [20]. The second difference scheme can be viewed as a correlation of the image with coefficients given by a sequence like $\{-1, +2, -1, 0, 0, 0 \dots 0\}$. Proper bias has to be applied to the coefficients to avoid negative taps in the digital circuitry. Fig. 4.5 shows a possible set of normalized coefficients (in decimal form) along with the results of correlation with a rectangle. Fig. 4.6 shows the actual result obtained in such an application.

Experimental results on edge detection revealed however that image contours or edges produce rather low amplitude output spikes since this particular correlation has only three non-zero taps. The bias applied to the coefficients further reduces the output swing. By increasing the number of non-zero tap weights, it is possible to improve the output signal amplitude. For example, the set $\{-1, -1, -1, 6, -1, -1, -1, 0, 0, 0 \dots 0\}$ is used in 4.7a. This should be compared with the set $\{-1, -1, -1, -1, -1, -1, +12, -1, -1, -1, -1, -1, -1, 0, 0, \dots 0\}$ used in Fig. 4.7b. However, the increase in output amplitude is done at the cost of a slight spreading of the edges.

Referring again to Fig. 4.6, it can be seen that the three rectangles forming the image (top trace) have different amplitudes. They are in fact identical and the difference observed on the picture is due mainly to the poor focussing system used and the non uniform light source. The bottom trace is a digital approximation of the analog output waveform.

Fig. 4.5. A possible set of coefficients for edge detection is shown in the middle. When convolved with the image displayed in the top, it produces the result shown in the bottom. Other sets of coefficients can also be used; for example, the set $\{0, 0, 0, 1, 0, 0, 0, .16, .16, .16 \dots .16\}$ is used in Fig. 4.6 and 4.7a.

Vertical scale:
 top trace: 10 volts/div.
 middle trace: 0.5 volts/div.
 bottom trace: 2 volts/div.

horizontal scale: external mode

length of frame:
 top trace: 0.77 msec
 middle and
 bottom trace: 3.8 msec

Fig. 4.6. (a) Tap weight pattern used for edge detection;
 (b) top trace - image; middle trace - results of correlation between image and the tap weights;
 bottom trace - output of the comparator

Vertical scale: 5 volts/div.
horizontal scale: external mode

Vertical scale: 1 volt/div.
horizontal scale: external mode
length of frame: 3.8 msec

(a)

Vertical scale: 10 volts/div.
horizontal scale: external mode

Vertical scale: 5 volts/div.
horizontal scale: external mode
length of frame

(b)

Fig. 4.7. Edge detection of a rectangle with different tap weight patterns.
In (a) 7 taps were used
In (b) 13 taps were used
Amplitude of the output signal increases when the number of taps defining the edge detection is increased. Sharpness of the output signal is however slightly reduced.

The single bit digital output given by a comparator (output C in Fig. 3.11) has a logic level 1 whenever there is an edge. A pair of ones define the boundaries of a rectangle image. This digital output is very useful to accurately locate the edges of an image or to store the output in digital mass storage devices. A more complex 8 bit digitizing circuit is used in the frequency analysis experiment, where accurate approximations are needed.

4.3 Some limitations of the CCD image processor

4.3.1 Noise sources and transfer inefficiencies

Transfer inefficiency in a CCD has previously been discussed in Chapter 2. In general, transfer of charges is affected by the speed of operation of the device and by trapping states in the conducting channel. The latter effect, combining bulk state trapping and edge effect is dominant in BCCD's when the device is operated at relatively low frequencies, which is the case in this work (clocking frequencies between 4 kHz and 0.5 MHz).

Using simple techniques, the total transfer inefficiency can be measured [14]. An experiment was done with the CCD operated in the camera mode and two photocells illuminated: one near the input end of the CCD and one near the output end. Both charge packets were clocked out and their amplitudes compared. If the two photoelements are n cells apart, the transfer inefficiency ϵ is given by: [14]

$$\epsilon = \frac{V_o - V_1}{nV_o} \quad (4.2)$$

where V_1 is the output voltage corresponding to the cell near the input end and V_o the output voltage corresponding to the other cell.

Preliminary experiments demonstrate that ϵ has little effect on

the system performance as compared to the optical effects like blurring and non uniformity of light and therefore measurements of ϵ alone could not be made with accuracy. Non uniformity of the incident light is due to the fact that a common light bulb (G.E. Reflector Flood; 300 w; 120v) was used as the light source. The beams hitting the two illuminated photocells might differ a little. A monochromatic narrow beam light source such as a laser beam would eliminate this problem.

Blurring of the image is due to the fact that some part of the incident light does not travel in a direction perpendicular to the photoelements frontal surface. This part of the incident light might not reach the proper photoelements but neighbouring ones, thereby creating charges where there should not be any. Proper alignment of the photoelements on the device package and proper alignment of the CCD, the photographic negative and the incident light on the same axis would greatly reduce the blurring effect but are very difficult to achieve.

Dark current level non uniformities are another important limiting factor. According to the CCD 110F specification sheets in Appendix B, the average dark signal is about 0.4 millivolts or 0.25% of the saturation output voltage of the device, which is around 150 millivolts in this case. However, the dark level non uniformities may take much higher values than the average dark current and they can be a serious problem in experiments like edge detection.

Dark current measurements were made but it was unfortunately impossible to isolate it from noise sources such as reset noise. However, the temperature dependence of dark current was verified fairly easily.

The results show that the localized dark currents increase exponentially with temperature and are dominant above room temperature (25°C). Cooling the device reduces both the average dark current and the dark level non uniformities. The latter, however, remains important along with reset noise at low temperatures (below 0°C).

4.3.2 Distortion effect

In the CCD 110F image sensor, charges are continuously integrated in the photosites and are cyclically transferred to the shift registers according to the time varying clock cycles. The variations in cycle time affect the linearity of the CCD output. To illustrate this problem, a convolution between two rectangles is taken as example.

The optical input and the simulated rectangle are shown in Fig. 4.8 together with clock ϕ_1 . Clock ϕ_1 illustrates the various clock cycles needed to simulate a rectangle. In this example, twelve long cycles of 206.5 microseconds each were used to define the rectangle; the remaining 116 cycles of the frame define the bias level.

All clocks follow the same cycle as ϕ_1 . The reset clock ϕ_R then resets the output diffusion at unequal intervals and output samples are held for unequal periods of time in the sample and hold circuit. Remembering that the CCD image processor is processing a time dependent version of a steady image, the time dependent output signal is a distorted waveform as compared to the expected result shown in Fig. 4.9a. The frequency spectrum of the output signal is also distorted but can be disregarded because we are only interested in the time representation of a spatially defined image.

Several methods can be used to correct the CCD output signal. A possible one consists of a RAM and an analog-to-digital converter. The

Fig. 4.8. Convolution of two rectangles.

The optical input is shown on the top. It occupies 10 photocells in the CCD. The other rectangle is shown in the middle and is simulated by 12 long clock cycles of time $t_2 = 206.5 \mu\text{sec}$. The other 116 cycles of a frame define the bias level.

Fig. 4.9. Convolution of two rectangles.

The expected result of a convolution of two rectangles is a trapezoid with equal slopes and is shown in (a). (It could be a continuous or discrete time signal). T_1 represents the base of the trapezoid and T_0 the frame time. The actual waveform coming out of the CCD is shown in (b). T_0 and T_1 are the same. Unequal sampling intervals distort the output.

samples are digitized as they come out of the CCD and are sequentially entered in the RAM. The effect of unequal intervals is suppressed by reading out the memory at a fixed rate.

Other methods do not correct the signal itself but rather the visual representation of the time dependent output signal. This can be done for example by making use of the x-y mode (on the time base) of an oscilloscope and feeding the x input with a ramp and the y input with the CCD output signal. The ramp voltage level would be controlled by ϕ_1 and incremented one unit every time ϕ_1 goes "HIGH". Output samples would therefore have equal weighting or equal spreading on the display and the expected convolution product would appear on the oscilloscope.

The second correction mechanism was used in this study because it is relatively inexpensive and because the emphasis was put on the time domain representation of an image. Fig. 4.10 illustrates the two correction mechanisms and Fig. 4.11 is a picture of the original output and the corrected one using the second correction approach.

A CCD with a different internal configuration would avoid the distortion problem. Photosites would ideally integrate charges only during the ON time of some clock, say ϕ_p , controlled by the same clock generation circuit as the other CCD clocks. The total cycle time would remain constant but the amount of integrated charges would depend on the light intensity and on ϕ_p .

4.4 Experiments

The CCD linear image processor finds applications in many areas: in industry where control of I-D variables are often required, in the military or more generally in security oriented applications, as a surveillance and recognition system. The following experiments were done to demonstrate

Fig. 4.10. Output correction methods for the CCD 110F. A convolution between two rectangles is made. In method "A" only the visual representation of the time signal is corrected in method "B", the signal is corrected.

Fig. 4.11. Output signal of a convolution.

For the same example as in Fig. 4.8, the CCD output without any correction mechanism, is shown in the top trace. The effects of unequal sampling time intervals can be seen in the negative slope of the trapezoid. The bottom trace is the corrected representation of the time signal using a ramp and the x-y mode (time base) of a Tektronics 463 oscilloscope.

Vertical scale: 2 volts/division

horizontal scale:

top trace: 0.5 msec/division

bottom trace: external mode

length of frame: 4.9 msec.

some of the possible applications of the proposed system.

4.4.1 Fluid level indicator

In industry, the quality of manufactured products often depends on an automated control of one-dimensional parameters. This control is usually done by electro-mechanical devices. The proposed CCD linear image processor could well replace these control systems and offer more flexibility, more reliability and more compactness. On a wire production line for example, the processor could monitor the diameter of the final product. Another example is the control of fluid level in reservoirs, containers, etc. ...

An easy method of measuring the liquid level in a container is to have a floating gauge in the container and mechanically or electrically measure the gauge level. The information can then be transmitted to a control or display unit, as in a car gas tank for example. Sometimes it is not practical and even possible to put a gauge in the liquid, which might be too corrosive or too light, for example. In these cases, a system of communicating reservoirs can successfully be used to measure the liquid level in a container. Fluid dynamics equations linking volumes and pressures of the main reservoir and the sample or monitor tube can be found in basic physics textbooks [21, 22].

However, these easy solutions are not always applicable. Some special cases require sophisticated equipment such as laser or ultrasonic beams to get an accurate measurement without any interaction with the fluid. One such system could be made of a light source shining on one side of the reservoir, and a CCD on the opposite side. An optical system can reduce the image, i.e.: the reservoir, to the CCD's dimensions.

The CCD image processor, operated in the camera or edge detection mode,

would give an accurate reading of the fluid level.

A similar system could use the communicating reservoir principle. The image processor would look at a small tube in which the fluid level is proportional to that of the main reservoir.

An advantage of the CCD based system over the others is that it is versatile: it can be programmed to execute more than one task. For example, the image processor can be designed to monitor the fluid level and send out a signal when it is too low or too high. To do so, the image processor would convolve the image with a set of preprogrammed tap weights defining the minimum or maximum acceptable levels in the container. When a perfect match is reached, a warning signal is sent to a control board and immediate action can be automatically or manually taken. Real time convolution allows the image processor to control very fast processes with accuracy. Present levels can easily be changed by modifying the tap weights.

An alternate approach to monitor the liquid level in the reservoir is based on edge detection. Using the digitizing circuit described in Chapter 3 and edge detection algorithms, it is possible to automatically monitor the parameter of interest. Fig. 4.12 illustrates this application. The top trace of Fig. 4.12a is the image given by the processor when operating in the camera mode. The bottom trace is the result of an edge detection. As the reservoir fills up, the edge moves from left to right in the image (Fig. 4.12b). A digital approximation of the edge detection product in a comparison circuit, could provide automatic control of the process and stop it at a preset level.

Some drawbacks are unfortunately associated with this system. First, it is probably more expensive than most existing systems. Its

Fig. 4.12. Fluid level indicator.

In both pictures the top trace indicates the amount of liquid in the reservoir. Presence of liquid is shown by a low state of the output. The bottom trace is the output of the CCD when used as edge detector.

For both pictures: Top trace: imaging mode
 vertical scale: 10 volts/division
 horizontal scale: length of frame: 1.7 msec
 tap weights: "EE" (hex)

Bottom trace: edge detection
 vertical scale: 0.5 volts/division
 horizontal scale: length of frame: 6.3 msec
 tap weights: bias: "DC" (hex)
 FE, FE, FE, 00, FE, FE, FE

cost would be justified in very specific applications where speed and versatility are of prime concern. However, the unit price would probably go down drastically with mass production. Second, the resolution of the prototype CCD image processor used in this study is not good. Improvement in the optical system is required for better performance.

4.4.2 Bar code reader

The previous examples showed how the CCD image processor could be used in industrial applications where one-dimensional parameters are to be monitored. The next example illustrates other industrial applications in which the main objective of the processor is to read a bar code and match a given pattern with a set of fixed ones. Such a reader would be very useful in retail stores and supermarkets.

Most food products in supermarkets are labelled with a serial number called the Universal Product Code (UPC), which consists of a series of black bars of various widths on a white background. The serial numbers are useful to the producer and the government as a tool in food quality control. The supermarket chains are not very much concerned with them and do not have automatic decoding facilities for these serial numbers.

In a retail store or supermarket, the price of each item could be encoded in a similar manner, using black and white bars. These bars of various widths would in fact be an optical representation of a binary number, a black bar representing a low logic level and an empty space or white bar, a high logic level. A CCD image processor could be used in conjunction with a cash register to decode the price of every item and automatically add the bill.

This example is in fact an automation of cash registers in supermarkets or retail stores. The image processor attached to a cash register would "read" the code on the item label. To do so, a light source like a small laser beam would shine on the label and, by reflection, CCD photoelements would integrate light for the white portion of the label only. Using edge detection algorithms, the black bars could be identified by their edges. If the bar pattern were a binary representation of the price, digitization of the CCD output could automatically indicate the price in a binary form. A sophisticated cash register would take the digital output of the CCD and automatically add all binary numbers together. The total amount of the bill would be converted in decimal form and printed out or shown to the customer.

In this example, it is assumed that the bar pattern is directly changed into a binary representation of the price by the CCD and its peripherals. Another method could involve a search in a memory bank, containing a complete set of bar pattern edges, for the best match with the label bar pattern. The best match would indicate the item price, also stored in memory, in binary or decimal form.

This system, when compared to conventional cash registers, has some advantages and disadvantages too. First, it is faster than existing cash register systems in that the cashier just has to pass every item price label in front of the CCD. All decoding and adding operations are done internally at very high speed and the cashier does not have to press any keys to enter item prices in the register. Another advantage is a reduction in the amount of errors made. Considering human errors as an important source of errors in any hybrid system (humans and machines), a reduction of the cashier's task will improve overall performance.

The physical implementation of the price decoding system is the main drawback. Packaging of goods does not have to be changed but the CCD must be located so that it can read price labels on all types and all sizes of containers. The CCD focussing system must be good enough to correctly interpret a slightly misaligned label. A warning circuit with an LED could however be incorporated in the system to indicate to the operator an unfocussed label.

It should be noted that the image processor needed in the price decoding system does not have to be as complex as the system described in Chapter 3. Edge detection is the only type of processing done here. The microcomputer used in the experimental set up to determine sets of tap weights needed for several types of processing, can be replaced by a simple ROM containing the coefficients needed for edge detection. The circuit would also have to be slightly modified so that edge detection would be performed only once on each label and not continuously. The price decoder would be reset at every reading. An acknowledge line would also be useful to tell the cashier that the price has been recorded.

4.4.3 Frequency analysis of an image

In communications, the frequency spectrum of a signal is a major tool for analysis, transmission and storage of data. A large amount of equipment (hardware/software) is usually required to transform a time dependent signal into a frequency dependent one. In the case of a sampled time signal, a transform function called Discrete Fourier Transform (DFT) is used to execute the time to frequency conversion. The basic theory of DFT can be found in many text books dealing with the subject of digital signal processing [23, 24]. In recent years, special algorithms known as Fast Fourier Transforms (FFT) were developed to save processing time

when computing the Fourier transform of a time dependent signal using large computers. Nevertheless, these algorithms still require a lot of computer processing (CPU) time. This transformation is relatively expensive and it may not be processed in real-time.

A variation of the Fast Fourier Transform algorithm, called the chirp-z-transform (CZT) [25], can be easily implemented in hardware with CCD transversal filters [26]. Both FFT and CZT algorithms apply to a time-to-frequency conversion. In other words, the input signals are discrete (sampled analog) time signals and the output signals are frequency spectra of the inputs. However, the signals to be analysed in this study are images. Therefore, the variable parameter is not time but space. As discussed in Chapter 2, time defined functions can however be used in a CCD image sensor to process the converted image (image converted to a time dependent electrical signal in the CCD). The following application illustrates the implementation of DFT algorithms in the CCD image processor to obtain the (spatial) frequency spectrum of the image.

Referring to digital signal processing text books [23, 24], it can be seen that for a real and even discrete time signal, the frequency components are also real and even. The resulting frequency components $y(n)$ of the DFT are given by eqn. (4.3):

$$y(n) = \sum_{m=0}^{N-1} \cos \frac{2\pi mn}{N} x(m) \quad (4.3)$$

where the $x(m)$'s are the time dependent signal samples and the cosines are the coefficients or tap weights needed to execute the DFT. N is the total number of samples taken in the time domain, which is also equal to the total number of frequency components given by the DFT. N is 128

in this case because the CCD separates an image into 128 parts and each one is considered as a sample in the processing of the image. In other words, the continuous space defined image is treated as a continuous time signal. It is sampled and then processed exactly like a discrete time signal. Because both the time and frequency signals are real and even, it is necessary to calculate only the first 64 frequency components. The other ones will be their mirror image. The Discrete Fourier Transform is in fact reduced to a cosine transform. The cosines needed to compute these frequency components were calculated on a Sigma-9 computer.

Two experiments were conducted. In the first one, the image is a single rectangle and in the second one, it is made of two rectangles of the same size. For each case a computer simulation was run on the Sigma-9 computer and compared with the results obtained by the CCD image processor.

It should be noted that the output of the processor is valid only at every 128th sample of the sample-and-hold circuit at the CCD output. As explained in Chapter 2, the shift-and-add process of the CCD shift registers gradually computes a frequency component. The final value is obtained after 128 shifts, i.e.: when all CCD photoelements contribute to the output and this situation happens after 128 "add" operations.

The number of frequency components that can be computed in one run of the system depends on the size of the external RAM containing the tap weights required for DFT. The external memory consists of two Intel 2114 RAM's. Each has a storage capacity of 1024×4 bits. Thus, a maximum of eight frequency components can be computed on one run of the processor, each requiring 128 taps. It was mentioned in Chapter 2 that the use of a microcomputer with DMA facility would increase the computing capability of the CCD image processor. This system limitation is not

severe for the following two examples since the first eight frequency components contain most of the information necessary to define the image. For display purposes however, only four components were evaluated in one run of the processor or, in other words, four frames were displayed at once. It takes about 25 milliseconds to display four CCD frames and it is a convenient limit for sweep time on a CRT display.

The data collection system described in Chapter 3 was used in both experiments so that a hard copy of the digital approximated output could be compared with the computer simulation for each experiment. The following figures show, for each experiment, the computer simulation, the experimental results and a comparison between the expected results and the experimental ones.

To eliminate some of the noise due to the data collection system (spikes on the Gould 4000 scope display), it was necessary to take a few measurements of the analog to digital conversion results. By taking a few measurements and averaging them, this noise source becomes less important and a better estimation of the exact experimental frequency components is obtained.

From Tables 4.1 and 4.2, it can be seen that there is a relatively good agreement between computer simulation results and the experimental data. Normalized frequency component amplitudes match fairly well in most cases.

For better video display, it was necessary to evaluate only four frequency components at a time with the CCD image processor. This is why there are two pictures in Fig. 4.15 and in Fig. 4.18. The arrows in these pictures indicate the frequency component amplitudes, which appear at every 128th CCD output sample.

Fig. 4.13. Experiment one: DFT of a single rectangle image.
The image is shown in this figure. The CCD is operated in the camera mode.
The image consists of a centered rectangle that occupies 19 photoelements
in the CCD.

Vertical scale: 5 volts/division

horizontal scale: 0.6 msec/division

Figure 4.14. Experiment 1: DFT of a single rectangle. DFT, from computer simulation results

Vertical scale:
5 volts/division

Horizontal scale:
2 msec/division

(a)

Vertical scale:
2 volts/division

Horizontal scale:
1.5 msec/division

(b)

Fig. 4.15. Experiment one: DFT of a single rectangle image. The output waveform of the image processor shows the first four frequency components of the image in (a), and the next four in (b). Markers indicate the precise frequency component (1 sample every 128).

<u>FREQUENCY</u>	<u>AMPLITUDE</u>	
	<u>THEORETICAL</u>	<u>EXPERIMENTAL</u>
D.C.	1.00	1.00
FUNDAMENTAL	-0.96	-0.92
1st HARMONIC	0.88	0.84
2nd "	-0.76	-0.80
3rd "	0.60	0.60
4th "	-0.42	-0.72
5th "	0.24	0.12
6th "	-0.08	-0.32

Table 4.1. Experiment one: DFT of a single rectangle. The computer simulation results are compared with the experimental results. Frequency amplitudes are normalized. For better results, experimental results were taken several times and averaged. Normalized amplitudes range from a minimum of -1.0 to a maximum of +1.0.

Fig. 4.16. Experiment two: DFT of two rectangles. The image is shown in this figure. The CCD is operated in the camera mode. The image consists of two identical rectangles, occupying each 14 photoelements in the CCD and separated by 19 cells. The image is centered.

Vertical scale: 10 volts/division
horizontal scale: 0.5 msec/division

OF / DE

Fig. 4.17 Experiment 2: DFT of two rectangles.DFT, from computer simulation results

Vertical scale:
2 volts/division

Horizontal scale:
2 msec/division

(a)

Vertical scale:
2 volts/division

Horizontal scale:
1.5 msec/division

(b)

Fig. 4.18. Experiment two: DFT of two rectangles. The output waveform of the image processor shows the first four frequency components of the image in (a), and the next four in (b). Markers indicate the precise frequency component (1 sample every 128).

<u>FREQUENCY</u>	<u>AMPLITUDE</u>	
	<u>THEORETICAL</u>	<u>EXPERIMENTAL</u>
D.C.	1.00	1.00
FUNDAMENTAL	-0.72	-0.56
1st HARMONIC	0.20	0.26
2nd "	0.42	0.48
3rd "	-0.78	-0.92
4th "	0.72	0.72
5th "	-0.32	-0.42
6th "	-0.06	-0.14

Table 4.2. Experiment two: DFT of two rectangles. As in experiment one, experimental and theoretical normalized frequency amplitudes are compared. Normalized amplitudes range from a maximum value of +1.0 to a minimum value of -1.0.

In the two DFT experiments, the data collection circuit was used to digitize and store all 128 samples of a CCD frame. Although the first 127 samples are not valid frequency amplitudes, they are useful in evaluating the performance of the CCD image processor and in comparing with a computer simulation.

Finally, for both experiments, the calculated frequency components were used to perform an inverse DFT to reconstruct the image. The Sigma-9 computer was used to compute the inverse DFT for all sets of data: experimental and theoretical ones. The reconstructed images first illustrate the degree of agreement between theory and experimental results. They also show how accurate an image can be defined by its first eight frequency components.

From the reconstructed images (Fig. H.1 and H.2), it is seen that a good agreement exists between experimental and theoretical data. However, eight frequency components do not define an image very well. Sharpness would be improved by taking more frequency components and ripples in the signal would also be greatly reduced. Although high harmonics have relatively small amplitudes, they are useful in defining fine details of an image.

In conclusion, the CCD linear image processor can be successfully used in frequency analysis experiments. The inherent shift-and-add capability of a CCD imager makes the computation of frequency components of an image a fairly easy task.

CHAPTER 5

CONCLUSIONS

5.1 Summary and conclusions

The main objective of this thesis is essentially to prove the feasibility of a CCD linear image processor that uses integration time modulation to perform processing of an image. The shift-and-add capability of a CCD imager is a very powerful tool in implementing image processing algorithms in a CCD. Throughout the thesis, it was understood that images should be steady or at least slow moving so that spatially defined images could be converted in time dependent electrical signals for processing purposes in the CCD. Moving images, or scenes, would require a more complex CCD image processor that could process both the time and spatial features of a scene.

From the experimental results, it was concluded that the CCD image processor overall performance was limited mainly by the poor optical arrangement used in this work. Inherent CCD limitations, due to dark current, noise and transfer inefficiency, had little apparent effect. This would not be the case with the use of an upgraded optical apparatus and careful attention should then be paid to minimize CCD limitations. For example, the spatial resolution of the image processor could then be improved by using a CCD imager with smaller element-to-element spacing.

An improved optical system would increase the dynamic range of the image processor. Better results would be obtained at low light levels. Effects like the temperature dependence of the dynamic range via an increase of dark current with temperature, could be noticed. The average dark current and dark current level non uniformities have indeed

a strong temperature dependence that could be an important limiting factor at high temperatures.

Total power consumption of the image processor was not considered in this thesis. However, in applications where it is important to minimize power consumption, a careful choice of hardware components is necessary and low power devices should be used whenever possible.

Preliminary experiments demonstrated the feasibility of the CCD integration time modulation approach in image processing. Convolution and edge detection algorithms were successfully implemented using the CCD image processor. Specific applications were also discussed and experimentally verified. Reported results demonstrate the versatility and the potential of this system. Industrial applications are numerous in single parameter monitoring and bar code reading. Most important perhaps, is the potential applicability of the CCD image processor in complex image processing applications demonstrated by the image spatial frequency analysis.

The main advantage of this system over conventional digital image processing systems is that it is an "in situ" image processor. The CCD image processor has indeed the unique capability of looking at an image and processing it at the same time. Most conventional digital image processing systems first require the use of an optical device to look at an image and possibly record it, and, in a second step, image processing is done on the recorded image with a digital computer.

5.2 Suggestions for future work

The first improvement to be made on the CCD image processor was defined as an upgrading of the optical system. In a second step, future work could also be done on the CCD design itself in order to optimize it for image processing. For example, CCD shift registers could be built to

best handle the gradual increase in charge packets size as they are shifted towards the output stage.

Instead of using a general purpose CCD imager in the image processing system, CCD's could also be designed for specific image processing applications. High speed devices could be used in fast processing applications to achieve real-time image processing; low light level and infrared CCD's could be very useful in military surveillance applications.

Future work could also be done to extend the integration time modulation approach in CCD image processing to two-dimensional cases. 2-D images could then be processed by a CCD linear image processor and a scanning mirror arrangement or by a 2-D CCD imager.

Studies have been done on 2-D image processing using CCD's [27]. However, the devices used are signal processing CCD's and not image sensors. There is a need for a separate imaging device to first store the image and then send it to the processor. Therefore, an "in situ" 2-D CCD image processor based on integration time modulation, has more potential for fast image processing.

Many military applications of a 2-D CCD image processor can be foreseen. Plans are already made in the USA to develop an artillery-launched television target location system using a CCD TV camera, which would be the only system capable of consistently surviving the high setback acceleration when the shell is fired [28]. The use of a CCD image processor could enhance the potential of this system by providing an extra capability for target identification (based on physical parameters).

Another application of the CCD technology consisting of a tactical fighter aircraft mounted CCD camera is to provide gunsight image recording of combat and training operations [28]. The CCD camera offers

many advantages over the traditional 16 mm. film cameras: immediate access to data, smaller size and more recording capability. The use of a CCD image processor would provide extra monitoring capability to the system.

Target location and identification, monitoring of 2-D parameters and spatial surveillance are a few of the many areas of applicability of a 2-D CCD image processor based on integration time modulation.

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APPENDIX A

CIRCUIT DIAGRAM OF THE CCD IMAGE PROCESSOR

RAMP CIRCUIT

APPENDIX B

CGD 110F SPECIFICATION SHEETS

CCD110/110F

256-ELEMENT LINEAR IMAGE SENSOR

GENERAL DESCRIPTION — The CCD110/110F are monolithic self-scanned 256-Element Image Sensors designed for optical character recognition and other high sensitivity, high speed imaging applications.

The device contains a row of 256 sensing elements that accept light photons and converts them to electrical charge packets.

In addition to a row of 256 sensing elements, the CCD110/110F chips include two charge transfer gates, two 2-phase analog shift registers, an output charge detector/preamplifier and a compensation output amplifier. The 2-phase analog shift registers both feed the input of the charge detector resulting in sequential reading of the 256 imaging elements.

The cell size is 13μ (0.51 mil) by 17μ (0.67 mil) on 13μ (0.51 mil) centers. The device is manufactured using Fairchild charge coupled device buried channel technology.

- DYNAMIC RANGE TYPICAL: 500 TO 1 (PEAK TO PEAK), 2500 TO 1 (RMS)
- 256 ELEMENTS ON A SINGLE CHIP
- ON-CHIP PREAMPLIFIER AND COMPENSATION AMPLIFIER
- LOW POWER REQUIREMENTS
- ALL OPERATING VOLTAGES UNDER 15 V
- PACKAGED IN 18-PIN DUAL IN-LINE PACKAGE
- LOW NOISE EQUIVALENT EXPOSURE
- WIDE RANGE OF VIDEO DATA RATE
- DIMENSIONALLY PRECISE PHOTOSITE SPACING

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-25°C to 100°C
Operating Temperature	-25°C to 55°C
Clock Inputs, Pins 2, 3, 4, 5, 6, 7, 10, 12, 13, 14, 15	-0.3 V to 12 V
Pins 1, 8, 11, 16, 17, 18	-0.3 V to 18 V

Caution: The device has limited built-in gate protection. It is recommended to control and minimize static charge build up. Care should be taken to avoid shorting pins OS and CS to ground during operation of the device.

FUNCTIONAL DESCRIPTION – The CCD110/110F consists of the following functional elements illustrated in the Block Diagram

Image Sensor Elements – A row of 256 Image sensor elements separated by diffused channel stops and covered by a silicon photogate. Image photons pass through the transparent polycrystalline silicon photogate and are absorbed in the single crystal silicon by hole-electron pair production. The photon generated electrons are accumulated in the photosites. The amount of charge accumulated is a linear function of the incident illumination intensity and the integration period. The output signal will vary in this analog manner from a thermally generated noise background at zero illumination to a maximum at saturation.

Two Transfer Gates – Gate structures adjacent to the row of Image Sensor Elements. The charge packets accumulated in the image sensor elements are transferred out via the transfer gates to the transport registers. Alternating charge packets are transferred to the right and left (A and B) analog transport shift registers. The HIGH states of the transfer gates must be contained by the HIGH state of the transport shift register clocks. The next light integration period is started when transfer gates go LOW.

Two 130-Bit Analog Shift Registers – One on each side of the row of Image Sensor Elements and separated from it by a Transfer Gate. The two registers are used to move the image generated charge packets serially from the sensor elements to the charge detector/preamplifier. The phase relationship of the last elements of the two shift registers provide for alternate delivery of charge packets to re-establish the serial sequence of the photosites.

A Gated Charge Detector/Preamplifier – Charge packets are transported to a precharged diode whose potential changes linearly in response to the quantity of the signal charge delivered. This potential is applied to the gate of the output n channel MOS transistor producing a signal output at OS. The reset transistor is driven by a reset clock (QR) so as to recharge the charge detector diode capacitance before the arrival of each new signal charge packet from the transport registers.

Generation of the necessary waveforms to operate the device is explained in detail in the CCD110/110F Board Brochure that includes a typical drive circuit diagram, a printed copy of the layout of a two-sided PC board, a parts list of components that are needed to build the board and oscilloscope photographs of the driving waveforms.

DEFINITION OF TERMS

Charge Coupled Device – A charge coupled device is a semiconductor device in which isolated charge packets are transported from one position in the semiconductor to an adjacent position by sequential clocking of an array of gates. The charge packets are minority carriers with respect to the semiconductor substrate.

Transfer Gate Clock ϕ_XA , ϕ_XB – The voltage waveform applied to the transfer gate to move the accumulated charge from the image sensor elements to the CCD shift registers.

Analog Shift Register Transport Clocks, ϕ_1A , ϕ_2A , ϕ_1B , ϕ_2B – The two sets of 2 phase clock applied to the gates of the CCD shift registers to move the charge packets received from the image sensor elements to the gated charge detecting preamplifier.

Gated Charge Detector Preamplifier – The output circuit of the CCD110/110F which receives the charge packets from the CCD shift registers and provides a signal voltage proportional to the size of each charge packet. Before each new charge packet is sensed, a reset clock returns the output voltage to a base level.

Reset Clock QR – The voltage waveform required to drive the gated charge detector preamplifier.

Dynamic Range – The saturation exposure divided by the peak to peak noise equivalent exposure.

This does not take into account dark signal non uniformities or average dark signal.

Dynamic range is sometimes defined in terms of rms noise. To compare the two definitions a factor of 4 to 6 is generally appropriate. (Peak to peak noise is approximately equal to 4 to 6 times rms noise.)

DEFINITION OF TERMS (Cont'd)

Peak to Peak Noise Equivalent Exposure — The exposure level which gives an output signal equal to the peak to peak noise level at the output in the dark.

Saturation Exposure — The minimum exposure level that will produce a saturated output signal. Saturation exposure is equal to the light intensity times the photosite integration time.

Spectral Response Range — The spectral band in which the response per unit of radiant power is more than 10% of the peak response.

Responsivity — The output signal voltage per unit exposure for a specified spectral type of radiation. Responsivity equals output voltage divided by exposure level.

Photoresponse Non-uniformity — The difference of the response levels of the most and the least sensitive element under uniform illumination. This is commonly expressed as a percentage of the saturation output voltage.

Average Dark Signal — The output signal level in the dark averaged over all elements and measured relative to the base line output voltage established by the reset clock. This is a linear function of the integration time. It is also strongly dependent on temperature. This is commonly expressed as a percentage of the saturation output voltage.

Dark Signal Non-uniformity — Maximum deviation of the output voltage of any element from the background level in the dark. This is commonly expressed as a percentage of the saturation output voltage.

Saturation Output Voltage — The maximum signal output voltage.

Integration Time — The time interval between the falling edges of any transfer pulse ϕ_{XA} and ϕ_{XB} as shown in the timing diagram. The integration time is the time allowed for the photosites to collect charge.

Output Signal Range — The output signal range is defined as $OSR = V_{sat} - (t_{INT} + t_{Transfer}) \times \text{Rate of Average Dark Signal}$ where t_{INT} = Integration Time, $t_{Transfer}$ = time necessary to transfer the charge packets from the analog shift registers and is equal to $\frac{260}{f_{DR}}$. Integration time (t_{INT}) does not necessarily equal transfer time ($t_{Transfer}$). If long integration times are required, $t_{Transfer}$ should be minimized (increase f_{DR}) to maximize OSR.

TEST LOAD CONFIGURATION

Fig. 1

DC CHARACTERISTICS, $T_A = 25^\circ\text{C}$

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP	MAX		
V_{OD}	Output Transistor Drain Voltage	14.5	15.0	15.5	V	
V_{RD}	Reset Transistor Drain Voltage	14.5	15.0	15.5	V	
V_{OG}	Output Gate Voltage		6.0			Note 1
V_{PG}	Photogate Voltage		9.0		V	Note 2
TP1, TP3	Test Points		0.0		V	
TP2, TP4	Test Points	14.5	15.0	15.5	V	

CLOCK CHARACTERISTICS $T_A = 25^\circ\text{C}$

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP	MAX		
$V_{\phi 1AL}$ $V_{\phi 1BL}$ $V_{\phi 2AL}$ $V_{\phi 2BL}$	Analog Shift Register Transport Clocks LOW	0.0	0.5	0.8	V	Notes 3 4
$V_{\phi 1AH}$ $V_{\phi 1BH}$ $V_{\phi 2AH}$ $V_{\phi 2BH}$	Analog Shift Register Transport Clocks HIGH		8.0			Notes 3 4 12
$V_{\phi XAL}$	Transfer Gate Clock LOW	0.0	0.5	0.8	V	Notes 3 4
$V_{\phi XAH}$	Transfer Gate Clock HIGH		8.0		V	Notes 3 4 12
$V_{\phi RL}$	Reset Clock LOW	0.0	0.5	0.8	V	Notes 3 4
$V_{\phi RH}$	Reset Clock HIGH		10.0		V	
$f_{\phi 1A}$ $f_{\phi 1B}$ $f_{\phi 2A}$ $f_{\phi 2B}$	Analog Shift Register Transport Clock Frequency		5.0		MHz	Notes 5 6
$f_{\phi R}$	Reset Clock Frequency (Output Bit Rate)		1.0		MHz	Notes 5 6

AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$ $f_{\phi 1} = f_{\phi 2} = 2.5\text{ MHz}$ $f_{\phi R} = 5\text{ MHz}$ $t_{INT} = 275\text{ }\mu\text{s}$ $t_{TRANSFER} = 260\text{ }\mu\text{s}$

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP	MAX		
DR	Dynamic Range	250	500			Notes 7 8 9
NEE	Peak-to-Peak Noise $\times$ Exposure		1×10^{-3}		$\mu\text{J}/\text{cm}^2$	Notes 8 9
SE	Saturation Exposure		0.5		$\mu\text{J}/\text{cm}^2$	Notes 8 9
SR	Spectral Response Range Limits		0.45-1.05		μm	
R	Responsivity		0.4		$\text{V per } \mu\text{J}/\text{cm}^2$	Note 13
PRNU	Photoresponse Non-uniformity		± 4	± 6	% of V_{sat}	Note 10
ADS	Average Dark Signal		0.25	1.25	% of V_{sat}	
DSNU	Dark Signal Non-uniformity		0.5	2.5	% of V_{sat}	
V_{sat}	Saturation Output Voltage	100	200		mV	Note 11
P	Power Dissipation		100		mW	$V_{DD} = 15\text{ V}$
Z	Output Impedance		1000		Ω	
N	Peak to Peak Noise		400		μV	
RDS	Rate of Average Dark Signal		2		mV/ms	

NOTES

- Adjustment in the range of 4 V to 8 V may be required for optimum operation.
- Adjustment in the range of 5 V to 12 V may be required for optimum operation.
- Negative transients on the clocks below 0.0 V may cause an increase in apparent dark signal.
- $C_{AXA} = C_{AXB} = C_{\phi 1A} = C_{\phi 1B} = C_{\phi 2A} = C_{\phi 2B} = 50\text{ pF}$; $C_{\phi R} = 15\text{ pF}$.
- The resulting data output frequency f_{DO} is twice that of each analog shift register clock $f_{\phi 1A}$, $f_{\phi 2A}$, $f_{\phi 1B}$, $f_{\phi 2B}$.
- Clock rates shown are typical rates at which the device operates. Operation of the devices at lower or higher frequencies will not damage the device.
- $t_{INT} =$ integration time $= 275\text{ }\mu\text{s}$.
- The dynamic range is measured by taking the ratio of the saturation output voltage to the peak to peak noise of the device in the dark. Because of the high degree of linearity of the device the dynamic range measurement is also approximately equal to the ratio of the saturation exposure to the peak to peak noise (equivalent) exposure.
 $1\text{ }\mu\text{J}/\text{cm}^2 = 0.02\text{ fcs at } 2854\text{ K}$; $1\text{ fcs} = 50\text{ }\mu\text{J}/\text{cm}^2\text{ at } 2854\text{ K}$.
- Measurement is done at 50% of saturation output level. Measurement excludes first and last elements.
- See Fig. 1 for test load configuration.
- Adjustment in the range of 5 V to 10 V may be required for optimum operation.
- See definition of terms.

OUTPUT SIGNAL LEVEL VS INTEGRATION TIME
28540K TUNGSTEN SOURCE

Fig. 2

PHOTOELEMENT DIMENSIONS

All dimensions are typical values

Fig. 3

TIMING DIAGRAM DRIVE SIGNALS

Fig. 4

APPENDIX C

INTEL PROMPT 48 SPECIFICATION SHEETS

8048/8748/8035

SINGLE COMPONENT 8-BIT MICROCOMPUTER

- *8048 Mask Programmable ROM
- *8748 User Programmable/Erasable EPROM
- *8035 External ROM or EPROM

- 8-Bit CPU, ROM, RAM, I/O in Single Package
- Interchangeable ROM and EPROM Versions
- Single 5V Supply
- 2.5 μ sec and 5.0 μ sec Cycle Versions
- All Instructions 1 or 2 Cycles.
- Over 90 Instructions: 70% Single Byte
- 1K x 8 ROM/EPROM
- 64 x 8 RAM
- 27 I/O Lines
- Interval Timer/Event Counter
- Easily Expandable Memory and I/O
- Compatible with 8000 Series Peripherals
- Single Level Interrupt

The Intel® 8048/8748/8035 is a totally self-sufficient 8-bit parallel computer fabricated on a single silicon chip using Intel's N-channel-silicon gate MOS process.

The 8048 contains a 1K x 8 program memory, a 64 x 8 RAM data memory, 27 I/O lines and an 8-bit timer/counter in addition to on-board oscillator and clock circuits. For systems that require extra capability, the 8048 can be expanded using standard memories and MCS-80™ (8080A) peripherals. The 8035 is the equivalent of an 8048 without program memory. The 8035L has the RAM Power down mode of the 8048, while the 8035 does not.

To reduce development problems to a minimum and provide maximum flexibility, three interchangeable pin-compatible versions of this single component microcomputer exist: the 8748 with user-programmable and erasable EPROM program memory for prototype and preproduction systems; the 8048 with factory-programmed mask ROM program memory for low-cost high volume production; and the 8035 without program memory for use with external program memories.

This microprocessor is designed to be an efficient controller as well as an arithmetic processor. The 8048 has extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and no instructions over two bytes in length.

PIN CONFIGURATION

LOGIC SYMBOL

BLOCK DIAGRAM

PIN DESCRIPTION

Designation	Pin #	Function
V _{SS}	20	Circuit GND potential
V _{DD}	26	Programming power supply. +25V during program, +5V during operation for both ROM and PROM. Low power standby pin in 8048 ROM version.
V _{CC}	40	Main power supply. +5V during operation and programming
PROG	25	Program pulse (+25V) input pin during 8748 programming. Output strobe for 8243 I/O expander
P10-P17 Port 1	27-34	8-bit quasi bidirectional port
P20-P27 Port 2	21-24 35-38	8-bit quasi bidirectional port P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243
DB ₀ -DB ₇ BUS	12-19	True bidirectional port which can be written or read synchronously using the RD, WR strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of PSEN. Also contains the address and data during an external RAM data store instruction, under control of ALE, RD, and WR
T0	1	Input pin testable using the conditional transfer instructions JTO and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction. T0 is also used during programming.
T1	39	Input pin testable using the JT1 and JNT1 instructions. Can be designated the timer counter input using the STRT CNT instruction
INT	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low)

Designation	Pin #	Function
RD	8	Output strobe activated during a BUS read. Can be used to enable data onto the BUS from an external device. Used as a Read Strobe to External Data Memory (Active low)
RESET	4	Input which is used to initialize the processor. Also used during PROM programming verification, and power down (Active low) (Non TTL V _{IH})
WR	10	Output strobe during a BUS write (Active low) Used as write strobe to External Data Memory
ALE	11	Address Latch Enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory
PSEN	9	Program Store Enable. This output occurs only during a fetch to external program memory (Active low)
SS	5	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction. (Active low)
EA	7	External Access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification. (Active high)
XTAL1	2	One side of crystal input for internal oscillator. Also input for external sources (Non TTL V _{IH})
XTAL2	3	Other side of crystal input.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin With Respect to Ground	-0.5V to +7V
Power Dissipation	1.5 Watt

COMMENT

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. AND OPERATING CHARACTERISTICS $T_A = 0^\circ\text{C to } 70^\circ\text{C}$, $V_{CC} = V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
V_{IL}	Input Low Voltage (All Except XTAL1, XTAL2)	-5		8	V	
V_{IH}	Input High Voltage (All Except XTAL1, XTAL2, RESET)	2.0		V_{CC}	V	
V_{IH1}	Input High Voltage (RESET XTAL1)	3.0		V_{CC}	V	
V_{OL}	Output Low Voltage (BUS, RD, WR, PSEN, ALE)			45	V	$I_{OL} = 2.0\text{mA}$
V_{OL1}	Output Low Voltage (All Other Outputs Except PROG)			45	V	$I_{OL} = 1.6\text{mA}$
V_{OL2}	Output Low Voltage (PROG)			45	V	$I_{OL} = 1.0\text{mA}$
V_{OH}	Output High Voltage (BUS, RD, WR, PSEN, ALE)	2.4			V	$I_{OH} = 100\mu\text{A}$
V_{OH1}	Output High Voltage (All Other Outputs)	2.4			V	$I_{OH} = 50\mu\text{A}$
I_{IL}	Input Leakage Current (T1, EA, INT)			10	μA	$V_{SS} < V_{IN} < V_{CC}$
I_{OL}	Output Leakage Current (Bus, T0) (High Impedance State)			10	μA	$V_{CC} > V_{IN} > V_{SS} + 45$
I_{DD}	V_{DD} Supply Current		10	20	mA	
$I_{DD} + I_{CC}$	Total Supply Current		65	135	mA	

A.C. CHARACTERISTICS $T_A = 0^\circ\text{C to } 70^\circ\text{C}$, $V_{CC} = V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

Symbol	Parameter	8048/8748 8035/8035L		8748-8 8035-8		Unit	Conditions (Note 1)
		Min.	Max.	Min.	Max.		
t_{LL}	ALE Pulse Width	400		600		ns	
t_{AL}	Address Setup to ALE	150		150		ns	
t_{LA}	Address Hold from ALE	80		80		ns	
t_{CC}	Control Pulse Width (PSEN, RD, WR)	900		1500		ns	
t_{OW}	Data Set-Up Before WR	500		640		ns	
t_{WD}	Data Hold After WR	120		120		ns	$C_L = 20\text{pF}$
t_{CY}	Cycle Time	2.5	15.0	4.17	15.0	μs	6 MHz XTAL (3.6 MHz XTAL for -8)
t_{DH}	Data Hold	0	200	0	200	ns	
t_{RD}	PSEN, RD to Data In		500		750	ns	
t_{AW}	Address Setup to WR	230		260		ns	
t_{AD}	Address Setup to Data In		950		1450	ns	
t_{AFC}	Address Float to RD, PSEN	0		0		ns	

Note 1: Control Outputs $C_L = 80\text{ pF}$
 BUS Outputs $C_L = 150\text{ pF}$

$t_{CY} = 2.5\mu\text{s}$ *Standard 8748 and 8035 - 5%, 10% available

WAVEFORMS

INSTRUCTION FETCH FROM EXTERNAL PROGRAM MEMORY

READ FROM EXTERNAL DATA MEMORY

WRITE TO EXTERNAL DATA MEMORY

A.C. CHARACTERISTICS

T_A 0°C to 70°C V_{CC} = 5V±10%

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t _{CP}	Port Control Setup Before Falling Edge of PROG	110		ns	
t _{CC}	Port Control Hold After Falling Edge of PROG	140		ns	
t _{PR}	PROG to Time P2 Input Must Be Valid	910		ns	
t _{OP}	Output Data Setup Time	220		ns	
t _{OH}	Output Data Hold Time	65		ns	
t _{PI}	Input Data Hold Time	110		ns	
t _{PP}	PROG Pulse Width	1510		ns	
t _{PL}	Port 2 I/O Data Setup	400		ns	
t _{HP}	Port 2 I/O Data Hold	150		ns	

PORT 2 TIMING

AC TIMING SPECIFICATION FOR PROGRAMMING

 $T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$, $V_{DD} = 25\text{V} \pm 1\text{V}$

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{AS}	Address Setup Time to $\overline{\text{RESET}}$	41cy			
t_{AH}	Address Hold Time After $\overline{\text{RESET}}$	41cy			
t_{DS}	Data In Setup Time to PROG	41cy			
t_{DH}	Data In Hold Time After PROG	41cy			
t_{PH}	$\overline{\text{RESET}}$ Hold Time to Verify	41cy			
t_{VDDW}	V_{DD}	41cy			
t_{VDDH}	V_{DD} Hold Time After PROG	0			
t_{PW}	Program Pulse Width	50	60	MS	
t_{TW}	Test 0 Setup Time for Program Mode	41cy			
t_{WT}	Test 0 Hold Time After Program Mode	41cy			
t_{DO}	Test 0 to Data Out Delay		41cy		
t_{WW}	$\overline{\text{RESET}}$ Pulse Width to Latch Address	41cy			
t_r, t_f	V_{DD} and PROG Rise and Fall Times	0.5	2.0	μs	
t_{CY}	CPU Operation Cycle Time	5.0		μs	
t_{RE}	$\overline{\text{RESET}}$ Setup Time Before EA	41cy			

Note: If Test 0 is high t_{DO} can be triggered by $\overline{\text{RESET}}$.

DC SPECIFICATION FOR PROGRAMMING

 $T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$, $V_{DD} = 25\text{V} \pm 1\text{V}$

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{DDH}	V_{DD} Program Voltage High Level	24.0	26.0	V	
V_{DDL}	V_{DD} Voltage Low Level	4.75	5.25	V	
V_{PH}	PROG Program Voltage High Level	21.5	24.5	V	
V_{PL}	PROG Voltage Low Level		0.2	V	
V_{EAH}	EA Program or Verify Voltage High Level	21.5	24.5	V	
V_{EAL}	EA Voltage Low Level		5.25	V	
I_{DD}	V_{DD} High Voltage Supply Current		30.0	mA	
I_{PROG}	PROG High Voltage Supply Current		16.0	mA	
I_{EA}	EA High Voltage Supply Current		1.0	mA	

WAVEFORMS

COMBINATION PROGRAM/VERIFY MODE (EPROM'S ONLY)

VERIFY MODE (FROM EPROM)

NOTES

1. $PROG$ MUST FLOAT IF EA IS LOW (i.e., +25V) OR IF $\overline{TO} = 5V$ FOR THE 8741. FOR THE 8041 $PROG$ MUST ALWAYS FLOAT.
2. V_{EAS} FOR 8041 = 11.4V MIN. 12.8V MAX.
3. THE FOLLOWING CONDITIONS MUST BE MET:
 $CS = TTL\ 1$
 $AO = TTL\ 0$
 THIS CAN BE DONE USING 10K RESISTORS TO V_{CC} , V_{EE} RESPECTIVELY.
4. X_1 AND X_2 DRIVEN BY 3 MHz CLOCK WILL GIVE 5 μ SEC t_{CY} . THIS IS GOOD FOR 8 PARTS AS WELL AS NON-8 PARTS.

The 8748 EPROM can be programmed by either of two Intel products

1. PROMPT-48 Microcomputer Design Aid
2. Universal PROM Programmer (UPP-101 or UPP-102) peripheral of the Inteltec® Development System with a UPP-848 Personality Card

APPENDIX D

EXAMPLES OF TAP WEIGHT GENERATION PROGRAMS

As discussed in Chapter 3, an Intel PROMPT 48 microcomputer is used to generate all necessary tap weights needed to control CCD driving clock waveforms for various image processing applications. The microcomputer also controls the access to an external RAM, containing the required set of tap weights for a specific application. In a first step of any image processing application, the PROMPT 48 fills the RAM with proper tap weights. In a second step, the PROMPT 48 is disabled from the circuit and the hardware circuitry (clock generation circuit) reads the RAM sequentially and generates CCD driving clock waveforms according to the tap weights.

To access any peripheral circuitry, the PROMPT 48 has two input-output (I/O) ports and a BUS port. I/O port 1 brings the address lines to the external RAM while I/O port 2 brings the data lines. Some lines of the BUS port are assigned to special control functions.

PORT 1 LINE 0: TO RAM ADDRESS LINE 0 (LSB)

1:	"	"	"	"	1
2:	"	"	"	"	2
3:	"	"	"	"	3
4:	"	"	"	"	4
5:	"	"	"	"	5
6:	"	"	"	"	6
7:	"	"	"	"	7 (MSB)

PORT 2 LINE 0: TO RAM DATA LINE 0 (LSB)

1:	"	"	"	"	1
2:	"	"	"	"	2
3:	"	"	"	"	3
4:	"	"	"	"	4
5:	"	"	"	"	5
6:	"	"	"	"	6
7:	"	"	"	"	7 (MSB)

BUS LINE 0: to control tri-state buffers for
selecting proper address for the RAM.

It is HIGH when the PROMPT 48 has
access to the RAM

1: to control the $R/\overline{W}$ line of the RAM.

It is HIGH when the RAM is in READ
mode and LOW when it is in WRITE mode.

4: to control the operation mode of the
image processor when it is HIGH, the
camera mode is selected. When it is
LOW, the processing mode is selected.
This line also controls the selection
of ϕ_T (which is different for camera
and processing modes).

Two examples of programs that generate the appropriate tap
weights for specific image processing applications, are given: one for
the camera mode of operation and one for an edge detection. Flow diagrams
and program listings are given.

EXAMPLE 1: CAMERA MODE

FLOW DIAGRAM

EXAMPLE 1: CAMERA MODE

PROGRAM

	Assembly Language	Machine Language	Comments
START	MOV A,#01	23 01	; to disable address counter and
	OUTL BUS,A	02	put the R/w line in the "write" mode
	MOV R2,#7F	BA 7F	; R2 contains the RAM address
LOOP 1	MOV A,R2	FA	
	OUTL P1,A	39	
	MOV A,#F9	23 F9	; "F9" is the data to be sent into
	OUTL P2,A	3A	the RAM at the address contained in R2
	DJNZ R2 LOOP 1	EA LOOP 1	
	MOV A,#00	23 00	: to send the same tap weight (F9)
	OUTL P1,A	39	to address 00 because the loop stops
	MOV A,#F9	23 F9	at address 01 (does not do 00)
	OUTL P2,A	3A	
	MOV A,#03	23 03	; to put the RAM in the READ mode
	OUTL BUS,A	02	
	MOV A,#FF	23 FF	
	OUTL P1,A	39	; to disable the ports. They are put
	OUTL P2,A	3A	in a tri-state (all lines high) mode
	MOV A,#12	23 12	; to enable the address counter: it
	OUTL BUS,A	02	resumes control of the RAM.
	JMP BACK	24 BACK	

EXAMPLE 2: PROCESSING MODE: EDGE DETECTION

FLOW DIAGRAM

EXAMPLE 2: PROCESSING MODE: EDGE DETECTION

PROGRAM

Assembly Language	Machine Language	Comments
START MOV A,#01	23 01	; to disable the address counter and put
OUTL BUS,A	02	the R/ $\overline{w}$ line in the "WRITE" mode
MOV A,#00	23 00	; to send the same tap weight (D8) to
OUTL P1,A	39	address 00, the following loop sending
MOV A,#D8	23 D8	it to addresses 0 to 7F
OUTL P2,A	3A	
MOV R2,#7F	BA 7F	; R2 contains the RAM address
LOOP: MOV A,R2	FA	
OUTL P1,A	39	
MOV A,#D8	23 D8	; D8: tap weight representing bias level
OUTL P2,A	3A	
DJNZ R2,LOOP	EA LOOP	
MOV A,#03	23 03	; to put the RAM in the "READ" mode;
OUTL BUS,A	02	otherwise some "garbage" could get in
MOV R3#05	BB 05	; five tap weights are special; they are
MOV R5,#10	BD 10	used for edge detection; they are
		stored in locations 10 to 14
ENC: MOV A,R5	FD	
OUTL P1,A	39	
MOV A,#01	23 01	
OUTL BUS,A	02	
MOV A,#FE	23 FE	; FE is the tap weight value representing
OUTL P2,A	3A	-1/4
MOV A,#03	23 03	
OUTL BUS,A	02	
INC R5	1D	
DJNZ R3	EB ENC	
MOV A,#12	23 12	
OUTL P1,A	39	
MOV A,#01	23 01	
OUTL BUS,A	02	
MOV A,#2B	23 2B	; 2B is the tap weight representing 1
OUTL P2,A	3A	
MOV A,#03	23 03	
OUTL BUS,A	02	
MOV A,#FF	23 FF	; to disable the ports. The address
OUTL P1,A	39	counter takes over
OUTL P2,A	3A	
MOV A,#02	23 02	; to enable the address counter and keep
OUTL BUS,A	02	the RAM in the "read" mode
BACK JMP BACK	24 BACK	

APPENDIX E

DATA COLLECTION SYSTEM SOFTWARE CONTROL

Following is a flow diagram and a program listing of the program used in the INTEL SDK-85 to control the data collection system. It basically interfaces the offset binary data coming out of a Gould 4000 oscilloscope with a teletype, in order to obtain a hard copy.

ADDRESS	DATA OR INSTRUCTION	LABEL	MEMORIC	COMMENT
2 0.0.0	3.1		SET SP, 2008	STACK POINTER SET
1.1	1.8			
1.2	1.0			
1.3	1.5		MVE A, 08	INTERUPT MASK SET
1.4	0.8			
1.5	1.0		SIM	
1.6	1.21		LXI H, 1ST	REGISTER PAIR H HOLDS MEMORY ADDRESS
1.7	0.0			WHERE FIRST INTR DATA WILL BE
1.8	1.28			PLACED
1.9	1.6		MVE D, 02	SET RAM COUNTER
1.A	0.2			
1.B	1.5		ET	ENABLE INTERRUPT FROM GROUND SC-70
1.C	0.0	LOOP	NOP	WAIT FOR INTERRUPT
1.D	1.3		JMP LOOP	
1.E	0.0			
1.F	2.0			
1.0	3.5	TSR	MVE A, 00	SET INPUT PORT TO READ IN 8 BITS
1.1	0.0			
1.2	0.3		CIT02	
1.3	0.2			
1.4	0.0		IN 00	READ IN 8 BIT BYTE
1.5	0.0			
1.6	0.6		SUB 7F	SUBTRACT OFFSET
1.7	1.5			
1.8	1.2		JP PS	IF RESULT IS POSITIVE JUMP
1.9	1.0			
1.A	2.0			
1.B	2.5		CMA	TAKE INVERSE OF ALL BITS
1.C	4.5	PS	MOV A, A	STORE DATA TEMPORARILY
1.D	5.6		ANI 0F	DATAIN FOUR LSBS
1.E	0.5			
1.F	1.6		ADI 00	CLEAR CARRY FLAG
2.0	0.0			
1.1	2.7		DAA	CONVERT FOUR LSBS TO BCD
1.2	4.5		MOV B, A	STORE BCD DATA TEMPORARILY
1.3	3.9		MOV A, C	RECALL FULL DATA BYTE
1.4	5.6		ANI 0A	OBTAIN FOUR MSBS
1.5	1.0			
1.6	0.5		RRC	
1.7	0.5		RRC	
1.8	0.5		RRC	
1.9	0.5		RRC	
2 0.2.1	5.5		PSH H	ADDRESS LST PUSHED ON STACK

ADDRESS	DATA OR INSTRUCTION	LABEL	MEMORIC	COMMENT
2 0.2B	2.1		LXI H, BASE	ADDRESS "BASE" READ IN REGISTER PAIR H
1.5C	5.2			
1.4D	2.0			
1.6E	5.2	COUNT	DCR A	ONE SUBTRACTED FROM MODIFIED
1.7F	5.2		JM ADD	IF FOUR MSBs OF RESULT NEGATIVE
1.3.0	3.6			GO TO ADD, OTHERWISE
1.1	2.0			
1.2	2.3		INX H	CHANGE POSITION ON LOOK-UP TABLE
1.3	5.3		JMP COUNT	LOOP UNTIL HAVE DECREMENTED
1.4	2.6			MODIFIED FOUR MSBs TO
1.5	2.0			NEGATIVE ONE
1.6	7.6	ADD	MOV A, M	MOVE CONTENTS OF ADDRESS IN
1.7	8.2		ADD B	REGISTER H TO ACCUMULATOR
1.8	6.6		ADDC	AND ADD 6CD FOUR LSBs TO
1.9	0.0			ACCUMULATOR
1.A	2.7		JAA	IF CARRY CONVERT OFFSET BINARY
1.B	5.1		POP H	TO DEC
1.C	7.7		MOV M, A	STORE RD IN MEMORY
1.D	7.5		PUSH B	
1.E	DS		PUSH D	
1.F	5.5		PUSH H	
1.0	5.5		PUSH B0	
1.1	5.2		CALL UPDOT	
1.2	6.5			
1.3	9.3			
1.4	1.1		LXI B, 0040	Keyboard display button
1.5	4.6			
1.6	0.0			
1.7	6.7		CALL DELAY	
1.8	5.1			
1.9	0.5			
1.A	5.1		POP PSW	
1.B	5.1		" H	
1.C	2.1		" D	
1.D	6.1		" B	
1.E	2.2		INX H	Increment for next storage location
1.F	2.0		MOVA, L	Check to see if RAM address is
1.5.0	2.6		SUI 80	
1.1	9.0			
1.2	6.2		JNZ CONT1	Not jump, TURN TO CONT1, OTHERWISE
1.3	5.2			
1.4	2.0			
2 0.5.5	1.5		DCR D	DECREMENT RAM COUNT

APPENDIX F

DFT COEFFICIENTS CALCULATION

As mentioned in Chapter 4, the images used in the frequency analysis experiments are all real and centered. Therefore, frequency components will be real and even and they are given by:

$$y(n) = \sum_{m=0}^{N-1} \cos \frac{2\pi mn}{N} x(m) \quad (F.1)$$

where $x(m)$ are the image samples and the cosines are the coefficients or tap weights needed to execute the DFT, which is simplified, in fact, to a cosine transform. N is the total number of image samples taken and is also equal to the total number of frequency components given by the transform.

Following is a computer program that calculates the coefficients (cosines) needed for a 128 point transform.

```

.500 C      IT CALCULATES THE COS NEEDED
.600 C      COS STORED IN FILE OUT
1.000      DIMENSION A(64,128)
2.000      DO 9 II = 1,64
4.000      I = II - 1
- 4.500      DO 8 JJ = 1,128
5.000      J = JJ - 1
6.000      A(II,JJ) = COS(2*3.14158*I*J/128)
11.000 3    CONTINUE
12.000 9    CONTINUE
12.200      DO 4 I = 1,64
12.500      WRITE (108,10) (A(I,J),J=1,128)
12.600 4    CONTINUE
13.000 10   FORMAT(7(X,F6.3))
14.000      END
--EOF HIT AFTER 14.

```

*

APPENDIX G

COMPUTATION OF A COSINE TRANSFORM ON SIGMA-9 COMPUTER

The following program is a computer simulation of experiment "one" of the frequency analysis application of Chapter 4 (section 4.4.3). A DFT, reduced to a cosine transform, is applied to a rectangle image. The rectangle amplitude is normalized.

```

.020 C THIS PROGRAM CALCULATES A 128 POINT COSINE
.020 C TRANSFORM
.030 C RESULTS STORED IN FILE FREQ
.100 DIMENSION A(64,128),X(128),Y(128)
.200 DO 25 L=1,128
.300 X(L) = 0.
.400 25 CONTINUE
.500 X(77) = .2
.550 X(78) = .6
.600 DO 26 LL = 79,85
.650 X(LL) = 1.
.700 26 CONTINUE
.750 X(85) = .5
.800 X(87) = .15
.850 X(88) = .05
1.100 DO 27 I = 1,4
1.200 READ(105,22) (A(I,J),J=1,128)
1.250 22 FORMAT(7(X,F6.3))
1.300 27 CONTINUE
2.000 DO 20 I = 1,4
3.000 Y(I) = 0
4.000 DO 21 J = 1,128
9.000 Y(I) = A(I,J)*X(J) + Y(I)
9.200 WRITE(108,222) Y(I)
9.400 222 FORMAT(30X,F8.3)
10.000 21 CONTINUE
11.000 II = 129 - I
12.000 Y(II) = Y(I)
13.000 20 CONTINUE
14.000
15.000 24 FORMAT(6(X,F8.3))
16.000 END
--EOF HIT AFTER 16.

```

*

APPENDIX H

COMPUTATION OF INVERSE DFT ON SIGMA-9 COMPUTER

With the results of experiments "one" and "two" of section 4.4.3, an inverse DFT was computed to reconstruct the images used in both experiments. A XEROX SIGMA-9 computer was tasked to calculate the inverse DFT from frequency components obtained by both experiments measurements and computer simulation. The program listing and computer results are presented in this Appendix. Finally, Fig. H.1 and H.2 are plots of the reconstructed images.

```

.500 C      THIS PROGRAM EXECUTES AN INVERSE DFT
1.000      DIMENSION A(66,128),X(128),Y(128)
1.100      DO 30 J = 9,128
1.200        Y(J) = 0.
1.300 30    CONTINUE
1.400      Y(1) = 16.75
1.500      Y(2) = -16.275
1.600      Y(3) = 14.89
1.700      Y(4) = -12.75
1.800      Y(5) = 10.08
1.900      Y(6) = -7.12
2.000      Y(7) = 4.17
2.100      Y(8) = -1.37
3.000      DO 40 I = 1,64
4.000      READ(105,41) (A(I,J),J=1,128)
5.000 41    FORMAT(7(X,F6.3))
6.000 40    CONTINUE
9.000      DO 44 I = 1,64
10.000     X(I) = 0.
11.000     DO 43 J = 1,128
12.000       X(I) = (X(I) + A(I,J)*Y(J))
13.000 43    CONTINUE
13.500     X(I) = X(I)/64
14.000     II = 129 - I
15.000     X(II) = X(I)
16.000 44    CONTINUE
17.000     WRITE(108,45) (X(I),I=1,128)
18.000 45    FORMAT(7(X,F6.3))
19.000     END

```

*X

!SET F:1/OUT;IN;SAVE

!FLAG INV

FLAG VERSION D04

WITH>F:1=105

.131	.131	.131	.132	.132	.132	.132
.132	.131	.130	.130	.128	.128	.127
.127	.128	.129	.130	.132	.135	.136
.137	.138	.137	.135	.133	.130	.126
.123	.120	.119	.119	.121	.125	.131
.137	.143	.149	.153	.154	.151	.145
.134	.121	.107	.093	.082	.076	.090
.095	.124	.169	.231	.310	.404	
.629	.751	.873	.990	1.094	1.182	
1.289	1.289	1.248	1.182	1.094	.990	
.751	.629	.512	.404	.310	.231	.169
.124	.095	.080	.076	.082	.093	.107
.121	.134	.145	.151	.154	.153	.149
.143	.137	.131	.125	.121	.119	.119
.120	.123	.126	.130	.133	.135	.137
.138	.137	.134	.135	.132	.130	.129
.128	.127	.127	.128	.128	.130	.130
.131	.132	.132	.132	.132	.132	.131
.131	.131					

STOP

!BYE

CPU = 1.1633 CON= 00:14:00 INT = 48 CHG = 515

.134	.135	.142	.151	.162	.173	.184
.192	.198	.199	.195	.188	.177	.163
.152	.141	.132	.128	.129	.135	.147
.162	.190	.198	.214	.227	.233	.231
.222	.204	.180	.151	.119	.089	.064
.048	.045	.057	.088	.137	.204	.289
.387	.496	.608	.720	.824	.916	.989
1.040	1.063	1.059	1.026	.965	.880	.774
.653	.524	.392	.266	.152	.057	-.016
-.061	-.061	-.016	.057	.152	.266	.392
.524	.653	.774	.880	.965	1.026	1.059
1.063	1.040	.989	.916	.824	.720	.608
.496	.387	.289	.204	.137	.088	.057
.045	.048	.064	.089	.119	.151	.180
.204	.222	.231	.233	.227	.214	.198
.180	.162	.147	.135	.129	.128	.132
.141	.152	.165	.177	.188	.195	.198
.198	.192	.184	.173	.162	.151	.142
.135	.134					

STOP

!BYE

.195	.199	.199	.195	.187	.177	.164
.151	.139	.131	.126	.126	.131	.142
.156	.173	.190	.205	.217	.223	.222
.214	.198	.175	.147	.117	.088	.063
.048	.045	.056	.085	.133	.199	.283
.380	.488	.601	.713	.819	.914	.989
1.042	1.069	1.067	1.036	.976	.891	.785
.663	.531	.397	.267	.151	.052	-.023
-.069	-.069	-.023	.052	.151	.267	.397
.531	.663	.785	.891	.976	1.036	1.067
1.069	1.042	.989	.914	.819	.713	.601
.488	.380	.283	.199	.133	.085	.056
.045	.048	.063	.088	.117	.147	.175
.198	.214	.222	.223	.217	.205	.190
.173	.156	.142	.131	.126	.126	.131
.139	.151	.164	.177	.187	.195	.199
.199	.195	.188	.179	.169	.159	.151
.146	.144					

STOP

.106	.106	.108	.110	.112	.115	.118
.121	.124	.127	.130	.132	.135	.138
.141	.143	.150	.154	.160	.163	.169
.172	.175	.175	.175	.172	.168	.163
.158	.152	.147	.143	.140	.139	.139
.141	.142	.143	.143	.140	.134	.125
.113	.099	.084	.070	.060	.056	.061
.078	.110	.159	.225	.308	.407	.519
.641	.739	.895	1.013	1.124	1.215	1.284
1.326	1.325	1.284	1.215	1.124	1.013	.395
.739	.641	.519	.407	.308	.225	.159
.110	.078	.061	.056	.060	.070	.084
.099	.113	.125	.134	.140	.143	.143
.142	.141	.139	.139	.140	.143	.147
.152	.158	.163	.168	.172	.175	.175
.175	.172	.169	.165	.160	.154	.150
.145	.141	.138	.135	.132	.130	.127
.124	.121	.118	.115	.112	.110	.108
.106	.106					

STOP

IE
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*

Figure H.1: Inverse DFT for experiment one.

Figure H.2: Inverse DFT for experiment 2

END

1 5 1 2 8 1 1

FIN