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A HIGH-SPEED, TWO-DIMENSIONAL CROSS-CORRELATOR
FOR REAL-TIME IMAGE PROCESSING

BY

© Thomas G. Ray, B. Eng.

A thesis submitted to the Faculty of Graduate
Studies and Research in partial fulfillment
of the requirements for the degree of

Master of Engineering

Carleton University
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June 1982

The undersigned recommend to the Faculty of Graduate Studies the acceptance of the thesis:

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Real-Time Image Processing"

submitted by Thomas G. Ray in partial fulfillment of the requirements for the degree of Master of Engineering.

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Real-Time Two-Dimensional Correlator

ABSTRACT

A high-speed, two-dimensional cross-correlator for real-time image processing has been developed. The correlator employs a parallel array of multiplying digital-to-analog converters to produce the cross-correlation function of a raster-scanned image with any of a set of programmable 8x8 pixel reference images stored within the correlator. Image sampling rates exceeding 6.6 megasamples per second have been tested without noticeable loss in performance.

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LIST OF SYMBOLS AND ABBREVIATIONS

A	Address, analog
ADC	Analog to digital converter
AGND	Analog ground
BCD	Binary coded decimal
BW	Bandwidth
col.	Column
CMOS	Complimentary metal oxide semiconductor process
D	Digital, data
DAC	Digital to analog converter
DGND	Digital ground
div.	Division
f	Image signal, arbitrary function
FIR	Finite impulse response
GND	Ground
h	Tap weight
hi	Logic '1'
IC	Integrated circuit
k	Correlation variable, kilo = 10^3
l	Correlation variable
lo	Logic '0'
LS	Low-power Schottky TTL logic
LSB	Least significant-bit
LSI	Large scale integration

m	Summation variable, milli = 10^{-3}
M	Magnitude, reference dimension, mega = 10^6
MDAC	Multiplying digital to analog converter
MOS	Metal oxide semiconductor
MSB	Most significant bit
MSI	Medium scale integration
Mag.	Magnitude
n	Bit number, sample number, summation variable, nano = 10^{-9}
N	Reference dimension
NBUS	Negative current summing bus
p	Sampling period, pico = 10^{-12}
PBUS	Positive current summing bus
r	Reference signal
R	Read
R_{fr}	Correlation signal between f and r
RAM	Random access memory
ROM	Read only memory
RMS	Root mean square value
RSCAB	Reference signal column address bus
RSDB	Reference signal data bus
RSIB	Reference signal inhibit bus
RSLB	Reference signal latch bus
S, SCN	Sign
S/H	Sample and hold

SLC Single line correlator circuit

t Time

T Sampling duration

TTL Transistor-transistor logic

VLSI Very large scale integration

VREF Voltage reference

VREF⁺ Positive line of differential voltage reference bus

VREF⁻ Negative line of differential voltage reference bus

W Write

$\phi 1, \phi 2, \phi 3, \phi 4$ Clocks for refresh scheme

τ Correlation variable

Analog ground

Auxiliary analog ground (on image ADC)

Digital ground

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CHAPTER 1

INTRODUCTION

1.0 Introduction

Interest in digital image processing techniques dates back to the 1920's when digitized pictures were first sent by submarine cable between newspaper offices in London and New York [1]. Application of digital image processing techniques, however, did not become widespread until the availability of suitably high-powered digital computers in the 1960's. Since then, the field has experienced tremendous growth, with applications that now range from optical character recognition to space-mission image enhancement.

Within the field of image processing, two-dimensional linear filters find applications in many areas, including image enhancement, image restoration, feature extraction and pattern recognition [20]. Until now, two-dimensional filters have been almost exclusively digital. Optical techniques for linear filtering have received success in the laboratory since the mid 1960's. However, lack of ruggedness and interfacing difficulties, which are only now being overcome, have excluded them from many applications [16].

Two fundamental techniques exist for implementing linear digital filters in two dimensions, and each has its own benefits and drawbacks. Recursive two-dimensional filters are fraught with the

problems of inseparability and instability, although their potentially greater hardware efficiency has caused them to be advantageously employed in many instances [5,20]. Non-recursive, or "finite-impulse response" (FIR) filters are potentially inefficient but they have neither separability nor instability problems. As a result, non-recursive filters tend to be more desirable.

An important application of the FIR filter has been in pattern recognition systems where the filter is used as a correlator [12,18]. In the past, correlators have been implemented in non-real time on general-purpose digital computers that were optimized for flexibility rather than speed, so that their application would not be restricted. The addition of array processors and the use of multiple processors sped up the processing to near real-time rates; however, at the expense of increased weight, power and cost.

1.1 Thesis Motivation

The specific interest, which initiated this thesis, is a desire on the part of the military to produce a cost-effective, light-weight, real-time target detector for applications in remote sensing. Implied within such a device is a real-time two-dimensional correlator. Thus, there is an active need for such a correlator.

Recent work [6,8,14,15] has shown the feasibility of using mixed analog-digital techniques to implement one-dimensional correlators, which otherwise meet the fundamental requirements outlined above.

Adaptations and expansions of these designs have led to the development, in this thesis, of a high-speed two-dimensional correlator. This correlator demonstrates the feasibility of using the mixed analog-digital approach and prepares the way for future integration of the correlator onto one or several integrated circuit chips in order to realize the full potential of the mixed analog-digital approach.

1.2 Thesis Objective

The objective of this thesis is three-fold. Primarily, it is to demonstrate the feasibility of using mixed analog-digital signal processing techniques for performing real-time two-dimensional correlation. A second objective is to perform this demonstration with a circuit that will model a future correlator that may be integrated onto one or more IC chips. The final objective is to show that, at present in certain cases, the mixed analog-digital approach may be an advantageous alternative to digital processing for the implementation of such a correlator.

1.3 Thesis Format

Chapter 2 of this thesis reviews the theory of correlation in both one and two dimensions. It proposes a possible parallel architecture for calculating the two-dimensional correlation function in real time, and then discusses several alternatives for implementing

the architecture. The chapter then proposes a mixed analog-digital chip for use as a building block in implementing the correlator.

Chapter 3 presents the design details of a discrete component version of the mixed analog-digital two-dimensional correlator. Its components are designed to model the chip proposed in the previous chapter so that its operation can be studied before committing to an actual, and costly, IC design. The chapter also includes the design details on some specialized hardware used later for evaluating the correlator.

Chapter 4 presents some results obtained from the operation of the correlator. Results are given primarily for the use of the system in correlation detection, but others are presented as well. One of these is the result of an experiment illustrating image enhancement.

Finally, concluding remarks and suggestions for further research are presented in Chapter 5.

CHAPTER 2

CORRELATION THEORY AND PROPOSED CORRELATOR IMPLEMENTATION

2.0 Introduction

This chapter reviews correlation theory for one and two-dimensional signals, and then states the requirement for having the correlation function produced in real time. Several approaches to performing the correlation are discussed, leading to a proposed model of an integrated sampled-analog correlator.

2.1 Correlation Theory

Correlation¹ is most often used to identify components of received signals that bear close resemblance to some other signal, usually one that is stored locally, as a reference. The points at which the two signals correspond are indicated by peaks in the correlation function. These peaks are readily identifiable by their relative height and sharpness.

Correlation is based on the averaged product of the received signal and the locally stored reference signal. Forming the averaged product can be done by multiplying the signals and then integrating. The process will be explained in more detail in the following sections of this chapter.

1 The correlation referred to here is properly called cross-correlation. This is different from auto-correlation, in which a shifted version of the received signal is used as the reference signal.

2.1.1 Correlation of One-Dimensional Signals

For any continuous signal, $f(t)$, and a reference signal, $r(t)$, that is zero outside of the range $0 < t < T$, the correlation function is defined by [4]:

$$R_{fr}(\tau) = \frac{1}{T} \int_0^T f(t+\tau)r(t)dt \quad (2.1)$$

Figure 2.1 shows an example of the correlation of a simple received signal with a simple reference signal. As can be seen in this figure, the time τ at which the received signal and the reference signal most closely correspond is indicated by a conspicuous peak in the correlation function. Figure 2.2 shows the correlation of a noisy signal with a clean reference signal. Again, the correlation function clearly indicates when the two signals most closely correspond.

A signal can be sampled at discrete time instants so as to form a representation of the original signal as a sequence of values. For the specific case of $f(t)$ and $r(t)$, the signal and reference respectively, let the samples be labelled $f(n)$ and $r(n)$, where n is the sample number. If the samples are taken every p seconds, then the sample number, n can be related to time, t , by $n = t/p$.

For the sampled signals $f(n)$ and $r(n)$, the equivalent correlation function is mathematically similar to (2.1), except that the integral is replaced by a summation. The equivalent correlation function is, therefore:

Figure 2.1: Illustration of Correlating Two Simple Signals

a) Noisy Signal, $f(t)$

b) Reference Signal, $r(t)$

c) Correlation Signal, $R_{fr}(\tau)$

Figure 2.2: Illustration of Correlating a Noisy Signal with a Noise-Free Reference. Of note is the large peak in the correlation signal at $\tau = 15$.

$$R_{fr}(k) = \frac{1}{N} \sum_{n=0}^{N-1} f(n+k)r(n) \quad (2.2)$$

where N and k are related to T and τ of (1) by:

$$N = T/p$$

$$k = \tau/p$$

Unlike (2.1), this equation can be readily programmed on a digital computer. However, the computation of the correlation function involves N multiplication and accumulation operations for every sample in the correlation function and may take some time to compute.

For example, let us assume a computer which can perform a single multiply-and-accumulate operation, along with the necessary fetch and store overhead, in $10\mu s$. On this machine, the correlation of just one second of a signal sampled at 8 kHz (8000 samples), with a 100 ms reference (800 samples), would take a total of 64 seconds to compute. Sixty seconds of the same signal would take over an hour to compute. Thus, when N is large and the complete correlation function must be calculated, this computation can require a large amount of time.

2.1.2 Correlation of Two-Dimensional Signals

In much the same way as a one-dimensional signal can be sampled, a two-dimensional signal, such as the image signal from a raster-scanned imaging device, can also be sampled, and hence represented by a two-dimensional matrix. With this done, it is possible to extend the one-dimensional correlation function, (2.2), into two dimensions as [5]:

$$R_{fr}(k, l) = \frac{1}{MN} \sum_{m=0}^{M-1} \sum_{n=0}^{N-1} f(k+m, l+n) r(m, n) \quad (2.3)$$

where $f(m, n)$ is the image frame

$r(m, n)$ is the reference frame

$R_{fr}(k, l)$ is the correlation frame

k & l are the independent variables defining a particular picture element in the correlation frame

m & n are the independent summation variables

and M & N are the dimensions of the reference frame.

The correlation operation in two dimensions is illustrated in Figure 2.3. The figure shows the reference being positioned on the image frame to produce one element in the correlation frame. This single correlation element is calculated by summing the products of the elemental pairs between the image and reference frames. By positioning the reference over all possible locations in the image, the entire correlation frame can be calculated.

Figure 2.3: Illustration of the Correlation Procedure

Again, as was the case in one dimension, the correlation equation can be readily programmed on a digital computer, however, here the required computation time will be very long, even for small values of M and N . This is because $M \times N$ products must be calculated for each sample in the image, thus requiring a total of $(K \times L) \times (M \times N)$ multiplications to produce the correlation function for the entire image.

For example, let us assume an image size of 512×512 picture elements and a reference that is 32×32 . Computing the correlation of these two functions requires a total of 268×10^6 multiplication-and-accumulation operations. Let us further assume that there is available to us a computer which can perform a single multiply-and-accumulate operation, along with all the necessary overhead, in just μs . On this machine, it would take $4\frac{1}{2}$ minutes to perform the correlation of these two functions.

2.1.3 Intrinsic Limitations of Correlation Detection

It is important to realize that the correlation function is intrinsically dependent on both the size and the orientation of the reference image relative to the observed image. In practical applications the exact reference size is often known beforehand and so it can be accommodated. Image orientation, on the other hand, often cannot be known, and presents a serious problem, except in those cases where the reference is circularly symmetric, or can be approximated with a circularly symmetric function.

2.1.4 Alternative Applications

An image correlator is actually a generalized two-dimensional convolution processor. As such it is capable of implementing any arbitrary two-dimensional finite impulse response (FIR). The impulse response is limited in its spatial duration by the size of the reference, a larger reference providing a correspondingly larger spatial impulse response.

The FIR filter types that exist in one dimension, such as bandpass, bandstop, lowpass etc., all exist as well in two-dimensions. These are well documented in the literature [5, 20] and are only mentioned here in passing.

2.2 Real-Time Processing Requirements

Classical techniques for the implementation of the correlation function have proven satisfactory in many non-real-time applications and will likely continue to be used for some time in the future.

There are, however, other applications where the real-time generation of the correlation function could be of considerable benefit. "Seeing" robots used by industry for assembly is one example where the correlation function could be used to help detect and orient objects in the robot's field of view. Optical character recognition is another possible example. Finally, military applications of real-time image correlation to remote sensing and other areas [27] can be envisaged.

In none of these areas do there exist standards dictating the data rates required for real-time processing of the collected images. The data rates do however tend to be fairly high. Remote sensing by the military uses data sampling rates of typically 1 to 3MHz [2, 3]. It was the requirement to process information from these sensors that determined the data rate for the image correlator that is the subject of this thesis.

Reference frame size must also be considered, as it directly affects the computational throughput requirements for any processor computing the correlation function in real time. Ideally, the processor would be capable of handling an arbitrarily large reference signal, however in order to make the problem tractable for the purposes of this thesis, a reference array size of 8x8 picture elements was chosen. This small size of array must be considered as only marginal for correlation purposes, since it is clear that any reference image sampled at so few points cannot contain much information, and any correlation with it may not be well defined. The requirement for future expansion was therefore recognized and the need to accommodate such expansions formed a further constraint on the design.

The 8x8 reference and 3 MHz processing rate for this minimal correlator are still non-trivial. Producing the correlation function for each image element within one data sampling period requires a minimum processing bandwidth of 192 million multiply-and-accumulate operations per second. Serial processing of the data at this rate

7

using presently available technology does not appear possible (for example see the available components list in [23]) especially in view of the desired expandability feature that would put further strains on the hardware.

A parallel processing architecture has therefore been assumed for the implementation of the correlator, at least for the time being.

2.3 Data Flow Paths in an Image Correlator Employing Parallel Processing

The continuous image signal from a raster-scan imaging device can be easily sampled to make it compatible with (2.3) so that the correlation function can be calculated. For processing, the samples can then be converted to a digital representation, or they can be left in their analog form, depending upon the dictates of the chosen processing hardware. For the moment it is necessary only to specify that the imagery has been sampled.

Due to the time-dependent nature of any raster-scanning device it is always possible to identify a "present scan-line" and a "most recent sample" in the imagery, as shown in Figure 2.4. By figuratively positioning the reference signal over the image signal so that the upper left¹ corner of the reference signal is always over the most recent sample of the image, the reference signal can be made to scan the

¹ Refer to Figure 2.4

Figure 2.4: Positioning of the Reference Signal Over the Most Recent Image Sample
 (The reference signal dimensions shown were chosen for illustration only.)

complete image in real time. Production of the correlation signal, using (2.3), then requires the multiplication of all the reference samples with the underlying image samples, once every time a new image sample is taken.

Figure 2.5 shows the details of a proposed parallel structure for computing the correlation function in the manner just discussed. For simplicity, the figure shows an example 3×3 reference, however the structure can be made any size. In the figure the reference signal samples are organized into an array corresponding exactly in orientation to the reference shown in Figure 2.4. Associated with each reference sample is a discrete multiplier used to form the products with the image signal samples.

The image signal samples are shifted past the first row of multipliers in order to produce the partial-products for the correlation function along the first line. A chain of exact one-line sample-delay circuits store the image signal samples before transferring them to the following rows of multipliers which in turn produce the partial products along the remaining lines of the image. The partial products are finally summed together in a single function block to complete the correlation operation.

Figure 2.5: Structural Details of an Image Correlator Based on a 3x3 Reference Example

2.4 Possible Implementation of the Image Correlator

2.4.1 Possible Digital Implementation

The proliferation of digital signal processing circuitry throughout electronics today make it a logical first choice to consider for the implementation of the correlator. Such an approach requires an analog interface between the digital hardware and the analog image signal. However, this can be readily provided by any one of the many high speed data converters available today. Analog output, if desired, is also easily provided. Two questions are: how, and with what hardware could the digital processing be accomplished.

Today's integrated circuit (IC) technology has allowed the manufacturing of high-speed digital multipliers on single ICs with product-computation times as short as 65ns [23]. At present such devices appear to be limited to having one multiplier per chip. With this constraint, the implementation of a parallel processor as suggested in the previous section, using an array of these multiplier chips seems most logical. The remaining components of the system, the image shift registers, the image-line delays and the reference storage, can be readily implemented using standard MSI and LSI digital components, and so are not a problem.

Consideration of the power requirements and physical size of such a correlator must be made. The minimum power consumed by the multipliers enumerated in [23] is about one watt. A parallel correlator

constructed using these devices would require an amount of power proportional to the number of multipliers used, assuming that the support circuitry would draw little power by comparison. Thus, the 8x8 correlator proposed for this thesis would consume 64 watts, which is very reasonable even in view of the envisaged application. However, a more reasonable reference array size of perhaps 32x32 elements would consume over 1000 watts and would occupy considerable space. A better device with reduced power dissipation has recently been announced [29] but it does not offer any improvement in size and will not be available for some time.

The cost of these devices must also be considered in determining the overall feasibility of the approach. At present, this cost is high owing to the complexity of the chips and the limited demand for them. Thus, the approach of using digital multipliers in a parallel array to implement a real-time correlator is feasible, but only marginally so, when the criteria of low power consumption, small size and low cost are brought in.

Two other general categories of digital signal processing devices [23] should also be discussed although neither one is properly suited to the task of implementing the correlator. The first is the so-called "function chip". Within this category, there exist several implementations of a one-dimensional binary correlator that could conceivably be used to form the correlations along the lines of the processor. Unfortunately, the desire to correlate continuous-tone imagery

rules out the use of these devices. A one-dimensional five-level correlator has recently been announced [11], but is still not available. Regardless, five levels of input signal quantization could be considered only marginal at best, and so, its use must also be ruled out.

Also within the function chip category are several one-dimensional Fourier transform chips. However, these are much too slow and their sample dimensions much too small to allow their consideration in this application.

The other category of digital signal processing devices are the so-called "general signal processors". These are high-speed microprocessors optimized for signal processing with fast on-chip multipliers. Unfortunately, their speed is not great enough to provide real-time correlation, even in a parallel array.

Thus, the parallel array of digital multiplier chips remains the best choice so far for implementing the correlator. The digital approach in general, unlike analog methods, also has the advantages that it can be made arbitrarily accurate and it is completely interference-free. However, restrictions on the cost, size and power of the envisaged correlator oblige us to consider other alternatives.

2.4.2 Possible Analog Implementation

The sampled analog approach, using charge-transfer devices as the delay elements and analog multipliers to perform the computations,

has been used with much success in one-dimensional analog signal processing in the past [30]. This approach has several advantages, the first being that no analog-to-digital conversion of the image data is required, thus saving some expense. The others are due to the density of the charge-transfer device technology, which would make the correlator physically small and consume very little power. It would also be relatively inexpensive once integrated onto an IC.

However, the approach would suffer inaccuracies incurred in the long analog delays between lines due to charge-transfer inefficiency, and charge leakage [7]. Recent advances in charge-transfer technology have largely overcome these problems, to the extent that, in the future, this approach may become the most practical. However, for the interim it is still not viable. Two additional disadvantages of the analog approach are that it does not intrinsically provide a convenient method for storing the reference image, and it is also susceptible to noise contamination.

2.4.3 Possible Mixed Analog-Digital Implementation

A third approach to implementing the architecture involves the use of a mixture of digital and analog hardware, in such a way as to provide a compromise between the benefits and drawbacks of the two. The mixed analog-digital approach is based on the use of multiplying digital-to-analog converters (MDACs) to perform the computations.

The MDAC is a digital-to-analog converter which has been

optimized to permit a large variation in the input reference voltage. The usual digital-to-analog converter produces an analog output which is the scaled product of the digital input and a fixed analog reference. The MDAC, on the other hand, has a variable reference input level and so provides the function of a one quadrant multiplier; it forms the product of the digital and analog inputs and delivers this product to its output as an analog signal.

The implementation of an array of such multipliers on a single integrated circuit chip can be easily achieved in a metal-oxide-semiconductor (MOS) process using binary-ratioed capacitors and switches [6,8,14]. Such an approach would be highly compact, owing to the density with which the multipliers could be implemented on a chip. It would also consume very little power, due to the fact that the technique has no static power drain.

In referring to the proposed parallel structure for the correlator shown in Figure 2.5, the question arises as to which of the reference signal and the image signal should be applied to the MDAC's analog input, and which to the digital input. Initial consideration of the input forms of the reference and image signals would indicate that the image signal should remain in its analog form, simply to save converting it to digital, and the reference signal, which must remain accurate indefinitely, should be made the digital input. However, as noted in the previous section, the time length of data storage and number of data transfers required for the image signal in this application

are not consistent with sampled-analog storage methods. It is, therefore, necessary to assume the other alternative, that of a digitized image signal and analog reference.

The problem of obtaining a suitable analog reference must, therefore, now be addressed. This problem is easily solved by the use of a digital read-only-memory (ROM), a digital-to-analog converter (DAC), and a separate sample-and-hold device at the analog input to each multiplier. The reference signal samples would be stored in the ROM and then sequentially converted to their analog equivalents by the DAC. The sample-and-hold devices would then acquire the appropriate output from the DAC in a cyclical manner, so as to refresh the stored samples and counteract the effects of charge leakage.

The conversion of the analog image signal to digital form would have to be carried out by a separate circuit at the input to the system in order to achieve the required conversion rate, but, as noted earlier, this would be no problem. Similarly, the long image-line delays are also best implemented off-chip because of their size, but once again this would not pose a problem. Lastly, the product summation would be implemented on-chip using an integrated op amp and charge-balancing. Thus there is no fundamental technical restriction preventing the implementation.

The fixed reference structure of this implementation has one additional benefit not yet mentioned. Briefly, the structure

circumvents the problem of fixed pattern noise (FPN), which is a particular output noise that can appear within the Nyquist bandwidth of a system. FPN had been associated with the rotating reference structure of some previous one-dimensional correlators [6,8,14].

The accuracy with which the correlation function can be calculated using such a structure must also be addressed. For the envisaged application it was not known at the outset what resolution or signal-to-noise ratio the image signal would have, nor how much quantization it could withstand. Estimates, however, ranged up to 8-bits of signal-to-noise ratio for the input, although many estimates were actually much less. For the requirements of output accuracy, no information was available.

For the input accuracy, the 8 bit quantization suggested as the required maximum is fully compatible with the mixed analog-digital approach [6,8,14]. This level of quantization was found to be consistent with the output accuracy that could be obtained with the approach and so it is reasonable to adopt it for the correlator as well, at least for the interim. Future studies may eventually indicate some allowable reduction in accuracy.

Such mixed analog-digital processing chips, however, are not available commercially, although they are easily realized using presently available MOS technology. A similar chip has been fabricated by Y.A. Haque [6] of Carleton University with the co-operation of Bell-Northern Research.

The development cost of such a chip would be substantial, but

could be justified for the envisaged application if it could be amortized over many units.

Thus, the mixed analog-digital approach appears to satisfy most if not all of the requirements for the proposed application.

2.5 A Proposal for a Mixed Analog-Digital Correlator Using Large-Scale Integration Techniques

With the present state of MOS technology, it is practical to put perhaps 16 or 32 MDAC multipliers on a single chip. This will not be sufficient for an acceptable reference frame size, since, for example a 32x32 frame requires 1024 multipliers. Therefore, it has been assumed, for the moment, that a multiplier array on a single chip would operate on only one line of the image. The remaining lines of the image would be processed by parallel connection of the basic chips into an array. This approach is consistent with the parallel-processing architecture that was discussed in section 2.3.

2.5.1 Proposed Multiplier Array Chip

The proposed multiplier array chip is shown in Figure 2.6. The eight multipliers shown in the figure are an example only. The organization and operation of the chip are as follows.

A single row of parallel MDAC multipliers is used to perform the correlation along one line of the reference. The reference signal forms the analog input to the multipliers and is stored in sample-and-hold registers. The image samples are obtained from a

Figure 2.6: Envisaged One-Line Correlator Chip. Eight multipliers are shown for example only.

digital shift register and input to the MDACs' digital inputs. The analog outputs of the MDACs are summed together, buffered, and then transferred out from the chip in analog form.

The image signal samples are sent into the chip on a bus and are moved through the internal digital shift registers past the reference signal samples at the MDACs. The image samples, after being clocked completely through the digital shift registers, are then transferred from the chip. This allows chip cascading along the lines, so that any width of reference signal can be accommodated.

The reference signal is delivered to the chip as a series of digitized samples. These are sent to an internal digital-to-analog converter (DAC) where they are converted to analog levels. The analog samples are then demultiplexed and stored in the analog sample-and-hold circuits which drive the MDAC multipliers.

The analog output buffer minimizes the chip's output impedance to prevent noise interference. Off-chip a separate analog summing network is required to sum together the outputs from all the chips in the system to produce the final correlation signal.

2.5.2 Summary of the Proposed Correlator

The components comprising the proposed correlator, which is pictured in Figure 2.7, are:

- i) the multiplier array chips for each line of the correlation,
- ii) the digital line storage units, which contain those

Figure 2.7: Internal Structure of the Image Correlator

lines presently being correlated with the reference signal,

- iii) an analog-to-digital converter to interface the analog image signal to the digital multiplier arrays,
- iv) a digital memory for the reference signal, and
- v) a summing amplifier to combine the outputs of all the multiplier array chips into the correlation signal

There are also three basic signals within the correlator:

- i) the digitized image signal,
- ii) the digitized reference signal, and
- iii) the analog partial-sum outputs of the multiplier array chips.

The digitized reference signal samples stored in the memory are sent to all the multiplier array chips. These chips receive the series of samples and store the appropriate ones in storage registers within each chip, as was discussed in the previous section.

The image signal is digitized at the input to the correlator by a high-speed converter. The digitized image samples are then sent through the shift registers of the first multiplier array, past the reference signal samples held in the analog buffers. At the same time, the internal multipliers compute the correlation of the two signals along the first line. In this way, the first line of the image signal is moved past, and correlated with, the first line of the reference signal.

The image samples, digitized at the input to the correlator, are also stored in a digital line storage unit, where they are delayed by exactly the same amount of time that the imaging device takes to scan one line. At precisely the same time as an image sample from the present scan-line emerges from the converter, a stored image sample from the corresponding position of the last scan-line appears at the output of the first line storage unit. This sample is then sent to the line 2 multiplier array, to produce the correlation signal for the second line, in synchronism with the correlation signal for the first line. Subsequent lines are delayed and correlated in the same manner. Finally, the partial-sum outputs of all the multiplier arrays are brought to one summing amplifier, where they are combined to produce the final correlation signal output of the system.

The basic correlator may be expanded to accommodate any length or width of reference frame. Any number of points may be correlated along each line by adding extra multiplier array chips and cascading their image signal shift registers. Additional lines may be correlated by the addition of more digital line storage units and multiplier array chips, following the same pattern as shown in Figure 2.7.

2.6 A Model for the Proposed Mixed-Analog-Digital Correlator

Before proceeding with an expensive custom integrated circuit design for the correlator it is necessary to demonstrate the feasibility of the mixed analog-digital approach for performing a real-time

two-dimensional correlation. To be convincing, such a demonstration should be with a system that models the internal operation of the proposed correlator. The model could also be used to later study the effects of variations in the parameters of the correlator, such as dynamic range, bit resolution and reference frame size. It is the design and initial demonstration of such a model that constitutes the body of the next two chapters of this thesis.

2.7 Summary

The background theory of two-dimensional correlation is reviewed in this chapter. Some of its limitations are given and more general applications are discussed. The requirement for a real-time two-dimensional correlator is stated.

Arguments for and against possible implementations of the correlator are made. It is shown that a mixed analog-digital implementation might be optimum. A proposal for implementing the correlator using MOS LSI technology is made. Finally, the motivation for a discrete component model of the correlator is presented.

CHAPTER 3

CIRCUIT DESCRIPTIONS

3.0 Introduction

In this chapter the circuitry of the discrete component model for the proposed integrated correlator is described. The model correlator is based on an 8x8 reference frame.

Also described in this chapter is a video interface circuit for the correlator. Its function is to synchronize the correlator to a video camera and a monitor to allow real-time tests of the correlator in the laboratory.

3.1 Image Correlator Implementation

This section introduces the constructed (i.e. model) image correlator in terms of its constituent parts. A block diagram of the correlator showing these parts, along with the correlator's salient data paths, is shown in Figure 3.1. Detailed descriptions of the component parts will be given in the subsequent sections of this chapter.

The analog image signal input to the correlator is converted to digital form by a converter at the correlator's input. The digitized image signal is then sent to a cascade of 7 line storage registers, each of which delays the signal by exactly one scan-line. The outputs of these registers, together with the output of the

Figure 3.1: Image Correlator Block Diagram and Salient Data Paths

converter, then make up a column of 8 image samples, which are transferred, in parallel, to the line correlator circuits. Throughout the system, the image signal is represented by 8 bit, straight-binary numbers, with an additional sign bit¹.

The main building block of the correlator is the line correlator circuit, of which there are 8 in the present correlator. Each of these circuits is driven by a line of image data and computes the correlation function for that line, which it transfers out over a differential current-summing bus. This bus feeds a differential amplifier which then feeds a sample-and-hold to provide the correlator's output signal.

The operation of the circuit is synchronized to an external master clock. This clock runs a system timing generator which controls the image signal sampling rate and the progression of the image data through the system. All operations within the correlator are triggered on the leading edge of the master clock in order to allow transient clock noise, coupled into the analog computation circuitry, to decay before the computed analog correlation values are sampled and transferred out of the correlator.

An external line synchronization signal controls the effective length of the line storage registers to ensure that they

¹ For generality, the image, reference and correlation signals can be either positive or negative in value, despite the fact that negative image intensities have no physical significance. The ability to handle bipolar reference and correlation signals allows the correlator to be used as a generalized two-dimensional filter. The ability to accommodate bipolar image signals, which required negligible additional circuitry, would be most important to processing signals other than imagery, especially one-dimensional signals, for which the proposed IC might also be used.

provide an exact one-line signal delay.

Two remaining circuit blocks are associated with the refreshing of the reference signal samples stored in the line correlator circuits. The first is the refresh controller which cyclically restores the analog reference samples from an internal read-only-memory. The second is a precision voltage reference which is used as a conversion standard by the reference-signal digital-to-analog converters in the line correlator circuits.

The next seven sections of this chapter describe in more detail the circuitry just introduced. Complete schematic diagrams of the model correlator are included in Appendix C of this thesis.

3.2 Input Analog-to-Digital Converter

The image signal input to the correlator is digitized by a high-speed parallel-type analog-to-digital converter (ADC), which is shown in Figure 3.2. Input image signals must be within the range of 0.0 to 1.0 volts with black represented by 0.0 volts. The output of the ADC is coded in straight binary with 8 bits of resolution. A positive sign-bit is sent to the remaining correlator circuitry for compatibility with the signed-magnitude image data used throughout the system.

The start-conversion signal for the ADC is the same as the master clock of the correlator.

Separate analog and digital grounds are provided for the ADC

Figure 3.2: Input Analog-to-Digital Converter

to prevent digital noise from contaminating the analog input.

Further discussion of this point will be made later.

The analog input to the ADC is not preprocessed by an anti-aliasing filter and sample-and-hold in the usual manner as is normally required. The discrete sample-and-hold, normally required to maintain constant ADC input voltage during conversion, is unnecessary due to the intrinsic sampling action of the parallel conversion technique. The usual anti-alias filter also has been omitted because the limited bandwidth of many imaging devices does not require it, and in other cases, the characteristics of the filter will be set by the image sampling rate and not by the correlator itself.

3.3 Line Storage Registers

The line storage registers each consist of two 9-bit by 4k-word random-access memories (RAM) arranged in parallel, as shown in Figure 3.3. The two RAMs have separate address buses, but between them they have a common data-input bus, and a common data-output bus. This organization allows writing into one RAM while reading from the other, which is fundamental to the operation of the line storage register as a high-speed delay element.

Operational details of the line storage registers and the associated controller are given in Appendix B of this thesis.

Figure 3.3: Line Storage Register

3.4 Line Correlator Circuit

The line correlator circuits each compute the correlation function along one line of the image. These circuits emulate the operation of the previously described correlator chips. The two, therefore, have the same basic architecture and design philosophy.

A simplified schematic diagram of the line correlator circuit is shown in Figure 3.4. Its primary components are a row of MDAC multipliers, a row of analog sample-and-hold circuits, and an image signal shift register. Circuitry also exists for on-board conversion and demultiplexing of the digitized reference samples, as well as switching and control circuitry to steer the MDACs' outputs to the appropriate current-summing bus. All of these components will be described in the following subsections.

3.4.1 Image Shift Registers

The image shift registers have been implemented with TTL low-power-Schottky (LS) octal D-type latch arrays. These are cascaded and clocked together from the master clock to provide the shift register action. The output of each latch array in the shift register drives a separate MDAC in the circuit.

3.4.2 Multiplying Digital-to-Analog Converters and Related Circuitry

The MDACs used to perform the multiplications in this implementation are of the bipolar type with current outputs. The

Figure 3.4: Simplified Schematic Diagram of the Line-Correlator Circuit

current outputs allow the partial-correlation products to be easily summed using the current-summing buses. Depending on the sign of the individual product, each MDAC output current is switched to one of the two current-summing buses, one bus providing the sum of all the positive products, and the other the sum of all negative products. The difference between the signals on these two buses eventually forms the correlation output of the system.

The switching of the MDAC output currents between the two summing buses is carried out by single-pole double-throw CMOS analog switches. The position of each switch is calculated as the exclusive-or of the image and reference sample sign-bits stored in two latch arrays.

The analog inputs to the MDACs, like the outputs, are also in the form of currents. These currents are derived by taking the fixed output voltages of the sample-and-hold buffers and driving them through calibrated resistances into the low-impedance, ground-potential inputs of the MDACs. This provides the MDACs with input currents which are proportional to the voltages at the outputs of the sample-and-holds.

3.4.3 Reference Sample-and-Hold and Sample-Refresh Circuitry

The sample-and-hold circuits and demultiplexer are implemented together, using a CMOS 8-channel analog demultiplexer, low-leakage sample capacitors and FET-input operational amplifiers.

In operation, the inhibit line on the demultiplexer is held

high while a sample voltage and a sample-and-hold address are set up on its inputs. The sample voltage is then placed on the selected sample-capacitor by lowering the inhibit line. The operation is completed by raising the demultiplexer's inhibit line, after which a new sample voltage and address can be set up.

The digitized reference samples are sent to the line correlator circuit over the reference-signal data bus (RSDB), and are latched into an array. At the same time, the sample-and-hold address is latched into another array from the reference-signal column-address-bus (RSCAB), to address the demultiplexer.

The reference-signal sample in the first array is sent to a digital-to-analog converter (DAC). This DAC is of the current-output type, so to make the reference signal compatible with the sample-and-hold, an op amp is employed as a current-to-voltage converter.

The reference-current used by the DAC is derived from an off-board, 10 volt reference, V_{REF} . This voltage reference is buffered and filtered in the line correlator circuits to prevent loading of the V_{REF} bus and to remove noise. The resulting voltage reference is applied to a calibrated resistance to provide the input reference current required by the DAC.

3.4.4 Line Correlator Circuit Board

A photograph of one of the completed line correlator circuit boards is shown in Figure 3.5. In the photograph, the top row of eight integrated circuits forms the image shift register. Immediately below each of the ICs in this row is an MDAC together with its calibrated input resistor. To the left of every pair of MDACs are the CMOS current switches. The two current-summing buses appear running horizontally just below the switches.

Just below the centre of the board are the sample-and-hold circuits. To the right appears the reference signal DAC and filter, and to the left, eight on-board voltage regulators, in various forms (monolithic TO-92, TO-220 and zener diode) which are used to provide power to the analog circuitry.

The image signal is transferred to and from the board through the connectors at the top edge. The connector at the bottom of the board supplies power, data, control signals, timing signals, the DAC's voltage reference and, it also connects to the two current-summing buses.

3.5 Differential Amplifier and Related Circuitry

The difference between the signals on the current-summing buses is determined by terminating the buses into separate, matched impedances and then measuring the difference in the developed voltage using a high-bandwidth differential amplifier. The circuit for

Figure 3.5: Photograph of One of the Line Correlator Boards

performing this operation is shown in Figure 3.6.

Each bus termination resistance, dominated by the resistance R_O' , determines the corresponding bus voltage level. Maximization of the signal-to-noise ratio of the bus implies a large signal level which requires a large value of termination resistance. In contrast, minimization of the bus settling time, which is determined by the RC time constant of the stray bus capacitance, C_{stray} , and the bus termination resistance, requires a small resistance value. R_O' optimizes the trade-off between these two opposing requirements by maximizing the signal level without significantly decreasing the overall system bandwidth¹.

The current-summing buses, in addition to providing convenient high-speed product accumulation, have two attributes that tend to make noise coupled to the buses appear to be invisible. Firstly, because the two buses follow the same path in the circuit, noise tends to be coupled equally to both buses and is then rejected by the differential amplifier's common-mode rejection characteristic. Secondly, the current-source nature of each bus allows the bus output voltage to be conveniently developed with respect to the ground of the differential amplifier, thus circumventing any noise in the correlator's ground circuit that might otherwise not be rejected by the amplifier. This second feature is significant in this implementation of the correlator because the analog ground, by necessity, must also carry the analog power supply return

¹ The actual value of the stray bus capacitance is about 2000 pf. The 8 ohm value chosen for the bus termination resistance gives a bus time constant of 16ns.

Figure 3.6: Differential Amplifier and Sample-and-Hold

current and the noise of the MDACs' digital-input return currents.

The differential amplifier used in this implementation is based on a very high-bandwidth operational amplifier. The gain of five is optimum for the internal compensation of the amplifier employed, and provides an output signal level compatible with most equipment.

An output sample-and-hold with a short acquisition time is used to hold the correlator's output at a constant value throughout the clock cycle while the next correlation sample is being computed. This gives the correlator a stable output free of MDAC output spikes and clock feedthrough noise.

3.6 Voltage Reference and Distribution

The correlator uses a single voltage standard for the reference-signal DACs of the line correlator circuit-boards to avoid tracking problems between boards that might otherwise occur. Figure 3.7 shows the voltage reference and its distribution to the line correlator circuits as well as the additional noise filter and DAC interface in the line correlator circuits. The voltage reference itself is provided by a monolithic integrated circuit.

The voltage reference is delivered to the correlator circuits over a differential bus to prevent differences in analog ground potential between circuits from affecting the perceived reference voltage. Dc loads on the bus are also minimized, again

Figure 3.7: Voltage Reference and Distribution

to prevent affecting the reference voltage.

At each correlator circuit low-pass filters remove ac noise from the bus lines. V_{REF}^- noise, with respect to the correlator circuit board's ground, is removed with a simple RC filter, R1-C1. V_{REF}^+ noise, with respect to the filtered V_{REF}^- line, is removed with an active low-pass filter. The filtered voltage reference is then provided to the differential inputs of the DAC as shown in the figure.

3.7 Reference-Signal Refresh-Controller

The purpose of the reference signal refresh controller is to maintain the reference-signal samples stored in the sample-and-hold circuits of the line correlator circuits. This is done in synchronism with the master clock running the correlator to minimize noise coupling. The details of the refresh operation are given in Appendix A of this thesis.

In summary, the refresh operation is as follows. The first sample-and-hold, in every line correlator board, is first selected and then refreshed with data from the refresh controller. Subsequent columns of sample-and-hold circuits are then refreshed in a like manner until all have been refreshed, at which point the cycle is repeated. The refreshing of the sign bits for all the reference samples is interleaved with the refreshing of the first column of sample-and-holds.

The refresh cycles for all eight correlator boards are overlapped so that the refreshing can be accomplished in minimum time. This maintains accurate reference samples in the correlator circuits by minimizing the refresh period.

3.8 System Timing Generator

The system timing generator produces two primary timing pulses from the leading edge of the master clock running the system, as shown in Figure 3.8. The first of these pulses is used exclusively to sample the output of the analog circuitry from the previous cycle and transfer this sample to the output of the correlator. The second pulse is used to control all other clocked operations in the correlator and thus it serves as the system's master clock. This simple clock scheme allows transient clock noise, coupled into the analog circuitry, to decay before the analog correlation signal is sampled and output.

3.9 Power Busing and Ground Connections

Figure 3.9 shows the power supply connections amongst the internal circuitry of the correlator.

A dual supply, providing +5 volts and +15 volts, powers all the digital circuitry in the system. The +15 volt rail is provided for some of the CMOS interface circuitry of the line correlator circuits. All other digital logic operates from the +5 volt rail.

Figure 3.8: Primary Timing Pulses

(Parentheses indicate designations of times and pulses as used in Appendix C)

* Connection internal to output sample-and-hold.

Figure 3.9: Power Busing and Ground Distribution

Another dual supply, providing ± 24 volts,* powers all the analog components of the system, except the input ADC. Local regulators throughout the system bring the ± 24 volts down to the operating levels of the analog components. Local regulation eliminates power supply noise, with respect to the local ground of the components. Analog ground noise between components is not critical due to other precautions discussed in sections 3.5 and 3.6.

The connection between the analog and digital grounds is internal to the output sample-and-hold circuit. This single connection eliminates digital noise from the analog circuitry, to the largest degree practical. The major noise source avoided is the digital power supply return current.

Figure 3.10 shows the connection more clearly, as well as the remaining digital signal return currents that flow in the analog ground circuit. These currents are the MDAC digital input returns, which are relatively small owing to the high input impedance of the MDACs. The previously mentioned precautions are therefore sufficient to diminish the effect of this noise to an insignificant level.

The ± 15 volt analog power supply for the input ADC provides power that was not within the capacity of the ± 24 volt supply used elsewhere, and it eliminates potential ground loops.

Figure 3.10: Major Ground Connections and Signal Return Noise Sources

3.10 Correlator Evaluation Set-Up.

Figure 3.11 shows a block diagram representation of the set-up used for real-time demonstrations and evaluations of the correlator. It uses a standard non-interlaced monochromatic video camera to provide image data to the correlator. The output of the correlator is displayed on a standard video monitor. An oscilloscope and a Honeywell Visicorder are used for waveform monitoring.

A frequency synthesizer provides the master clock for the system, and specially built video controller and divide-by-N circuits provide all the necessary interfacing and synchronization. These last two circuits are described in Appendix D.

A synchronous pseudo-random noise source is also available in the set-up to allow correlation tests in the presence of noise.

3.11 Summary

The description of the discrete component model for the proposed integrated correlator is given. The model is based on an 8x8 reference signal frame. It uses signed 8 bit magnitude numbers in its digital parts. The line correlator circuit, containing the MDAC multipliers fundamental to the proposed integrated correlator, is described in detail. Also described are the circuits of the input ADC, line storage registers, voltage reference, output differential amplifier and output sample-and-hold. The

Figure 3.11: Correlation Evaluation Set-Up

* Connection of image signal to correlator, and correlation signal from correlator, are shown simplified. Actual connections are made through the video controller. See Appendix D.

reference-signal refresh controller and system timing generator are also described. The philosophy behind the power, ground and analog signal bussing is presented.

Finally, an evaluation set-up for the correlator is described.

CHAPTER 4

RESULTS

4.0 Introduction

This chapter presents the completed image correlator described in the previous chapter and goes on to present experimental results obtained from its operation. Results are given pertaining to the operation of the individual line correlator circuits, as well as the operation of the image correlator as a system, in terms of its application to filtering, correlation detection, and image enhancement. Key performance ~~measures~~ are also presented.

4.1 Image Correlator Assembly

The circuits that comprise the image correlator, and that were described in Chapter 3, may be seen in the photograph of the image correlator assembly that appears in Figure 4.1. The photograph indicates the three major components of the system: the input-image analog-to-digital converter (a), the line-storage registers (b), and the line correlator circuitry (c). The board in front of b) is the system's timing generator, and the one in front of c) is the reference-storage and refresh circuitry. Appearing in both front and back of the circuitry in the photograph, are the analog and digital power supplies for the system. The control box on the left is used

Figure 4.1: Photograph Showing the Image Correlator and its Components
a) Image Analog-to-Digital Converter, b) Line Storage Circuitry, c) Line Correlator Circuitry.

to select the reference signal as well as the desired quantization level for the image¹ and reference signals.

A view of the correlator as seen from a different angle also appears as the frontispiece to this thesis. The view shows the line-correlator boards more clearly, and in front of these, the board containing the voltage reference, differential amplifier and output sample-and-hold, which are obscured from view in Figure 4.1.

The correlator measures $21\frac{1}{2}$ by 22 inches and consumes approximately 360 watts of power.

4.2 Line-Correlator Circuit Impulse Response Tests

During fabrication of the image correlator, the line-correlator circuit boards, corresponding to the circuit shown in Figure 3.4, were tested and calibrated. A portion of this procedure involved checking the impulse response of the boards. The results of some of these tests are presented here.

The results were obtained by installing a single board in the correlator, and observing the current output of the board by driving it through a 100 ohm calibration resistance. The image impulses were applied directly to the board's digital inputs. The tap weights, in each case, were obtained from the reference-signal ROM and refreshed in the usual manner.

1 Selectable image quantization is not yet implemented in the system.

4.2.1 Stepped Tap-Weight Impulse Response

Figure 4.2 shows the image-signal impulse-response of a single board with stepped tap weights. The tap weights are spaced 32 units apart and begin at 27. In the figure at the top and to the left, no impulse is yet applied to the board and hence no output is generated. An impulse applied to the board first samples the weight of tap 0, and sends it out. During subsequent sample periods the remaining tap weights are sent out until the impulse finally passes out of the board and the output returns to zero.

This test was useful for quickly determining whether or not a board was operational. With defective boards, the test usually gave sufficient information to allow the fault to be localized so that it could be corrected.

4.2.2 Equal Tap-Weight Impulse Response

Figure 4.3 shows the impulse response of a single board with equal tap weights. Several magnitudes of impulse are applied to the board and the various responses are shown superimposed. The impulse magnitudes are chosen to exercise one bit of the image shift register at a time, in this way individually testing each bit of every MDAC in the board. The noise that appears in this figure, as well as the previous one, is due to the quantization of the signal caused by the digital sampling oscilloscope used to record the waveforms. The test also showed up any calibration errors, or voltage offset problems.

Figure 4.2: Single-Board Impulse Response: Correlation of 8 equally-spaced tap weights with a unit impulse in image data.

Magnitude of Impulse: +255 (all bits set)

Sampling Frequency: 10kHz

Output taken across 100 ohm resistor

Vertical Sensitivity: 80 mV/in.

Horizontal Sweep Rate: 180 μ s/in.

Figure 4.3: Single-Board Impulse Response: Correlation of 8 maximum-amplitude tap weights with several impulses in image data.

Magnitude of all tap weights: +255

Magnitude of Impulses: 16, 8, 4, 2, 1 and 0

Sampling Frequency: 10 kHz

Output taken across 100 ohm resistor

Vertical Sensitivity: 8 mV/in.

Horizontal Sweep Rate: 180 μ s/in.

4.2.3 High-Speed Impulse Response

Figure 4.4 shows the result of a high-speed impulse-response test that is in all respects other than sampling rate the same as that performed in section 4.2.1 and shown in Figure 4.2. This test was used to assure the high-frequency response of the line correlator boards.

4.3 Image Correlation Results

In order to obtain the results presented in this section, a standard non-interlaced monochromatic video camera was used to provide image data to the correlator. The output of the correlator was then displayed on a standard video monitor. Synchronization of the entire system was provided by the special interface circuit described in Section 3.10.

The set-up used to obtain all of the image correlation results presented here is shown in the photograph in Figure 4.5. In the photograph, the correlator appears in the lower left, with the special interface circuitry to its right. The video camera and monitor are at the top and right. The other equipment shown in the photograph includes an oscilloscope and a Honeywell Visicorder for waveform monitoring, along with two pulse generators and a frequency synthesizer for generating the clock and synchronization signals for the correlator.

In order to provide a one-to-one aspect ratio between the vertical image sampling performed by the camera and the horizontal sampling performed by the image correlator, the video scan-lines were sampled at a rate of 6.6 megasamples per second. At this rate the

Figure 4.4: Single-Board Impulse Response: Correlation of 8 equally-spaced tap weights with a unit impulse in image data.

Tap Weights: same as figure 4.2

Magnitude of Impulse: +255 (all bits set)

Sampling Frequency: 1.0 MHz

Output taken across 100 ohm resistor

Vertical Sensitivity: 100 mV/div.

Horizontal Sweep Rate: 1 μ s/div.

Figure 4.5: Photograph of Test Set-Up Used to Perform Image Correlation Experiments

correlator performed the equivalent of 420 million multiply-and-accumulate operations every second. Although this was faster than the correlator's circuitry was designed to operate, there was no visible indication of any performance degradation.

4.3.1 Correlation with Unweighted Averaging References

The results presented in this section depict those obtained by correlating a simple image with four different sizes of averaging-type tap-weight matrices. These matrices provide a crude low-pass filtering action on the image.

Each of the matrices is square and has its tap weights normalized so that the intensity of the correlation image is the same in each case. The four chosen matrices have the sizes 1×1 , 2×2 , 4×4 , and 8×8 , and are shown in Figure 4.6. Of note is the 1×1 matrix which provides no averaging but instead returns the original image. This image can be used as a measure by which to judge the effectiveness of the averaging provided by the other matrices.

Figure 4.7 shows the results of applying these matrices to a simple image. The gradual removal of the high-frequency step transitions at the edges of the objects as the averaging is carried out over larger areas corresponds to the progressive lowering of the spatial cut-off frequency of a two-dimensional filter. As may be seen, in this case, the processing performed by the correlator is very effective.

a)

Row	Column							
	0	1	2	3	4	5	6	7
7	1	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0

b)

Row	Column							
	0	1	2	3	4	5	6	7
7	1	0	0	0	0	0	0	0
6	1	1	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0

c)

Row	Column							
	0	1	2	3	4	5	6	7
7	16	16	16	16	0	0	0	0
6	16	16	16	16	0	0	0	0
5	16	16	16	16	0	0	0	0
4	16	16	16	16	0	0	0	0
3	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0

d)

Row	Column							
	0	1	2	3	4	5	6	7
7	4	4	4	4	4	4	4	4
6	4	4	4	4	4	4	4	4
5	4	4	4	4	4	4	4	4
4	4	4	4	4	4	4	4	4
3	4	4	4	4	4	4	4	4
2	4	4	4	4	4	4	4	4
1	4	4	4	4	4	4	4	4
0	4	4	4	4	4	4	4	4

*Reference tap corresponding to latest image sample.

Figure 4.6: Reference Matrices for Averaging. Matrices are normalized to Eweights = 256 to ensure equal intensity of correlated images.

- a) 1x1 Matrix. Unit impulse in reference domain.
- b) 2x2 Averaging Matrix.
- c) 4x4 Averaging Matrix.
- d) 8x8 Averaging Matrix.

Figure 4.7: Correlation Images Using Averaging Matrices from Figure 4.6. Original raster-scanned monitor image is shown in Figure 4.9 a). Image sampling rate is 6.6 megasamples per second.

- a) Correlation Image for 1×1 Matrix. Notice that the unit impulse in the reference domain gives rise to the original image.
- b) Correlation Image for 2×2 Averaging Matrix
- c) Correlation Image for 4×4 Averaging Matrix
- d) Correlation Image for 8×8 Averaging Matrix

4.3.2 Correlation of Cross-Shaped Patterns

As a demonstration of image correlation, a cross was programmed as a reference signal. The cross was both 8 pixels high and 8 pixels wide, and its members were 2 pixels thick. The reference cross was oriented horizontally. The tap-weight matrix for this reference was chosen to have an average weight of zero, to remove all sensitivity of the correlation function to average intensity level and, as well, it tended to provide a sharper correlation peak. The matrix is shown in Figure 4.8.

Two crosses corresponding in size to the reference cross were placed in the image plane. One had the same orientation as the reference cross and the other one was rotated by 45° . As well, a one-pixel bright spot was placed in the image plane to serve as a unit impulse to demonstrate the finite impulse response of the correlator. This original image is shown in Figure 4.9 a), as it was viewed by the camera.

The correlation between this image and the reference image is shown in Figure 4.9 b), as displayed on the video monitor. The very intense and well-defined spot where the horizontally orientated cross was in the image plane is the correlation peak. Its small size and high intensity are characteristic.

The cross that was orientated at 45° to the reference shows no well-defined peak in the correlation plane, indicating a lower correlation between it and the horizontally-orientated reference cross.

The unit impulse that was in the image plane gave rise to the

Row	Column							
	0	1	2	3	4	5	6	7
7	-198	-198	-198	255	255	-198	-198	-198
6	-198	-198	-198	255	255	-198	-198	-198
5	-198	-198	-198	255	255	-198	-198	-198
4	255	255	255	255	255	255	255	255
3	255	255	255	255	255	255	255	255
2	-198	-198	-198	255	255	-198	-198	-198
1	-198	-198	-198	255	255	-198	-198	-198
0	-198	-198	-198	255	255	-198	-198	-198

*Reference tap corresponding
to latest image sample.

Figure 8.8: Reference Tap-Weight Matrix for Cross Pattern.

Figure 4.9: Correlation of a Cross Pattern

- a) Original Image
- b) Correlation Image

Of note is the intensity and sharpness of the correlation peak in the correlation image for the properly oriented cross. Also of note is the impulse in the original image, between and below the two crosses, and the image of the reference that it creates in the correlation image. Image sampling rate is 6.6 megasamples per second.

impulse response of the correlator by producing an image of the reference signal in the correlation plane.

Figure 4.10 shows the video signal for the correlation image of Figure 4.9 b). The correlation peak for the right-hand cross appears in line 4. Of note is the relative magnitude and sharpness of this peak, as compared with the signal in the surrounding region. The peak amplitude of the correlation signal produced by the aligned cross is more than double that of the mis-aligned cross. Figure 4.11 shows the details of the correlation peak shown in Figure 4.10.

4.3.3 Correlation of Checkered Patterns

As a second demonstration of image correlation a checkered pattern was programmed into the reference memory and correlated with a similar pattern in the image plane. The reference pattern consisted of 16 2x2 pixel squares arranged as a 4x4 checkerboard, as is shown in Figure 4.12. Tap weights in each position were either +255, representing white, or -255, representing black. Again, making the average tap weight zero provided a sharper correlation peak and removed all sensitivity of the correlation function to low-frequency intensity changes. The checkered pattern that was placed in the image plane is shown in Figure 4.13 a) as it was viewed by the camera and displayed on the monitor.

The result of the correlation operation, as it appeared on the monitor, is shown in Figure 4.13 b), while the actual video signal for this result is shown in Figure 4.14. Again the correlation peak is

Figure 4.10: Video Signal for the Correlation Image shown in Figure 4.9 b). Six lines of video data are shown, the peak of the correlation function occurring in line 4. Figure 4.11 shows the correlation peak in more detail.

Image Sampling Rate: 6.6 megasamples per second
Vertical Sensitivity: 1 V/div.
Horizontal Sweep Rate: 2 μ s/div.

Figure 4.11: Details of Video Signal shown in Figure 4.10. Three lines of video data are shown expanded to clearly indicate the correlation peak. These lines correspond to lines 4, 5 and 6 of Figure 4.10.

Image Sampling Rate: 6.6 megasamples per second

Vertical Sensitivity: 0.5 V/div.

Horizontal Sweep Rate: 500 ns/div.

		Column							
		0	1	2	3	4	5	6	7
Row	7	+255	+255	-255	-255	+255	+255	-255	-255
	6	+255	+255	-255	-255	+255	+255	-255	-255
	5	-255	-255	+255	+255	-255	-255	+255	+255
	4	-255	-255	+255	+255	-255	-255	+255	+255
	3	+255	+255	-255	-255	+255	+255	-255	-255
	2	+255	+255	-255	-255	+255	+255	-255	-255
	1	-255	-255	+255	+255	-255	-255	+255	+255
	0	-255	-255	+255	+255	-255	-255	+255	+255

*Reference tap corresponding to latest image sample.

Figure 4.12: Reference Tap-Weight Matrix for Checkered Pattern.

a)

b)

Figure 4.13: Correlation of a Checkered Pattern

- a) Original Image
- b) Correlation Image

Image sampling rate is 6.6 megasamples per second.

Figure 4.14: Video Signal for the Correlation Image shown in Figure 4.12 b). Five lines of video information are shown, the peak of the correlation function occurring in line 3.

Image Sampling Rate: 6.6 megasamples per second
Vertical Sensitivity: 1 V/div.
Horizontal Sweep Rate: 1 μ s/div.

fairly well defined, although comparison of Figure 4.14 with Figure 4.11 will show that the magnitude of the peak correlation signal for the cross pattern was about 70% greater. The difference is mostly attributed to camera blur, which attenuates high spatial-frequency information in an image and thus tended to have more of an effect on the more complicated checkered pattern. This blur is visible in the monitor image of the camera signal for the checkered pattern shown in Figure 4.13 a).

Raising the bandwidth of the imaging system would improve the result presented here, however, in practice such an improved system might also respond beyond the Nyquist bandwidth limit of the sampling performed by the correlator. This would cause high frequency components of the image to be aliased back into the baseband where they would tend to degrade the image. (Such components would probably appear to add noise to the image.) The implication of this is that, as with any sample-data system, the maximum usable bandwidth of the correlator is limited to less than the simple theoretical Nyquist sample-rate limit, not by the device itself, but rather by the pre-filtering that must be done on the input signal, which for two-dimensional signals is very difficult to perform.

4.3.4 Correlation in the Presence of Noise

As a final demonstration of image correlation the cross-pattern correlation demonstration of section 4.3.2 was repeated this time in the presence of white additive noise. This type of noise is often prevalent in detectors and low-level amplifiers.

For the experiment, one-dimensional pseudo-random noise was bandlimited, (to prevent aliasing at the correlator's input) and added to the camera's output signal before being applied to the correlator. The pseudorandom noise was synchronized to the video frame rate, for the sole purpose of obtaining stable images that could be readily recorded. The noise level was set to provide a 1:1 signal level relative to the peak video signal. This can be seen in Figures 4.15 a) and c) which show, respectively, the uncorrupted video signal of the cross, and the same signal with noise added. In the second figure, however, the signal representing the cross has been almost totally obscured by noise and is almost unrecognizable.

Figure 4.15 b) and d) show the output of the correlator corresponding to the two previous input signals. In both cases the correlation peak occurs in the fourth line. In the noise-free observation, b), the correlation peak is clearly visible. In the noise-added observation, d), although the correlation peak is partly obscured in the photograph by the overlapping of the previous line, the correlation peak is still readily discernable.

Figure 4.16 shows the monitor images corresponding to the

Figure 4.15: Video Signals for Correlation of Cross Patterns in the Presence of Noise.

- a) Noise-Free Original b) Noise-Free Correlation
c) Noise-Added Original d) Noise-Added Correlation

For clarity in b) and d) the lines with correlation peaks are coloured yellow.

Image Sampling Rate: 6.6 megasamples per second

Vertical Sensitivity: a), c) 0.5 V/div, b), d) 1.0 V/div.

Horizontal Sweep Rate: 1 μ s/div.

Figure 4.16: Correlation of Cross Patterns in the Presence of Noise.

- a) Noise-Free Original Image
- b) Noise-Free Correlation Image
- c) Noise-Added Original Image
- d) Noise-Added Correlation Image

Image Sampling Rate: 6.6 megasamples per second.

video signals just shown in Figure 4.15. The noise-added correlation image is seen in Figure 4.16 d), and shows a definite correlation peak, although the presence of noise in this image does tend to obscure the observation. To show the result more clearly, the brightness and contrast of the monitor were adjusted to enhance the image, with the resulting image appearing as shown in Figure 4.17. In the figure two spots stand out against an otherwise dark background. The centre spot is the correlation peak, and it is clearly identifiable by its high intensity and small size. The other spot, in the upper left corner, is due solely to noise, however its diffuse nature and low intensity indicate that it is not a valid correlation peak.

The results presented here are also typical of the results that were obtained when the cross was repositioned elsewhere in the image plane. With the same monitor settings that were used to produce Figure 4.17, the correlation peak level seldom dropped enough to make it indiscernable. This result is very encouraging because it indicates the ability to detect objects even in the presence of very high noise levels.

4.4 Image Enhancement

The usefulness of the correlator is not restricted to signal detection. Image enhancement using a so-called "local operator" [9] is a convolution technique that employs a reference signal usually chosen to accentuate fine detail while at the same time reducing the

Figure 4.17: Noise-Added Correlation of Cross Patterns after Video Image Adjustment.

line-storage register. For reference this data word is designated a' .

During the next memory cycle the counter address remains at a value of n , however the LSB is now set. This causes the n^{th} location of RAM1 to be written into with data. The data word that is written is designated as a'' since its position in RAM1 is the same as the data that was previously designated a' . During this same cycle, a' is also output from the output-data latch of the register. As well, the n^{th} location of RAM2 is read, the data read being designated b' . This data also appears at the output-data latch one cycle later.

In the following cycle the counter address is incremented to $n+1$, causing the $n+1^{\text{th}}$ location in RAM1 to be read, while at the same time causing the n^{th} location of RAM2 to be written into.

These cycles are continuously repeated, sequentially emptying memory locations of old data and replacing them with new, until the time that a line synchronization pulse is received. This pulse resets the address counter to zero and, therefore, determines the quantity of memory that is used to store one line. Subsequent cycles output the previously stored data with a time delay of exactly one scan-line from the point at which they were stored.

variation in average intensity level. From an observer's viewpoint, this tends to produce higher quality images, especially if the output medium has limited dynamic range.

To demonstrate the effectiveness of the correlator in this application, a 3x3 pixel local operator from a paper by Hall and Awtrey [9] was used as a reference signal. The original matrix and the scaled matrix used by the correlator are shown in Figures 4.18 a) and b), respectively. The experimental arrangement was otherwise identical to that used in the previous section.

To perform the demonstration the camera was trained on an area of the lab which had both a large amount of detail in it as well as nonuniform illumination. The image was purposely degraded by defocussing the camera to remove much of the fine detail. The resulting degraded image, after digitizing, is shown in Figure 4.19 a), and displays the poor resolution and non-uniform illumination that tend to make it a good candidate for enhancement. The enhanced image is shown in Figure 4.19 b) and displays sharper edges, finer detail, as well as more information in the shadow areas.

4.5 Noise and Dynamic Range

The measurement of the dynamic range of the correlator is based on the ratio of a typical peak correlation signal and the peak-to-peak output noise below the Nyquist frequency, with respect to the one-dimensional electrical output signal from the correlator. Properly,

-2	1	-2
1	6	1
-2	1	-2

a)

		Column							
		0	1	2	3	4	5	6	7
Row	7	*-85	+42	-85					
	6	+42	+255	+42					
	5	-85	+42	-85					
	4								
	3								
	2								
	1								
	0								

b)

*Reference tap corresponding to latest image sample.

Figure 4.18: Image Enhancement Matrix Using a 3x3 Local Operator.

- a) Original Matrix given in [9]
- b) Reference Tap-Weight Matrix Scaled for Correlator

a) Original Image

b) Enhanced Image

Figure 4.19: Example of Image Enhancement Using a 3x3 Local Operator.

the noise should be measured in the presence of an input signal in order to account for input quantization effects, however at video bandwidths this requires superior instrumentation in order to sort the output noise from the signal. Also, quantization noise tends to be signal dependent especially when the number of quantization levels is small, thus complicating the interpretation of results. For these reasons the output noise level was measured in the absence of an image signal. To perform this measurement, the image signal input to the correlator was connected to the output of a dc power supply which was later adjusted to ensure that the image bias level did not affect the output noise. The correlator's output was band-limited to approximately 1 MHz to remove high-frequency clock feedthrough noise and the resulting signal was then observed on an oscilloscope. The signal appeared as broadband noise with a small amount of 120 cycle power supply interference, as shown in Figure 4.20. The measured noise level was 12 mV peak-to-peak.

The peak correlation signal which can be produced by the correlator is a function of the reference signal chosen. The correlation peak shown in Figure 4.11 for the cross-pattern correlation experiment was 1.7 volts. Assuming this value to be typical, then the output dynamic range of the correlator is

$$20 \log \frac{1.7 \text{ V}}{12 \text{ mV}} = 43 \text{ dB}$$

based on the typical peak correlation signal and peak-to-peak inband

Figure 4.20: Correlator Output Noise

Vertical Sensitivity: 5 mV/div.
Horizontal Sweep Rate: 2 ms/div.
Bandwidth: 1 MHz
Reference Tap Weights: All +255
Image Input: dc
Image Sampling Rate: 6.6 megasamples per second

output noise, but without regard for input quantization errors.

The input dynamic range for both the image and reference signals is 48 dB based on the 8 bit resolution used for both signals in the system.

4.6 Summary

The discrete component correlator that was previously described is shown in its completed form in this chapter. Single correlator board impulse responses are presented and their significance to the development of the correlator is outlined. The experimental set-up for image correlation is described and image correlation results for several simple patterns as well as for patterns in the presence of noise are also presented. These results show the feasibility of performing real-time image correlation using a mixed analog-digital approach. Finally, the application of the correlator to image enhancement is demonstrated and a measure of the system's dynamic range is given.

CHAPTER 5

CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

5.0 Summary

This thesis has demonstrated a high-speed two-dimensional correlator based on mixed analog and digital signal processing hardware. The correlator is a discrete-component model for a proposed integrated version that might be developed in the future.

The correlator produces the cross-correlation function of a set of programmable 8x8 pixel reference images stored within itself. Computations are performed by a parallel array of multiplying digital-to-analog converters. Image sampling rates exceeding 6.6 megasamples per second, (corresponding to 420 million multiply-and-accumulate operations per second) have been tested without any noticable loss in performance.

The dynamic range of the analog output signal of the correlator is 43dB, without regard for input quantization noise. The input dynamic range, for both the image and the reference, is limited by the effect of quantization, and for both signals it is -48dB.

In this thesis it has been argued that an integrated version of the correlator could be constructed as a matrix of custom-designed, interconnectable, multiplier array chips which would perform the products of the correlation, in parallel. Using these arrays, arbitrarily large objects could be recognized simply by employing more

chips in the basic correlator; the chips themselves would not have to change. As a result, these chips can be employed in different designs with very little additional cost, most of the cost being incurred for the initial development of the integrated circuit chip.

5.1 Conclusions

Based on the success of the model correlator, the feasibility of the mixed analog-digital signal processing technique for performing real-time two-dimensional correlation has been demonstrated.

Considerations have been made in the model for future IC implementations of the correlator. These have led to an architecture and circuit implementations that emulate the future IC chips that could be fabricated. Thus, the model correlator prepares the way for future integration of the correlator onto one or more integrated circuit chips.

Finally, it was argued in this thesis that such an integrated implementation of the correlator would have definite advantages in systems to which overall size, speed and power consumption are of prime importance. In fact only an integrated version of the correlator can realize the full potential of the mixed analog-digital approach.

5.2 Recommendations for Further Work

5.2.1 Further Performance Measurements

Further performance measurements should be made on the model correlator to complete its characterization. Measurements of correlation

accuracy, distortion and noise can be made as a function of sampling rate and two-dimensional signal frequency. It should be noted that these measurements may be difficult to perform, and to interpret, due to their dependence on several variables. However, the benefits of such a characterization, to the understanding of internal error sources in particular, would aid the design process of an IC and, therefore, should be performed before commencing with any IC design.

5.2.2 Systematic Problems with Correlation Detection

Problems associated with correlation detection caused by the technique's sensitivity to object size, orientation and viewing angle, as well as variations in image intensity, may make it beneficial to reconsider its value in target recognition. A study of the above problems should be undertaken to determine their significance and perhaps find ways to alleviate their effects.

To remove the effect of varying image intensity, consideration should be given to using the correlation index [10], which is a function based on correlation but normalized to the range of ± 1 for all signal levels. The image correlator could be used to compute the cross-correlation portion of the correlation index function.

5.2.3 Systematic Problems with Bandwidth and Aliasing

Systematic problems have been noted for complicated imagery where the conflicting requirements of high-bandwidth and anti-aliasing must be compromised. The problem of bandlimiting the input signal to

prevent aliasing is even more complicated than the problem of constructing the correlator itself, owing to the two-dimensional nature of the signals involved. Band-limiting the optical signal before conversion to an electrical signal appears to be the most practical solution to the problem. Regardless, over-sampling will always be necessary to prevent aliasing, and in general will always require a larger reference frame size.

5.2.4 System Requirements Definition

Before proceeding with an IC design, further consideration should be given to the required reference size, optimal quantization level for the image and reference, and image sampling rate. Reference size and sampling rate are largely application dependent.

In contrast, quantization level is not so application dependent. Experience appears to show that three or four bits of quantization for both input signals might be acceptable for correlation detection, although for feature extraction and general image processing the full 8 bits of the prototype should probably be retained. Regardless, more studies are needed in this area, before committing to an IC design.

5.2.5 Recommendation on an Integrated Circuit Design

The system architecture that has been employed in this thesis appears to be optimum for the direct implementation of the cross-correlation function in two dimensions, especially in view of its conceptual simplicity and its compatibility with available technology.

In an IC design the segmentation of the implementation made in the model correlator should be retained so that the correlator chips and line storage memory remain separate. If the chosen chip implementation requires approximately 8 bits of resolution, then, based on previous designs of up to 32 taps [6,8], the chip implementation should be very similar to that given in Chapter 2.

On the other hand, if fewer bits are required then it becomes possible to consider other configurations. Again, based on the previous design of 32 taps and 8 bits, a reconfiguration could be made with 4 lines, each of 8 elements, and still retain the 8 bit resolution of the original chip. A preferable architecture would include all 8 lines on a single IC so that no accounting for process variations between chips need be considered, and noise pickup can be kept to a minimum.

By accepting the reduced accuracy of a 3 bit multiplier and then repartitioning the bits in the multipliers and shift registers of the previous design, we can obtain a nearly three-fold increase in the number of multipliers. It can therefore be said, with confidence, that an 8x8 image correlator on a single IC with 3 bit resolution is possible.

For this chip one reference input digital-to-analog converter would be shared amongst all eight lines. Any problem of excessive interface pins can be easily accommodated by multiplexing the digital signals on the chip itself. Proper IC layout will ensure noise-free performance. This architecture is highly recommended if it is determined that the size of the reference and the accuracy of the multipliers are acceptable.

5.2.6 Alternative Applications

Alternative applications of the correlator should be considered including feature extraction, image filtering and image enhancement. As well, parallel applications of the mixed analog-digital processing technique to one dimensional signal processing should also be considered. This is especially true in view of the fact that it is possible to construct a single correlator chip so as to be applicable to both one and ~~two~~ dimensional signal processing without chip modification. The wide range of applications for such a chip should make its development and fabrication justifiable.

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APPENDIX A

REFERENCE SIGNAL REFRESHING

This appendix describes the reference-signal refresh controller in terms of the external signals that it generates. The signals are used to maintain the analog reference-signal samples stored in the sample-and-hold circuits of the line-correlator circuits. The signals are shown in Figures A.1 and A.2.

The refresh controller runs in synchronism with the correlator circuits by deriving all of its timing from the master clock sampling the image. The clock is divided by 4 in frequency to produce micro-cycle timing for the controller. During each of these 4-cycle periods one reference sample-and-hold can be refreshed.

Referring to Figure A.1, the beginning of cycle-0, the first refresh cycle, the magnitude of the row-0 column-0 reference sample is accessed from an internal read-only memory (ROM) and sent over the reference-signal data-bus (RSDB) to the line-correlator circuits. At the same time, the reference-signal column-address bus sends out the sample-and-hold address 0 for the sample. This sample is next latched into the reference-signal DAC of the row-0 correlator circuit by the reference-signal latch-bus signal, RSLB-M0. The "M" in this designation refers to the fact that this sample has magnitude only, the sign-bits are handled separately.

To give the correlator's reference-signal DAC time to settle

before its output is latched into the reference-signal sample-and-hold, the correlator's sample-and-hold demultiplexer is inhibited before the data is latched into the DAC. This is achieved by the reference-signal inhibit-bus line 0 (RSIB-0) being held high for a total of 4 refresh-cycle periods, after which it is again lowered to initiate the sampling action in the sample-and-hold. The sampling action then takes place over the next 12 refresh-cycle periods while the inhibit line remains low. This inhibit timing is shown in Figure A.2.

Referring again to Figure A.1 it may be seen that during refresh-cycle 1, the reference-signal data bus contains the sign-bits for all of the row-0 reference samples. These are latched into the correlator by the reference-signal latch-bus line SO (signs, row-0) going true in the middle of the cycle. The reference-signal column address bus is inactive during this cycle.

The start of refresh-cycle 2 begins the refreshing of the row-1, column-0, sample-and-hold, which is in the second single-line correlator circuit. The refreshing is carried out in the same way as the refreshing for the first column of the row-0 correlator circuit. The operation consists of transferring the reference sample to the reference-signal data bus while the appropriate column address, that is 000, appears on the column-address bus and the sample-and-hold demultiplexer is inhibited, this time by RSIB-1. The reference sample is next latched into the correlator's DAC, this time by RSLB-M1. The sample-and-hold demultiplexer is then enabled by RSIB-1 and, finally, the demultiplexer is once again inhibited by RSIB-1, after the sample

Figure A.1: Reference-Signal Refresh: Micro-Timing

Refresh-Cycle	S/H Inhibit- Lines Activated		RSDB Contents:		
	Even-Row	Odd-Row	Data Type:	Data Destination:	
			Magnitude/ Sign	Row (RSLB)	Column (RSCAB)
124	6	5	M	7	6
125	6	5			
126	6	7	M	7	7
127	6	7			
0	0	7	M	0	0
1	0	7	S	0	
2	0	1	M	1	0
3	0	1	S	1	
4	2	1	M	2	0
5	2	1	S	2	
6	2	3	M	3	0
7	2	3	S	3	
8	4	3	M	4	0
9	4	3	S	4	
10	4	5	M	5	0
11	4	5	S	5	
12	6	5	M	6	0
13	6	5	S	6	
14	6	7	M	7	0
15	6	7	S	7	
16	0	7	M	0	1
17	0	7			
18	0	1	M	1	1
19	0	1			
20	2	1	M	2	1

Figure A.2: Reference-Signal Refresh: Macro-Timing

has been properly acquired by the sample-and-hold circuit.

Refresh cycle 3 serves to store the sign bits for all of the row-1 reference samples in the row-1 correlator circuit, again, in a manner like before. The sign-bits for the remaining rows are then stored during the next 6 odd-numbered refresh cycles, that is, cycles 5, 7, 9, 11, 13 and 15. After cycle 15, the remaining odd-numbered refresh cycles are unused since the first 8 cycles stored the sign bits for all of the 64 reference-signal samples.

The remaining even-numbered refresh cycles continue to refresh the analog samples in the sample-and-holds. Cycle 4 initiates the refreshing of the column-0 sample-and-hold in the row-2 correlator circuit, cycle 6 column-0 in row-3, cycle 8 column-0 in row-4, and so on, until cycle 14 in which the column-0 sample-and-hold in the last correlator circuit is refreshed.

After this, the refresh controller begins refreshing the column-1 sample-and-holds in each correlator circuit. It then proceeds through all the remaining columns until the end of cycle 126 when it has refreshed the last sample-and-hold. The refresh procedure is then repeated, in this way constantly maintaining the analog reference-signal values stored in the sample-and-holds of the correlator circuits.

APPENDIX B

IMAGE SIGNAL LINE STORAGE

The image signals to the line correlator circuits are delayed, in succession, by digital line-storage registers. Each line-storage register consists of two 9-bit by 4K-word random-access memories (RAM) arranged as shown in Figure B.1. These RAMs have separate address buses, but between them they have a common data-input bus and a common output bus. This organization is crucial to the operation of the line-storage register as a delay element as it allows one RAM to be written into at the same time as the other RAM is being read from.

In each storage register, the RAM designated in Figure B.1 as RAM1, obtains its address from a 13-bit counter of which the 12 most significant bits are used for the address. RAM2 is also addressed by these same 12 bits, but the address is delayed one cycle by a latch. The least significant bit of the counter is used to determine which RAM is to be read from and which one is to be written into during any one cycle.

Figure B.2 shows the essential operation of the line-storage register. When the counter address reaches a value of n , the n^{th} location of RAM1 is read. The data read is then delayed by the output-data latch for one cycle before it is output from the

Figure B.1: Line Storage Register and Controller

Counter Address (Excluding LSB)	RAM1		RAM2		Data Input	RAM Output	Data Output
	Address	Read/ Write	Address	Read/ Write			
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
n	n	R	n	R	a''	a'	a'
n	n	W	n	W	b''	b'	b'
n+1	n+1	R	n	W	c''	c'	c'
n+1	n+1	W	n+1	R	c''	d'	c'
n+2	n+2	R	n+1	W	d''	e'	d'
.	.	.	n+2	R	e''	e'	e'
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.

Figure B.2: Line-Storage Register Operation

line-storage register. For reference this data word is designated a'.

During the next memory cycle the counter address remains at a value of n, however the LSB is now set. This causes the n^{th} location of RAM1 to be written into with data. The data word that is written is designated as a" since its position in RAM1 is the same as the data that was previously designated a'. During this same cycle, a' is also output from the output-data latch of the register. As well, the n^{th} location of RAM2 is read, the data read being designated b'. This data also appears at the output-data latch one cycle later.

In the following cycle the counter address is incremented to $n+1$, causing the $n+1^{\text{th}}$ location in RAM1 to be read, while at the same time causing the n^{th} location of RAM2 to be written into.

These cycles are continuously repeated, sequentially emptying memory locations of old data and replacing them with new, until the time that a line synchronization pulse is received. This pulse resets the address counter to zero and, therefore, determines the quantity of memory that is used to store one line. Subsequent cycles output the previously stored data with a time delay of exactly one scan-line from the point at which they were stored.

APPENDIX C

ENGINEERING SCHEMATICS OF THE IMAGE CORRELATOR

114

11-4

TITLE LINE CORRELATOR CIRCUIT

SYSTEM

W.D. NO.

ENG. 7. KAY

DATE

SHEET 1 OF 2

(NOT IMPLEMENTED IN
PRESENT IMPLEMENTATION
PER CALCD NO. 1.108)

POWER	CONNECTIONS	TYPE	W.C.	Q.W.
421	74LS273	70,1	10	
422	74LS273	70,1	10	
423	7407	14	7	
430	74LS273	70,1	10	
431	74LS273	70,1	10	
432	74LSMC*	14	7	
433	74LS92	14	7	
403-470	74LS273	70,1	10	

VOLTAGE REGULATOR
PINOUTS
(TOP VIEW)

EDGE CONNECTOR PINOUT	
1	RSB S
2	RSB-H
3	M3B, M3BENT
4	
5	
6	RSDB
7	
8	
9	
10	LSB, SIGMO
11	
12	
13	RSAB
14	RSB-H
15	
16	
17	
18	
19	
20	
21	
22	
23	
24	
25	
26	
27	
28	
29	
30	
31	
32	
33	
34	DEEF
35	DEEF
36	
37	
38	
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41	
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43	
44	
45

- NOTES: 1. KEEP ALL CONNECTIONS, ESPECIALLY GROUND, AS SHORT AS POSSIBLE.
 2. ALL RESISTORS ARE METAL FILM TYPE $\frac{1}{2}\%$ TOLERANCE AND $\frac{1}{4}$ WATT UNLESS NOTED.
 3. CARBON COMPOSITION RESISTORS (RECOMMENDED BY HARRIS SEMICONDUCTOR) HAVE BETTER
 HIGH FREQUENCY RESPONSE BUT LOWER ACCURACY.
 4. R_1 RESISTORS MATCHED TO WITHIN 10% .
 5. VARIABLE RESISTORS HAVE CERTAIN ELEMENTS AND $100\% TOLERANCE$.
 6. CAPACITORS WITH VALUES GREATER THAN 10^{-6} ARE SOLID TANTALUM, THOSE UNDER
 10^{-6} ARE DISC OR MULTILAYER CERAMIC. VOLTAGE RATINGS ARE ALL 25 VOLTS OR GREATER.
 7. CALIBRATION DIFFERENTIAL GAIN: SIMULTANEOUSLY APPLY EQUAL AC CURRENTS TO IN_1 AND IN_2 .
 AND ADJUST R_1 TO GIVE 0.000 VOLTS RMS AT THE OUTPUT OF HARRIS.
 PEDAL MEET (CLOCK FEEDTHROUGH) ADJUST R_2 FOR MINIMUM 100mV FEEDTHROUGH AT 2.5 MHz.
 VOLTAGE OFFSET: GROUND IN_1 AND IN_2 AND ADJUST R_3 TO GIVE 0.000 VOLTS DC AT OUTPUT.

Plan View of Correlator

APPENDIX D

VIDEO INTERFACE CIRCUITRY

The video interface circuitry, introduced to in Section 3.10, is comprised of two independent circuits: the divide-by-N counter which sets the number of image samples in a video line, and the video controller which synchronizes the equipment in the system and facilitates observations of images and waveforms.

A detailed schematic diagram of the divide-by-N circuit is shown in Figure D.1. It consists of a high-speed synchronous 4-decade counter, a thumbwheel switch array, and a 4-decade comparator. The comparator resets the counter to zero whenever the terminal count is reached and thus provides an output once every N cycles, where N is the number set in the switches.

A block diagram of the video controller's circuitry appears in Figure D.2, and a detailed schematic diagram appears in Figure D.3.

The most important signals generated by the video controller are the synchronous horizontal and vertical drive signals to the camera. Horizontal drive is obtained from the 15.750 kHz input clock by duty cycle control and level shifting. Vertical drive is derived from the same clock by a video line counter and another level shift circuit. The video line counter produces an output pulse for the vertical drive once every 262 lines, to be compatible with the National Television System Committee standards for non-interlaced

NOTES: 1. REPLACE EVERY DEVICE WITH 90% CERAMIC DISC
2. DECADE BOARD WITH 33-P TANTALUM

DEVICE	TYPE	POWER	CONNECTIONS
U1-U4	74100	16	5V
U5-U8	74100	16	5V
U9	74100	16	5V
U10	74100	16	5V

Figure D.1: Programmable Divide-by-N Counter Schematic Diagram

Figure D.2: Video Controller Block Diagram

Figure D.3: Video Controller Schematic Diagram

television, to which the camera and monitor were built.

The controller also provides convenient connection between the camera and the correlator's input. Additional connections, and the monitor select switch, allow the correlator's output, or the camera's output, to be displayed on the video monitor, the oscilloscope or the Honeywell Visicorder.¹ An analog multiplexer ensures that the monitored correlator output signal is blank during horizontal and vertical synchronization periods.

A divide-by-261 counter provides low-speed line-synchronization pulses to the Visicorder. The pulses enable the Visicorder to record a video frame in non-real time by allowing sufficient time for paper advance between video lines. This is achieved by taking successive lines from successive video frames. The choice of a divide-by-261 (over a divide-by-263) produces a Visicorder output that has the same orientation as the monitor image (instead of inverted).

The staircase output to the oscilloscope is synchronized to the line-scanning rate. It provides Y-deflection of the oscilloscope beam to allow the displaying of many video lines below one another on the face of the oscilloscope. The "down" steps of the staircase produce a display that is also of the same orientation as the monitor image.

¹ Owing to limited bandwidth in the Visicorder, and poor retention properties of its output images, the use of the Visicorder was dropped, after initial testing, in favour of photographs taken from the video monitor and the oscilloscope.

The staircase is generated by a one-shot 4 bit counter which counts video lines and drives a DAC. The counter can be triggered to count beginning from any line in the video field.

A synchronization illumination switch allows the monitored video image to be intensified in the region of the oscilloscope staircase, or the Visicorder sync. This feature primarily facilitates positioning of objects in the image field for correlation signal monitoring on the oscilloscope. The intensification is achieved by summing a small dc offset into the correlation signal during either the staircase or Visicorder synchronization periods.

END

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