

A Tunable Conjoined-Ring Vernier (CRV) TDC with Sub-picosecond Time Resolution and the Correction of Parallel-Output-Misalignment Effects

by

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Abstract

The purpose of this thesis was to study the insight of the time-to-digital converter (TDC) technology which is expected to be employed in an all-digital phase-locked loop (ADPLL) frequency (clock) synthesizer application in order to reduce its phase noise (jitter). A novel ring-type TDC architecture and design have been proposed for achieving competitive performances in contrast to the current state-of-the-art literature.

A phenomenon called parallel-output misalignment (POM), which intrinsically occurs in every ring-type TDCs like gated ring oscillator (GRO) or Vernier-ring TDCs is analyzed comprehensively. We found that the phase noise caused by POM error may be larger than that due to quantization error (from time resolution characteristic) by up to 22dB or even more. Consequently, the overall phase noise contribution might be dominated by the POM effect rather than the quantization error.

This paper proposes a (tunable) conjoined-ring Vernier (CRV) TDC with a POM error correction circuit that can eliminate the POM error and its consequent corruption on phase noise performance, making quantization error being the only contribution of the overall phase noise. Meanwhile, the proposed TDC implementation may maintain competitive performance in terms of fine time resolution (0.8ps) and a flexible large time residual detection range in a 40nm CMOS technology.

In addition, a configurable digital control that enables a tuning time resolution (0.8ps~1.1ps) function and achieves a superior sub-pico-second performance has been built up. A freely switchable coarse/fine resolution scheme has been realized so as to achieve the best figure of merit considering both resolution performance and power consumption. The proposed Partial Conjoined-Ring Vernier TDC design and the corresponding circuit have been approved and issued by US Patent Office in 2018.

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pointed out the flaws in the research and the places in the literature which may confuse readers. Furthermore, he encouraged me when I got stuck somewhere and shared his experience, ideas from a positive view. His support has been solid and powerful to drive this research going forward.

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Table of Contents

Abstract.....	2
Acknowledgements	3
Table of Contents	6
List of Tables	10
List of Figures.....	11
List of Acronyms	21
Chapter 1: Introduction.....	25
1.1 Phase-Locked Loop.....	25
1.2 Fractional-N PLL synthesizer.....	27
1.3 Motivations of All Digital PLLs and TDCs	30
1.4 Other Motivations.....	33
1.4.1 Delayed Locked Loop	33
1.4.2 Biomedical Imaging System with TDC	35
1.4.3 Laser Rangefinder with TDC	36
1.4.4 Other TDC Applications	37
1.4.5 Research Focus.....	38
1.5 Time-to-Digital Converter and Time Resolution Parameter	38
1.6 TDC Detection Range Parameter	40
1.7 Other TDC parameters	42
1.8 TDC Key Performances Specifications Summary	42
1.9 Thesis Outline.....	43
Chapter 2: Background	45
2.1 Analog TDC	45
2.2 Inverter (or Buffer) Based TDC	46

2.3	Vernier TDC.....	52
2.4	Ring Oscillator TDC.....	55
2.5	GRO TDC.....	56
2.6	Vernier Ring TDC	59
2.7	2-D Vernier TDC.....	60
2.8	Time amplifier (TA) TDC	62
2.9	Other TDCs and Techniques in Tandem	64
2.10	Ring type embedded TDC	65
Chapter 3: POM Effect Analysis.....		66
3.1	Ring type TDCs and their Multiple Outputs	66
3.2	Parallel Outputs Misalignment (POM) Effect	71
3.3	POM Effect Quantization	75
3.4	Comparison between POM Correction and Glitch Correction.....	85
3.5	Conclusion.....	86
Chapter 4: Conjoined-Ring VTDC Architecture and Pre-Design.....		88
4.1	The Idea of a Partially Conjoined Ring	89
4.2	Block Level Function Design and Considerations	90
4.3	Specifications for the TDC design in the ADPLL application	96
4.4	Design of the Conjoined-Ring Vernier TDC.....	96
4.4.1	Pre-treatment Unit.....	97
4.4.2	Partially-conjoined-ring VTDC Core.....	98
4.5	Coarse & Fine Steps and Short Latency Design.....	104
4.6	Pre-logic Circuit Design	108
4.6.1	Flip-Flops Considerations for RRD generation	109
4.6.2	Offset Compensation.....	113
4.6.3	Metastability of RRU Generation Unit	114

4.6.4	Compensation Design at the Clock cycle Slip Zone	116
4.6.5	Double-Sampling RRD Generation	118
4.7	Selections of N and N , B_m and T_{Nor}	121
4.8	High-Speed Loop Counter Design	123
4.9	POM-error Correction Circuit	127
4.10	Implementation of the Evaluation Unit and Non-Interrupted N -Calibration	130
4.11	Arbiter Set Design for Vernier Core.....	136
4.12	Fast Delay Chain Design with Configurable Pseudo-NMOS Inverters	138
4.13	Testbench Circuits Design.....	143
4.14	Conclusion.....	147
Chapter 5: Layout Implementation		148
5.1	32-stage Layout Implementations	148
5.2	Vernier delay chain.....	150
5.3	Tunable Conjoined-ring Vernier TDC Layout Implementations	152
5.4	Package and Bonding Design	165
5.5	Evaluation PCB Layout Design.....	168
Chapter 6: Fabrication and Experimental Result.....		174
6.1	TDC and ADPLL Chip Die.....	174
6.2	Evaluation PCB and Test Bench	178
6.3	32-Stage Conjoined-Ring Vernier TDC Experimental Result	182
6.4	Tunable Sub-picosecond Conjoined-Ring Vernier TDC Experimental Result	189
6.5	TDC Performance Comparison with State-of-the-art.....	195
6.6	Limitation and Drawback.....	195
6.6.1	Uneven Granularity of the Input Interval of the Testbench	195
6.6.2	Sensitivity and Reliability of the Tunable Sub-picosecond TDC Solution	197

6.6.3	Synchronization between Johnson-Ring and 2 nd Stage Binary Counters.....	197
Chapter 7:	Thesis Summary.....	198
References		201
Appendix 1 TDC Timing Consideration for Higher Reference Frequency		211
1A	General Operating-Time Procedure	211
2A	Operating-Period Performance Comparison	213
Appendix 2 ADPLL System Calculation Simulation.....		220
3A	Phase Noise Contribution and Synthesizer	221
4A	ADPLL System Modeling and Simulation	223
5A	Simulation with Type-I	225
6A	TDC Block Diagram	226
7A	Simulation with Type-II.....	226
8A	Comparison between different Configurations	227
9A	Preferred Solution----- Switchable TYPE-I & TYPE-II ALL DIGITAL PLL	228

List of Tables

Table1: Feature of different types of TDCs	64
Table2: Specifications of the ADPLL and the TDC applied	96
Table 3: Performance Analysis at a Fixed 25MHz Reference Frequency (40ns period)	107
Table 4 TDC stages and Counter bit consideration	123
Table5 4-Bit Johnson Counter Sequence	126
Table 6 TDC Performance Comparison With State-of-the-Art	195
Table 7: Improvement of the Phase Noise Performance with Different Accepted Reference Frequency (1GHz of DCO output)	216
Table 8: Comparison of Several TDC Architectures	218
Table 9 Jitter with PLL band width	223

List of Figures

Fig. 1 General phase-locked loop system block diagram	26
Fig. 2 Noise contribution of a fractional-N PLL with (a) narrow bandwidth and (b) wide bandwidth [8].....	30
Fig. 3 Simple integer ADPLL system block diagram.....	31
Fig. 4 Digital low passband LF diagram.....	32
Fig. 5 Block diagram of the modern type of the ADPLL	33
Fig. 6. Waveforms of a REF signal and a higher frequency DCO signal with an arbitrary phase difference in an ADPLL.	33
Fig. 7 DLL system block diagram	34
Fig. 8 Waveforms of a REF signal and a DLL output signal with a random phase difference in a DLL.....	35
Fig. 9 Diagram of the TDC architecture for PET [10].....	36
Fig. 10 Replacement of a conventional medical sensing system by TDC in ISFET [13]	36
Fig. 11 Block diagram time of flight laser rangefinder [15].....	37
Fig. 12 Receiver chip with TDC for laser rangefinder [14].....	37
Fig. 13 Noise Contributions of TDC and DCO in an ADPLL loop	40
Fig. 14 Block and signal diagram of basic analog time-to-digital converter [23]	46
Fig. 15 Illustration of the principle of an inverter delay-line based TDC architecture.....	47
Fig. 16 Illustration of the signals at various nodes of a buffer-based delay chain of a TDC	49
Fig. 17 Illustration of the nodes' state of the delay chain with transition occurrence	50
Fig. 18 D Flip-Flop response to reversed states [27]	51

Fig. 19 Vernier TDC Structure	54
Fig. 20 Timing diagram of a Vernier delay chain TDC with $T_{res} = \tau = \tau_2 - \tau_1$	54
Fig. 21 Ring Oscillator TDC Structure	56
Fig. 22 Gated-Ring Oscillator TDC.....	58
Fig. 23 Vernier Ring TDC Structure.....	59
Fig. 24 2-Dimensional Vernier TDC operational plane.....	62
Fig. 25 (a) Concept of a TA. (b) Shifted SR latch delay characteristics. (c) TA characteristics. [37].....	63
Fig. 26 Ring type TDC diagrams (a) ring-oscillator TDC, (b) GRO TDC, (c) Vernier ring TDC.....	69
Fig. 27 Ideal Transfer characteristic of a single ring-type TDC (N=8) with a single-edge triggered loop counter	70
Fig. 28 Ideal transfer characteristic of a single-ring-type TDC (N=15) with a single-edge triggered loop counter	70
Fig. 29 Practical transfer characteristic of a single ring-type TDC (double-edge counter)	74
Fig. 30 Practical transfer characteristic of a single ring-type TDC (single-edge counter).....	75
Fig. 31. Quantization characteristic of a raw 1-ring TDC (single-edge loop counter)	77
Fig. 32 DPLL system diagram with the TDC applied.	77
Fig. 33 POM effect for random occurrence in (a) time domain (b) frequency domain (fref=20MHz, fdco=1GHz, Tres=2ps, Tpom=2ps, N=15)	81
Fig. 34 PSD due to POM effect and quantization error	82

Fig. 35. POM effect for periodic occurrence in (a) time domain (b) frequency domain ($f_{ref}=20\text{MHz}$, $f_{dco}=1\text{GHz}$, $T_{res}=2\text{ps}$, $T_{pom}=2\text{ps}$, $N=15$)	84
Fig. 36 Glitch correction scheme in [48]	85
Fig. 37. Simple Illustration of the idea with only one ring in the Vernier delay chain. ...	90
Fig. 38 The new TDC scheme diagram (a), with its timing function diagram (b)	91
Fig. 39 Conjoined-ring Vernier TDC block diagram.....	95
Fig.40 Timing diagram of the signals in pretreatment unit.	98
Fig.41 Partially-conjoined-ring VTDC core (a) block diagram, (b) Signals' timing, (c) timing operation diagram of the signals at different nodes.....	101
Fig. 42 TDC final output computing vs time interval input	104
Fig. 43. Degree of activities of the VRTDC and Phase-scaled Vernier TDC.	106
Fig. 44 Timing diagram of the operations and latency time of the various TDCs	107
Fig. 45 Simplified circuits of the pre-logic unit in [34].....	109
Fig. 46. Rough sketch of (a) a RRD generation unit, (b) a master-slave D flip-flop, (c) a basic $C^2\text{MOS}$ flip-flop, (d) a pre-charge flip-flop.	111
Fig. 47 the mismatch due to the single clock trigger in 45 nm process	112
Fig. 48 Circuit of a single to complementary converter with dummy loads.....	113
Fig. 49. Waveform illustration of the pre-logic unit.	113
Fig. 50 the delays in the D flip-flop being associated with metastability.....	116
Fig. 51 The Proposed ADPLL system operation diagram.....	117
Fig. 52 ADPLL timing and computation example ($FCW=3.25$).....	118
Fig. 53 (a) Double sampling block diagram, (b) (c) complementary pair of RRD signals generations in case of $C^2\text{MOS}$ flip-flops for arbiter set.....	120

Fig. 54 Schematic of the double sampling circuit.....	120
Fig. 55 Simulation of the double sampling circuit.....	121
Fig. 56 4-Bit modified Johnson ring counter	126
Fig. 57 Schematic of the 4-Bit modified Johnson ring counter	127
Fig. 58 TDC computation and POM-error vs. time interval: (a) TDC final output, (b) counter output and clip signal flip-flop output, (c) Vernier core output.....	129
Fig. 59 POM-error recognition and correction determination process.....	130
Fig. 60 (a) Implementation of the evaluation unit, (b) Implementation of the POM-error correction circuit, (c) Implementation of the self-calibration circuit.....	134
Fig. 61 Illustration of the Quarter No. identification and N -calibration (when $Z<0:3>$ & $K<0:3>$ being non-zero).....	135
Fig. 62 Optimization and Simulation for 50% duty cycle of the signal along the conjoined ring.....	136
Fig. 63 Transistor level schematic illustration of a semi-dynamic flip-flop (SDFF).....	137
Fig. 64 schematical illustration of the n^{th} Vernier delay stage with a tunable voltage control in clock propagation delay.....	139
Fig. 65 Illustration of the tunable pseudo-NMOS inverter for propagation delay control function.....	140
Fig. 66 schematical illustration of the n^{th} Vernier delay stage with a tunable voltage control in clock propagation delay for the SDFF circuit.....	140
Fig. 67 Block diagram of digital control system.....	141
Fig. 68 Schematic of the digital to analog voltage converter.....	142
Fig. 69 Voltage dividing resistors' value calculator.....	143

Fig. 70 Block diagram of the on-chip testbench.	145
Fig. 71 Tunable delay unit in the external source path.	145
Fig. 72 Time interval coverage of the tunable delay unit branches.	146
Fig. 73 External signal source's edge rate impact simulation.	147
Fig. 74 32-stage conjoined-ring Vernier TDC layout with blocks definitions: 1.1: On-chip ring oscillator; 1.2: Configurable Frequency Divider; 1.3: External signal path with tunable delay control; 1.4: Multiplexer and some pre-logic circuit; 1.5: Metal and poly dummy-fill; 1.6: Conjoined ring and clipping circuit; 1.7: Vernier delay chain; 1.8: Loop counter; 1.9: Edge finder and decoder	149
Fig. 75 32-stage conjoined-ring Vernier TDC Die layout: 1. Main area; 2. Some post evaluation	150
Fig. 76 Vernier delay chain top-level schematic illustration.	150
Fig. 77 Vernier delay chain layout.....	152
Fig. 78 Tunable Vernier delay chain layout.....	153
Fig. 79 tunable conjoined-ring Vernier TDC layout: A. Core circuit; B. Post logic evaluation circuit; C. Pads and ESD.	153
Fig. 80 The core circuit (A) of the conjoined-ring Vernier TDC. A.1: tunable Vernier delay chain (128 stages); A.2: Eight TDC delay chain output post evaluators; A.3: Eight TDC delay chain output (16/4 bit) encoder; A.4: Testbench circuits; A.5: TDC Pre-logic and double-sampling RRD circuit; A.6: Conjoined-ring circuit with clipping switches; A.7: High speed loop counter with clipping signal indicator and corresponding determination circuit; A.8: High speed DCO period counters with encoders; A.9: DCO	

counting and loop counting output (16/4 bit) encoders; A.10: Digitally controlled DC voltage supply circuit for configurable time resolution.	156
Fig. 81 One of the TDC Vernier delay chain post evaluation (A.2).	157
Fig. 82 One of the TDC output (16/4 bit) encoder	158
Fig. 83 Testbench Circuit.....	159
Fig. 84 TDC Pre-logic and double-sampling RRD circuit.	159
Fig. 85 Conjoined-ring circuit with clipping switches.....	160
Fig. 86 High speed loop counter with clipping signal indicator and corresponding determination circuit.	161
Fig. 87 High speed DCO period counters with encoders.....	162
Fig. 88 Digitally controlled DC voltage supply circuit for configurable time resolution.	163
Fig. 89 chip-level layout of an ADPLL design that includes the tunable conjoined-ring Vernier TDC (A and TDC post evaluation logic part of B) (designed by Tuoxin Wang), digital loop filter and SPI interface and control (part of B)(compiled and synthesized by	

Krste Mitric and Yasuhide Goto, backup S2P IO control and interface (part D), digitally controlled VCO (part E) (designed by Shakeeb Abdullah).	165
Fig. 90 Bonding and packaging design (Version I TDC in QFN-32 5X5 package).....	165
Fig. 91 QFN5X5-32 Package description.....	166
Fig. 92 Bonding and packaging design (Version II TDC in QFN-64 9X9 package)	167
Fig. 93 Bonding and packaging design (Version II-2 TDC in QFN-64 9X9 package)..	168
Fig. 94 Evaluation PCB layout (top layer) for Version 1 TDC verification.	169
Fig. 95 Evaluation PCB layout (bottom layer) for Version 1 TDC verification.....	170
Fig. 96 Evaluation PCB layout (power layer) for Version 1 TDC verification.	171
Fig. 97 Evaluation PCB layout (top layer) for Version 2 TDC verification.	172
Fig. 98 Evaluation PCB layout (power layer) for Version 2 TDC verification.	173
Fig. 99 Die images of the first version of the proposed TDC design.	175
Fig. 100 Die images of the second version of the proposed TDC design.....	176
Fig. 101 Die samples' image of the second version of the proposed tunable sub-picosecond conjoined-ring Vernier TDC design.	176
Fig. 102 Images of the TDC verification chips (packages) (a): for Version I, 32-stage conjoined-ring Vernier TDC; (b): for Version II, tunable sub-picosecond conjoined-ring Vernier TDC.	177
Fig. 103 Images of second version TDC (all-digital PLL system chip) die with bonding wire and the corresponding layout design as comparison.	178
Fig. 104 Images of the evaluation board for the first version TDC verification.	179
Fig. 105 Images of the evaluation board for the second version TDC verification.....	179

Fig. 106 Images of the evaluation board for the ADPLL verification (designed by Shakeeb Abdullah).....	180
Fig. 107 Photo of the test bench for test and verification.	181
Fig. 108 Photo of the evaluation board for the ADPLL verification.	182
Fig. 109 32-Stage Conjoined-ring Vernier TDC transfer function measurement with POM correction.	183
Fig. 110 32-Stage Conjoined-ring Vernier TDC output measurements (with/without POM correction).	184
Fig. 111 32-Stage Conjoined-ring Vernier TDC output measurements in power spectral density (with/without POM correction).	184
Fig. 112 32-Stage Conjoined-ring Vernier TDC output comparisons between simulation and measurement results (with POM correction and N-calibration scheme).	185
Fig. 113 32-Stage Conjoined-ring Vernier TDC output comparisons between with/without N-calibration.....	186
Fig. 114 32-Stage Conjoined-ring Vernier TDC linearity results (small range).	186
Fig. 115 32-Stage Conjoined-ring Vernier TDC linearity results.....	187
Fig. 116 Single-shot precision measurement of the TDC output code @200 and @ 400	188
Fig. 117 PSD of the single-shot precision measurement of the TDC output code @200 and @ 400	188
Fig. 118 Tunable sub-picosecond Conjoined-ring Vernier TDC transfer function measurement result (large range).....	189

Fig. 119 Tunable sub-picosecond Conjoined-ring Vernier TDC transfer function measurement result (zoom into a small range).	190
Fig. 120 Tunable sub-picosecond Conjoined-ring Vernier TDC output comparisons in power spectral density between simulation and measurement results.....	191
Fig. 121 Tunable sub-picosecond Conjoined-ring Vernier TDC time resolution comparisons with voltage variation (at room temperature).	192
Fig. 122 Tunable sub-picosecond Conjoined-ring Vernier TDC time resolution comparisons with temperature variation (1v of power supply).	193
Fig. 123 Single-shot precision measurement of the tunable sub-picosecond conjoined-ring Vernier TDC output code @200 and @ 0.9ps of time resolution.	194
Fig. 124 Single-shot precision measurement of the tunable sub-picosecond conjoined-ring Vernier TDC output code @200 and @ 0.75ps of time resolution.	194
Fig. 125 Testbench time interval granularity characteristics.	196
Fig. 126 Operating-period Performance Comparison Between (a) VRTDC and (b) Phase-Scaled Vernier TDC.....	213
Fig. 127 ADPLL System Specificaitons from Microsemi.....	220
Fig. 128 Jitter calculation from phase noise	220
Figure 129 Phase noise contributions of PLL.....	221
Figure 130 PLL and TDC characteristics bond	222
Figure 131 Ddiagram of PLL operation in block level.....	224
Figure 132 PLL operation in time domain.....	224
Figure 133 Updated diagram of a type I PLL operation.....	225
Figure 134 TDC RTL level implementation.....	226

Figure 135 Updated diagram of a type II PLL operation.....	227
Figure 136 Phase noise comparisons among different PLL designs	228
Figure 137 Comparison among different PLL types	229

List of Acronyms

AC	alternating current
ADC	analog-to-digital converter
ADPLL	all-digital phase-locked loop
AND	"and" logic gate
CDR	clock and data recovery
CMOS	complementary metal-oxide-semiconductor
CRV	conjoined-ring Vernier
DC	direct current
DCO	digitally-controlled oscillator
DLF	digital loop filter
DLL	delayed locked loop
DNL	differential non-linearity
DPLL	digital PLL
DRC	design rule check
FCW	frequency command (control) word
FD	frequency division (divider)
GHz	giga-hertz
GPS	global positioning system
GRO	gated ring oscillator
INL	integral non-linearity
ISFET	ion-sensitive field-effect transistor
kHz	kilo-hertz

LAN	local area network
LF	loop filter
LPF	low-pass filter
LSB	the least significant bit
LVS	layout vs schematic
MASH	multi-stage noise shaping structure
MHz	mega-hertz
NAND	complementary to "and" logic gate
NMOS	n-channel MOSFET
NOR	complementary to "or" logic gate
OR	"or" logic gate
PCB	printed circuit board
PD	phase detector
PET	positron emission tomography
PLL	phase-locked loop
PMOS	p-channel MOSFET
POM	parallel-output-misalignment
PSD	power spectral density
PVT	process, voltage and temperature
RC	resistors and capacitors
REF	reference signal
RMS	root mean square
RRD	reference resampled (retimed) by DCO signal

SR	set and reset
TA TDC	time amplifier based TDC
TDC	time-to-digital converter
TOF	time-of-flight
VCDL	voltage-controlled delay line
VCO	voltage-controlled oscillator
VRTDC	vernier ring TDC
VTDC	vernier TDC
XOR	exclusive "or"

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Chapter 1: Introduction

1.1 Phase-Locked Loop

A phase-locked loop (PLL) is a circuit that causes a particular system to track with a referenced one in frequency or phase aspect [1]. Recently, it usually indicates an indirect type of frequency synthesizer (or clock generator) or phase restitution device in microelectronics, and PLL-based synthesizers are about the most common ways to implement synthesizers, so this area is the subject of a great deal of research and development [2]. A PLL acts as a feedback system in which the output signal is fed back to compare with the input reference, so that they can operate at the same or a determined ratio in frequency.

A general PLL is commonly comprised of a phase detector (PD), a loop filter (LF) and a voltage-controlled oscillator (VCO), as shown in Fig. 1. A PD is used to capture and compare the phase (and frequency) difference between the reference input signal and the feedback signal. The magnitude of the PD output is used to control the VCO operating frequency and force it to operate at a desired frequency. A frequency divider may be necessary for the scenario where the frequency of output signal is N times that of the reference signal. Once the phase difference between the reference and the feedback signals stays at zero (or a constant value depending on the type of the PLL), the loop stabilizes implying that the frequency of VCO output signal is locked up based on the frequency of the reference signal, and thus the system behaves as a frequency synthesizer or a clock generator which is locked at a frequency N times that of the reference.

The loop filter (LF) is used to condition the output of the PD, filtering out immediate and drastic changes of the PD output so that the output of the LF can adjust the VCO

gradually and smoothly. Note that immediate drastic changes in time domain corresponds to high frequency energy in frequency domain, thus, to remove that immediate change out the LF is actually a function of low pass filtering in frequency perspective. Thus, sometimes “LPF” has been used as the same meaning as “LF”. The characteristics (the bandwidth and the order) of the LF determine the dynamics of the feedback system. Consequently, the overall phase noise (RMS jitter), acquisition speed and stability performance of the PLL can be optimized and balanced by adjusting the LF parameters.

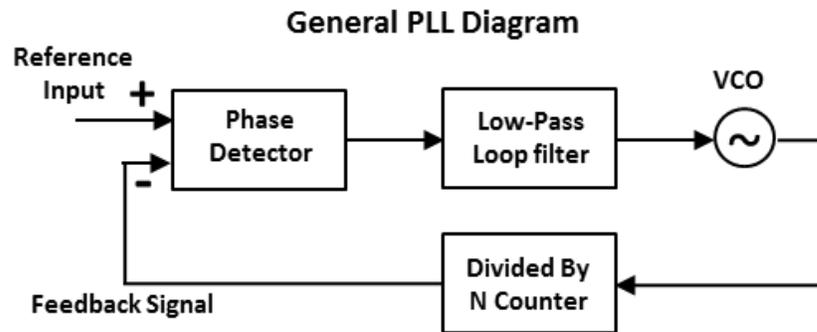


Fig. 1 General phase-locked loop system block diagram

The very first form of a PLL frequency synthesizer was purely an analog device, consisting of a four-quadrant multiplier phase detector, a passive or active RC (capacitors and resistance) loop filter and a well-known VCO. The considerations for competitive performance of PLL devices with high yield mainly include: a) achieving sufficient precision of the off-chip passive components, b) reducing the additional impact of parasitic parameters such as capacitance, resistance and inductance caused by inter-connection wires on the PCB board and c) PVT (process, voltage and temperature) variation of the analog components of the PLL.

As the demand for low cost and high integration devices for wireless or portable applications increases, the design and implementation of electronic devices keep migrating

to the most advanced process technologies available. It has been realized that a digital solution for the implementation of the PLL can benefit more from the evolution of the process technology than an analog counterpart. The first digital PLL (DPLL) appeared in the 1970s, with the phase detector being built by a digital circuit, which makes this DPLL in effect a semi-analog device. However, the loop filter either in an analog PLL device or in a DPLL uses off-chip passive capacitors and resistors, which do not shrink in size at smaller process geometries and therefore may occupy a larger and larger proportion of the area with the migration to smaller process technologies, which counteracts the potential benefit in area and cost reduction.

Due to analog implementations of the PLL not being competitive in meeting increasingly challenging requirements, digital replacements have been developed in aspects of the PD (phase detector) and the FD (frequency divider). Those PLLs have been implemented using mixed-signal topologies [1] due to the combination of the analog and digital circuits.

1.2 Fractional-N PLL synthesizer

In the previous section, the value of the mentioned frequency divider, N , is either an integer or fractional number. An integer- N type PLL (only integer number of N being available) is the simplest version, owing to the fact that in terms of the frequency divider implementation, that is it is not possible (easy) to make a solo divider with a non-integer value of the division. It leads to the result that the step size of the output signal is equal to the input reference frequency. Therefore, the spacing of the channels of an integer- N PLL is limited by the minimum value that can be chosen for the reference signal, which is an undesirable constraint.

While, a fractional-N frequency synthesis method is particularly well suited to integrated circuit applications, like in demanding wireless applications in mobile phones, WLAN, etc., owing to it enabling very narrow channel spacing, large loop bandwidth and consequently, high output frequency compared to the integer counterpart. Specifically, the ability of a fractional-N synthesizer which allows operation at a high reference frequency while achieving a fine step size is realized by continually swapping the division ratio in between two adjacent integer numbers [2]. The desired fractional ratio of N is supposed to be located between those two numbers so that the average of the overall two integer instances can be the desired fractional division ratio. A higher reference frequency and therefore a lower division ratio leads to a relatively low noise (spurs) performance and facilitates a huge leap in the performance of frequency synthesizers for use in industry products [3].

The techniques that are used for the swapping control for a fractional N frequency divider includes pulse swallowing, phase interpolation and Wheatley random jittering which each have their advantages and disadvantages [4]. There is also a first-order delta sigma modulation method creating a similar effect compared to its pulse swallowing counterpart in terms of single integration (accumulator) and the carrying out (comparator) functions [5] [6]. It offers similar noise shaping to push the quantization noise to higher offset frequencies by randomizing the error in some degree. However, the integration of the PD creates a pole when converting frequency to phase, removing the zero created by the first-order noise-shaping function. Finally, the overall characteristic of the spurs is to be of periodicity (not being able to be flattened).

Fortunately, the sigma-delta method is extendable in orders to push the distribution of the phase noise or spurs back to high offset frequency again. It has been proven that high order delta-sigma modulation has been gaining popularity in the last 20 years in fractional-N PLL applications.

Due to its switching behavior of division control function, a fractional-N PLL will create spurs in the output spectrum because there is an instantaneous nonzero phase error and corresponding net charging (or discharging) in the charge pump during each reference cycle. This results in the ripples that modulate VCO output frequency increasing phase noise depending on how the frequency divider is controlled. Additional measures in the FD controller like randomization or some other dithering techniques like probability mass redistribution [7] could be options to further improve the phase noise, however, again, the spurious impact due to the fractional-N frequency division action cannot be reduced entirely.

The power spectral density (PSD) of the PLL output phase noise contribution with narrow loop bandwidth and wide loop bandwidth is presented in Fig. 2. Without consideration of the effect of the loop filter, phase noise increases with the offset frequency in the range from carrier frequency to half sampling frequency offset. Thus, in a narrow bandwidth, a large proportion of the quantization error caused phase noise can be rejected. The cost of that achievement is narrow bandwidth might not provide enough suppression on in-band phase noise Fig. 2 (a), due to its high-pass filtering function of the LF to VCO phase noise. Consequently, the overall phase noise contribution will be dominated by that of the VCO. If a wide bandwidth is used, the VCO caused phase noise in-band can be reduced dramatically however, this allows a greater proportion of the quantization noise

contribution to pass through to the output. Close to the edge of the LF bandwidth this can cause a peak in the phase noise PSD. Thus, the loop bandwidth must be carefully optimized against a number of different trade-offs. These difficult trade-offs have been some of the motivations for the study of all digital PLLs and time-to-digital converters (TDCs).

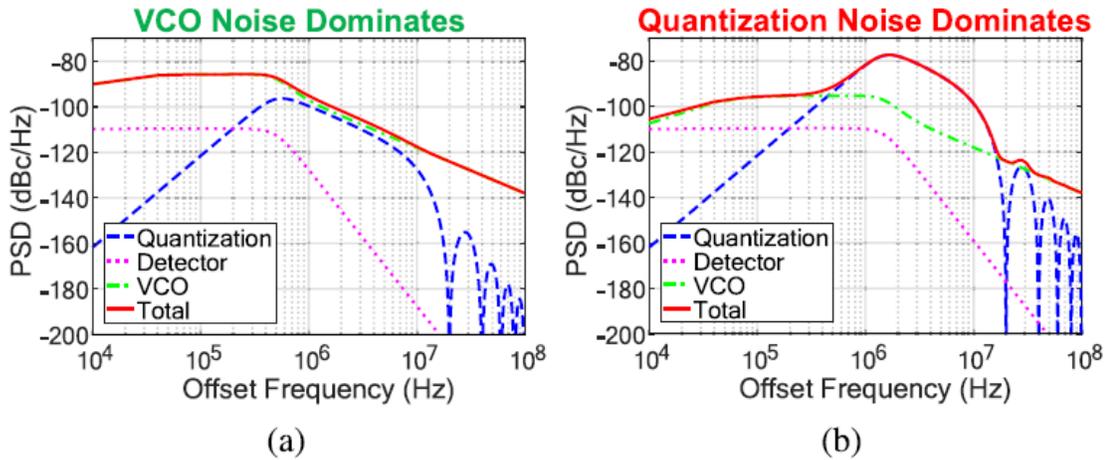


Fig. 2 Noise contribution of a fractional-N PLL with (a) narrow bandwidth and (b) wide bandwidth [8]

1.3 Motivations of All Digital PLLs and TDCs

Motivated by the challenge of the design and optimization of the phase noise in a traditional fractional-N PLL, the study of true all-digital phase locked loops (ADPLLs) [9] with TDC function has been a growing field of interest in recent years. It is also driven by the potential advantage of chip size and chip cost that can be reduced proportionally with process node.

A straightforward way to convert a fractional N PLL into an ADPLL is to replace all parts in the analog PLL (Fig. 1) directly with digital functional blocks. Even the low pass filter located between the PD and the DCO should be implemented completely in a digital manner. As shown in Fig. 3, the inputs and outputs of the components of the ADPLL

system are represented as either a multi-digit binary number or a digital streaming signal. FCW (a binary number) stands for Frequency-Control Word and its value indicates the expected number of DCO (digitally-controlled oscillator) periods in one period of the reference signal. An integer counter is used to count and accumulate the integer number of DCO periods in the current reference period. The output of the PD, indicating the difference of its two inputs as a binary number, is the input to the digital LF (DLF). The frequency of the DCO is controlled by a binary number output from the DLF. Besides the advantage of chip size and cost reduction with process, ADPLL solutions also facilitate a flexible configuration of the DLF for configurable loop dynamics (Fig. 4) allowing the system to achieve both fast acquisition and optimized phase noise performance simultaneously.

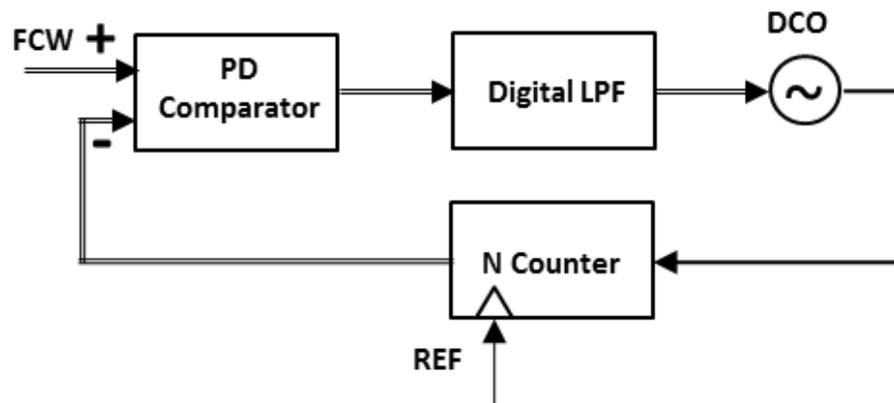


Fig. 3 Simple integer ADPLL system block diagram

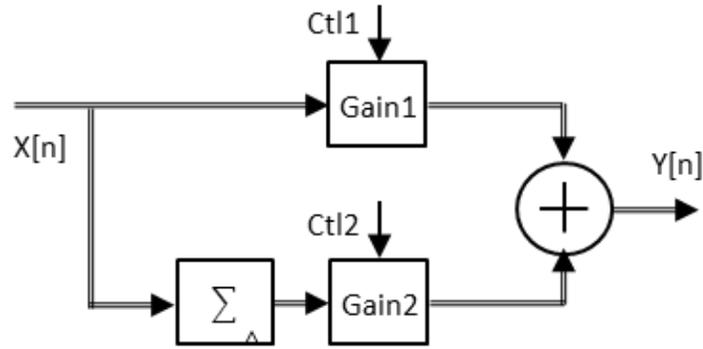


Fig. 4 Digital low passband LF diagram

However, this simple type of ADPLL exhibits relatively large ripple (bad phase jitter) due to their discrete-time manner and the fact that they only count an integer number of DCO cycles between reference edges. Thus, this form of ADPLL can be regarded as equivalent to an integer-N PLL. To realize a demanding phase noise (jitter) performance, a simple ADPLL might not be sufficient. A time-to-digital converter (TDC) device, which is able to measure the fractional residual part of a DCO period with a finer time resolution, can be introduced into the simple ADPLL, becoming a type of modern ADPLL system as shown in Fig. 5

The TDC is employed to quantitatively measure the time interval between the edge of reference signal and the closest preceding one of the DCO signal, corresponding to F_{Rn} shown in Fig. 6. As illustrated in Fig. 5, the rising edge of the reference signal acts as a trigger for multiple blocks of the system. If a modern ADPLL locks and stabilizes at a constant frequency, the phase comparator output will be zero (1), and no further adjustments are made to the DCO output frequency.

$$\sum FCW - \varepsilon[n] - \sum i[n] = 0 \quad (1)$$

It is noted that by accumulating the outputs of FCW and integer counter respectively, the modern ADPLL generates first-order noise shaping of the phase error, so that the phase noise caused by a fluctuation of the reference signal can be improved.

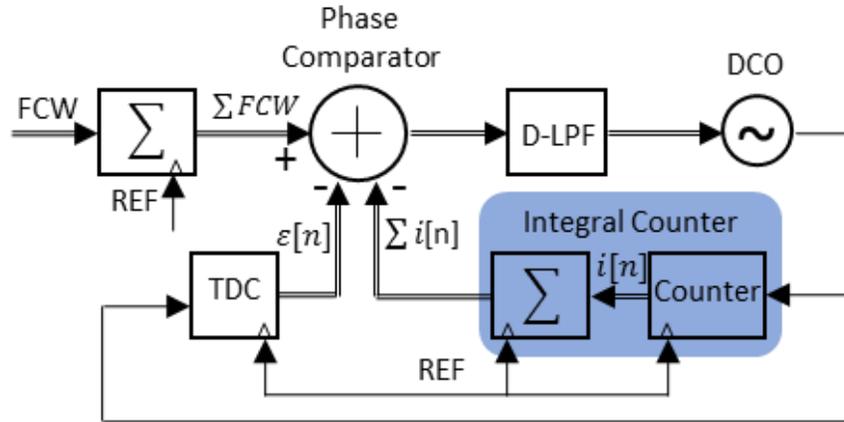


Fig. 5 Block diagram of the modern type of the ADPLL

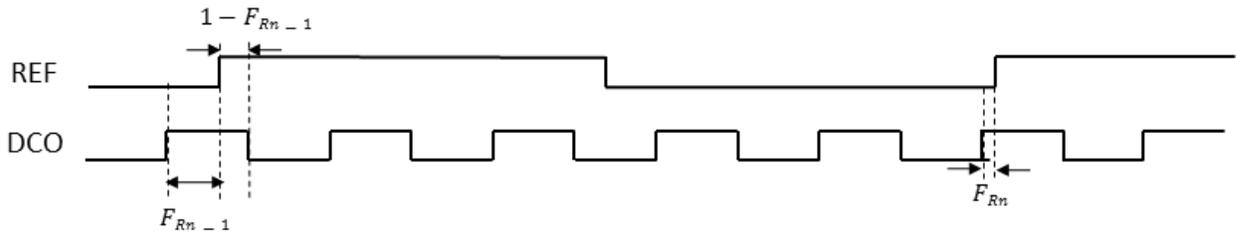


Fig. 6. Waveforms of a REF signal and a higher frequency DCO signal with an arbitrary phase difference in an ADPLL.

1.4 Other Motivations

1.4.1 Delayed Locked Loop

A delayed locked loop (DLL) is a similar system to a PLL and aligns its output (feedback) signal to an input reference clock. However, a DLL uses a voltage-controlled

delay line (VCDL) (Fig. 7) rather than a VCO or DCO as in a PLL. Without a frequency oscillation circuit, the DLL limits itself to controlling the output signal only in terms of the phase. Therefore, the DLL is regarded as a phase restitution or clock and data recovery system (CDR). However, compared to a PLL, in which there is an accumulation of the jitter for every cycle of the VCO output, a DLL system phase jitter comes from only the current cycle without any accumulation. Thus, a DLL results in lower jitter, minimizing the skew of the recovered clock when compared with that of the PLL. In addition, a DLL usually uses a first-order loop filter, facilitating fast settling and good stability performance.

Note from Fig. 7, a VCDL commonly consist of a buffer chain which can be adjusted for various delay time lengths. It should be emphasized that a TDC is sufficient for replacement of the PD of the analog solution if a digital DLL solution is needed. The effect of the TDC on a digital DLL is similar to that on an ADPLL.

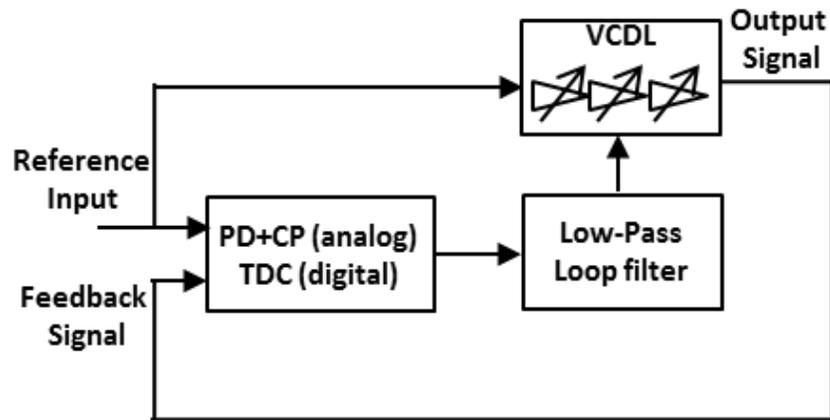


Fig. 7 DLL system block diagram

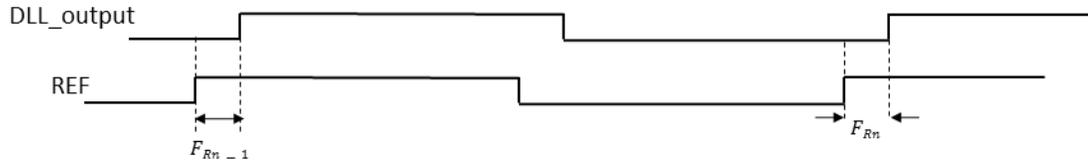


Fig. 8 Waveforms of a REF signal and a DLL output signal with a random phase difference in a
DLL

1.4.2 Biomedical Imaging System with TDC

Positron emission tomography (PET) is a medical imaging methodology based upon the measurement of concentrations of positron-emitting radioisotopes within a living body. In a PET scanner, many gamma ray detectors are arranged in paralleled rings that encircle the patient to be imaged. A time measurement is required to detect the coincidence of two opposing gamma rays that hit two detector pairs. The motivation for the development of a custom front-end CMOS integrated circuit include lower manufacturing costs, reduced physical size requirements, improved system reliability, and reduced power dissipation while simultaneously increasing performance of the system. The sub-nanosecond TDC (Fig. 9) development described here is part of a new custom mixed-signal CMOS integrated circuit developed for high-performance PET tomography front-end applications [10]. In order to meet the higher resolution and low latency requirements, high speed and low power TDC designs must be integrated in nuclear medicine imaging systems [11] [12].

In medical sensing applications like an Ion-Sensitive-Field-Effect-Transistor, it can be refined from a traditional method Fig. 10 to a new form which combines the sensors and TDC. By doing so a compact interface system is realized with direct digital conversion capability [13].

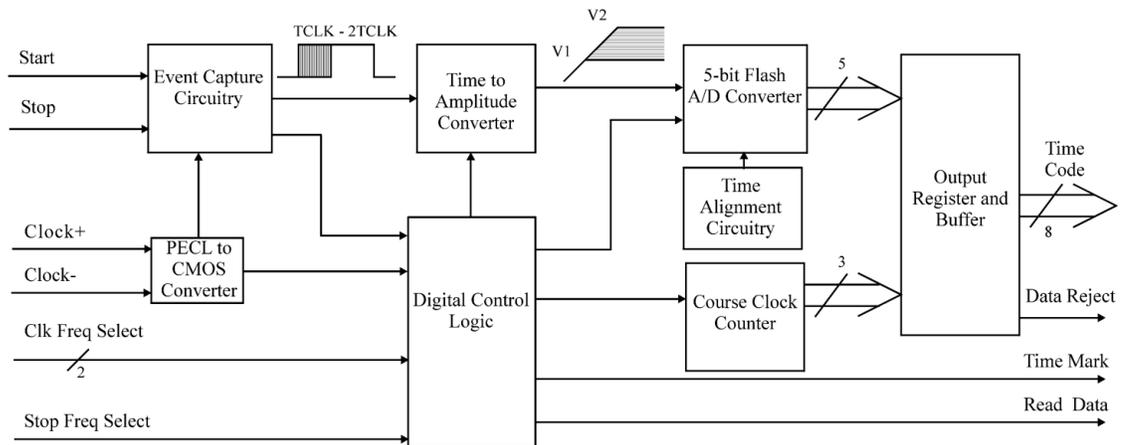


Fig. 9 Diagram of the TDC architecture for PET [10]

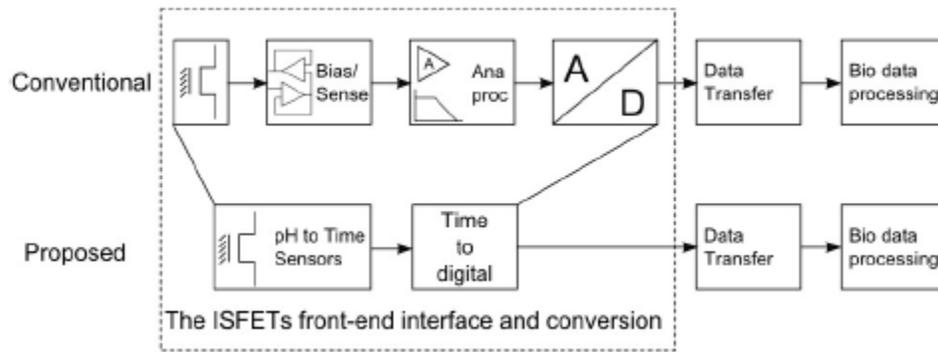


Fig. 10 Replacement of a conventional medical sensing system by TDC in ISFET [13]

1.4.3 Laser Rangefinder with TDC

A pulsed time-of-flight (TOF) laser rangefinder operates by means of measuring the flight time of a light pulse from a laser transmitter to the target and back to an optical detector, in which a receiver is needed to identify a time interval between the start signal coming from transmitter directly and the stop signal being reflected by the target (Fig. 11). A TDC could be expected to provide an excellent result (resolution) in time interval measurement over a wide detection range [14]. In order to improve residual timing walk

performance, a compensation scheme based on a high-performance multichannel TDC might be realized [15].

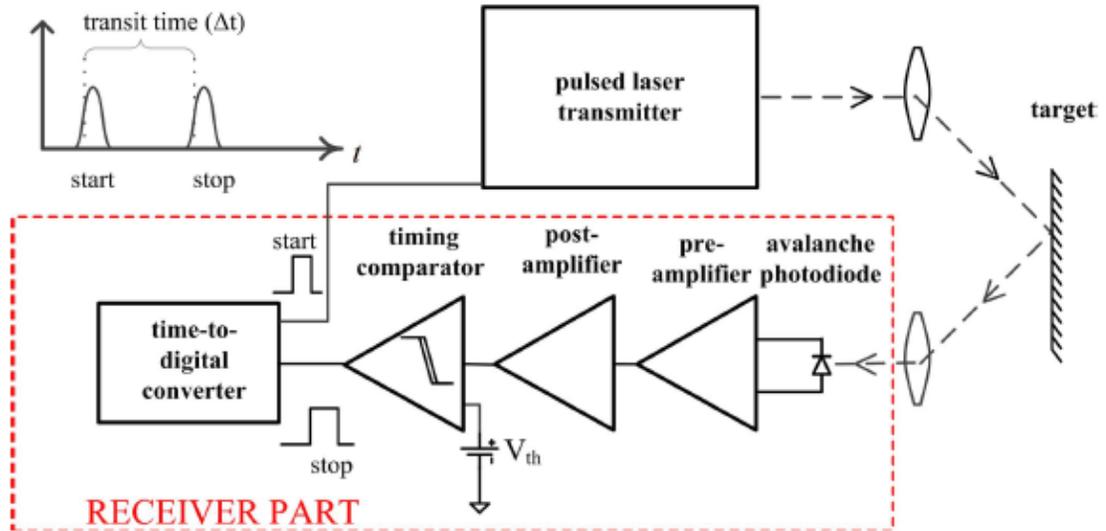


Fig. 11 Block diagram time of flight laser rangefinder [15]

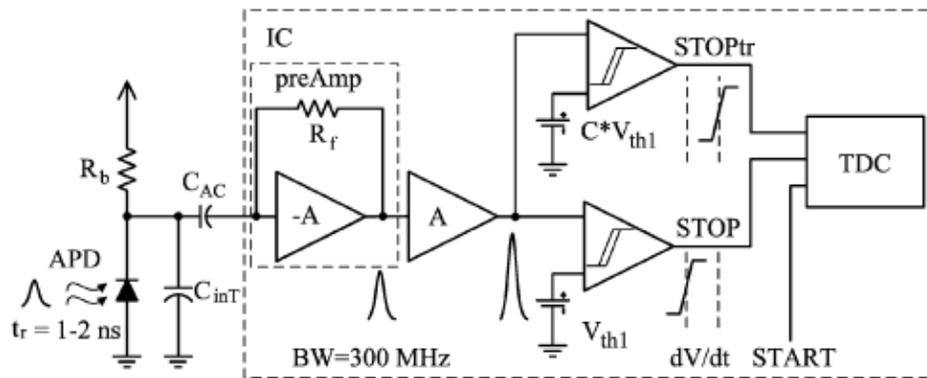


Fig. 12 Receiver chip with TDC for laser rangefinder [14]

1.4.4 Other TDC Applications

As a competitive approach to time interval measurement in digital format, the TDC has been widely employed in many other applications such as temperature sensors [16] [17], space science instruments [18] [19], etc. These applications benefit from TDC solutions and digital-intensive circuitry, which replace bulky analog elements such as

charge pumps, phase/ frequency detectors and passive filters within small geometry processes for the purpose of cost reduction.

In addition, different applications need TDCs with different performance characteristics. For instance, when aiming at a digital DLL application, a first-order noise shaping type TDC solution could improve the effective time resolution performance, benefiting in-band phase noise performance. However, the first-order noise shaping type TDC may be meaningless for improving the phase noise performance in the case of an ADPLL application, due to the accumulation of the FCW and integral counter in the modern ADPLL dominate the first-order noise shaping of phase error. This will be discussed in more detail later.

1.4.5 Research Focus

This research into the TDC's architecture and design will focus on an application in ADPLL synthesizer in the multi-giga-hertz frequency range.

1.5 Time-to-Digital Converter and Time Resolution Parameter

As mentioned in the section 1.3-1.4, to realize an ADPLL or DLL with high performance, a time-to-digital converter (TDC) is crucial because a TDC can provide finer time resolution of the quantitation of the fractional residue of the phase difference F_{Rn} (Fig. 6). The analysis of the TDC principle and design will be mainly based on modern ADPLL applications unless otherwise noted.

The TDC can measure and quantize the time interval (phase difference) (ΔT_{Tot}) between the edges of reference clock signal and the ADPLL feedback clock signal (DCO output signal), which corresponds to F_{Rn} shown in Fig. 6 (or Fig. 8 in the DLL). The digital-format of a TDC output allows for an accurate arithmetic operation in the

comparator, avoiding the issue of noise injection compared to an analog PLL's charge pump. However, every quantization operation has a finite accuracy because only a finite number of bits can be used to represent the digital output. The least significant bit (LSB) of the TDC output corresponds to the finest time segment that can be measured. This finest time segment of the TDC is defined as the time resolution of the TDC (T_{res}).

The time resolution of the TDC (T_{res}) is one of the most important TDC performance metrics, indicating the accuracy of resolving the timing difference of the reference (REF) and DCO edges. Therefore, with a linear conversion [20], the RMS phase error ϕ_{error} can be determined by:

$$\phi_{error} = 2\pi \cdot \frac{T_{res}/\sqrt{12}}{T_{DCO}} \quad (2)$$

where T_{DCO} is the period of the DCO output. This noise will be spread from dc to the sampling frequency (reference frequency, f_{ref}). Thus, the phase noise caused by the TDC is:

$$L_{\{\Delta f\}} = 10 \log_{10} \left[\frac{(2\pi)^2}{12} \cdot \left(\frac{T_{res}}{T_{DCO}} \right)^2 \cdot \frac{1}{f_{ref}} \right] \quad (3)$$

where $L_{\{\Delta f\}}$ stands for power spectral density (PSD) of the phase noise in logarithm unit (dBc/Hz).

Note that (3) represents the amount of TDC phase noise contribution in decibel units, which corresponds to the "Raw TDC" illustration in Fig. 13. Fig. 13 describes briefly the phase noise contribution of the DCO, TDC and overall ADPLL system versus the frequency offset from the carrier, in which index "raw" stands for the independent (original) phase noise contribution of the DCO or TDC without the loop filter effect. When

considering the loop effect, if the LF is implemented as a low pass filter, the amount of the overall TDC phase noise would remain the same as the raw TDC phase noise inside the loop bandwidth (in-band) and drop with constant slope (in dB) as the frequency offset increases outside the loop bandwidth (out-band). It means that once the TDC time resolution for a certain ADPLL is decided, the in-band phase noise caused by TDC will be determined. Note from the illustration in Fig. 13, the overall DCO in-band phase noise contribution maybe appreciably less than overall TDC phase noise contribution; so that the ADPLL in-band phase noise performance can be optimal. In a conclusion, pursuing a TDC with the finest time resolution performance should be the first priority, due to the fact that the TDC phase noise dominates the in-band phase noise performance of the ADPLL system.

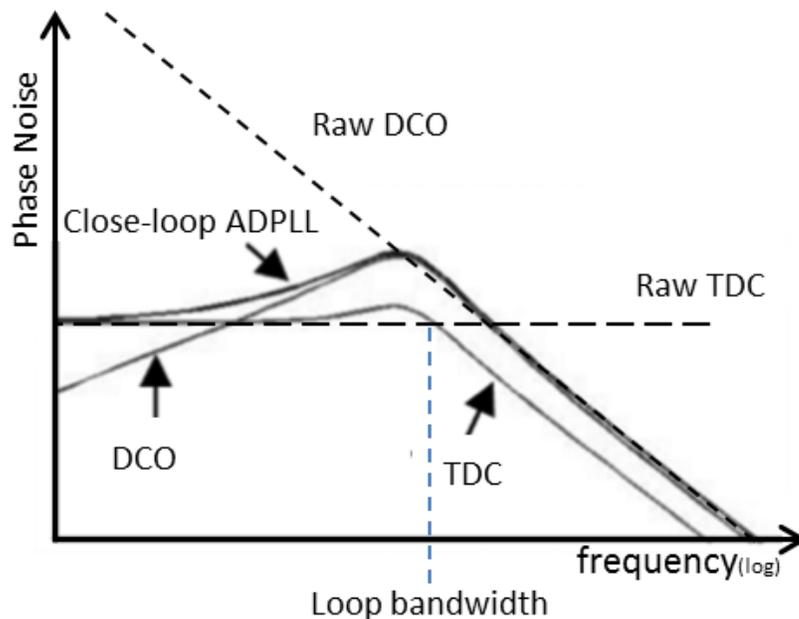


Fig. 13 Noise Contributions of TDC and DCO in an ADPLL loop

1.6 TDC Detection Range Parameter

In addition to being able to achieve a competitive phase-noise performance by improving the time resolution, the output of the synthesizer (ADPLL) also needs to be adjustable over a certain frequency range. For some demanding wireless applications, this frequency range could be relatively large. Considering the requirements of state-of-the-art ADPLL applications in the wireless field (television broadcast, mobile phones, wireless LAN, Bluetooth, ZigBee, GPS, microwave devices/communications, etc.), a modern ADPLL may be required to cover the frequency range from 90MHz to 8GHz. The TDC needs to be able to measure up to one period of the feedback signal (DCO signal), so the maximum required phase detectable range is defined as the maximum TDC phase detection range (ΔT_{Tot_max}), which corresponds to the time period value of the lowest frequency of the DCO signal, which could be applied. For an application requiring DCO output as low as 100MHz, ΔT_{Tot_max} should not be less than 10ns.

From the perspective of digital binary expression, the maximum phase (time) detection range of a TDC can be defined by how many output bits (X) it produces. The relationship between X (bits) and ΔT_{Tot_max} (time or phase) is:

$$\Delta T_{Tot_max} = T_{res} \cdot (2^X - 1) \quad (4)$$

For instance, a 10-bit TDC with 2ps resolution can detect up to 2ns of the maximum phase (time) detection range, while a 12-bit one can cover more than 8ns. Equation (4) implies that in the case of a fixed number of digital bits, the phase detection range gets narrower with the finer TDC time resolution, which means that a TDC design must trade-off time resolution for phase detection range.

In summary, a fine TDC time resolution combined with a wide phase detection range are the most important performance specifications in most wireless applications.

1.7 Other TDC parameters

Linearity of the quantitation of the TDC is supposed to be considered as a metric to ensure the practical phase noise performance is comparable to theoretical expectation. Integral non-linearity (INL) and differential non-linearity (DNL) are mostly used to assess the linear capabilities of output with sweep of the input. INL and DNL result in a degradation of the announced time resolution. The practical time resolution in a specific TDC design can be named as effective time resolution.

Note from (3), a higher reference frequency would improve the in-band phase noise performance of the ADPLL (decreasing the phase noise value). Thus, a TDC solution that allows a higher reference frequency is desired. This entails a short latency time of the TDC operation, this topic and research will be discussed in Chapter 4 and Appendix 1.

Low power consumption and small chip area are some of the most important considerations to achieve a relatively low-cost solution. A low voltage supply would allow an application in portable consumer products.

1.8 TDC Key Performances Specifications Summary

In summary, the TDC key parameters that need to be considered during research and design are listed as below:

- Time resolution, T_{res} , in ps or sub ps.
- Maximum phase (time) detection range, ΔT_{Tot_max} , >10 ns.
- Linearity of the quantitation.

- Low power consumption compared to current state of the art architectures.
- Small chip area compared to current state of the art architectures.
- Highest reference frequency available ($>50\text{MHz}$).

1.9 Thesis Outline

In Chapter 2 we will introduce the fundamental concept of TDC architectures and designs accompanied with some published literatures, focusing on the characteristics of the time resolution, maximum phase (time) detection range and other crucial performance parameters. The principles of a couple of typical delay-line based TDC designs as well as their advantages and disadvantages will be discussed in more depth.

Chapter 3 will discuss a crucial phenomenon called the parallel output misalignment (POM) effect which mainly takes place in a ring-type TDC. Based on the study demonstrated in the chapter, the noise injection due to POM error will degrade the overall phase noise contribution by up to 25dB.

Chapter 4 describes the proposed new TDC architecture, called the partially conjoined-ring Vernier TDC, and comprehensively describes the details of the proposed scheme including the system specifications provided and the circuit level specifications required for successful operation. It also provides the circuit level implementation of the TDC core, pre-logic circuitry and the evaluation unit of the TDC system. It also provides TDC timing considerations in order to achieve best phase noise performance by allowing a higher reference clock in the ADPLL system.

Chapter 5 introduces two implementations of the proposed TDC layout designs, and

their chip level fabrications, bonding and packaging plans.

Chapter 6 demonstrates the experimental results from various perspectives and the comparisons with other published researches.

Chapter 7 summarizes the overall proposed TDC designs and implementations as the conclusion of the thesis.

Chapter 2: Background

In this Chapter, the evolution of the TDC research and development during the past a few decades is briefly described. The studies of the TDC mainly focus on improving the performance in terms of time resolution, detection range and linearity as well as the cost in complexity and power consumption. Section 2.1 briefly introduces analog TDCs, which are used to measure the length of a certain time interval by analog means and then convert the analog result into a digital one. Section 2.2 describes inverter or buffer based TDCs which may be the first matured digital TDCs, although their performance is limited. Section 2.3 to 2.8 bring up the principles of some popular advanced TDCs, that are refined in one or more aspects of performance compared to the analog or basic digital counterpart. Section 2.10 emphasizes ring type TDCs and their advantage over non-ring types. It also mentions a complicated issue from parallel outputs of the ring type TDC. However, the details and analysis of this issue will be discussed in the next chapter. In the end of the chapter, a comparison table is built up to contrast the overall performance among the discussed TDCs.

2.1 Analog TDC

The first generation of the TDCs [21], [22], were mainly implemented by converting a time interval into an analog voltage potential and then transforming it by a traditional analog-to-digital converter (ADC). As shown in the block diagram Fig. 14, the time interval is defined by the edges of the start and stop signals. When V_p , a pulsed signal, is high the integrator senses and accumulates a voltage potential V_{eq} . V_{eq} is fed into the ADC to digitize the measured result. A delayed version of the stop signal is used to synchronize ADC output. This a straightforward and simple approach to create a TDC

based on an ADC. However, the linearity of the TDC has been proved to be a challenge at high-speeds due to the finite output resistance of the current source. Even if in an advanced version of an analog TDC is used in which an active RC integrator could be employed to replace passive integrator to address the above-mentioned issue, the speed limitation of the op-amp circuits remains.

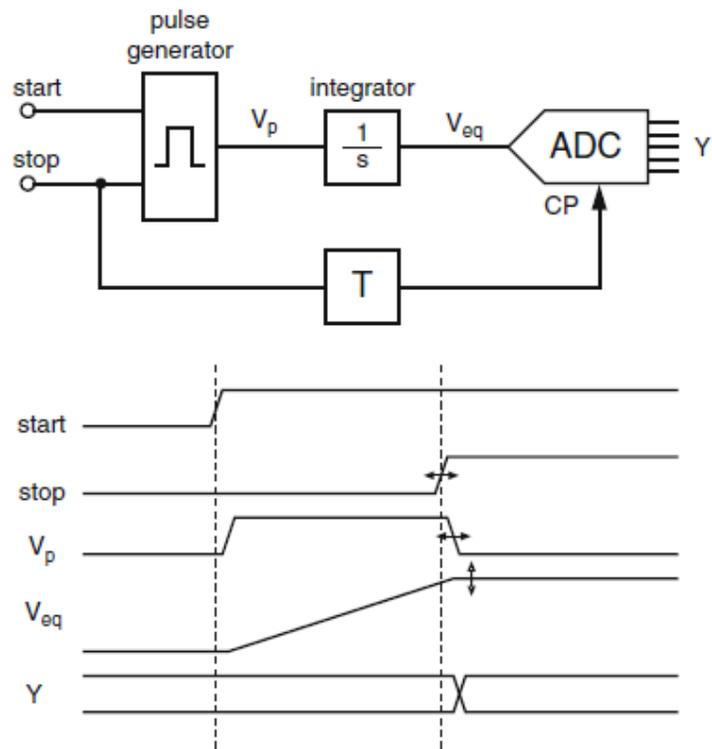


Fig. 14 Block and signal diagram of basic analog time-to-digital converter [23]

2.2 Inverter (or Buffer) Based TDC

Due to the motivation to meet more demanding requirements like linearity performance and flexible control in detection range, and the trend to use a more fully digital implementation, fully digital TDCs have become dominate in research and development in both academia and the industry. The first well-known generation of digital TDCs may be called delay-chain based TDCs [24], [25], [26], who's principle is shown in Fig. 15. A

delay-chain based TDC consists of a delay chain with N-stage delay elements, an arbiter set and a thermo encoding circuit. Each stage of the delay chain, being defined as delay element, can be an inverter or a buffer. An arbiter set is made of a set of D flip-flops.

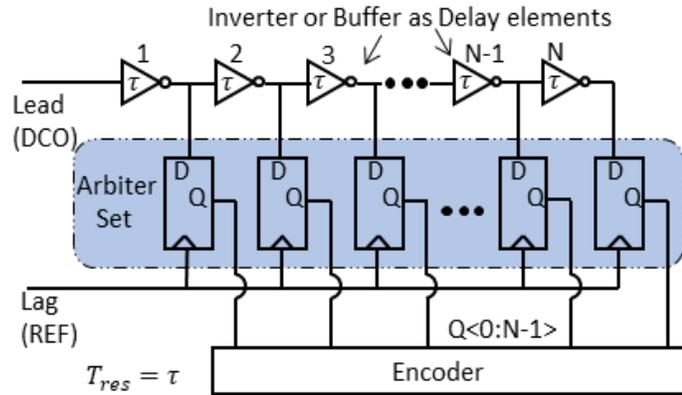


Fig. 15 Illustration of the principle of an inverter delay-line based TDC architecture

As mentioned, the inputs of a TDC are supposed to be two signals with a certain time interval which is usually defined by the difference between two signals' adjacent edges. As shown in Fig. 15, the leading signal (edge coming early) is fed into the delay chain, and the lagging signal (edge coming later) is used to trigger the clock terminals of the D flip-flop set. For a TDC applied into a PLL circuit, if a DCO (VCO) output is related to the leading signal, the reference signal will correspond to the lagging signal, or vice versa. The TDC starts a new measuring cycle with the rising edge of the leading signal appearing at the input node of the first delay element, since when the leading signal propagates along with the delay chain with a propagation delay (τ) after each stage. Later when the rising edge of the lagging signal (REF) arrives, it triggers the sampling of all D flip-flops in parallel. The state of each delay element's output (this can also be the data terminal of the D flip-flop set) at the moment is captured and stored as $Q\langle 1:N \rangle$ or $Q\langle 0:N-1 \rangle$ (a

thermometer code), which is the output of the D flip-flop as well as the input of a following thermo encoder which convert the amount of the arbiter's measurement from a thermometer version to a binary number.

Fig. 16 is an illustration of the timing diagram of the leading signal with its delayed signals appearing at nodes of a buffer-based delay chain and the lagging signal (assuming the REF signal is lagging behind DCO signal). The signal on any node of the delay chain has a duplicated version of the DCO signal and a constant delay (τ) compared to the signal at the adjacent preceding node. The total time delay of the signal at any node relative to the original DCO signal is proportional to the number of delay elements that have been passed through. Thus, when the reference signal triggers the clock of the D flip-flop set, the output of the arbiter set can be separated into two groups by the criteria of whether the state of the DCO signal has been passed or not. Note that the time resolution (T_{res}) capability of this TDC corresponds to the propagation delay of each stage of inverters or buffers:

$$T_{res} = \tau \quad (5)$$

Obviously, the former (close-in) part of the delay stages should be the ones that the DCO signal has past through, and the state of these should be inversed (low-to-high or high-to-low), while the rest of delay stages on the latter part haven't got a chance to change yet so that their stored state would be their original state. The illustration of the nodes' state of the buffer-based and the inverter-based delay chain with transition occurrence is shown in Fig. 17. Therefore, the location of the transition between change and nonchanged zones

of the state of the arbiter's outputs can indicate the time interval (or phase difference) (ΔT_{Tot}) between the edge of the DCO and of the REF in quantization by:

$$\Delta T_{Tot} = k \cdot \tau, \quad k = 1, 2, \dots, N \ \& \ k < N \quad (6)$$

where k locates at the particular digit of $Q \langle 1 : N \rangle$ where the state of the next adjacent digit is a different from. Note that k should not be larger than N , which is the total stage number of delays in the chain of the TDC core circuit. Apparently, the maximum phase detection range (ΔT_{Tot_max}) depends on the propagation delay of the delay chain and can be determined by:

$$\Delta T_{Tot_max} = N \cdot T_{res} = N \cdot \tau \quad (7)$$

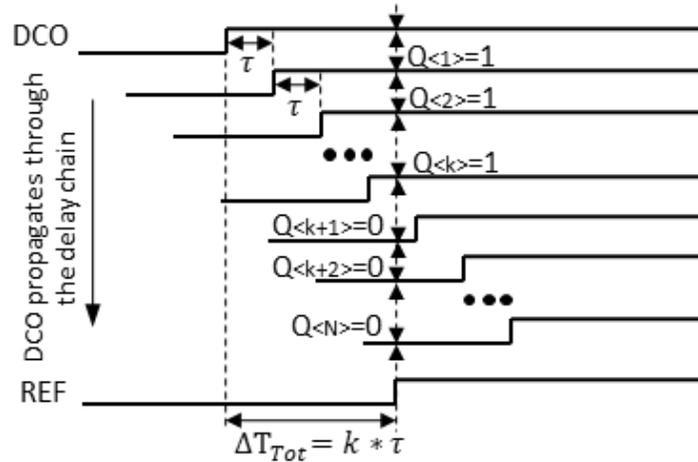


Fig. 16 Illustration of the signals at various nodes of a buffer-based delay chain of a TDC

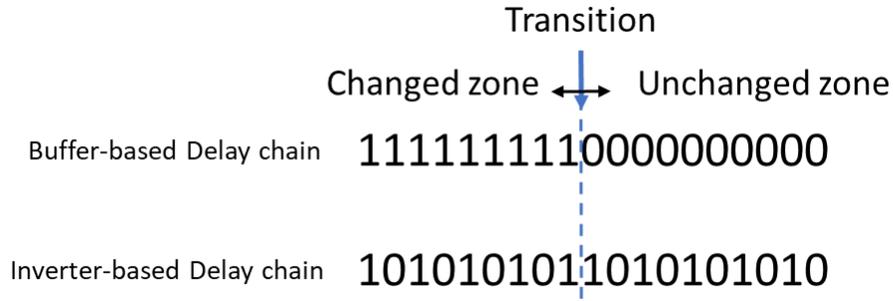


Fig. 17 Illustration of the nodes' state of the delay chain with transition occurrence

Basically, a buffer-based delay chain has a roughly doubled time delay (τ) in value compared to that of an inverter-based delay chain, simply due to a buffer being made of two inverters. Thus, in the aspect of time resolution performance, the inverter based TDC surpasses its buffer-based counterpart by a factor of 2. However, for an inverting delay chain structure, the output signals at an even order of the delay chain present an inverse state to that of the odd order of the delay chain, requesting different types of D flip-flops leading further mismatch. The unavoidable mismatch of transition curves between the rising edge and falling edge of the inverter results in uneven propagation time arriving at odd and even D flip-flops. The level of the mismatch can be alleviated by designing proper complementary pairs of PMOS and NMOS transistors for inverters, although it only works well in a typical situation and deviates with process, voltage and temperature (PVT) variations. In addition, as we consider the details of the operation of the D flip-flop, the setup time and hold time of D flip-flop to the rising edge of the data always differs from that of the falling edge of the data, as indicated in Fig. 18. Thus, the value of the mismatch affects the effective τ of the delay chain. Due to the above unbalanced even-odd characteristic inherited in inverter-based TDCs degrades the time resolution, and the overall improvement of time resolution of the inverter-based TDC over that of the buffer-

based TDC is much less than the expected factor of two. The relative INL and DNL of the inverter-based TDC are not as good as the expectation. The inverter-based TDC also has the additional risk of multi-transition (bubbles) taking place mostly when the skew of the overall delay between each pair of two adjacent propagation paths is comparable to τ in some extreme PVT situations.

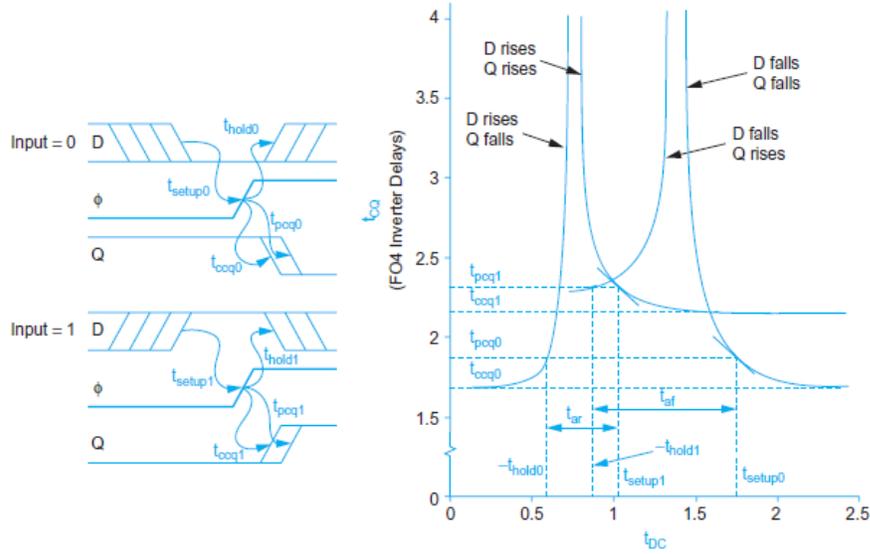


Fig. 18 D Flip-Flop response to reversed states [27]

In (7), the maximum phase detection range parameter, ΔT_{Tot_max} increases with the τ and the number of stages (N). As mentioned above, τ also limits the TDC time resolution T_{res} , thus increasing N is usually the desired way to meet a larger phase detection range with a reasonable time resolution figure. For instance, to detect a 1GHz DCO ($\Delta T_{Tot_max}=1000ps$) with 10ps of T_{res} , 100 stages of a delay chain are required. While, to detect a range, ΔT_{Tot_max} of 10ns (maybe in DLL or other applications), the required number of stages (N) would be 1000. Obviously, large N leads to a proportional cost in

chip area and power consumption, resulting in a less competitive or even an impractical TDC solution.

In conclusion, the time resolution performance of the basic delay chain based TDC is limited by the propagation delay of the delay element, which relies on the process employed in a semiconductor fabrication. An inverter-based TDC implemented in a 90ns process may have around 20ps of the propagation delay, i.e. time resolution. Also, to get enough phase detection range, a large number of stages in the delay chain is required, costing more in chip area and power consumption. Because of the triggering of the arbiter set occurring simultaneously (no delay chain located on lagging signal path), this type of TDC is called a flash TDC, which is often compared with the Vernier TDC discussed later this chapter.

2.3 Vernier TDC

The time resolution of inverter-based or buffer-based delay line TDCs is limited at the gate-delay level. A Vernier type TDC aims to improve time resolution to a sub-gate-delayed level [28] [23]. In a typical Vernier delay chain structure (Fig. 19), two delay chains are used for propagating the leading signal and the lagging signal respectively. The propagation delay of the delay element in the leading delay chain needs to be larger than that in the lagging delay chain. τ_1 and τ_2 are used to present the time propagations of the delay element for the lagging (fast) delay chain and the leading (slow) delay chain. The arrival of the leading signal edge always initiates the TDC core operation and its propagation through the slow delay chain. Then after a time interval, the lagging signal edge arrives and launches its propagation along the fast delay chain. A set of delayed arrivals of the lagging signal are used to lock and capture the state of delayed arrivals of

the DCO signal. Due to the lower propagation delay length of the fast delay element compared to that of the slow delay chain, the time interval between the delayed leading signal and the delayed lagging signal on corresponding pairs of nodes will be reduced by $\tau_2 - \tau_1$ when passing through each stage. This is illustrated in Fig. 20 in which the lagging signal seems like it is chasing the leading signal until it locks and captures the transition by finding first unchanged state of a delay chain node. Similarly, the output of the transition of the arbiter set indicates a certain number of delay elements that relates to the length of the time interval in:

$$\Delta T_{Tot} = k \cdot T_{res}, \quad k = 1, 2, \dots, N \ \& \ k < N \quad (8)$$

Where the formula is identical with the flash TDC. However, the time resolution T_{res} is not related to the gate delay of the transistor but determined by:

$$T_{res} = \Delta\tau = \tau_2 - \tau_1 \quad (9)$$

Where, the time resolution is determined by the difference of the propagation delay between slow and fast delay elements, and is able to achieve a sub-gate-delay time resolution with at least several times improvement compared to a flash TDC. To distinguish the competitive time resolution advantage of the Vernier TDC from the flash TDCs, $\Delta\tau$ is employed for the Vernier delay chain difference instead of τ . Ideally, $\Delta\tau$ could be reduced to close to zero and practically when this research topic was starting, Vernier TDCs with a 2 pico-second delay difference were studied, implemented and published such as [29].

$$\Delta T_{Tot_max} = N \cdot T_{res} = N \cdot (\tau_2 - \tau_1) \quad (10)$$

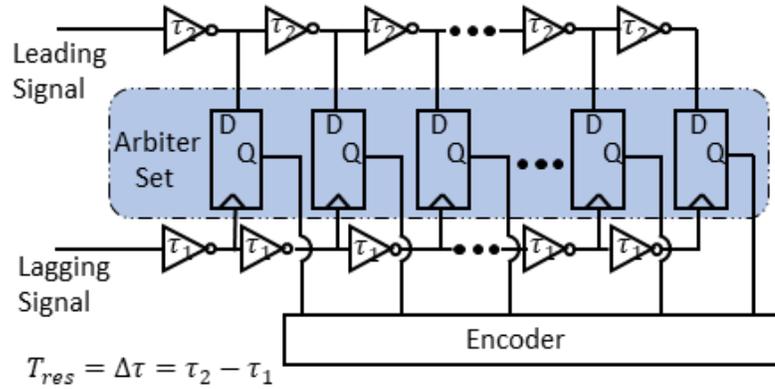


Fig. 19 Vernier TDC Structure

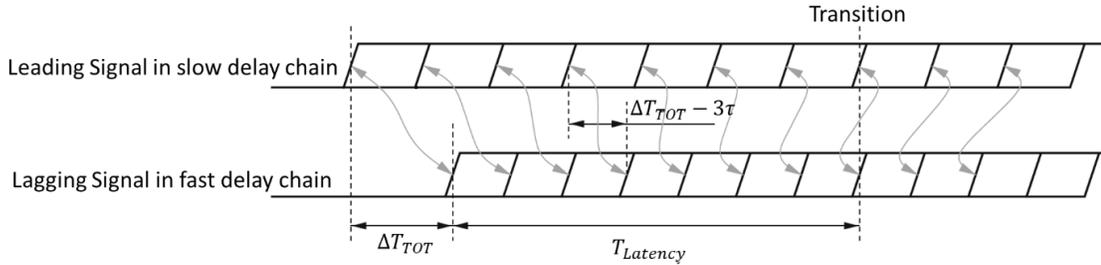


Fig. 20 Timing diagram of a Vernier delay chain TDC with $T_{res} = \tau = \tau_2 - \tau_1$

Compared to the flash TDCs, Vernier type TDCs improve the time resolution by a certain degree but at the same time they degrade the maximum time detection range. Maximum detection range can only be maintained at the cost of the multiplication of the number of stages needed in the delay chains to cover the same detection range. For example, aiming for T_{res} of 4ps and ΔT_{Tot_max} of 10ns, a Vernier TDC will require 2500 stages. The Vernier TDC may have a time resolution improvement by a factor of 5

compared to that of the traditional flash TDC at expense of 5 times the number of stages of delay chains, which will cause it to have a less competitive area & power consumption. In addition, it will take an extremely long time period ($\tau_1 \cdot N$) of the latency time to complete the lock of all arbiters' values ($Q < 1:N >$) and the storage of the register bank for further determination. In the case of $\tau_1 = 20ps$, the latency period could be up to $20 \cdot 2500 = 50ns$ which is impractical for the case where the frequency of the leading or lagging signal is 20MHz or higher.

A Vernier TDC also improves the linearity and the stability of the time resolution performance because to a first-order, PVT variations are automatically cancelled [28].

2.4 Ring Oscillator TDC

To avoid a very large number of the stages in the delay chain of a TDC, the ring oscillator structure has been developed [30], [31], [32]. As shown in Fig. 21, a ring type TDC is formed by connecting the output node of the last stage with the input node of the first stage of a delay chain (the blue line). By passing the signal through the same delay elements multiple times, a wide phase detection range is achievable. Besides the arbiter-set outputs of TDC delay chain, it is necessary to capture a parallel output from a counter which is used to count the number of the rotations of the signal through the ring structure (M). Thus, the evaluated result of the final TDC measurement can be determined by:

$$\Delta T_{Tot} = (M \cdot N + k) \cdot \tau \quad (11)$$

where k indicates the location of the transition of the delay chain outputs, and N is the number of the delay chain stages. The ring type TDC provides an excellent solution for a

large phase detection range requirement in terms of a low cost in chip area and power consumption. However, T_{res} is still limited to τ which is hard to shrink to 5ps or less even with an advanced process, making it unsuitable for the wireless applications with demanding phase noise performance. Note that it breaks the relationship of (7) and provides an advanced solution for a large phase detection range requirement with a reasonable cost in chip scale and power consumption. However, embedding a ring into a flash TDC cannot improve the time resolution to a sub-gate-delay level, making the traditional TDC or ring oscillator TDC less desirable for demanding applications.

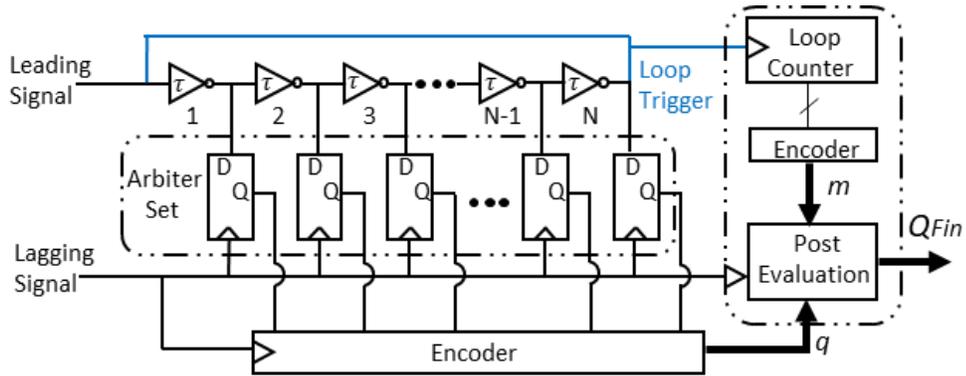


Fig. 21 Ring Oscillator TDC Structure

2.5 GRO TDC

A Gated-Ring oscillator TDC [33] is an advanced type of ring oscillator TDC. The GRO type delay chain (Fig. 22) is enabled when the control signal is in high state. During this period, the propagation of the transition of the delay elements is performed along the ring. This propagation behavior is disabled by the arrival of the falling edge of the control signal. The positive period of the control signal corresponds to the time interval (phase difference) to be measured. Every transition of the delay elements triggers a counter set

and an accumulator is used to count the number of the transitions during an effective enable period, i.e. length of the time interval.

Unlike the ring oscillator TDC in which the propagation of the transition behavior in the ring structure is entirely regenerated zero phase offset from the beginning of each operational cycle, the GRO TDC resumes the propagation of the transition behavior from the stage and even the phase where it stopped last round. This memory is due to the enable and disable controls on power supply of the delay elements, consequently, it controls the charge/discharge or idle to their loads. Thus, the residue state of the preceding measured time interval can be stored and accumulated to the next measured time interval, resulting in a first-order noise error cancellation (noise shaping in the frequency domain). This noise scrambling of the quantization on the dc transfer characteristics of a TDC benefits the effective time resolution performance of the TDC.

However, the GRO TDC structure causes an extra time-offset due to the immediate transition of the enabling control not being the case in practice. It also entails extra switch-transistors being inserted into each delay element and extra double-edge counters to be driven for each stage, causing a larger loading capacitance, which distinctly increases the transition time of each stage of the delay element. The above characteristic limits the propagation delay of each delay element, causing it to be inferior to its counterpart, the traditional ring oscillator TDC. Consequently, the overall improvement of the time resolution performance of a GRO TDC by first-order noise shaping will be degraded. In addition, the benefit of first-order noise shaping of the GRO TDC is distinct only in a delay locked loop (DLL), in which a similar cycle period between reference signal and feedback signal entails the TDC outputs are interpreted as a phase error. Conversely, in an ADPLL

system, the function of FCW accumulator block and integral counter block provide first-order noise shaping, and the extra first-order noise shaping of the TDC is unnecessary and meaningless in this application.

To make a GRO TDC work with high time resolution performance, multiple and fast-responding counters are also crucial considerations, which further multiplies the loading of the TDC core. Still even-odd mismatch of two adjacent inverters may cause linearity degradation and potential error of the TDC outputs.

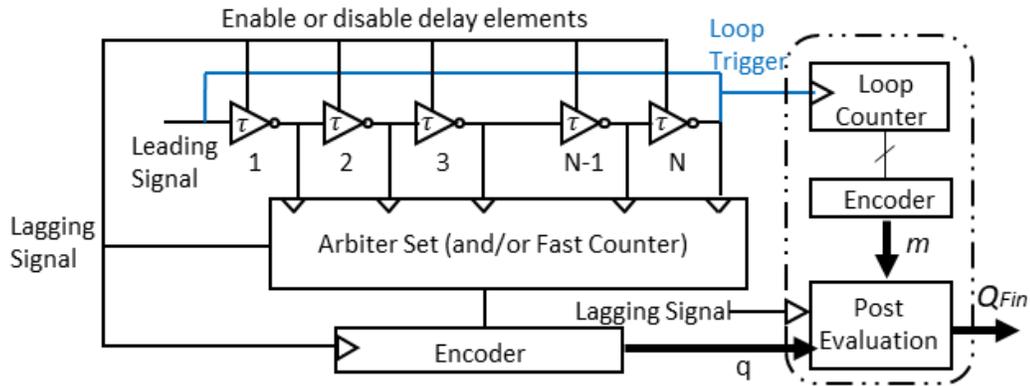


Fig. 22 Gated-Ring Oscillator TDC

2.6 Vernier Ring TDC

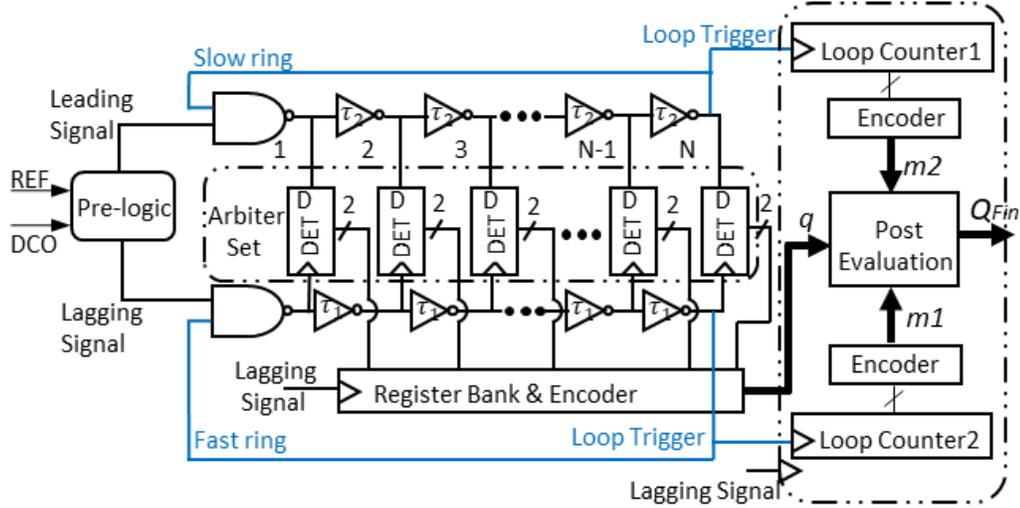


Fig. 23 Vernier Ring TDC Structure

By employing a ring type structure like the one in the ring oscillator TDC into a Vernier TDC, an advanced type of TDC called the Vernier Ring TDC (VRTDC) was developed aiming at both fine time resolution performance and wide phase detection range [34]. The principle of the VRTDC (Fig. 23) is to connect the output end terminal to the input terminal of each Vernier delay chain which has only a small number of stages. The leading signal and the lagging signal run laps (rotations) along their own delay chain loops until the judgment of the arbiters shows that the lagging signal has caught up to the leading signal. The reuse of the delay chains in the VRTDC greatly reduces the number of delay stages, facilitating an area and power cost reduction of the delay chain. Two counting units need to be introduced to record how many times the lagging signal and the leading signal traverse the entire loop when the lagging signal catches up with the leading signal. The final TDC result can be determined by:

$$\Delta T_{Tot} = (M_2 \cdot \tau_2 - M_1 \cdot \tau_1) \cdot N + k \cdot (\tau_2 - \tau_1) \quad (12)$$

The VRTDC requires a couple of extra demanding logic operations, which include a pulse generating pre-logic unit, double-scaled arbiter-sets for odd-rotation and even-rotation and a registration bank with fast reading and decision logical operations. Note that a pre-logic unit is a common treatment for TDC inputs, which is used for identifying and distributing two inputs for the leading signal path and the lagging one. As mentioned, it is usually embedded inside a pulse generator. Alternatively, it can be done by sampling one signal by the other one to ensure same average period of two inputs, avoiding bubbles (fake transitions). We will discuss the details later.

The VRTDC works correctly only if the above comprehensive considerations and corresponding complex logical operations can be performed with very high precision. However, a phase error due to a finite width of the negative pulse degrades the performance of the TDC occasionally. Overall, a VRTDC is one of the most effective and efficient TDC solutions, possessing fine time resolution performance, wide phase detection range and compact size due to a small number of delay stages. On the other hand, a VRTDC also requires a large amount of high-speed circuitry due to its two-ring structure and usage of the multi-capturing & multi-updating or the large register bank.

2.7 2-D Vernier TDC

A two-dimensional (2-D) Vernier TDC which is another advanced Vernier type TDC, focuses on sub-gate time resolution performance and at the same time it can leverage an enlarged detectable range with a reasonable increase of the delay chains' length. 2-D

Vernier TDCs usually include two delay chains and an array of time (phase) comparators [35] as its core. As shown in Fig. 24, an example of a Vernier plane (5 by 8), line x related to the leading signal propagation illustrates a slow delay chain with 8-stages and 5τ of the propagation delay of each delay element, whereas, line y for the lagging signal corresponds to a fast delay chain with 5-stage and 4τ of the propagation delay of each delay element. An array of time comparators is employed to decide the order of arrivals of each pair of signals among all possible combinations of two nodes from different branches of the line x and y. In the current example, a Vernier comparator array with size of 5 by 8 are formed. The 2-D Vernier TDC provides roughly a square times increase in the time detection range, although the effective region (the gray region in Fig. 24) is separated from the array by cutting two dummy corner parts (in up-left and bottom-right) away. However, a 2-D Vernier TDC brings in an extra 1st-order nonlinearity issue due to the folding point error, causing the effective time resolution performance to be rippled or even a bubble issue due to PVT variations. A $\Sigma\Delta$ modulator might be used to randomize the folding error, alleviating systematic noise contributed from it. A 2-D Vernier TDC can be expanded to a spiral 2-D Vernier TDC [36] which arranges the comparator line with shorter distance as folding occurs, aiming at an improvement in linearity performance compared to the traditional 2-D VTDC. Like the conversion from a Vernier TDC to a Vernier ring TDC, 2-D VTDC can be converted to a ring type to further shrink the stage number of the delay chains. Similarly, a GRO type could be also embedded to form a 2-D gated Vernier TDC [29] as well.

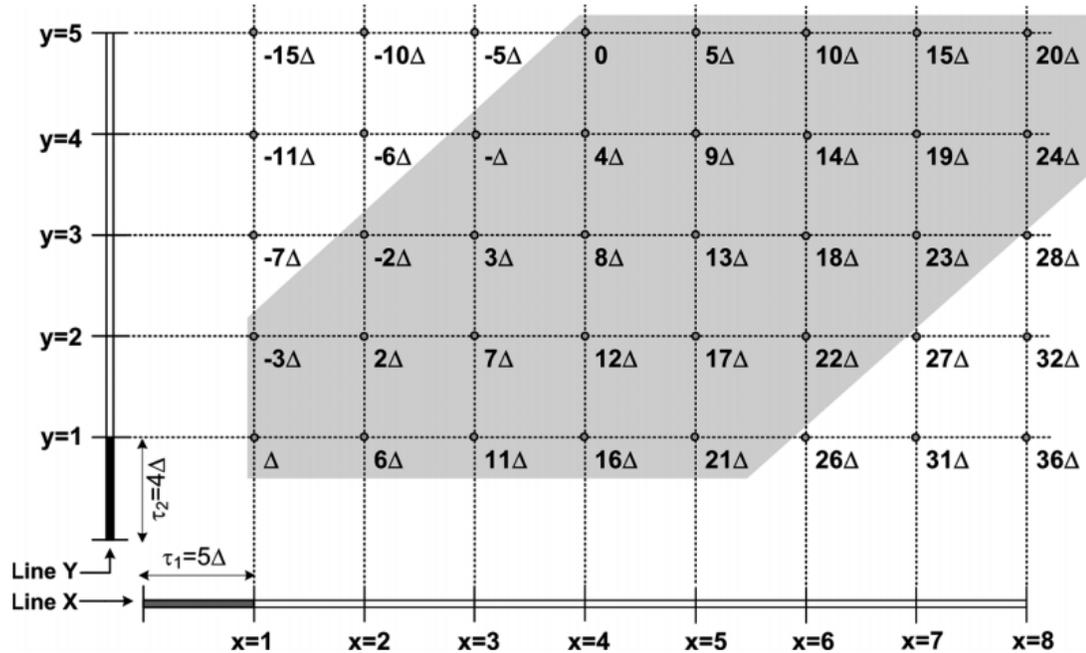


Fig. 24 2-Dimensional Vernier TDC operational plane

2.8 Time amplifier (TA) TDC

A time amplifier TDC is a TDC that amplifies a time residue by a set of (shifted) SR latches [37] or by a pulse-train generation [38] in order to improve time resolution performance. A two-hierarchy structure (two-step) with coarse and fine time resolution is common for a time amplifier TDC application in which the time amplifier circuit is used to bridge two TDC cores, enlarging the time residue of the transition delay element in the first TDC core by a large gain (in the time dimension), allowing a further measurement and quantization by the second TDC core. Ideally, the time resolution performance could be ultra-competitive due to the hierarchical amplification and quantization. However, the effective linear performance of a time amplifier TDC depends on the linearity of the response of the output to the input time residue in the applied range and the offset and mismatch that the TA circuit brings in. In [37], a shifted SR latch delay circuit is applied

as the function of the time amplifier, in which the linearity is available in a range close to the origin. Like a Vernier type, the TA type would improve time resolution at the expense of scaling up the complexity of the circuit mainly in the second hierarchy. Therefore, the limitation of the scale of the second hierarchy constrains the delay chain length of the first hierarchy. A ring type delay chain may be a solution for the first hierarchy for expansion of the overall detectable range of a TDC. A competitive conversion rate (short latency) performance has been achieved in [38]. The power consumption of TA-TDC is relatively high compared to a flash type and Vernier TDC.

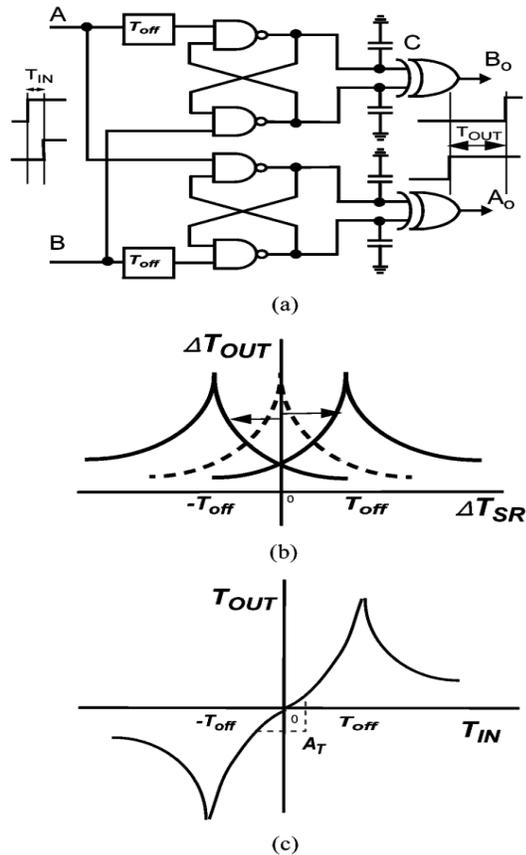


Fig. 25 (a) Concept of a TA. (b) Shifted SR latch delay characteristics. (c) TA characteristics.

[37]

2.9 Other TDCs and Techniques in Tandem

The stochastic TDC (STDC) exploits the stochastic properties of a set of latches to achieve high resolution capability [39] but at the cost of big fan-out load (power consumption as well) and nonlinearity issue (when large bits needs) caused by its typical principles. [40] shows an extreme example in which by employing stochastic-based branching structures, it achieves sub-picosecond time resolution capability at the expense of 70mw of power consumption of the core circuit.

There have been some other advanced TDC designs published that are combined with several classic TDC types mentioned in previous sections to form a novel type of TDC to gain an extra advantage in some specific respects. Readers can check with them ([41] [42] [43]) as interested. Also, [44] provides a review literature of TDCs by describing new architectures along with their benefits and trade-offs, as well as their implementation and suggests suitable use cases for the various techniques. Table1 briefly summaries the performances contrast among the variety of TDC techniques.

Table1: Feature of different types of TDCs

TDC type	Time resolution performance τ or $\Delta\tau$	Phase detection range capability ($\Delta T_{Tot,max}$)	Length of delay chain(s) requested (N)
Flash TDC	Coarse	Moderate	Long
Ring-Oscillator TDC	Coarse	Wide	Short
GRO TDC	Moderate	Wide	Short
Vernier TDC	Fine	Narrow	Super Long
Vernier-Ring TDC	Fine	Wide	Moderate
2-D Vernier TDC	Fine	Moderate	Moderate

Time Amplifier TDC	Fine	Narrow	Moderate
Ring type embedded			
2-D Vernier or TA TDCs	Fine	Wide	Short

2.10 Ring type embedded TDC

After the above introduction of different TDC types, it is noticed that the fine time resolution is traded for the detection range with a constant stage numbers of the delay chain. However, this constraint might be broken by embedding ring type structure(s) into each original TDC. Thus, state-of-the-art TDCs that are embedded ring structure(s) have been getting popular due to their capability of avoiding a very large number of stages in TDC delay chain(s) and meanwhile maintaining a wide time-length detection range. Since a loop (ring) can carry the signal along itself continuously, it leverages the availability of reusing and leads to a huge shrinkage of the number of core stages. By using this advantage, the time-length detection range can be scaled up as needed without increasing the TDC length. Therefore, the ring type TDC competitively satisfies demanding requirements at low complexity and cost, compared to non-ring type TDCs [45]. However, the ring type TDC needs parallel outputs for the final TDC result calculation. Because these operations are asynchronous, changes in the value of M never align with the carry-over-action of k , resulting in computing-errors. Consequently, a ring type TDC intrinsically produces extra phase noise due to the parallel-computing-error, degrading the in-band phase noise performance of the TDC. The details and analysis of the computing-error issue will be discussed in the next chapter.

Chapter 3: POM Effect Analysis

In this Chapter, a phenomenon mostly taken place in the ring-type delay chain TDC is discussed, which is called parallel output misalignment (POM). The description of why and how the POM effect occurs in a ring type TDC has been presented in section 3.1. The consequence of the introduction of the POM effect (error) is described in section 3.2 qualitatively in various design schemes. Section 3.3 focuses on the noise injection to phase noise PSD caused by the POM error quantitatively. POM_{dB} is defined and determined in this part as well to find the factors that directly impact the POM effect. The conclusion is given in the last section.

3.1 Ring type TDCs and their Multiple Outputs

Fig. 26 illustrates three types of TDCs that are embedded with ring structure(s). It is noted that in Fig. 26 (a) or (b), a single ring structure is employed to a flash TDC, which has only one delay chain, to form a ring-oscillator TDC and GRO TDC respectively. Whereas in Fig. 26 (c), a 2-ring structure is introduced to a Vernier type TDC, which has two delay chains, to form a Vernier ring TDC. We will see in the below description that the ring(s) structure adds extra input(s) for evaluating the final output result of the TDC.

Generally, for a one ring flash TDC, the delay chain and the loop counter are activated by the edge of the leading signal and are shut down by the edge of the lagging signal. During this active period, the transition of the leading signal keeps propagating along the looped delay chain, and every time it runs to the output node of the last stage it triggers the loop counter. Once the edge of the lagging signal comes up, both the D flip-flop arbiter-set and the loop counter are expected to be triggered to lock their outputs simultaneously. Then

the parallel numerical outputs will be sent to the post evaluation circuit for the final TDC output calculation. Here q is used to represent the decimal number of the stages (location) where the serial N-bit binary output of the arbiter-set transit and m is the numerical output of the loop counter.

If a single edge triggered loop counter is applied, one cycle of the propagation corresponds to completing two rotations of the transitions (one rotation with the symbol of the falling edge arriving and the other rotation with the symbol of the rising edge arriving). The final output, q_{fin} can be represented by:

$$q_{fin} = \frac{\Delta T_{Tot}}{T_{res}} = m \cdot 2N + N \cdot S_D + q \quad (1)$$

where ΔT_{Tot} stands for the time interval to be measured, defined by the edges of the reference signal (leading signal) and the feedback signal (lagging signal), T_{res} represents the time resolution of the TDC core, and N is the number of stages of the delay chain. S_D equals 0 at the odd rotation and equals 1 at the even rotation. q is between 0 and $N-1$. Equation (1) is plotted in Fig. 27 with $N=8$ as an example. As the time interval (ΔT_{Tot}) increases, q increases accordingly and overflows every N increments. Note that every second time that q is refreshed back to 0, m rises by 1, and q_{fin} is computed using the measured m and q values and the value of N and is supposed to increase linearly (in steps) and monotonically.

An alternative approach is to use a double edge triggered loop counter, by which the loop trigger comes on each rotation and q_{fin} can be represented by:

$$Q_{Fin} = \frac{\Delta T_{Tot}}{T_{res}} = m \cdot N + q, \quad (q < N) \quad (2)$$

Equation (2) is plotted in Fig. 28 with $N=15$ as an example. As the time interval (ΔT_{Tot}) increases, q increases accordingly and overflows every N increments. Every time that q is refreshed back to 0, m rises by 1, and q_{fin} is computed using the measured m and q values and the value of N . It is noticed that the requested double operating speed of the double-edge loop counter limits the stage number of the delay chains and consequently does so on the overall performance, compared to the single-edge version.

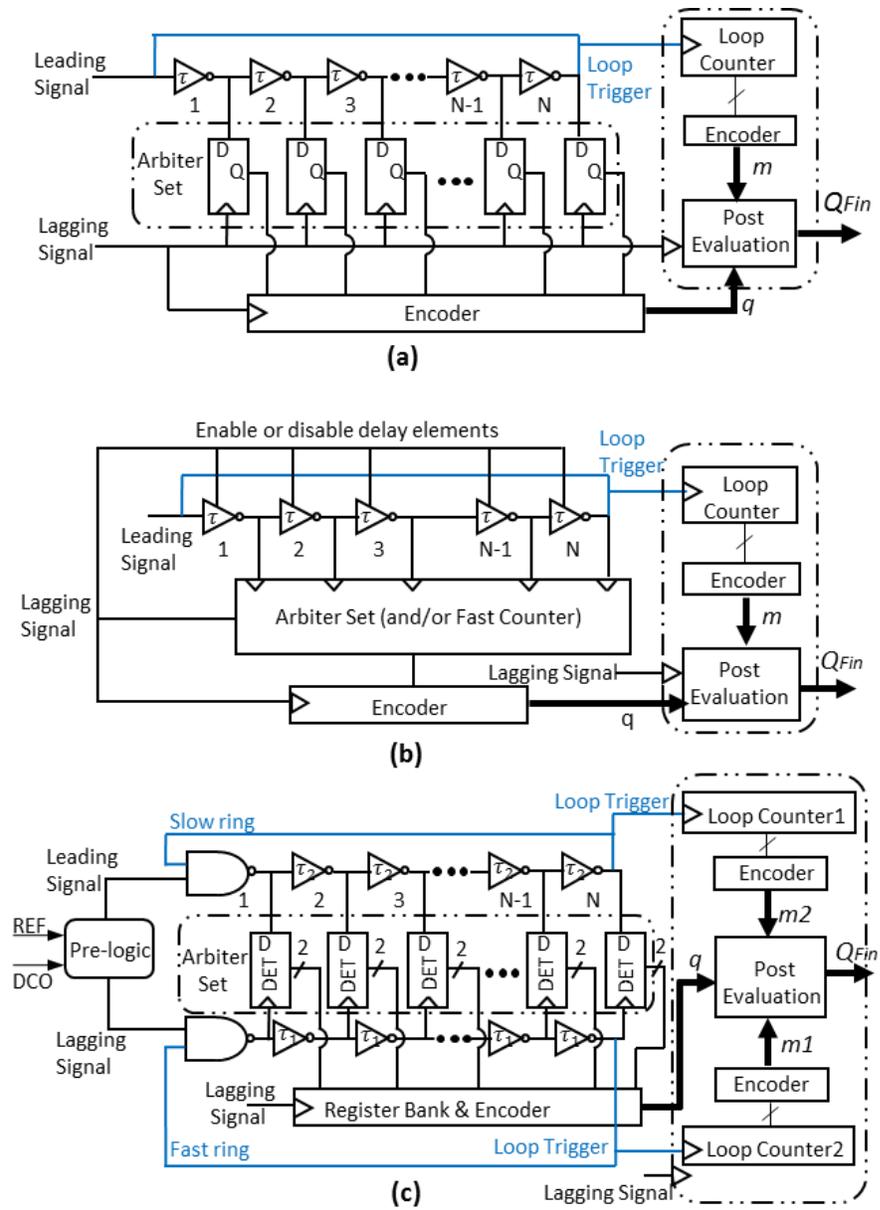


Fig. 26 Ring type TDC diagrams (a) ring-oscillator TDC, (b) GRO TDC, (c) Vernier ring TDC.

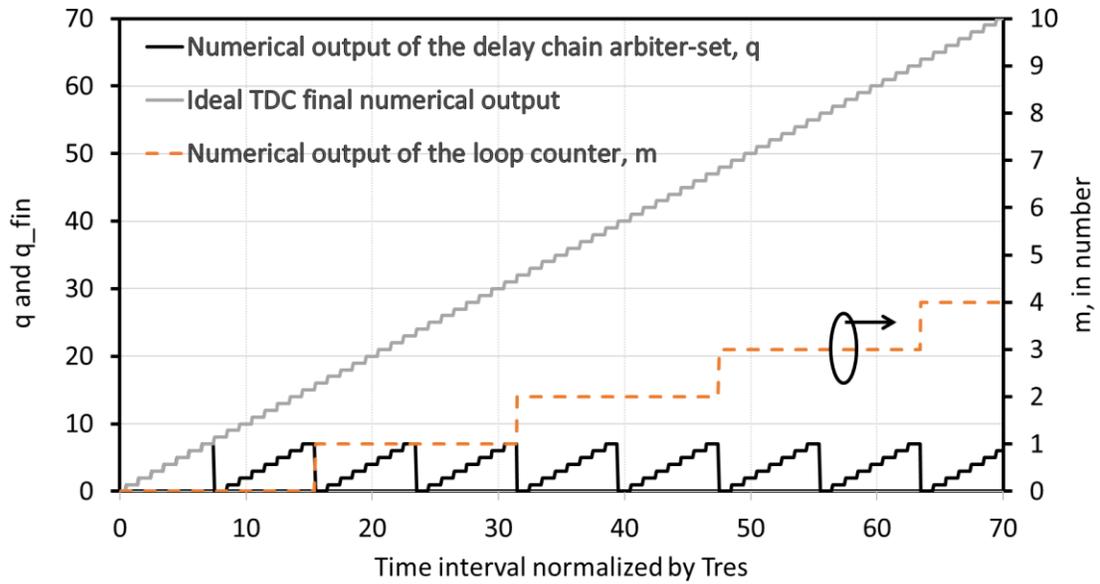


Fig. 27 Ideal Transfer characteristic of a single ring-type TDC ($N=8$) with a single-edge triggered loop counter

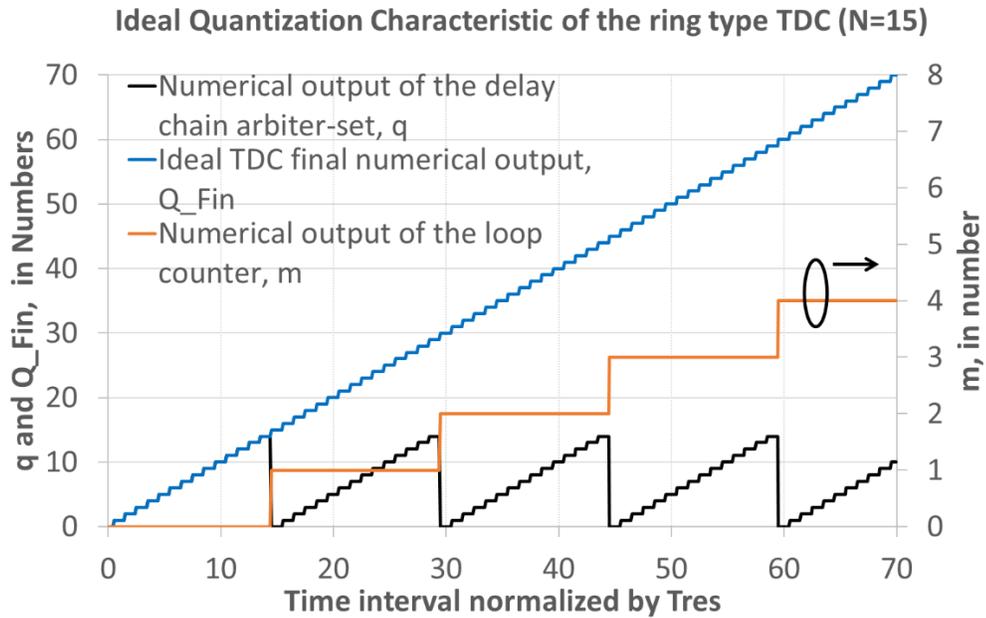


Fig. 28 Ideal transfer characteristic of a single-ring-type TDC ($N=15$) with a single-edge triggered loop counter

For a 2-ring TDCs, like the Vernier-ring TDC (Fig. 26(c)), the final TDC output, Q_{Fin} can be represented by:

$$Q_{Fin} = \frac{\Delta T_{Tot}}{T_{res}} = \frac{(m_2 \cdot \tau_2 - m_1 \cdot \tau_1) \cdot N}{\tau_2 - \tau_1} + q \quad (3)$$

where m_1, m_2, q respectively stand for the fast-ring loop counter, the slow-ring loop counter, and the arbiter- set output.

Now if we look at the relationship between ring structure and the factors (outputs) that cause the final TDC output, it is realized that the number of the outputs would be determined by:

$$Num_{Out} = 1 + Num_{Ring} \quad (4)$$

Where Num_{Out} stands for the number of the medium-process outputs that determine the final output and Num_{Ring} represents the number of the ring structures embedded into the core circuit. Note that “1” corresponds to the delay chain output and for a non-ring TDC where the final output depends only on the delay chain output. Another example as in the Vernier TDC mentioned above and (3), m_1, m_2, q are the medium outputs, in which q is from delay chain output and m_1, m_2 correspond to the fast and slow ring outputs. We define the medium outputs of the ring type TDC as the parallel outputs. All the medium outputs should be collected synchronously to generate the correct result.

3.2 Parallel Outputs Misalignment (POM) Effect

As shown in Fig. 27 and Fig. 28, q_{fin} is supposed to be expected to increase linearly (step by step) and monotonically with the time interval. This is true only when the point of

the time interval where the change in m is same to where q overflows. In other words, m , the loop counter updates and q the delay chain arbiter refreshes should take place simultaneously to make the system generate a correct result in all cases. However, the truth in practice is the two immediate time instants can never be aligned with each other perfectly, no matter how accurately the circuit operates. Specifically, although m and q are locked by the same trigger clock (lagging signal), the data-to-output delay of the loop counter cannot be the same as that of the arbiter-set. In conclusion, the misalignment among the parallel outputs is unavoidable in a raw ring-type TDC. It is noticed that a computed error of Q_{Fin} appears when the point of the time interval which makes m change is not aligned with the point that makes q overflow. This phenomenon is named the parallel-outputs-misaligned (POM) effect.

The transfer characteristic in Fig. 27 would convert to the one with large spikes illustrated in Fig. 29, due to occurrence of the POM effect. The spikes caused by POM will always be seen in the sweep the time interval parameter provided the sweep range is across the overflow of the output of the delay chain arbiter set. Note that the granularity of the increments of the time interval needs to be fine enough to guarantee the recognition of the POM effect (spikes). If the time interval sweep range is enlarged sufficiently, the POM spikes can be found periodically in every N for a double-edge counter design or in every $2N$ for a single-edge one. The spikes are related to the sharply huge unwanted change of the final output due to mismatched computing. Spikes point upwards when the loop counter output's incremental change takes place whereas, the arbiter set output is not refresh yet. We call this a prior-POM effect, corresponding to the case of m changing prior to q overflowing. On the other hand, a named lag-POM effect occurs when the point at

which m changes lags q overflowing, and spikes are directed downwards. The amount of the error due to POM is summarized below:

	1-ring double-edge loop counter	1-ring single-edge loop counter	multi-ring TDC
Prior-POM	N	2N	Depends on design
Lag-POM	-N	-2N	Depends on design

Note that a multi-ring TDC design usually encounters mis-alignment issue between more outputs, causing a more complicated POM effect. The details of the POM effect are dependent on the specific circuitry of the TDC. Let us focus on a 1-ring TDC for now. It is the case that either the pure lag-POMs or the pure prior-POMs phenomenon taking place during the operation of a certain physical TDC device. After briefly looking into the magnitude of the spike, now let us see the width of it. As shown in Fig. 29, the width of the spike is determined by the mismatch between the m increment and q overflow in the time dimension. The mismatch is due to the data-output delay and clock-output delay of an m decision differing from those of the q decision. A straightforward idea to address the mismatch can be to add a time delay circuit into the branch with the shorter delay so as to reduce the width of the mismatch (POM width), T_{POM} (Fig. 30), reducing the proportion of the occurrence of the misalignment over the whole sweep range. With a careful design and accurate implementation, T_{POM} may be minimized to a level less than 1ps. However, it is risky for a too small T_{POM} to make POM error toggle between the lag-POM and prior-POM in PVT variations, leading to a more complex situation to tackle.

In fact, the POM error caused nonlinearity in a ring type TDC has a similar mechanism as the nonlinearity caused by a comparator array folding error in a 2-D Vernier TDCs [35].

Both the POM error and the folding error come from the occurrence of the mismatch among the multiple parallel TDC outputs. They both occur periodically with increased time interval and once the error happens, the amount of the error may be much larger than 1 LSB. [36] presents a randomization method to minimize the folding error in the 2-D Vernier TDC.

In next section, the POM effect, and its impact on the phase noise of the frequency synthesizer will be analyzed quantitatively. It will be shown that even 1ps of T_{POM} may adversely affect the phase noise by up to tens of dB.

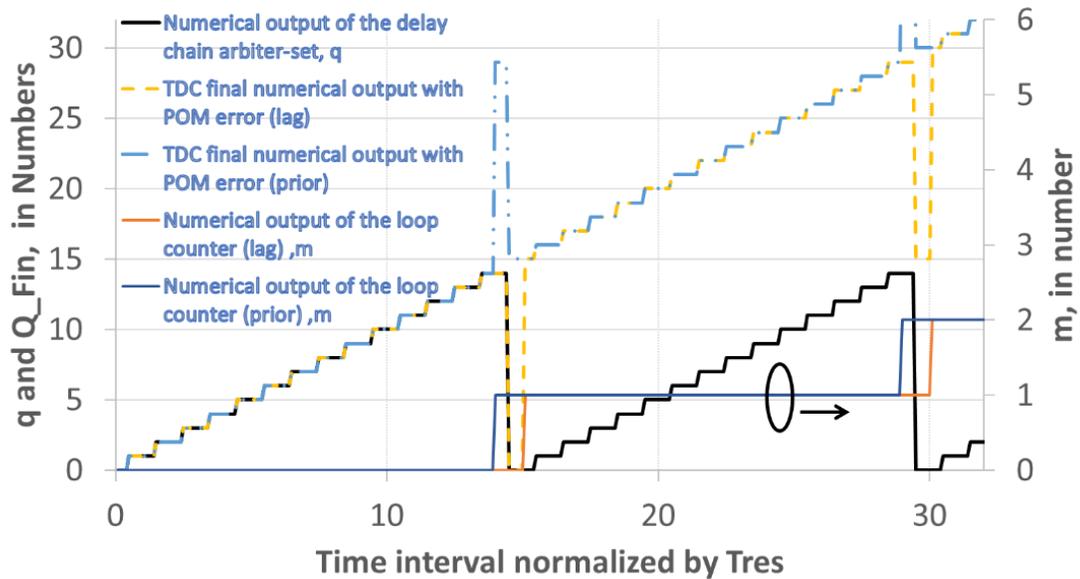


Fig. 29 Practical transfer characteristic of a single ring-type TDC (double-edge counter)

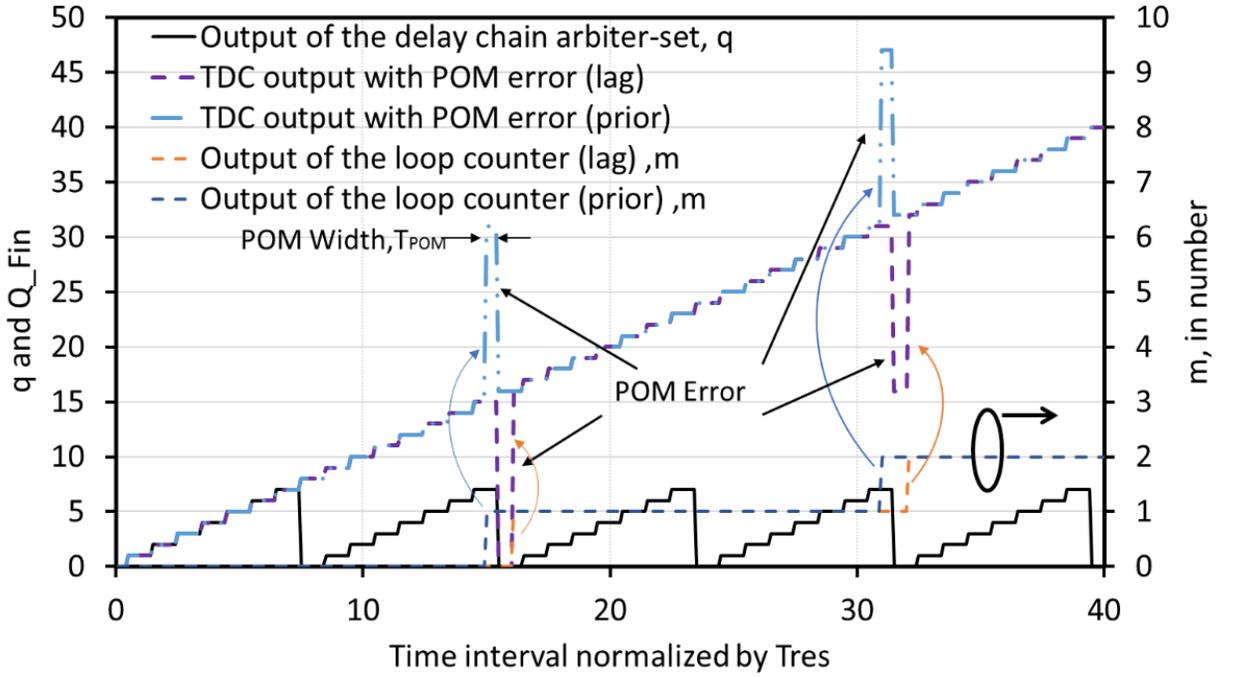


Fig. 30 Practical transfer characteristic of a single ring-type TDC (single-edge counter)

3.3 POM Effect Quantization

Before the POM effect quantitative analysis is performed, the TDC quantization error and its phase noise contribution to the ADPLL's output is briefly discussed. The time resolution of the TDC, T_{res} is the most important performance metric, indicating the accuracy of resolving the time interval, ΔT_{Tot} . E_0 is defined to express the normalized amount of the smallest increment of the resolution [46], and thus, is determined by:

$$E_0 = \frac{T_{res}}{\Delta T_{Tot_{max}}} \quad (5)$$

where ΔT_{Totmax} is the maximum value of the time detection range. To simplify the calculation, ΔT_{Totmax} is assumed to be equal to the cycle period of output signal, T_{DCO} . Thus, E_0 can be determined by:

$$E_0 = \frac{T_{res}}{T_{DCO}} \quad (6)$$

As we knew in [47], the mean square error caused by quantization is:

$$\overline{\epsilon^2} = \frac{s}{E_0} \int_{-E_0/2s}^{E_0/2s} (st)^2 dt = \frac{E_0^2}{12} \quad (7)$$

where s is the slope of the transfer characteristic curve (black curve in Fig. 31) and ϵ , the magnitude of the error, is equal to st within the range between $-E_0/2$ and $E_0/2$. Substituting (6) to (7) and converting to the phase domain, the root-mean-square (RMS) phase error, $\Phi_{errorQUAN}$ can be represented by:

$$\Phi_{errorQUAN} = 2\pi\sqrt{\overline{\epsilon^2}} = \frac{2\pi}{\sqrt{12}} \cdot \frac{T_{res}}{T_{DCO}} \quad (8)$$

Assuming a uniform distribution of the quantization noise, the phase noise spreads evenly from dc to the frequency of the sampling signal (i.e. reference signal, f_{ref} , in an ADPLL system) offset. The TDC quantization error and its phase noise contribution to the fractional-N DPLL (Fig. 32) output is represented as:

$$L_{\{\Delta f\}QUAN} = 10 \log_{10} \left[\frac{(2\pi)^2}{12} \cdot \left(\frac{T_{res}}{T_{DCO}} \right)^2 \cdot \frac{1}{f_{ref}} \right] \quad (9)$$

where $L_{\{\Delta f\}QUAN}$ stands for the power spectral density (PSD) of the phase noise in dBc/Hz between zero and the reference frequency offset.

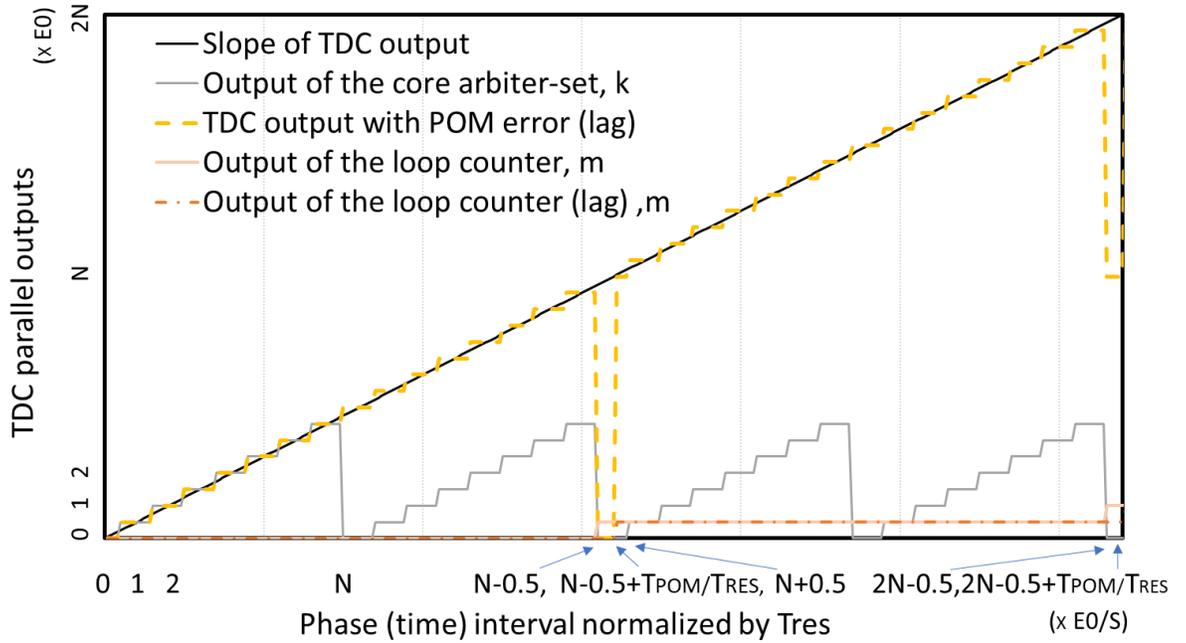


Fig. 31. Quantization characteristic of a raw 1-ring TDC (single-edge loop counter)

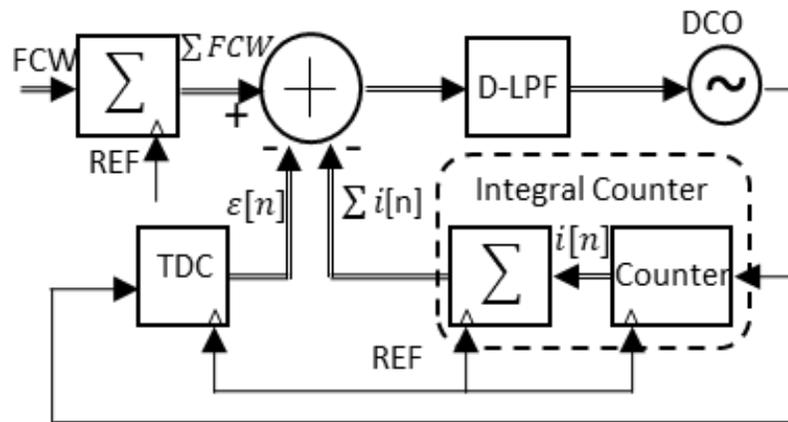


Fig. 32 DPLL system diagram with the TDC applied.

Similar to the calculation of the quantization error, the mean square error caused by the POM error is able to be determined. Taking the lag-POM phenomenon of a single-edge loop counter solution as an example, the mean square error is determined by:

$$\overline{\epsilon_{POM}^2} = \frac{s}{2NE_0} \int_0^{(2N-0.5) \cdot \frac{E_0}{s}} 0 dt + \int_{(2N-0.5) \cdot \frac{E_0}{s}}^{(2N-0.5 + \frac{T_{POM}}{T_{res}}) \cdot \frac{E_0}{s}} (2NE_0)^2 dt \quad (10)$$

It is turned out after the simplification as:

$$\begin{aligned} \overline{\epsilon_{POM}^2} &= \frac{s}{2NE_0} \cdot (2NE_0)^2 \cdot \frac{E_0}{s} \cdot \frac{T_{POM}}{T_{res}} \\ &= 2N \frac{T_{POM}}{T_{res}} E_0^2 \end{aligned} \quad (11)$$

For a double-edge loop counter solution, (11) becomes:

$$\begin{aligned} \overline{\epsilon_{POM}^2} &= \frac{s}{NE_0} \cdot (NE_0)^2 \cdot \frac{E_0}{s} \cdot \frac{T_{POM}}{T_{res}} \\ &= N \frac{T_{POM}}{T_{res}} E_0^2 \end{aligned} \quad (12)$$

Note that the magnitude of the mean square error of the double-edge loop counter solution is half of that of the single-edge one. To simplify the analysis, the double-edge case will be used to for phase error calculations. Substituting (6) into (12) and converting to the phase domain, the RMS phase error of the POM, $\phi_{error_{POM}}$ can be represented by:

$$\begin{aligned}
\Phi_{error_{POM}} &= 2\pi \sqrt{N \frac{T_{POM}}{T_{res}} \cdot \frac{T_{res}}{T_{DCO}}} \\
&= 2\pi \sqrt{N \cdot T_{res} \cdot T_{POM}} \cdot \frac{1}{T_{DCO}}
\end{aligned} \tag{13}$$

In general, when mapping the input (time interval) value in a large sampling set, the input may occur randomly over the whole range which forms a uniform continuous distribution. Thus, the phase noise caused by the POM error should be similar to that caused by the TDC time resolution quantization, spreading from dc to f_{ref} and its PSD value can be determined by:

$$L_{\{\Delta f\}_{POM}} = 10 \log_{10} \left[N \frac{T_{POM}}{T_{res}} \left(\frac{2\pi T_{res}}{T_{DCO}} \right)^2 \cdot \frac{1}{f_{ref}} \right] \tag{14}$$

The magnitude of the phase noise caused by the POM effect turns out to be worse than that of the TDC's quantization error. The random POM error occurrence in the time domain is illustrated in Fig. 33 (a), which spikes indicate the random POM error whereas the rippled floor indicates the quantization error or noise. Fig. 33 (b) demonstrates the power spectral density of the quantization error and random POM error. It can be found that the random POM phase noise contribution could be worse than that of the pure quantization error by 22dB on average. Therefore, the overall phase noise caused by the TDC is dominated by the POM effect instead of the quantization error.

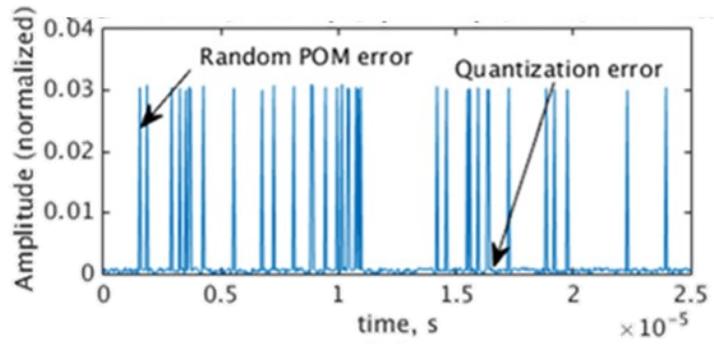
Fig. 34 illustrates the phase noise contribution with the time resolution changed and a sweep of the stage number of the delay chain N at T_{POM} equals 1ps (the best achievable T_{POM} in a raw ring type TDC). With constant T_{POM} and N , both $L_{\{\Delta f\}_{POM}}$ and $L_{\{\Delta f\}_{QUAN}}$

improve as the time resolution is decreased. However, due to the 1st order of T_{res} 's weight on $L_{\{\Delta f\}_{POM}}$ but the 2nd order of T_{res} 's weight on $L_{\{\Delta f\}_{QUAN}}$, the degradation due to $L_{\{\Delta f\}_{POM}}$ compared to $L_{\{\Delta f\}_{QUAN}}$ becomes large. An increased N (25) can also cause a worse overall phase noise contribution by up to 25 dB. The larger the value of N used in a delay chain, the worse of phase noise contribution caused by POM would appear.

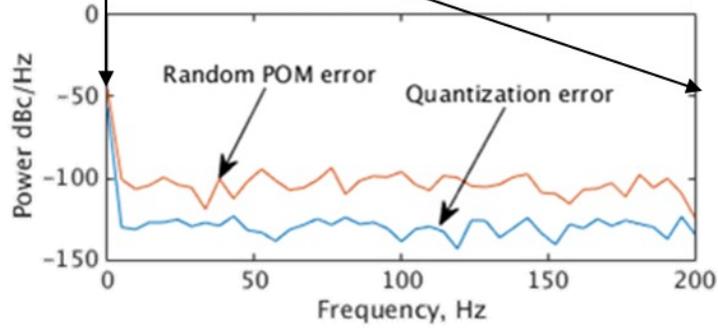
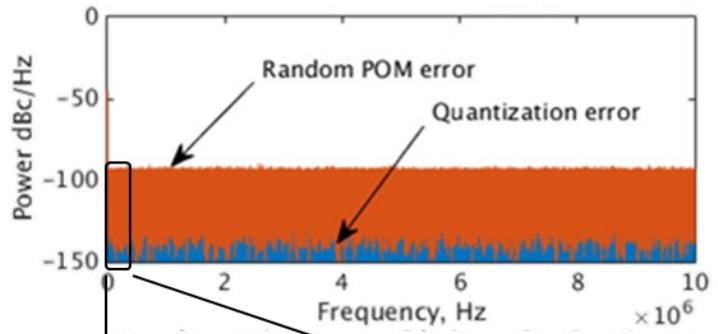
A coefficient, POM_{dB} is defined to indicate how much the phase noise was worsened by a POM effect, compared to that only caused by the linear quantitation error in dB. Thus, by subtracting (9) from (14) POM_{dB} is achieved as:

$$\begin{aligned} POM_{dB} &= L_{\{\Delta f\}_{POM}} - L_{\{\Delta f\}_{QUAN}} \\ &= 10 \log_{10} \left[12 \cdot N \cdot \frac{T_{POM}}{T_{res}} \right] \end{aligned} \quad (15)$$

The advantage of using the POM_{dB} is that it is independent of the system parameters like f_{ref} or T_{DCO} , and is only affected by the TDC parameters (N, T_{POM}, T_{res}).



(a)



(b)

Fig. 33 POM effect for random occurrence in (a) time domain (b) frequency domain

(fref=20MHz, fdco=1GHz, Tres=2ps, Tpom=2ps, N=15)

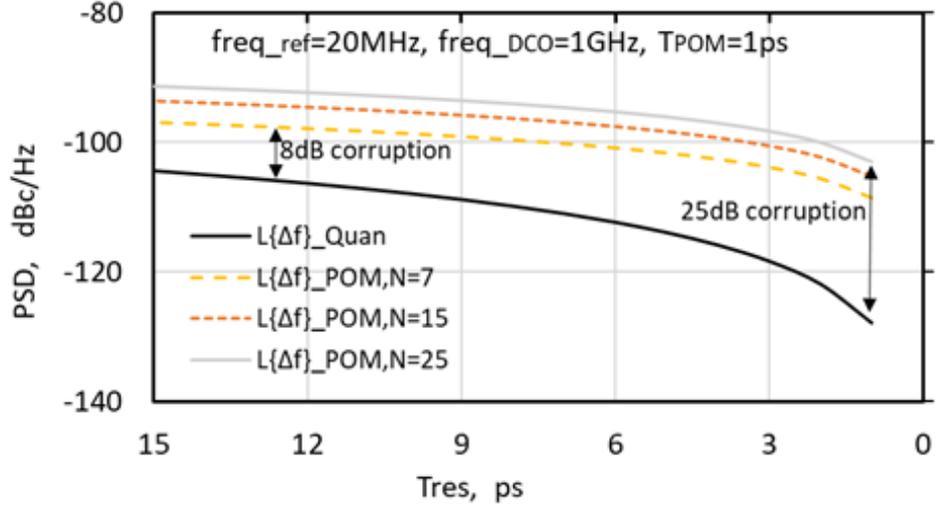


Fig. 34 PSD due to POM effect and quantization error

In some situations of TDC operation (in an ADPLL), rather than random occurrence and uniform distribution, the POM error occurs periodically in the time domain (Fig. 35 (a)). The impact of periodical-POM errors differs from that of random-POM errors and is discussed below.

Assume the loop filter in an ADPLL is neglected for now and the probability of the periodical-POM error is the same as that of the random-POM error. The periodical-POM error can be expressed as:

$$\epsilon[n] = \sum_{k=0}^{\infty} N E_0 \cdot \delta[n - kN] \quad (16)$$

Where E_0 corresponds to the LSB. The Fourier coefficient of the Fourier transform of (16) would be:

$$a_k = \frac{1}{N} N \cdot E_0 = E_0 \quad (17)$$

Thus, the magnitude of the spectral distribution of (16) can be expressed in the frequency domain. For an angular frequency it is:

$$X[e^{jw}] = 2\pi \cdot E_0 \sum_{k=-\infty}^{\infty} \delta \left[w - \frac{2\pi f_{ref} k}{N} \right] \quad (18)$$

or in frequency as:

$$X[\Delta f] = 2\pi \cdot E_0 \sum_{k=-\infty}^{\infty} \delta \left[\Delta f - \frac{k \cdot f_{ref}}{N} \right] \quad (19)$$

The PSD of the periodical-POM effect appears as discrete spurs. Ideally, the bandwidth of each spur occupied is zero and the power of each spur compared to that of the carrier, $L_X[\Delta f]$ in dBc is:

$$L_X[\Delta f] = 10 \log_{10}(2\pi \cdot E_0)^2 \quad (20)$$

The distance between any two adjacent spurs is:

$$D_{spur} = \frac{f_{ref}}{N} \quad (21)$$

Usually, D_{spur} is wider than the bandwidth of the loop filter in a DPLL, and the spurs are all located in the outer band of the loop filter. As shown in Fig. 35, the periodic-POM example, -39dBc/Hz of $L_X[\Delta f]$ and 1.3MHz of D_{spur} have been found. Note that the choice of the bandwidth of the loop filter is based on the point of the cross-section between the PSD curve of the raw DCO and that of the TDC quantization [9]. Assuming a loop filter with 100 kHz of bandwidth and a 40dB/decade of roll-off in the stop-band is used,

the first and the second sideband spurs may be as high as $-83\text{dBc}@1.3\text{MHz}$ offset and $-95\text{dBc}@2.6\text{MHz}$ offset, compared to -121dBc/Hz of quantization error caused phase noise.

In practice, it is prone to toggle between the periodic-POM and the random-POM.

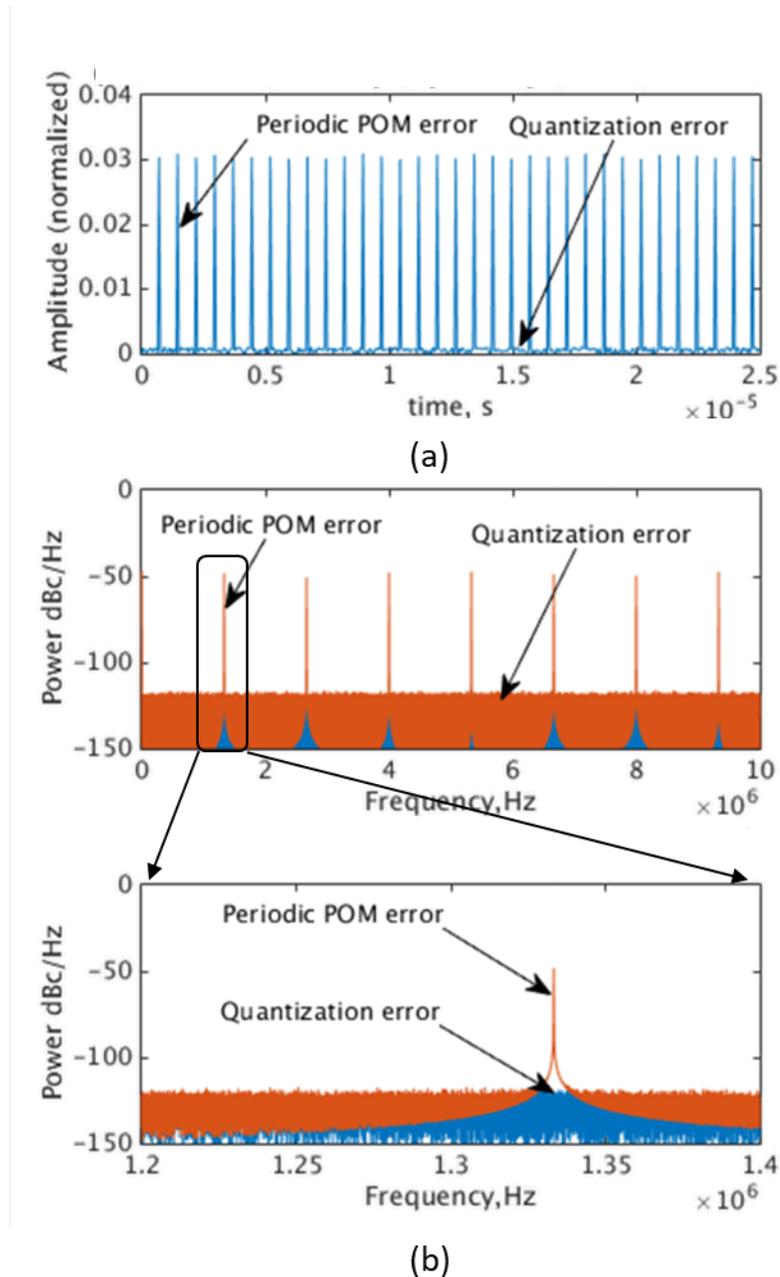


Fig. 35. POM effect for periodic occurrence in (a) time domain (b) frequency domain

($f_{ref}=20\text{MHz}$, $f_{dco}=1\text{GHz}$, $T_{res}=2\text{ps}$, $T_{pom}=2\text{ps}$, $N=15$)

3.4 Comparison between POM Correction and Glitch Correction

It is realized that there is a method called glitch correction as mentioned in [48] which seems to deal with the same problem as POM error in first view. But when we compare more details of them, it can be seen that the two correction methods face different kinds of issues in different situations respectively.

One key distinction in the reference paper [48] (as shown in **Fig. 36**) is that the phase output (to be evaluated and corrected) is predictable to be a constant number and the glitch is about the mismatch between the DCO Counter and TDC. In steady state, the phase output is supposed to be constant and same to FCW value.

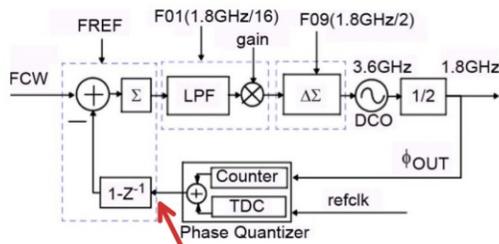


Fig. 9. Digital control loop. **Phase output for the whole feedback signal**

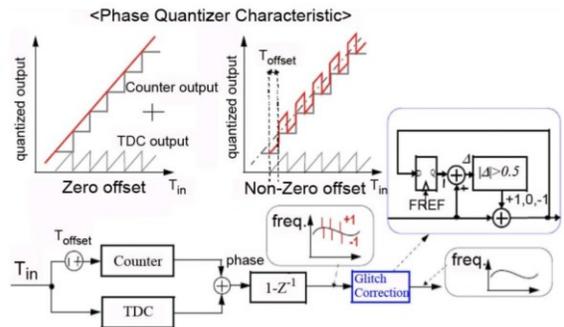


Fig. 11. Glitch detection and cancellation.

Fig. 36 Glitch correction scheme in [48]

Thus, this is not hard to deal with this glitch if we consider the glitch issue only in the steady state. A lowpass filter could be used to follow the block to solve it or ignoring the current round of samples and making use of the next sampling result. However, the effect of the additional lowpass filter could be added onto the whole PLL loop system, degrading the loop filter rejection to DCO noise over the outside band range. When we consider the unlock or acquisition process, with the mentioned glitch correction circuit the PLL can be

expected a shrinkage of the pull-in range (limiter of the pull-in range). Thus, it might bring extra noise and/or a larger ripple of the carrier by using the mentioned glitch correction.

In this paper, The POM is not between the DCO counter and TDC but between the TDC core output and the loop counter output. And the key point is the phase output of the sum of the loop counter and TDC core is not predictable and not linearly increase or being constant (no matter in lock-in state or acquisition process).

3.5 Conclusion

This chapter analyzes the parallel output misalignment and POM effect qualitatively and quantitatively. It also presents the impact of the phase noise contribution caused by the POM error. A detailed analysis for a 1-ring TDC has been performed. The intrinsic POM effect causes a significant degradation of the phase noise performance in both random POM and periodic POM situations. The phase noise injection due to the POM error could be up to a few tens of dB higher than the phase noise caused by TDC time quantization.

The analysis for a multi-ring POM effect would be dependent on the specific scheme and be much more complicated. Consequently, the measures used to address the POM for a multi-ring design could be proportionally more complicated.

Therefore, only pursuing an improvement of the time resolution performance without addressing the POM error issue could be futile. In next chapter, a novel architecture that employs a 1-ring structure to sidestep the complicated POM error situation from multi-ring type, and at the same time provide a measure to distinguish and treat the POM error of the

proposed 1-ring TDC circuit, so as to completely remove the noise injected by POM error will be presented.

Chapter 4: Conjoined-Ring VTDC Architecture and Pre-Design

This chapter mainly focuses on presenting a proposal on a novel TDC architecture and circuit design that has achieved the following advantages over others:

- Create a correction circuit that can distinguish the occurrence of the parallel output misalignment during its operation so as to eliminate unwanted noise injection caused by the POM error.
- In the meantime, retain the high performances especially in terms of a fine time resolution and extendable phase (time) detection range.
- Build up a configurable digital control to enable a tuning time resolution function and achieve a superior sub-pico-second performance.
- Achieve a competitively short latency time characteristic by creating a new structure, allowing higher reference frequency to be applied for better in-band phase noise performance.
- Realize a freely switchable coarse/fine resolution scheme so as to achieve the best figure of merit considering both resolution performance and power consumption.
- Address the metastability issue by employing a double-sampling circuit. Furthermore, it is able to eliminate the tiny phase variation.

Section 4.1 introduces how this idea was derived. Section 4.2 shows the block-level designs as well as the formula for the computation. According to the ADPLL specification described in appendix 2, the TDC specification is deduced in section 4.3. In section 4.4 the details of the pre-design of the core circuit have been demonstrated. The function of a pre-logic circuit, a fast loop-counter circuit, a POM-error correction and the whole evaluation circuit are presented in sections 4.6, 4.8, and 4.10, respectively. The considerations of the latency time capability and the choice of the design parameters are performed in section

4.5 and 4.7. The transistor level design of the TDC and its implementation will be described in the following chapters.

4.1 The Idea of a Partially Conjoined Ring

In the preceding chapter, the analysis of the parallel output misalignment (POM) effect implies the complexity of the analysis of imported errors and the noises they cause, which relies on the number of rings that the delay chain employs. It could be much harder to address the POM issue in a 2-ring (or multi-ring) design due to more misaligned scenarios being the cases that need to be considered and treated. On the other hand, due to the advantage of the ring structure mentioned earlier, it is undesirable to give it up.

Thus, it was hoped to invent a single ring structure which can replace the regular two-ring structure in the known ring-type TDCs. Secondly, owing to the competitive performance of Vernier type TDCs in time resolution, especially being reliable in PVT variations, we also hope a Vernier delay chain can be retained in the proposed TDC design. As the time of this writing, all published design and implementations of Vernier type TDCs that are combined with ring-structures use the same number of rings as the number of delay chains. This rule is true in Vernier ring TDCs, GRO VTDCs and 2-D Vernier ring TDCs.

A method to realize the use of only one ring for a double delay chain structure and make the TDC work is demonstrated in this thesis in Fig. 37. It is illustrated that a vernier TDC can be refined by embedding a short wire (connector) into the slow delay chain, such that the looped stages can operate as a ring oscillator that would repeat the propagation periodically when the leading signal is carried on it, and hopefully, the ring oscillator part

does not impact the operation of the Vernier delay chain itself. The details of its operation and constraints will be discussed in section 4.2 and 4.3.

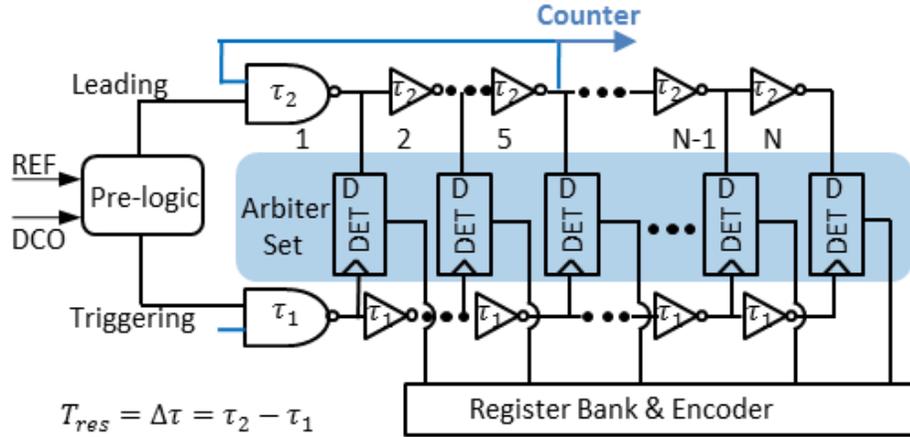


Fig. 37. Simple Illustration of the idea with only one ring in the Vernier delay chain.

4.2 Block Level Function Design and Considerations

As a continuation of the brief description in Section 4.1, the targeted TDC core circuit (**Fig. 38 (a)**) is designated to be comprised of a coarse resolution block implemented by a ring oscillator, a fine resolution block realized by a Vernier delay chain, and an assistant circuit used to coordinate the operations between the ring oscillator (the coarse detection circuit) and the Vernier delay chain (the fine detection circuit). The whole TDC module also includes pre-core and post-core circuits in order to integrate the whole function.

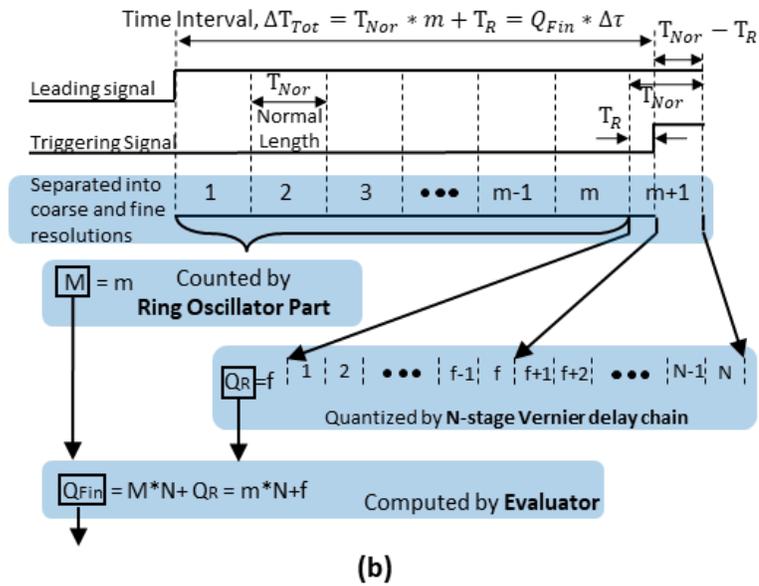
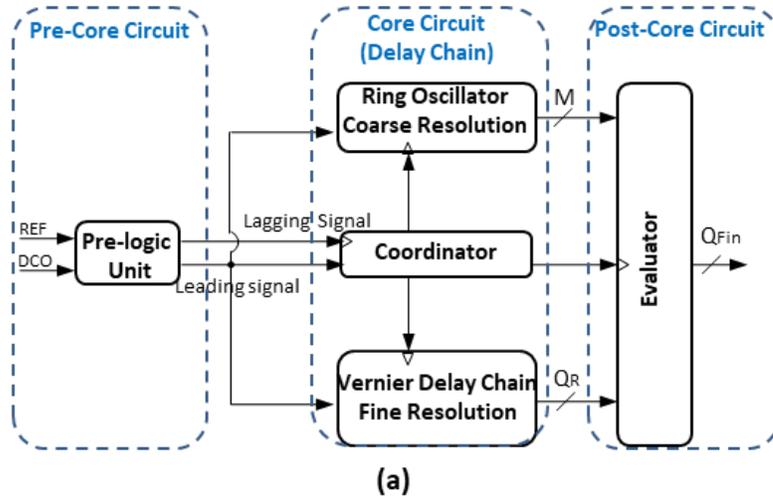


Fig. 38 The new TDC scheme diagram (a), with its timing function diagram (b)

The key points of the operation of the defined core circuit consists of the following aspects:

- a. To use the ring oscillator part to measure the time interval (ΔT_{Tot}) (again between the rising edge of the leading signal and the rising edge of the triggering signal) in a coarse granularity (as shown in **Fig. 38** (b)). The time resolution of the coarse measurement

corresponds to one or half period of the ring oscillator and is represented by T_{Nor} . General speaking for an arbitrary ΔT_{Tot} , all the time segments have an identical length, called the normal-length (T_{Nor}), except for the remaining time segment, which is symbolized as T_R . M stands for an output of a loop counter that counts how many cycles have been passed through the ring oscillator during the time interval. The amount of M that is output is m .

b. The residual segment, T_R which is certainly shorter than T_{Nor} , will be the one for a very fine time resolution measurement by the Vernier delay chains. And it will be quantized as Q_R by a N -stage fine resolution Vernier TDC core. The value of the Q_R output is f , a number between 0 and N (the stage number of the delay chain).

c. The main idea is to separate the whole time interval (ΔT_{Tot}) into 2 parts, the residual segment (T_R) and a integer number of time length ($\Delta T_{Tot} - T_R$) by a coordinator that ensures a seamless cooperation between the measurements of these two functions. Most importantly, it should be able to address the POM effect issue and eliminate the consequent noise injection.

Now let us see the mathematical relationship between the terms mentioned above. Note that the value of N should be chosen allowing the Vernier delay chain to just quantize one T_{Nor} length. However, considering PVT and volume variations, it is reasonable to leave some margin for the physical stage number that is guaranteed to be large enough for the coverage. Thus, an expected N at a certain determination cycle is defined as $\widetilde{N}(n)$ that is expected to show the exact number of the stages that can just cover the quantization of the length of the propagation delay along one rotation of the conjoined ring at the n th determination cycle. $\widetilde{N}(n)$ should be always a little bit less than N in value due to margin considerations. $\widetilde{N}(n)$ is determined by:

$$\widetilde{N}(n) = \frac{T_{Nor}}{T_{res}} = \frac{T_{Nor}}{\Delta\tau} \quad (13)$$

For instance, if T_{Nor} is set to be 100ps and the desired T_{res} is 5ps, $\widetilde{N}(n)$ should be 20. And the physical designated stage number of the delay chain, N can be chosen from 22 to 24.

And Q_R output is determined by:

$$f = \frac{T_R}{\Delta\tau} \quad 0 < f < \widetilde{N} \quad (14)$$

where \widetilde{N} is an average value of $\widetilde{N}(n)$ during a short time period during which the PVT variation is very small so that it can be ignored. Thus, the time interval is determined by:

$$\Delta T_{Tot} = m \cdot T_{Nor} + T_R \quad (15)$$

Where, m is the decimal value of M output. Substituting equation (13) and (14) into (15), it gives:

$$\begin{aligned} \Delta T_{Tot} &= m \cdot \widetilde{N} \cdot \Delta\tau + f \cdot \Delta\tau \\ &= (m \cdot \widetilde{N} + f) \cdot \Delta\tau \end{aligned} \quad (16)$$

Therefore, the final output of the TDC (Q_{Fin}) can be expressed as:

$$Q_{Fin} = \frac{\Delta T_{Tot}}{\Delta\tau} = m \cdot \widetilde{N} + f \quad (17)$$

The result of Q_{Fin} is computed in the evaluator based on the inputs from M , \tilde{N} and Q_R .

Note that the detection range of the Vernier delay chain in the proposed TDC is shrunk to same as T_{Nor} , compared to the traditional (Vernier) TDC solutions, in which the number of stages of the delay chains is proportional to ΔT_{Tot_max} . The equation given below shows the merit ratio of the former solution to the latter one:

$$\begin{aligned}
 R_{merit} &= \frac{N_{common\ law}}{N_{this\ work}} \\
 &= \left(\frac{\Delta T_{Tot_max}}{T_{res}}\right) / \left(\frac{T_{Nor}}{T_{res}}\right) \\
 &= \frac{\Delta T_{Tot_max}}{T_{Nor}}
 \end{aligned} \tag{18}$$

where R_{merit} stands for the ratio of merit. For instance, in order to target a time resolution of 5ps and time interval of 2.5ns, a traditional Vernier TDC needs 500 stages while the scaled TDC only needs 20 stages (set T_{Nor} as 100ps). Actually, the TDC core in Fig. 38 can also be implemented in any other fine resolution style (such as a time-amplifier TDC) provided its time resolution performance is sufficiently good. Theoretically, the set of the normal-length phase of the ring can be set as short as desired, resulting in a shorter Vernier delay chain. However, making this length shorter than 60ps is not cost-efficient, because a shorter T_{Nor} means a larger value of m , and requires a scale-up of binary bits in the loop counter. In this thesis, choosing $T_{Nor}=80ps$ and m to be up to 256 (8 bits of M) enables a detection range of 20ns, which is sufficient for an ADPLL applied to a set of wireless requirements ranging from sub one hundred MHz to tens of GHz.

After the above analysis and considerations, the block diagram (Fig. 38) can be refined as shown in Fig. 39 in which the post core evaluation has been refined and subdivided into several functional blocks. The function of the evaluation unit can be classified into a normal-phase loop counter, a Vernier core output post-operator, a computing-error correction part and a final TDC output calculator. The normal-phase counter is triggered by the rising edge of the loop signal to count out m which is represented by a T-bit binary number, $M<0:T-1>$. The Vernier core output post-operator is expected to locate the transition of Vernier core outputs ($Q<1:31>$) and convert them to a binary number ($QE<0:4>$), a binary expression of q_{core} . The computing-error correction part collects the clip signal (defined and detailed in next section) through the conjoined-ring output and the state of the signal $Q<1>$ and signal $Q<16>$ through the Vernier core output, then it determines a calibration result ($EC<0:2>$) to correct the computing-error problem. The details of the computing-error and the implementation of its correcting operation will be discussed later. The computation of final TDC output is performed using $M<0:T-1>$, $QE<0:4>$ and $EC<0:2>$.

More details of the design will be discussed in section 4.4.

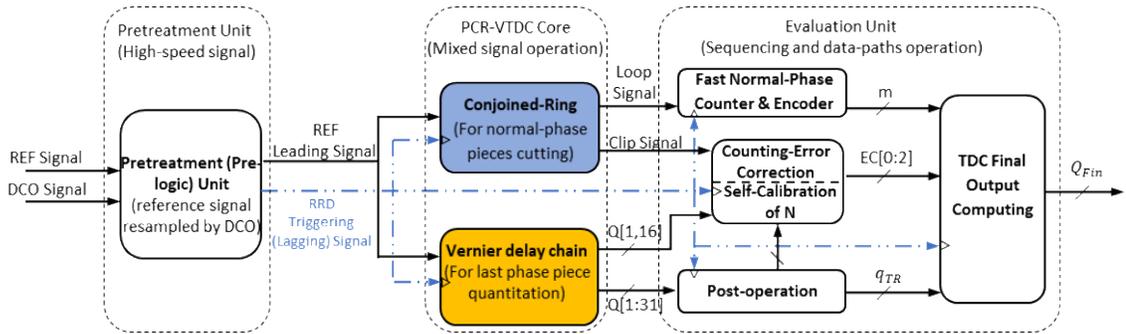


Fig. 39 Conjoined-ring Vernier TDC block diagram

4.3 Specifications for the TDC design in the ADPLL application

Considering the requirements of state-of-the-art ADPLL applications that could employ a competitive TDC, a set of specifications was chosen for the design of the TDC and is presented in Table2.

Table2: Specifications of the ADPLL and the TDC applied

Specification	Symbol	Value
TDC Time Resolution	$T_{res}(\Delta\tau)$	1~2ps
DCO Output Frequency	f_{DCO}	500MHz~10GHz
(Period)	(P_{DCO})	(100ps~2.5ns)
Detection Range	$\Delta T_{Tot,max}$	>12.5ns
Reference Frequency	f_{REF}	10~50MHz

4.4 Design of the Conjoined-Ring Vernier TDC

Now we continue the content discussed at the end of section 4.2. As shown in Fig. 39 the proposed TDC architecture consists of three parts: a partially-conjoined-ring Vernier core, a pre-treatment unit and a post-evaluation unit. The partially-conjoined-ring Vernier core is supposed to be a crucial mixed signal component in the TDC because its characteristics determine the time resolution performance, the phase detection range capability and the linearity performance of the quantization. The pre-treatment unit is used to generate the leading signal and the lagging signal in a manner that is acceptable by the

core inputs, and the post-evaluation unit counts the outputs of the core, and performs logical operations and calculations with POM error correction and so forth. The edge of the lagging signal (RRD) causes all TDC blocks to operate synchronously.

4.4.1 Pre-treatment Unit

As shown previously, a TDC is used to measure F_{Rn} or F_{Rn+1} , the time interval between the rising edge of the reference signal and either side of the adjacent DCO rising edges. Generally, the reference signal is used as the lagging signal of the arbiter-set. The reason why the DCO signal is rarely used as the lagging signal is because there would be multiple rising edges occurring in one TDC operation cycle, causing an undesirable multi-trigger issue and a failure of transition determination. However, if we apply the DCO signal directly as the leading signal, its multiple rising edges will also lead to issues like multiple transitions, which will cause problems during encoding unless a priority encoder is employed. A priority encoder could pick up the true transition from the fake ones to avoid the bubble error, however, at expense of complexity that exponentially increases with the length of the delay chain.

Referring to [49], a reasonable and concise way to achieve the TDC core input request is to use the reference signal as the leading signal and meanwhile to create a lagging signal by using the DCO signal to resample the reference signal, obtaining the RRD signal (reference retimed by DCO) (Fig.40). In this case, RRD is also called a triggering signal to emphasize that it is used as a synchronous triggering signal for the system. Using this method, the average time length of the period of the RRD signal will be equal to the period of the REF signal. Comparing the reference signal and the RRD signal in a manner of accumulating n continuous time cycles, the phase error would correspond to F_{Rn}

(lowercase n corresponds to nth sampling activity). By doing this and replacing the DCO with the RRD signal as the lagging signal, the issues caused by directly using DCO signal as an input of the TDC core can be addressed. The outputs of the pre-treatment unit, the delayed REF signal and the RRD signal will be fed into the TDC core.

The details of the design of the RRD signal generation and the analysis and treatment of the potential metastability during the sampling will be introduced in next chapter.

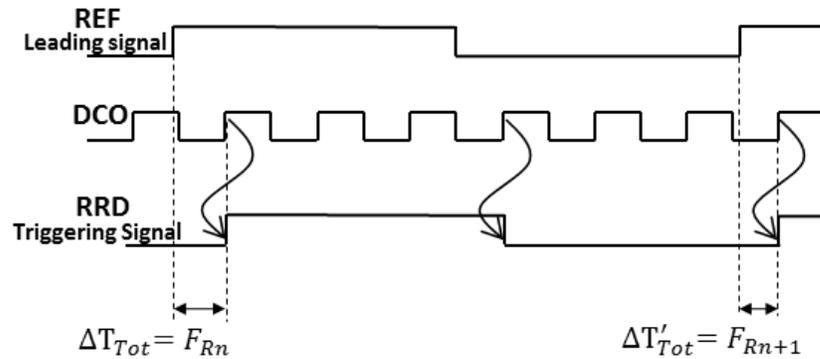


Fig.40 Timing diagram of the signals in pretreatment unit.

4.4.2 Partially-conjoined-ring VTDC Core

The conjoined-ring circuit is built up for the purpose of measuring the time interval (F_{Rn} or ΔT_{Tot}) between the rising edge of the leading signal and the rising edge of the triggering signal in a coarse time resolution (Fig.41 (a)). From the timing operation perspective (Fig.41 (b)), the conjoined-ring is likely to cut F_{Rn} into pieces. Those pieces often have an identical normal-length (T_{Nor}), except for the last piece (T_R). The normal-phase length corresponds to a cycle of the signal repeating along the conjoined-ring, aiming at a value of around 160ps in this work. Thus, the time interval can be represented by:

$$F_{Rn} = \Delta T_{Tot} = m \cdot T_{Nor} + T_R \quad (22)$$

where m is the number of the normal-phase pieces that are captured by the loop counter within one round of a measuring cycle. Thus, m is expected to be obtained by a loop counter which is supposed to be triggered for m times by the edge of the signal propagating along the conjoined ring.

Two switches (named the clipping switch-set) have been employed in the ring for the purpose of forming a time window to clip the overflow activity of q being used in the post evaluation unit to detect the occurrence of the POM error. AND1 gate should be off to deactivate the Vernier delay chain when the TDC is desired to work in the coarse resolution mode and needs to be on in the full functional mode. The leading signal and the lagging signal would be fed into the slow and the fast delay chains respectively and are set to the low level initially. The initial states of nodes A, B, C are all low and node D and D' are high initially (Fig.41 (c)). Note that the low state of the lagging signal enables the two clipping switches. The operation of the conjoined ring is launched by the presence of the rising edge of the leading signal, enabling the signal to propagate along the loop. The propagation of the signal along the Vernier delay chain stops at the 6th stage due to the AND3 gate being disabled by the low level of the lagging signal for the purpose of saving energy. Placing the AND3 gate on the sixth stage allows the first five stages to propagate more than 80ps, which corresponds to the signal's time propagation of one rotation along the loop, which also corresponds to a maximum time length of the signal edge on the slow chain being earlier than that on the fast chain. Once the rising edge of the leading signal enables the AND2 gate, the transition of the signal starts propagating along the A-B-C-D-

A loop. It completes one rotation when the falling edge of the signal arrives at node D, and later, the second rotation completes when the rising edge of the signal arrives at node D. This reappearance of the rising edge of the signal at node D indicates the completion of a cycle of the signal travelling along the conjoined-ring, which corresponds to a time length called normal length, T_{Nor} . The signal will not stop rotating along the ring until the lagging signal goes high. The rising edge of the lagging signal will:

- lock and disable the loop triggering activities.
- shuts off the propagation of the signal along the conjoined ring by turning off the switches.
- activates the operation of the Vernier delay chains for finest time resolution measurement by enabling AND1 and AND3.

The clipping switches and the embedded AND gates should cooperate properly to allow the delay chain and the conjoined ring to operate synergistically and focus on their own roles. Specifically, the conjoined-ring is likely to separate ΔT_{Tot} into segments and perform measurement in the coarse resolution of T_{Nor} , while the Vernier core is used for a fine resolution measurement of the residue segment in T_{res} . Note that the length of the delay chain depends on the request of just measuring the coverage of a half of T_{Nor} . The outputs of the clipping switches, Clip1 and Clip2 will be the triggering inputs of a fast loop counter and a D flip-flop respectively for the loop counting, the POM-error correction and the final evaluation.

Compared to a traditional Vernier TDC in which the quantitative measurement needs to cover the phase length F_{Rn} which corresponds to the period of the lowest applied DCO frequency, the proposed short Vernier delay chain is targeted to only cover the length corresponding to the measurement of the last phase piece T_R which is less than 160ps. Furthermore, any improvement of the time resolution of the T_R ($T_{res_{T_R}}$) performance would be leveraged to the entire TDC time resolution ($T_{res_{TDC}}$) performance, due to the fact that T_R is the only fractional phase piece not being quantized by the ring structure:

$$T_{res_{T_R}} = T_{res_{TDC}} \quad (23)$$

In fact, as mentioned, T_{Nor} corresponds to two rotations of the signal travelling along the ring. The signal propagation in the first rotation will be indicated by a high level of the loop signal and the second rotation of the loop signal is indicated by a low level of the loop signal. Therefore, the real phase length coverage for the short Vernier delay chain is only half of T_{Nor} , 80ps. The required number of the stages of the short Vernier delay chain should be determined by:

$$\tilde{N} = \frac{0.5 \cdot T_{Nor}}{T_{res}} = \frac{0.5 \cdot T_{Nor}}{\tau_2 - \tau_1} \quad (24)$$

$$\text{or } T_{Nor} = 2\tilde{N}\Delta\tau$$

where τ_2 and τ_1 stand for the propagation delay of the slow delay stage and the fast delay stage respectively. In the design, if the T_{res} is designated to be 3ps, \tilde{N} is required to be 27.

Consequently, the value of T_R can be determined by:

$$T_R = S_D \cdot 0.5 \cdot T_{Nor} + q_{core} \cdot \Delta\tau \quad (25)$$

where S_D equals zero when $Q\langle 1 \rangle$ is high corresponding to the first rotation of the loop signal and equals one when $Q\langle 1 \rangle$ is low corresponding to the second rotation of the loop signal. Note that two rotations of the signal travelling along the ring means a whole cycle of the signal repeats. The value of q_{core} indicates the series stage number where the arbiter-set outputs toggle. q_{core} is the numerical value between 0 and \tilde{N} and can be obtained by a priority-encoding operation on $Q\langle 1 : N \rangle$. Substituting (24) and (25) into (22) gives:

$$F_{Rn} = (m \cdot 2\tilde{N} + S_D \cdot \tilde{N} + q_{core}) \cdot \Delta\tau \quad (26)$$

Therefore, the numerical output of the TDC (q_{fin}) is represented by:

$$\begin{aligned} q_{fin} &= \frac{F_{Rn}}{\Delta\tau} = m \cdot 2\tilde{N} + S_D \cdot \tilde{N} + q_{core} \\ &= m \cdot 2\tilde{N} + q_{TR} \end{aligned} \quad (27)$$

q_{fin} is computed by the evaluation unit, and expressed in binary bits, $Q_{Fin} \cdot q_{TR}$ is the quantization output of T_R and has a maximum value of $2N - 1$. Fig. 42 represents the computation of the q_{fin} based on (27). Note that the horizontal axis is not the time domain but a sweep of various time interval cases (the range from 0ps to 340ps is illustrated in the figure). Using typical design parameters, \tilde{N} is set to be 27 and $\Delta\tau$ is 3ps. The grey solid

line represents q_{TR} , which ranges from 0 to 53 ($2\tilde{N} - 1$). The value (curve) of the grey solid line repeats periodically every $2\tilde{N}$. The yellow solid line indicates m , and the black solid line shows q_{fin} . q_{fin} is supposed to increase linearly with an increase of F_{Rn} according to (27) provided the values of the m , S_D and q_{core} are being collected correctly. The POM error correction scheme will be discussed later.

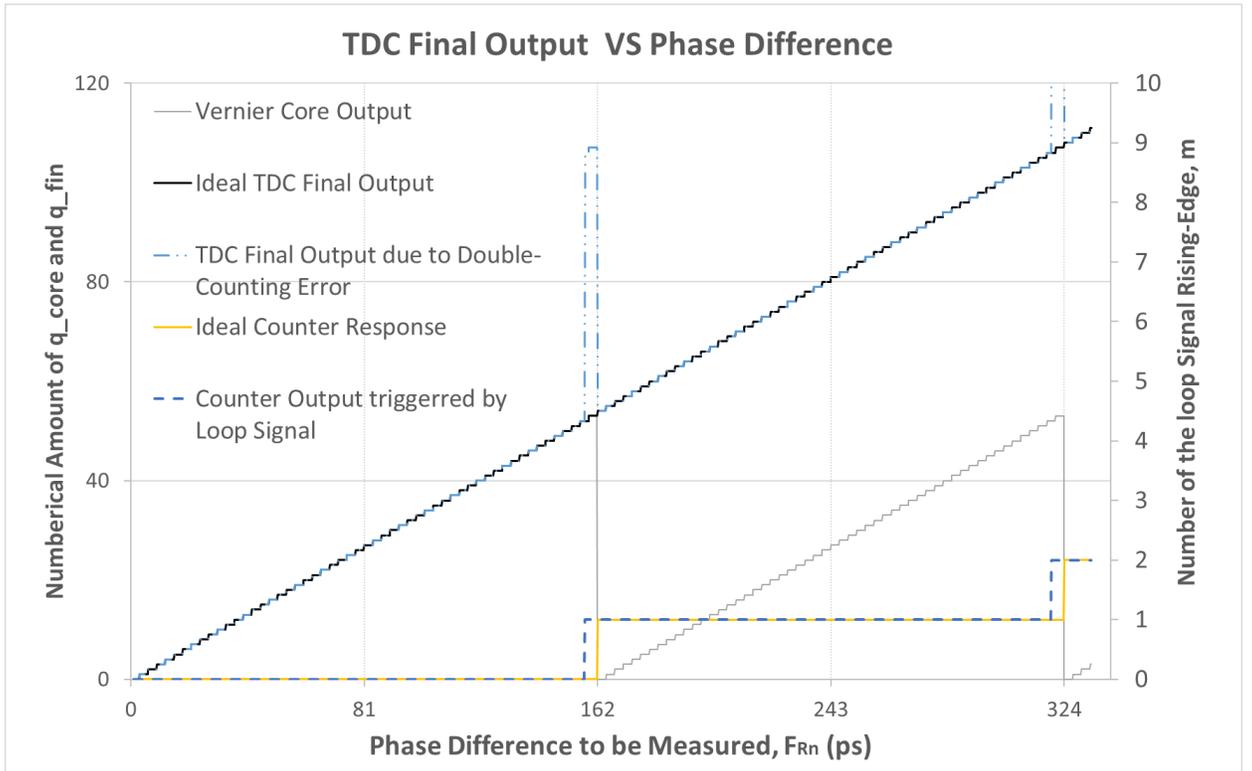


Fig. 42 TDC final output computing vs time interval input

4.5 Coarse & Fine Steps and Short Latency Design

The proposed partially conjoined ring Vernier TDC actually enables a switchable coarse & fine time resolution function. The refined phase regulator is also operating as a TDC with a coarse time resolution of 27ps (80ps/3). By replacing the 6th stage (in the slow path) and the first stage (in the fast path) with NAND gates (the other input terminal of the

NAND is triggered by the RRD signal), the time window of the activity of the fine resolution Vernier TDC core can be easily managed. The circuitry is supposed to be active only when the last fractional phase piece is coming through.

In practice, the fine resolution TDC core can be turned off in most less demanding scenarios. For a demanding requirement, the fine resolution TDC core can still be off during the acquisition & coarse-resolution tracking period until the ADPLL requests it to turn on.

Fig. 43 (a) illustrate a comparison among various Vernier TDCs in terms of the mandatory time length (normal phase length) needs a fine-resolution measurement. Different normal phase length characteristics cause proportional differences in the amount of transition activities of inverters. The power consumption due to transition activities of the Vernier delay chain in the proposed TDC solution could be less than that in a Vernier Ring solution by 10 times (assume a 15-stage delay chain as an example for comparison) or more.

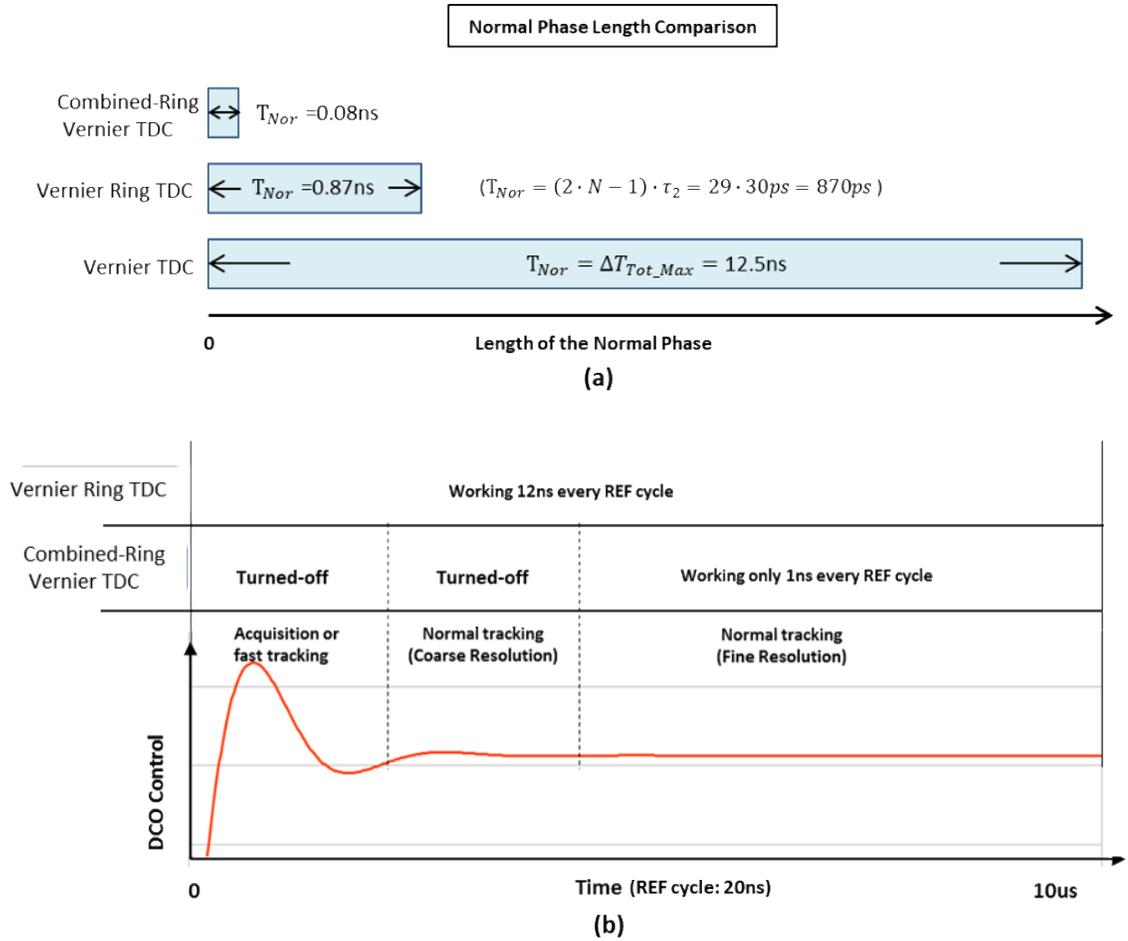


Fig. 43. Degree of activities of the VRTDC and Phase-scaled Vernier TDC.

Furthermore, the combination of the configurable coarse/fine modes function and scaled-down mandatory normal-phase asset enables an additional improvement in power consumption of the proposed TDC design. Fig. 43 (b) shows the preferred strategy of the proposed TDC operation in various PLL stages. Note that coarse mode might be used in the acquisition stage when less demanding time resolution is needed. The fine resolution mode needs to be active only during the normal locking stage. Due to short latency, it dissipates less power compared to the one with longer latency. Fig. 44 shows the timing diagram of various TDCs' operation, emphasizing the importance of the latency performance of a TDC for a competitive ADPLL that allows higher frequency of the

reference signal. Readers can find more details in Appendix 1.

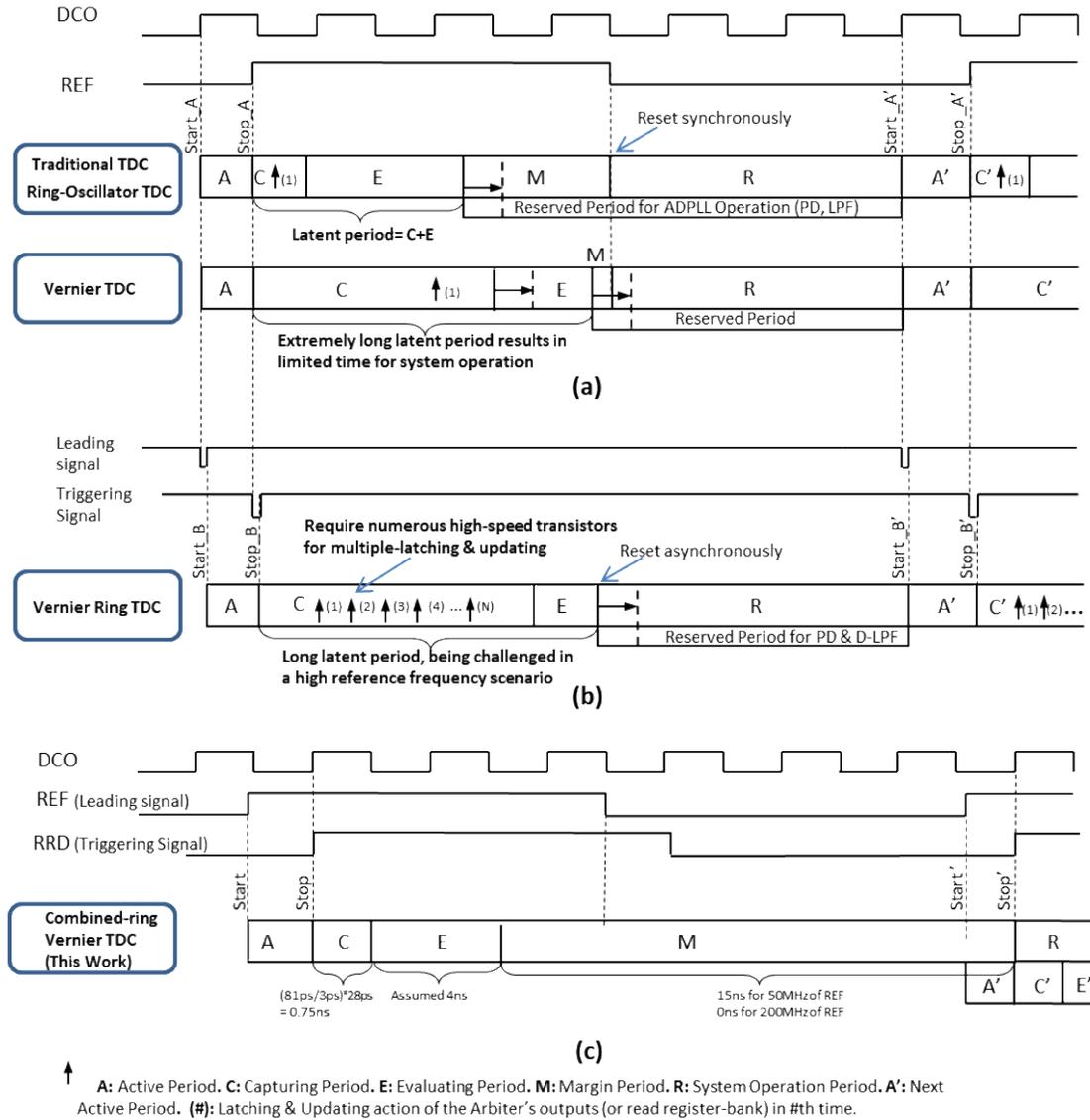


Fig. 44 Timing diagram of the operations and latency time of the various TDCs

Table 3: Performance Analysis at a Fixed 25MHz Reference Frequency (40ns period)

Specification	Symbol	Vernier	15-stage Vernier Ring	Conjoined-ring Vernier
TDC Time Resolution	$T_{res}(\Delta\tau)$	2ps	2ps	2ps

Phase-Detection Range	ΔT_{Tot_max}	12.5ns	12.5ns	12.5ns
Normal-Inverter Delay	$\tau_2 \& \tau_1$	30ps&28ps	30ps&28ps	30ps&28ps
Mandatory Fine Resolution				
Phase Length	T_{NOR}	12.5ns	$(2*N-1)*\tau_1=870ps$	80ps
Effective N stages	N_e	6250	30	40
Max Capture Period	P_{C_max}	$6250*28ps=$ 175ns	$(870ps/2ps)*28ps=1$ 2ns	$40*28ps=1ns$
Transition-activities in the core in one reference period	F_Power	$6250*2=12500$	$435*2=870$	$40*2=80$
Conclusion		Impractical	Medium level power consumption	Good

4.6 Pre-logic Circuit Design

The pre-logic unit is used to modify some manners of the reference signal and the DCO signal to avoid multi-transitions in each determination cycle in order to ensure the upcoming well treatment by TDC core circuit and the correct conversion of thermal to binary encoding. It could be a pulse generation circuit as in [34], in which, however, the width of the pulse needs a careful design to avoid the occurrence of the risk that the pulse signal may get faded while propagating along the delay chain.

Secondly, the pre-logic circuit is also used to identify and distribute the REF signal and the DCO signal into the slow path and the fast path respectively, so as to avoid the occurrence of the metastability by choosing the appropriate order of the two signals. However, the charge and discharge of the branches on both paths shake the designated signal propagation, and this mismatch could inject extra unpredictable phase error into time interval to be measured.

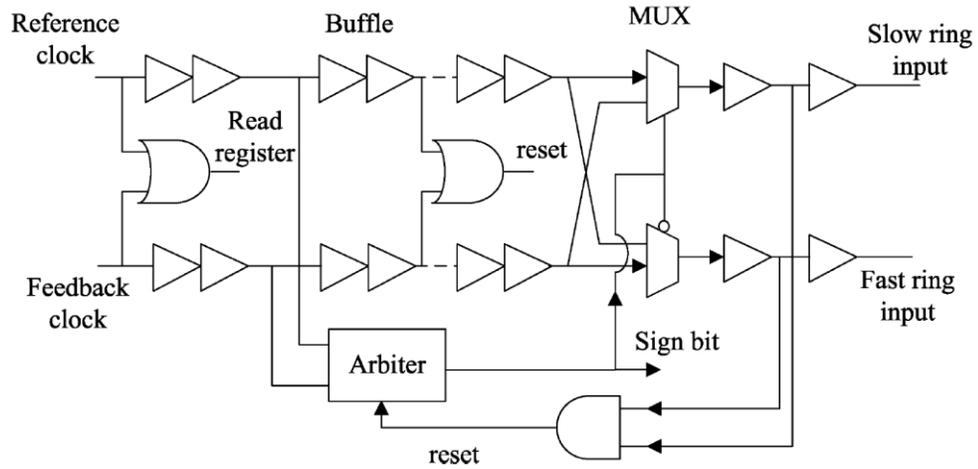


Fig. 45 Simplified circuits of the pre-logic unit in [34]

A concise style of the pre-logic circuit is expected in the proposed solution. In Fig. 46 (a), the reference signal can be sampled by the DCO signal which has a higher rate, yielding a “reference-retimed-by-DCO” signal (RRD). And RRD should have the same cycle period length as that of REF on average and each time difference between the edges of RRD and REF corresponds to the quantity ΔT_{Tot} , (Fig. 49) to be measured by the TDC core. However, in practice, the delay of data-to-clock and the delay of clock-to-output exist and that brings an extra unwanted delay and error into the time interval, ΔT_{Tot} . This error can be regarded as a constant value without considering the effect of metastability on the sampling and could be cancelled by introducing an additive parameter stored in the digital part of the circuit during the calibration phase.

4.6.1 Flip-Flops Considerations for RRD generation

Conceptually, a typical D flip-flop as shown in Fig. 46 (a) is sufficient to generate the RRD signal. Flip-flops are basic elements that are used in designing synchronous circuit and memory elements, like in counters, digital PLLs and shift register banks applications.

The demands for a short clock cycle, less delay, less power dissipation and more efficiency in area occupation are of primary importance to be considered during a flip-flop design. Depending on the various requirements, a diverse set of options may be chosen to make a balanced optimal fit.

A traditional master-slave flip-flop usually includes two identical latches that stage up together (Fig. 46(b)). PowerPC and C²MOS flip-flops are well known especially for their power efficiency. However, the delay of the first latch leads to an appreciable amount of input-to-clock delay (T_{DC}), resulting in a positive setup time. Fig. 46(c) uses a basic dynamic style C²MOS flip-flop because the outputs of the latches could be in a high impedance state. The counterpart of dynamic flip-flops would be static ones, which can be built up by embedding a bistable element to each output node of the dynamic latches. The dynamic flip-flop has the advantage of shorter delay and setup time as well as small clock load, while the static one provides better noise immunity and rail-to-rail outputs remaining constant with the time.

Several other flip-flops like semi-dynamic flip-flop (SDFF), sense-amplifier flip-flop (SAFF) and hybrid-latch flip-flop (HLFF) have become primary options in a high-performance flip-flop design that differ from traditional master-slave latches. They could be grouped as half dynamic flip-flops and be considered as an option when the value of the setup time (T_{setup}) is desired to be as low as zero. The key point of the design of SDFF, SAFF, HLFF to realize zero (negative) setup time is replacing the master latch with a pre-charged but short transparent latch as shown in Fig. 46(d).

Specifically, in this RRD generation unit design, a static flip-flop is overall superior to

a dynamic one because a low value of T_{setup} is not needed in this case, and most important a static flip-flop avoids a race-through issue that is a typical risk in a half dynamic flip-flop due to a potential positive hold time (T_{hold}). Finally, C²MOS flip-flops are employed owing to its less load request of the clock signal compared to that of a PowerPC type.

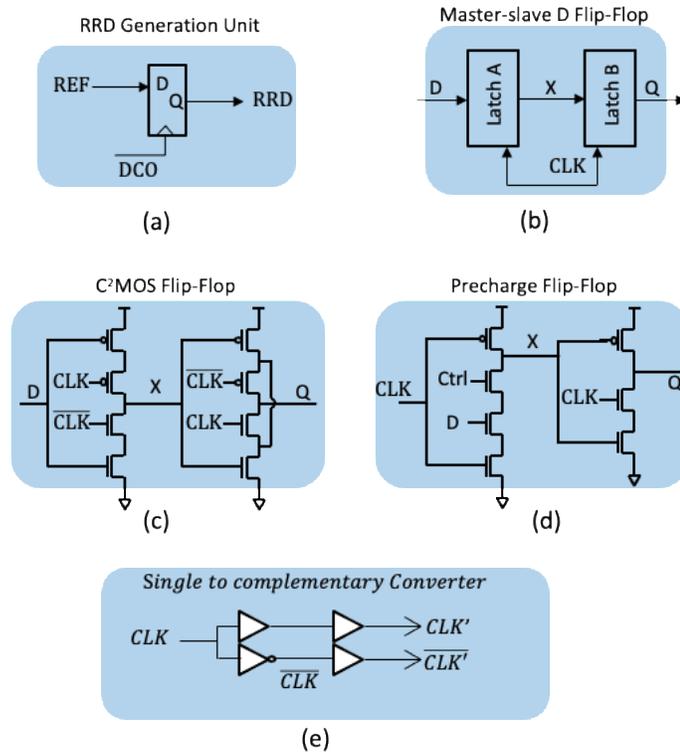


Fig. 46. Rough sketch of (a) a RRD generation unit, (b) a master-slave D flip-flop, (c) a basic C²MOS flip-flop, (d) a pre-charge flip-flop.

It is noticed that a single outer clock system that is to generate the complementary (differential) clock pair inside of a flip-flop might introduce mismatch between the response to the falling data input and that to the rising data input (Fig. 47), resulting in different data-to-output delays. The amount of the mismatch might be a few ps, which is acceptable for the RRD generation unit because only the rising edges are used for TDC measurement.

However, it is important to keep in mind that matched differential clock pairs are essential when they are used to trigger delay chain's flip-flop set. This is because the inverters that used in the delay chain toggle the level of the signals from one node to the next along with slow and fast delay chains. In this case, a single to complementary converter (Fig. 46(e)) may help. Fig. 48 shows a schematic design of a single to complementary converter with dummy loads.

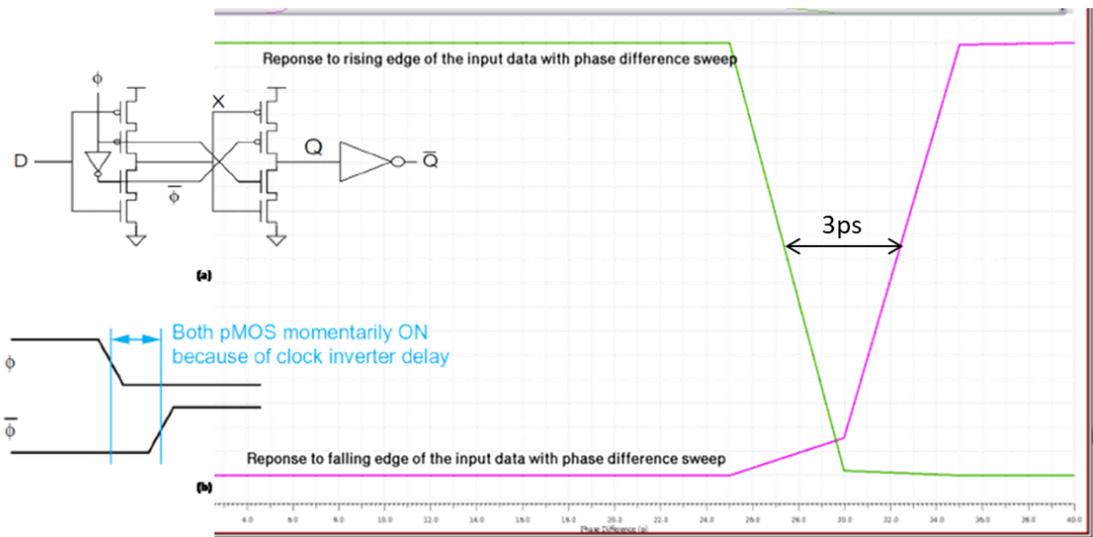


Fig. 47 the mismatch due to the single clock trigger in 45 nm process

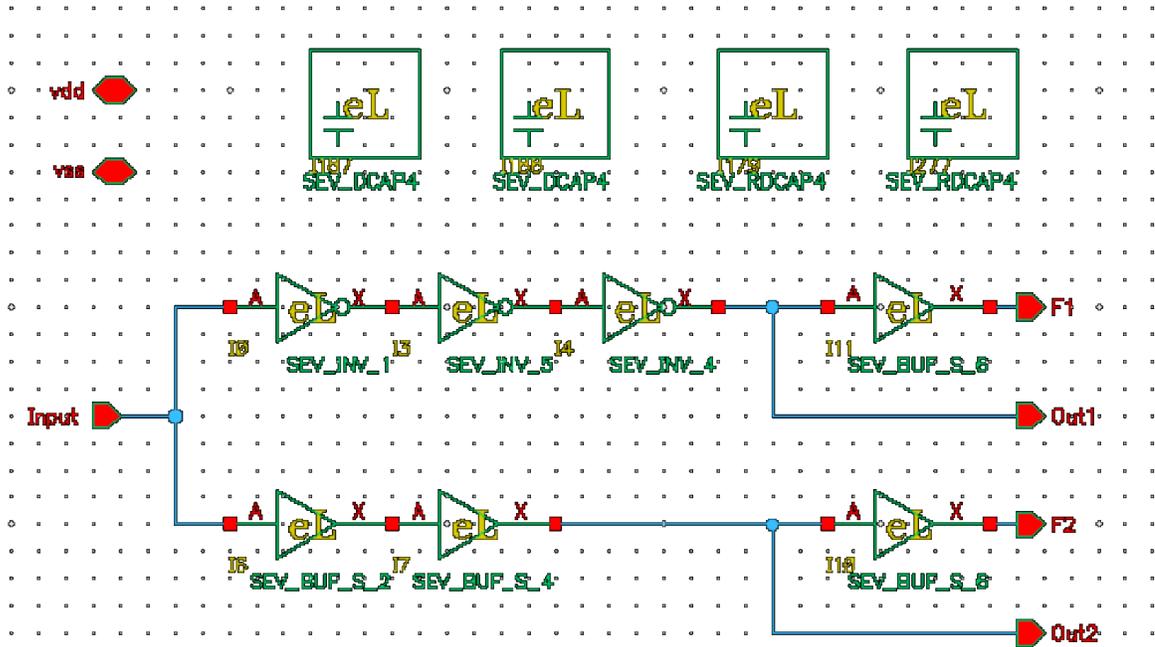


Fig. 48 Circuit of a single to complementary converter with dummy loads

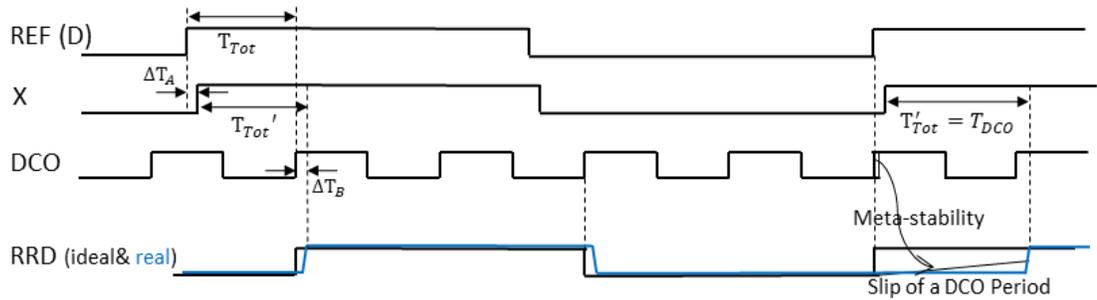


Fig. 49. Waveform illustration of the pre-logic unit.

4.6.2 Offset Compensation

As we mentioned at the beginning of this section,

As shown in Fig. 49 and Fig. 46 (c), when the clock triggers, the arbiter does not directly capture the signal state at D but rather that at node X. ΔT_A represents the

propagation delay due to master latch. ΔT_B in Fig. 49 stands for the clock-to-output delay.

Note that $\Delta T'_{Tot}$ labeled in Fig. 49 is determined by:

$$\Delta T'_{Tot} = \Delta T_{Tot} + \Delta T_B - \Delta T_A \quad (28)$$

If a proper circuit design can make ΔT_B equals to ΔT_A , the latter two items in (28) will be canceled out, making:

$$\Delta T'_{Tot} = \Delta T_{Tot} \quad (29)$$

Which means the REF signal at node X could be used as the leading signal pairs with the RRD signal, having the same time interval as that in the original pair (REF and DCO signals).

4.6.3 Metastability of RRU Generation Unit

Now let us investigate the metastability issue in the RRD generation circuit (pre-logic) design. As we discussed, the metastability issue might take place during the sampling activity of a flip-flop when the clock signal edge gets closer to the edge of the input signal, implying a various clock-to-output delay.

Fig. 50 plots curves of clock-to-output delay (T_{CQ}) and data-to-output delay (T_{DQ}) as data-to-clock delay (T_{DC}) changes of a general master-slave flip-flop. Note that T_{DC} is the time interval to be measured and can also be represented as ΔT_{Tot} . After the RRD generating operation, the practical time interval, ΔT_{Tot} will corresponds to T_{DQ} , which is the sum of T_{DC} and T_{CQ} as referred below:

$$T_{DC} = \Delta T_{Tot} \quad (30)$$

$$T_{DQ} = T_{DC} + T_{CQ} = \Delta T_{Tot} + T_{CQ} = \Delta T_{Tot}''$$

If T_{CQ} is constant, T_{DQ} or $\Delta T_{Tot}''$ should increase linearly with T_{DC} so as to represent the time interval ΔT_{Tot} with a timeless offset. As mentioned in the previous section a constant offset can be feasibly and efficiently cancelled or compensated.

Along with the x-axis of Fig. 50, it has been separated into three regions: stable zone, metastable zone and slip zone. The stable zone is defined as when T_{DC} is large enough and T_{CQ} (offset) is constant at t_{ccq} (contamination clock-to-output delay). The stable zone implies a desirable region due to zero nonlinearity injected. Moving away from the stable zone, T_{CQ} increases as T_{DC} decreases, corresponding to the metastable zone. T_{DQ} changes by both T_{DC} and T_{CQ} but in opposite direction. The minimum value of T_{DQ} is located at middle stream of the metastable zone and the corresponding T_{DC} value is referred to T_{setup} to be generally used as a metric to evaluate the response speed capability of a flip-flop. The below equation can be set up then:

$$T_{DQmin} = T_{setup} + T_{pcq} \quad (31)$$

where T_{pcq} is the propagation clock-to-output delay. When T_{DC} is getting further smaller away from the point of T_{setup} , T_{CQ} will increase exponentially from the value of T_{pcq} , so does the T_{DQ} . Overall, in the metastable zone, T_{CQ} that exponentially increases with the decrease of T_{DC} makes T_{DQ} a parabolic function, introducing unwanted various phase error into ΔT_{Tot} (form $\Delta T_{Tot}''$). The phase error would range from 0 to a time length of one clock period, not monotonically but parabolically in the metastable zone.

As a further decrease of T_{DC} when T_{DQ} exceeds the value of the length of the clock period (DCO signal period), the output of the flip-flop at this determination cycle will not reflect the data transition at the input. It will do so until next clock edge. Because of this one clock period delay of the determination, we group and define this situation and occurrence as taking place in the slip zone. The slip region implies the occurrence of a one clock cycle delayed data transfer of a flip-flop which is called a slip of a DCO cycle period.

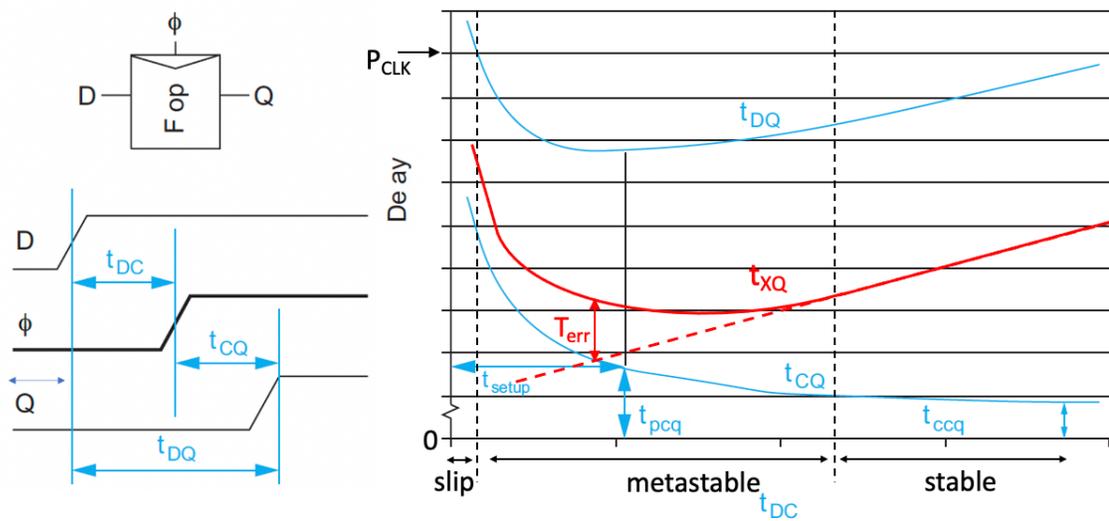


Fig. 50 the delays in the D flip-flop being associated with metastability

It can be seen in Fig. 50 that if we use the signal at node X as the leading signal, T_{XQ} (node X-to-output delay) will be used to represent ΔT_{Tot} , the overall data-to-output delay will be dropped and the slip zone could be shrunk to an even smaller range.

4.6.4 Compensation Design at the Clock cycle Slip Zone

The occurrence of the clock cycle slip leads to a phase error with amount of one period of the clock signal. Fortunately, there is no need to be concerned, because this slip can be

compensated in the operation of the ADPLL system solution in Fig. 51. Fig. 52 shows an example of the ADPLL system-level operation in the time domain based on the principle shown in Fig. 51. Assuming a DCO output signal running at the frequency that is 3.25 times that of the reference signal, and with zero phase difference at the beginning, the REF edge coincides with the DCO edge every thirteen DCO period, triggering slip activity. If the RRD signal is used as the synchronous trigger clock for the whole ADPLL system, the occurrence of a clock slip would cause:

- The DCO period counting (i) would accumulate one more in value.
- The error in TDC output would correspond to one DCO period as well.

Note that above two impacts due to clock slip would be cancelled out in the calculation phase. In other words, the proposed pre-logic (RRD generation) unit can be perfectly matched with the ADPLL system oversampling-time strategy, compensating the TDC error due to clock slip in the system level operation.

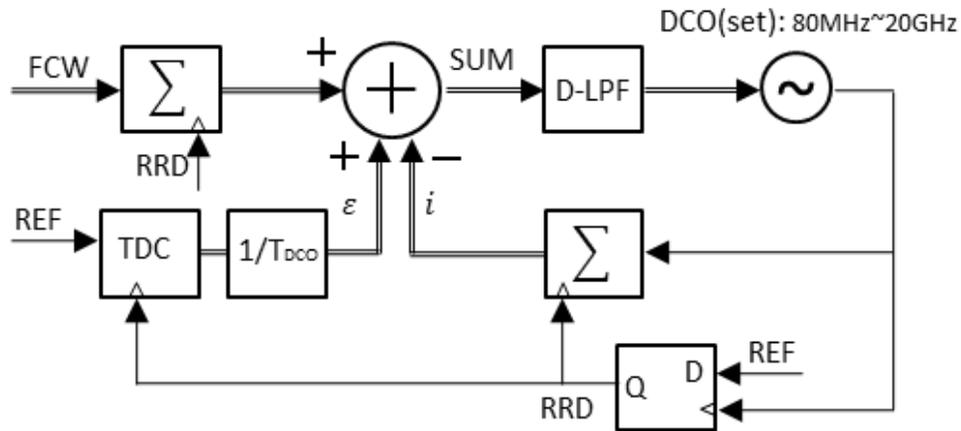


Fig. 51 The Proposed ADPLL system operation diagram

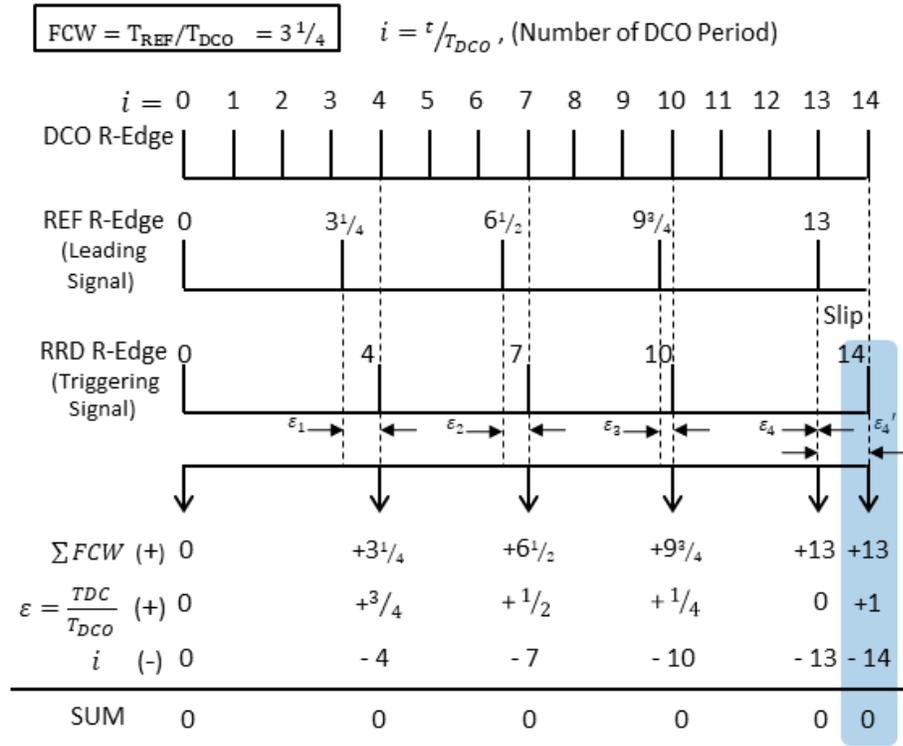


Fig. 52 ADPLL timing and computation example (FCW=3.25)

4.6.5 Double-Sampling RRD Generation

Now, let's investigate the phase error injection when T_{DC} falls into the metastable zone. The expected time interval to be measured is determined by:

$$\Delta T_{Tot} = T_{DQ} = T_{DC} + T_{CQ} \quad (32)$$

In which a constant offset, T_{offset} , that can be calibrated out is determined by:

$$T_{offset} = t_{ccq} \quad \text{if node X as the leading signal} \quad (33)$$

and the various errors injected in metastable region (Fig. 50) are determined by:

$$T_{err} = T_{CQ} - t_{ccq} \quad (34)$$

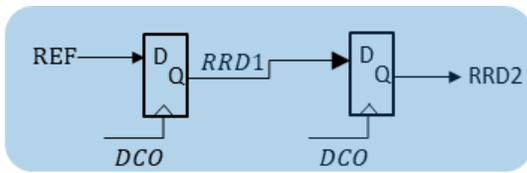
If T_{err} , ranges from 0 to almost one DCO period long, it would lead an appreciable degradation of the TDC quantization precision. To address this issue, a double-sampling design circuit has been introduced as shown in Fig. 53 (a) to convert the various delay offset (error) to a constant time length of one DCO period. RRD2 would have one more DCO period length leading to the following relationship:

$$\begin{aligned} \Delta T_{Tot} &= RRD2_{rise} - REF_{rise} \\ &= T_{DC} + P_{DCO} + t_{ccq} \end{aligned} \quad (35)$$

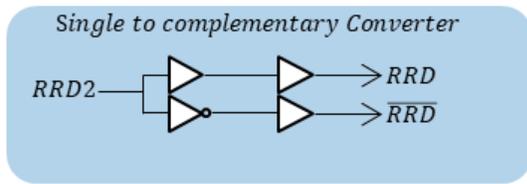
In which the constant offset, T_{offset} , would be:

$$T_{offset} = P_{DCO} + t_{ccq} \quad (36)$$

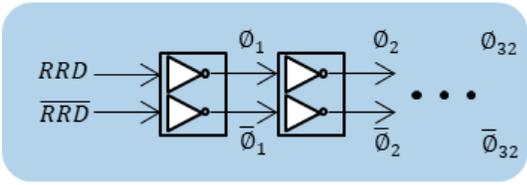
Thus, the various errors injected would be zero. The schematic connection and the simulation result are shown in Fig. 54 and Fig. 55.



(a)



(b)



(c)

Fig. 53 (a) Double sampling block diagram, (b) (c) complementary pair of RRD signals generations in case of C²MOS flip-flops for arbiter set.

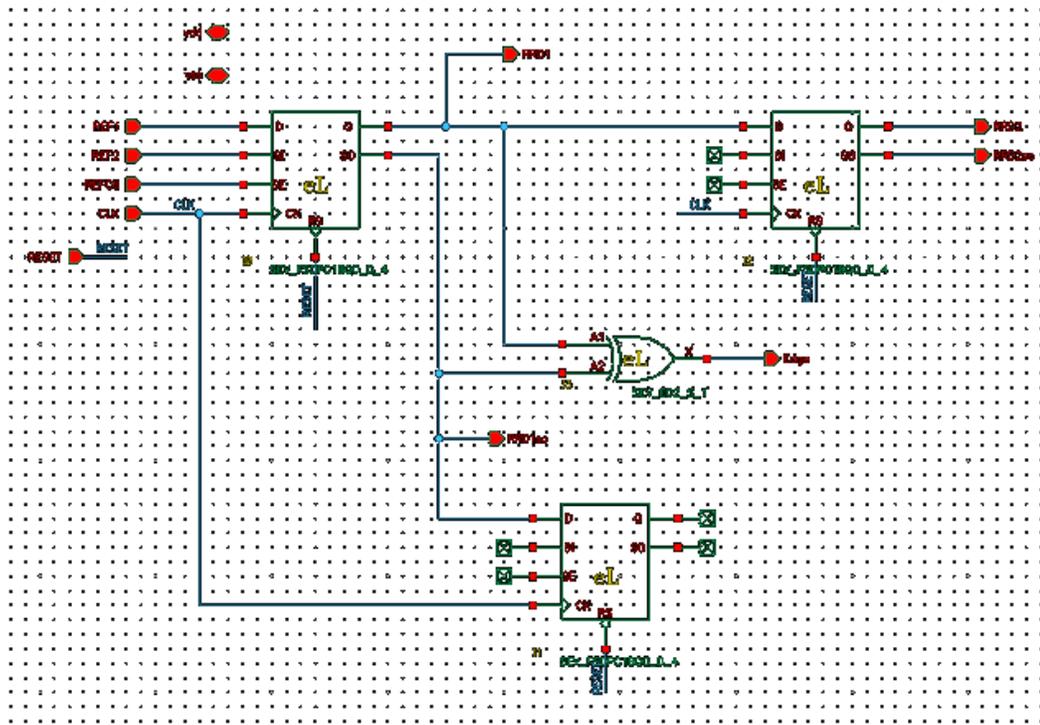


Fig. 54 Schematic of the double sampling circuit.

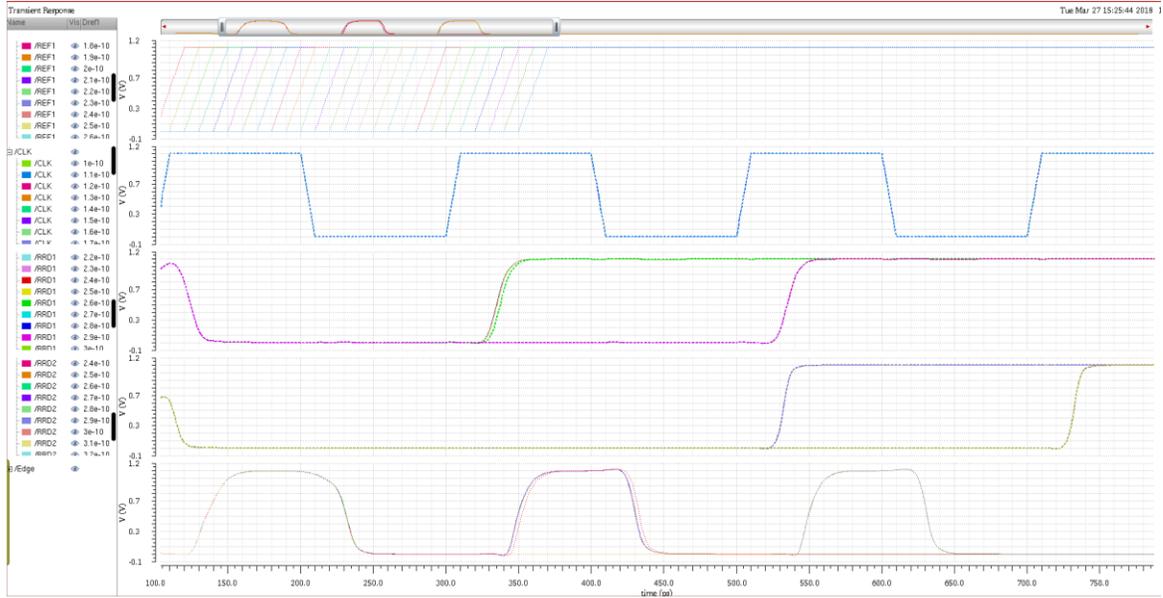


Fig. 55 Simulation of the double sampling circuit.

Complementary pairs of the lagging signals and their delayed versions along the fast delay chain have also been employed to eliminate the mismatch caused by the outer single clock (Fig. 53 (b) (c)).

In conclusion of this section, the proposed RRD generation unit can generate the leading and lagging signals without introducing extra phase error by considering and treating the clock slip problem at the system level of the ADPLL and by eliminating the metastable phase error in a double-sampling circuit.

4.7 Selections of \tilde{N} and N , B_m and T_{Nor}

As discussed in section 4.4, a short Vernier delay chain (small N) that could save both power consumption and chip area is achievable owing to only a relatively short normal-phase length, T_{Nor} , that needs to be measured. Note that the minimum T_{Nor} value is constrained by the limitation of the operating speed of the loop counter. The present loop counter operation must complete before the arrival of the next clock trigger to ensure

correct capture of outputs by the following register bank. The constraint of normal-phase length is shown below:

$$0.5 * T_{Nor} > T_{LoopCounter} \quad (37)$$

Thus, to obtain a short normal phase property, a high-speed loop counter is desirable. In Table 4, different design options are listed changing among \tilde{N} and B_m , where \tilde{N} stands for Vernier core stage number, B_m represents the bit widths of the loop counter output and B_{QE} is the bit widths of the Vernier core output, m_{max} represents the maximum decimal value of the loop counter output, and $f_{DCO_{min}}$ indicates the minimum available DCO frequency according to the parameters chosen.

The relationship among above variables are determined in the equations below:

$$m_{max} = 2^{B_m} \quad (38)$$

$$N = 2^{B_{QE}} \quad (39)$$

$$0.5 * T_{Nor} = N * T_{res} \quad (40)$$

$$f_{DCO_{min}} = 1 / (T_{Nor} * m_{max}) \quad (41)$$

The constrains and boundary for T_{Nor} is listed as the priorities of design:

- (a) A low value of T_{Nor} is expected to ensure a short N-stage Vernier core.

(b) T_{Nor} equals two times propagation delay of the signal travelling along the conjoined-ring loop.

(c) T_{Nor} must be larger than the minimum operating cycle capability of the loop.

TABLE 4 TDC STAGES AND COUNTER BIT CONSIDERATION

T_{res}	N	B_{QE}	$B_m, (m_{max})$	$0.5 * T_{Nor}$	f_{DCOmin}
3ps	7	3-bit	5-bit (31)	21ps	1.5GHz
	15	4-bit	4-bit (15)	45ps	
3ps	15	4-bit	5-bit (31)	45ps	720MHz
	31	5-bit	4-bit (15)	93ps	
3ps	31	5-bit	5-bit (31)	81ps	400MHz

A reasonable value of T_{Nor} is in the range between 140ps and 170ps. Assuming a balanced 5-bit widths for B_{QE} and B_m , a 31-stage Vernier core may have a maximum value of $T_{Nor} = 186ps$ at 3ps of T_{res} . Considering T_{Nor} changes with process, voltage and temperature variations (PVT), 162ps is chosen for T_{Nor} which theoretically could be covered by 27 stages in typical situation.

4.8 High-Speed Loop Counter Design

In the previous section, it was mentioned that a loop counter with high operating speed is crucial. The operating cycle time of a regular binary counter is determined by:

$$T_{Counter_{min}} = Md_{adder} + d_{FF} \quad (42)$$

where d_{adder} stands for the propagation delay of an adder, M is the number of bits of the counter, and d_{FF} is the propagation delay of a flip-flop which is used in the counter. The operating cycle time of the binary counter increases with the bit number (M) due to the ripple-carry characteristic of the adder. Thus, a traditional binary counter is inferior choice to be used in a high-speed requirement.

If the whole binary counter can be separated into two stage-up counters and the first stage of the counter has small bit widths (typically 3) and the second stage counter is then implemented with $M-3$ bits, the operating cycle time of this two-stage fast-binary counter might be shrunk. The limit of the operating cycle time of the first stage would be determined by:

$$T_{Counter_{min}} = 3d_{adder} + d_{FF} \quad (43)$$

The operating cycle time of the two-stage binary counter can be improved to a few hundred pico-seconds, compared to a nano-second level in a traditional counterpart. However, in this work, an even higher-speed counter should be required and the operating cycle of it should meet (37).

A modified Johnson (ring) counter (Fig. 56) consisting of 4-bit shift register is employed as the first stage counter. It can be extremely fast due to each counter outputs ($CQ<1:4>$) calculated independently (no carry-in or carry-out) and the operating cycle can be as low as one flip-flop clock-to-output delay plus one inverter propagation delay (roughly equals to data-to-output delay of the flip-flop). The $T_{Counter_{min}}$ of the modified

Johnson counter is not hard to achieve one hundred pico-seconds at a 40 nm node of the CMOS process. CQ_{ov} is used to indicate the overflow of the counting.

The pattern of the outputs of the 4-bit Johnson Counter is shown in Table 5. The initial state of flip-flops is supposed to be zero except $CQ_{<4>}$ which is high (one). CQ_{ov} is high according to the logic operation illustrated in Fig. 56. $CQ_{<1:4>}$ is triggered by the rising edge of the loop signal, and the counter cycles through eight unique states before it repeats every $2M$. Thus, the 4-bit modified Johnson counter (repeating in every 8 clock cycles) is equivalent to a regular 3-bit binary counter. The rising edge of CQ_{ov} implies the overflow of counting and triggers the second-stage binary counter ($M_{<3:4>}$). Note that the outputs of the Johnson counter $CQ_{<1:4>}$ need to be encoded into a binary number $M_{<0:2>}$ eventually.

As for the design of the flip-flops employed in the modified Johnson ring counter, static flip-flops have been chosen instead of pre-charged (half dynamic) flip-flops. The reason for this is to avoid occurrence of the risk of the race-through issue caused by positive hold time (T_{Hold}). Positive hold time can only take place in half dynamic flip-flops due to the fact of its unequal pulse-width scheme shifting the real trigger time from the front edge of the pulse to its ending edge. The schematic of the 4-bit modified Johnson ring counter is illustrated in Fig. 57

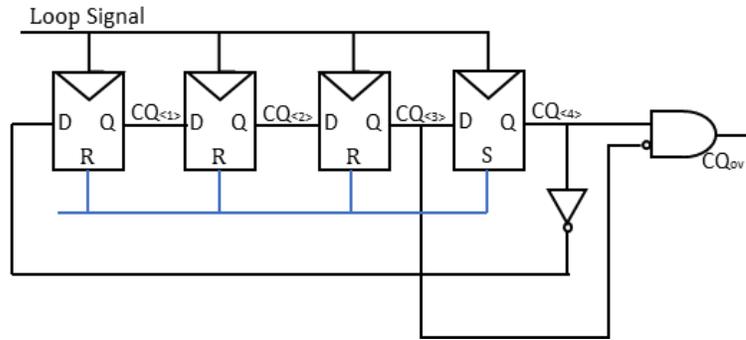


Fig. 56 4-Bit modified Johnson ring counter

TABLE5 4-BIT JOHNSON COUNTER SEQUENCE

Loop Signal Rising Edge #	$CQ<1>$	$CQ<2>$	$CQ<3>$	$CQ<4>$	Encoding $CQ<1:4>$, $M<0:2>$	CQ_{ov} , trigger to $M<3:4>$
0	0	0	0	1	000	1
1	0	0	0	0	001	0
2	1	0	0	0	010	0
3	1	1	0	0	011	0
4	1	1	1	0	100	0
5	1	1	1	1	101	0
6	0	1	1	1	110	0
7	0	0	1	1	111	0
8	0	0	0	1	000	1 (rising)

Keep Repeating from 0 to 7

In this case, the phenomenon called prior-POM error zone is expected to be identified by the concurrence of the debatable zone and the fourth quarter zone. Applying two flip-flops triggered by clipping signals are used to form the indication of the debatable zone, which is the key point to find the POM error zone. The prior-POM zone is covered inside the debatable zone and they share the same starting point. Also, the prior-POM zone is covered inside the 4th quarter zone but with the same ending point. Thus, the concurrence of the debatable zone and 4th quarter zone indicates the prior-POM error. Once this concurrence is detected, the POM correction process is supposed to be activated and the final TDC formula, (27) will be updated to:

$$q_{fin} = (m - 1) \cdot 2\tilde{N} + \tilde{N} + q \quad (44)$$

As shown in the determination process illustration (Fig. 59), the debatable zone can be identified by reading of the states of the LSB output of the loop counter ($m_{<0>}$) and the output of the Clip2 flip-flop ($Clip2_{<0>}$). If both 4th quarter and the debatable zone are detected it implies that a POM error has occurred. Then, the correction process will be activated to eliminate the error. The fourth quarter zone indicator is employed to cover a range from $(\frac{3}{4} \cdot 2\tilde{N})$ to the even overflow of q_{TR} , $2\tilde{N}$. The implementation of fourth quarter zone identification will be discussed in detail in next section.

In summary, the concurrence of the debatable zone and the fourth quarter zone implies the occurrence of the miss-alignment zone (the double-computing error in this work). In this case the POM-error correction will be activated and the computation of the final TDC output follows,(44) otherwise the final TDC output is still computed by (27).

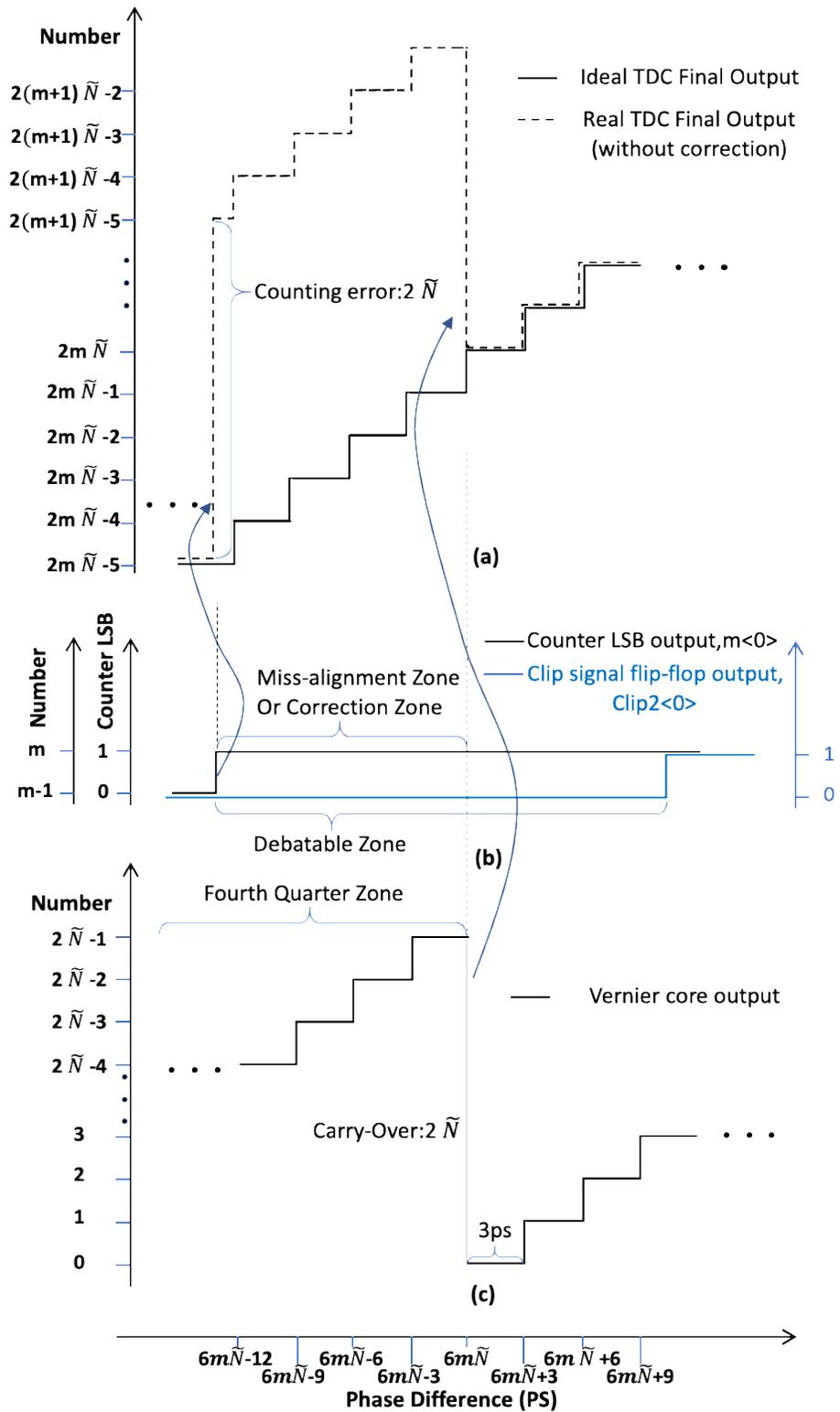


Fig. 58 TDC computation and POM-error vs. time interval: (a) TDC final output, (b) counter output and clip signal flip-flop output, (c) Vernier core output.

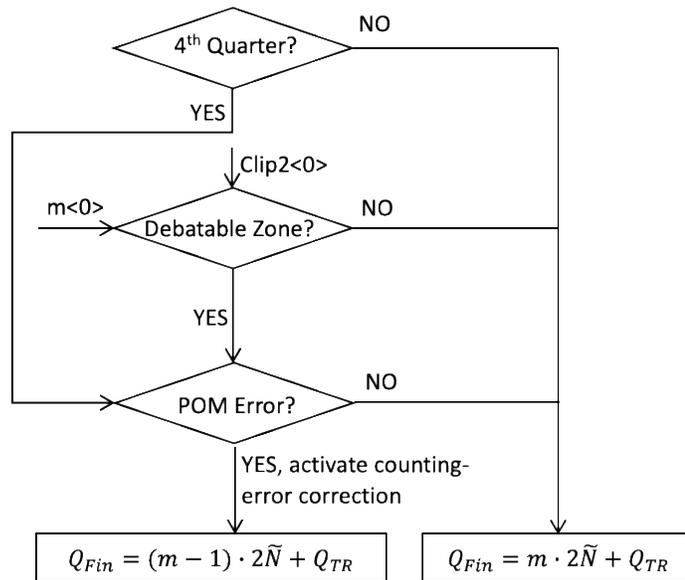


Fig. 59 POM-error recognition and correction determination process.

4.10 Implementation of the Evaluation Unit and Non-Interrupted N-Calibration

The partially-conjoined-ring Vernier TDC evaluation unit is implemented as illustrated in the black dashed box in Fig. 60 (a). Its inputs from the TDC delay chain core include the Vernier core arbiter set output ($Q_{<1:31>}$), one loop trigger ($clip1$) and one clipping trigger ($clip2$).

Inside of the evaluation unit, the design of the first stage loop counter (modified Johnson ring counter) have been discussed in section 4.8. The 3-bit output of the first stage counter ($m < 0:2 >$) can basically cover the time-length detection range up to 1.2ns. The second stage counter is made by a regular fast binary counter, which is triggered by CQ_T . A 3-bit second stage binary counter can cover the time-length detection range up to 10ns. For an application with the DCO frequency higher than 0.83GHz (1.6 GHz for a double-

sampling design), the second stage binary counter can be in an idle state to save more power.

The POM-error correction circuit is used to modify $m < 0:2 >$ to $m' < 0:2 >$. The implementation of the POM-error correction circuit is shown in Fig. 60 (b). When experiencing the potential POM-error situation, the different status between $m < 0 >$ and $Clip < 0 >$ causes the output of the XOR gate to become high (indicating the debatable zone). Meanwhile, the low status of both $Q < 1 >$ and $Q < 16 >$ leads to a true value of the output of the NOR gate (indicating 4th quarter zone), referring to Fig. 59. The XOR gate output and the NOR gate output are fed into an AND gate. If both XOR output and NOR output are true (high), the AND gate outputs high or 1, otherwise the output of the AND gate equals 0. Then, the output of the AND gate is used as the correction parameter (Δ) that will be subtracted from m to achieve m' . Finally, we have:

$$m' = m - \Delta \quad (45)$$

The value of m' is updated and stored into the register by the trigger of the falling edge of the RRD signal.

The Vernier core outputs ($Q < 1:31 >$) are imposed into two 16-bit wide parallel data streams ($Q < 1:16 >$ and $Q < 16:31 >$). Then in each one of $Q < 1:16 >$ and $Q < 16:31 >$, exclusive-or (XOR) operation was conducted for each pair of two adjacent bits, producing $X < 1:15 >$ and $X < 16:30 >$ respectively. Presumably, in $X < 1:15 >$ and/or $X < 16:30 >$ one or two bits can be found with a high value and the rest at low level. The location of the high-level bits indicates where the transition occurs. By using a simple 16-to-4 bit encoder for

$X\langle 1:15 \rangle$ and $X\langle 16:30 \rangle$, the transition location can be expressed as a binary number ($Z\langle 0:3 \rangle$ or $K\langle 0:3 \rangle$).

Introducing the above operation of $Q\langle 1:31 \rangle$ facilitates the simplification of implementation of the q_{TR} computation and allows a function called On-going \tilde{N} - calibration to calibrate out PVT variations.

The last remaining phase piece T_R is quantized with the finest time resolution and can be expressed by $Q\langle 1:31 \rangle$. The result of the quantization is classified into four-quarter ranges as shown in Fig. 61, those are defined by the values of $Q\langle 1 \rangle$ and $Q\langle 16 \rangle$. $Q\langle 1 \rangle$ toggling to 1 while $Q\langle 16 \rangle$ remaining 0 indicates the transition location is between $Q\langle 1 \rangle$ and $Q\langle 16 \rangle$ of the first rotation, which is defined as the first quarter. If both result in 1, the transition is located between $Q\langle 16 \rangle$ and $Q\langle 31 \rangle$ of the first half rotation, which is defined as the second quarter. If $Q\langle 1 \rangle$ outputs 0 while $Q\langle 16 \rangle$ outputs 1, it indicates the transition location is between $Q\langle 1 \rangle$ and $Q\langle 16 \rangle$ of the second rotation, which is defined as the third quarter. And both $Q\langle 1 \rangle$ and $Q\langle 16 \rangle$ being 0 shows that the transition location is on the second rotation and between $Q\langle 16 \rangle$ and $Q\langle 31 \rangle$, which is defined as the fourth quarter. The length of the first quarter and the third quarter is 15, and the length of the second quarter and the fourth quarter equals $\tilde{N} - 15$, where \tilde{N} stands for the expected average number of stages which just cover half of the normal-phase length quantization.

q_{TR} is calculated by the sum of the in-quarter output ($Z\langle 0:3 \rangle$ or $K\langle 0:3 \rangle$) and the previous-quarter compensation (0 or 15 or \tilde{N} or $\tilde{N} + 15$):

$$q_{TR} = \begin{cases} Z < 0:3 > + 0 & , Q < 1,16 > = 1,0 \\ K < 0:3 > + 15 & , Q < 1,16 > = 1,1 \\ Z < 0:3 > + \tilde{N} & , Q < 1,16 > = 0,1 \\ K < 0:3 > + \tilde{N} + 15 & , Q < 1,16 > = 0,0 \end{cases} \quad (46)$$

The outputs of $Q < 1 >$ and $Q < 16 >$ are used to control two multiplexers, which will pick up a proper input for correct computations. Specifically, for the situation that the phase difference is less than 48ps, q_{TR} can be expressed by only $Z < 0:3 >$. For the situation that the phase difference from 48ps to less than $(\tilde{N} + 1) \cdot 3ps$, q_{TR} should be $K < 0:3 >$ plus 15, where 15 is the number corresponding to the first quarter length quantization. Similarly, from $(\tilde{N} + 1) \cdot 3ps$ to less than $(\tilde{N} + 16) \cdot 3ps$ of the phase difference, q_{TR} equals $Z < 0:3 >$ plus \tilde{N} and q_{TR} also equals $K < 0:3 >$ plus $\tilde{N} + 15$, where $\tilde{N} + 15$ corresponding to the first three quarters quantization.

Most of the time during the operation, single transition in q_{TR} is the case, meaning that one of $Z < 0:3 >$ and $K < 0:3 >$ should be zero. However, there is a small chance, $Z < 0:3 >$ and $K < 0:3 >$ are non-zero simultaneously (Fig. 61), which corresponds to a double transition situation. It is noticed that the occurrence of the double transition would not impact the operation of the post evaluation owing to $Q < 1 >$ and $Q < 16 >$ being able to choose the proper one (between $Z < 0:3 >$ and $K < 0:3 >$) for next step calculation. Most importantly, double transition detection would be used for \tilde{N} calibration due to PVT and volume variation. It is determined by conducting subtraction between $K < 0:3 >$ and $Z < 0:3 >$ as:

$$\widetilde{N}(\tilde{n}) = |K(n) < 0:3 > - Z(n) < 0:3 >| + 15 \quad (47)$$

Performing the \tilde{N} -calibration improves the linearity like the rippled counting error of a TDC mentioned in [35], [36]. Note that the \tilde{N} -calibration procedure is performed without stopping the operation of the TDC and the DPLL system. The implementation of the non-interruption self-calibration circuit is shown in **Fig. 60** (c).

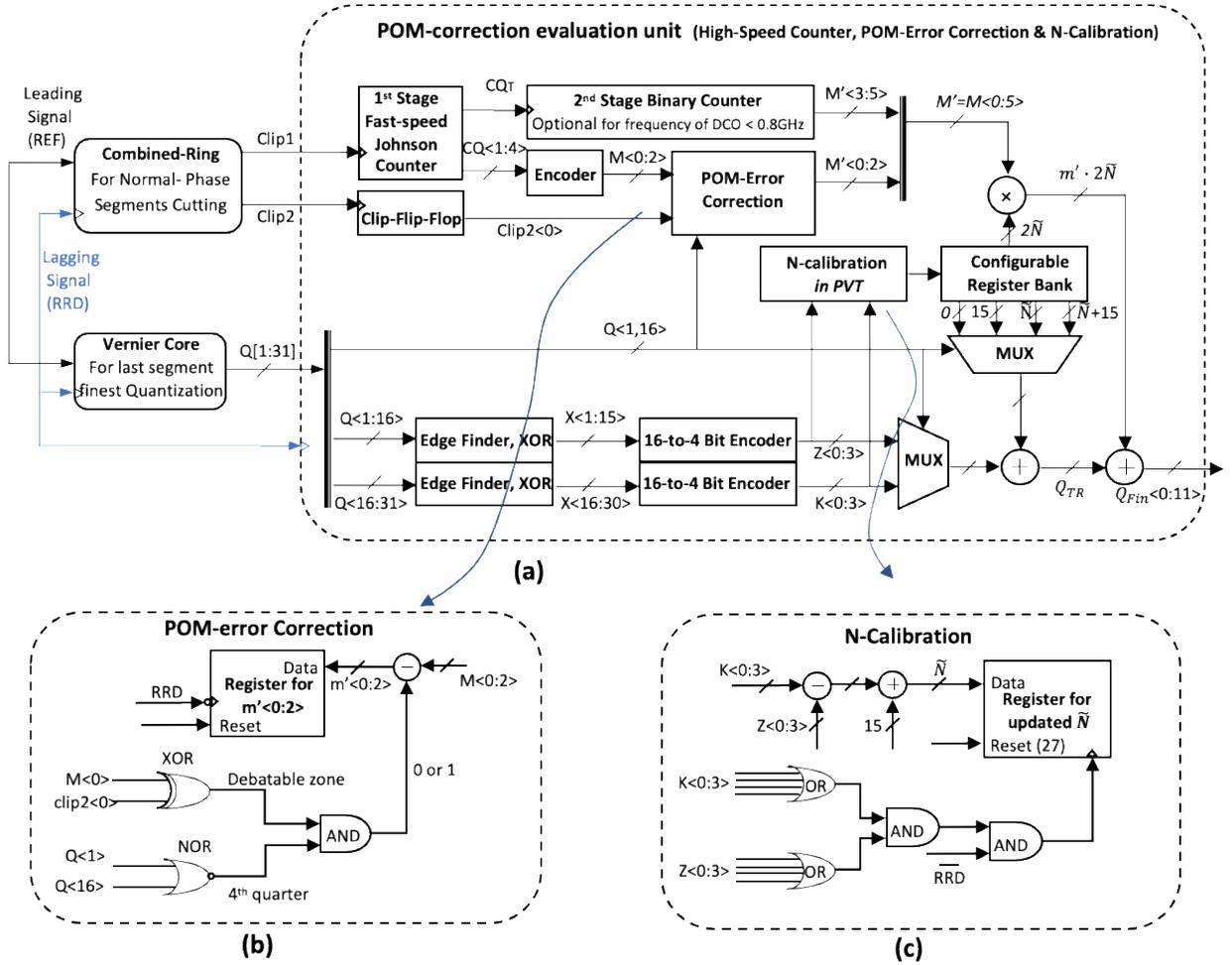


Fig. 60 (a) Implementation of the evaluation unit, (b) Implementation of the POM-error correction circuit, (c) Implementation of the self-calibration circuit.

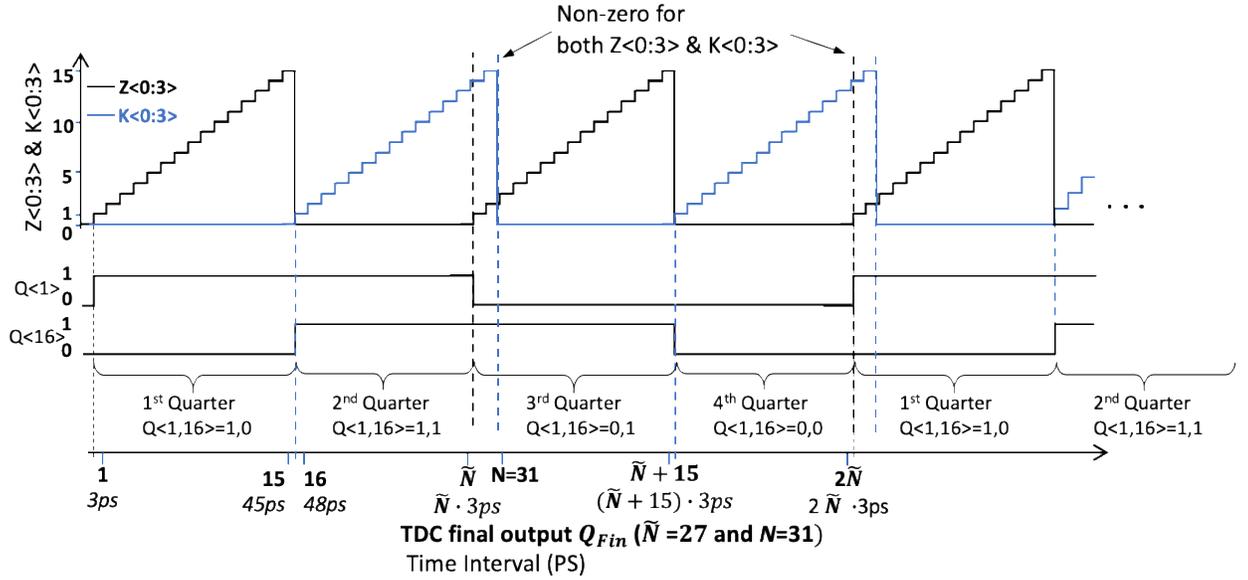
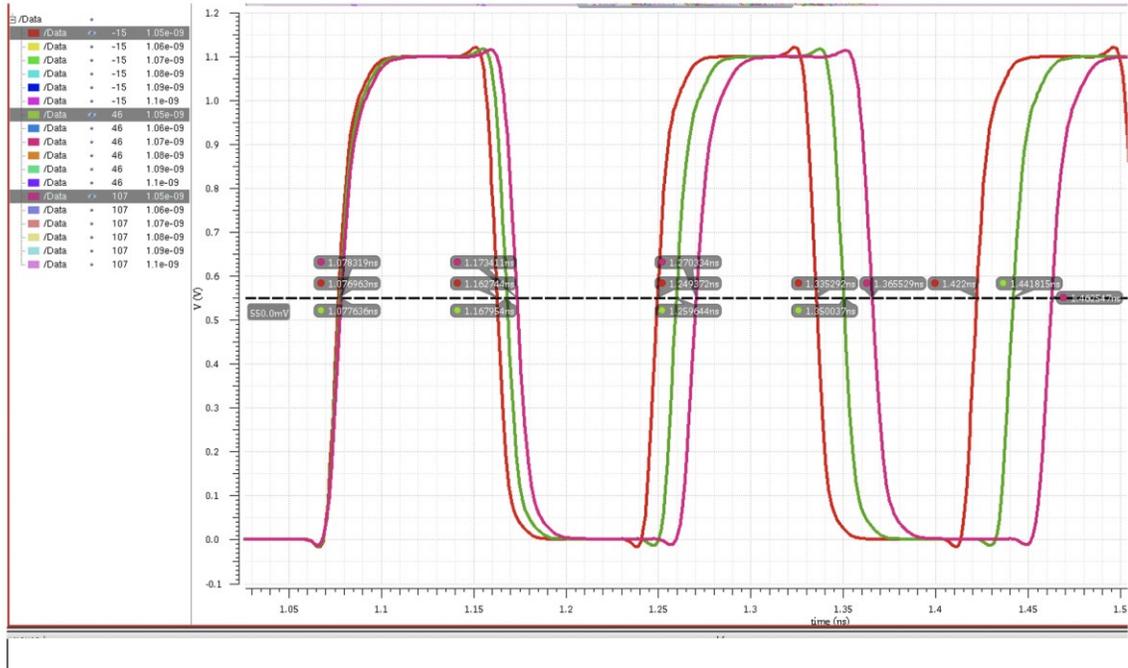


Fig. 61 Illustration of the Quarter No. identification and \tilde{N} -calibration (when $Z<0:3>$ & $K<0:3>$ being non-zero)

Note that on-going N-calibration could encounter two different \tilde{N} s that correspond to first and second half periods of the signal propagating along the conjoined ring, unless the duty cycle of the signal is exactly 50% making the two of them identical. In our design, to simplify the calibration circuit, a 50% duty cycle of the signal along the conjoined ring is pursued so that one \tilde{N} parameter value would fit best for both. Fig. 62 shows the circuit could be optimized and meet the requirement of 50% of duty cycle with temperature ranging from -15 to 107 degree, and the maximum mismatch would not be more than 1ps.

Note that the on-going N-calibration is mainly for compensating the mismatch between the conjoined ring and Vernier core circuits in PVT variations. The common mode offset of above two parts with PVT variations would be calibrated in ADPLL digital part with a calibration parameter table.



Temp condition	-15 p	-15 n	46 p	46 n	107 p	107 n
Loop width 1(ps)	163-77=86	250-163=87	168-77=91	260-168=92	173-78=95	270-173=97
period	173		183		192	
Loop width 2(ps)	335-250=85	422-335=87	350-260=90	442-350=92	365-270=95	462-365=97
period	172		182		192	

Fig. 62 Optimization and Simulation for 50% duty cycle of the signal along the conjoined ring.

4.11 Arbiter Set Design for Vernier Core

In pre-logic (RRD generation) circuit design (section 4.6) and the high-speed loop counter design (section 4.8), static master-slave flip-flops have been employed mainly due to the purpose of avoiding risks of race-through issues. Race-through may take place under the conditions of first, pipelined (staged up) flip-flops structure and second, negative setup delay time (T_{setup}). If T_{setup} is positive, which is always true in traditional (static master-slave) flip-flops, the output updates its change that reflects the input data state after the

clock edge and its value relies on the data state that setup before clock edge, keeping data change from jumping over two flip-flops in one clock cycle.

In the Vernier delay chain arbiter set design, an encoding circuit is supposed to follow the flip-flop set so that there is no need to worry about the race-through issue. Thus, a set of half dynamic (pre-charged) flip-flops may be optional due to the advantage of its negative T_{setup} property. However, the common inferior performance parameter of the half dynamic flip-flops compared to their static counterparts is the mismatch delays between the falling and rising responses, which can lead a bubble error of the output in a fine time resolution design. The solution to make half dynamic flip-flops viable is to alter the inverter-based delay chains to buffer-based delay chains. This solution has been implemented in second round of the implementation. SDFFs (Fig. 63) have been used to achieve high performance and low power dissipation.

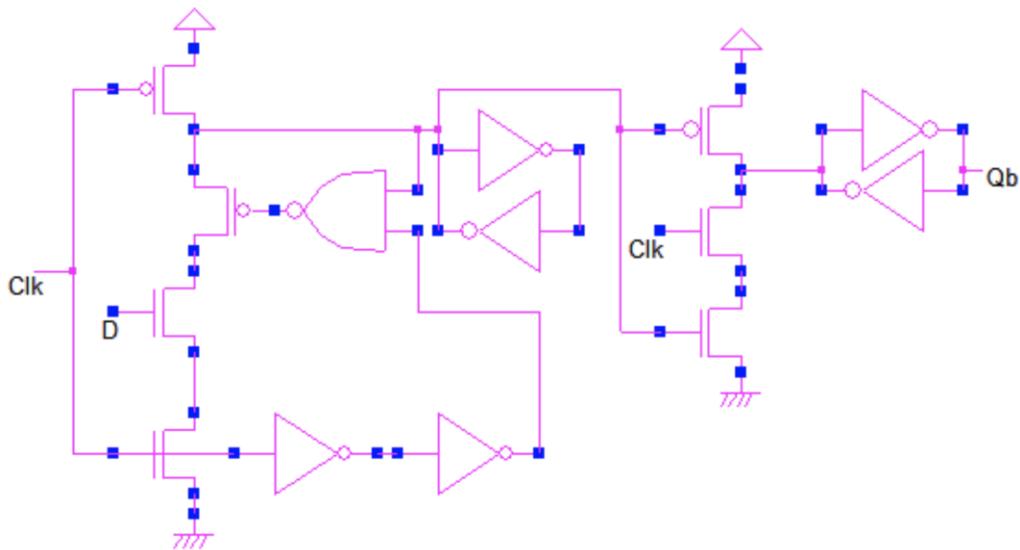


Fig. 63 Transistor level schematic illustration of a semi-dynamic flip-flop (SDFF)

4.12 Fast Delay Chain Design with Configurable Pseudo-NMOS Inverters

As mentioned in design of the Vernier delay chain, the time resolution is designated to be a constant value of a few seconds, that comes from the difference of the propagation delay between the transistors in the slow delay chain and the fast one. Generally, considering a safely functional device with a certain margin that allows the deviation due to process, voltage, temperature and volume variation, a sub-picosecond time resolution of a TDC is not easy to be realized practically.

We would like to challenge sub-picosecond time resolution performance in the second-round fabrication of this project. Specifically, a digitally controlled tunable scheme would be created to achieve an ultra-competitive performance and reliability simultaneously. Fig. 64 illustrates a schematic of one stage of the Vernier delay chain that includes a voltage control function (by V_{Tune}). The propagation delay of the inverters on the fast delay chain could be tuned by changing the value of V_{Tune} , and consequently the difference of the propagation delay between the transistor pair on the same stage of the fast and slow delay chain would change as well. In Fig. 64, CLK_x and D_x stand for the signal on a certain stage of the fast and slow delay chains respectively, and Q_x indicates output of the flip-flop (arbiter) of a certain stage. The subscripts (x) for them imply the stage number.

The voltage-controlled inverters in the fast delay chain are implemented by tunable pseudo-NMOS inverters that are shown at the transistor level in Fig. 65. Unlike the connection of the gate terminal of the PMOS transistor in pseudo-NMOS which is grounded, the tunable pseudo-NMOS inverter has the gate connected to an analog voltage

control terminal that ranges from 0.045 to 0.075 volts. The selection of the voltage range is based on the request of making $\Delta\tau$ tunable from 2ps down to 0.5ps.

Fig. 66 illustrates another tunable voltage control Vernier delay stage but with a semi-dynamic flip-flop as the arbiter, in which a buffer-based delay element is used to make a single clock trigger available. The power consumptions of static and half-dynamic style TDC cores are comparable.

Note that in the time period of the high-level state of the signals along the fast delay chain, leakage current exist in tunable pseudo-NMOS transistors, which is similar to the nature of traditional pseudo-NMOS inverters. To address this unwanted power dissipation, a pulse style of the lagging signal may be desirable in the design and implementation.

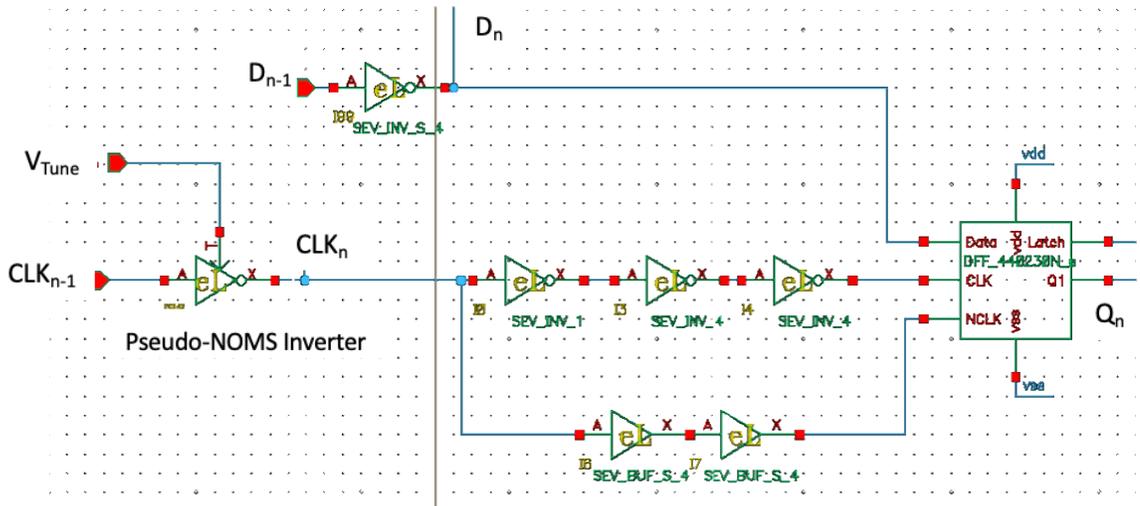


Fig. 64 schematical illustration of the n^{th} Vernier delay stage with a tunable voltage control in clock propagation delay.

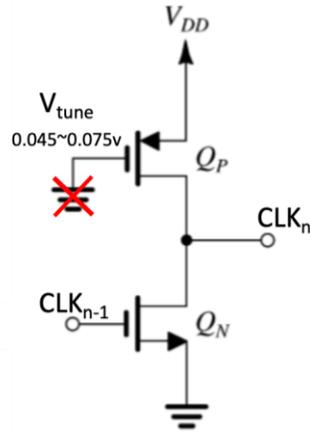


Fig. 65 Illustration of the tunable pseudo-NMOS inverter for propagation delay control function.

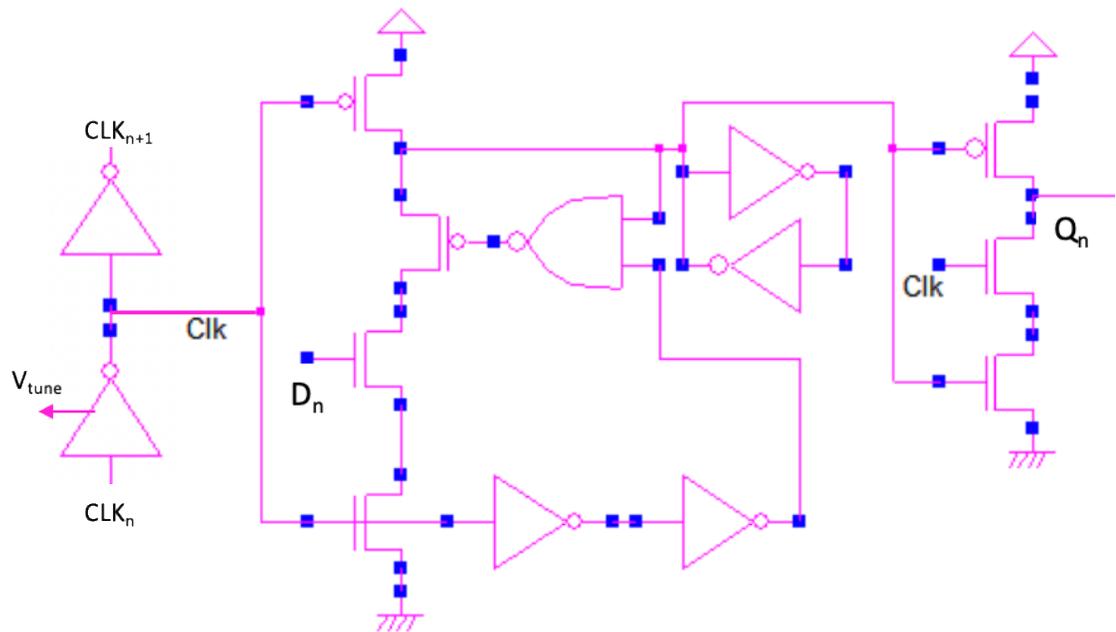


Fig. 66 schematical illustration of the n^{th} Vernier delay stage with a tunable voltage control in clock propagation delay for the SDFF circuit.

The digital control system for the tunable pseudo-NMOS circuits is shown in Fig. 67. 3-digit binary number ($D[0:2]$) is used as the input control with seven control options and

it will be decoded in to a 7-bit thermometer coding number (C[1:7]) in which only one digit is supposed to be set to zero (low level). C[1:7] will be fed into a digital-to-analog voltage conversion to generate the output (V_Tune). The digital-to-analog voltage converter is comprised of a set of voltage dividers that includes series resistors and a PMOS switch connecting to each node, as shown in Fig. 68. The analog voltage control (V_{Tune}) ranges from 0.045v, when C<7> is the only low-level, to 0.075v, when C<1> is the only low-level. Fig. 69 illustrates a calculator that finds out the voltage dividing resistors' value.

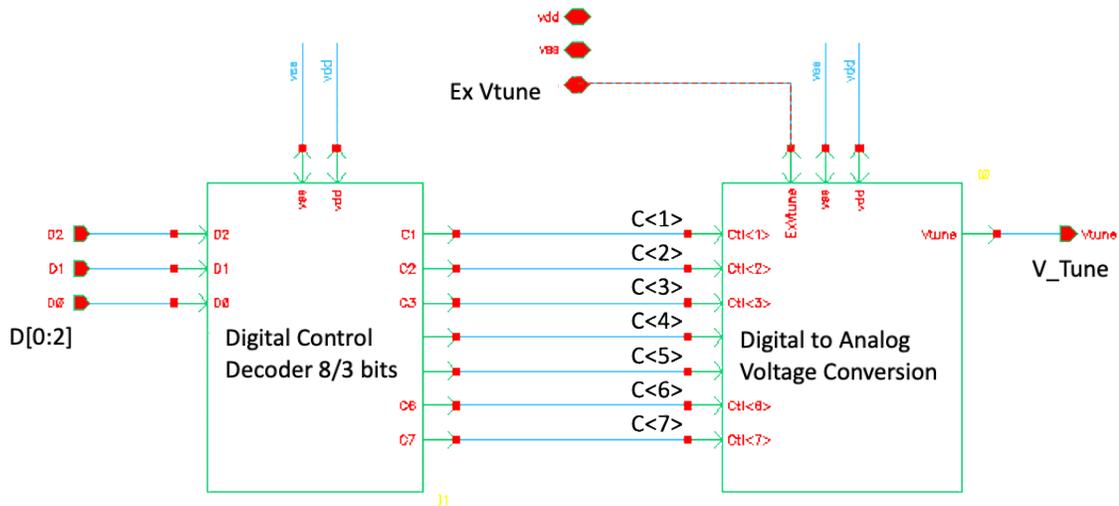


Fig. 67 Block diagram of digital control system.

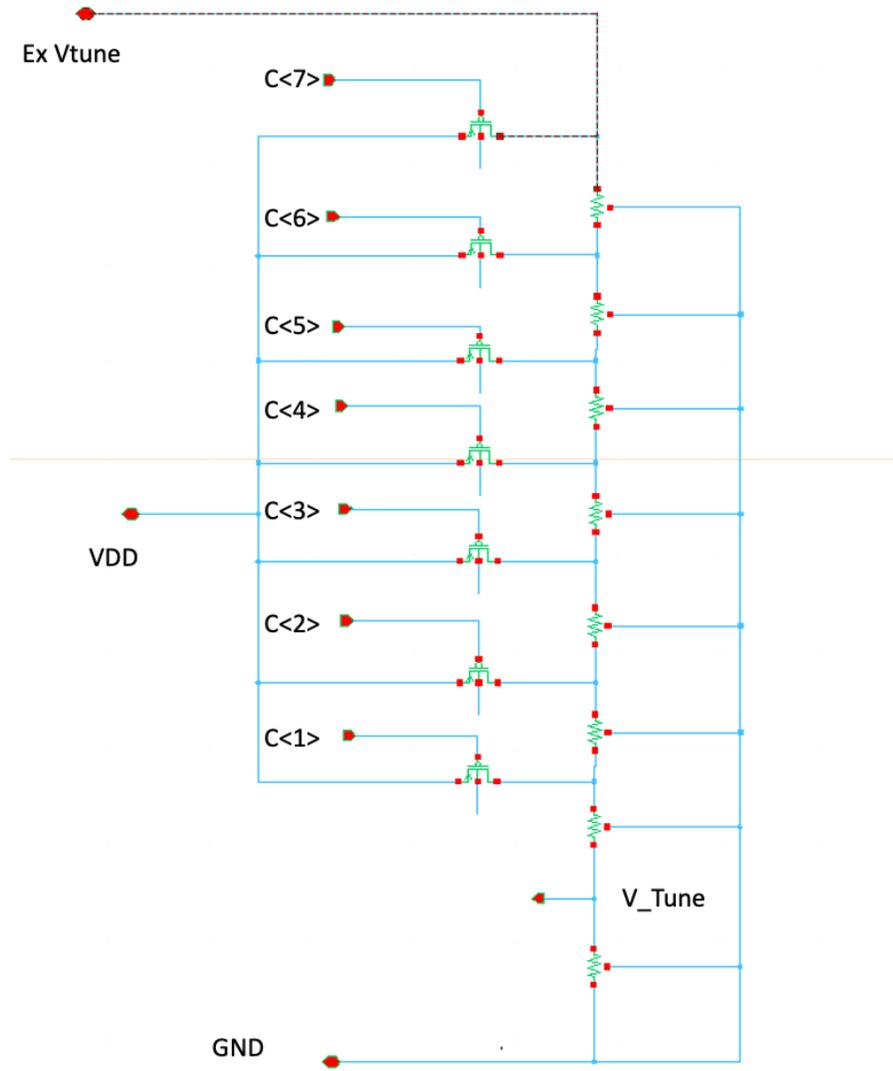


Fig. 68 Schematic of the digital to analog voltage converter.

					Resistance		Coefficient	Vtune(v)
All PMOS off		Output						
P7 GATE, C<7>	1	z	----->					
desired Vtune (v)	0.045			R1	1.222222	kohm	11.72222	0.045505678
P6 GATE, C<6>	1	z	----->					
desired Vtune (v)	0.05			R2	1	kohm	10.5	0.050500897
P5 GATE, C<5>	1	z	----->					
desired Vtune (v)	0.055			R3	0.833333	kohm	9.5	0.055496139
P4 GATE, C<4>	1	z	----->					
desired Vtune (v)	0.06			R4	0.705128	kohm	8.666667	0.060491404
P3 GATE, C<3>	1	z	----->					
desired Vtune (v)	0.065			R5	0.604396	kohm	7.961538	0.065486691
P2 GATE, C<2>	1	z	----->					
desired Vtune (v)	0.07			R6	0.52381	kohm	7.357143	0.070482002
P1 GATE, C<1>	1	z	----->					
desired Vtune (v)	0.075			R7	6.833333	kohm	6.833333	0.075477334
				R8	0.50	kohm		

Fig. 69 Voltage dividing resistors' value calculator.

4.13 Testbench Circuits Design

An on-chip testbench system is expected to be implemented in parallel with the TDC design to verify its performance from the perspective of time resolution, linearity and so forth, especially without the operation of the ADPLL system. The testbench allows the TDC to operate independently and should be provided with various TDC inputs (phase difference between the leading signal and the lagging signal).

As shown in the test bench diagram (Fig. 70), there are two optional paths that provide a pair of signals (the leading and lagging signals). One path is called internal path and its source comes from a ring oscillator implemented on-chip with its operating frequency at 400MHz. A couple of branches have been pulled out along the ring oscillators to generate various time interval pairs. The length of the time interval is supposed to be digitally controlled and range from 100ps to 1000ps with a granularity of 100ps. Those ten internal-sourced inputs are expected to act as a calibrator in the measurement system (coordinate). Specifically, those discrete reference points form a precise linear line connecting them to

indicate the slope (time resolution) performance of the TDC to be tested. The ring oscillator is followed by a configurable frequency division circuit to setup the desired reference frequency of the internally generated signal to be 25MHz, 50MHz or 100MHz for measurement.

The other option to choose the leading and lagging signal pair is to use an external signal generator combined with a tunable delay unit. The length of the time interval between the leading and lagging signals can be continuously controlled by tuning the DC bias voltage of the tunable delay block. Fig. 71 illustrates the method to obtain a continuously varying time interval, in which basically the buffer units could be tuned in propagation delay by tuning the DC voltage supply for them. The relative time interval range would cover $\pm 20\%$ of the rated value that corresponds to the propagation delay at 0.97 volt. The DC bias range would roughly range from 0.85 volt to 1.10 volt. An expandable range of 0.8 to 1.15 volt could guarantee the overlap of the coverage between adjacent branches. The time interval coverage of each branch is shown in Fig. 72. One thing that needs to be emphasized is the external path source of the leading and lagging signal pair should be calibrated by the internal ring oscillator to eliminate the nonlinearity due to the DC voltage biasing (propagation delay changes with DC supply reversely). To further improve the granularity of the time interval of the testbench, the digitally controlled tunable time interval system (described in previous section) could be used.

In summary, the internal and the external time interval sweep setup can provide a linear and continuous time interval range up to 1.3ns for the TDC measurement and evaluation.

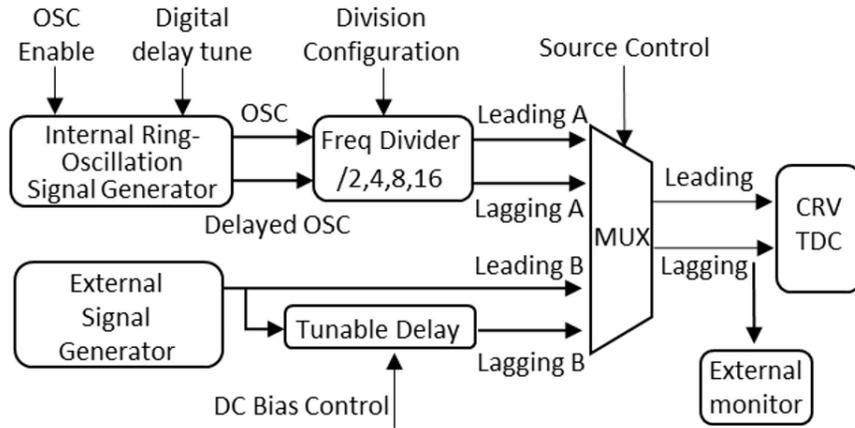


Fig. 70 Block diagram of the on-chip testbench.

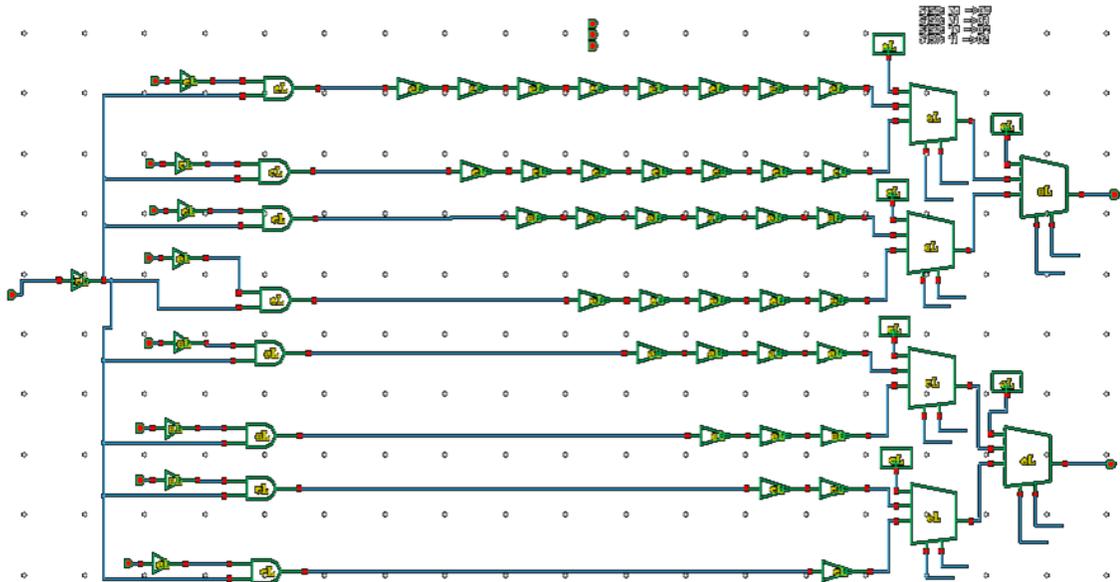


Fig. 71 Tunable delay unit in the external source path.

Sub Path #	-20%	Rated time interval	20%
	(ps)	(ps)	(ps)
Branch 0 (shift -40 ps from 1)	44	65	86
Branch 1	84	105	126
Branch 2	124	155	186
Branch 3	164	205	246
Branch 4	248	310	372
Branch 5	332	415	498
Branch 6	456	570	684
Branch 7	664	830	996
Branch 8	872	1090	1308

Fig. 72 Time interval coverage of the tunable delay unit branches.

The other consideration of the testbench would be whether the edge rate variation of the external generated signal impacts the measurement result or not. A simulation with various edge rates and temperatures has been performed and shown in Fig. 73. It can be seen in simulation result that the time resolution result (indicated by slope of the curve) basically stays constant. This is predictable because the leading and lagging signal come from one signal source and the variation would be same for both leading signal and lagging signal. However, there is a small shift among curves, especially for large edge rate situations. Thus, an average over multi-samples would be expected during the measurement to overcome the edge rate impact.

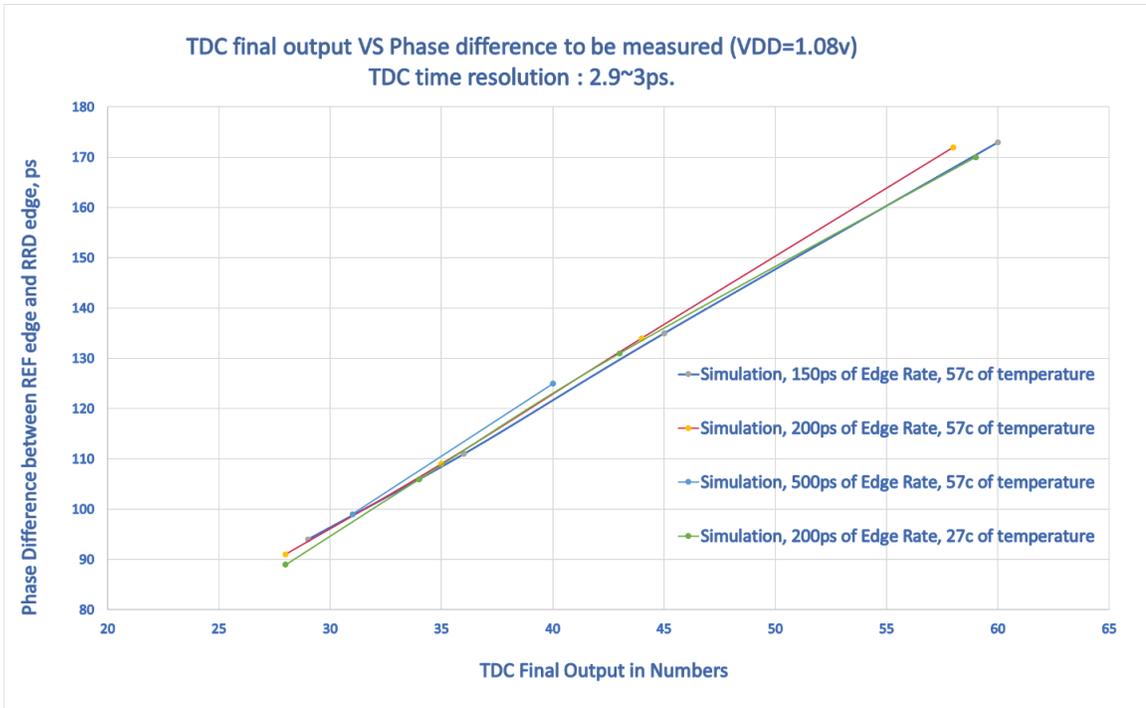


Fig. 73 External signal source's edge rate impact simulation.

4.14 Conclusion

A competitive TDC architecture and circuit has been developed to achieve many advantages, that includes: POM error correction (25dB phase noise improved), configurable time resolution scheme with as good as sub-picosecond time resolutions, coarse/fine structure switchable for trade-off between performance and power consumption, short latency feature enabling high reference frequency applied, and double-sampling circuit and its surrounding circuit to cancel the phase error caused by metastability issue. The next chapter will present the implementation and fabrication based on this design as well as the measurement result.

Chapter 5: Layout Implementation

This chapter presents two versions of layout implementations of the proposed TDC designs, and the corresponding chip level fabrications, bonding and packaging designs. The layout designs have been performed in Cadence Virtuoso Layout with 45nm and 40 nm TSMC and eight metal layers for traces' routing.

5.1 32-stage Layout Implementations

The first-round implementation of the conjoined-ring Vernier TDC design is to mainly verify the validation and functionality of the conjoined-ring and its synergy with Vernier TDC delay chain. As shown in Fig. 74, the core layout (main area) of the 32-stage conjoined-ring Vernier TDC includes on-chip ring oscillator (#1.1), configurable frequency divider (#1.2), external signal path with tunable delay control (#1.3), multiplexer and pre-logic circuit (#1.4), conjoined ring and clipping switches circuit (#1.6), Vernier delay chain (#1.7), loop counter (#1.8), and edge finder and decoder circuits (#1.9). The core circuits are surrounded by metal and poly dummy fills (#1.5) that are performed manually inside of the core circuits and automatically outside of the core part. The core circuit occupies in an area of 85um * 100um.

Fig. 75 illustrates the overall layout design of the 32-stage conjoined-ring Vernier TDC in chip level. Beside core circuit (main area, #1) that is zoomed in and presented in Fig. 74, the chip also includes some post evaluation and buffers (#2), power supply distributions (#3) and ESD circuits and pads that are used for solid connection with exterior for the purpose of providing with DC power supply, external signal connection, digital control paths and output measurement paths.

Fig. 76 is the top-level schematic design that corresponds to the layout design shown in Fig. 75, and briefly shows the logical connections among the blocks and definitions of the ports.

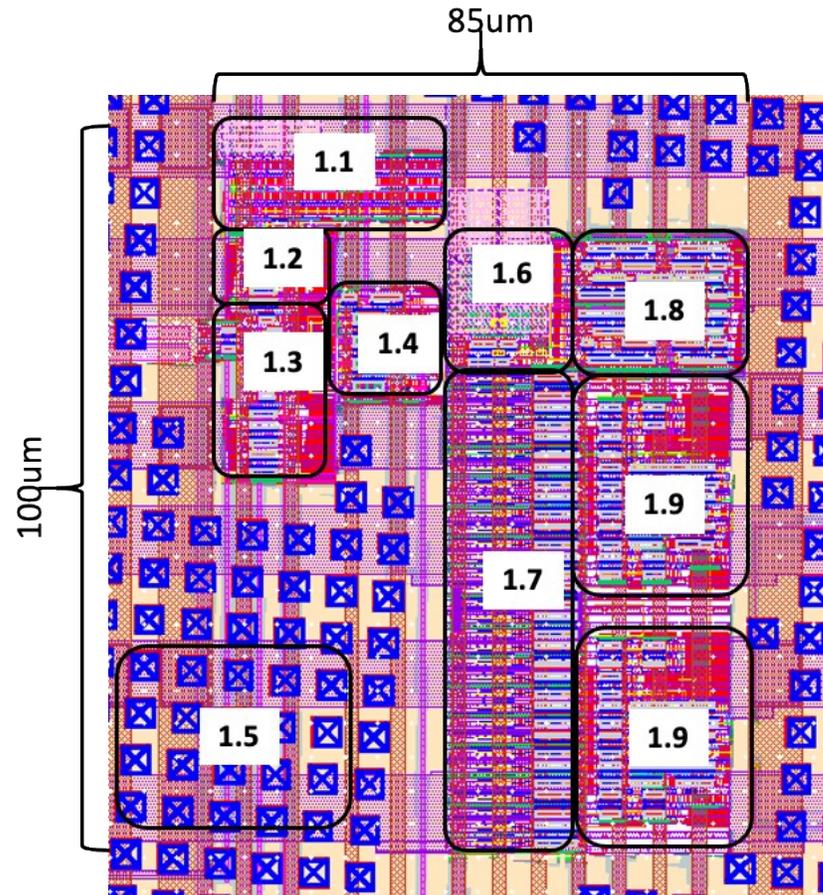


Fig. 74 32-stage conjoined-ring Vernier TDC layout with blocks definitions: 1.1: On-chip ring oscillator; 1.2: Configurable Frequency Divider; 1.3: External signal path with tunable delay control; 1.4: Multiplexer and some pre-logic circuit; 1.5: Metal and poly dummy-fill; 1.6: Conjoined ring and clipping circuit; 1.7: Vernier delay chain; 1.8: Loop counter; 1.9: Edge finder and decoder

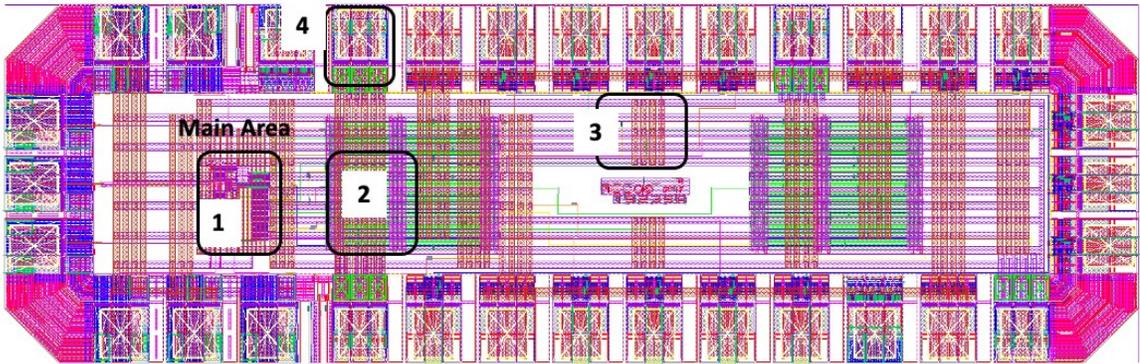


Fig. 75 32-stage conjoined-ring Vernier TDC Die layout: 1. Main area; 2. Some post evaluation and buffers; 3. Power supply distributions; 4. ESD and pads for bounding.

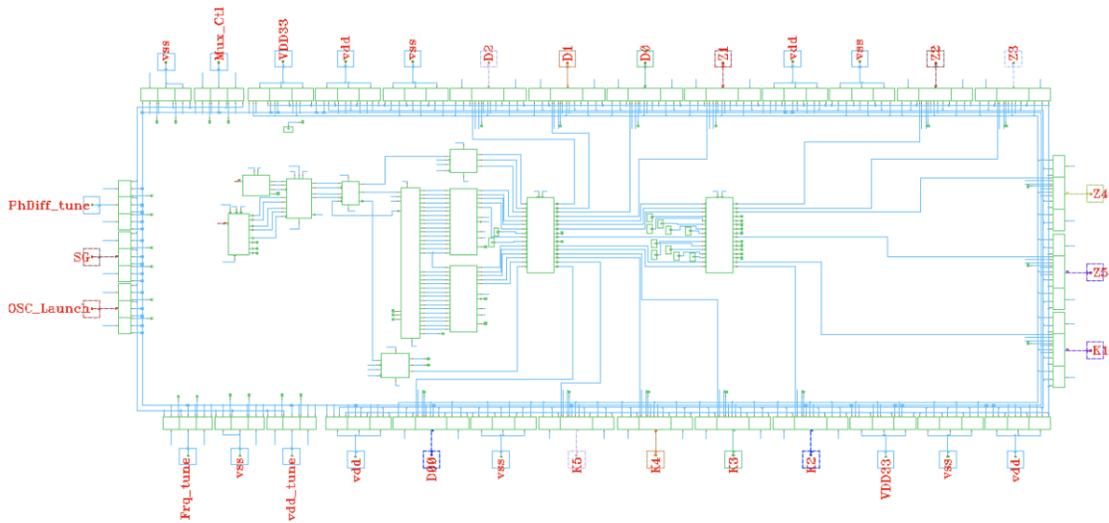


Fig. 76 Vernier delay chain top-level schematic illustration.

5.2 Vernier delay chain

Vernier delay chain is basically the most important part of the TDC due to it functioning the time resolution performance by measuring the difference of the two inter-stage propagation delay between the slow and fast chain. Theoretically, the time difference

comes only from the propagation delays of two inverters in a certain stage. However, in practice, in addition to above factor, the parasitic resistive and reactive existence of the connecting traces between stages and the branch traces could affect the delay and strength of the propagation of the signals. Obviously, various characteristics of the traces (thickness, width and length etc.) cause different parasitic. Automated drawing of the interconnected traces may not guarantee the consistent length of the traces between stages as well as the circumstance around the traces. Consequently, the deviations of the parasitic existence cause mismatch and result in nonlinearity of the TDC performance, degrading TDC time resolution performance. In some extreme PVT situation, TDC operation could be even ruined when mismatch introduced larger than rated time resolution especially for sub-picosecond time resolution design.

Thus, the layout of the vernier delay chain is quite crucial and should be done manually rather than automatedly. One rule that is necessary to be applied to control the mismatch (nonlinearity) problem is all inter-connection traces among in the Vernier delay chain should be drawn in same width and length at same layers. In our design, a more stringent constraint has been forced to maximumly reduce the impact of the parasitics. In implementation, the interconnected traces have been drawn fully duplicatedly and the same circumstances have been imposed on in order to form same parasitic capacitances. Those above measures ensure same resistive and reactive parameters that imposed on each stage, canceling out the affection caused by the interconnected traces.

Apparently, to ensure the interconnected traces duplicated, a reasonable arrangement of the circuit should be considered and conducted. Fig. 77 illustrates the floorplan of the Vernier TDC delay chain in which each stage (one slow chain inverter, one fast chain

inverter and one flip-flop) places in a row and the delay chain rolls out downwards.

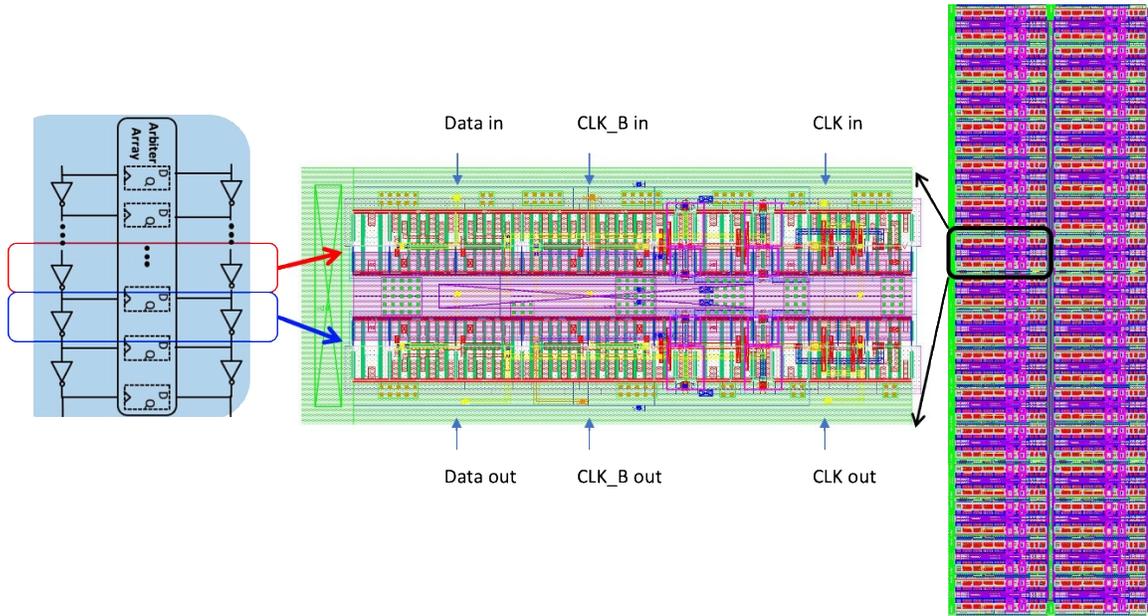


Fig. 77 Vernier delay chain layout.

5.3 Tunable Conjoined-ring Vernier TDC Layout Implementations

An advanced version of the proposed single-ring Vernier TDC, named tunable conjoined-ring Vernier TDC, has been refined based on the 32-stage version one and equipped with tunable inverter stages along the fast delay chain, as shown in Fig. 78. As mentioned previously, SDFFs have been used and to avoid the issue of mismatch between rise and fall edge responses, buffer-based delay stages have been applied.

Fig. 79 presents the tunable conjoined-ring Vernier TDC layout implementation in which the core circuit (A) has been implemented manually and post evaluation has been implemented automatically in Part B (part B also includes digital loop filter for an all-digital PLL implementation). Part C shows the ESD circuit for IO and pads. The overall size for it is 1mm by 0.5mm.

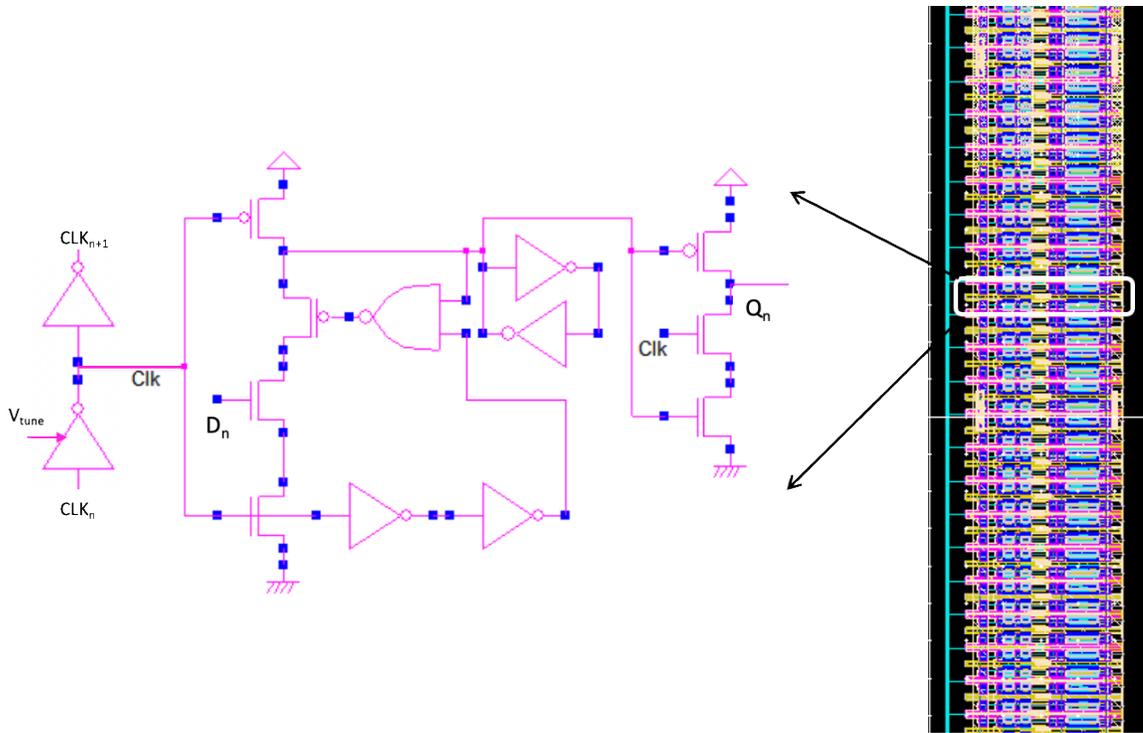


Fig. 78 Tunable Vernier delay chain layout.

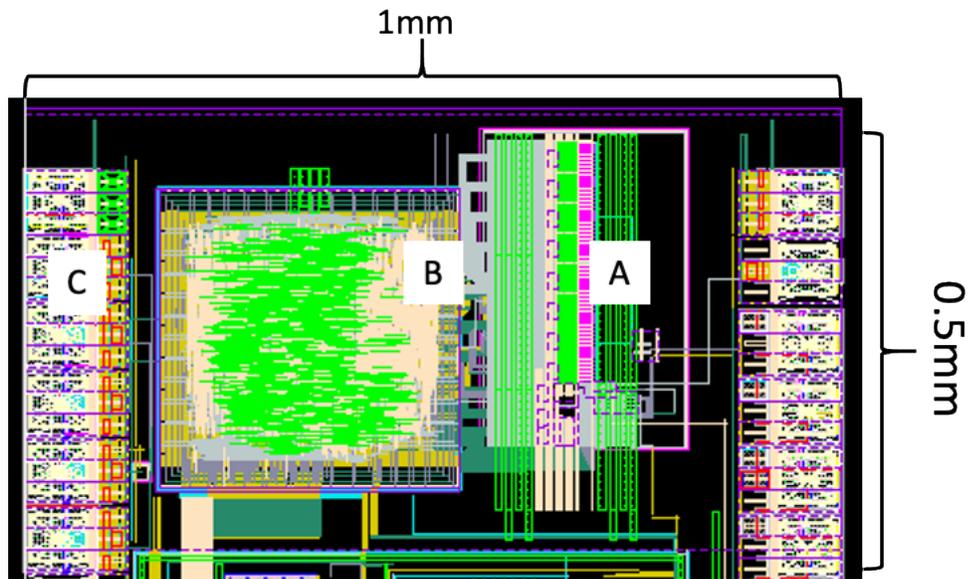


Fig. 79 tunable conjoined-ring Vernier TDC layout: A. Core circuit; B. Post logic evaluation circuit; C. Pads and ESD.

Fig. 80 indicates the TDC core layout view (Fig. 79 part A) in which the following blocks have been implemented to make the whole function works well:

A.1: tunable Vernier delay chain. To make sufficient coverage of 80ps ($0.5 * T_{Nor}$) and target 0.65ps of extreme time resolution performance, a maximum stage number of 128 has been designated.

A.2: Eight TDC delay chain output post evaluators. In the core circuit, there are eight TDC delay chain post logic units that are identical. Each of them deals with 16 stages outputs, mainly conducting transition location determination. Fig. 81 shows one of the TDC delay chain output post evaluators.

A.3: Eight TDC delay chain output (16/4 bit) priority encoders that are used to follow delay chain post evaluators respectively. Each encoder converts 16 stages' delay chain outputs to 4 bits binary code. Fig. 82 illustrates one of TDC delay chain output (16/4 bits) priority encoders.

A.4: Testbench circuits and as shown in Fig. 83.

A.5: TDC Pre-logic and double-sampling RRD circuit. It is to generate the leading and lagging signals and to avoid phase error caused by metastability. It is also presented in Fig. 84.

A.6: Conjoined-ring circuit with clipping switches, and also be emphasized in Fig. 85.

A.7: High speed loop counter with clipping signal indicator and corresponding determination circuit. The outputs of it would be a loop counter and a debatable zone

indicator. The layout of this unit is indicated in Fig. 86.

A.8: High speed DCO period counters with encoders, that is used to count the integer number of DCO period in one reference period (also shown in Fig. 87).

A.9: DCO counting and loop counting output (16/4 bit) encoders. This unit has similar function as above-mentioned delay chain output (16/4 bit) priority encoder.

A.10: Digitally controlled DC voltage supply circuit for configurable time resolution, which is presented in Fig. 88.

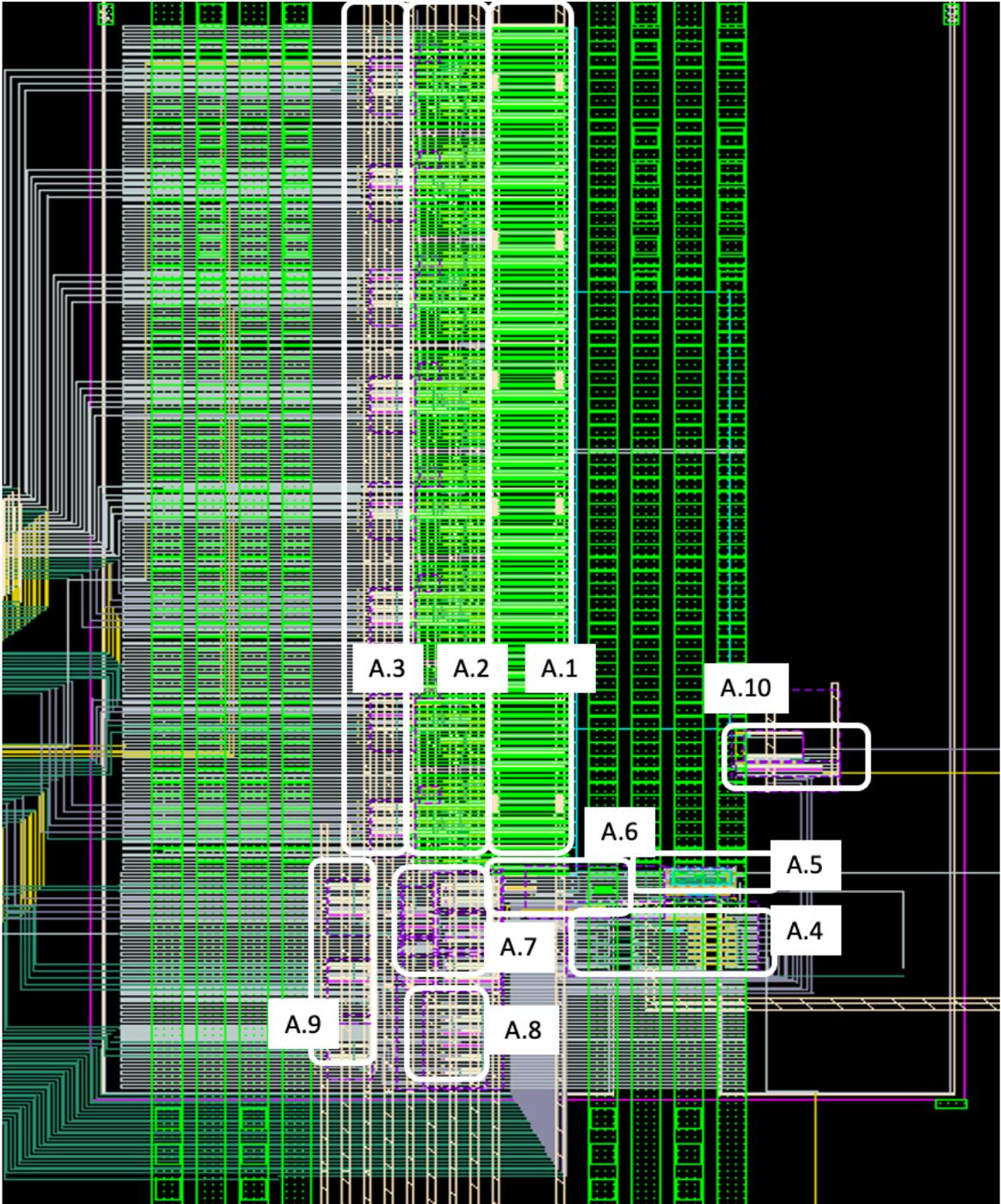


Fig. 80 The core circuit (A) of the conjoined-ring Vernier TDC. A.1: tunable Vernier delay chain (128 stages); A.2: Eight TDC delay chain output post evaluators; A.3: Eight TDC delay chain output (16/4 bit) encoder; A.4: Testbench circuits; A.5: TDC Pre-logic and double-sampling RRD circuit; A.6: Conjoined-ring circuit with clipping switches; A.7: High speed loop counter with clipping signal indicator and corresponding

determination circuit; A.8: High speed DCO period counters with encoders; A.9: DCO counting and loop counting output (16/4 bit) encoders; A.10: Digitally controlled DC voltage supply circuit for configurable time resolution.

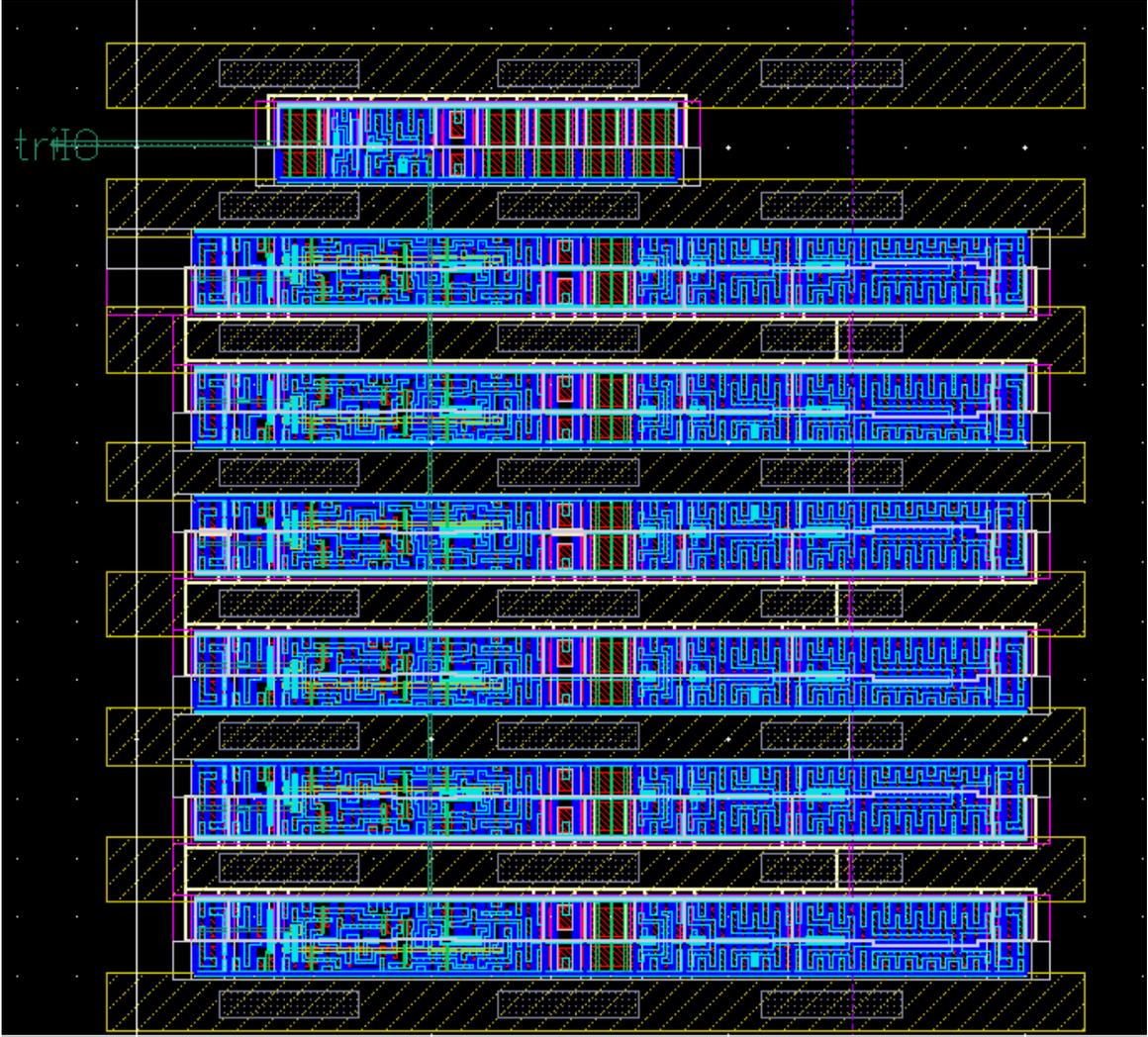


Fig. 81 One of the TDC Vernier delay chain post evaluation (A.2).

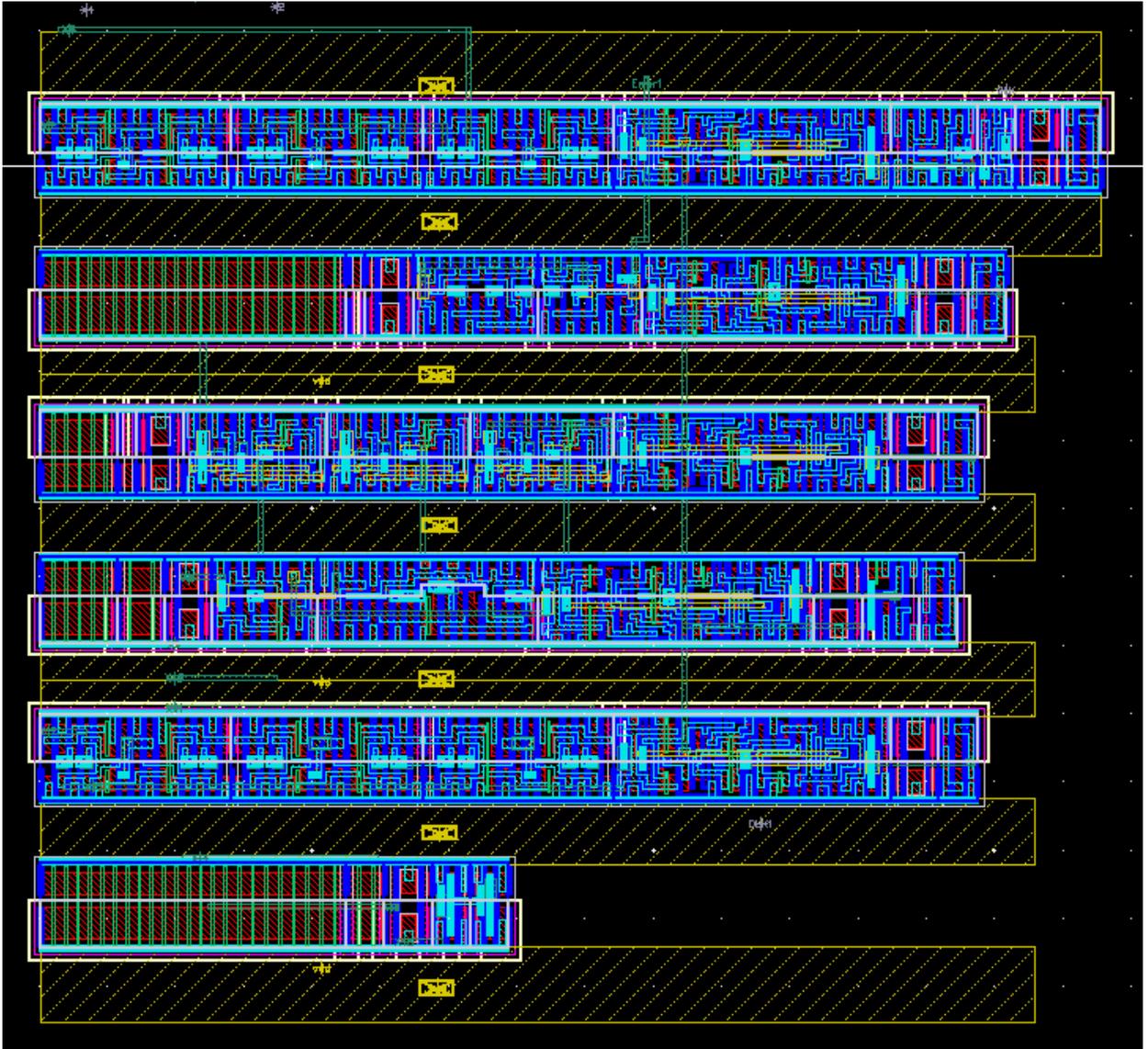


Fig. 82 One of the TDC output (16/4 bit) encoder

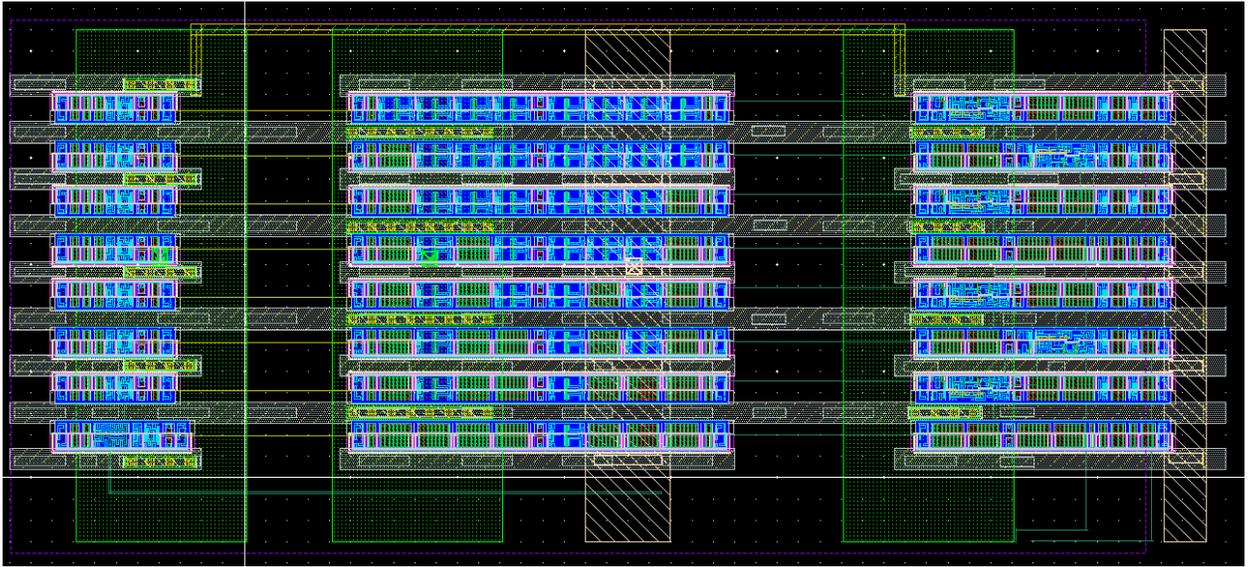


Fig. 83 Testbench Circuit.

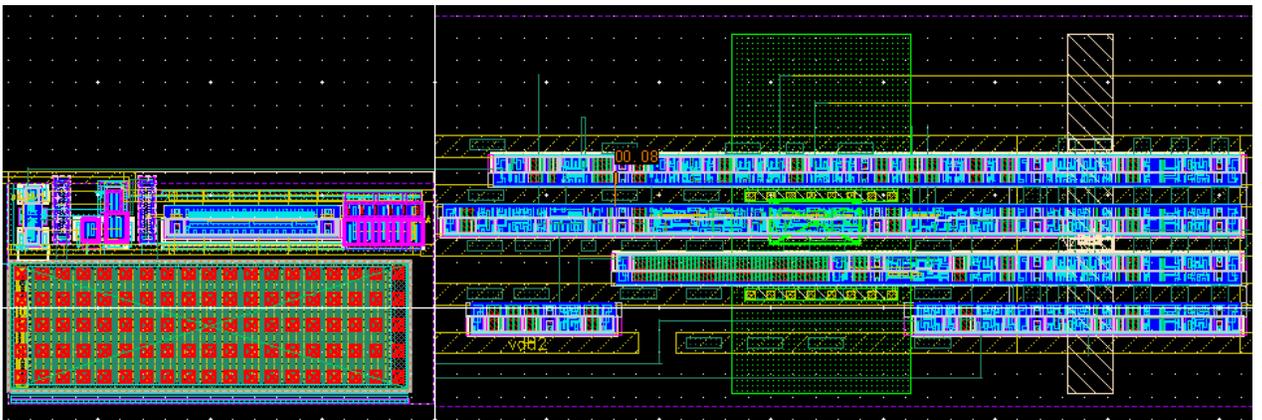


Fig. 84 TDC Pre-logic and double-sampling RRD circuit.

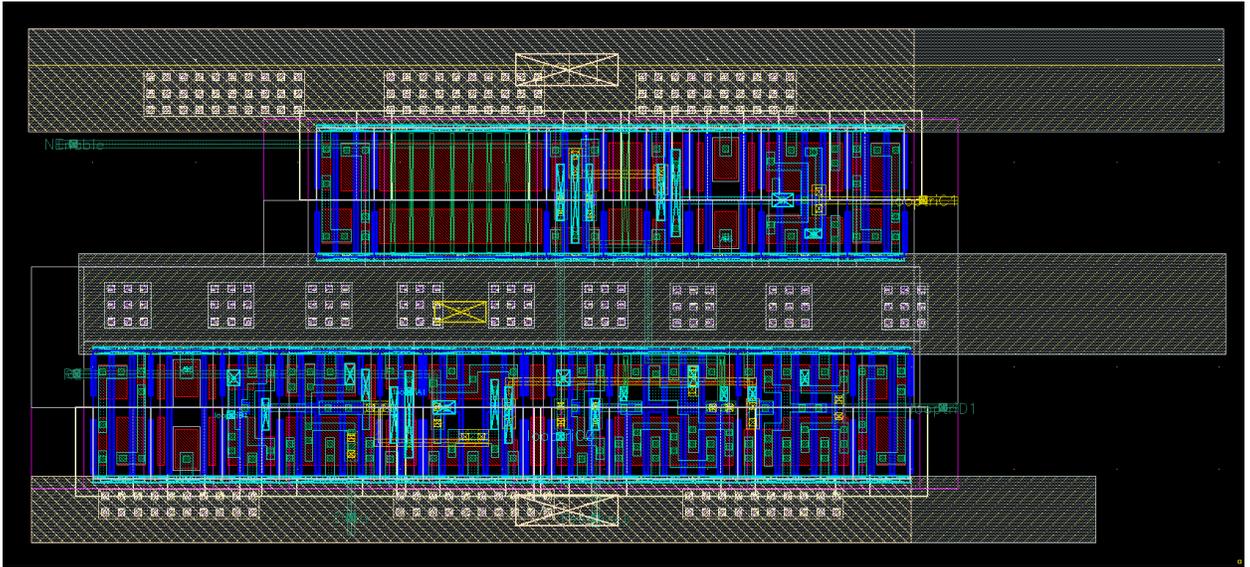


Fig. 85 Conjoined-ring circuit with clipping switches.

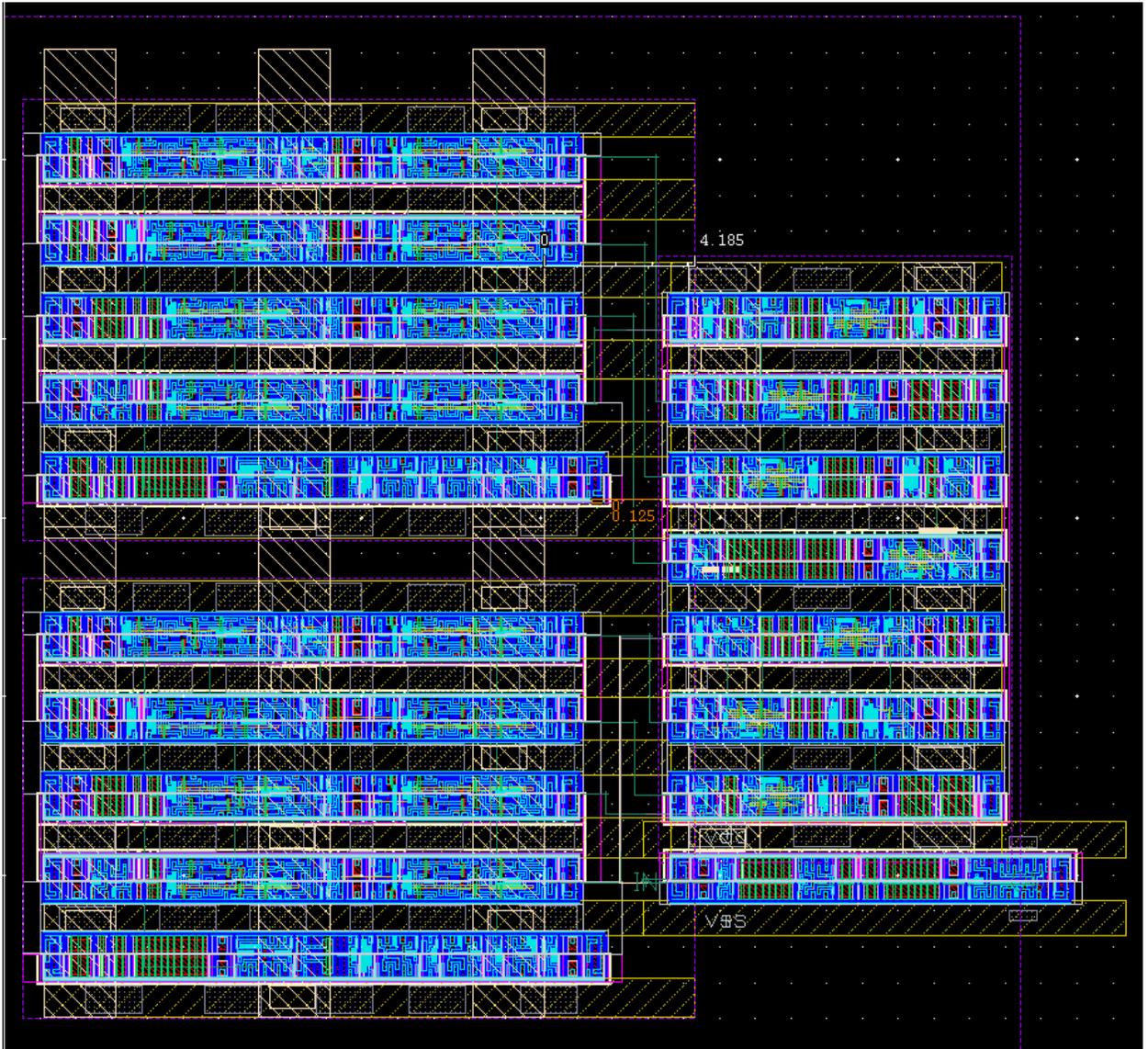


Fig. 86 High speed loop counter with clipping signal indicator and corresponding determination circuit.

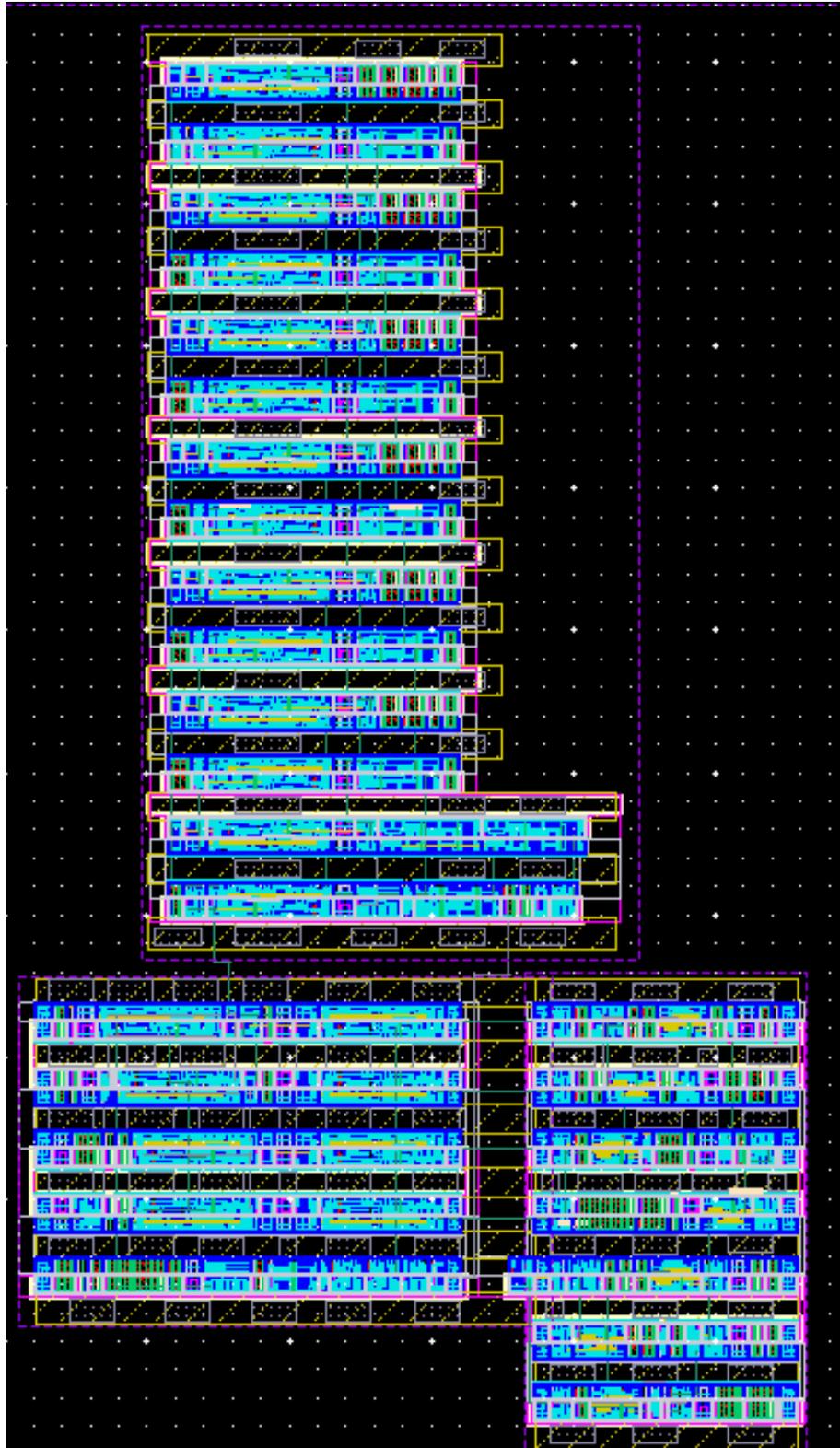


Fig. 87 High speed DCO period counters with encoders.

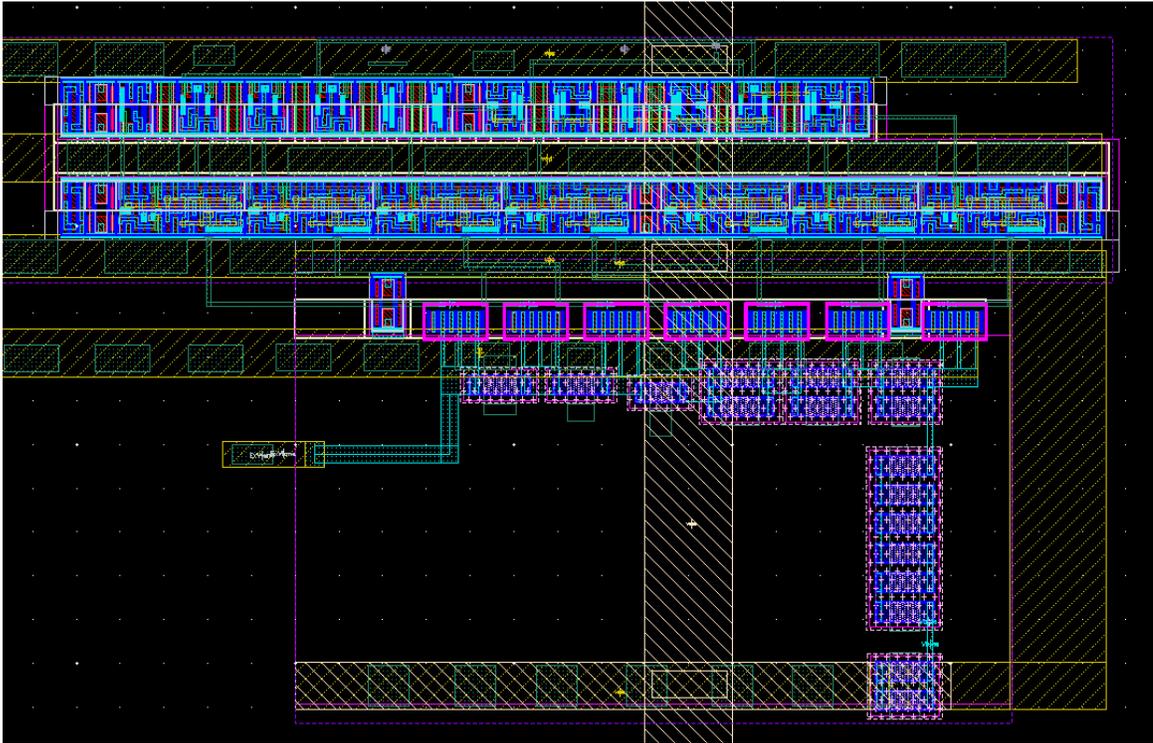


Fig. 88 Digitally controlled DC voltage supply circuit for configurable time resolution.

An all-digital PLL chip-level layout has been demonstrated in Fig. 89, in which part A stands for design of TDC core circuit, part B is about TDC post evaluation circuit plus digital filter design and all digital activities. Part E is for DCO design. Part D is a backup IO interface in SPI style. Part C shows outer pads and ESD circuit underneath.

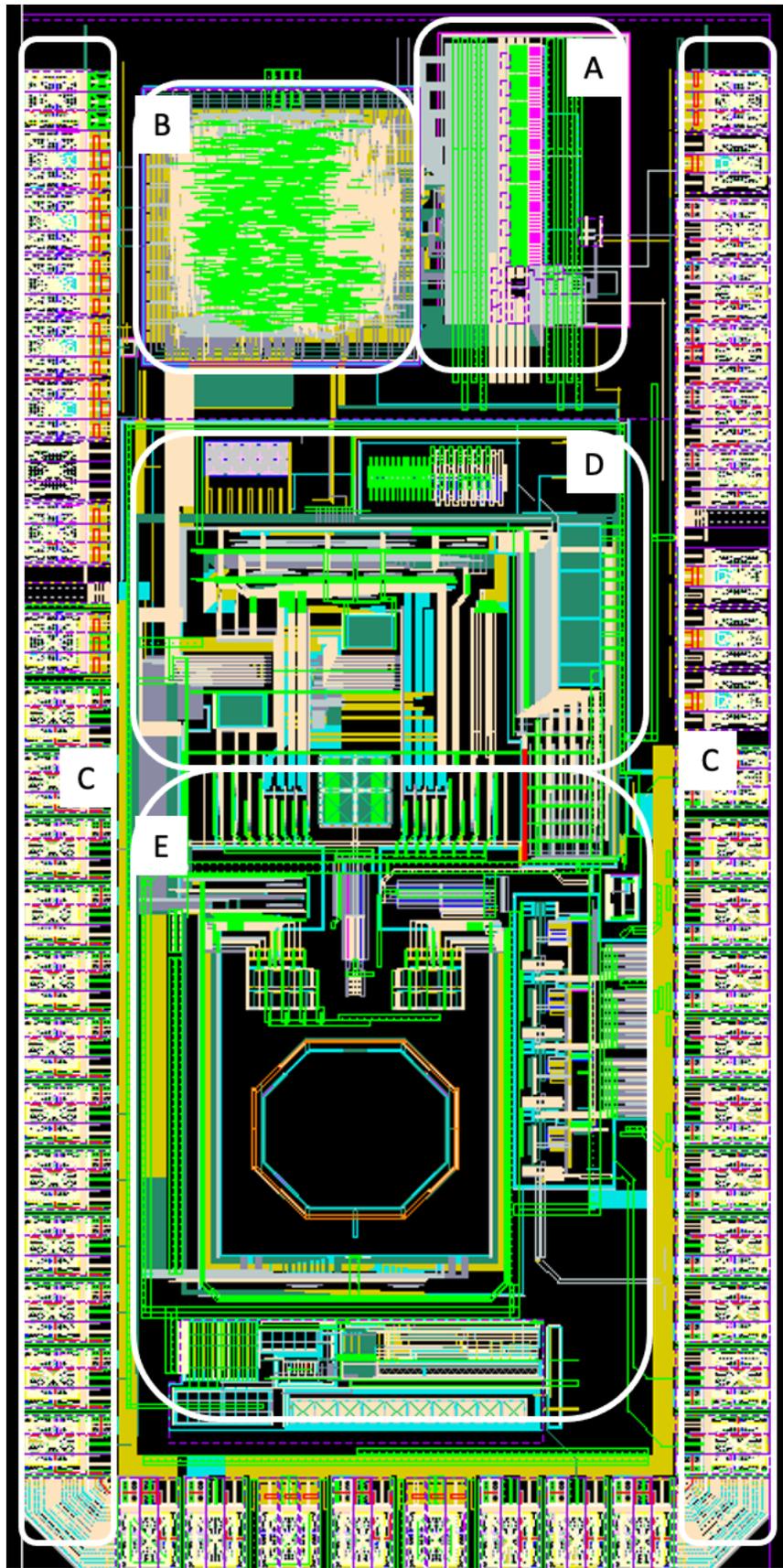


Fig. 89 chip-level layout of an ADPLL design that includes the tunable conjoined-ring Vernier TDC (A and TDC post evaluation logic part of B) (designed by Tuoxin Wang), digital loop filter and SPI interface and control (part of B)(compiled and synthesized by Krste Mitric and Yasuhide Goto, backup S2P IO control and interface (part D), digitally controlled VCO (part E) (designed by Shakeeb Abdullah).

5.4 Package and Bonding Design

The packaging and bonding descriptions for two versions of TDCs have been shown in Fig. 90, Fig. 91 and Fig. 92.

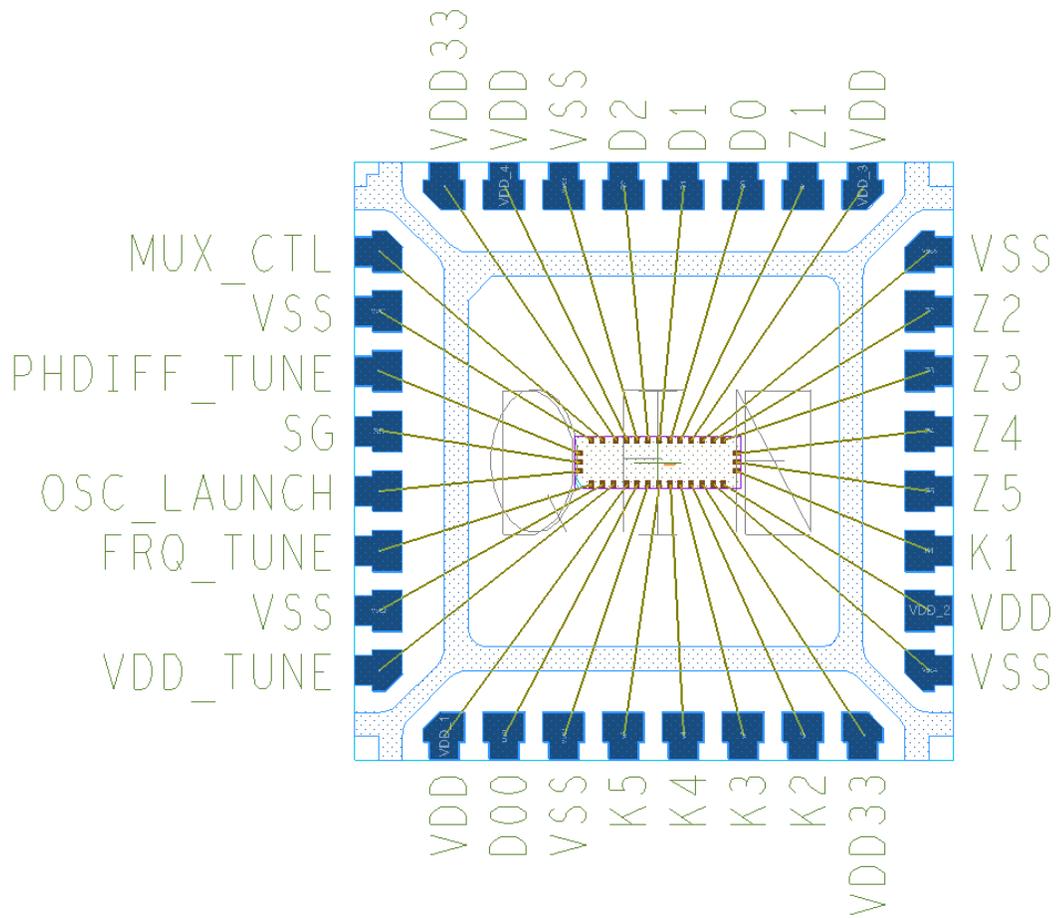


Fig. 90 Bonding and packaging design (Version I TDC in QFN-32 5X5 package)

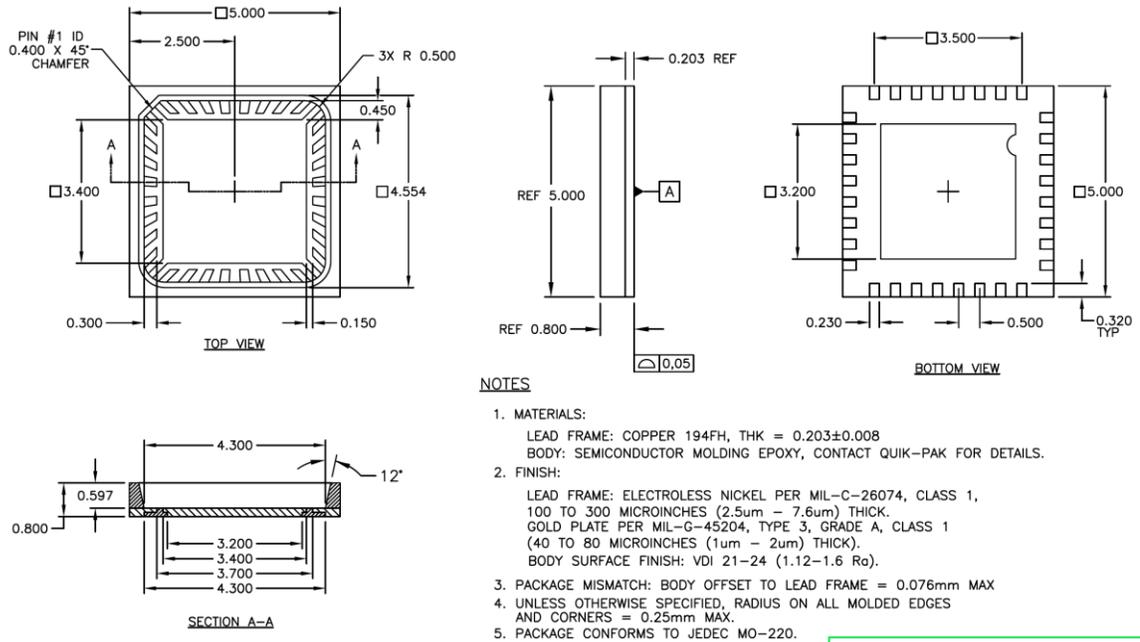


Fig. 91 QFN5X5-32 Package description

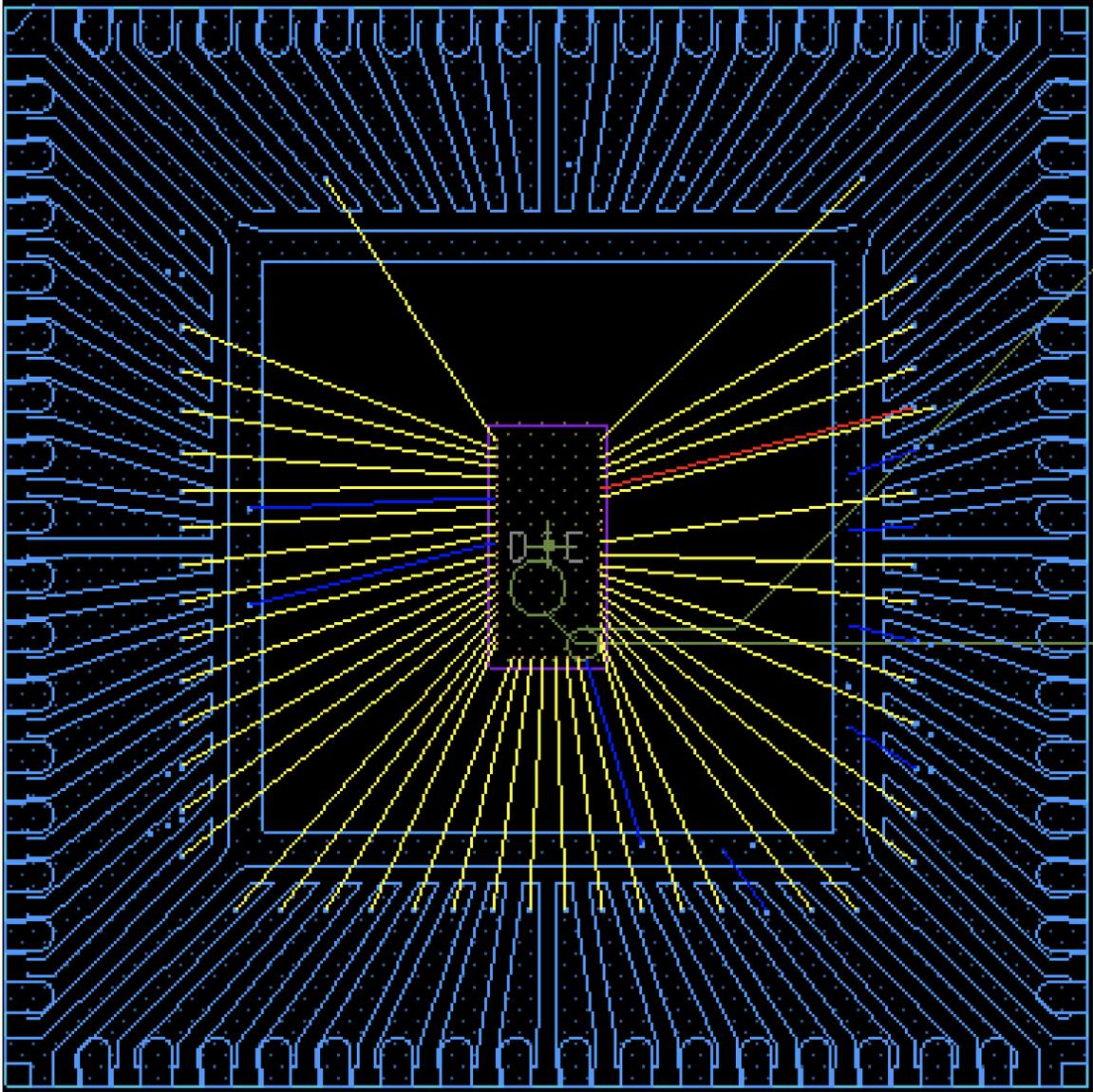


Fig. 92 Bonding and packaging design (Version II TDC in QFN-64 9X9 package)

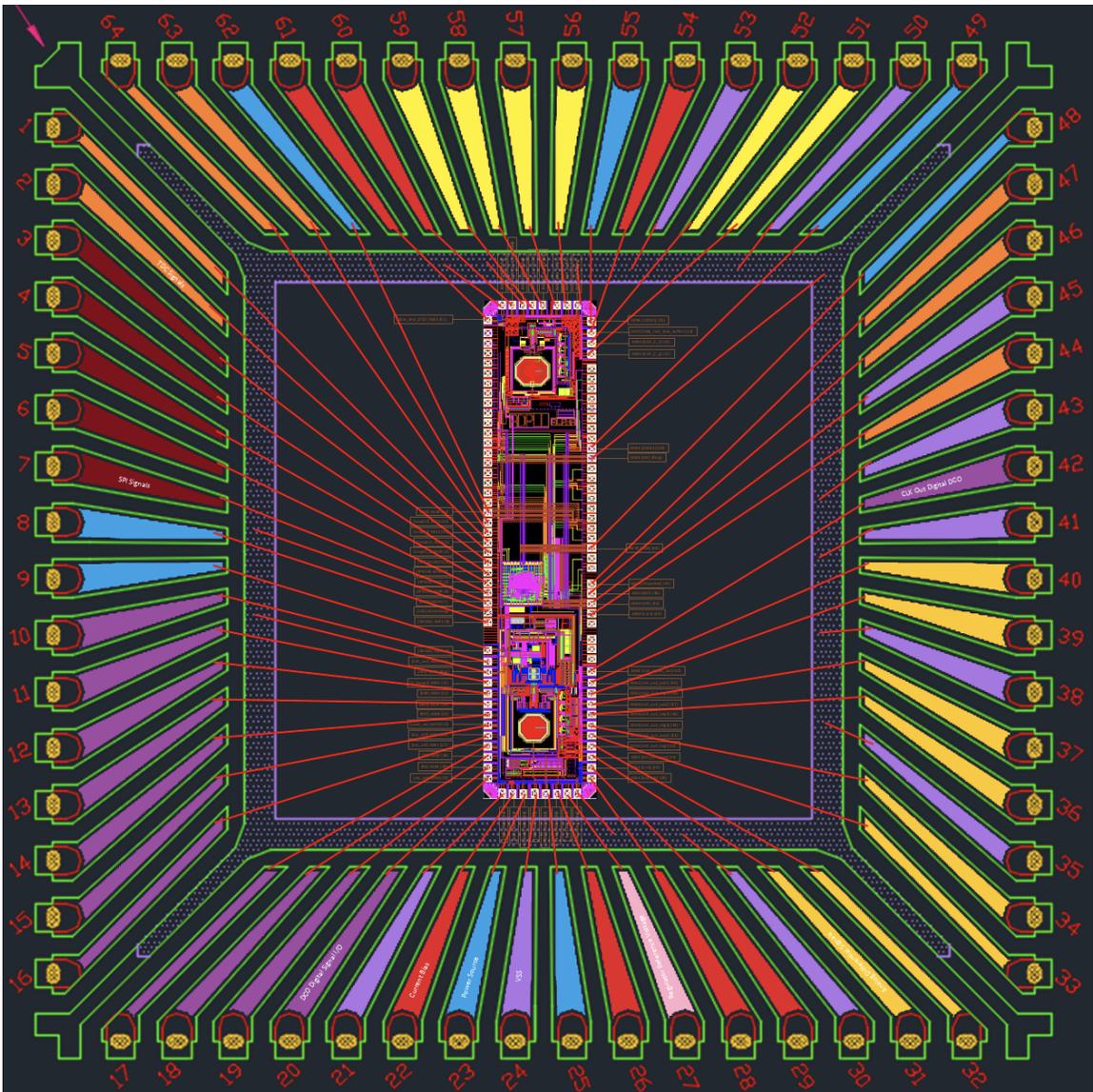


Fig. 93 Bonding and packaging design (Version II-2 TDC in QFN-64 9X9 package)

5.5 Evaluation PCB Layout Design

Fig. 94, Fig. 95 and Fig. 96 illustrate the top layer, bottom layer and power layer of the evaluation PCB layout that is used for first version TDC (32-stage conjoined-ring Vernier TDC) test and verification.

Fig. 97 and Fig. 98 are the PCB layout design (top layer and bottom layer) for the second version TDC (tunable conjoined-ring Vernier TDC) test and verification.

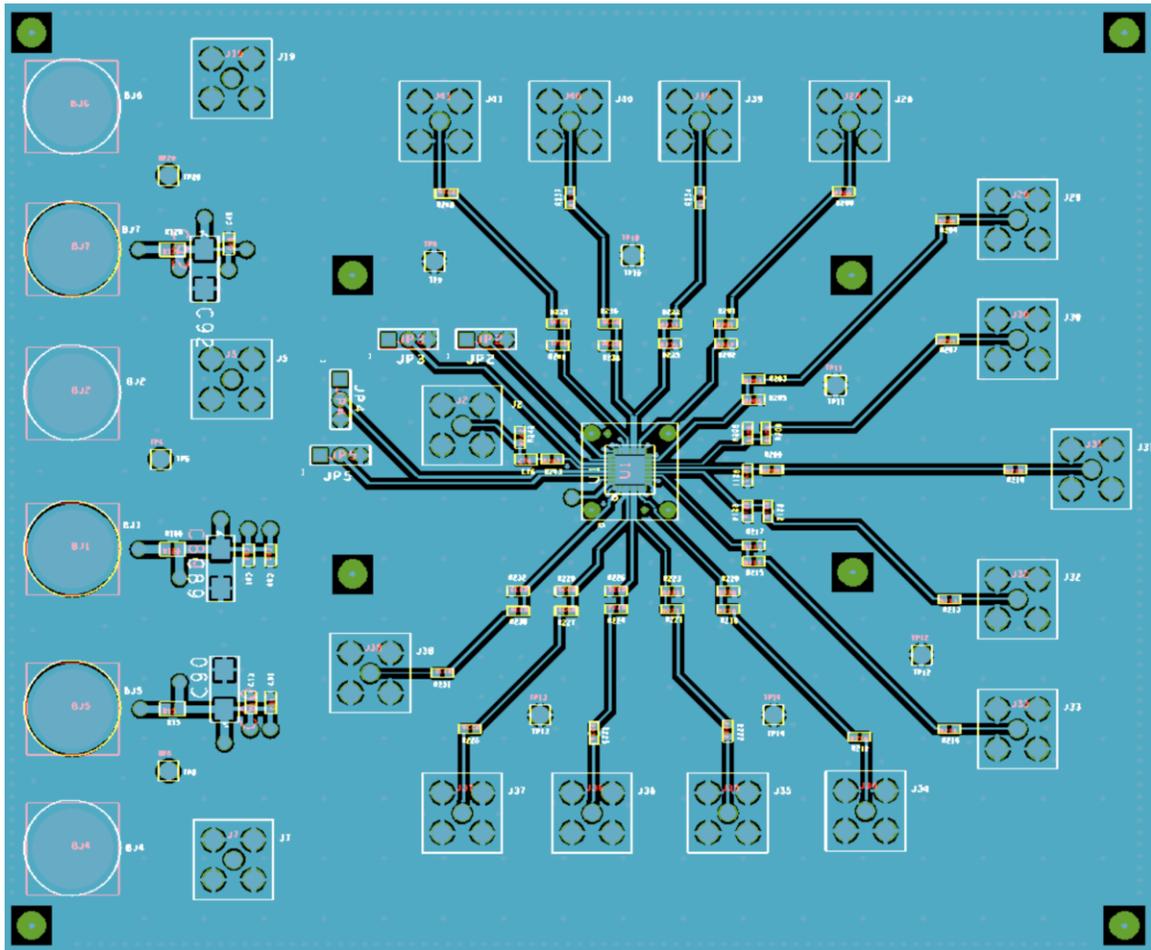


Fig. 94 Evaluation PCB layout (top layer) for Version 1 TDC verification.

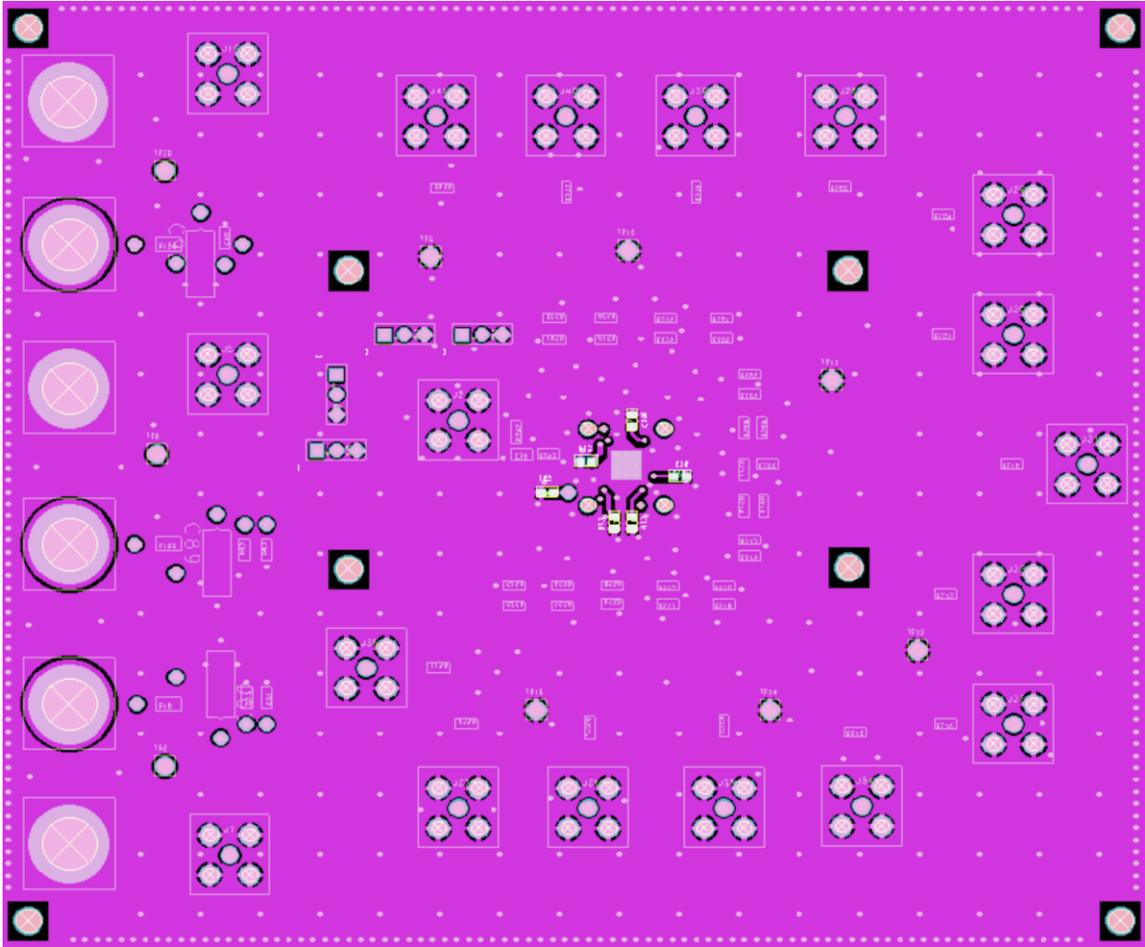


Fig. 95 Evaluation PCB layout (bottom layer) for Version 1 TDC verification.

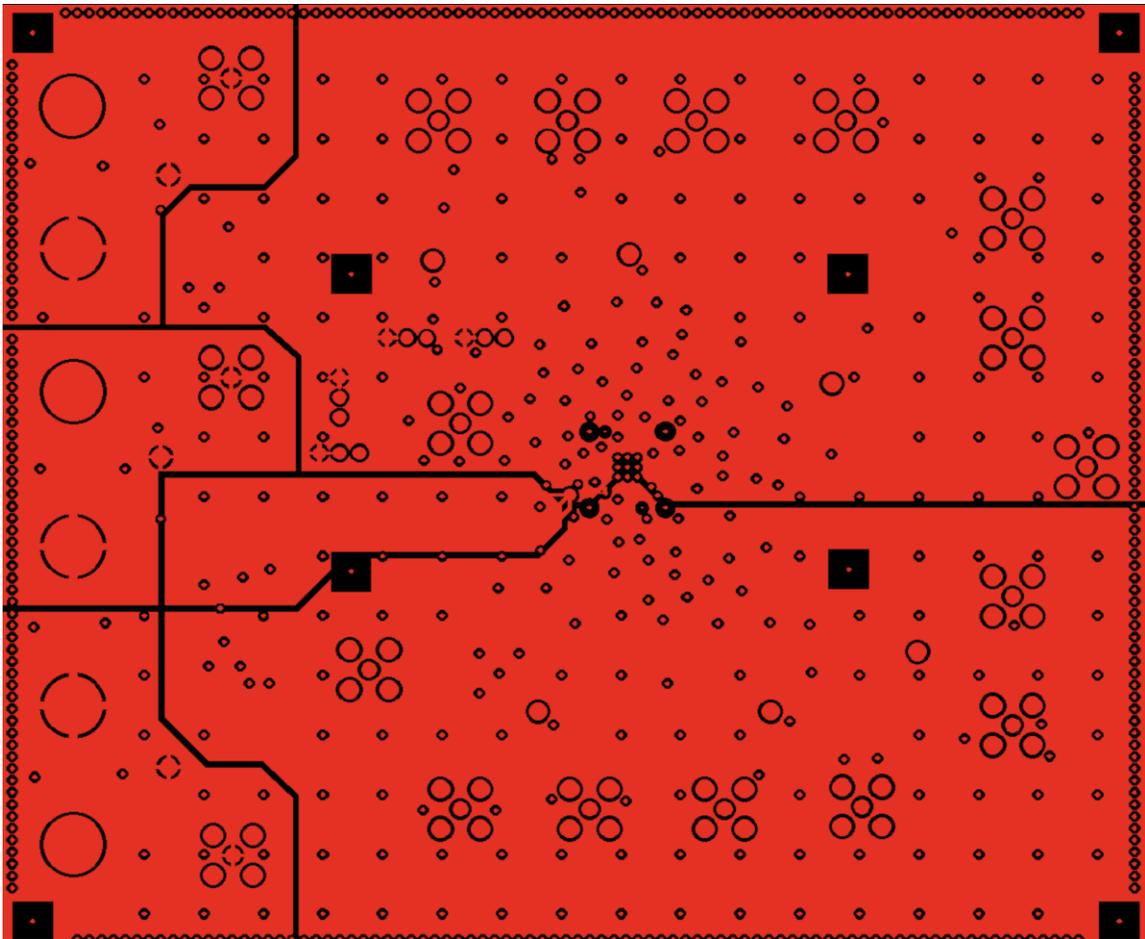


Fig. 96 Evaluation PCB layout (power layer) for Version 1 TDC verification.

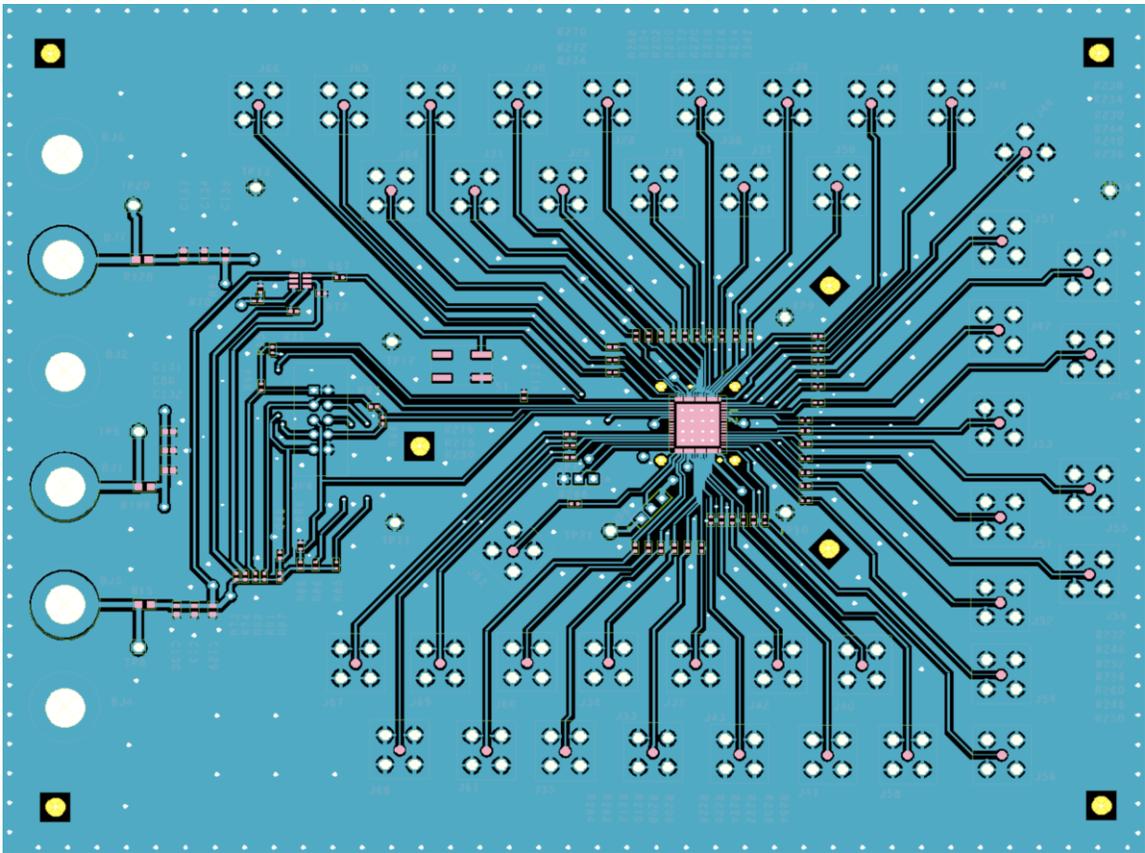


Fig. 97 Evaluation PCB layout (top layer) for Version 2 TDC verification.

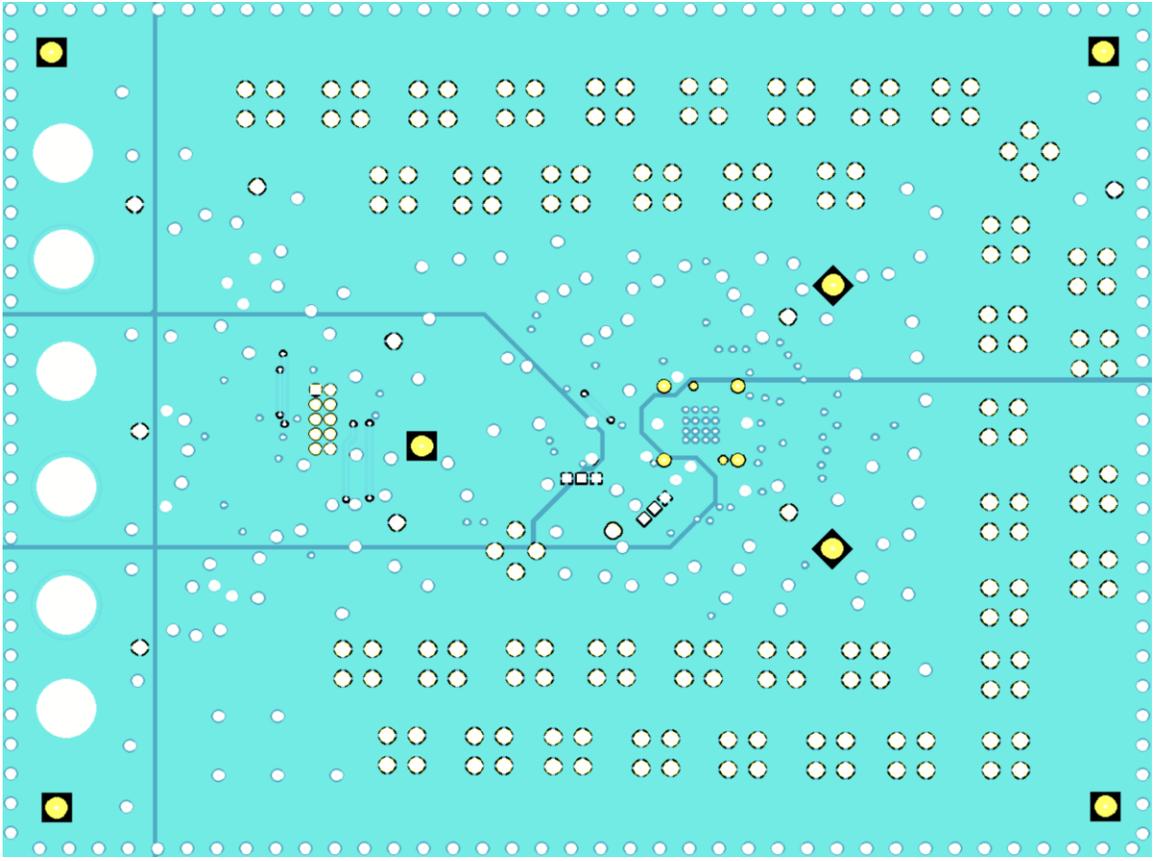


Fig. 98 Evaluation PCB layout (power layer) for Version 2 TDC verification.

Chapter 6: Fabrication and Experimental Result

This Chapter will present the bonding and packaging of the fabricated chip, and the corresponding physical evaluation board. In the second part of this chapter, the experimental results will be presented and discussed from the perspectives of the first version TDC (32-stage conjoined-ring Vernier TDC or 32-CRV TDC) and the second version TDC (tunable sub-picosecond conjoined-ring Vernier TDC or tunable sub-ps CRV TDC) respectively.

6.1 TDC and ADPLL Chip Die

The technology for the fabrication of the chip implementations is TSMC 40nm. The fabricated die photograph of the first version of the proposed TDC is shown in Fig. 77. It includes 32 pads for IO connection. The rectangular shape of the die chip is due to the limitation of the room that remain for the prototype as taping out together with product fabrication in one mask.

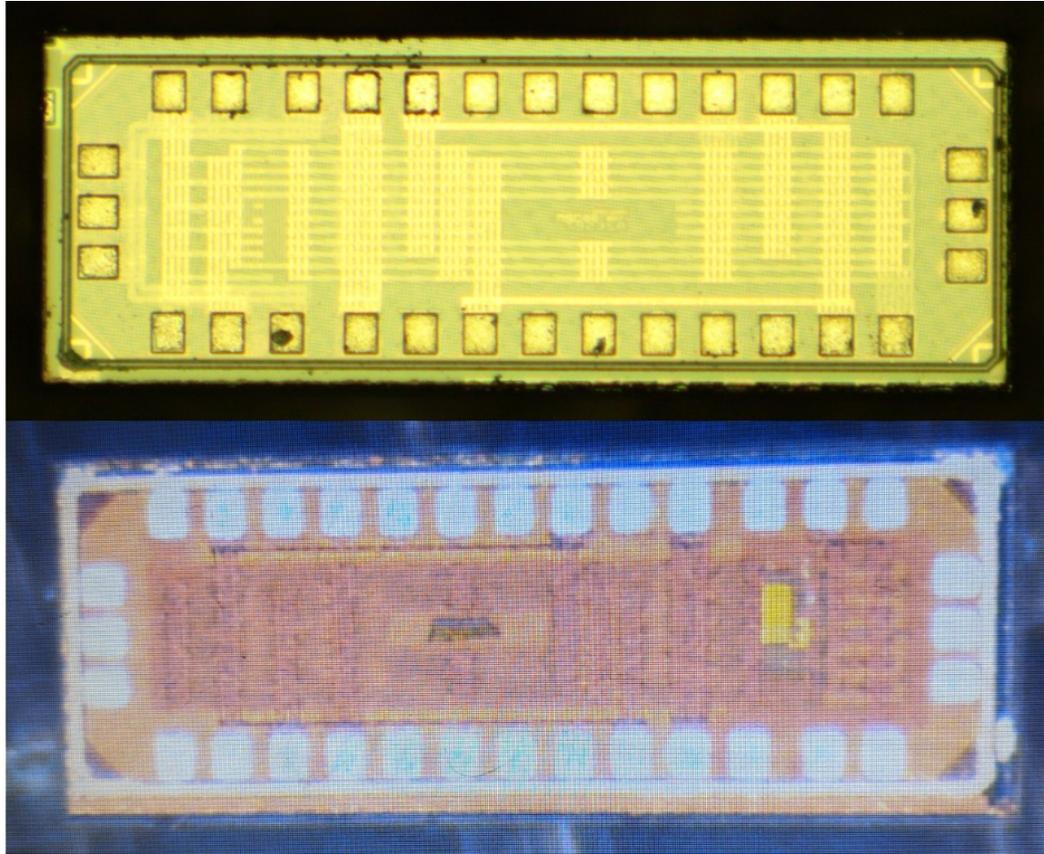


Fig. 99 Die images of the first version of the proposed TDC design.

Fig. 100 and Fig. 101 indicate the photos of the die chip and the chip samples of the second version of the proposed TDC, tunable sub-picosecond conjoined-ring Vernier TDC implementation.

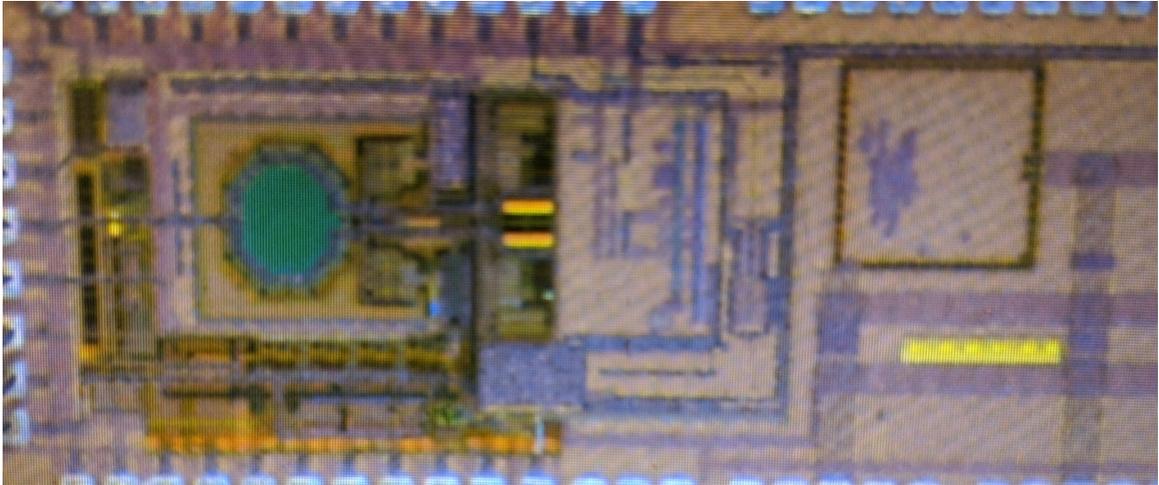


Fig. 100 Die images of the second version of the proposed TDC design.



Fig. 101 Die samples' image of the second version of the proposed tunable sub-picosecond conjoined-ring Vernier TDC design.

The packaging solution for TDC verifications has been mainly focused on minimizing parasitic impact of the chip leads that should be as short as possible. Thus, QFN type

packages have been chosen and QFN-32 5X5 and QFN-64 9X9 are used for different versions of chip design, as shown in Fig. 102.

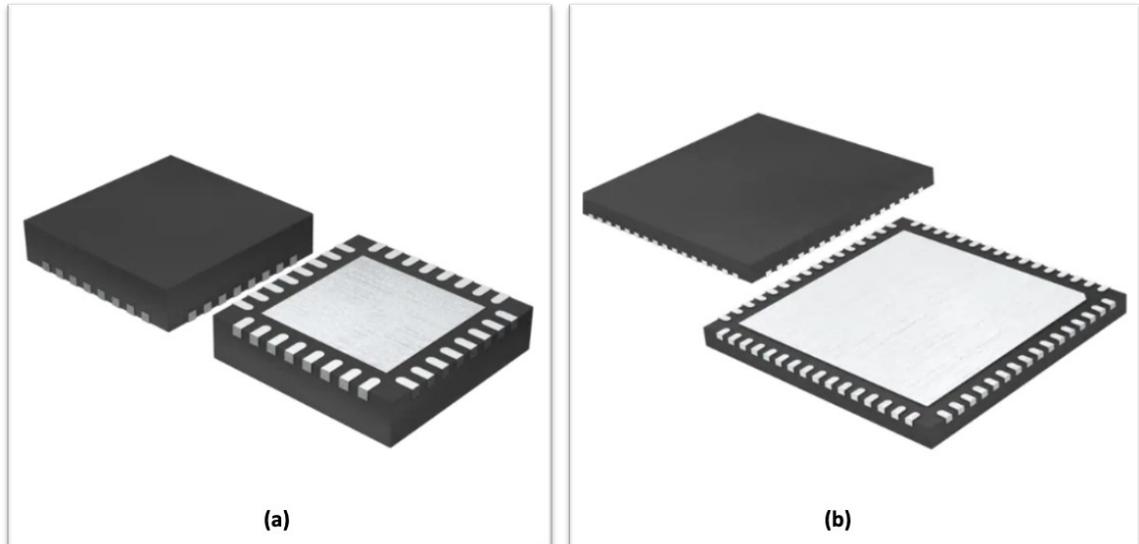


Fig. 102 Images of the TDC verification chips (packages) (a): for Version I, 32-stage conjoined-ring Vernier TDC; (b): for Version II, tunable sub-picosecond conjoined-ring Vernier TDC.

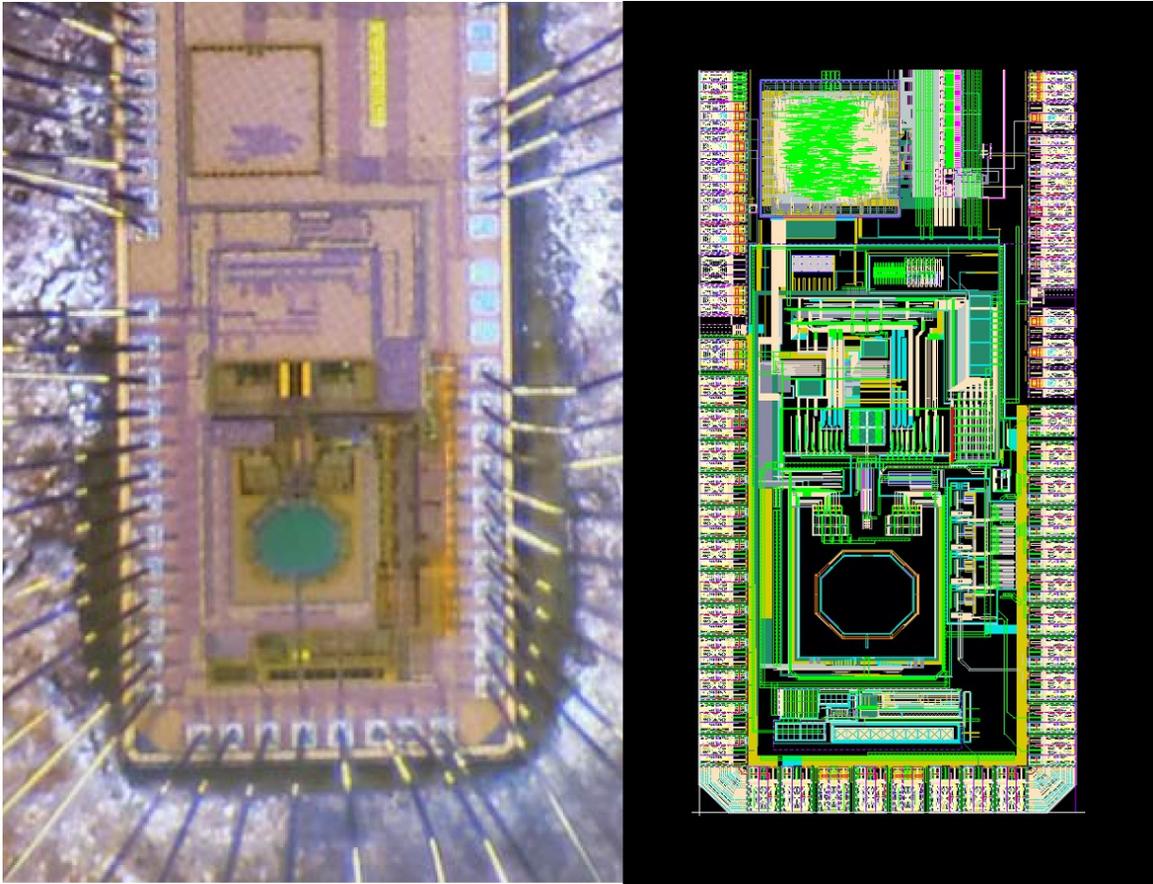


Fig. 103 Images of second version TDC (all-digital PLL system chip) die with bonding wire and the corresponding layout design as comparison.

6.2 Evaluation PCB and Test Bench

The image of the evaluation PCB for 32-stage conjoined-ring Vernier TDC chip verification is shown in Fig. 104. SMA connectors are used for feeding input reference signal and for testing output signals. Fig. 105 shows the image of the evaluation board for tunable sub-picosecond conjoined-ring Vernier TDC. Note that the outputs of the signal can be captured from either SMA connectors or SPI interface. Fig. 106 shows the PCB for DCO and ADPLL chip testing.

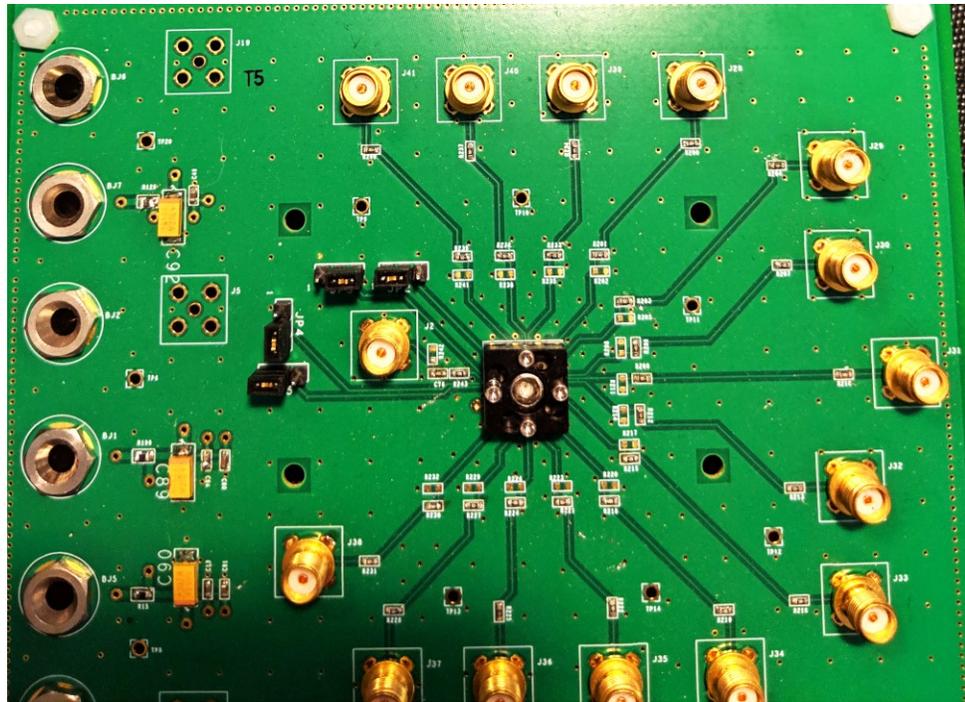


Fig. 104 Images of the evaluation board for the first version TDC verification.

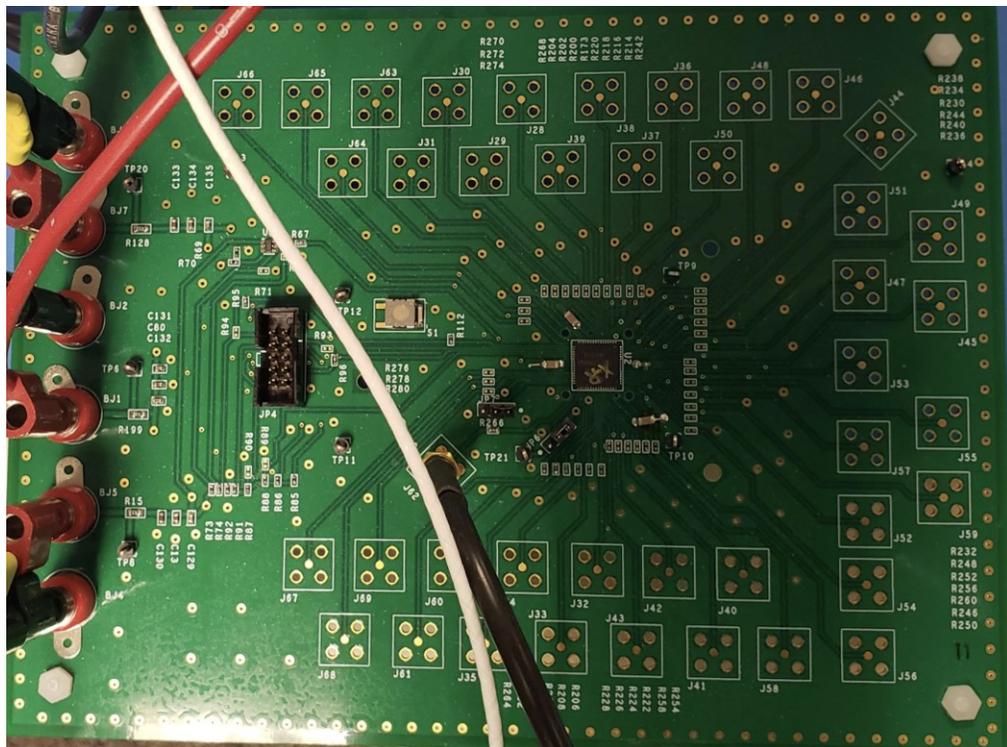


Fig. 105 Images of the evaluation board for the second version TDC verification.

include signal generators, oscilloscope, power supplies, spectrum analyzer, frequency meters and multi-meters. The illustration of the test environment has been shown in Fig. 107 and Fig. 108

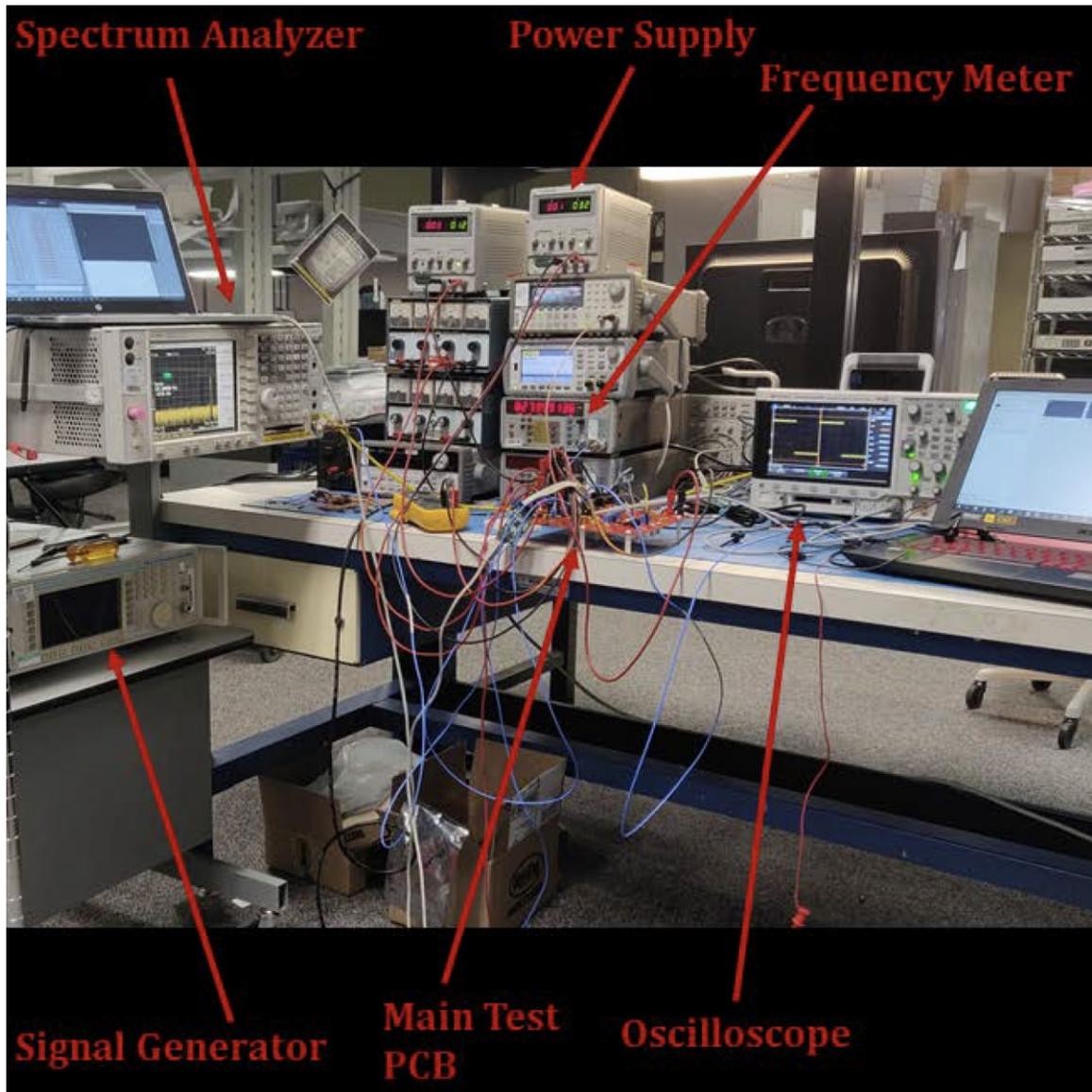


Fig. 107 Photo of the test bench for test and verification.

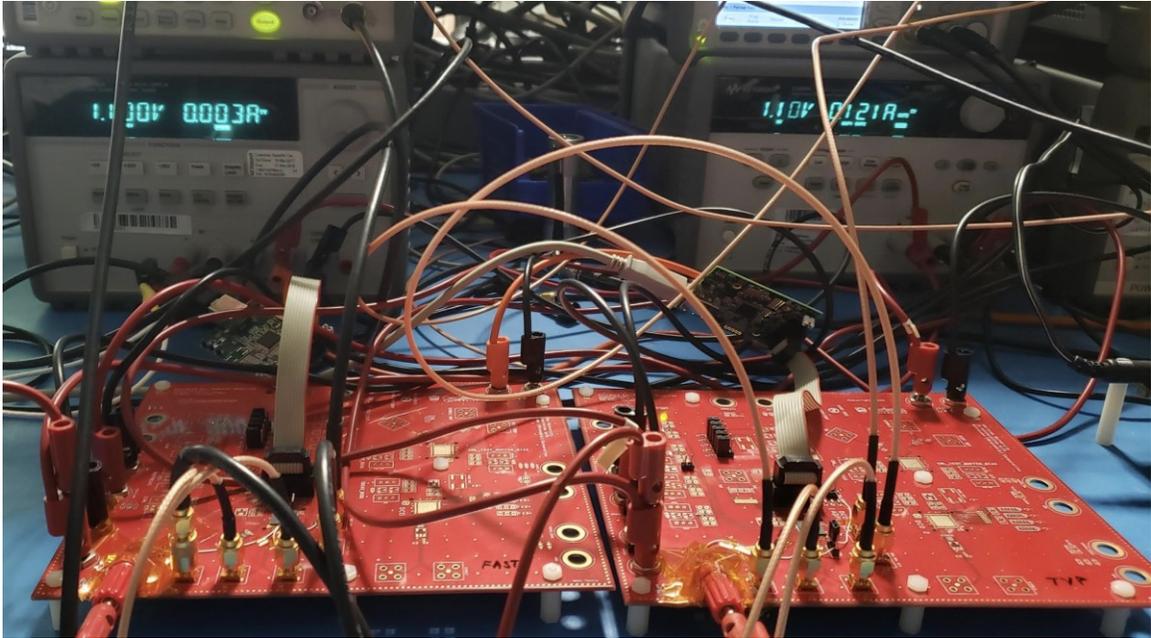


Fig. 108 Photo of the evaluation board for the ADPLL verification.

6.3 32-Stage Conjoined-Ring Vernier TDC Experimental Result

The first version chipset (32-stage conjoined-ring Vernier TDC) circuit operates at 1.0V power supply with 25MS/s of conversion rate (reference frequency). The output IOs are buffered up to 3.3v for measurement. The core circuit of the evaluating TDC circuit occupies less than 0.15mm*0.15mm in area in the die and typically consumes 0.3mW of the power.

Fig. 109 shows the measured transfer characteristic of the TDC final quantization output changing with the input time interval. The measurement indicates a stable 3ps of an effective time resolution performance in a 32-stage CRV TDC version. The available measurement range in the test bench is from 40ps to 1.3ns. Note that the capability of the detection range of the TDC chip is flexible and limited by the loop counter bit width. However, due to the test bench limitation and the practical requirement of the system, 1ns

of the detection range is sufficiently required for the application with DCO frequency of 100MHz and above.

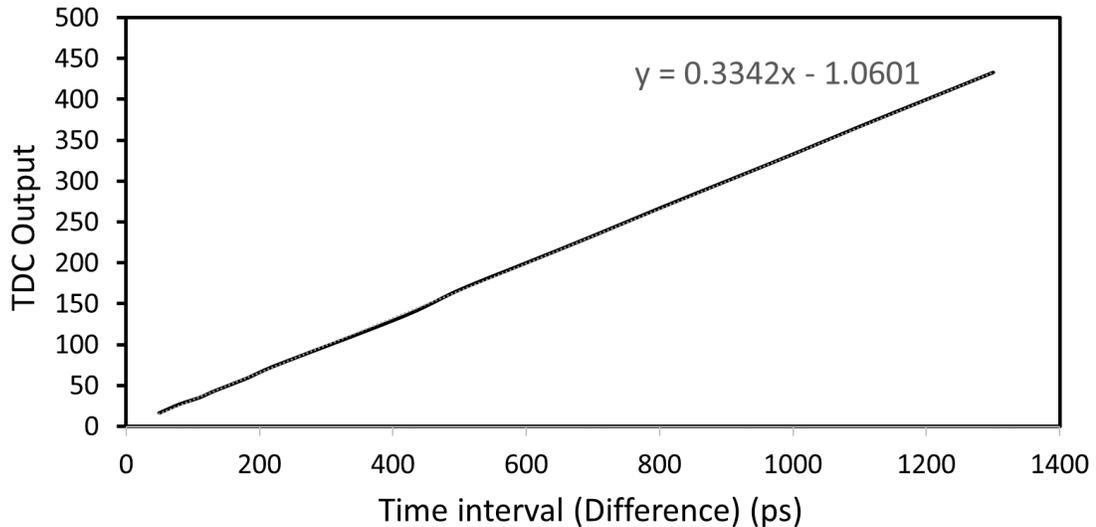


Fig. 109 32-Stage Conjoined-ring Vernier TDC transfer function measurement with POM correction.

Fig. 110 represents the contrast of the CRV TDC output measurements between performing and without performing POM correction as the time interval increase. It turns out without the POM correction, the TDC output suffers a $2N$ of quantitative error when it locates in the POM region (that has less than 5ps of POM width typically). As shown in Fig. 111, more than 20dB PSD performance improvement has been achieved by employing POM error correction implementation compared to that without POM correction circuit. Note that large POM width is intentionally chosen in the design in order to ensure an only prior-POM scenario to be the case in the PVT variations, so that the scheme of POM correction could be much simpler than that with a short POM width design in which POM errors would toggle between the prior-POM and the lag-POM scenario (being complicated to be corrected).

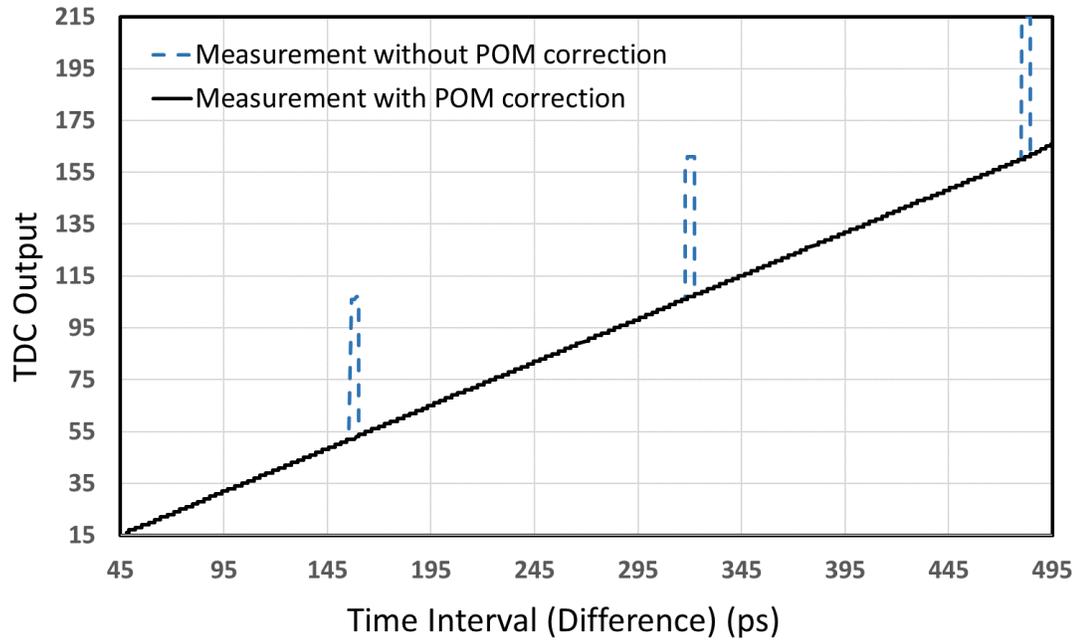


Fig. 110 32-Stage Conjoined-ring Vernier TDC output measurements (with/without POM correction).

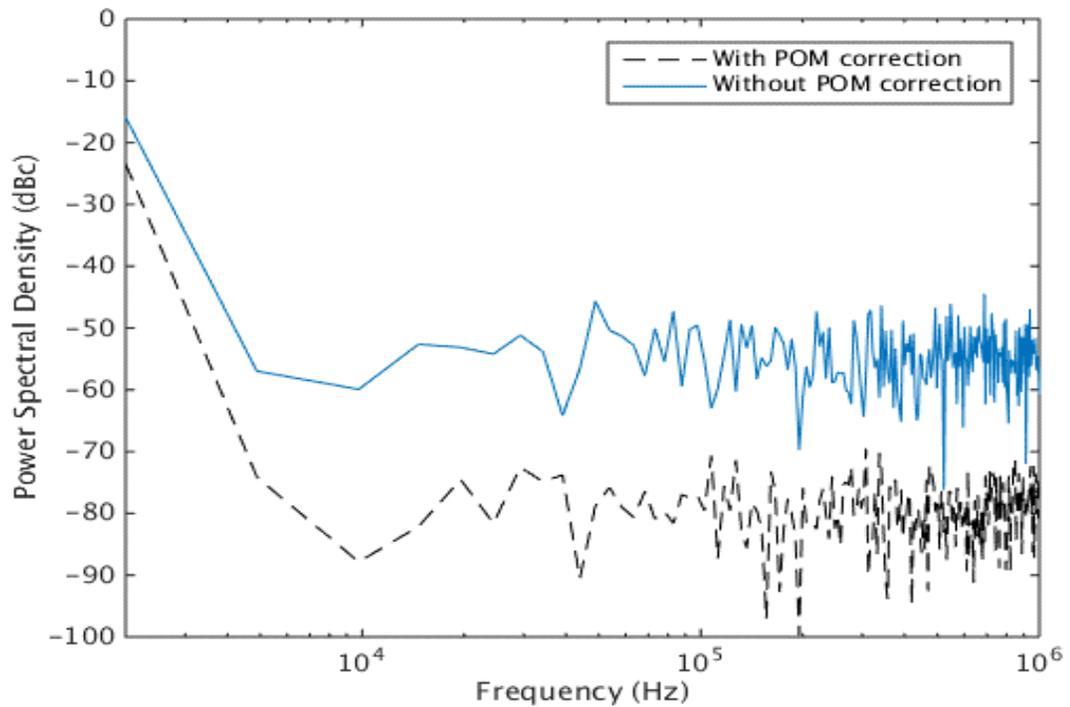


Fig. 111 32-Stage Conjoined-ring Vernier TDC output measurements in power spectral density (with/without POM correction).

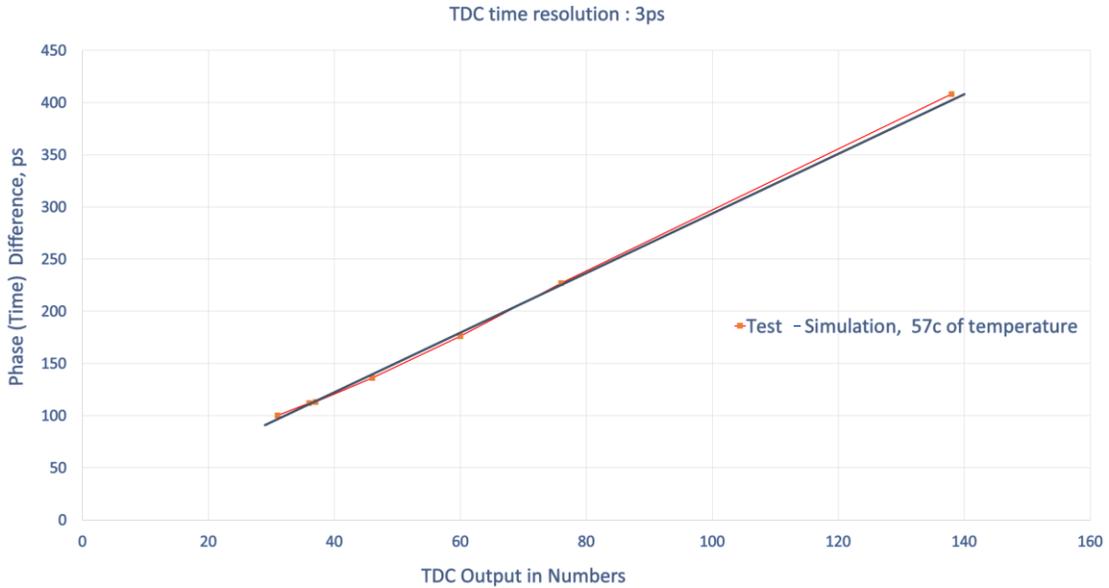


Fig. 112 32-Stage Conjoined-ring Vernier TDC output comparisons between simulation and measurement results (with POM correction and N-calibration scheme).

Fig. 112 shows the comparison between simulation result and the measurement result of the TDC transfer characteristic, showing consistency with each other.

Fig. 113 represents the comparison of the CRV TDC measurements between with and without performing N-calibration scheme as the time interval increase. Without the N-calibration design (curves in yellow color), the practical result of the TDC output would gradually deviate from the expected one as time interval (input) increases. Black curve shows that the N-calibration operation ensure the practical output will not deviate its expectation.

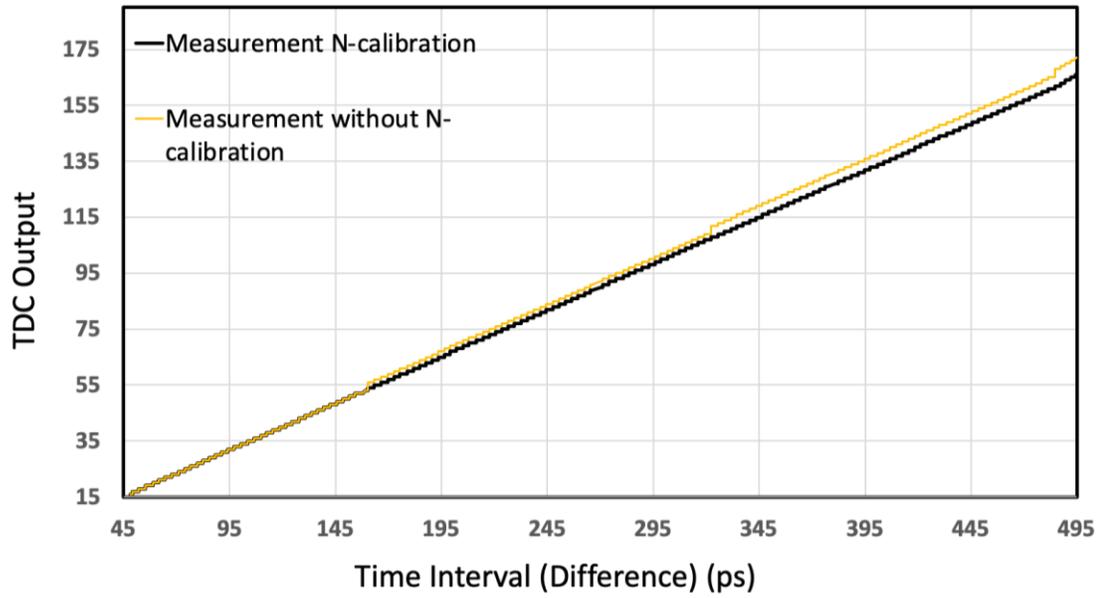


Fig. 113 32-Stage Conjoined-ring Vernier TDC output comparisons between with/without N-calibration.

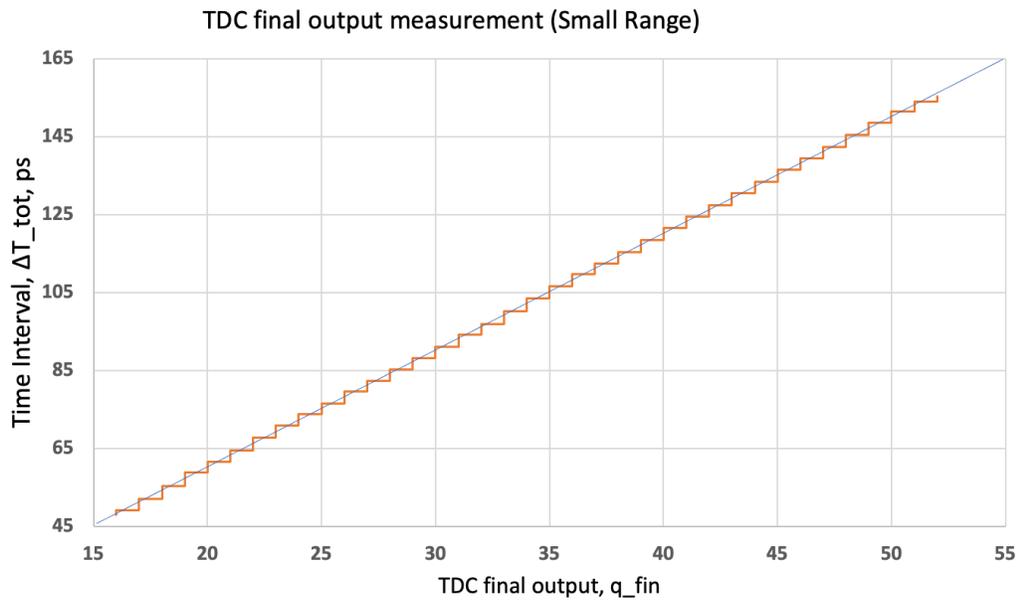


Fig. 114 32-Stage Conjoined-ring Vernier TDC linearity results (small range).

Fig. 114 shows the detail curve of the transfer characteristic in a small range and Fig.

115 represents the differential non-linearity (DNL) of less than 0.2 LSB and integral non-linearity (INL) of less than 0.7 LSB of the 32-stage CRV TDC over the range. The experimental results have been collected in an average of 10000 samples.

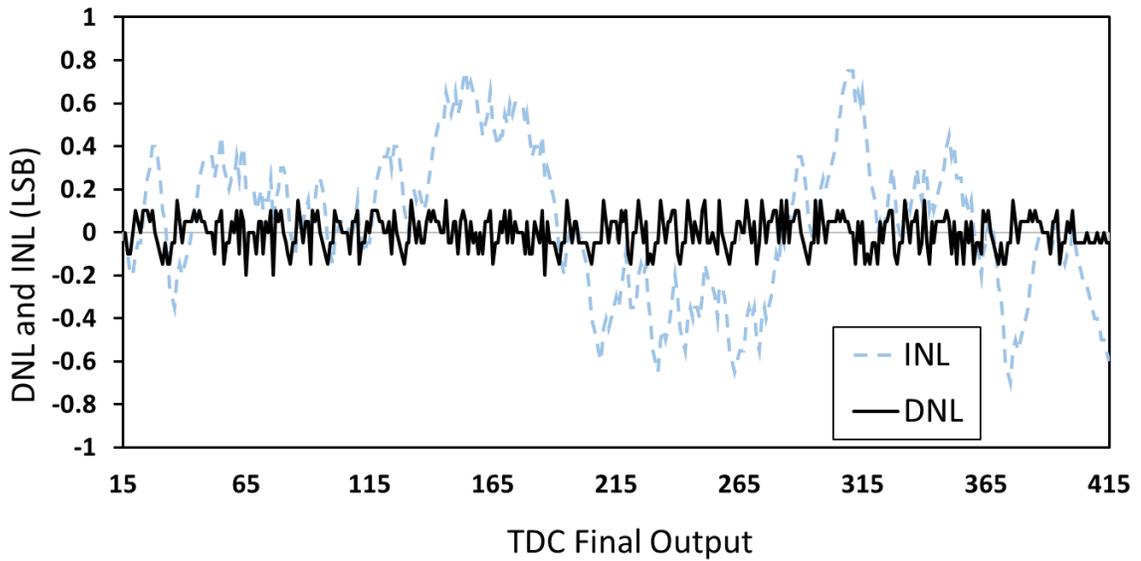


Fig. 115 32-Stage Conjoined-ring Vernier TDC linearity results.

One-shot precision histogram measurements of the CRV TDC outputs at the value of 200 and 400 have been given in Fig. 116, showing the concentration of the distribution of the output samples. and their PSD characteristics have been plotted in Fig. 117.

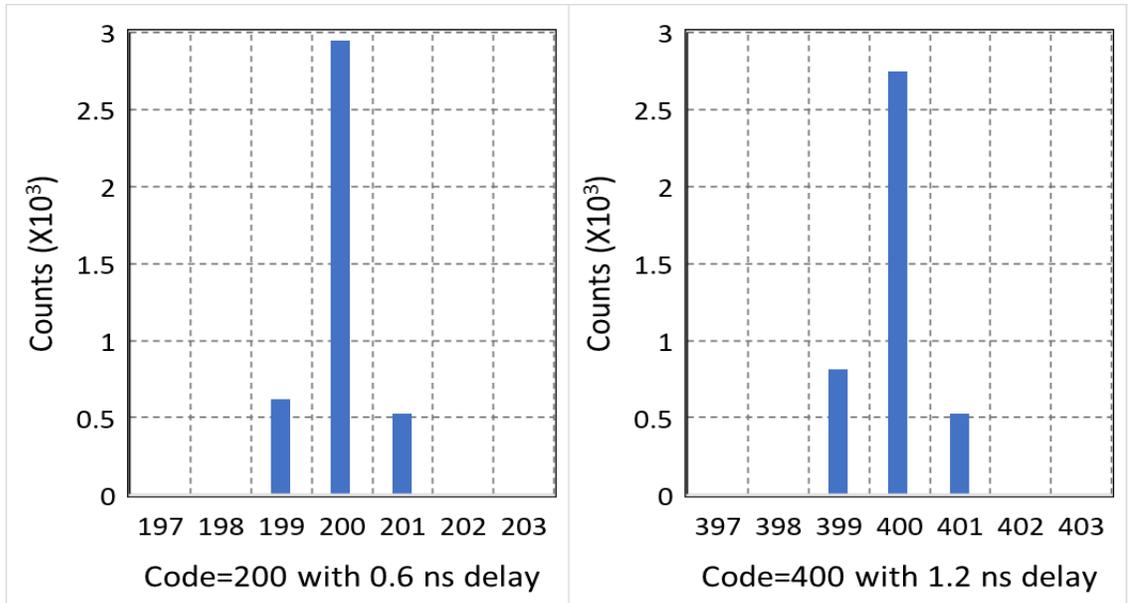


Fig. 116 Single-shot precision measurement of the TDC output code @200 and @ 400

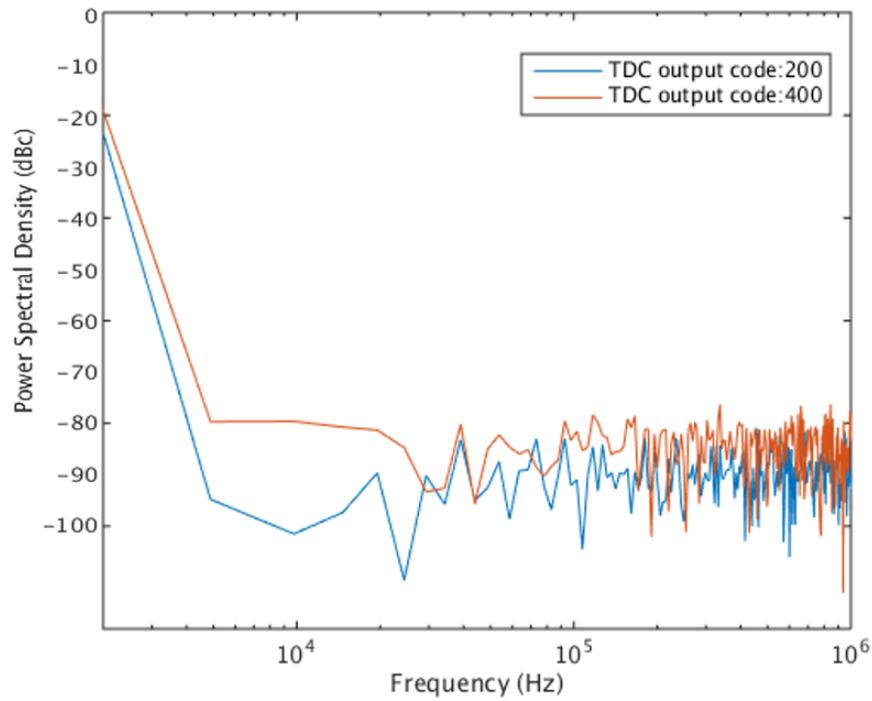


Fig. 117 PSD of the single-shot precision measurement of the TDC output code @200

and @ 400

6.4 Tunable Sub-picosecond Conjoined-Ring Vernier TDC Experimental Result

The second version chipset (tunable sub-picosecond conjoined-ring Vernier TDC) circuit operates at 1.0V power supply with 25MS/s of conversion rate (reference frequency). The output IOs are buffered up to 3.3v for measurement. The core circuit of the evaluating TDC circuit occupies less than 0.4mm*0.4mm in area in the die and typically consumes 1.2mW of the power.

Fig. 118 shows a series of the TDC measurement that indicates the transfer function with various time resolutions ranging from 0.75ps to 1.1ps. As shown in the figure the linearity of the lines behaves well in the overall range.

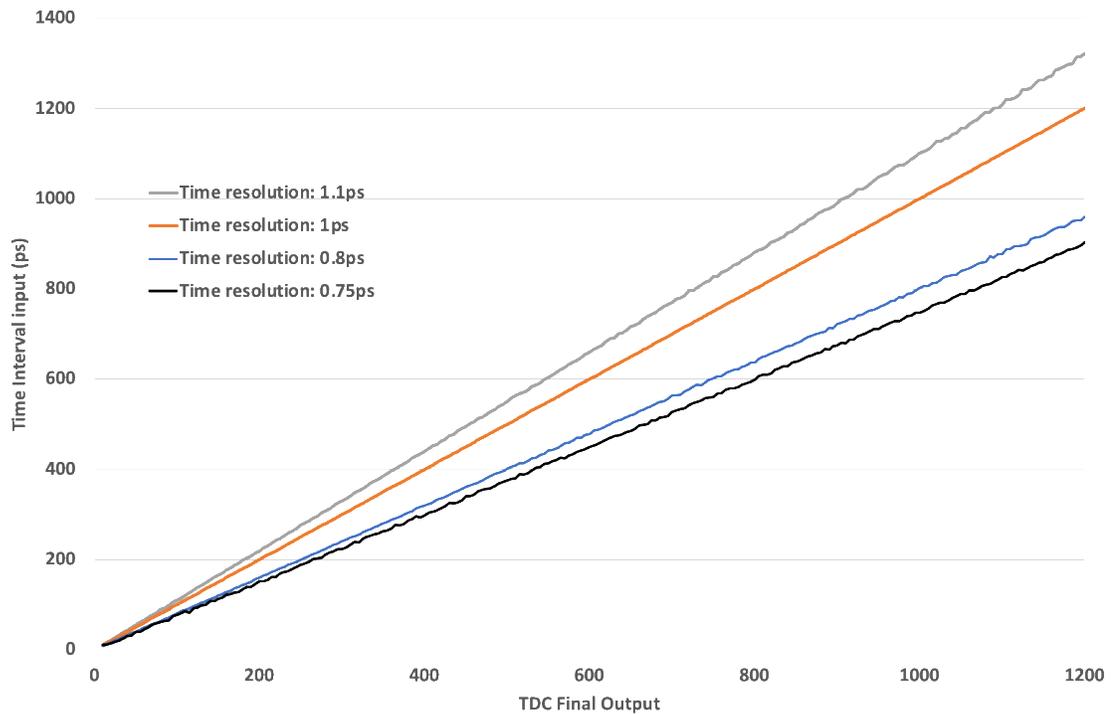


Fig. 118 Tunable sub-picosecond Conjoined-ring Vernier TDC transfer function measurement result (large range).

However, if we zoom into a relatively small range like shown in Fig. 119, it could be realized that the more volatility of the TDC transfer characteristics has been detected from some curves. This unexpected fluctuation behavior of the linear curve becomes explicit when time resolution being configured below 0.8ps. And the reason of this is mostly due to instability of the transition activity (edge rate) of the CMOS transistors in the core circuit tends to weight more compare to the value of the time resolution configured. A further nonlinear curve of the transfer function has been detected with the time resolution configuration of 0.7ps, which is unacceptable for the TDC's operation.

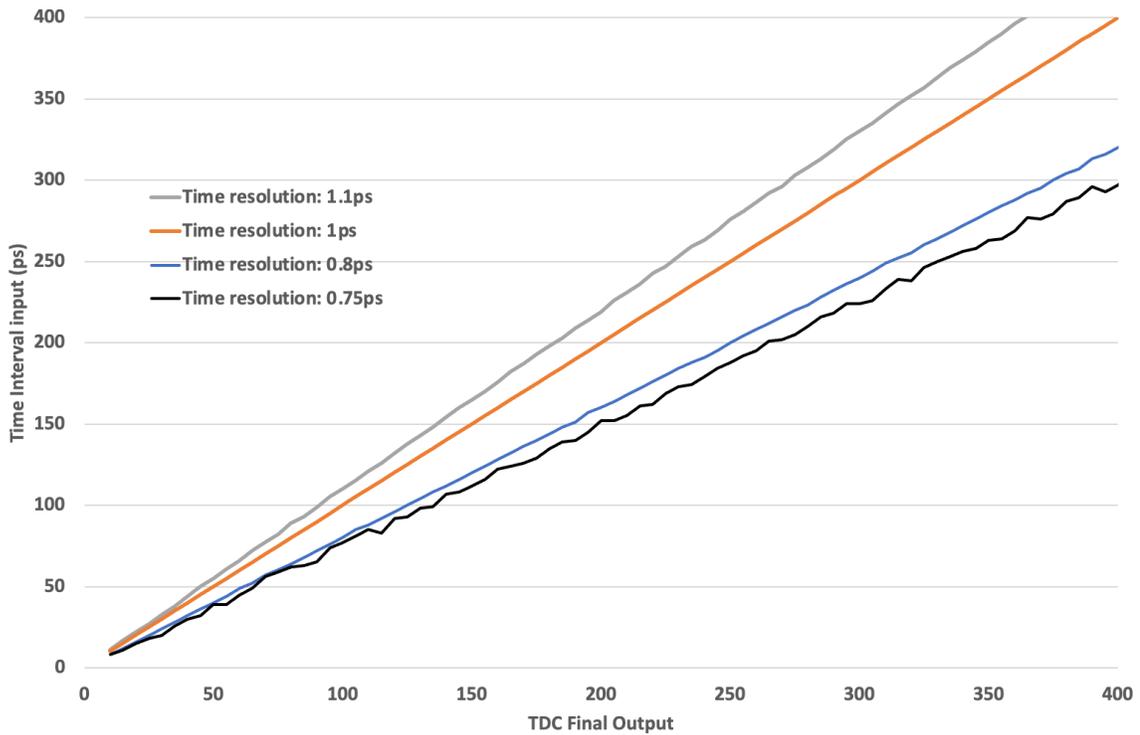


Fig. 119 Tunable sub-picosecond Conjoined-ring Vernier TDC transfer function measurement result (zoom into a small range).

Fig. 120 represents the measurements comparison of two versions of the proposed TDC designs in terms of the power spectral density contribution. The 0.8ps time resolution design contributes less noise power density by around 10dB compared to that (3ps) of the first version TDC. It means that the second version of the proposed TDC could improve the phase noise performance of the all-digital PLL at least by 10dB compared to that employed the first version of the proposed TDC.

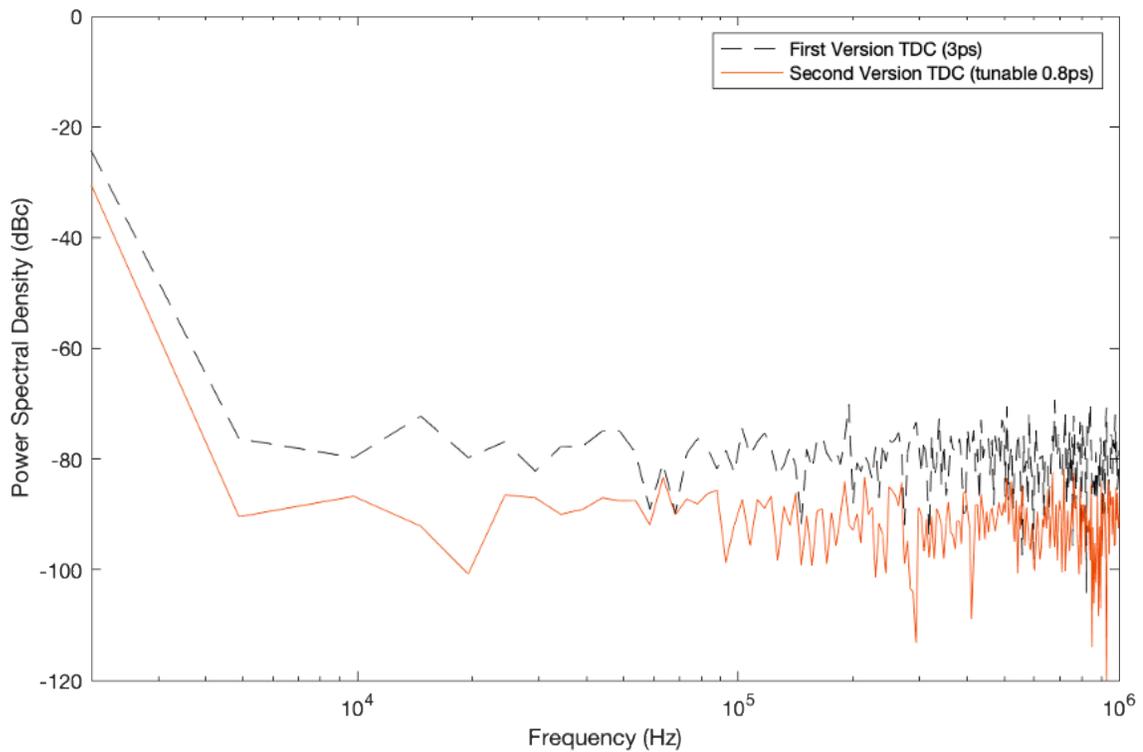


Fig. 120 Tunable sub-picosecond Conjoined-ring Vernier TDC output comparisons in power spectral density between simulation and measurement results.

Fig. 121 shows the time resolution response to different control code with various voltage supply values. Fig. 122 shows the time resolution response to different control code with various environment temperature. It could be realized that the time resolution would shift as the voltage and/or temperature vary. As in a traditional solution to address this shift

issue, a calibration table could be used to provide corresponding configurations according to different voltage and temperature situations. Owing to the configurable digital control capability of the time resolution parameters, there is an alternative to the calibration table which is to compensate the offset over PVT variations by tuning the time resolution configuration. By combining tunable function with the N-calibration scheme realization the TDC quantization and corresponding loop operation of the ADPLL system would operate precisely without any phase noise degradation.

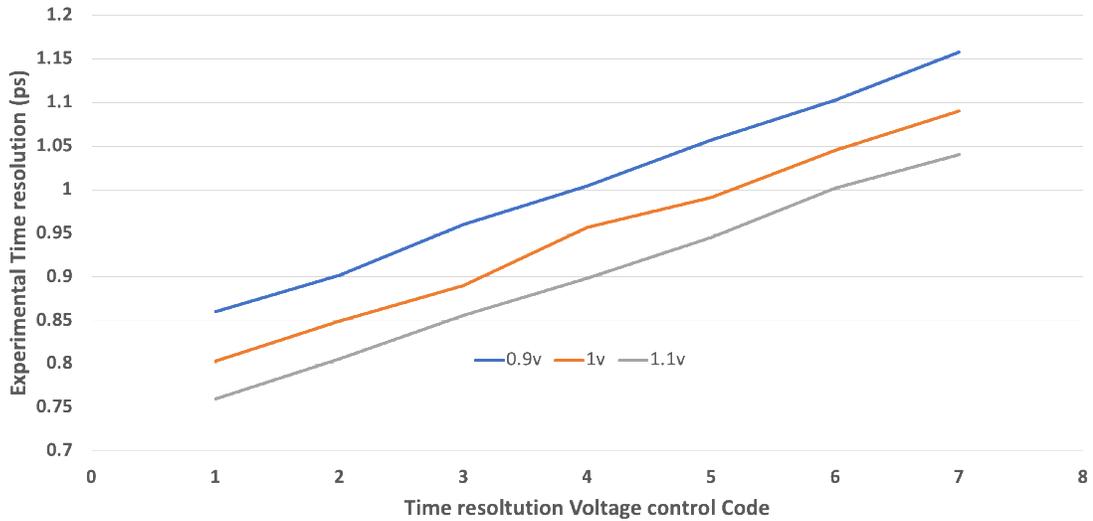


Fig. 121 Tunable sub-picosecond Conjoined-ring Vernier TDC time resolution comparisons with voltage variation (at room temperature).

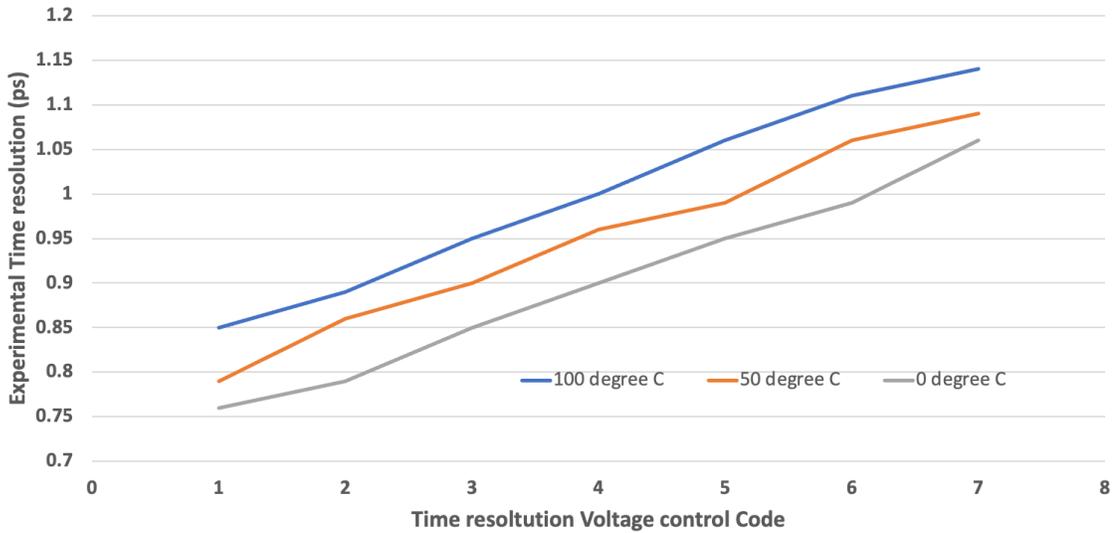


Fig. 122 Tunable sub-picosecond Conjoined-ring Vernier TDC time resolution comparisons with temperature variation (1v of power supply).

One-shot precision histogram measurements of the second version proposed TDC outputs at the value of 200 have been given in Fig. 123 and Fig. 124 respectively showing 0.9ps and 0.75 ps of the time resolution configurations. It turns out, at 0.9ps of the time resolution configuration, the concentration of the samples distribution basically conforms to a normal distribution, while at 0.75ps of the configuration, the distribution of the samples trends to depart from a normal distribution. This result is similar to the conclusion got in above transfer function figure (Fig. 119), which is the observations distribute more divergently at time resolution configuration below 0.8ps, compared to that with time resolution configuration above 0.8ps. Therefore, the TDC should operate with the time resolution not smaller than 0.8ps to avoid additional noise injection caused by degraded distribution. Experimentally, the operation of the second version of the proposed TDC with 0.7ps and below might not be accepted. Table 6 illustrates the overall performances of the proposed TDCs implementations in contrast to that of the published TDC works.

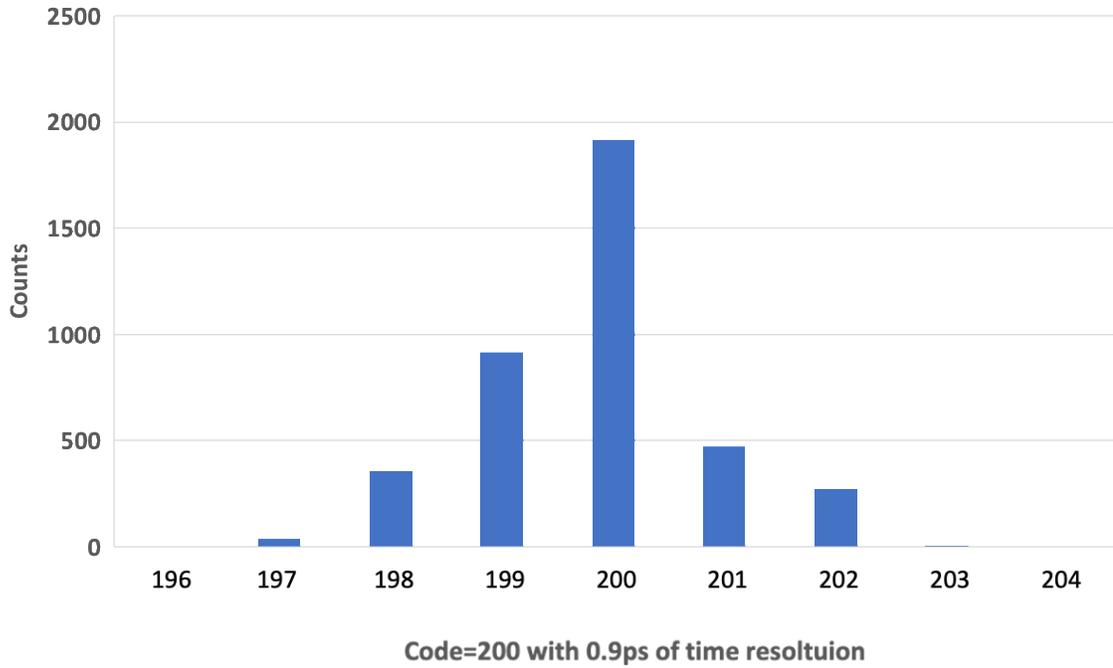


Fig. 123 Single-shot precision measurement of the tunable sub-picosecond conjoined-ring Vernier TDC output code @200 and @ 0.9ps of time resolution.

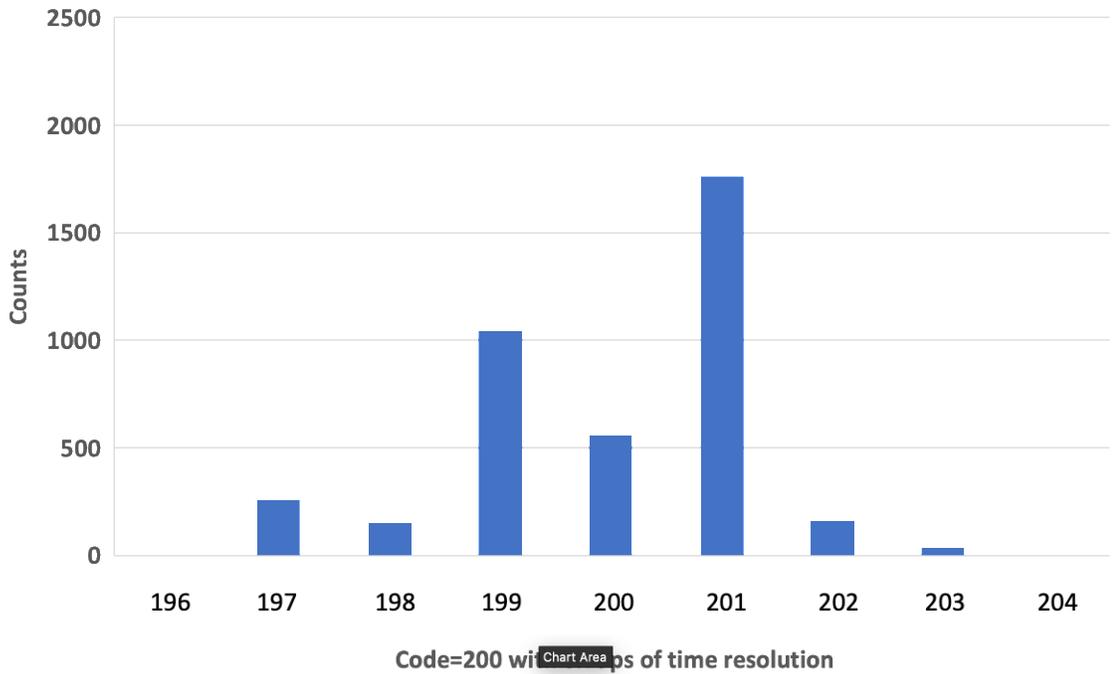


Fig. 124 Single-shot precision measurement of the tunable sub-picosecond conjoined-ring Vernier TDC output code @200 and @ 0.75ps of time resolution.

6.5 TDC Performance Comparison with State-of-the-art

An overall comparison of the TDC implementations to the published study has been illustrated in Table 6.

TABLE 6 TDC PERFORMANCE COMPARISON WITH STATE-OF-THE-ART

	[34] JSSC'10	[35] JSSC'10	[36]JSSC'18	[54]TCAS-II'16	[29] JSSC'12	[50]JSSC'17	This work
Technology	Vernier Ring	2-D Vernier No-Ring	2-D Vernier No-Ring	2-D Ver GRO 2-Ring	Vernier GRO 2-Ring	2-D Ver Ring 1-ring	CRV-TDC 1-ring
Process [nm]	130	65	45	90	90	130	40
Stage Number	30	11/19	13/16	3/3	9/9	13/16	32/128***
Num of Rings	2	0	0	2	2	1	1
Sampling Rate [MHz]	15	50	80	50	25~100	10	25
Resolution [ps]	8	4.8	1.25	2.2	3.2	1.0	3/0.8****
DNL [LSB/PS]	-	0.9/4.32	0.25/0.31	-	-	0.41/0.41	0.2/0.6
INL [LSB/PS]	-	3.3/15.8	0.34/0.4	-**	-**	0.79/0.79	0.7/2.1
Number of Bits	12	7	8	-	-	14	12****
Range [ns]	-	0.6*	0.32*	20	40	1.6	12 (1.3****)
Power [mW]	7.5	1.7	0.07-0.69	2.3	3.6/4.5	2.4	0.3/1.2****
Area [mm ²]	0.26	0.02	0.04	0.068	0.027	0.06	0.02/0.16 ***
Noise shaping	-	-	Yes	Yes	-	Yes	No
POM or folding error nonlinearity correction & Phase noise improvement [dB]	Redundancy	N.A.**	folding error correction \approx 21dB	N.A.**	N.A.**	N.A.**	POM error correction 22~30dB

*Range is estimated by Resolution x 2^{NoB}.

** Not Applied or Mentioned. If without the POM error correction in the ring TDC or the folding error correction in the 2-D (Vernier) TDC, DNL and/or INL could be worsen sharply with finer granularity sweep of the time interval and consequently the phase noise of DPLL could be degraded accordingly.

*** value for 128-stage version of CRV TDC.

**** The measurable range performance, which is limited by the capability of the test bench.

6.6 Limitation and Drawback

6.6.1 Uneven Granularity of the Input Interval of the Testbench

The uneven granularity of the input time interval of the testbench limits the precision of the measurement in some verification scenarios. Fig. 125 indicates the time steps that can be provided in various testbench branch configuration that are used to cover different regions from 0 to 1.4ns. The range of input coverage increases from branch #0 to branch #8 but at the cost of decrease the resolution of the time steps. Specifically, Branch0 can provide fine resolution at 0.3ps but with only 40ps coverage, while the resolution of Branch 8 is only 3.2 ps, but with a large coverage of 430ps. The above nonlinearity in granularity of the testbench output causes degraded precision when performing test, which might impact the integrity of the verification of the chip. However, the operation and the performance of the TDC itself would not be expected to be affected by the testbench limitation.

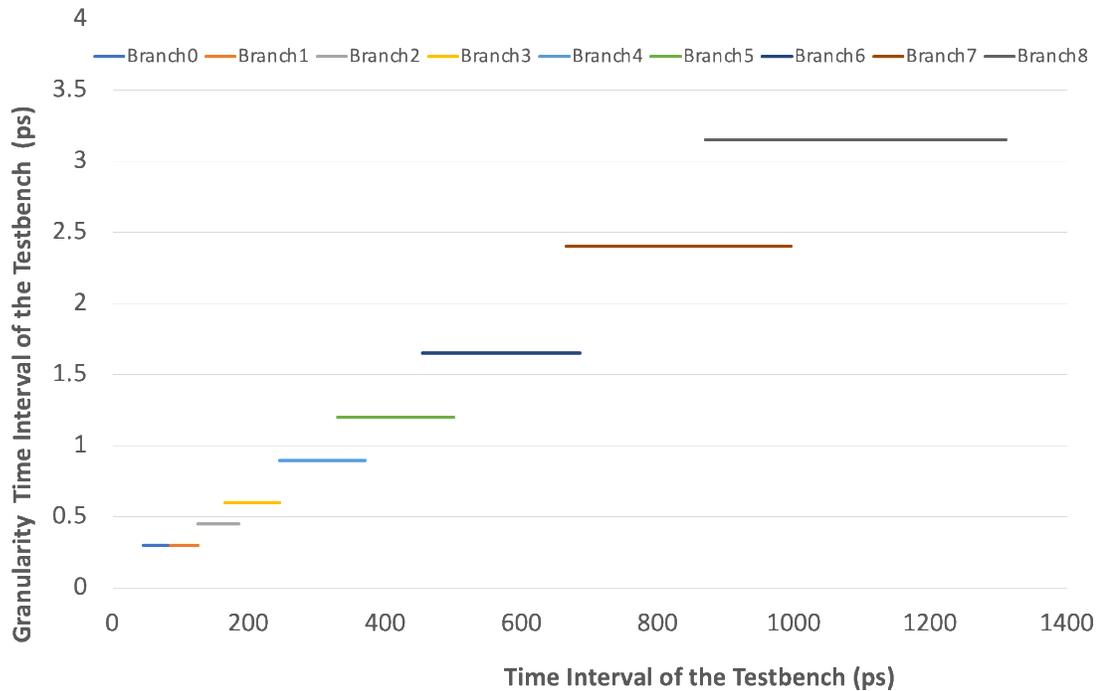


Fig. 125 Testbench time interval granularity characteristics.

6.6.2 Sensitivity and Reliability of the Tunable Sub-picosecond TDC Solution

The stability of the operation of the tunable sub-picosecond conjoined-ring Vernier TDC tends to be a challenge when the time resolution parameter being configured under 0.8ps. In practice of the operation of the prototype, it should avoid making it run with the time resolution of 0.7ps or below.

The measurement in low temperature had to be dismissed due to the lack of the resources that is caused by unexpected lockdown in the office and the lab of the company.

The more comprehensive measurement has been impeded by long-term lockdown caused by unexpected pandemic. For example, the maximum reference frequency limitation test has been missed.

6.6.3 Synchronization between Johnson-Ring and 2nd Stage Binary Counters

The synchronization between two stages of the loop counters (Johnson-ring counter and Binary Counter) has not been considered, owing to the second stage rarely used in current ADPLL application. A glitch correction circuit could be employed to address this issue if needed.

Chapter 7: Thesis Summary

This thesis presented a research on designs and implementations of the Time-to-digital converters (TDCs) that are mainly targeted to be used in an all-digital PLL synthesizer in order to improve the in-band noise contribution and to eliminate the spurs in frequency spectrum due to noise injection caused by the fractional-N frequency division (without TDC) in traditional PLL synthesizers.

In addition to the introduction and analysis of the fundamental concepts and understandings of the published state-of-the-art TDC architectures, the research mainly focused on the characteristics of the TDCs that are employed with ring structures, owing to ring structure being able to reuse a short number of stages in a loop so as to cover a large detection range. However, the ring structure(s) causing inherently parallel output determination mechanism leads to a potential misalignment issue between the outputs (parallel output misalignment). The research then discussed the details of the POM effect and analyzed quantitatively (for the first try in publish) how much it impacts on the phase noise performance in an all-digital PLL applied with various design schemes and situations. It turned out that the degradation could be up to 25 dB or more. It has been figured out from the result of the POM effect analysis that a single-ring type TDC combined with an adequate POM error correction design would be basically one of the most effective and efficient TDC solutions.

Then the thesis presented a new TDC architecture and circuit design implementation that has completed the following achievements and advantages:

- **POM correction:** It has created a parallel outputs misalignment correction

circuit that can distinguish the occurrence of the misalignment during its operation so as to eliminate unwanted noise injection by 25dB or more.

- **New architecture:** A novel partially conjoined single-ring Vernier architecture has been studied out for optimal overall quality among the high performance, simple design and low power consumption.
- **Sub-picosecond time resolution:** Meanwhile, it retains the high performances specially in terms of a fine time resolution as fine as 0.8ps.
- **Large detection Range:** and an extendable phase (time) detection range with a couple tens nanoseconds.
- **Tunable time resolution control:** It built up a configurable digital control to enable a tuning time resolution function. This function could be used broadly for different optimization purpose.
- **Short latency:** It achieves a competitively short latency time characteristic by creating a new structure, allowing higher reference frequency applied for better in-band phase noise performance.
- **Coarse/fine switch:** It has realized a freely switchable coarse/fine resolution scheme so as to remain a choice between the best resolution performance and the lowest power consumption.
- **Nonstop N-Calibration:** It provides an uninterrupted N-calibration method to continuously optimize the functions and characteristics of the TDC during work period.
- **Metastability phase shift elimination:** Address pseudo-metastability issue by employing a double-sampling circuit. Furthermore, it is able to eliminate the

tiny phase variation.

In conclusion, the proposed two versions of the TDC (32-stage conjoined-ring Vernier TDC and tunable sub-picosecond conjoined-ring Vernier TDC) have been implemented to eliminate (not minimize) the intrinsic computing error due to the parallel-output misalignment (POM) in the ring type TDC, eliminating the phase noise corruptions by 25dB or even more. The tunable digital control implementation ensures the practical effective time resolution at 0.8ps even in PVT variations. The detectable range is flexible to be expanded as need due to ring structure and enough width of the bits of the loop counter. Furthermore, the CRV TDC employs only one ring structure in the TDC circuit to significantly simplify the complexity of the POM error correction circuit compared to that in the traditional Vernier ring TDC (2-ring). The multi-transition situation in the work will not cause any encoding error, on the contrary it can be used to continuously perform N-calibration during the operation, leading to the improvement of the rippled-curve nonlinearity performance of the TDC.

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Appendix 1 TDC Timing Consideration for Higher Reference Frequency

TDC operating-period performance is seldom discussed due to sufficient time margins in most applications under low REF frequency circumstances. However, a high REF frequency requirement trends to be becoming more popular in order to achieve better phase noise performance. Therefore, the operating period performance will play a more important role in TDC research to achieve an optimal solution, especially in scenarios which need a high reference frequency (>50MHz). Operating-period (P_L) is defined as a time period starting from the moment of the rising edge of the triggering signal and ending with the guaranteed moment when the TDC can accomplish a final output for the ADPLL system computation. The purpose of the operating-period performance is primarily to estimate whether a certain kind of TDC solution is feasible for a specific applied reference frequency. Meanwhile, it can also predict the upper limit of the frequency of the reference signal being used by this TDC solution. Moreover, by learning about the time margin of a TDC solution, a comprehensive optimization is available for the purpose of obtaining an optimal solution not only of the TDC but also of the end-to-end synthesizer design.

1A General Operating-Time Procedure

Prior to a detailed discussion of the operating-period performance analysis, a general operating procedure of a TDC is described as follows (Fig. 126):

- a) P_A : The active period starts with the rising edge of the leading signal and stops at the moment of the rising edge of the triggering signal. The active period corresponds to the phase difference of a TDC.
- b) P_C : The capturing period is regarded as the time period that a TDC takes to ensure all necessary states of arbiters have been stored.

c) P_E : The evaluation period indicates how long a TDC spends to process the output of the arbiters and produce a final quantitative binary number which shows the measured phase difference. Usually this period is relatively stable and less than a few ns in a variety of TDC solutions, unless the number of the arbiters is too large (more than 200) or the computations are complicated. 4ns of P_E is assumed for all TDCs for comparison in this thesis.

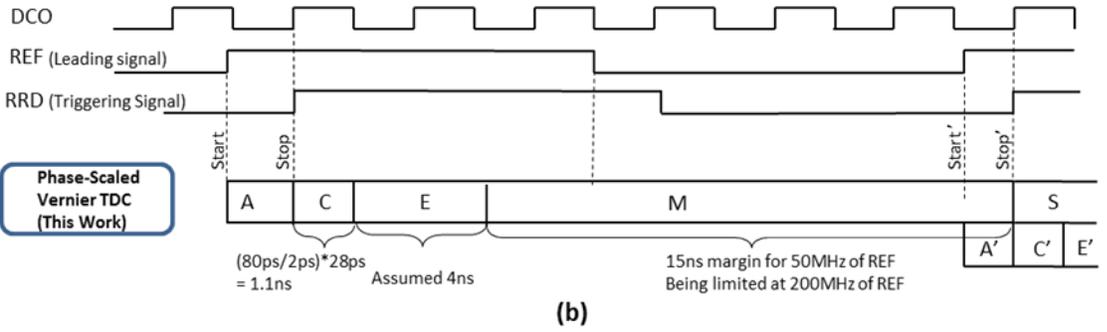
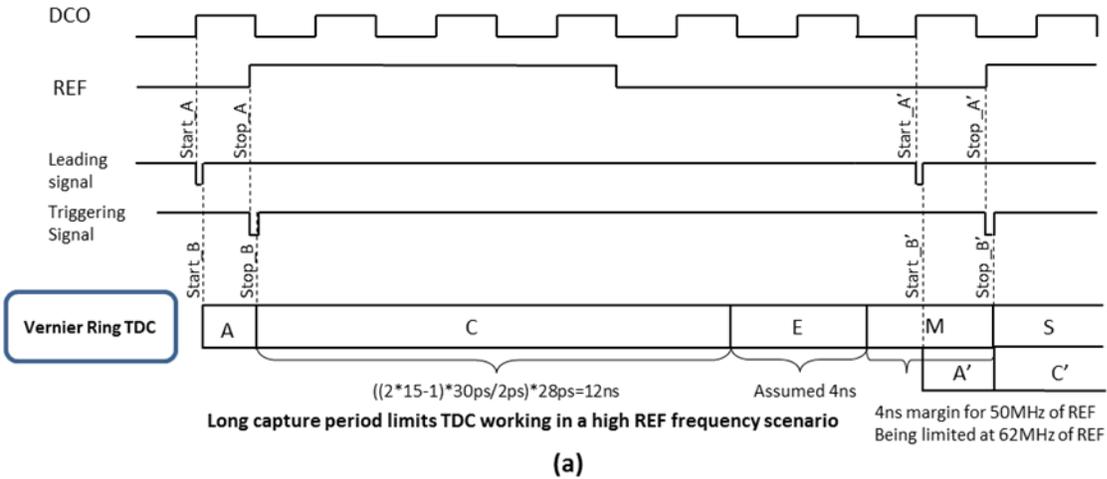
d) P_M : The margin period is the remaining time length after subtracting P_C and P_E from the REF period P_{REF} .

e) P_S : The period for ADPLL system computation and operation. P_S is expected to occupy the next REF period.

Therefore the REF period, P_{REF} and the maximum value of f_{REF} , f_{REF_MAX} can be expressed by:

$$P_{REF} = P_C + P_E + P_M \quad \text{Eq.(19)}$$

$$f_{REF_MAX} = 1/(P_C + P_E) \quad \text{Eq.(20)}$$



A: Active Period. C: Capturing Period. E: Evaluating Period. M: Margin Period. S: System Operation Period. A': Next Active Period.

Fig. 126 Operating-period Performance Comparison Between (a) VRTDC and (b) Phase-Scaled Vernier TDC.

2A Operating-Period Performance Comparison

First, a quantitative operating period analysis is performed for the presented phase-scaled Vernier TDC. According to the principle of the phase-scaled Vernier TDC, the mandatory fine-resolution phase length (i.e. normal length, T_{nor}) is 80ps in this case and the Vernier TDC core will need 40 stages with each stage having a resolution of 2ps (30ps-28ps). The guaranteed capturing period is determined by:

$$P_c = \left(\frac{T_{nor}}{\Delta\tau} \right) \cdot \tau_1 = \left(\frac{80ps}{2ps} \right) \cdot 28ps \quad \text{Eq.(21)}$$

$$= 1.1ns$$

The length of the evaluating period depends on the complexity and the parameters of the evaluator. Choosing 4ns for the evaluation period will be adequate in most modern CMOS processes for a moderate number of inverter stages. Thus, for a 25MHz REF, the margin period is:

$$P_M = P_{REF} - P_C - P_E \quad \text{Eq.(22)}$$

$$= 40n - 1.1n - 4n \approx 35n$$

Also note that the highest accepted reference frequency is:

$$f_{REF_MAX} = \frac{1}{P_C + P_E} = 200MHz \quad \text{Eq.(23)}$$

As for a 15-stage Vernier Ring TDC, the mandatory fine-resolution phase length (i.e. normal length, T_{nor}) is $(2*N-1)*\tau_1=870ps$. The guaranteed capturing period is determined by:

$$P_c = \left(\frac{T_{nor}}{\Delta\tau} \right) \cdot \tau_1 = \left(\frac{870ps}{2ps} \right) \cdot 28ps = 12ns \quad \text{Eq.(24)}$$

Similarly, for a 25MHz REF, the margin period will be only 4ns and highest accepted reference frequency will be 62MHz. The above results and performances are summarized in Table 7, which also includes the result of a traditional Vernier TDC. Note from Table 3 and Table 7 that a traditional Vernier TDC may need an extremely large number of delay stages in the case of demanding specifications (fine resolution and wide phase-detection range), resulting in an

impractical solution. Thus, for a Vernier type, the phase-detection range performance and corresponding stages of delay chains would be a tough limitation, although it can achieve a fine resolution. Compare to the VRTDC, the phase-scaled Vernier TDC can accept a f_{REF_MAX} 3 times higher (200MHz/62MHz), which can improve the phase noise performance (caused by the TDC time resolution) by over 5 dB. In fact, the phase-scaled Vernier due to its ring-less structure of the triggering path enables one-off latching action, compared to the ring structure of the triggering path in a Vernier ring TDC where the multiuse of the delay chains and arbiters needs a multi-latching and updating function which demands longer operating-period performance.

Table 7: Improvement of the Phase Noise Performance with Different Accepted Reference
Frequency (1GHz of DCO output)

Specification	Symbol	Vernier	15-stage Vernier Ring	Phase-scaled Vernier
TDC Time Resolution	$T_{res}(\Delta\tau)$	2ps	2ps	2ps
Normal-Inverter Delay	$\tau_2 \& \tau_1$	30ps&28ps	30ps&28ps	30ps&28ps
Mandatory Fine Resolution Phase Length	T_{NOR}	NO	$(2*N-1)*\tau_2=870ps$	$3*\tau_2=90ps$
Effective N stages	N_e	500	30	40
Max Capture Period	P_{C_max}	$500*28ps=14ns$	$(870ps/2ps)*28ps=12ns$	$40*28ps=1ns$
Operating-period	$P_E + P_C$	$14n+4n=18ns$	$12n+4n=16ns$	$1n+4n=5ns$
Highest REF Frequency	REF_{max}	$1/(14n+4n)=55MHz$	$1/(12n+4n)=62MHz$	$1/(1n+4n)=200MHz$

Phase noise			
performance	0	0.5dB	5.6dB
Improvement			

Table 8: Comparison of Several TDC Architectures

Specification	Traditional TDC	Ring-Osci TDC (9-stage)	Vernier TDC	Vernier Ring TDC (15-stage)	Phase-scaled Vernier TDC
Resolution	10ps	10ps	2ps*	2ps	2ps
Effective stages	12.5n/10p= 1250	9	6250	30*	40
Operating-Period (Assume PE=4ns)	4ns	4ns	183ns	16ns	5ns
Highest f_REF	250MHz	250MHz	5.5MHz	62MHz	200MHz
Phase Noise***	0dB	0dB	2.6dB worse	7.9dB better	13dB better
Area Cost	High	Low	Super high	Medium	Medium
Power Consumption	High	Low	High	Medium	Low

Applied field	Wide range, coarse resolution, low cost	Narrow range, high resolution	Wide range, high resolution, medium cost	Wide range, fine resolution, low cost
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*: effective stages doubles due to ring type of triggering path completing a rotation every other rotation.

Appendix 2 ADPLL System Calculation Simulation

Research topic

- All digital PLL based on TDC with the following targeted performance
 - Reference frequency: 10-50 MHz
 - Output Carrier frequency: min 3GHz, max 20GHz
 - Tuning range: min 1GHz
 - Phase noise @3GHz carrier frequency:
 - -112dBc/Hz @ 10kHz,
 - -117dBc/Hz @ 100kHz,
 - -130dBc/Hz @1MHz,
 - -165dBc/Hz @ 10MHz
 - Max PLL bandwidth: 3MHz
 - RMS jitter: 60fs RMS @ 12kHz to 20MHz, 80fs RMS @ 1kHz to 20MHz
 - Power dissipation: 100mW
 - Factor of Merit: -242dB
 - Area: 1mm²
 - Process: not lower than 55nm

Fig. 127 ADPLL System Specifications from Microsemi

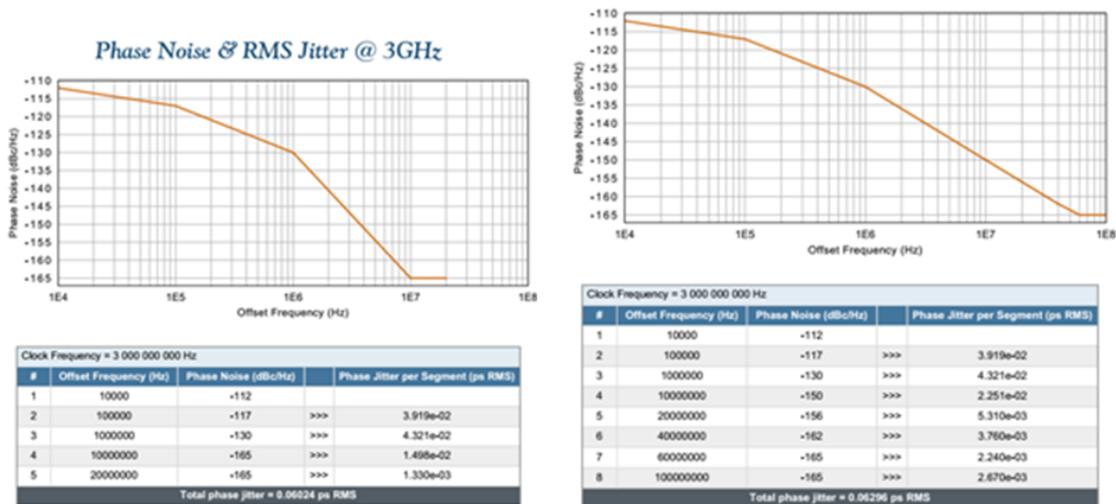


Fig. 128 Jitter calculation from phase noise

- Commonly best VCO phase noise at 10MHz offset is around -155dBc/Hz for high frequency (>10GHz) application, and -165dBc/Hz@10MHz offset seems for relative low frequency or for thermal noise floor.
- To ensure maximum 20dB/decade slope of phase noise, Modify phase noise to -150dBc/Hz@10MHz offset that makes RMS phase Jitter worse to 63fs.

3A Phase Noise Contribution and Synthesizer

$$\text{Total PhaseNoise} = \text{VCO_Noise} + \text{TDC_Resolution_Noise} + \text{CO_Quantization_Noise}$$

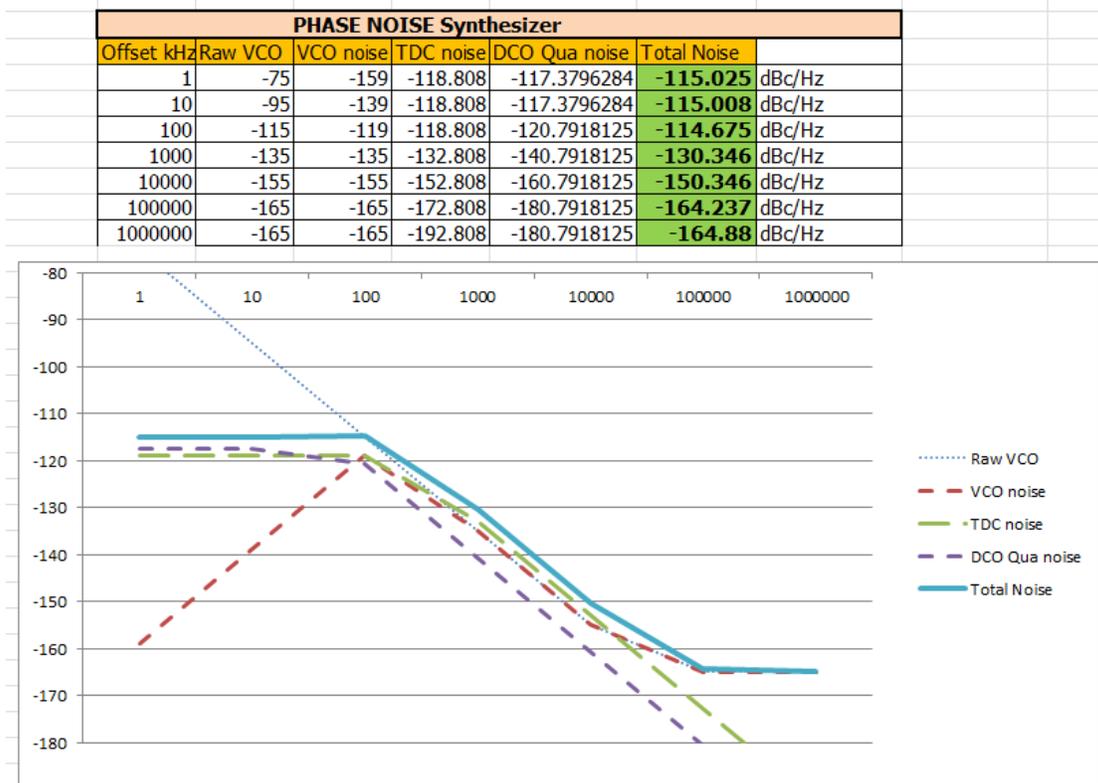


Figure 129 Phase noise contributions of PLL

PLL Frequency performance Calculation							
Fref	FDCO	Wn	Damping factor	Alpha	Rho	TDC Resolution	DCO resolution
MHz	GHz	MHz	non	non	non	ps	kHz
40	4	0.3	0.707	0.010605	0.00005625	1	2
				2 ⁻⁸	2 ⁻¹⁷		
DCO WF Dithingwordlength		DCO WI wordlength		DCO rough range wordlength	DCO freq fine-tuning range		DCO freq whole tuning range
6		10		4	0.131072 GHz		2.097152
In-band TDC PN							
-118.808 dBc/Hz							
DCO phase noise of quatization							
-117.38	dBc/Hz	in-band					
-120.792	dBc/Hz	0.1 MHz offset					
-140.792	dBc/Hz	1 MHz offset					
-160.792	dBc/Hz	10 MHz offset					
-180.792	dBc/Hz	100 MHz offset					
RAW VCO Noise							
Q factor of VCO	Power of Carrier	Noise Factor of Osc	Noise Floor	Freq Offset	RAW VCO Noise		
	dBm		dBc/Hz	kHz	dBc/Hz		
15	0	1	-165	100	-114.3705717		
RAW VCO Noise			Slope of Curve				
-155		10 MHz offset		20 dB/Decade			

Figure 130 PLL and TDC characteristics bond

To achieve the above specifications, it

- Entails VCO with acceptable Raw VCO phase noise between 0.1 MHz and 20MHz, because this range is out-side band of loop filter and mostly not possible to be filtered out.
- Needs sufficiently high DCO frequency resolution to make quantization-noise appreciably smaller than VCO's raw phase noise at outside-band range, making it as a neglectable contribution?
- Needs proper Alpha and Rho combined value for the right loop bandwidth by achieving which it makes PN of TDC equal to PN of DCO quantization noise at place of 3dB-edge. And that yields roughly best phase jitter as common experience.

- According to in-band phase noise of TDC, figure out TDC effective resolution.
- Optimization based on integral RMS jitter as shown below.

Table 9 Jitter with PLL band width

Wn (MHz)	0.1	0.25	0.3	0.5
RMS Jitter (fs)	83	73	66	72

4A ADPLL System Modeling and Simulation

To design a novel TDC, a simulation platform is necessary and important, by using which a configurable environment could be setup to help estimate and design a certain type of TDC and to verify the performance of TDC and PLL, as well as it is a good starting point for improvement of system structure of an ADPLL.

Hopefully, this simulation structure will be improved and refined step by step according to requirements and suggestions from discussion within the group.

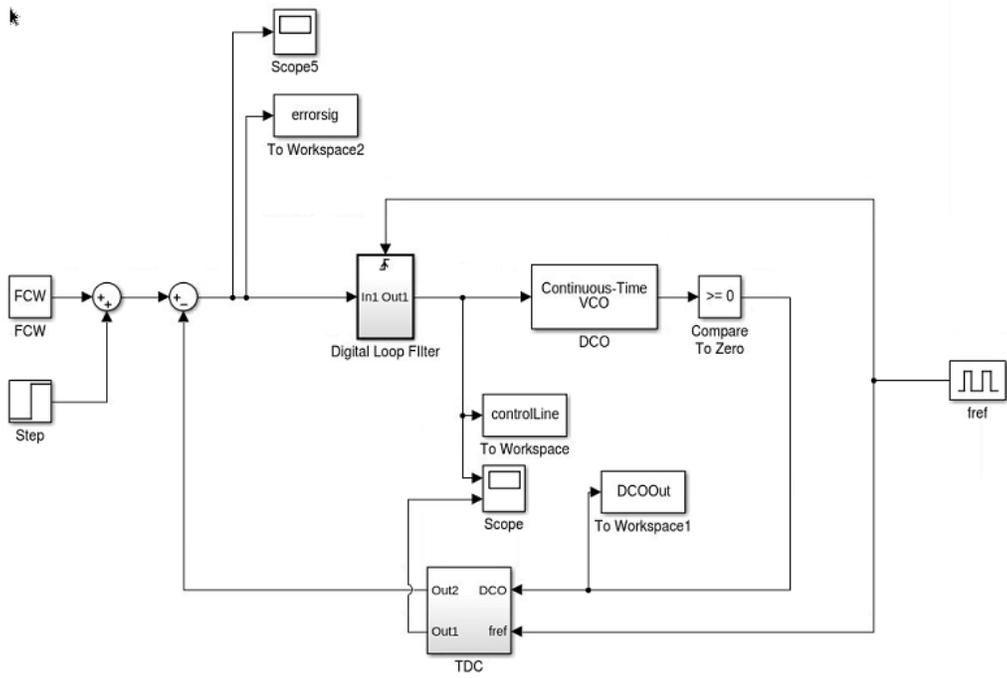


Figure 131 Ddiagram of PLL operation in block level

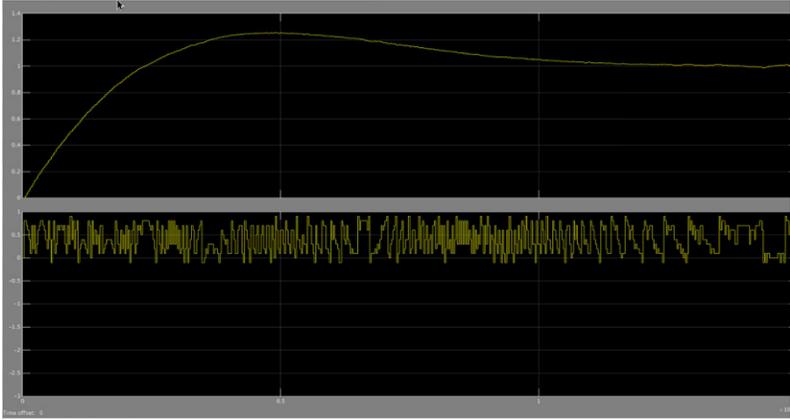


Figure 132 PLL operation in time domain

To build up a basic fractional-N division ADPLL system model in Simulink. It yields reasonable acquisition and tracking.

5A Simulation with Type-I

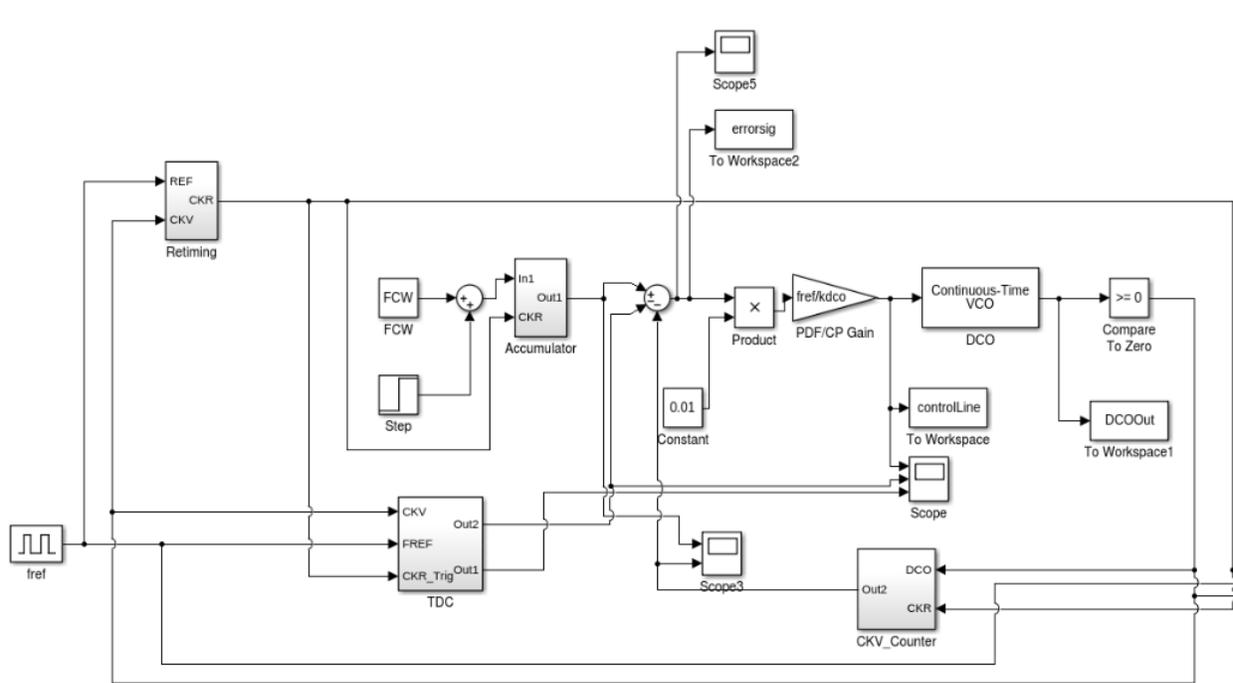


Figure 133 Updated diagram of a type I PLL operation

One integrating pole, feature faster dynamics and fast frequency/phase acquisition.

PD is not conventional one but an arithmetic subtractor, avoiding noise and spurs by feeding-through.

Phase error is proportional to the frequency offset of DCO (actual freq away from central freq). Operating

Synchronous digital architecture by using reference re-timing solution, avoiding impact of injection pulling on spurs.

Alpha could be configurable to control the feature of PLL, such as loop bandwidth or phase noise.

Dynamic range of phase error depends on word-length of accumulator.(compare with $\pm 2\pi$ linear range of conventional solution)

6A TDC Block Diagram

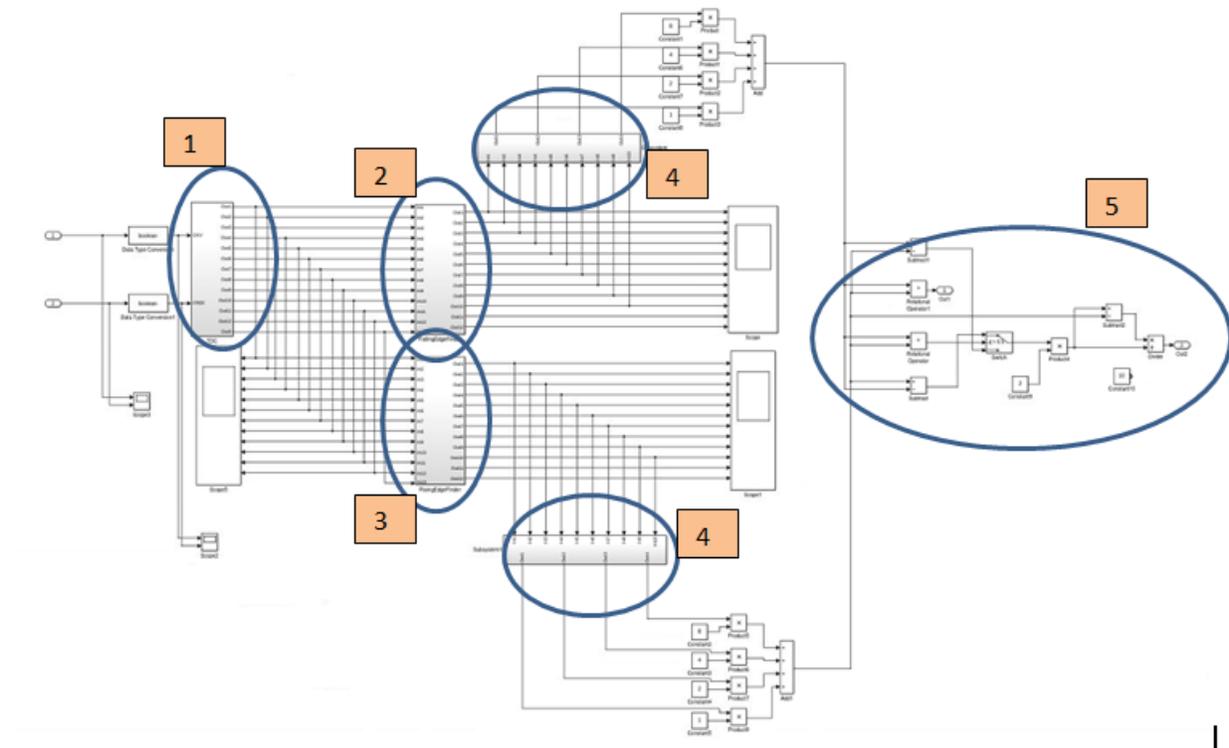


Figure 134 TDC RTL level implementation

#1: TDC delay-chain. #2: Falling-edge finder. #3: Rising-edge finder.

#4: Encoder or Priority Encoder. #5: Period Calculator and fractional part calculator.

7A Simulation with Type-II

Adding a second pole at zero frequency by proportional-integral-controller.

Achieve better noise rejection at in-band range, (further 20dB/decade), remove flicker noise and VCO noise.

No frequency error.

Zero phase offset between FREF and FDCO.

Slow time for acquisition.

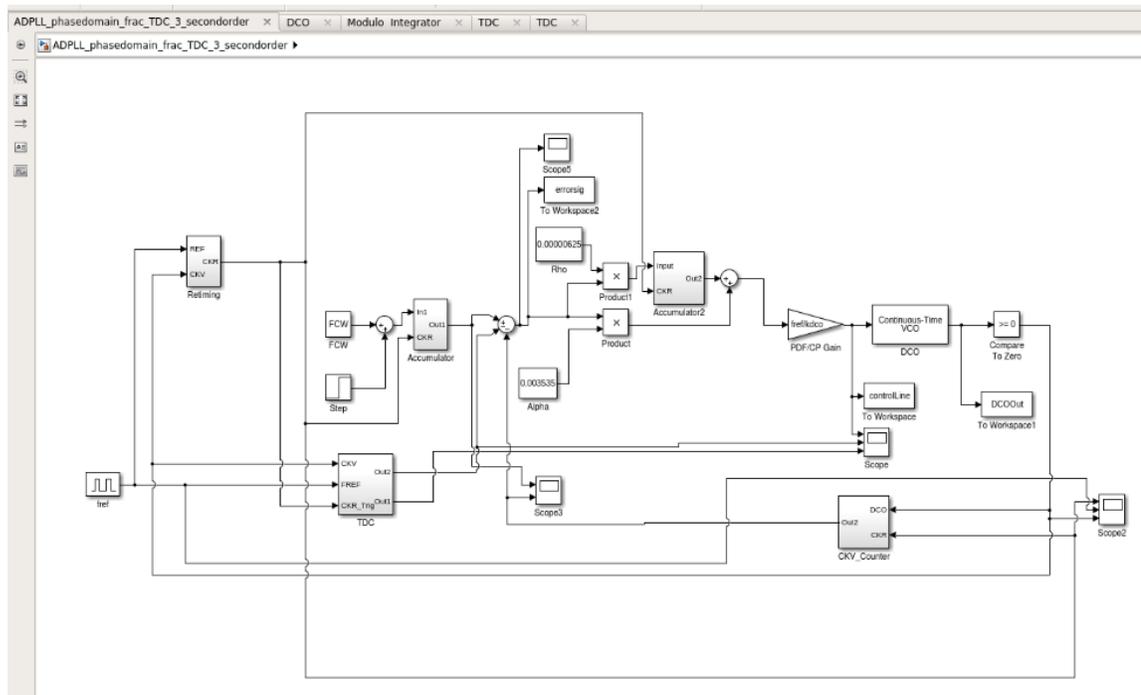


Figure 135 Updated diagram of a type II PLL operation

8A Comparison between different Configurations

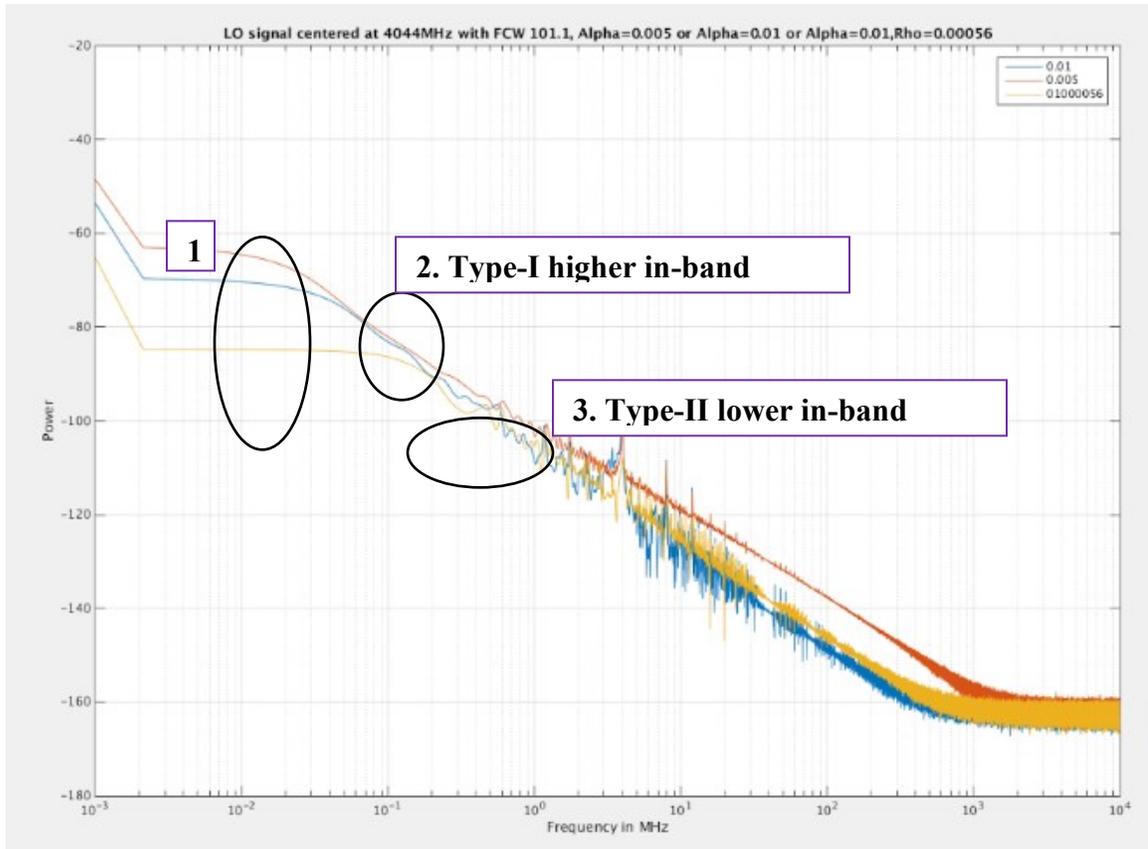


Figure 136 Phase noise comparisons among different PLL designs

1. Due to 2kHz resolution bandwidth of FFT conversion.
2. In type-I ADPLL, in-band phase-noise level increases inversely with Alpha.
3. Comparing with Type-I, Type-II ADPLL yields lower in-band phase-noise due to extra rejection from second-order loop.

9A Preferred Solution----- Switchable TYPE-I & TYPE-II ALL DIGITAL PLL

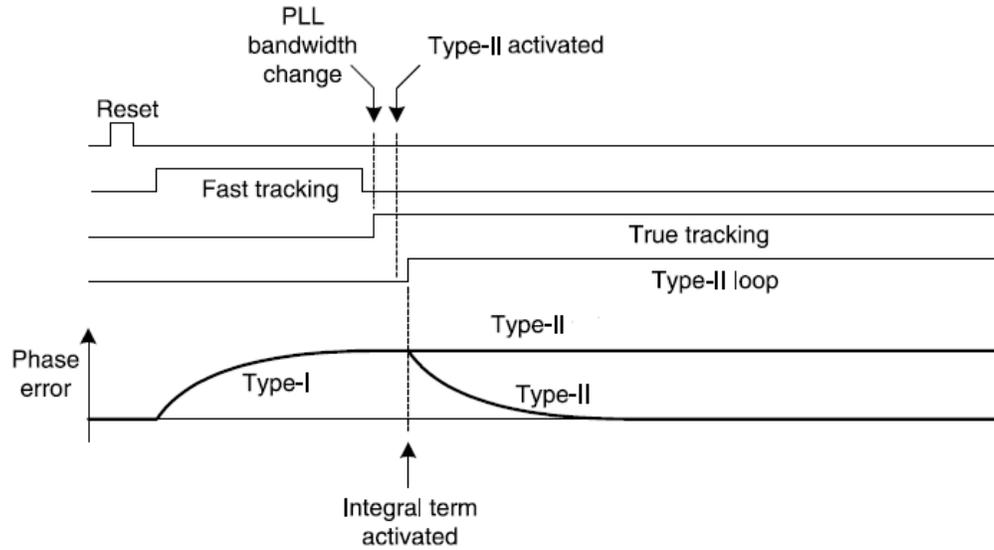


Figure 137 Comparison among different PLL types

Acquisition mode: Type I with high gain for fast acquiring. (wide bandwidth)---->High Alpha, Rho off

Tracking mode: Type I with low gain for tracking. (narrow bandwidth) -----> small Alpha, Rho off

Performance mode: Type II with Proportional-integral controller for tracking with best performance. -----> small Alpha & Rho on

