GaN HFET Modeling and Model Validation Through High Efficiency Power Amplifier Design

by

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Abstract

This work presents the implementation and application of a modified Curtice cubic model for AlGaN/GaN HFETs. Modifications to the standard Curtice cubic model include the addition of two limiting functions that are applied to the main current source in the model. The limiting functions are continuous equations that provide the ability to model pinch-off in a model that does not currently support this functionality. Parameter extraction is performed over a wide range of operating conditions to dertermine the values of the model components for a 100 μm Nitronex AlGaN/GaN HFET. An empirical class-F PA is designed using the 100 μm Nitronex AlGaN/GaN HFET as a form of black box validation of the model. Simulated power added efficiency of 29 % is predicted for an output power density of 0.361 W/mm with a transducer gain of approximately 6.5 dB while measured power added efficiency of 37 % is achieved for an output power density of 0.411 W/mm with a transducer gain of more than 7 dB. Comparison to the standard Curtice cubic model shows a simulated PAE of 23 %. Subtracting the offset in DC power consumption that results from not being able to model pinch-off brings the simulated PAE to 26.94 %, which is a 10 % improvement in simulated PAE.

Acknowledgments

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List of Abbreviations

2DEG	2-dimensional electron gas
BFOM	Baliga figure-of-merit
BJT	Bipolar junction transistor
DC	Direct current
DUT	Device under test
GaAs	Gallium arsenide
GaN	Gallium nitride
HB	Harmonic balance
HEMT	High electron mobility transistor
HFET	Heterojunction field effect transistor
HPA	High power amplifier
JFOM	Johnson figure-of-merit
LCD	Liquid crystal display
LED	Light emitting diode
LUT	Look-up-table

PA	Power amplifier
PAE	Power added efficiency
PCB	Printed circuit board
VNA	Vector network analyzer
RF	Radio frequency

Chapter 1

Introduction

This chapter provides an introduction to gallium nitride (GaN), power amplifiers (PA) and the rest of this thesis. It will be shown that GaN is a competitive alternative to gallium arsenide (GaAs), which is an existing technology used throughout the electronics industry, particularily for PA design. Since GaN technology's applications in the RF field is still in its infancy accurate models for large-signal operation are few and far between. This thesis presents an implementation of a model and applies said model to a large-signal application at RF frequencies. The work in this thesis was performed using a 100 μm GaN heterojunction field effect transistor (HFETs) provided by Nitronex.

1.1 AlGaN/GaN as an emerging technology

GaN devices first found a foothold in the consumer electronics market as high-intensity blue and white light emitting diodes (LED), commonly used for keypad backlighting and liquid crystal display (LCD) backlights on handsets [1]. GaN as a

material has a direct band-gap voltage that is more than three times larger than that of silicon, which gives GaN devices the ability to efficiently convert electrical energy into light, which is appealing to photonics. It is this same, large, direct band-gap that allows for high-temperature operation and large breakdown voltages [1], which makes GaN appealing to the electronics industry, more specifically the high power amplifier designers. Power densities as high as 12 W/mm of gate width have been observed with noise figures lower than 1 dB at 10 GHz. In low speed applications sufficiently large gates can be used to achieve breakdown voltages exceeding 1 kV which is appealing for power switching applications [2]. These large breakdown voltages, current densities and power handling capabilities make GaN devices an attractive prospect for use in RF base stations and other high-power applications.

GaN can also be doped quite easily with aluminum in order to control the characteristics of the bandgap. This is primarily useful in fabrication of LEDs but also allows for engineering of strain controlled lattices [3]. These strain controlled lattices are required in fabrication of HFETs, which are not subject to electron drift velocity limitations [1].

A well established alternative to GaN is GaAs. GaAs devices have been present for some time and GaN devices have been shown to have many of the same properties as their GaAs counterparts. These properties include high sheet electron density, direct band-gap, high electron mobility and velocity saturation, among other things [1]. A simple and basic method of rating semiconductor materials can be applied to these two competitors using figures of merit. There exist two common figures of merit that are used throughout the semiconductor industry; the Baliga figure-of-merit (BFOM) [4] and the Johnson figure-of-merit (JFOM) [5]. The Baliga figure-of-merit can be used

to get a metric of the power loss at high frequencies for a given material. The Johnson figure-of-merit can be used to get a metric of the power-frequency performance. Both of these figures-of-merit are essentially the product and quotient of several physical constants of the material being rated. In both cases a larger figure-of-merit is desirable over a low figure-of-merit.

In [6], Yoder computes both of these figures-of-merit for several materials, a small subset of which is shown in Table 1.1. From the values listed in Table 1.1 it is clear

Figure-of-merit	Si	GaAs	SiC	GaN
JFOM	9	62.5	1440	15670
BFOM	1	15.7	Not reported	24.6
Thermal conductivity (W/ cm · K)	1.5	0.46	4.9	1.3

Table 1.1: Figures-of-merit

that, at least from a semiconductor material standpoint, GaN is very attractive.

The constants used to derive the JFOM and BFOM are what give GaN HFETs their performance advantages. HFETs are implemented in a similar fashion to traditional FETs, where the source and drain are contacted using ohmic contacts to the conducting layer. However, in traditional FETs the gate pulls charge carriers from the substrate to create a channel between the drain and source. In the HFET, however, the Schottky gate is used to repel an abundance of charge that exists naturally in the channel. Under no bias, a 2D electron gas (2DEG) forms at the barrier of the active material and the underlying interface layer as shown in Figure 1.1.

Typically, the density of electrons in GaN HFETs is an order of magnitude greater than that of comparable GaAs HFETs at that interface [1]. As stated above, the high electron density and bandgap that is significantly larger in GaN than that of GaAs results in larger breakdown voltage, better thermal characteristics, higher drift

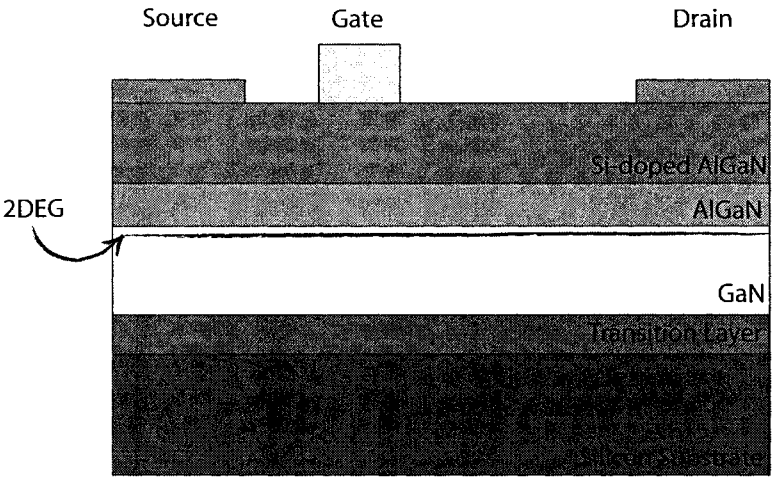


Figure 1.1: HFET physical structure from [1]

saturation as well as other advantages. These differences make GaN a promising improvement over GaAs technology, especially in the field of HPA design.

1.2 Modeling of AlGaN/GaN HFETs

There exist many different device models each with their own advantages and shortcomings which could have been used for this work. Selection of a single model as a starting point is a significant task in its own respect. Studies have shown that, for GaAs devices, the Curtice cubic model provides the best results for direct current (DC) operation [7]. Searches for resources on GaN modelling and power amplifier (PA) design made it clear that the Curtice cubic model was the most common starting point. Even though the Curtice cubic model was originally designed for GaAs devices it ports well to GaN due to the number of similarities between the two materials' properties. Similarities start with the physical structure of the device and

extend to operating characteristics such as RF dispersion resulting from carrier trapping and self-heating effects [8], [9]. Given the similarities between the two different technologies it is not surprising that the typical starting point for a GaN model is the same as for GaAs devices [10], mainly the Curtice cubic model.

In [10] Green *et al.* use the Curtice cubic model as a starting point and add a branch to model RF dispersion. They go on to show that such a model can accurately predict the behaviour of an AlGaN/GaN FET. Lee and Webb go one step further in [11] and show that the addition of a thermal sub-circuit can further improve the model's accuracy by modelling self-heating related effects. It is based on these findings that the final model used in this work was that discussed by Lee and Webb in [11].

1.3 Power amplifiers

As the last active stage of a typical RF system the PA is of great importance, amplifying the output signal to the required level for the given application. Performing this amplification in an efficient manner makes the design an especially difficult one.

Of the different classes of amplifiers each has its own strengths and weaknesses. PAs are classified by the amount of time in which the active device is conducting. Conduction angle is the term used to quantify the fraction of the RF cycle where conduction occurs. By changing the bias point such that the conduction angle is increased, linearity can be improved at the cost of efficiency as the range of operation that does not incur clipping is expanded as is quiescent current. A reduction in the conduction angle causes the opposite. Naturally, there are other factors that determine PA characteristics. Trade-off management is required by the designer to

create a PA with the desired behaviour.

Class-A PAs are such that the active device is biased so that it is on for 360° of the RF cycle. Due to the inefficient bias point the PA can operate over a broader range of input signal amplitudes without clipping. This is possible because the PA operates closer to mid-rail than other classes, which allows for larger signal swing at the output. The result is a higher output power capability. In addition to the linearity and output power, the maximum operating frequency of class-A PAs is higher than other classes [12]. However, since the PA is always conducting current the theoretical max efficiency of this class of PAs is the lowest of all classes.

Class-B PAs are biased such that the active device is conducting current for exactly half of the RF cycle. As with class-A PAs but to a lesser extent this class of PAs typically has high linearity but at a higher efficiency [12]. A class-AB PA is one that has a conduction angle between 360° (Class-A) and 180° (Class-B).

Class-C PAs are even more efficient than class-B PAs due to the fact that their conduction angles are reduced to less than half of the RF cycle. In this case linearity, gain and output power are sacrificed [12].

Class-F PAs have bias points most similar to class-AB PAs. The key difference is the use of harmonic tuning circuits at the output that shape the drain voltage and current waveforms. By overdriving the class-AB PA and using proper harmonic terminations, the voltage and current at the drain of the active device approach a square and half-sine wave, respectively [12]. The result is a more efficient means of achieving high output power at the cost of linearity. However, since class-F PAs have a low-conduction angle to start with and are overdriven, they are not a good choice for modulation schemes that convey information through amplitude rather

than frequency or phase content [13]. Class-F theory is discussed in much more detail in Section 4.

PA performance is a strong function of both the output loading conditions and the bias point. A common method of performing matching is to use a conjugate match, particularily for small signal designs. Such a match ensures that maximum power transfer occurs from the active device to the load. However, during normal operation one of the many physical limitations of the active device (*e.g.* maximum allowable drain current, breakdown voltage) will be reached before the others. A load-line match leads to higher output powers than the conjugate match method because device limitations are taken into account in this method. For amplifiers operating in the linear range, the standard load-line match methodology is commonly used in selecting the optimal load impedance. There exists a more brute force method of performing a match called a load-pull. A load-pull is essentially an evaluation of the PA characteristics of interest (*e.g.* power added efficiency (PAE), output power) over the entire impedance-plane. This is nitially performed very coarsely, then evaluated at a finer resolution over the area of the load-plane of specific interest. When performing empirical circuit design the load-pull is the best way to perform matching but requires an accurate model.

1.4 Thesis outline

This thesis details the steps taken during the creation of a GaN device model followed by the parameter extraction techniques that were used to populate said model. Following this, the theory behind the operation of class-F PAs is examined as well as

their potential efficiencies and output powers. Once, the reader is familiar with the theory of class-F operation, the steps taken to designing a clss-F PA are examined and simulation results are presented. The resulting class-F PA's implementation is then discussed and a comparison between simulated and measured results is presented. Finally, future work and contributions are outlined.

Existing work performed by other researchers at Carleton University within the department of electronics that relate closely to this topic include [14] [15]. In [14], Chyurlia presents a feasibility analysis of the integration of AlGaN HFETs with CMOS on silicon substrates. In [15] Panesar designs a class-E switch mode power amplifier using a 2 mm transistor from the same die that the 100 μm transistor for this work came from. The key difference between those two theses and this work is that this thesis is primarily an exercise in modelling that uses class-F PA design as a method of validating the model that was created.

Chapter 2

AlGaN/GaN Device Modeling

2.1 Model description

This chapter presents a brief description of the model used, followed by a review of the physical origins of each of its components. As discussed in Section 1.2 model selection can be quite difficult as there exist so many options. This chapter will also address the reasoning behind the selection of the final model used in this work. However, the most logical starting point is some derivative of the Curtice cubic model. Based on existing documentation the model presented in [11] was selected and implemented using Agilent advanced design system's (ADS) *c*-based model entry tool. ADS was the design suite that was chosen to work with as it was the tool that the author was most familiar with and it provides the simplest interface for creating a highly customizable model. This tool allows for the user to follow a wizard to get a model template. The template consists of several functions that define the linear and non-linear currents, voltages, capacitances and charges at any number of nodes. The model created can

be seen in Figure 2.1.

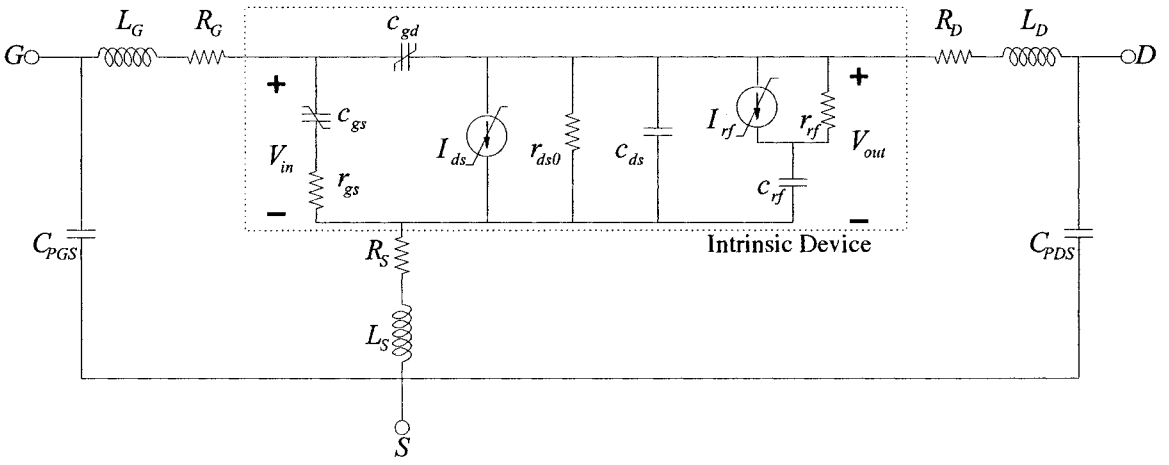


Figure 2.1: Compact model implementation (based on [11])

Since the original Curtice cubic model's inception in [16] there have been many documented modification and improvements. Two key additions that are discussed below are (1) the ability to model self-heating effects and (2) RF dispersion. There still exists one obvious drawback to this model: the existence of a DC path from drain to source that can not be pinched-off in traditional implementations. This results in a leakage current that can be quite significant depending on the design. This is particularly problematic with large drain biases that are common in high power amplifier designs. As a result a method of modelling a fully pinched off HFET is presented in Section 2.3.3.

2.2 Extrinsic components

The extrinsic components that required modeling were the capacitance associated with the bondpads and the series resistance and inductance associated with the trace

from the bondpad to the device periphery. These are shown as all the components outside of the area labeled "Intrinsic Device" in Figure 2.1. The extrinsic gate and drain capacitances were modeled using the shunt capacitors C_{PGS} and C_{PDS}, respectively. The parasitic resistances associated with the gate, drain and source series traces were modeled using the series resistors R_G, R_D and R_S, respectively. Similarly, the parasitic inductances associated with the same series traces were modeled using the series inductors L_G, L_D and L_S.

Since the characterized device was mounted to a microwave substrate, any parasitics that were not a result of the die (*e.g.* bondwires) were modeled as part of the external circuit.

2.3 Intrinsic components

The physical structure of the HFET used in this work is shown in Figure 1.1 on page 4. It is this structure that gives rise to the intrinsic parasitics of the device, which can be divided into three main sections: the gate-source, gate-drain and the drain-source active regions. Two other sub-circuits are included in the model to account for the effects of self-heating and RF dispersion. This work uses the terms RF dispersion branch and thermal sub-circuit to refer to these two groups of components in their respective orders.

This section describes the physical origins for each of the components in the intrinsic region of the compact model shown in Figure 2.1.

2.3.1 Gate-source region

The gate-source region's effects are modelled with a series combination of c_{gs} and r_{gs}. The gate-source capacitance (c_{gs}) varies in proportion to the physical distance between the gate and source. The gate-source resistor (r_{gs}) is a result of the ohmic contact of the gate material and the routing layer in addition to the distributed resistance of the narrow gate itself. Mathematically, the capacitor c_{gs} is defined as a non-linear capacitance given by (2.1) in [17].

$$c_{gs}(V_{in}, V_{out}, T) = c_{gs}(T)\left(\frac{1 + c_{v1}V_{out}}{1 + c_{v1}V_{ds0}}\right)\left(\frac{1 + f_{c1}\tanh[f_{c2}(V_{in} + v_{fcg})]}{1 + f_{c1}\tanh[f_{c2}(V_{gs0} + v_{fcg})]}\right) \tag{2.1}$$

where the parameters of the capacitance equation are as defined in Table 2.1

Parameter	Description
V_{gs0}	gate-source voltage where extraction was performed
V_{ds0}	drain-source voltage where extraction was performed
v_{fcg}	used to offset the center point around which limiting occurs
f_{c1}	used to determine how quickly limiting is applied
f_{c2}	used to how much of an effect V_{in} has on limiting
c_{v1}	used to scale scale capacitance from extrapolation point V_{ds0} to operating point V_{out}

Table 2.1: Parameters for c_{gs} equation

More complex implementations would also include the gate-source leakage current but it has been omitted here. The omission was made because the preliminary charaterization of the HFET showed gate currents under 5% of the applied drain current. In most cases the leakage current was well below 2% of the drain-source current. Accurate characterization of the input capacitances and resistances of the device is required to ensure that the input impedance is accurately characterized.

2.3.2 Gate-drain region

The gate-drain region's effects are modelled using c_{gd}. The gate-drain capacitance (c_{gd}) varies in proportion to the physical distance between the gate and drain. The capacitor c_{gd} is defined as a non-linear capacitor with the capacitance given as (2.2) in [17].

$$c_{gd}(V_{in}, V_{out}, T) = c_{gd}(T)\left(\frac{1 + c_{v2}V_{in}^2}{1 + c_{v2}V_{gs0}^2}\right)\left(\frac{1 - f_{c3}\tanh(f_{c4}V_{out})}{1 - f_{c3}\tanh(f_{c4}V_{ds0})}\right). \tag{2.2}$$

where the parameters of the capacitance equation are as defined in Table 2.2

Parameter	Description
V_{gs0}	gate-source voltage where extraction was performed
V_{ds0}	drain-source voltage where extraction was performed
f_{c3}	used to determine how quickly limiting factor is applied
f_{c4}	Used to determine how much of an effect V_{out} has on the limiting factor
c_{v2}	used to scale scale capacitance from extrapolation point V_{gs0} to operating point V_{in}

Table 2.2: Parameters for c_{gd} equation

2.3.3 Active region

Perhaps the most crucial part of the compact model is the drain-source active region, which is comprised of r_{ds0}, c_{ds} and I_{ds}. The parallel combination of r_{ds0} and c_{ds} is included to model the output impedance of the device, whose accurate characterization is crucial in any PA design. However, in class-F PA design, accurate characterization of the output capacitance is exceedingly crucial as this value is used in computing the required harmonic terminations.

The output current source is used to model the device's current characteristic and, by extension, the transconductance. The equation that defines the output current is

$$I_{ds} = (A_0(T) + A_1(T)V_1 + A_2(T){V_1}^2 + A_3(T){V_1}^3) \cdot \tanh(\gamma V_{out}(t))(1 + \lambda V_{out}(t)), \quad (2.3)$$

where

$$V_1 = V_{in}(t - \tau)[1 + \beta(V_{ds0} - V_{out}(t))], \quad (2.4)$$

and γ is the drain current saturation parameter, λ is used to control I_{ds} when in saturation, τ is the time delay of the device, and β is used to describe the pinch-off dependence on the output voltage [11]. $V_{out}(t)$ is also included in these equations as the drain source current is a function of that same voltage. In this case t refers to time and not temperature. All of the A coefficients are polynomial coefficients that are used to fit the current characteristic over the linear region into both the pinch off and saturation regions. This coefficients can be used as functions of temperature and interpolation that defines the temperature dependence of these coefficients can be performed linearly or using spline fitted coefficients to avoid discontinuous temperature behaviour near the breakpoints.

2.3.4 Drain current limiting

One of the drawbacks of the model in [11] is that the pinch-off behaviour of an HFET can not be accurately modeled. Standard simulators such as ADS simply limit the output current to its minimum value. This prevents the problem of large output currents for negative gate voltages. This does not remove the effect of the DC path, which leads to a simulated current flowing that is greater than it should be. This is

due to the DC path between the drain and source of the device.

To compensate for this the current equation was initially scaled in a piece-wise continuous method over three ranges defined as follows.

1. $V_1 > V_{int}$
2. $V_p < V_1 \leq V_{int}$
3. $V_1 \leq V_p$

Where V_{int} is defined as the lowest value of V_1 that still yields I_{DS} curves that are similar to the measured data. V_p is the pinch-off voltage and V_1 is as described in (2.4).

Over the range labelled 1) the current source was configured to behave as described in (2.3), which is the normal region of operation. The range labelled 2) has the drain source current defined as

$$I_{ds} = \alpha \cdot I_{ds}(V_{int}) - (1-\alpha) I_{leak,unscaled} \tag{2.5}$$

where,

$$\alpha = \frac{(V_1 - V_p)}{(V_{int} - V_p)}, \tag{2.6}$$

$$I_{leak,unscaled} = V_{ds}/r_{ds0} \tag{2.7}$$

and $I_{ds}(V_{int})$ is the drain-source current when the device is biased at $V_1 = V_{int}$. Finally, over the range labelled 3) I_{ds} was computed to oppose the current due to the

DC path using (2.8), resulting in an output current of 0 A.

$$I_{ds} = -(V_{ds}/r_{ds0}) \tag{2.8}$$

The result was a model that supported modeling of pinch-off behaviour in the HFET for simple cases. The model achieved convergence when performing DC simulations and small-signal s-parameter simulations. However, during harmonic balance (HB) simulations it was not possible to get the model to converge for large input signals due to the piecewise nature of the I_{ds} equation. To resolve this issue, continuous equations were sought to achieve the same result without causing convergence issues.

The equation in (2.4) was solved to obtain the pre-limited value of V_1. This value is then limited to V_p for all $V_1 < V_p$, using the following equation.

$$V_{1,limited} = V_p + \phi \cdot (1 - \tanh(\xi \cdot (V_p - V_{gs} + \psi))) \cdot (-V_p + V_1) \tag{2.9}$$

Parameter	Value	Description
ξ	15	Eccentricity that determines how quickly limiting occurs
ϕ	0.5	Offset to move function centered around 0 to 0.5
ψ	0.1	$V_{1,limited}$ adjustment factor

Table 2.3: Parameters for V_1 limiting equation

Using (2.9) and the values listed in Table 2.3, the limited value of V_1 is shown in Figure 2.2 for $V_{ds} = 8$ V and $V_p = -2.5$ V

With the value of V_1 limited, the next step was to impose a similar form of limiting to the drain source output current. This is because the cubic fit does not apply over

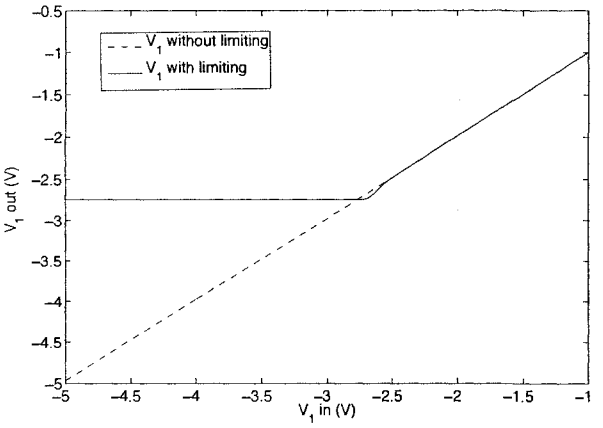


Figure 2.2: V_1 limiting factor

all ranges. When using the model described in [11], in the presence of large input voltages it is not uncommon to see the drain current increase dramatically for large negative voltages at the gate. I_{ds} was computed as described in (2.3). This was then limited by applying a limiting factor as shown below.

$$I_{ds,limited} = I_{ds} \cdot \phi \cdot (1 - \tanh(\xi \cdot (V_p - V_1 + \psi))) \tag{2.10}$$

Parameter	Value	Description
ξ	10	Eccentricity that determines how quickly limiting occurs
ϕ	0.5	Offset to move function centered around 0 to 0.5
ψ	0	$I_{ds,limited}$ adjustment factor

Table 2.4: Parameters for equation (2.10)

Using (2.10) and the values listed in Table 2.4, the limited value of I_{ds} is shown in Figure 2.3 for $V_{ds} = 8$ V.

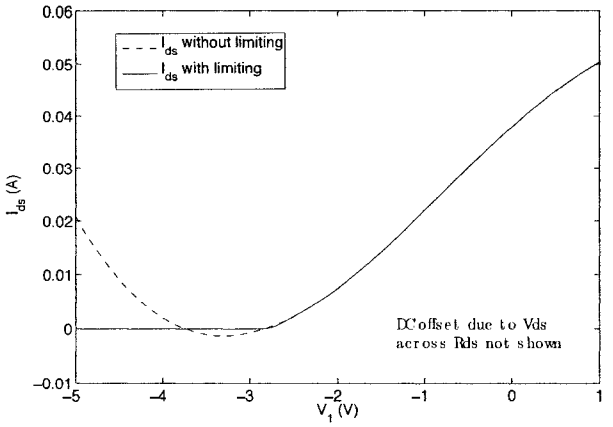


Figure 2.3: I_{ds} limiting factor

Up to this point the current from the DC path is still present. To remove this effect, the value of all I_{ds} computations was offset by $-(V_{ds}/r_{ds0})$. Since every I_{ds} point would end up being offset by this value, the measured data was offset be the same amount in the opposite direction (*i.e.* $+(V_{ds}/r_{ds0})$). This method effectively models pinch-off behaviour in the HFET.

2.3.5 Temperature dependence

The output current source incorporates the temperature dependence described in [11]. However, due to the inability to characterize the device isothermally the A_i table from [11] and a corresponding table of cubic spline coefficients has been built into the model to serve as placeholders for valid data. Since there was no representative data, a method disabling the modelling of self-heating effects in the model was required. A parameter was included that allowed for the selection of the I_{ds} mode of operation. There were three modes of operation that could be used to determine the

A_i coefficients in the Curtice cubic equation: cubic spline-interpolated coefficients, linear interpolation, and constant coefficients (*i.e.* not functions of temperature).

Due to the fact that the temperature effects of any device can only be characterized over a finite range of temperatures, a strategy was required to account for temperatures outside of the characterized range. In the event that a temperature outside of the characterized range is encountered, linear extrapolation is used and a warning is issued in the simulator status window. When linear extrapolation is used, it is based on the two nearest known temperature points. This is the case regardless of the I_{ds} mode that is specified, excluding the constant case in which the A_i coefficients remain the same regardless of temperature.

When cubic spline interpolation is selected, the A_i for a given temperature are determined by using a set of pre-computed cubic spline coefficients for each of the four A_i in (2.3). These spline coefficients are functions of temperature and are hardcoded in four look-up tables (LUTs). The cubic spline coefficients for each A_i are used to interpolate between the two nearest characterized temperature points that bracket the current temperature. In cases where the characterized temperature points are far from linear, this method will result in faster simulation times and more robust convergence due to the continuous nature of the spline interpolated temperature coefficients.

When the mode selected is linear interpolation, the A_is for a given temperature are determined by using

$$A_i(T) = A_i(T_0) + [A_i(T_1) - A_i(T_0)] \left(\frac{T - T_0}{T_1 - T_0} \right) \tag{2.11}$$

Where T is the current operating temperature, T_0 is the nearest characterized tem-

perature that is less than T, and T_1 is the nearest characterized temperature that is greater than T. The values of $A_i(T_0)$ and $A_i(T_1)$ are read from a hardcoded look-up-table (LUT) containing the A_i coefficients that were extracted for several known temperatures.

2.3.6 Self-heating effects

Self-heating describes how a device's characteristics change with temperature, where the temperature is unique for each operating point. In bipolar junction transistors (BJT) this can lead to thermal runaway as the conductance of the BJT increases with temperature and temperature increases with current, resulting in a positive feedback loop. With GaN HFETs the opposite is true; as temperature increases the conductance decreases because the electron mobility decreases [18]. This is what leads to the decrease in output current as a device is pushed further and further into the saturation region of operation.

To accurately characterize the thermal behaviour of the device, a series of isothermal measurements is required. These are completed using a heated chuck to characterize the device's behaviour at several different temperatures with pulsed current measurements. These pulsed measurements are made using small enough pulse durations and long duty cycles to ensure that the temperature of the device does not increase due to self-heating. This was not possible during the given time-frame for this work. For this reason the temperature related behaviour of the device is not currently modeled although the functionality is included in the model.

The sub-circuit used to model channel temperature is the common implementation shown in Figure 2.4 [11]. This sub-circuit models self-heating by determining the

channel temperature of the device based on the instantaneous power being dissipated. The current source labelled P_{diss} generates a current that is equal to the power being dissipated. Combining P_{diss} with a thermal resistance generates a voltage difference from the T_{amb} node to the T_{chan} node. This voltage difference corresponds to the temperature increase of the channel over ambient in degrees Centigrade. The thermal capacitor, C_{therm}, is included to model the thermal time constant.

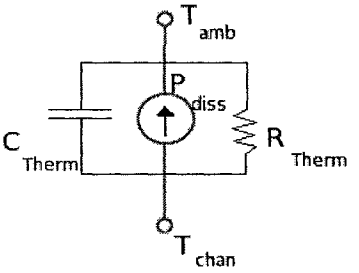


Figure 2.4: Thermal sub-circuit

2.3.7 RF dispersion effect

RF dispersion is a phenomenon that is common to all AlGaN/GaN FETs. RF dispersion is the name given to the phenomena that results in reduced transconductances when operating at RF frequencies when compared to the same device operating at its DC equivalent. The mechanism that causes this reduced transconductance is a result of hot carriers that temporarily become trapped in the AlGaN-GaN interlayer. This trapped charge effectively creates a virtual gate that works against the existing gate reducing device transconductance [19]. Since these trapping sites do not exist in the same manner in CMOS devices RF dispersion is not a problem for these devices.

The ability to model RF dispersion was built into the model using the three com-

ponent sub-circuit that is made up of I_{rf}, r_{rf}, and c_{rf} shown in Figure 2.1. A corner frequency for the RF dispersion branch is created by the resistor (r_{rf}) and capacitor (c_{rf}), above which the RF current source appears in parallel with the main I_{ds} current source. Below the corner frequency the RF current source is effectively shorted out, having no effect on drain current.

The current source is defined in a similar fashion as (2.3) but with different coefficients and effectively operating in the opposite direction (by sourcing a negative current) effectively causing a reduction in drain-source current. The $A_{i,rf}$ coefficients used in the polynomials are different than the A_i coefficients used by the main output current source whose governing equations are shown in (2.12) and (2.13).

$$A_{i,rf} = (\delta_{gm} - 1)g_m \quad \text{for } i = 1, 2, 3, \tag{2.12}$$

$$A_{0,rf} = -(A_{1,rf}V_p + A_{2,rf}V_p^2 + A_{3,rf}V_p^3), \tag{2.13}$$

where δ_{gm} is used to adjust the magnitude of the reduction in transconductance.

Since the device was characterized at the frequency of interest, the dispersion was not characterized. Modeling of RF dispersion can effectively be turned off by setting c_{rf} to a small value so that its impedance becomes very large and negligible amounts of signal from i_{rf} can oppose i_{ds}. Furthermore, a small value for r_{rf} can be used to push the corner frequency of the RF dispersion to well outside of the frequency of operation.

Chapter 3

Device Parameter Extraction Techniques

This chapter discusses the measurement techniques used to determine the values of parameters in the model that was used. In addition to the extraction methods used, this chapter will present the final values used when simulating the model.

3.1 Extrinsic resistance extraction technique

K. Lee *et al.* in [20] present a measurement technique of extracting the extrinsic resistances of a device. The technique involves biasing the gate and source of a transistor while leaving the drain terminal floating. The drain can then be used as a voltage probe, as shown in Figure 3.1. I_{DS} is chosen such that $V_{DS} << V_{BI} - V_G$, where V_{BI} is the built-in potential of the Schottky junction, to ensure that the charge distribution under the gate as a result of the gate current is not significantly affected by the applied drain current. The current distribution under the gate can be assumed

to be constant along the width of the gate but varies with the length. Using the simplified circuit shown in Figure 3.1, it can be determined that

$$V_{DS} = V_S + I_{GS}(R_S + \alpha \cdot R_{CH}) + I_{DS}(R_S + R_D + R_{CH}) \tag{3.1}$$

where α is a constant used to account for the fractional R_{CH} that is seen when looking into the gate. This fractional R_{CH} is a result of the increasing current density as $x \rightarrow 0$ in Figure 3.1 (*i.e.* going from source to drain).

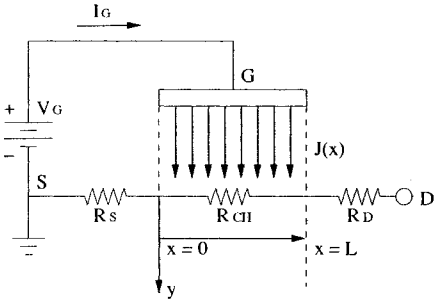


Figure 3.1: "End" resistance measurement technique (based on [21])

Lee *et al.* go on to show that α is constant with gate current provided that I_G does not exceed the theoretical drain to source current that will result in a relatively linear distribution of charge under the gate (I_T), which is defined as

$$I_T = \left(\frac{nkT}{q}\right)\frac{1}{R_{CH}}. \tag{3.2}$$

Where n is the diode ideality factor. An upper limit on R_{CH} can be determined using (3.2) and the maximum gate current in the measurement ($I_{G,max}$). $I_{G,max}$ and n in this work were 0.5 mA and 1.28, respectively. The value of n was determined from the slope of Figure 3.3 (a). Determination of n is described further on in this section.

The computation of the upper limit of R_{CH} for $I_{G,max} = 0.5$ mA and $n = 1.28$ follows.

$$0.5 \text{ mA} = I_{G,max} \leq I_T = \left(\frac{nkT}{q}\right)\frac{1}{R_{CH}} \tag{3.3}$$

$$65.8\ \Omega \geq R_{CH} \tag{3.4}$$

which will be the case with any device of reasonable gate width to be used in high power amplifier (HPA) design. By extension we can say that the assumption on α is valid for $I_{G,max}$ used in this work.

By plotting V_{DS} as a function of I_G for several constant values of I_{DS} two important resistances can be extracted. These resistances are the total drain to source resistance (R_T) and the source end-resistance (R^S_{END}), which are both explained below. A plot of V_{DS} *vs.* I_G for the device being characterized is shown in Figure 3.2.

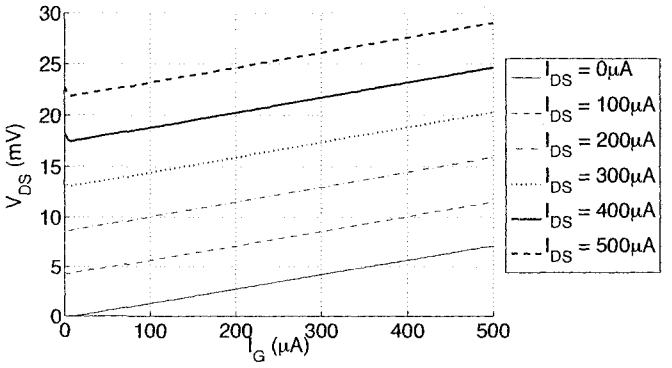


Figure 3.2: Source end-resistance measurement results

As discussed in [21], the slopes of the lines described above are equivalent to

$$\frac{dV_{DS}}{dI_G} = \frac{R_{CH}}{2} + R_S \equiv R^S{}_{END}. \tag{3.5}$$

The y-intercepts for each I_{DS} line yield a second equation as shown in (3.6).

$$V_{DS}|_{I_G=0} = I_D(R_T) \tag{3.6}$$

where the total drain to source resistance R_T is defined as,

$$R_T = R_S + R_D + R_{CH} \tag{3.7}$$

From this measurement the values for $R^S_{END} = 14.4\ \Omega$ and $R_T = 43.5\ \Omega$ shown in Table 3.1 were extracted. R^S_{END} was extracted using (3.5) and the $I_{DS} = 0$ A line in Figure 3.2. R_T was extracted using the y-intercepts of the non-zero I_{DS} lines shown in Figure 3.2 by dividing out the constant, non-zero drain currents.

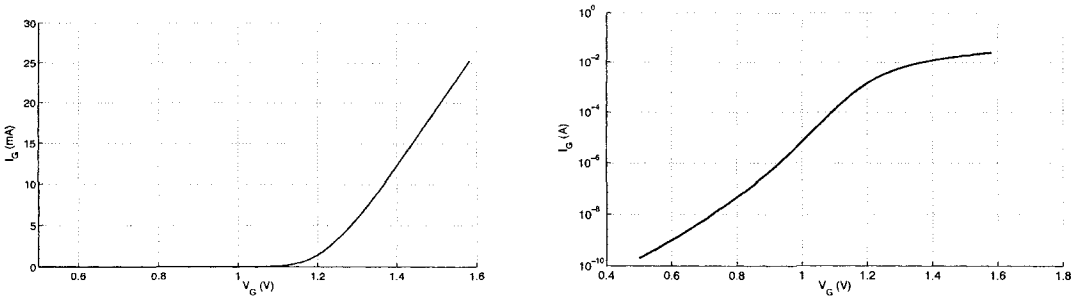
To solve for the three extrinsic resistors R_S, R_D and R_{CH}, a third dataset and equation were required. The equation for the open-channel resistance (R_{OPEN}), which is defined as

$$R_{OPEN} = R_S + R_D \tag{3.8}$$

will allow for the extraction of R_{CH} provided that a dataset for R_{OPEN} is obtained. This is because $R_T - R_{OPEN} = R_{CH}$ [22]. Before R_{OPEN} can be determined, prior knowledge of the built-in potential (V_{bi}) and the pinch-off voltage (V_p) are required. Both of which were obtained as described in the two following paragraphs.

V_{bi} was obtained by shorting the drain and source terminals then measuring the current characteristic of the Schottky diode that results from the gate contacting the active region. The data was then plotted on a linear scale, as shown in Figure 3.3 (a), and $V_{bi} = 1.2$ V was then determined by performing a linear extrapolation of the

data over the saturation region of the diode back to the x-axis.



(a) linear scale

(b) logarithmic scale

Figure 3.3: Schottky diode characteristic

V_p of the transistor was obtained by plotting I_{DS} as a function of V_{GS} for several V_{DS}, as shown in Figure 3.4. The linear portion of the curve (between -2.4 and 2 V) was then extrapolated back to the x-axis to obtain $V_p = -2.5$ V.

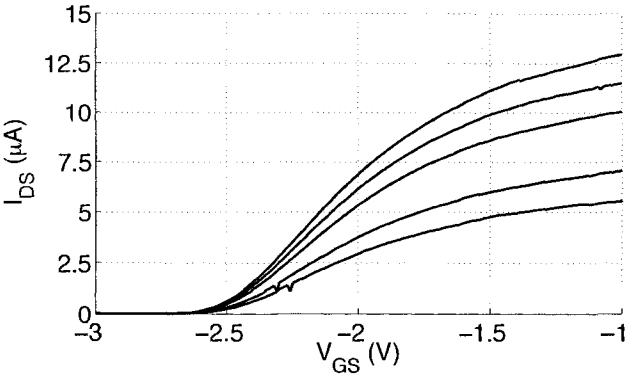


Figure 3.4: DC current characteristic in the linear region of operation when acting as a diode

n was obtained by plotting the same data shown in Figure 3.3.(a) on a logarithmic scale, as shown in Figure 3.3.(b). The slope of the linear region on the logarithmic plot was then calculated to yield $n = 1.28$.

Once the values of V_{bi} and V_p were known the value of R_{OPEN} was extracted by plotting the total drain to source resistance (R_T), which is defined as

$$R_T = dV_{DS}/dI_{DS} \tag{3.9}$$

as a function of X, which Fukui defines in [22] as

$$X = \left[1 - \sqrt{\frac{V_{bi} - V_{GS}}{V_p + V_{bi}}}\right]^{-1} \tag{3.10}$$

R_{OPEN} was then determined by extrapolating the R_T line back to the y-axis, at which point $R_{CH} \rightarrow 0$ and the remaining offset is $R_D + R_S$, as shown in Figure 3.5. The extrapolation is required because it is not physically possible to apply so large a forward bias to the gate that the channel resistance reduces to 0 [22].

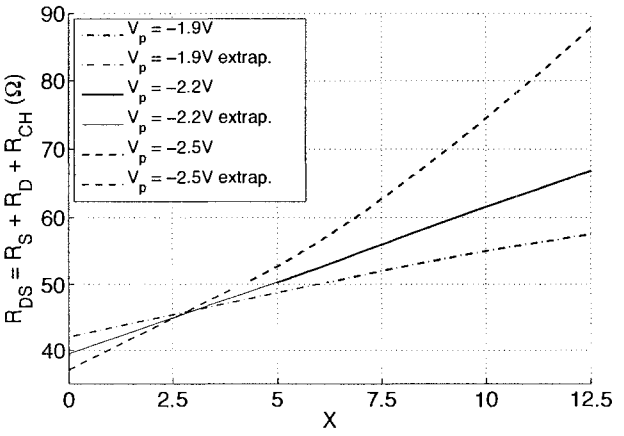


Figure 3.5: Open channel resistance plot as a function of X

Having measured results for R_T, R^s_{END} and R_{OPEN} the individual resistor values for R_D, R_S, and R_{CH} were found by solving the three following equations in three

unknowns:

$$R_T = R_S + R_D + R_{CH} \tag{3.11}$$

$$R^S_{END} = \frac{R_{CH}}{2} + R_S \tag{3.12}$$

$$R_{OPEN} = R_D + R_S, \tag{3.13}$$

which were extracted to be 43.5, 14.4, and 38.1 Ω, respectively. From the system of equations shown above the following three equations were used to determine each of the three resistances.

$$R_{CH} = R_T - R_{OPEN} \tag{3.14}$$

$$R_S = R^S_{END} - \frac{R_T - R_{OPEN}}{2} \tag{3.15}$$

$$R_D = R_T - R_S - R_{CH}. \tag{3.16}$$

The extracted resistances based on (3.14) through (3.16) were $R_{CH} = 11.7\ \Omega$, $R_S = 5.5\ \Omega$, $R_D = 26.4\ \Omega$, which are summarized in Table 3.1.

With the extrinsic resistances of R_S, R_D, and R_{CH} successfully extracted the value of R_G was then determined by plotting dV_{GS}/dI_G as a function of $1/I_G$, as shown in Figure 3.6.

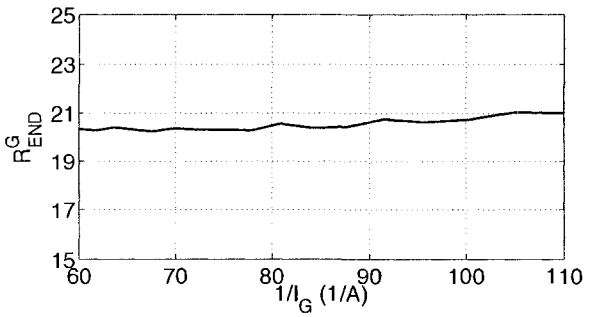


Figure 3.6: Gate end-resistance plot as a function of $1/I_G$

dV_{GS}/dI_G is plotted as a function of $1/I_G$ to extract R^G_{END} since

$$\frac{dV_{GS}}{dI_G} \equiv R^G{}_{END} \approx \frac{R_{CH}}{3} + R_S + R_G + \frac{nV_T}{I_G}. \tag{3.17}$$

$R_G = 7\Omega$ was obtained from $R^G_{END} = 20.5\Omega$, which is recorded in Table 3.1.

3.1.1 Section summary

Using the methods described in this section the extrinsic resistances recorded in Table 3.1 were extracted for the $100\mu m$ Nitronex GaN HFET used in this work

Resistor	Extracted Value (Ω)
R^S_{END}	14.4
R_T	43.5
R_G	7
R_D	26.4
R_S	5.5
R_{CH}	11.7

Table 3.1: Extracted extrinsic resistances

3.2 Extrinsic capacitance extraction technique

A compact model isolating the extrinsic capacitances, as shown in Figure 3.7, can be applied if the device is biased such that its channel is empty of any significant amount of charge [11]. This was achieved by biasing V_{GS} significantly lower than the pinch-off voltage, while applying a DC short to the drain and source. The fringing capacitance, denoted c_b, that results from the drain and source regions of charge's proximity to the gate was also determined from this measurement.

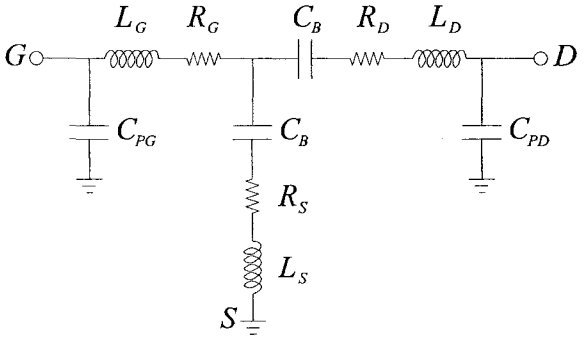


Figure 3.7: Small-signal equivalent model in [11] at pinch-off and $V_{DS} = 0V$

Since the extrinsic inductors present a comparatively small admittance and the effect of the resistors is purely real, the admittance parameters of Figure 3.7 yield the extrinsic capacitances. Knowing this the imaginary part of the admittance parameters were reduced to

$$\Im\{y_{11}\} = \omega(C_{PG} + 2 \cdot c_b), \tag{3.18}$$

$$\Im\{y_{12}\} = \Im\{y_{21}\} = -\omega c_b, \tag{3.19}$$

$$\Im\{y_{22}\} = \omega(c_b + C_{PD}). \tag{3.20}$$

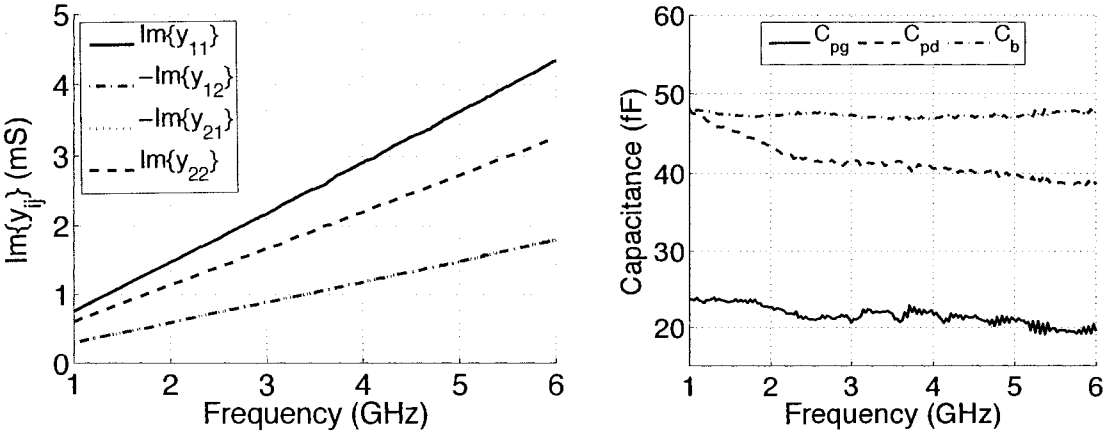
The resulting three equations in three unknowns are then solved to obtain the equations of the fringe, gate and drain capacitances as shown below

$$C_b = \frac{-\Im\{y_{12}\}}{\omega}, \tag{3.21}$$

$$C_{PG} = \frac{\Im\{y_{11}\}}{\omega} - 2 \cdot c_b, \tag{3.22}$$

$$C_{PD} = \frac{\Im\{y_{22}\}}{\omega} - c_b. \tag{3.23}$$

Figure 3.8.(a) shows the measured admittance parameters at a bias point of $V_{GS} = -4.5$ V and $V_{DS} = 0$ V. Using this plot the extracted capacitances were calculated using (3.21) through (3.23) and plotted as functions of frequency, as shown in Figure 3.8.(b).



(a) Imaginary part of y-parameters

(b) Extracted extrinsic capacitances

Figure 3.8: Extraction results for cold-FET measurement ($V_{GS} = -4.5\ V$, $V_{DS} = 0\ V$)

The final values for extrinsic capacitors that were extracted are summarized in Table 3.2.

Capacitor	Extracted Value (fF)
C_{PG}	21
C_{PD}	40
c_b	47.5

Table 3.2: Extracted extrinsic capacitor values

3.3 Extrinsic inductor extraction technique

To isolate the extrinsic inductors the channel was biased with its channel conductance maximized by applying a large positive voltage to the gate while applying a short between the drain and source terminals. An equivalent circuit for the gate region of an HFET at such a bias point is shown in Figure 3.9. The intrinsic device, when biased as above, can be easily expressed as the set of z-parameters, which are listed below [23]:

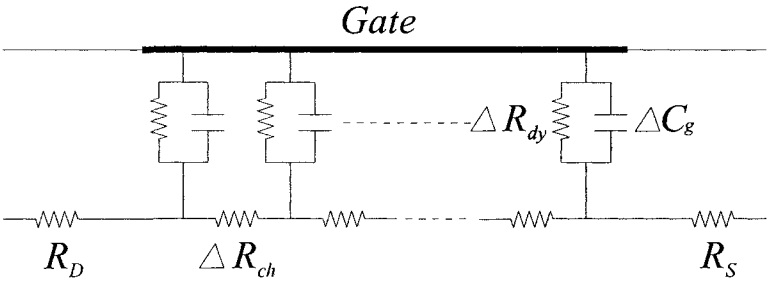


Figure 3.9: Small-signal equivalent model of an HFET when heavily forward biased with $V_{DS} = 0\ V$ [23].

$$z_{11} = \frac{R_{CH}}{3} + \frac{R_{dy}}{1 + j\omega C_g R_{dy}}, \tag{3.24}$$

$$z_{12} = z_{21} = \frac{R_{ch}}{2}, \tag{3.25}$$

$$z_{22} = R_{ch}, \tag{3.26}$$

where

$$R_{dy} = \frac{nkT}{qI_G} = \frac{nV_T}{I_G}. \tag{3.27}$$

The input impedance at such a bias point described above is given by

$$z = \alpha_g R_{CH} + z_{dy} \tag{3.28}$$

where z_{dy} is the last term in (3.24) and α_g. α_g is shown in [20] to be 1/3 for low values of I_g and $V_{DS} << 1$ V.

Including the extrinsic resistors and inductors the intrinsic z-parameters expand to

$$z_{11} = \frac{R_{CH}}{3} + \frac{R_{dy}}{1 + j\omega c_{gs} R_{dy}} + R_S + R_D + j\omega(L_S + L_G), \tag{3.29}$$

$$z_{12} = Z_{21} = \frac{R_{CH}}{2} + R_S + j\omega L_S, \tag{3.30}$$

$$z_{22} = R_{CH} + R_S + R_D + j\omega(L_S + L_D). \tag{3.31}$$

To simplify (3.29), Dambrine *et al.* in [23] make the assumption that z_{dy} tends to R_{dy} for current densities on the order of $5 \cdot 10^7 - 10^8 A/m^2$ in GaAs devices. A similar assumption can be made for GaN devices since the only material specific property of R_{dy} is n, which has been shown to be similar for GaAs and GaN. The value of n for the device being used was shown to be ≈ 1.28 in Section 3.1, which is suitably close to typical GaAs ideality factors which range from 1 to 2 [24].

The extrinsic inductors were extracted from the z-parameters of the device biased as described above. Given the z-parameters of a device at such an operating point,

the extrinsic inductors are defined by the following three equations:

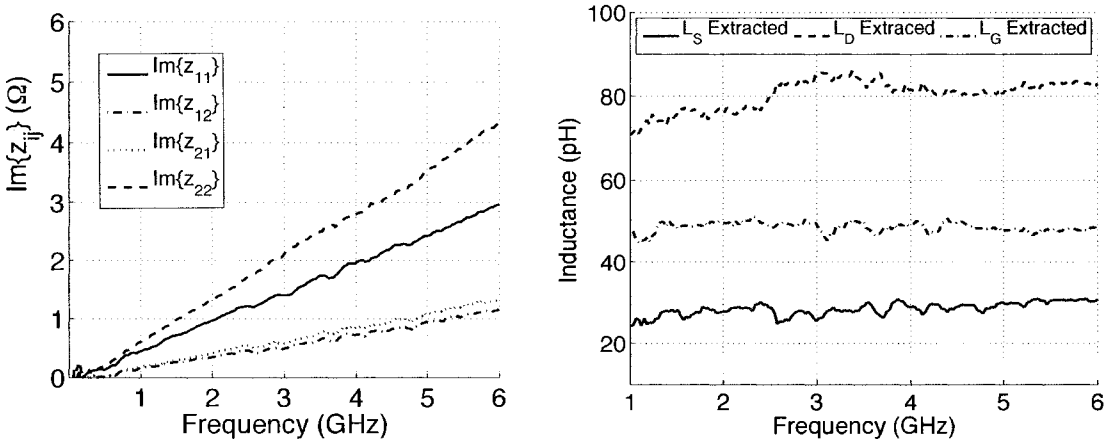
$$L_S = \frac{\Im\{z_{12}\}}{\omega}, \tag{3.32}$$

$$L_D = \frac{\Im\{z_{22}\}}{\omega} - L_S, \tag{3.33}$$

$$L_G = \frac{\Im\{z_{11}\}}{\omega} - L_S. \tag{3.34}$$

Before the extrinsic inductors were extracted, the effects of the extrinsic capacitors were de-embedded from the measurement data using the standard method described in Section 3.4.

Figure 3.10(b), which shows the extracted values as functions of frequency, was created by applying equations (3.32) through (3.34) to the data in Figure 3.10(a).



(a) Imaginary part of z-parameters

(b) Extracted extrinsic inductances

Figure 3.10: Extraction results for heavily forward biased HFET ($V_{GS} = 1\ V$, $V_{DS} = 0\ V$) measurement

3.3.1 Section summary

The final inductor values that were extracted are listed in Table 3.3.

Inductor	Extracted Value
L_G	49.3 pH
L_D	86.4 pH
L_S	25.7 pH

Table 3.3: Extracted extrinsic inductor values

3.4 De-embedding technique

With the extrinsic component values known, their effects could be de-embedded from device measurements, thereby isolating the characteristics of the intrinsic device. The de-embedding process was started by converting the s-parameters to y-parameters and removing the extrinsic capacitors' effects as shown in (3.35).

$$\begin{bmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{bmatrix} \rightarrow \begin{bmatrix} y_{11} - j\omega C_{PG} & y_{12} \\ y_{21} & y_{22} - j\omega C_{PD} \end{bmatrix} \tag{3.35}$$

The resulting matrix was then converted to z-parameters and the remaining series extrinsic components were de-embedded as shown in (3.36).

$$\begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \rightarrow \begin{bmatrix} z_{11} - R_S - R_G - j\omega(L_G + L_S) & z_{12} - R_S - j\omega L_S \\ z_{21} - R_S - j\omega L_S & z_{22} - R_S - R_D - j\omega(L_D + L_S) \end{bmatrix} \tag{3.36}$$

The final matrix was then converted back to the intrinsic device's y-parameters which are shown in (3.37) from [25].

$$Y_{intrinsic} = \begin{bmatrix} \frac{r_{gs}c^2{}_{gs}\omega^2}{D} + j\omega\left(\frac{c_{gs}}{D} + c_{gd}\right) & -j\omega c_{gd} \\ \frac{g_m e^{-j\omega\tau}}{1+jr_{gs}c_{gs}\omega} - j\omega c_{gd} & g_d + j\omega(c_{ds} + c_{gd}) \end{bmatrix} \tag{3.37}$$

where

$$D = 1 + \omega^2 c^2{}_{gs} r^2{}_{gs} \tag{3.38}$$

With a set of de-embedded y-parameters it was possible to extract the intrinsic elements of the compact model shown in Figure 2.1.

3.5 Intrinsic components extraction technique

Equation (3.37) can be simplified at frequencies low enough that the non-unity term in (3.38) is much less than 1 [25], which was verified to be the case for the frequency of interest (*i.e.* 3GHz). At low frequencies the second term in (3.38) tends to 0, resulting in $D \rightarrow 1$. This simplifies the y-parameters in (3.37) to

$$Y_{intrinsic} = \begin{bmatrix} r_{gs}c^2{}_{gs}\omega^2 + j\omega(c_{gs} + c_{gs}) & -j\omega c_{gd} \\ g_m - j\omega(c_{gd} + g_m(r_{gs}c_{gs} + \tau)) & g_d + j\omega(c_{ds} + c_{gd}) \end{bmatrix}. \tag{3.39}$$

The intrinsic parameters were determined using the equations [23]

$$c_{gd} = \frac{\Im\{y_{12}\}}{-\omega}, \tag{3.40}$$

$$r_{gs} = \frac{\Re\{y_{11}\}}{c^2{}_{gs}\omega^2}, \tag{3.41}$$

$$c_{gs} = \frac{\Im\{y_{11}\}}{\omega} - c_{gd}. \tag{3.42}$$

The remaining three variables were extracted from the same set of intrinsic admittance parameters using the following equations:

$$g_m = \Re\{y_{21}\}, \tag{3.43}$$

$$\tau = \Im\{y_{21}\}, \tag{3.44}$$

$$g_d = \Re\{y_{22}\}. \tag{3.45}$$

It should be noted that the RF dispersion branch was omitted in this analysis because the extraction of the intrinsic elements was performed at the frequency of interest and g_m as a function of frequency is required to characterize the branch.

3.5.1 Notes on non-linear c_{gs} and c_{gd}

The method described in [25] and discussed above can be used to determine the values of c_{gs} and c_{gd} as functions of bias, which can be applied to small- and large-signal cases alike. The s-parameters were analyzed for several bias points so that many values could be selected from during the design phase when a circuit's operating point was known.

The equations used for c_{gs} and c_{gd} were (3.46) and (3.47), respectively [11].

$$c_{gs}(T) = (c_{gs} + c_{gsT}\Delta T)\left(\frac{1 + c_{v1}V_{out}}{1 + c_{v1}V_{ds0}}\right)\left(\frac{1 + f_{c1}\tanh[f_{c2}(V_{in} + v_{fcg})]}{1 + f_{c1}\tanh[f_{c2}(V_{gs0} + v_{fcg})]}\right) \quad (3.46)$$

$$c_{gd}(T) = (C_{GD} + c_{gdT}\Delta T)\left(\frac{1 + c_{v2}V^2{}_{in}}{1 + c_{v2}V^2{}_{gs0}}\right)\left(\frac{1 - f_{c3}\tanh(f_{c4}V_{out})}{1 - f_{c3}\tanh(f_{c4}V_{ds0})}\right) \quad (3.47)$$

When simulations were attempted using the bias dependent implementation of c_{gd} it was not possible to get simulations to converge. As a result c_{gd} was extracted based on the operating point and the value of c_{gd} was adjusted during each design iteration.

Chapter 4

Class-F PA Theory

This chapter presents background theory on the operation of class-F PAs. This includes how waveform shaping results in improved efficiencies as well as class-F PA power capabilities and efficiency equations.

4.1 Waveform shaping through harmonic terminations

Class-F PAs achieve their high efficiencies by operating under heavy gain compression and using a principle called harmonic termination. By properly terminating certain harmonics that result from operating under heavy gain compression, the efficiency of a PA can be increased dramatically. The increase in efficiency is a by-product of the shaping of the drain voltage and current waveforms that results from the harmonic terminations. The waveforms are shaped such that they are maximally flat, meaning that the derivatives of the waveforms are equal to 0 at the maxima and minima [26].

As the the number of harmonics in the waveform increases so does the highest order of the derivatives that is required to be 0 for said waveform to remain maximally flat.

In the case of a class-F PA the even harmonics are shorted in the voltage waveform leaving only odd voltage harmonics present at the drain. The odd harmonics in the current waveform are then presented with an open circuit leaving only even current harmonics present at the drain. As a result the voltage waveform is referred to as the odd waveform and the current waveform is referred to as the even waveform. The more harmonics that are terminated in such a fashion the more efficiently the PA performs. However, higher order harmonic termination become increasingly difficult to implement due to their high frequencies and efficiency increases occur at a diminishing rate of return.

4.1.1 Odd-waveform - drain voltage

As the number of odd harmonics increases in the voltage waveform the resulting shape is that of a square wave, as can be seen if Figure 4.1. Similarily, as the number of even harmonics increases in the current waveform the resulting shape is that of a half-sine wave that is 180 degrees out of phase with the voltage waveform. The result is, theoretically, no power dissipation and by extension 100% drain efficiency for an infinite number of properly terminated harmonics [27]. However, 100% drain efficiency is by no means practical.

In [26] Raab performs the analysis for the power output capabilities and limitations of the class-F PAs. Starting with the equation of a square wave for the drain voltage

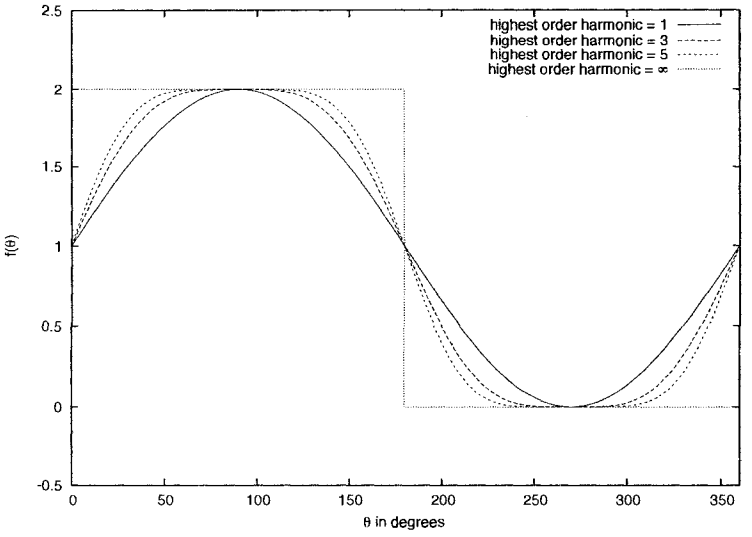


Figure 4.1: Waveforms with odd-harmonic content (based on [26])

and half-sine wave for the current, both in their Fourier forms.

$$v_d(\theta) = V_{DD} + V_1 sin\theta + V_3 sin3\theta + V_5 sin5\theta + ... \quad (4.1)$$

$$i_d(\theta) = I_{DC} - I_1 sin\theta - I_2 cos2\theta - I_4 cos4\theta - ... \quad (4.2)$$

From these two equations the weights of the harmonic components for maximal flatness can be determined.

To simplifiy the analysis Raab introduces the variables $\gamma_v, \gamma_i, \delta_v$ and δ_i. The γ terms are used to relate the fundamental-frequency component of the output voltage and current waveforms to their corresponding bias values. The δ terms are used to relate the peak drain voltage and current to the corresponding bias values. These

values are more clearly outlined in equations (4.3) through (4.6) [26].

$$\gamma_v = \frac{v_1}{V_{DD}}, \tag{4.3}$$

$$\delta_v = \frac{v_{D,max}}{V_{DD}}, \tag{4.4}$$

$$\gamma_i = \frac{i_1}{I_{DC}} \tag{4.5}$$

$$\delta_i = \frac{i_{D,max}}{I_{DC}}. \tag{4.6}$$

In a class-F PA the waveform containing the odd harmonics is the drain voltage waveform, which is described by (4.1). For the drain voltage to meet the maximally flat criteria the sinusoid's derivatives at the maximum and minimum phases of $\theta = \pi/2$ and $3\pi/2$, respectively, must be zero.

The most basic class-F PA uses third harmonic peaking. For third harmonic peaking, the third harmonic is the only in the odd waveform that is controlled at the drain. All other harmonics are shorted at the drain. To determine the maximally flat weights of the 1st and 3rd harmonics at least one derivative of (4.1) is required. The first derivative of (4.1) is

$$\frac{dv_d}{d\theta} = V_1 cos\theta + V_1 cos\theta + V_3 cos\theta + ..., \tag{4.7}$$

which is naturally zero at $\theta = \pi/2$ and $3\pi/2$, which are the two points of interest. By extension all odd derivatives of (4.1) are naturally zero at the maximum and minimum. Therefore, only the even derivatives require attention as they are the only ones that are not inherently zero.

The second derivative of (4.1), when only considering the third harmonic (*i.e.* third

harmonic peaking) is

$$\frac{d^2 v_d}{d\theta^2} = -V_1 sin\theta - 9V_3 sin\theta. \tag{4.8}$$

Setting the second derivative equal to 0 and substituting $\theta = 3\pi/2$ gives $V_3 = V_1/9$. By substituting V_3 in terms of V_1 into (4.1), which has been simplified to account for the presence of no harmonics higher than the third, will yield γ_v as shown below

$$v_d(\theta) = V_{DD} + V_1 sin\theta + V_3 sin3\theta \tag{4.9}$$

for $\theta = 3\pi/2$

$$\begin{aligned} 0 &= V_{DD} - V_1 + v_3 \qquad (4.10) \\ 0 &= V_{DD} - V_1 + V_1/9 \\ \frac{V_1}{V_{DD}} &= \frac{9}{8} = \gamma_v \end{aligned}$$

The weight for the third harmonic can then be found by isolating V_3 in (4.10) which results in

$$\frac{V_3}{V_{DD}} = \frac{1}{8}. \tag{4.11}$$

Using this weight, the plot labelled to "highest odd-order harmonic equalling 3" in Figure 4.1 was generated.

To find the maximum output voltage that will be used when computing the theoretical efficiencies the same starting of (4.1) is used. Then evaluating at $\theta = \pi/2$ and making the substitutions of both V_0 and V_3 in terms of V_{DD} yields $v_{D,max} = 2V_{DD}$ or $\delta_v = 2$.

This analysis can be extended to higher order class-F designs. This is achieved by computing higher-order even derivatives of the voltage waveform then applying the constraints for maximal flatness and solving for the weighting factors of the harmonics. In the extreme case of every odd-harmonic being properly terminated Krauss *et al.* in [28] show, through Fourier analysis, that the result is a square wave as is shown in Figure 4.1 for the case labelled " *highest order harmonic* $= \infty$". For this case the fundamental output voltage as a ratio of the bias voltage is

$$\gamma_v = \frac{4}{\pi}. \tag{4.12}$$

4.1.2 Even-waveform - drain current

The coefficients for the even-waveform can be found in a similar fashion. Starting from (4.2) the first derivative can be computed as

$$\frac{di_D}{d\theta} = -I_1 cos\theta + I_2 sin2\theta + I_4 sin4\theta + ... \tag{4.13}$$

Since maximally flat waveforms require the derivative at $\theta = \pi/2$ to be 0 it is clear that odd-order derivatives of the even-waveform are naturally 0 at the point of interest. As a result it is only the even derivatives that require treatment. The second derivative of (4.2) is

$$\frac{d^2 i_D}{d\theta^2} = I_1 sin(\theta) + 4I_2 cos(2\theta) + 16I_4 cos(4\theta) + ... \tag{4.14}$$

Considering the first even harmonic and setting the left side of (4.14) to 0 yields the result $I_2 = I_1/4$. If the Fourier form of a half-sine wave is shortened to only

include the second even harmonic the following equation is achieved:

$$i_d(\theta) = I_{DC} + I_1 sin\theta - I_2 cos2\theta \tag{4.15}$$

Upon substituting I_2 in terms of I_1 at the phase of interest ($\theta = \pi/2$) into the preceeding equation the value of γ_i is isolated as follows:

$$0 = I_{DC} - I_1 + I_1/4 \tag{4.16}$$

$$\frac{i_1}{I_{DC}} = \frac{4}{3} = \gamma_i. \tag{4.17}$$

The remaining coefficient I_2 is determined by substituting γ_i back into (4.2) and solving at $\theta = \pi/2$ to get

$$\frac{I_2}{I_{DC}} = \frac{1}{3} \tag{4.18}$$

Using these weights, the curve labelled "*the highest order harmonic = 2*" in Figure 4.2 was obtained. By computing further even-order derivatives, it is possible to apply the preceding steps to obtain coefficients for waveforms having a higher even harmonic content.

In [26], Raab goes on to show that in the extreme case of all even-harmonics being preserved the result is a half-sine wave as shown in Figure 4.2. In this case the ratio of the fundamental output signal to the bias is

$$\gamma_i = \frac{\pi}{2}. \tag{4.19}$$

The maximum and minimum currents in such a waveform are also computed from the same starting point, that is to say equation (4.2). The waveform reaches its

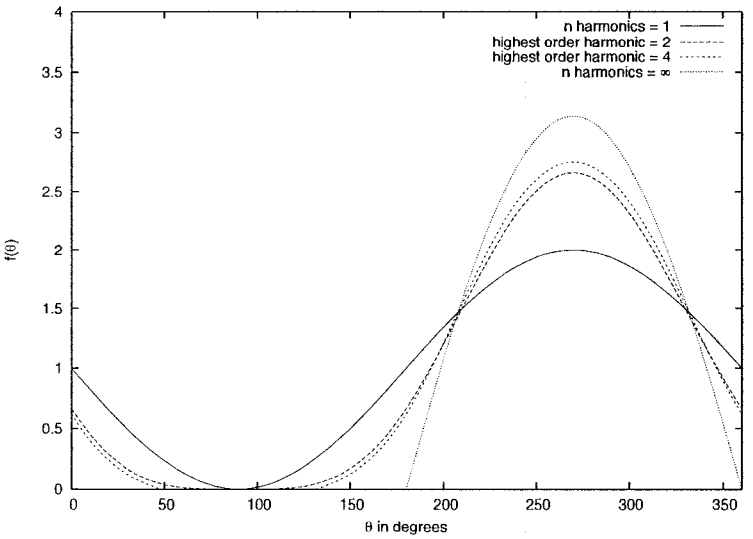


Figure 4.2: Waveforms with even-harmonic content (based on [26])

minimum at a phase of $\pi/2$, which is expressed as the following for a class-F PA with second harmonic peaking.

$$i_{d,min} = I_{DC} - I_1 + I_2 \tag{4.20}$$

If the values for I_1 and I_2 are substituted into (4.20) it becomes clear that the minimum drain current is zero.

The maximum current occurs at a phase of $3\pi/2$, which is the following for a class-F PA with second harmonic peaking,

$$i_{d,max} = I_{DC} + I_1 + I_2. \tag{4.21}$$

Again, if the values of I_1 and I_2 are substituted then $i_{d,max} = 8/3I_{DC}$, which was defined at the start of this section as $\delta_i = i_{d,max}/I_{DC}$.

Raab in [26] shows that this theory can be extended such that all even harmonics are included. The result for such a case is $\gamma_i = \pi/2$ and $\delta_i = \pi$, which corresponds to

a theoretical maximum current of $i_{d,max} = \pi I_{DC}$, while having $i_{d,min} = 0$.

4.2 Power output capability

To determine the power output capability, which Raab defines as the output power when $v_{d,max} = 1\ V$ and $i_{d,max} = 1\ A$ in [26] he starts with

$$P_{max} = \frac{P_o}{v_{d,max} i_{d,max}}. \tag{4.22}$$

Then by substituting γ and δ coefficients when possible he arrives at the equations

$$P_{max} = \frac{\eta}{\delta_v \delta_i} \quad \text{and} \tag{4.23}$$

$$P_{max} = \frac{\gamma_v \gamma_i}{2\delta_v \delta_i} \tag{4.24}$$

To further simplify (4.23) a method of organizing the δ terms in terms of γ is required. By computing the peak drain current $i_{d,max}$ when $i_{d,min} = 0A$ it can be shown that

$$i_{d,max} = 2I_1 = 2\gamma_i I_{DC}. \tag{4.25}$$

Then, through substitution of $I_1/I_{DC} = \gamma_i$ Raab obtains

$$\delta_i = 2\gamma_i. \tag{4.26}$$

As previously shown $\gamma_v = 2$. Both γ_i and γ_v can be substituted into (4.24) to arrive at

$$P_{max} = \frac{\gamma_v}{8}. \tag{4.27}$$

This shows that the output power capability of a class-F power amplifier is affected only by the odd-waveform (*i.e.* voltage waveform).

Assuming that the load at the fundamental is purely real and equal to R the output voltage and output current are related using Ohm's law as

$$V_1 = I_1 R \tag{4.28}$$

and output power can be determined as usual to be

$$P_O = \frac{V_1^2}{2R} = \frac{\gamma_v^2 V_{DD}^2}{2R} \tag{4.29}$$

4.3 Efficiency

To calculate efficiency, the average power consumed is required and is best expressed in terms of V_{DD} since P_O in (4.29) is in terms of this same variable. Such organization will allow the final equation for efficiency to be simplified in terms of the fundamental and bias voltages and current using the γ coefficients.

$$P_{DC} = V_{DD} I_{DC} = \frac{\gamma_v V_{DD}^2}{\gamma_i R} \tag{4.30}$$

The resulting efficiency can then be expressed as

$$\eta = \frac{P_O}{P_{DC}} \tag{4.31}$$

$$= \frac{\gamma_v \gamma_i}{2} \tag{4.32}$$

As is shown in (4.12) and (4.19) the ratios of fundamental output voltage and current to bias voltage and current are; $\gamma_v = 4/\pi$ and $\gamma_i = \pi/2$. Using these values in (4.32) results in the ideal class-F PA drain efficiency, from a theoretical standpoint, of 1.

More relevant to this work is the case of a third harmonic peaking PA. In this case $\gamma_v = 9/8$ and $\gamma_i = 1$, which yields a maximum theoretical efficiency of 88.4 %.

This chapter has shown how proper harmonic terminations can produce voltage and current waveforms at the drain of a class-F amplifier that do not overlap. Indicating that, at least from a theoretical standpoint, class-F PAs can have 100% efficiency.

Chapter 5

Class-F PA design and simulation

This chapter presents the design methodology that was used in the design process for this work. Following the design procedure simulation results are presented for both small and large signal measurements. Since this work was an exercise in modelling the purpose of the PA being designed was to validate the model that was implemented. As a result there were no goals for the PA from the outset beyond providing a method of validating the model that was more complex than small-signal analysis.

5.1 Bias selection

When selecting a bias point for a class-F PA there are several things to consider. The PA is to be operated in compression so that the required harmonic content is present. Otherwise the harmonic terminations that give the class-F PA its efficiency will not be used. Therefore, biasing the PA in a conservative region such as deep class-AB will ensure a higher efficiency for lower input signals. This comes at a cost to power output capability, which in this work, will be limited by the size of the device. For

this reason deep class-AB, or such that the HFET is on for slightly more than 50% of the RF cycle, was chosen for this PAs bias point.

Although the device used during the design was actually a 100 μm HFET pulsed-IV data for a known 2 mm device was used to obtain isothermal data. The pulsed-IV curves for a 2mm device on the same die as the 100 μm device used in this work were provided by Nitronex. The 2 mm device's data points were scaled by a factor of $\frac{1}{20}$ to relate them to the 100 μm device that was used. These scaled curves are shown in Figure 5.1 and were used to find an acceptable bias point for the gate-source voltage given the preceding constraints. The other two families of curves in Figure 5.1 are the results of measured DCIV curves on 100 μm device used and simulated data from model with no self-heating effects. From Figure 5.1 it can be seen that the range of desirable bias points for the gate lies in between -2 and -3V. The use of simulations then results in a more accurate determination of bias point.

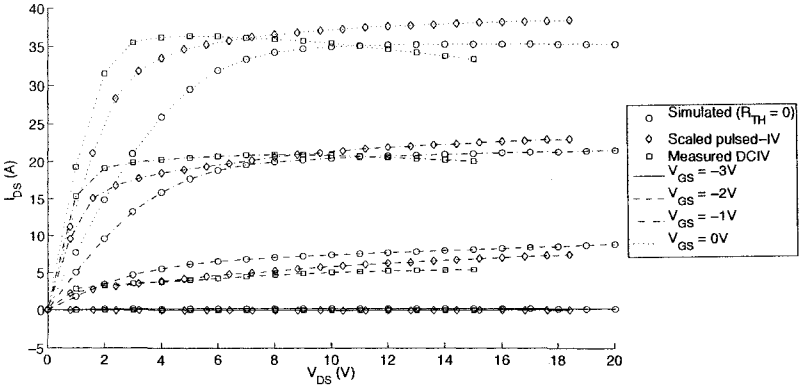


Figure 5.1: Current characteristics of HFET

The physical limitations of the device are best used as the starting point for drain voltage bias selection. Since the HFET being used could only be characterized out to

15 V the bias point allowing for the widest range of linear operation was 8 V. This was used despite the fact that a conservative estimate of the drain source breakdown voltage was 30 V. This meant that the ideal case for output power would have actually been 15 V.

5.2 Harmonic terminations

The transmission line characteristics for the harmonic termination network found at the drain were determined using loading networks that are based on Raab's work. In [29], Grebennikov presents a network and method of determining the network's corresponding components that can be used to achieve the desired harmonic terminations for a class-F PA with third harmonic peaking. A conceptual diagram of such a circuit is shown in Figure 5.2. The length of transmission line labelled $\lambda/4$ at the drain of the HFET in Figure 5.2 is a quarter wave transformer used to achieve an open for the fundamental and its harmonics while allowing for bias injection. The section of microstrip labelled l_c has the electrical length

$$\theta = \frac{1}{3} tan^{-1}\left(\frac{1}{3Z_0\omega_0 C_{out}}\right). \tag{5.1}$$

l_c is used to provide an open-circuit for the current waveform's third harmonic. Finally, the open-circuit stub labelled l_d is used as a quarter wave transformer (at $f = 3 \cdot 3\text{GHz}$) to present the voltage waveform's third harmonic with a short to ground.

Using this network allows for an implementation of a third harmonic peaking class-F PA.

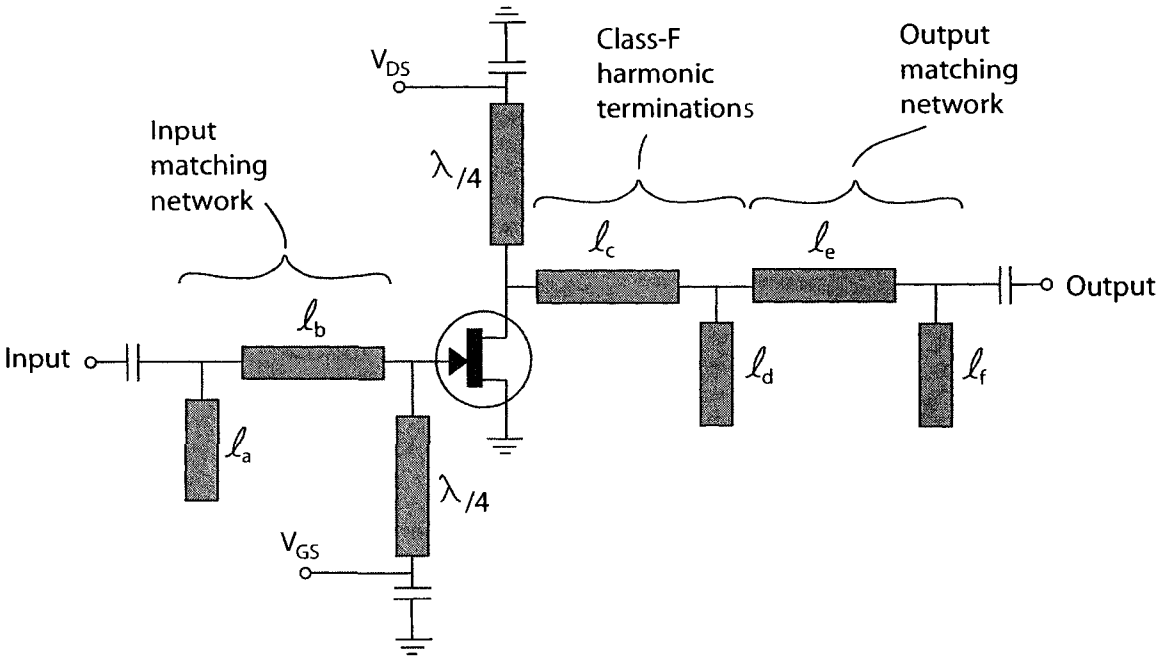


Figure 5.2: Generic class-F PA schematic (microstrip implementation)

5.3 Input matching network

The purpose of the input matching network is to transform the input impedance of the transistor to its optimal value such that maximum power transfer from a 50 Ω source is achieved. The optimal value is typically defined in one of two ways; as a conjugate match to the source that yields the best possible power transfer from source to device, or as the impedance that yields the most power at the load as a result of the PA. A common way of arriving at the latter network is to use the former network as a starting point and then iterate using a series of source- and load-pulls. A source-pull is an evaluation of the PA characteristics over the source plane. Typically one iteration is performed with a low resolution to obtain an initial estimate of the region of input impedances where desirable PA characteristics are achieved. Then a

high resolution sweep is performed over the region of the source-plane found in the first, low resolution iteration. The required input matching network is then selected based on the source impedance that results from the high-resolution sweep. With this input matching network in place the output match could be performed [30].

In this work, the method of the conjugate match as a starting point and the source- and load-pulls to achieve desired PA characteristics was used. The input impedance of the HFET was measured when the harmonic terminations computed as described in section 5.2 and a 50 Ω termination was presented to the drain.

From this starting point, a conjugate match was performed at the input resulting in a starting match for the input microstrip matching network, which is summarized later in Figure 5.8. Having performed a small-signal input match and determined the correct network to present the desired harmonic terminations to the drain meant that the output loading network was all that remained to be designed.

Figure 5.3 shows s_{11} in its log-magnitude representation. From this figure it is clear that, at the frequency of interest, there is very little incident power reflected from the input, which indicates a good input match.

5.4 Output matching network

The output matching network's purpose is to transform the standard 50 Ω load to a value that results in one of two things; more output power or a higher efficiency. To determine the desired load that maximizes the desired characteristic load-pull simulations are used. For this work, the load pull simulations that were performed were done so using several iterations of harmonic balance simulations for varying load

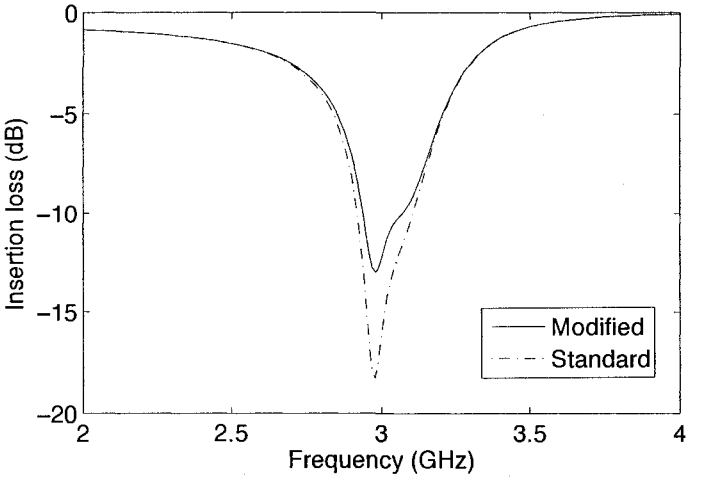


Figure 5.3: Simulated input match for PA during small-signal operation

impedances. The optimal of the resulting load impedances was then realized using a Smith chart to design a matching network to transform the actual load into the desired load.

As with any PA the amount of isolation from the drain to the gate is finite, this leads to a change in input impedance when the output loading changes. This change in input impedance results in an offset in the initial input match. To resolve the issue of an offset in input match, a source-pull was performed with the new output matching network in place. Several iterations of load- and source-pulls were performed to arrive at the matching networks shown in Figure 5.8 [30]. From these source- and load-pull simulations it was found that the ideal source impedance was $98.9 + j90.5\Omega$ and the ideal load impedance was $4 - j9.2\Omega$.

Figure 5.4 shows the simulated output match of the amplifier during small-signal operation. Since the PA will be operating under the large signal operating region the small-signal plots are of little use and are included for completeness.

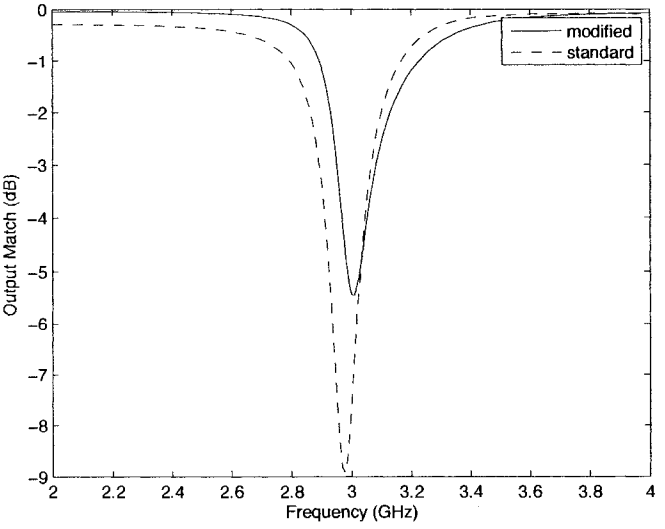


Figure 5.4: Simulated output match of PA during small signal operation

5.5 Stability

Before the design could be considered completed the stability of the full PA required evaluation. A circuit is considered unstable when the amount of reflected power from a port is larger than the incident power. Gonzalez shows in [31] that a series of equations for stability circles can be reduced to two very useful parameters. These parameters are the Rollett stability factor (K) and the stability measure (b). The stability factor is defined as

$$K = \frac{1 - |s_{11}|^2 - |s_{22}|^2 + |\Delta|^2}{2|s_{12}s_{21}|}, \tag{5.2}$$

and the stability measure is defined as

$$b = 1 + |s_{11}|^2 - |s_{22}|^2 - |\Delta|^2, \tag{5.3}$$

where

$$\Delta = s_{11}s_{22} - s_{12}s_{21} \tag{5.4}$$

For a PA to be considered unconditionally stable (i.e. stable for all possible loads) $K > 1$ and $b > 0$ are both required to be true. Figure 5.5 shows that, for the first design iteration, the circuit, which included matching networks in addition to the active device was not unconditionally stable. Upon plotting the load stability circles it was found that the PA was only marginally stable for 50 Ω loads.

Due to the marginal stability of the PA it was decided that another iteration of

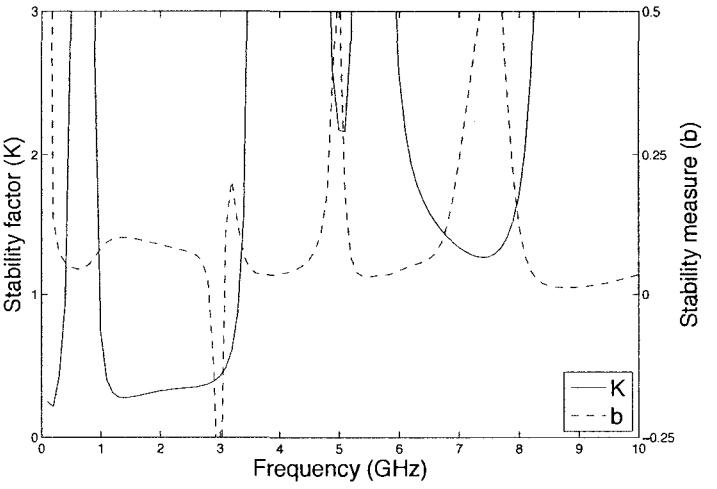


Figure 5.5: Simulated stability factor and measure before addition of R_{stab}

design would be completed with measures to improve the stability. To improve the stability a large resistor was placed as close to the gate of the device as possible. By decreasing the size of the resistor it was possible to increase the stability of the PA until a more stable PA was completed. Naturally, this affects the gain of the PA as less signal is present at the gate. Furthermore, this method of improving stability is not feasible in all forms of amplifier design (*e.g.* low noise designs would have a significantly increased noise figure from such a technique) [31]. The addition of the footprint for the resistor has an added bonus in that, during a first spin many values can be trialed if the PA is found to still be unstable.

Figure 5.6 shows the stability factor and measure for the PA that was redesigned to include a shunt resistor at the gate of 649 Ω. This value was achieved by trial and error over several iterations of design.

The stability measure, b, for the second iteration of the PA is greater than 0 for all

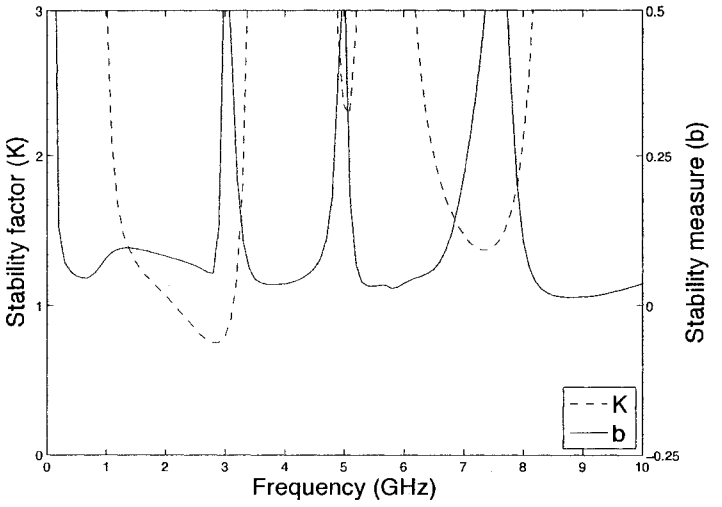


Figure 5.6: Simulated stability factor and measure after addition of R_{stab}

frequencies but the stability factor K still fails to meet the criteria for unconditional stability. As a result this iteration of PA is only conditionally stable. To verify whether or not the PA is stable over the range of loads of interest (*i.e.* 50 Ω) both the load and source stability circles were plotted over the range of frequencies that were only conditionally stable. All of the source stability circles showed that the PA was stable for all input loading conditions around 50 Ω. However, the output stability circles showed that the PA was unstable for loads found around the edge of the Smith chart as shown in Figure 5.7.

Since the PA is targeted at 50 Ω loads the PA is loaded in a region of stability when only conditionally stable. This analysis has shown that the PA designed will be stable over all frequencies when loaded with 50 Ω, as designed.

The final circuit that was fabricated is shown in Figure 5.8. This schematic includes the stability resistor introduced at the gate of the HFET and the fix for the 50 vs.

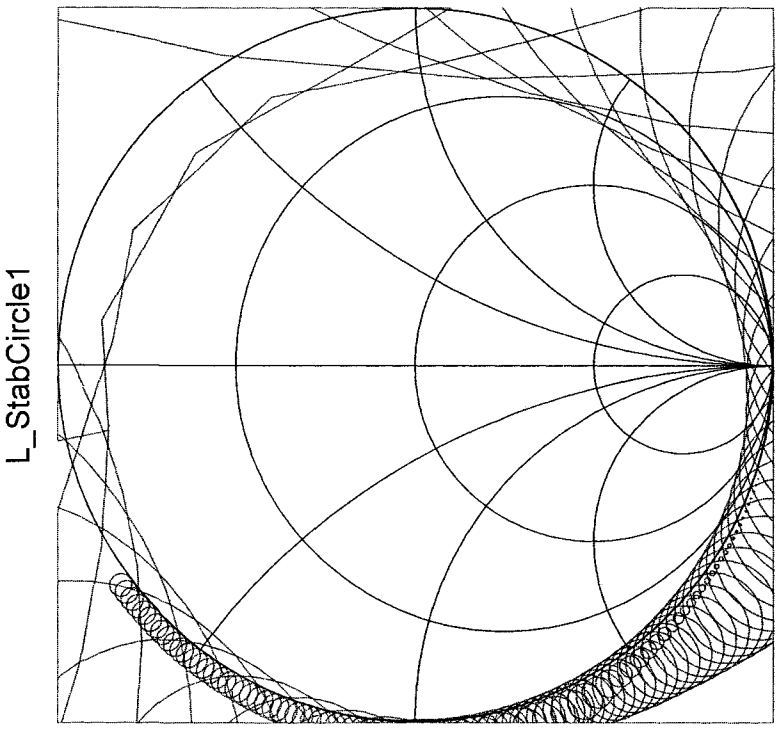


Figure 5.7: Simulated load stability circles after addition of R_{stab}

500 Ω error (this fix is highlighted by the dashed area.)

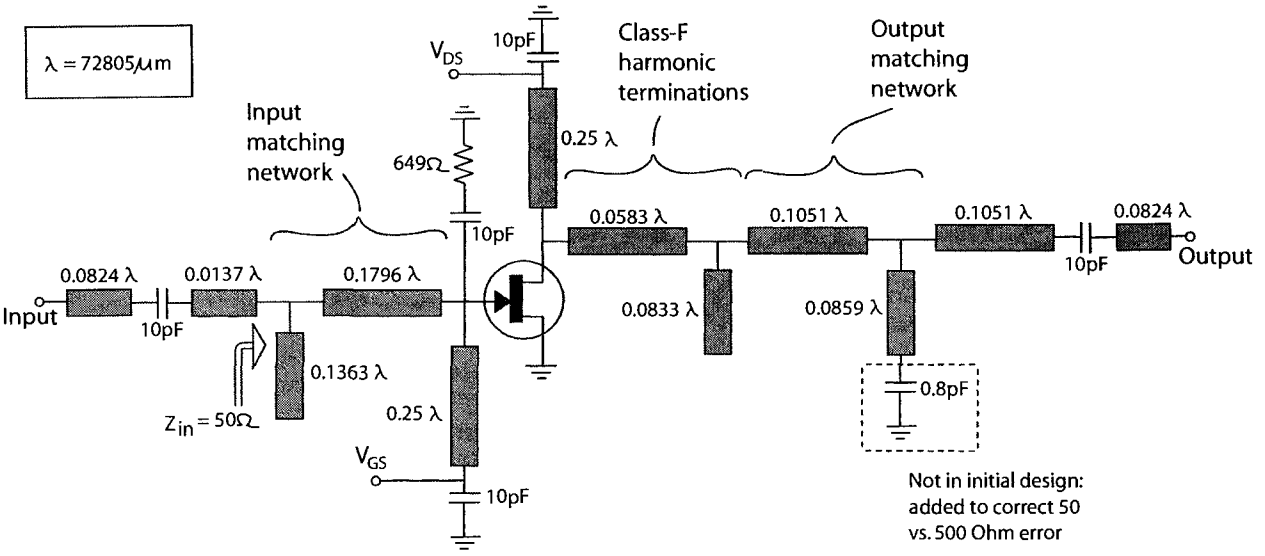


Figure 5.8: Schematic of fabricated PA

5.6 Simulation results

Simulations were performed using Agilent's ADS. Two main types of simulations were used. These were *s*-parameters and harmonic balance (HB) simulations. The *s*-parameter simulations were used to evaluate the small-signal behaviour of the PA, while the harmonic balance simulations were used to simulate the large-signal behaviour of the PA.

It should be noted that all of the simulation results presented below are for the re-designed class-F PA with the fix for the 50 *vs.* 500 Ω error made in the design. As a result, these resuls can be compared directly to the measured data, which is on the modified PA having this same fix.

5.6.1 Harmonic balance

Time domain simulation results were achieved using ADS' harmonic balance simulations and then using ADS' data display tool to convert the spectral weights to their time-domain equivalents. The simulation results for the drain voltages for the standard and modified Curtice cubic models with overlayed simultaneous gate voltage can be seen in Figure 5.9. To clarify; the standard Curtice cubic model uses the equation (2.3) while the modified Curtice cubic model uses the techniques described in section 2.3.4. This figure shows the drain voltage has a squared waveform due to the presence of the third harmonic. This is similar to the expected result as presented in Figure 4.1 although having different amplitudes.

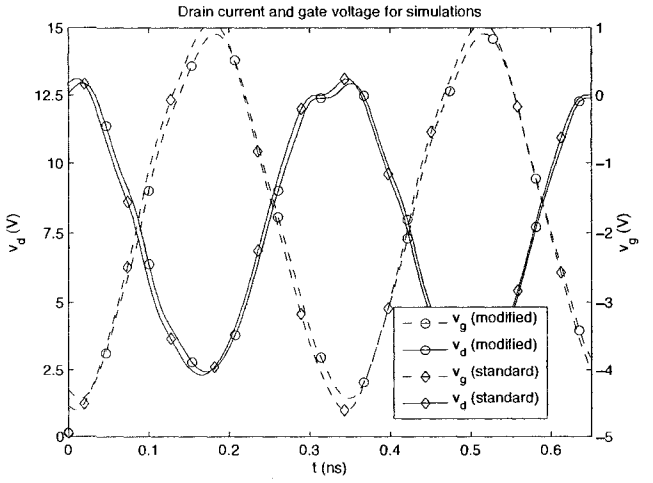


Figure 5.9: Simulated drain voltage at peak PAE

The simulated time domain drain currents for the standard and modified Curtice cubic models and overlayed simultaneous gate voltage can be seen in Figure 5.10. The bottom portions of the sinusoids are flattened while the top portions maintain their sinusoidal shape with a noticeably sharper profile as one would expect.

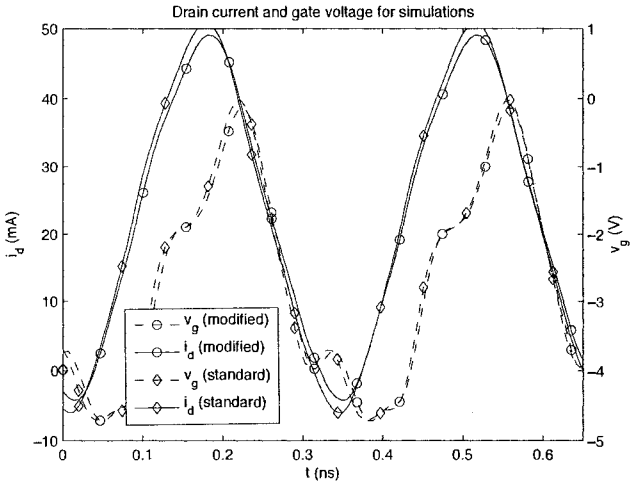
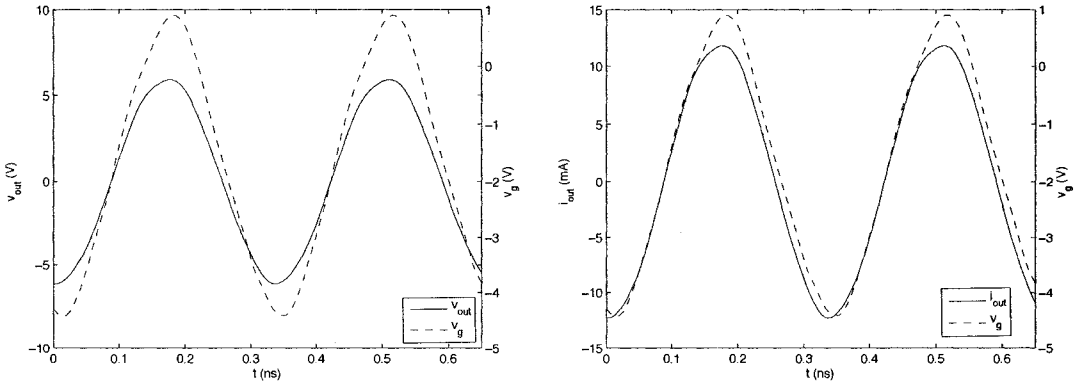


Figure 5.10: Simulated drain current at peak PAE

The drain waveforms make it apparent that the simulated PAs are indeed operating as a class-F PA. The output waveforms differ significantly from the drain waveforms given the filtering of higher order harmonics. The result is an amplified version of the input waveform having comparable frequency content in that the fundamental harmonic dominates the output. Figure 5.11 shows that there is clearly some amplitude distortion as can be seen by the rounding of the peaks of the waveforms. This further highlights why class-F PAs are best used in systems with modulation schemes that are based on frequency and phase content as opposed to amplitude content. Figure 5.11 shows the output voltage and current waveforms at the 50 Ω load, respectively. Since the output waveforms for the standard and modified Curtice cubic models were

essentially identical only the modified version is shown.



(a) Simulated output voltage

(b) Simulated output current

Figure 5.11: Simulated output waveforms

5.6.2 Simulated amplifier characteristics

The overall PA was then simulated using Agilent ADS's HB simulator to determine the expected characteristics such as gain and PAE for large and small signal operation. The simulations were performed for both the standard and modified Curtice cubic models. The simulation results from ADS were then plotted using MATLAB and can be seen in Figure 5.12.

Figure 5.12 shows that the standard and modified versions of the Curtice cubic model have similar results. PAE peaks occur for roughly the same input powers and the gain at these peaks for the standard and modified models; they differ by approximately 0.5 dB with 6.4 and 6.5dB, respectively. Peak PAE values differ by approximately 5% with 23 and 28%, respectively. Gain of the PAs over their linear regions of operation differs by no more than 2.5 dB. The primary reason behind the

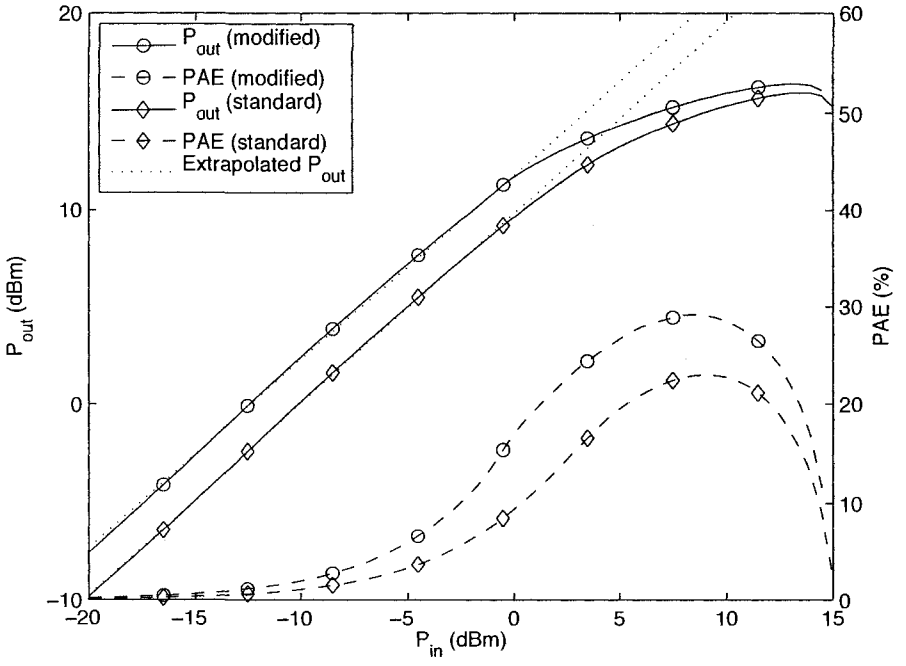


Figure 5.12: ADS simulation results for gain, compression and PAE

relatively low PAE and gain is the conservative drain voltage of 8 V.

The most significant contributor to the differences in the PAEs is the difference in simulated gain. Figure 5.13 shows this difference swept with input power at the bias point and frequency of interest for both models.

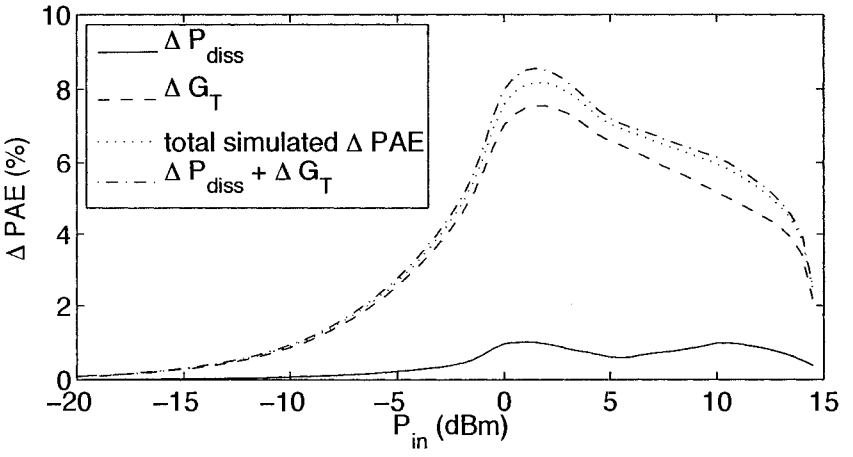


Figure 5.13: Sources of error in PAE simulations

From this plot we can see that for most input powers the total difference in simulated PAEs is very close to the error that results from the difference in simulated transducer gains. In fact, the differences in dissipated power contribute less than 1% for all input powers.

Chapter 6

Class-F PA Implementation and Results

This chapter discusses the implementation of the final PA. Following the implementation, the measurement results are presented and discussed.

6.1 Implementation

The lowest risk approach for a 3 GHz operating frequency was that of a microstrip design. The reason being that it is easier to get, at microwave frequencies, controlled impedance transformations using microstrip networks than if lumped elements are used. Since this work was not an effort in product development, the size of the circuit was of little concern. Hence the final circuit was implemented on a Rogers Duroid 5880 substrate.

The Nitronex HFET die was epoxied to the substrate with a silver epoxy. Bonding was then performed using equipment available at Carleton Univeristy. A diagram of

the bonding is shown in Figure 6.1.

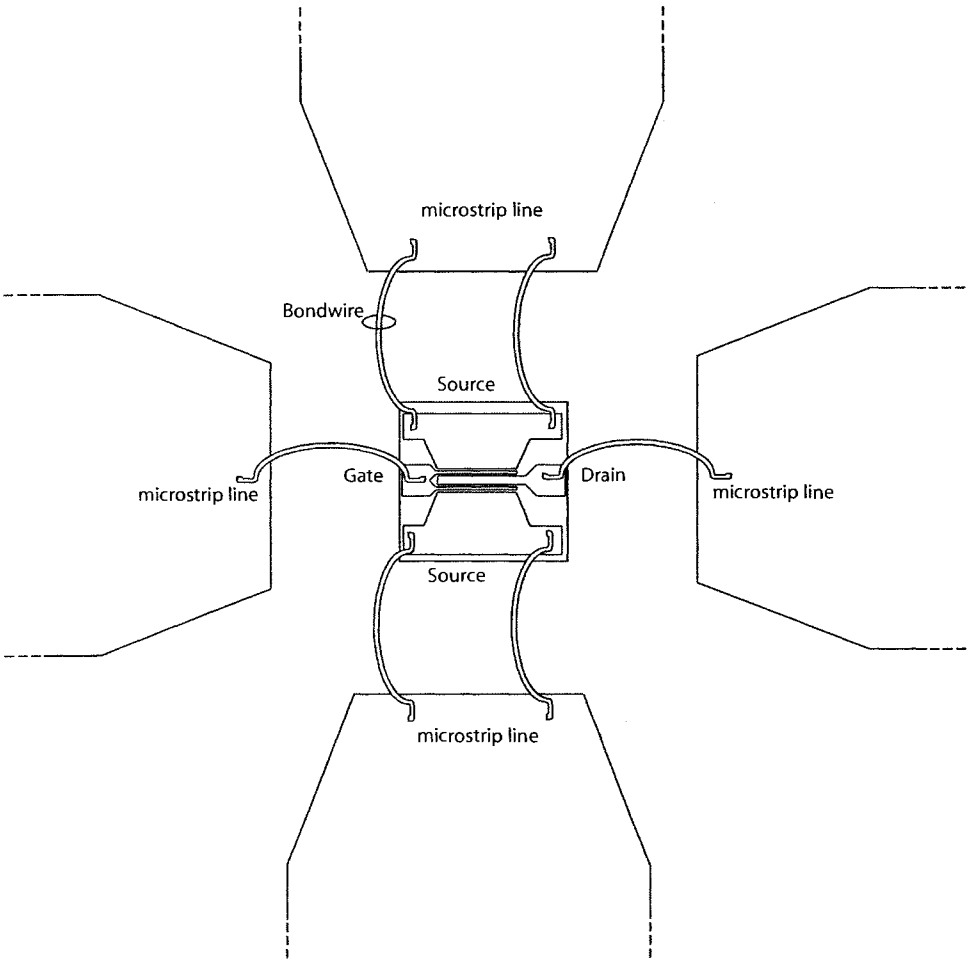


Figure 6.1: Die diagram and connections

Finally, passives and connectors were soldered onto the printed circuit board (PCB). The most important passive components on the final PCB were the coupling capacitors. These capacitors were chosen such that they were series resonant at the frequency of operation, 3 GHz. This reduces the amount of signal lost entering and leaving the PCB. The stability resistor used was a 649 Ω manufactured by Thin Films Technologies. Another critical component that was required was the shunt capacitor

added in the modification stage. Simulations showed 0.8 pF yielded the best results. However, a few experimental trials showed that 1 pF of capacitance in two 0.5 pF capacitors ended up yielding the best results. This discrepency is likely the result of stray parasitics that resulted from the method of implementing the fix. The connection to the groundplane from one end of the capacitors was made using a small wire through a drill hole, which could contribute some inductance, potentially offseting the expected capacitance.

The initial circuit was then modified to correct the error in expected load impedance as described in Section 6.1.1 to create the final PA, which is shown in Figure 6.2

6.1.1 Required modifications

To get the fabricated PA operating two modifications were required, which are discussed in this section.

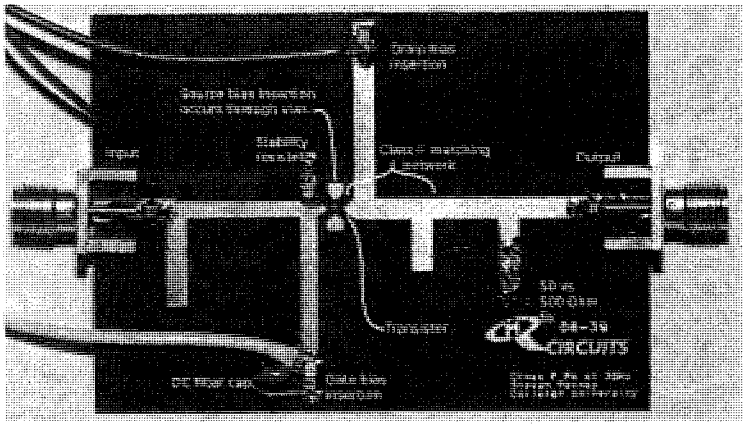


Figure 6.2: Photograph of fabricated class-F PA

Due to some oversight during the design phase of the project, the manufactured PCB did not work as expected when terminated with a 50 Ω load. Rather than

fabricate another PCB, simulations were performed to find a feasible modification to the PCB that would result in a functional PA. The output matching network was optimized using ADS simulation tool by sweeping the shunt capacitor's value and physical location along the various microstrips. It was found that the addition of a shunt capacitor at the location shown in Figure 5.8 would achieve the desired result.

Having modified the PA it was found that the modified circuit was subject to low frequency oscillations. To resolve this a large decoupling cap was added between power and ground as can be seen in Figure 6.2.

6.2 Measurements

Two different measurement types were performed during the measurement process. The first was a small signal s-parameter measurement that simply used a vector network analyzer (VNA) and dual output DC supply. This setup was quite simple and provided the fastest feedback of the PAs small-signal characteristics. The second test setup was a large signal measurement setup that consisted of an RF signal generator used to generate a sinusoid and a spectrum analyzer that was used to measure the PAs output. Using these two test setups it was possible to characterize the PA for both small and large signal operation. The large signal setup was also used to quickly verify the small signal operation to ensure that both setups were reporting the same results over the same regions of operation.

The measured results are compared to as many as two sets of simulated data. Simulated curves are labelled either "standard Curtice cubic" or "modified Curtice cubic". The standard curves are for the standard ADS implementation of the Curtice

cubic model while the modified curves include the modifications discussed in Section 2.3.4.

6.2.1 Small-signal measurements

Small-signal measurements of the modified PA were taken and compared to simulated data of the modified Curtice cubic model. Since the design was of a large-signal PA not much treatment is given to small-signal measurements, they are however included for completness sake.

Figure 6.3 shows the simulated and measured input return loss of the PA. From this figure it is clear that the optimal operating frequency of this amplifier when operating linearly is not the expected 3 GHz. The return loss is acceptably low (*i.e.* below -10 dB) over the frequency range 2.8 to 2.95 GHz. This is most likely due to the fact that the modifications to the board to correct for the error in design were less than ideal.

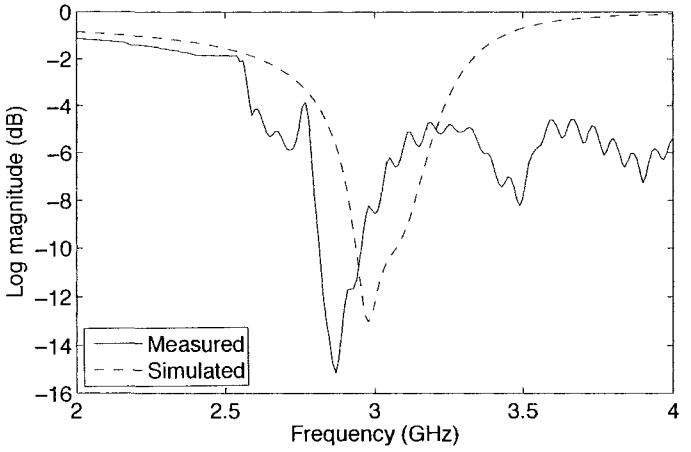


Figure 6.3: Measurement and ADS simulation results for PA input return loss (s_{11})

Figure 6.4 shows the reverse isolation of the PA. The measured isolation never drops below -50 dB even though simulation shows that it should. In reality there are many physical phenomena that simulations can not account for. This is the reason behind the unreasonably high isolation of 60 dB that occurs only in simulation as the model is simple in comparison to the physical device.

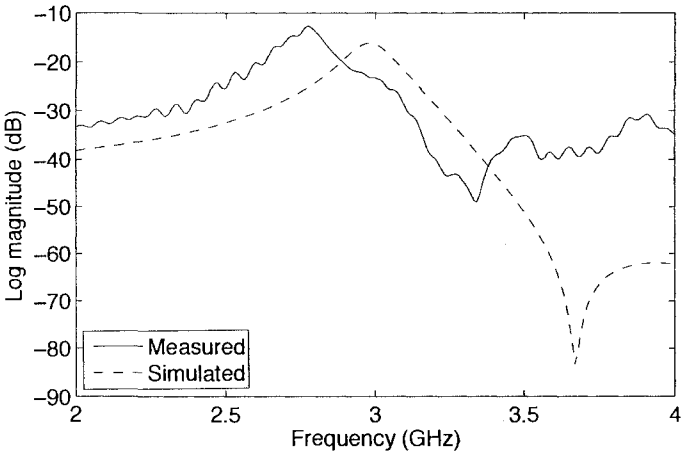


Figure 6.4: Measurement and ADS simulation results for PA reverse isolation (s_{12})

Figure 6.4 shows the same trends between both curves although offset by 220 MHz.

Figure 6.5 shows the forward gain of the PA. From this plot, it is clear that the gain peak occurs at 2.8 GHz and is approximately 2 dB below the expected gain. As with the previous two plots, this plot shows similar trends between simulated and measured curves. The two plots differing only by an approximate 200MHz frequency offset and "ringing", which is an artifact of the measurement and should not be mistaken for oscillations as they are functions of frequency and not time.

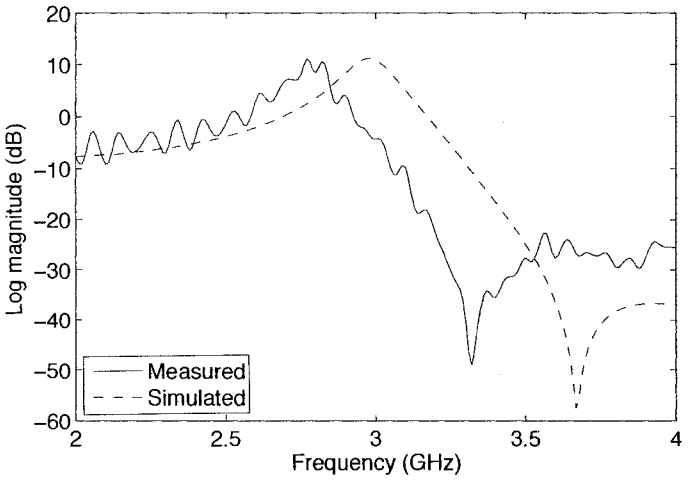


Figure 6.5: Measurement and ADS simulation results for PA gain (s_{21})

Figure 6.6 also shows similar trends between the two curves. As with the other s-parameter measurements, there is an approximate 200 MHz frequency offset with the simulated data.

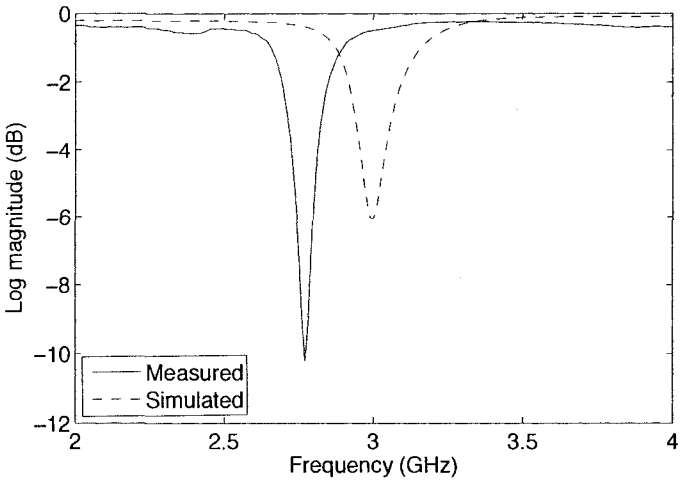


Figure 6.6: Measurement and ADS simulation results for PA output reflection (s_{22})

6.2.2 Amplifier gain and efficiency

The PA gain at 2.8 GHz was plotted as a function of input power in Figure 6.7 along with the simulated data for the standard and modified Curtice cubic models for comparison. From this figure, it is clear that there is more than 2 dB of gain measured when compared to the modified simulation results. Figure 6.5 shows the same trend as the measured gain is between 1 and 2 dB lower for the simulated data. The 1 dB compression point also differs between the plots; in the case of the measured data, the compression occurs at 7 dBm of input power, which is approximately 5 dB higher than simulation, which occurs for roughly 2 dBm of input power. The standard model shows better agreement over the small signal operating range. At peak PAE, which occurs for $P_{in} = 9$ dBm, the measured and both simulated gains are all within 2 dB of each other.

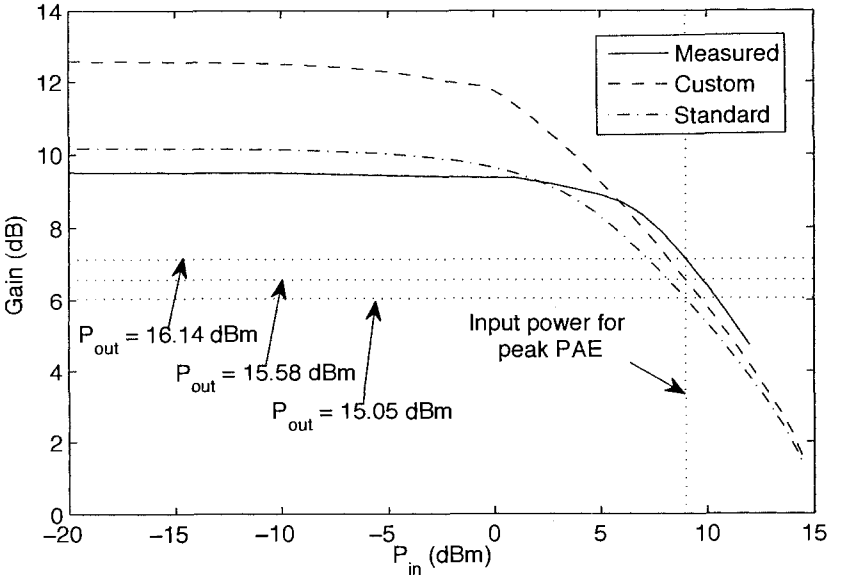


Figure 6.7: Comparison of simulated and measured gain as a function of input power

The DC power dissipation of the PA was plotted against input power as shown in Figure 6.8. This plot highlights that the modified Curtice cubic model tracks measured power consumption better than the standard.

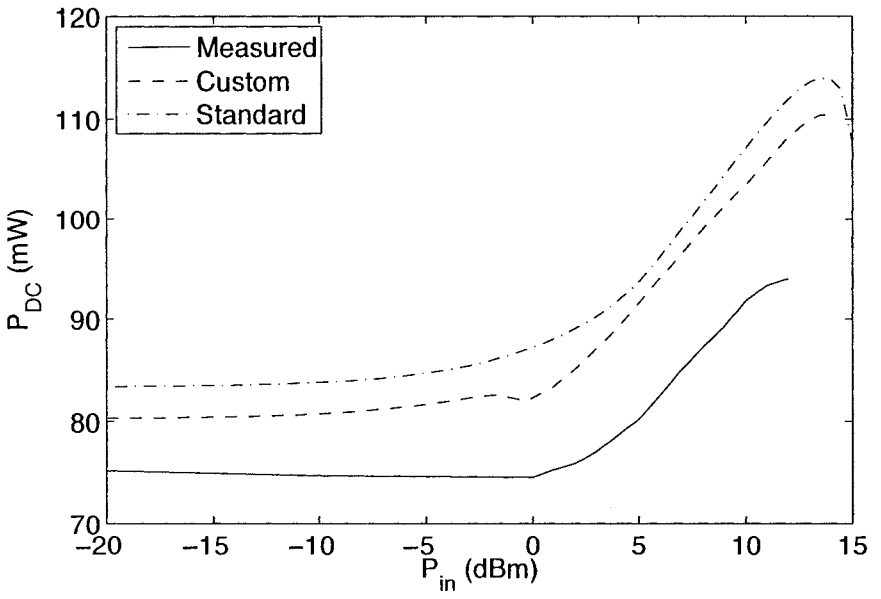


Figure 6.8: Measured and simulated DC power dissipation

The PA output power characteristic and efficiency was plotted as a function of input power as shown in Figure 6.9. This plot shows both measured and simulated data, all of which show significantly different PAE curves. The measured PAE peaked at 37 % for an input power of 9 dBm and corresponding output power of 16.1 dBm with a power dissipation of 89 mW. The PAE plot is quite sensitive to gain, that is to say that a small error in output power (or input power) can contribute to a significant difference in PAE. For example, if the output power for the peak PAE is reduced by 1 dB from 16.1 dBm to 15.1 dBm the result is a reduced PAE from 37 % to 28 %. This is further highlighted in a breakdown of the sources of error in the PAE plot, which is shown later in this chapter (*c.f.* Figure 6.11).

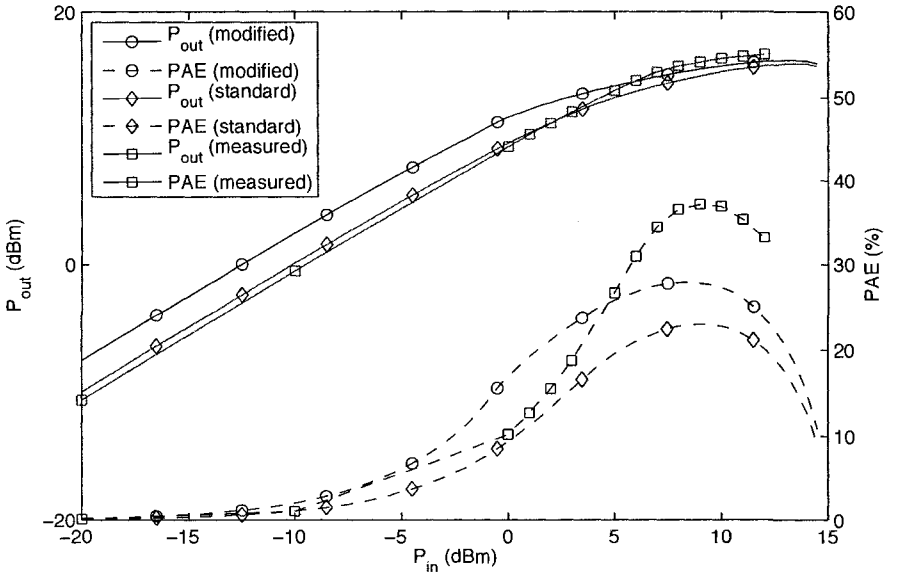


Figure 6.9: Measurement and ADS simulation results for PA characteristics

Figure 6.9 shows that at peak PAE, which occurs for an input power of 9 dBm for simulations and measurements, the PAEs differ by as much as 15 percentage points. Figure 6.10 shows the difference in PAEs for the two different models that were simulated when compared to the measured data.

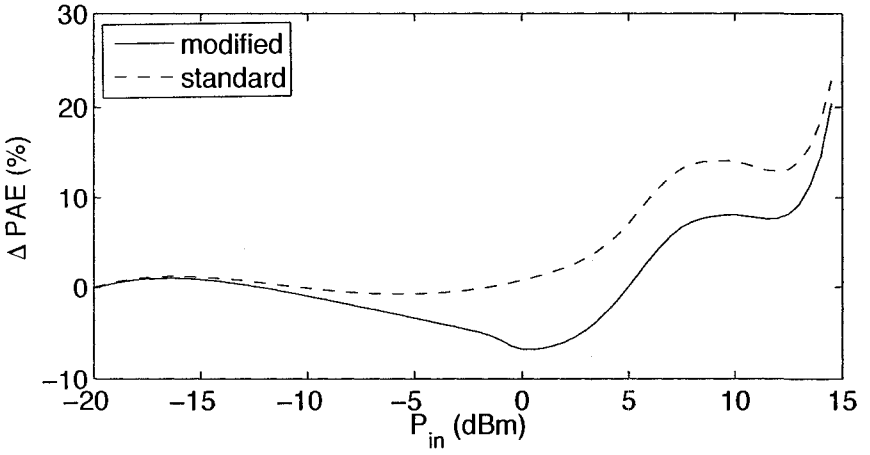
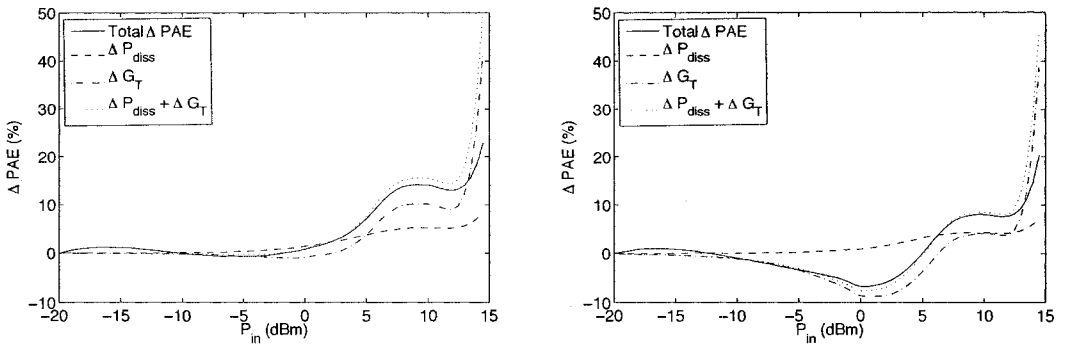


Figure 6.10: Difference in PAE between measured data and simulations

From this plot it is clear that, during linear operation, the standard Curtice cubic model tracks the measured data much better that the modified model. However, during large-signal operation, the modified model predicts PAE more accurately than the standard Curtice cubic model. The sources of the differences in PAEs from simulated data and measured data can be explained by examining the errors in the transducer gain and dissipated power. Figure 6.11 shows these sources of error and how they relate to the difference in PAE.

Figure 6.11 (a) shows that, for the standard Curtice cubic model, the error in simulated PAE at 8.5dBm is approximately 14%. Of this 14%, $\frac{9}{14}$ result from the error in simulated gain while the dissipated power accounts for the remaining $\frac{5}{14}$.



(a) Standard Curtice cubic model

(b) Modified Curtice cubic model

Figure 6.11: Sources of PAE differences between measurements and simulations

Figure 6.11 (b) shows that, for the modified model, the error in simulated PAE at 8.5dBm is approximately 9%. Of this 9%, $\frac{4}{9}$ result from the error in simulated gain while the dissipated power accounts for the remaining $\frac{5}{9}$.

From this data, it is clear that the modified model does not offer significant improvement over the standard Curtice cubic model in simulated results. For designs having a device biased closer to the pinch-off voltage the, modified model would offer further improvement, especially for large drain voltages.

Since the measured PAE is higher than the simulated PAE one would expect the gain to also show the same trend. Figure 6.9 shows that this is not the case, which points to a significant difference in the DC power consumption. Figure 6.8 was generated to verify that this was indeed the case. The simulated DC power consumption is higher by approximately 50 mW, which is a 24% difference.

Chapter 7

Conclusions and Future Work

7.1 Conclusions

This work has presented a modified version of the Curtice cubic model that has been applied to a Nitronex 100 μm device. Through modifications to the existing Curtice cubic model's equations, modeling of the pinch-off behaviour of the HFET was achieved. Further modifications were made to the model in the inclusion of a spline interpolation method for the thermal coefficients of the HFET. Unfortunately, this could not be used as it was not possible to characterize the HFET's thermal behaviour.

Measurements of the HFET's various characteristics were performed over a wide range of bias and frequency points. The model's parameters were then populated using various methods to extract their values from the measurement data.

With an accurate model of the HFET having been created, it was possible to design a class-F PA using an empirical design approach. Using the model that was created,

it was possible to perform equivalent large-signal source- and load-pull simulations with ADS' harmonic balance simulation tool. Using this design methodology, it was possible to complete the design of a 3 GHz class-F PA using a Nitronex AlGaN/GaN HFET on a Si subtstrate.

The implemented PA was then characterized and found to behave similar to simulations. The resulting measurements were used as a method to validate the model that had been created. The final characteristics of the fabricated 3 GHz class-F PA was a maximum PAE of 37% with more than 7 dB of gain at an output power density of 0.411 W/mm of gate width. Differences in measured and simulated PAEs were found to result from differences in both gain and simulated power dissipation.

7.2 Future work

This section outlines steps that can be followed to continue this work

- Isothermal measurements will provide the necessary information to complete an implementation that includes self-heating effects.
- RF dispersion characterization will provide the necessary information to extend the range of frequencies over which the model will provide accurate results.
- An investigation into the scalability of the implemented model would make the model easier to port to devices of different sizes.

With a completely characterized device that has been modelled to the full extent that the existing infrastructure will support, a further iteration can be performed on the class-F PA design.

- Assuming that the measurement capabilities are available, the characterization of a larger device over a broader range of operation could be completed. This would allow for much more desirable PA characteristics.

- Repeating the design with a proper load would further improve the resulting PA's characteristics.

Although HPAs are currently the most common circuits that use GaN HFETs, circuit implementations are not limited to this. With the foundation that is the infrastructure for a flexible compact model that has been shown to provide accurate results many other circuits can be implemented. A few other circuits that this technology can be applied to include but are not limited to;

- Various different classes of RF HPAs,

- High power RF oscillators.

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