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**LA THÈSE A ÉTÉ
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DESIGN AND CHARACTERIZATION
OF A
PROGRAMMABLE TRANSVERSAL FILTER

by

Yusuf Aminul Haque

A thesis submitted to the Faculty of Graduate Studies,
in partial fulfillment of the requirements for the
degree of

Doctor of Philosophy.

Carleton University
Ottawa, Ontario, Canada

May, 1977

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Yusuf Aminul Haque

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The undersigned recommend to the Faculty of Graduate Studies and Research acceptance of the thesis:

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ABSTRACT

The design and characterization of a real time programmable transversal filter has been presented. The filter converts signals to voltage levels as opposed to charge in earlier designs. This results in improvement of the device performance. A single level n-channel silicon gate MOS/LSI process was shown to be sufficient to implement the filter. A 16 tap filter multiplexed into two channels was accommodated in a chip whose dimensions are 120x125 mils.

Dynamic range of the filter is limited primarily by fixed pattern noise. This problem has been modelled and at present about a 45dB dynamic range is obtainable with less than 1% harmonic distortion on 4Ωcm substrates. Experiments on a 96 tap filter show excellent transfer function agreement with theory.

The processing capability of such a structure is expected to be extremely powerful, and offers advantages when compared with completely digital structures in cost and performance for real time signal processing.

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LIST OF PRINCIPAL SYMBOLS

$\{ \}$	denotes a set of numbers
0	low level state in positive logic
1	high level state in positive logic
ϵ_0	free space permittivity
ϵ_s	dielectric constant for silicon
ϕ_1, ϕ_2	two-phase clocks for the shift registers and ring counters
ϕ_f	Fermi potential
ϕ_g	clock used to control the floatation of the sensing electrode
ϕ_R	clock used to reset sensing surface
ϕ_S	clock used to sample output voltage
$\delta(t)$	Delta function
ω	angular frequency
CCD	charge-coupled devices
C_d	depletion capacitance of the semiconductor per unit area
C_{FB}	feedback capacitor used in amplifier at the output
C_o	oxide capacitance per unit area
C_{ox}	oxide capacitance
C_T	total electrode capacity
$F[\{h\}]$	Fourier transform of the set $\{h\}$
f_c	frequency of ϕ_1, ϕ_2
FPN	fixed pattern noise
h_1, h_k, h_m	tap weight coefficients

G_k	gain of the source followers in the kth channel
$H(\omega)$	programmed transfer function, i.e. Fourier transform of $\{h\}$
N	tap length of filter; substrate doping density.
$\text{sinc } x$	$\sin \pi x / \pi x$
T	period of delay unit in Chapter 2; period of ring counter repetition rate in Chapter 5
V_{dc}	d.c. bias on the signal
V_{dd}	d.c. voltage
V_{FB}	flat band voltage
V_g	peak amplitude of input signal
V_s	signal voltage
V_R	reference voltage
V_{SUB}	substrate voltage
V_{TO}	threshold voltage
z^{-1}	unit delay operator

CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

A transversal filter is a general purpose processor capable of implementing any arbitrary finite impulse response. A given set of tap weight coefficients yields a particular impulse response.

Linear MOS-LSI technology has progressed to the point where transversal filters can be implemented on a single chip, but the tap weight coefficients are not electrically alterable in real time. These fixed tap filters have had enormous success⁽²⁰⁾ since they provide greatly lowered costs over a comparable digital processor implementation.

The most versatile transversal filter is a real time correlator which requires analog tap weights which can be altered in real time under program control. Such a device can, in principle, implement all possible transversal filters.

It is the purpose of this thesis to present the design of a programmable transversal filter (correlator), with analog tap weights, which can be altered electrically in real time. The experimental characterization and demonstration of its use will also be presented.

1.2 NEED FOR TRANSVERSAL PROCESSORS

Fig. 1.1 shows the block diagram of a transversal filter. It consists of a sampling stage followed by delay stages, each of which

Fig. 1.1. Block diagram of a transversal filter.

delays the signal. The signal is non-destructively sampled at each delay stage, multiplied by the appropriate weighting coefficient and the weighted signals are summed together to give the filter output. Such a structure can, in principle, be realized by either analog or digital means.

The advantages of the silicon planar process have revolutionized the performance and cost of digital systems. Similar advances are only now being reported on the analog signal processing field. Discrete time analog signal processing has been extensively stimulated by the recent developments in charge transfer devices (CTD's). The availability of distributed analog storage and contiguous tapping structures has made possible the realization of mask programmable transversal filters on silicon LSI technology. Once this has been done, many other signal processing functions can be implemented. The integrated transversal filter will become a basic building block for integrated circuit designers (20)

Discrete time analog signal processing is similar to digital filtering with the added advantage that the signal need not be digitized in an A/D converter. Silicon LSI technology makes it feasible to implement the processor on a single chip, and with added peripheral circuitry to outperform a computer based digital system in cost and performance.

1.3 PRIOR ART

Industry has, so far, concentrated on the development of fixed tap filters for various applications (17). Future developments in CTD

signal processing will need programmable filters, i.e. filters whose taps may be electrically altered.

CTD implementation of fixed tap filters has come in several forms. The first filter reported was built around a Bucket Brigade Device (BBD) in which the weighting coefficients were obtained using split electrodes⁽¹⁵⁾. The split electrode concept was later used on charge coupled device (CCD) based filter⁽¹⁷⁾. Basically, the signal is transferred under the split electrode and weighting is achieved by connecting the split electrodes to two separate rails which drive a differential current meter. The length of each split electrode is chosen in the ratio $(1+h_m):(1-h_m)$ so as to produce the net weight of h_m at each tap.

A variable tap weight filter was reported in 1973⁽²²⁾, using MNOS transistors, which provide adjustable tap weights with inherent memory. The conductances under the MNOS capacitances can be altered when suitable pulses (high stress bias) are applied to the gate. This device was built around CCD's and was not a real time programmable device.

A more viable alternative to a real time programmable transversal filter was demonstrated by Tiemann et al⁽¹⁾. Here, the tap weights were restricted to a 1-bit binary number which could be electrically introduced in a binary signal shift register. The analog signal charge is loaded into a line of discrete cells in which charge transfer takes place repeatedly between only 3 storage electrodes as shown in Fig. 1.2a. The loading of a particular cell from the analog bus is controlled by a

Fig. 1.2a. Binary correlator using "charge sloshing" techniques.

Fig. 1.2b. An analog correlator using binary coded channels.

series of scan gates which are turned on in sequence; by passing a single addressing bit along the scan shift register. Charge can be transferred from the cell to either of two electrodes by appropriate control on two transfer gate lines. The transfer gate is controlled by another register which contains the binary sequence (tap weight).

The capacitive effect of charges in different cells are summed on the output electrode, a process that does not remove any charge from the cells. This device does not suffer from charge transfer inefficiency^(9,20) problems common in CCD based filters, as the charge is retained on the cell. Although this device does not have analog tap weight capability, it could be so built by using several channels with binary weighted amplifiers in each channel as proposed by Buss et al⁽²¹⁾. The approach is shown in Fig. 1.2b. This device, however, suffers from crosstalk (see Section 3.4.2) between cells - an effect that arises due to the fact that the signal information is charge on the semiconductor surface and the semiconductor capacitance is non-linear (with regard to voltage). A 2 level MOS process was used to fabricate the device.

In this thesis, a transversal filter design is proposed where the signal information is a voltage source on the silicon surface. A design will be proposed which will allow linear operation of the filter and circumvent the crosstalk problem. Further, analog tap weights will be achieved by digitizing the tap weights into binary bits and letting each binary bit propagate in a digital shift register which will control

signal flow into binary area ratioed capacitors. The design will allow filters of arbitrary length and will use a single level n-channel silicon gate MOS-LSI process. Fixed pattern noise behaviour, which limits the dynamic range of the device, will be related to device parameters and techniques will be developed to suppress its effects..

1.4 THESIS FORMAT

Chapter 1 ~~gives~~ a brief introduction to signal processing using charge transfer devices.

Chapter 2 gives a brief review of transversal filter theory and presents the system organization of the proposed filter.

Chapter 3 deals with the actual chip design and layout.

Chapter 4 discusses sensing techniques and output peripheral circuitry needed to operate the device.

Chapter 5 presents experimental results obtained with the filter chip; factors affecting filter performance are discussed and some improvements in the chip design are suggested. A model for fixed pattern noise behaviour of the processor is proposed and experimental results are shown to collaborate with it.

CHAPTER 2

FILTER THEORY AND ORGANIZATION OF THE PROPOSED PROCESSOR

2.1 INTRODUCTION

This chapter will deal with the general theory of a transversal filter. The implementation of such a filter will be discussed and the organization of the proposed processor will be presented.

2.2 FILTER THEORY

Fig. 2.1 shows the simplest realization of a transversal filter. The transfer function for such a configuration is

$$H(Z) = \sum_{n=0}^{N-1} h_n Z^{-nT} = \sum_{n=0}^{N-1} h_n Z^{-n} \quad \text{if } T = 1 \quad (2.1)$$

= unit delay operator

Thus given the set $\{h_n\}$, any finite impulse response may be approximated. The structure is inherently stable since it consists of an all zero configuration (feed forward). Other realizations of Eqn. 2.1 are possible⁽²⁾, but are not readily implementable with charge transfer device technology.

The above structure may be thought of as a convolver in the time domain, since the time domain output $y(n) = \sum_{m=0}^{N-1} h(m) \cdot X(n-m)$ is a convolution of the tap weights $h(m)$ with the input signals $X(n)$.

A transversal filter where the tap weights can be altered is sometimes referred to as a correlator, since it is capable of performing

Fig. 2.1. Block diagram of a transversal filter.

correlation, as will now be shown.

If $y(\tau)$ is the convolution of two real signals $h(t)$, $x(t)$, then

$$y(\tau) = \int_{-\infty}^{\infty} h(t) x(\tau-t) dt$$

Assuming a stationary process ⁽³⁾, the cross-correlation of two real signals $h(t)$, $x(t)$ is defined as ⁽²⁶⁾.

$$\begin{aligned} R_{hx}(\tau) &= \langle h(t), x(t-\tau) \rangle = \int_{-\infty}^{\infty} h(t) x(t-\tau) dt \\ &= [h(t)] * [x(-t)] = [x^*(t)] * [h(-t)] \end{aligned}$$

where $*$ designates convolution.

Comparing this to the expression for convolution, it is evident that if $h(t)$ represents the impulse response of a filter, feeding in the time inverse of this to the processor would yield the correlation between $x(t)$ and $h(t)$.

A more general schematic of a transversal filter realizable in the direct form is shown in Fig. 2.2. Here, there are M delay stages between tap weights. The output may be written as:

$$\begin{aligned} Y(t) &= \sum_{i=0}^{N-1} h_i \sum_{n=-\infty}^{\infty} X(t-iT) \delta(t-nT/M) \\ &= \sum_{i=0}^{N-1} \sum_{n=-\infty}^{\infty} h_i X(t-iT) \delta(t-nT/M) \end{aligned}$$

Fig. 2.2. A sampled data transversal filter with a total of N sectors with M delay stages in each section.

This equation is best understood by referring to Fig. 2.3 where the impulse response of the filter is sketched. The impulse occurs with period T and hence, in the frequency domain, the spectrum is repeated every $1/T$. Thus, the delay T determines the frequency scaling and periodicity of the transfer function; thus, using a higher value of M does not change the bandwidth restriction on the input signal which must still be bandlimited to $1/2T$. The sampled data input is also shown in Fig. 2.3. Since the samples are spaced T/M , the input data (after the sampler) spectrum would repeat every M/T in frequency domain. Thus, the number of stages per delay section (M) determines the position of the frequency translated baseband spectra. The principal advantage in using higher values of M is in signal reconstruction at the output. This is explained in the following material.

In the case just discussed, the output in the time domain consists of a train of impulses. However, in a practical realization of the filter, the output impulse is usually sampled and held for some time. The actual fraction of the period for which the signal is held determines the frequency characteristics of the filter and is best illustrated with the help of Figs. 2.4 and 2.5. Fig. 2.4 shows that the sampled and held output is a convolution of a rectangle with an impulse train. This amounts to a multiplication of the transform of the two in the frequency of the original frequency spectra. This is illustrated in Fig. 2.5 for the sampled data filter output.

IV

RESULTANT OUTPUT IS THE
CONVOLUTION OF I & III.

RESULTANT OUTPUT IS THE MULTIPLICATION
OF I & III.

Fig. 2.3. Transversal filter sample data waveforms.

SAMPLE & HOLD OUTPUT
IN TIME DOMAIN

$$\sum_{n=-\infty}^{\infty} P_T(t - \frac{nT}{M})$$

*

I

II

III

I * II

Fig. 2.4. The effect of a sample and hold on an impulse train is shown to cause roll-off in the frequency domain.

Fig. 2.5. Effect of hold time on the sinc function roll-off.

The output signal $S(t)$ may be expressed

$$S(t) = Y(t) * P_T(t)$$

where $Y(t)$ is the output of the sampled data filter without the hold and $P(t)=1$, $0 \leq t < \tau$

$=0$, for all other t .

Hence,

$$S(t) = \sum_{i=0}^{N-1} \sum_{n=-\infty}^{\infty} h_i X(t-iT) \delta(t-nT/M) * P_T(t)$$

$$= \sum_{i=0}^{N-1} \sum_{n=-\infty}^{\infty} h_i X(nT/M-iT) P_T(t-nT/M)$$

In the frequency domain

$$|S(f)| = |Y(f)| \cdot |\text{sinc}(f\tau)|$$

where

$$\text{sinc}(x) = \frac{\sin \pi x}{\pi x}$$

$$= \text{Fourier Xform of } P_T(\tau).$$

The effect of the holding circuit is to cause the ideal filter transfer function to be multiplied by a sinc function. The sinc suppresses the higher frequency harmonics, and also controls to some extent roll-off in the baseband. The value of M can be chosen to improve both the higher out of band frequency suppression and roll-off of

17.

the baseband signal as shown in Fig. 2.6⁽¹⁴⁾. It is observed that baseband roll-off and out of band signal suppression are improved by increasing M the number of delays per section between tap weights. An optimum value of M=2 is immediately evident, as beyond this is a point of diminishing returns.

The above method of signal reconstruction may be alternatively viewed in terms of a low pass filter action. An ideal signal reconstruction requires a sinc function interpolation of the output impulse train from the filter. (This result comes from the sampling theorem) i.e. the output impulses are convolved with a sinc function in the time domain. This implies that perfect reconstruction would occur if the impulses are fed into an ideal lowpass filter (since a sinc is a rectangle in the frequency domain). The act of sampling and holding the impulses effectively achieves this low pass filter action.

2.3 ORGANIZATION OF PROPOSED PROCESSOR

The impulse response of the transversal filter shown in Fig. 2.1 is

$$Y(t) = h_0 \delta(t) + h_1 \delta(t-T) + \dots + h_{N-1} \delta(t-(N-1)T) \quad (2.2)$$

The impulse ripples through the delay line giving the consecutive tap weights as the output of the filter. Here, the filter tap weights are stationary in space and the analog information propagates through the filter.

r = baseband roll-off at folding frequency $1/2T$

s = maximum gain of out-of-band components (assuming input band-limited to $1/2T$)

M	r	r (dB)	s	s (dB)
1	.6366	-3.922	.6366	-3.922
2	.9003	-0.912	.3001	-10.455
3	.9550	-0.401	.1910	-14.380
4	.9750	-0.224	.1392	-17.126
5	.9836	-0.144	.1093	-19.228
6	.9886	-0.099	.0899	-20.927
7	.9916	-0.073	.0763	-22.352
8	.9936	-0.056	.0662	-23.578

Fig. 2.6. Effect of M (Number of Stages per Delay Section)

The structure of Fig. 2.7 has the analog information stationary in space, and the tap weights propagate past them. The impulse response of this structure is

$$Y(t) = h_0 \delta(t) + h_1 \delta(t-T) + \dots + h_{N-1} \delta(t-(N-1)T)$$

where T is the period of propagation, of the register containing $\{h_n\}$. The result is identical to that obtained for the earlier configuration Eqn. (2.2). However, the transversal filter realization of Fig. 2.7 has powerful advantages over that of Fig. 2.1. The $\{h_n\}$ are now not fixed on the chip but can be fed from outside. This yields a very powerful processor since now any FIR filter is theoretically implementable. Also the filter size (number of taps) can be arbitrarily increased by cascading chips - thus, a modular design of a chip becomes possible. The other important advantage arises from the fact that unlike the structure of Fig. 2.1 the analog information input does not have to propagate in an analog delay line. This eliminates the problems associated with charge transfer inefficiency⁽⁴⁾ associated with delay lines implemented with charge transfer devices.

The register containing $\{h_n\}$ need not be an analog delay line if one is willing to digitize the $\{h_n\}$ into its binary equivalent and feed the binary information into digital shift registers in parallel. In fact, the use of an analog delay line for the $\{h_n\}$ is not too practical since it creates problems of multiplying the $\{h_n\}$ with input $\{x_k\}$. Also, the concept of modularization (cascading ability) would be jeopard-

Fig. 2.7. The impulse is stored in the (say) first sample and hold element. The $\{h_n\}$ are propagating in the register below with time period T .

Fig. 2.8. Binary area ratioed capacitors required to achieve analog tap weight per tap position.

ized since the signal from an analog delay line has to be sensed and reprocessed before it can be inputted into the next structure. In contrast, the output of a digital shift register may be fed in directly to the input of a similar register in another chip.

The more practical alternative of digitizing the $\{h_n\}$ into its n -bit binary equivalent was therefore adopted for the processor. The n -bits are fed to n digital shift registers. The output of each bit is combined with appropriate binary weighting to reconstruct the analog input tap weight. The appropriate weighting necessary is implementable using binary ratioed capacitors as shown in Fig. 2.8. Binary ratioed capacitors have been successfully utilized in A/D conversion with high precision⁽¹¹⁾. Since the multiplication and summation in the filter has to be done in parallel, N such capacitor networks are required for a N tap filter.

The non-propagating registers, needed to sample and hold the input analog information, can be realized by a ring counter sampling unit with source follower buffer amplifiers as shown in Fig. 2.9.

The actual multiplication of two signals can be achieved by using the configuration of Fig. 2.10. The switch is controlled by a binary signal B , such that

$B = 1$ when switch is close-circuited

$= 0$ when switch is open circuited.

The output is $V_a C B / (C + C_{LOAD})$. Thus, B is multiplied by the analog information V_a . The binary bits representing the $\{h_k\}$ could control

Fig. 2.9. Sample and hold input stage controlled by a ring counter scan shift register.

Fig. 2.10. Schematic used to multiply B (a binary control signal) with the analog information V_a .

similar switches in the filter. Thus, the act of opening or closing a switch performs the multiplication.

The output is actually charge on a capacitor. Thus, if several outputs are joined together, the individual outputs become automatically added by virtue of charge summation at the common output node. Thus, the act of hard wiring the outputs of all the taps amounts to the act of summation.

In order to be able to handle negative tap weights, a two's complement notation⁽⁵⁾ can be used to code the n bits assigned to $\{h_n\}$. The output electrodes assigned to the MSBX2 (most significant bit) are tied together and brought out separately from those assigned for all the other bits. This will be referred to as the negative sense line. The other commoned sense electrodes will be called the positive sense line.

The overall organization of the processor is shown in Fig. 2.11.

Fig. 2.11. CHIP organization of the filter.

CHAPTER 3

CHIP LAYOUT AND DESIGN CONSIDERATIONS

3.1 INTRODUCTION

This chapter will deal with the actual realization of the various components, the design parameters involved and the constraints imposed by the chip layout and geometry.

The first section will deal with an optimum shift register design suitable for this application. It will be followed by a section on MOS capacitors and will deal with those aspects which will directly influence the filter characteristics. The section following this will deal with sample and hold units and buffer amplifiers. Finally, the actual hardware necessary for the realization of one tap weight position of the filter will be discussed.

3.2 SHIFT REGISTER DESIGN

3.2.1 Introduction

It is clear from the discussion of the chip organization that a good portion of the chip will have to be devoted to shift registers. Thus, it is important to have an efficient design for a shift register which, among other things, must be compact, be capable of driving large capacitive loads with reasonable speed, must not consume too much power and if necessary be able to operate with low clock voltages.

-
- * The ring counter is also a shift register under appropriate external control.

Various logic systems and families exist, a review of which would be tedious. Basically, logic systems may be classified as static or dynamic. In static logic, the information is "latched" in - it is available for as long as the power supply is on. In dynamic logic systems, the information is stored on capacitors and due to leakage the information is eventually lost (in a few hundred milliseconds or less). Hence, the information must either be periodically refreshed or be clocked to another storage site. Dynamic logic systems consume a smaller area on chip and dissipate less power compared to static logic systems.

Dynamic logic systems can be again classified as ratioed and ratioless logic. In ratioed logic systems, the output voltage is the resistive voltage divider of say 2 MOSFET's. This establishes a direct path from the power supply to ground and therefore dissipates appreciable power. In ratioless logic systems, no direct path to ground from the power supply exists. Hence, it dissipates far less power. Hence, ratioless dynamic logic was chosen to implement the shift registers.

There are various ways of implementing ratioless dynamic logic. The parameters involved become clear from the implementation of an inverter (from which all logic is derivable) as shown in Fig. 3.1. MOSN1 is kept non-conducting and the output capacitor is charged up to the logic "1" level through MOSN2. Then, the information (a '1' or '0') is applied to node '1'. If it is a '0', the output voltage remains a '1', alternatively, if it is a '1', MOSN2 starts to conduct and discharges C_{out} to the '0' level through node 4 (which is kept at ground during

Fig. 3.1. Basic implementation of an inverter.

Fig. 3.2. 1-bit delay of a shift register using inverters.

Fig. 3.3. 1-bit delay of a shift register using non-inverters.

this period). Common to most implementations is that the "1" level output voltage is one threshold voltage below the gate voltage of MOSN2 (assuming the gate voltage and drain supply voltage are of the same magnitudes as is normally the case). This necessitates the need to use higher supply voltages. Another problem that arises is that the drain and gate supply voltages being equal, the MOS transistor is working in saturation. This increases the charging time of the output capacitor. The speed can be improved by using a higher supply voltage for the gate compared to the drain. These drawbacks can be overcome by using bootstrapped logic structures^(6,7). These devices working on the same drain and gate voltage levels are capable of eliminating threshold voltage losses at the output, and can make the inverter work in the triode region of operation thus improving its switching speed. More important, its current driving capability is excellent and makes it ideal for driving large capacitive loads. This is the reason bootstrapped dynamic ratioless logic was chosen over all others, to implement the shift registers.

These systems can be designed to operate with two phase, 3 phase or 4 phase overlapping or non-overlapping clocks. The pros and cons of these systems have been discussed in Reference (6).

To keep system clocking requirements simple, a 2 phase non-overlapping clocking scheme was preferred.

Usually, shift registers are implemented by cascading inverters as shown in Fig. 3.2. If one could use non-inverters to implement the

shift registers considerable advantages result. Fig. 3.2 shows a bit delay of a shift register using two cascaded inverters. Fig. 3.3 shows a bit delay of a shift register using 2 cascaded non-inverters. Information can be entered into the system at every bit delay only. Now, we will use the shift registers to carry "1"'s or "0"'s and we will use these as strobes to open and close switches. Referring to Fig. 3.2, it is seen that only 1 strobe per bit delay is available in that structure (node B cannot be used as a strobe since the information there is inverted). However, it is observed that for the structure of Fig. 3.3 2 strobes per bit delay are available (node B provides the extra strobes as now the information is not inverted). The area required to implement both structures is approximately the same. Hence, a non-inverter implementation was preferred. The extra strobe obtained does not carry any new information (the bit rate of the structure is unchanged) but can be used to multiplex another channel containing the same filter function. The two strobes obtained per bit are separated by a $1/2$ bit delay and the resulting transversal structure is similar to that of Fig. 2.2, with $M=2$. This multiplexing action, as previously explained in Section 2.2, improves signal reconstruction at the output. The block diagram of the filter now becomes that as shown in Fig. 3.4. A 2 phase shift register would give 1 strobe during ϕ_1 and another strobe during ϕ_2 for 1 bit delay; ϕ_1 and ϕ_2 being the 2 non-overlapping clocks it requires. Also, the outputs of the ϕ_1 strobe must be "0" after ϕ_1

Fig. 3.4. Block diagram of the filter.

goes low and similarly the output of the ϕ_2 'strobe' must become '0' after ϕ_2 goes low. Thus, we have 2 identical filters, one working during ϕ_1 and another a 1/2 bit later during ϕ_2 . This particular structure has other useful applications, among them being the ability to cascade 2 identical filters. This cascading ability is important for achieving a low pass filter with a high stop band attenuation.

3.2.2 Circuit Schematic

Fig. 3.5 shows the basic non-inverter bit delay of the 2 phase ratioless dynamic bootstrapped structure that was used to implement the shift register.

The mode of operation may be explained as follows. During time slot T1, ϕ_2 is on turning on MOSN1. The information is thus gated on the MOS capacitor gate. ϕ_2 then turns off isolating the gate of the capacitor. If the information is a high on node 1, MOSN3 turns on and the gate of MOSN5 is held at ground by ϕ_2 . If the information was a low, the gate of MOSN5 has a high voltage on it (which is retained from when ϕ_2 went off) and thus MOSN5 would be conducting. During T3, ϕ_1 turns on and delivers a kick to node 1 assuming C1 is switched on. If the capacitor is not switched in, no kick is delivered. The kick is delivered through the gate controlled capacitor C1. If a high (logic '1') voltage is present on node 1, the capacitor is "switched in"; otherwise, it is switched off. If the capacitor is switched off, MOSN2 is kept in a non-conducting state. The gate of MOSN5 has a high voltage on it.

Fig. 3.5 Bit delay of the noninverter

(This high voltage was retained from the last time slot when ϕ_2 was on.) ϕ_2 being on charged up the gate of MOSN5 high through MOSN4. ϕ_2 then goes off and a high voltage is retained on the gate of MOSN5, thus forcing the output to ground through MOSN5. (It is to be noted that MOSN2 is kept off when MOSN5 is on, thus avoiding a direct path from the supply to ground.) Thus, a logic "0" input results in a logic "0" output.

On the other hand, if a logic "1" input exists, i.e. node 1 is high, C1 is "switched in" and when ϕ_1 turns on during T1, it delivers a kick to node 1 (which is floating) and bootstraps it to a high voltage level. Node 2 starts charging up to ϕ_1 voltage level. If the voltage on node 1 is increased sufficiently by the bootstrap kick from the capacitor, the output voltage level would be equal to the ϕ_1 voltage level (thus eliminating all threshold voltage losses). Increasing the gate voltage forces MOSN2 into the triode region of operation giving it a good capacitive drive capability. During this time, MOSN5 is kept in a non-conducting state (MOSN3 is conducting due to a logic "1" on its gate; hence, ϕ_2 which is "0" at this time is connected to the gate of MOSN5).

Thus, a logic "1" input results in a logic "1" output. The outputs are valid only during the clock "on" time, i.e. during T1, T3, T5, etc. At all other times, they are forced to remain at "0". That is, for every bit delay, we will have 2 strobes, one during ϕ_1 and another during ϕ_2 .

In the next section, the parameters that determine the output voltage levels, speed, and thus the area of the non-inverter will be discussed.

3.2.3 Design Parameters

The gate controlled capacitor (varactor) is essential to the bootstrap operation of the non-inverter. The operation of these capacitors is explained with reference to Fig. 3.6. The gate of the MOST and varactor is precharged to V_{so} volts ($V_{so} > V_{To}$, the threshold voltage) and left floating. This causes a large capacitance to appear between the gate and drain of the MOST. This consists of the varactor capacitance as well as the capacitance due to the gate of the MOST. A pulse of height V_d (assumed to be an ideal step) is then applied to the drain. The application of the pulse causes a potential well to form at the drain and this will cause all the excess charge in the channel in the vicinity of the well to flow into it by field aided diffusion. The transfer of charge into the diffusion from under the gate of the varactor results in a change in the surface potential of the varactor. This change is reflected to the gate of the varactor and MOST via the insulator capacitance.

The steady state behaviour of these structures has been worked out in detail in Reference (6).

The output voltage level (for the logic "1" state) is dependent on the final voltage at the varactor gate. If the output voltage is to equal the ϕ_1 voltage level (see Fig. 3.5) the voltage on the varactor

The basic structure whose dynamics are to be investigated. The gate is assumed to be isolated.

Fig. 3.6. Structure showing the MOS varactor and MOS device layout (cross-section).

gate must be greater than ϕ_1 by at least one threshold voltage (the threshold voltage $V_T = V_{TO} + K_1 \sqrt{V_{out}}$; K_1 is a function of the doping of the chip and normally has a value between .5 to 2.0). The final output voltage of the varactor is determined by three parameters: the initial voltage V_{SO} to which the varactor was precharged to and floated prior to receiving the bootstrap kick, the substrate doping of the chip, and the bootstrap ratio r ($r = C_{ox} / (C_{ox} + C_{LOAD})$) where C_{ox} is the total oxide capacitance between the gate and drain of the device and C_{LOAD} is the total capacitive loading to ground of the gate of the device excluding C_{ox} . The amount of mobile charge transferred under the gate of the varactor due to a pulse applied to its drain is the item of interest.

If all the channel charge is not transferred, then we can conclude that full pulse height would appear under the gate of the varactor and be reflected on to the gate. If, however, all the channel charge is transferred out, the full pulse height would not appear under the varactor gate and the bootstrap would not be effective. o

The factors that govern the amount of mobile charge that has to flow out in order that the surface potential may rise to a certain value depend on three parameters: bootstrap ratio, the substrate doping and the initial voltage on the gate before application of the pulse to the drain of the varactor.

In strong inversion (assuming a step junction) and using standard 1-dimensional MOSFET theory and assumptions⁽²⁴⁾,

$$V_G = V_{FB} + 2\phi_f + V_S + \frac{(2\epsilon_s \epsilon_o q N / V_S + 2\phi_f)^{1/2}}{C_o} - \frac{q}{C_o}$$

where

V_S = quasi-Fermi level for the mobile charge in the inversion layer

V_G = gate voltage of varactor

ϕ_f = bulk Fermi potential

N = substrate doping density

V_{FB} = flatband voltage

C_o = oxide capacitance per unit area

q = mobile channel charge

ϵ_s = dielectric constant for silicon

ϵ_o = free space permittivity

Also,

$$V_G = V_{SO} + \frac{C_{ox}}{C_{ox} + C_e} V_S = V_{SO} + r V_S$$

where r is the bootstrap ratio and C_e is the capacitive load of the varactor to ground.

Using these two equations, the effect of V_{SO} , N and r on the channel charge transferred from under the varactor gate may be determined and is shown in Figs. 3.7 to 3.9. The design should be such that the channel is not lost (100% charge transfer does not take place)

Fig. 3.7. Effect of boot strap ratio on the amount of mobile charge transferred from under the gate of a varactor due to a pulse delivered to the diffusion.

Fig. 3.8. Effect of substrate doping on the amount of mobile channel charge transferred from under the gate of a varactor due to a pulse delivered to the diffusion.

Fig. 3.9. Effect of precharge gate voltage on the amount of mobile charge transferred from under the gate of a varactor due to a pulse delivered to diffusion. V_{SO} is the initial gate voltage.

for the operating conditions of the system. Fig. 3.10 shows the effect of N on the minimum gate voltage needed to retain a channel. Fig. 3.11 shows the maximum voltage to which the varactor gate may be taken as a function of r and V_{SO} . This may be derived as follows^(6d):

$$V_{G_{max}} = V_{d_{max}} + K_1 (\sqrt{V_{d_{max}} + 2\phi_f} - \sqrt{2\phi_f}) + V_{TO}$$

$$= V_{SO} + r V_{d_{max}}$$

From the above,

$$V_{G_{max}} = V_{SO} + r \left\{ \frac{2\alpha\gamma + K_1^2}{2\alpha^2} \left[1 - \sqrt{1 - \frac{4\alpha^2\gamma^2}{(2\alpha\gamma + K_1^2)^2}} \right] \right\}$$

where

$$K_1 = \frac{\sqrt{2\epsilon_s \epsilon_o q N}}{C_o}$$

$$\alpha = 1 - r$$

$$V_{SO} - V_{TO} = \gamma$$

The dynamic or transient response of the varactor is determined by the excess charge transfer on the inverted silicon surface. The application of a pulse to the drain of a varactor results in charge transfer out of the channel. As charge goes out of the channel, the surface potential increases and this is reflected to the gates of the varactor. Thus, the rise time of the varactor gate is the channel charge transfer time. The basic equation of charge transport along the surface of the MOS

Fig. 3.10. Minimum gate voltage necessary to retain channel under varactor gate for different surface potentials is shown. The minimum gate voltage is also the maximum gate voltage to which the varactor may be raised due to the given surface potential.

Fig. 3.11. Maximum voltages to which the gate of the varactor may be raised as a function of initial voltage for different boot strap ratios.

varactor is (6a):

$$\frac{\partial f}{\partial t} = \frac{\partial}{\partial x} \left[\mu C_o \frac{(V_{SO} - V_{TO})}{C_T} f \frac{\partial f}{\partial x} \right]$$

$$= \frac{\partial}{\partial x} \left[D_{eff} \frac{\partial f}{\partial x} \right]$$

where

$$D_{eff} = \frac{\mu C_o (V_{SO} - V_{TO})}{C_T}$$

$$C_d = \frac{\epsilon_s \epsilon_o q (N_a N_d)}{Q_T + \rho}$$

$$C_T = C_o + C_d$$

q = electronic charge

N_a = acceptor concentration in the bulk

N_d = donor concentration in the bulk

Q_T = charge density on the gate of the varactor

x = distance along the length of the varactor

μ = surface mobility

V_{SO} = precharge voltage on the varactor gate

V_{TO} = threshold voltage

$$f = \frac{\rho}{\rho_{max}} = \frac{\rho}{C_o (V_{SO} - V_{TO})} = \text{fraction of the equilibrium value of the charge under the gate}$$

The equation is similar to the diffusion equation for motion of minority carriers with the diffusion coefficient being dependent on the carrier density itself. The equation does not have a closed form solution, but with certain assumptions^(6a), the time taken to transfer 90% of the channel charge, $t_{90\%}$, can be defined as:

$$t_{90\%} = \frac{6.2}{\mu} \frac{L^2 (C_o + C_d)}{C_o (V_{SO} - V_{TO})}$$

where L is the channel length.

Fig. 3.12 illustrates the results of this equation. The charge transport equation was also solved numerically^(6b), and the results are shown in Fig. 3.13.

For fast operation, the channel length therefore must be kept small and the precharge voltage V_{SO} high. Substrate doping should also be kept low. Once the final gate voltage is known, the dimension of the MOS transistor charging up the output capacitor may be worked out using standard MOS theory^(8a). A compromise on the W/L (width to length ratio) vs speed attainable is required as a large W/L requires more chip area.

Another factor that is also important is the ratio of the overlap capacitance from the drain of MOSN2 and diffusion of C1 to node 1 to the total load to ground on node 1 (see Fig. 3.5). This ratio should be kept very small, so that the kick delivered by ϕ_1 (when node 1 is storing a "0") does not introduce erroneous information on node 1.

Fig. 3.12. Curves shown the 0-90% rise time of the varactor for different $V_{SO} - V_{TO}$ for various values of L , the length of the varactor.

Fig. 3.13. Normalized channel charge density as a function of distance from the drain for various times elapsed after application of a step voltage to the drain.

The design data obtained from the procedure described was tested by computer simulations before an actual layout of the circuit was done.*

The filter required eight banks of these shift registers - one being the ring counter and the other seven being the tap weight digital shift registers. The layout had to be such that the pitch (length) of the shift registers had to be minimized without exaggerating its width, as the pitch would ultimately determine the number of taps that can be accommodated on one chip. The outputs of all the shift registers were brought out to pads so that chips could be cascaded if necessary.

Fig. 3.14 shows the layout of a $1/2$ bit delay of the shift register.

3.3 SAMPLE AND HOLD UNIT AND BUFFER AMPLIFIER

3.3.1 Circuit Schematic

The basic sampling unit and the buffer amplifier are shown in Fig. 3.15.

MOSN1 samples in the analog information and stores it on node 1. MOSN2 and MOSN3 make up a source follower buffer amplifier. The voltage on node 2 (the output of the buffer amplifier) is one threshold voltage below that of node 1. If the voltage on node 1 decreases from its previous value, node 2 cannot respond to this change if MOSN3 was not included in the circuit. This is because node 2 voltage is greater than the voltage on node 1 and the channel under MOSN2 disappears.

* NANSIM, a simulation routine developed at Bell-Northern Research, was used. Circuit schematic was designed initially using data obtained by analytical means. This design was optimized using the simulation package.

FIG 3.14. Layout of 1/2 bit of the shift register.

Fig. 3.15. Sampling unit and buffer amplifier.

Fig. 3.16. Introduction of additional oxide capacitance onto the sample and hold capacitance through MOSN4.

MOSN3 behaves like a resistor and discharges the output voltage appropriately such that the channel under MOSN2 is restored and node 2 is allowed to follow node 1.

The signal on node 1 is stored on the gate capacitance of MOSN2 and the junction capacitance of the source of MOSN1. The information on node 1 would be accurate if node 1 was heavily loaded capacitively, as this would reduce the error due to kick received from the sampling clocks through the overlap capacitance. Also, the information may need to be stored on node 1 for a considerable period of time, specially for low frequency audio applications. The junction capacitance of the source of MOSN1 causes the voltage of node 1 to leak away due to generation processes. To reduce this leakage, provision was made to switch on additional oxide capacitance on to node 1 as shown in Fig. 3.16. The switch MOSN4 was included because the extra capacitance may not be desirable for high frequency applications, since it will slow down the circuit operation. Fig. 3.17 shows the layout of one sample and hold buffer source follower unit.

3.3.2 Linearity of Buffer Amplifiers

The linearity of the source follower buffer amplifiers is of key concern. As will be shown later, the principal source of non-linearity in the filter chip can be attributed to the source follower buffer amplifiers. Hence, a lot of effort was directed towards a solution of this problem. The following section is a quantitative analysis

FIG 3.17. Layout of one sample and hold stage with buffer amplifier.

of the non-linearity in the source followers. It will be followed by a section where a novel technique of reducing the non-linearity will be presented.

From a simple one dimensional model of a MOSFET, it can be shown^(6c,8) that for the MOSFET of Fig. 3.18a, the increase in threshold voltage ΔV_T due to V_{SUB} is given by (in strong inversion):

$$|\Delta V_T| = K_1 \left[\sqrt{V_{SUB} + 2\phi_F} - \sqrt{2\phi_F} \right]$$

where

$$K_1 = \frac{\sqrt{2\epsilon q N}}{C_O}$$

C_O = gate oxide capacitance per unit area

N = substrate doping density

V_{SUB} = substrate bias

ϕ_F = Fermi potential

ϵ = permittivity of silicon

q = electronic charge

Similarly, the increase in threshold voltage due to V_{out} at the source of the MOSFET (Fig. 3.18b) is given by:

$$\Delta V_T = K_1 \left[\sqrt{V_{out} + V_{SUB} + 2\phi_F} - \sqrt{2\phi_F} \right] \quad (3.1)$$

Fig. 3.19 shows the configuration which is to be analyzed. The non-linearity of the source follower arises from the non-linear behaviour of the depletion capacitance with voltage. A series expansion of the

Fig. 3.18a. Configuration used to calculate increase in threshold voltage of the FET.

Fig. 3.18b. Configuration used in non-linearity analysis.

Fig. 3.19. Figure explains the terminology used in the derivation.

non-linearity will now be done.

We have

$$V_{out} = V_G - V_T = (V_{dc} + V_g \sin \omega t) - V_T \quad (3.2)$$

where

V_{dc} = dc bias on the signal

V_g = peak amplitude of the input sinusoidal signal

V_T = threshold voltage under the operating conditions.

Using (3.1),

$$V_T = V_{TO} + K_1 (\sqrt{|V_{out}| + |V_{SUB}| + |2\phi_f|} - \sqrt{|2\phi_f|})$$

From (3.2),

$$V_{out} = V_{dc} + V_g \sin \omega t - V_{TO} - K_1 (\sqrt{|V_{out}| + |V_{SUB}| + |2\phi_f|} - \sqrt{|2\phi_f|}) \quad (3.3)$$

or

$$K_1 \sqrt{|V_{out}| + |V_{SUB}| + |2\phi_f|} = V_{dc} + V_g \sin \omega t - V_{TO} + K_1 \sqrt{|2\phi_f|} - V_{out}$$

Squaring both sides and rearranging, we get

$$\begin{aligned} & V_{out}^2 + V_{out} \left[-2(V_{dc} + V_g \sin \omega t - V_{TO} + K_1 \sqrt{|2\phi_f|}) - K_1^2 \right] - K_1^2 (|V_{SUB}| + |2\phi_f|) \\ & + (V_{dc} - V_{TO} + K_1 \sqrt{|2\phi_f|})^2 + V_g^2 \sin^2 \omega t + 2(V_{dc} - V_{TO} + K_1 \sqrt{|2\phi_f|}) V_g \sin \omega t \\ & = 0 \end{aligned}$$

or

$$AV_{out}^2 + BV_{out} + C = 0$$

where

$$A = 1$$

$$B = -2(V_{dc} + V_g \sin \omega t - V_{TO} + K_1 \sqrt{|2\phi_f|}) - K_1^2$$

$$C = -K_1^2(|V_{SUB}| + |2\phi_f|) + (V_{dc} - V_{TO} + K_1 \sqrt{|2\phi_f|})^2 + V_g^2 \sin^2 \omega t \\ + 2(V_{dc} - V_{TO} + K_1 \sqrt{|2\phi_f|})V_g \sin \omega t$$

Also

$$B^2 - 4AC = K_1^4 + 4K_1^2(V_{dc} - V_{TO} + K_1 \sqrt{|2\phi_f|} + V_g \sin \omega t) + 4K_1^2(|V_{SUB}| + |2\phi_f|) \\ = K_1^2 \{ K_1^2 + 4(V_{dc} - V_{TO} + K_1 \sqrt{|2\phi_f|}) + 4V_g \sin \omega t + 4(|V_{SUB}| + |2\phi_f|) \} \\ = K_1^2 \{ K_1^2 + 4(V_{dc} - V_{TO} + K_1 \sqrt{|2\phi_f|}) + 4(|V_{SUB}| + |2\phi_f|) \\ \left\{ 1 + \frac{4V_g \sin \omega t}{K_1^2 + 4(V_{dc} - V_{TO} + K_1 \sqrt{|2\phi_f|}) + 4(|V_{SUB}| + |2\phi_f|)} \right\} \}$$

Writing

$$K_1^2 + 4(V_{dc} - V_{TO} + K_1 \sqrt{|2\phi_f|}) + 4(|V_{SUB}| + |2\phi_f|) = \beta$$

$$\begin{aligned}
\sqrt{B^2 - 4AC} &= +K_1 \left\{ 1 + \frac{4V_g \sin \omega t}{\beta} \right\} \sqrt{\beta} \\
&= +K_1 \left\{ 1 + \frac{1}{2} \frac{4V_g \sin \omega t}{\beta} - \frac{1}{2} \cdot \frac{1}{4} \frac{4V_g \sin \omega t^2}{\beta} + \dots \right\} \sqrt{\beta} \\
&= +K_1 \left\{ 1 + \frac{2V_g \sin \omega t}{\beta} - \frac{2V_g^2 \sin^2 \omega t}{\beta} + \dots \right\} \sqrt{\beta}
\end{aligned}$$

The expansion is carried on for up to the second harmonic only, as this is the dominant source of non-linearity in source followers. Thus,

$$\sqrt{B^2 - 4AC} \approx +K_1 \sqrt{\beta} \left\{ 1 - \frac{V_g^2}{\beta^2} + \frac{2V_g \sin \omega t}{\beta} + \frac{V_g^2}{\beta^2} \cos 2\omega t \right\}$$

Now

$$V_{out} = \frac{-B + \sqrt{B^2 - 4AC}}{2A}$$

Hence

$$\begin{aligned}
V_{out} &= 2(V_{dc} + V_g \sin \omega t - V_{TO} + K_1 \sqrt{|2\phi_f|}) + K_1^2 + K_1 \sqrt{\beta} \left\{ 1 - \frac{V_g^2}{\beta^2} + \frac{2V_g \sin \omega t}{\beta} \right. \\
&\quad \left. + \frac{V_g^2}{\beta^2} \cos 2\omega t \right\}
\end{aligned}$$

Only the minus sign is retained since substitution of the above satisfies equation (3.3) only if the minus sign is used.

Thus,

$$V_{out} = (V_{dc} + V_g \sin \omega t - V_{TO} + K_1 \sqrt{|2\phi_f|}) + \frac{K_1^2}{2} - \frac{K_1 \sqrt{\beta}}{2} \left\{ 1 - \frac{V_g^2}{\beta^2} \right\}$$

$$\left. \begin{aligned} &+ \frac{2V_g \sin \omega t}{\beta} + \frac{V_g^2}{\beta^2} \cos 2\omega t \end{aligned} \right\}$$

Thus,

$$\begin{aligned} V_{out}(\text{fundamental}) &= V_g \sin \omega t - \frac{K_1 \sqrt{\beta}}{2} \cdot \frac{2V_g \sin \omega t}{\beta} \\ &= V_g \sin \omega t - \frac{K_1}{\sqrt{\beta}} V_g \sin \omega t \\ &= V_g \sin \omega t \left(\frac{1-K_1}{\sqrt{\beta}} \right) \end{aligned}$$

The second harmonic term is

$$\frac{-K_1 \sqrt{\beta}}{2} \cdot \frac{V_g^2}{\beta^2} \cos 2\omega t$$

Thus, the second harmonic content of the output relative to the fundamental is:

$$\begin{aligned} \text{S.H.R.F. (second harmonic} &= \frac{\left| \frac{-K_1 \sqrt{\beta}}{\beta^2} \frac{V_g^2}{\beta^2} \right|}{\left| V_g \left(1 - \frac{K_1}{\sqrt{\beta}} \right) \right|} = \frac{\left| \frac{K_1 \sqrt{\beta} V_g}{2\beta^2 \left(\frac{K_1}{\sqrt{\beta}} - 1 \right)} \right|}{\left| \right|} \\ \text{relative to} & \\ \text{fundamental)} & \end{aligned}$$

Figs. 3.20a and b and Figs. 3.21a and b present a comparison of the experimentally obtained value of the second harmonic content (relative to fundamental) of a source follower under different conditions of operation with that predicted in the equations derived in this section.

Fig. 3.20a.

Fig. 3.20b. Experimental verification of the formula predicting the second harmonic content in the output signal.

Fig. 3.21a. Experimental verification of the formula predicting the second harmonic content in the output signal.

Fig. 3.21b. Theoretically expected second harmonic content as a function of the doping density of the substrate.

3.3.3 Linearization of the Source Follower Stage

From the discussion in the last section, it is evident that parameters such as input signal amplitude, dc signal bias, chip substrate doping density have to be kept at appropriate values in order to minimize the non-linearity of the source follower stage.

In this section, a method will be presented which will, by incorporating feedback in the source follower stage, linearize the behaviour. A similar technique was used by MacLennan and Mavor⁽⁹⁾ to linearize the input stage of a CCD.

Essentially the linearization is achieved by placing the network to be linearized in the forward loop of a high gain operational amplifier operating in the voltage follower mode^(10a) as shown in Figs. 3.22 and 3.23.

Since the non-inverting input of the operational amplifier is forced to follow the inverting (signal input) input (see Figs. 3.22 and 3.23), the output of the circuit becomes linearized. Fig. 3.23 shows the schematic required to linearize a source follower amplifier. The two sampling gates MOSN1 and MOSN3 operate in the triode region of operation. The operational amplifier has a gain since its output has to be 1 threshold voltage above the output (which is assumed to be identical to the input signal). Thus, the operating region (dc signal bias at the input) would be different from that occurring without the use of the linearizing circuitry.

Fig. 3.22. Operational amplifier working in the voltage follower mode.

Fig. 3.23. Schematic required to linearize a source follower amplifier.

Let V_{in} be the input to the non-inverting input of the operational amplifier and let V_{out} be its output. Then,

$$V_{in} = V_{\text{source follower output}} = V_{out} - V_T$$

Therefore,

$$V_{out} = V_{in} + V_T = V_{in} + V_{TO} + K_1 (\sqrt{V_{out} + V_{SUB} + 2\phi_f} - \sqrt{2\phi_f})$$

Solution of this equation will yield the gain of the operational amplifier as a function of V_{SUB} , N and V_{in} . Fig. 3.24 shows the results obtained from such a solution. The gain of the operational amplifier will determine the dc bias and ac signal amplitude that need be applied to the input of the operational amplifier such that the input sampling stage is in its proper range of operation (does not become saturated).

The operational amplifier in order to work properly needs a high slew rate. It also may need to be over compensated to achieve proper stability of operation. Introduction of large capacitors (at say node 1, Fig. 3.23) could, for example, cause oscillation. The general criteria in order to achieve stable operation is not to introduce any corner frequency higher than or equal to ω_c^2 / ω_u where ω_c is the open loop corner frequency and ω_u is the unity gain point of the operational amplifier (see Fig. 3.25).

Fig. 3.24. The transfer characteristics of the amplifier under different operating conditions.

Fig. 3.25. From the figure, $W_U/W_C = K$; $W_C/W = K$ or $W = W_C/K = W_C^2/W_U$. Thus, no corner frequencies should be introduced such that $W > W_C^2/W_U$ since that would introduce a phase shift of 180° at W_C and oscillations could take place.

The behaviour of the linearizing circuitry was first studied using discrete circuit components to simulate its behaviour. Figs. 3.26 to 3.30 show the behaviour of the circuit qualitatively under different conditions of operation (discussion of each situation included in the respective figure).

The linearizing circuitry also has another important benefit. It helps remove differences in gains and offsets of each source follower amplifier stage in the transversal filter. Differences in gain and offset in the source follower amplifiers gives rise to fixed pattern noise (FPN). This is treated in more detail in Chapter V.

Linearity measurements using discrete components showed that, using the feedback mechanism, one could cut down the second harmonic content at the output of the source followers by better than 20dB. The other harmonics (all of which are smaller than the second harmonic) are also suppressed.

Results obtained by using the linearizing technique on the filter chip will be presented in Chapter V.

Fig. 3.31 shows the actual schematic used in the filter chip to linearize the source followers.

3.4 DESIGN CONSIDERATIONS AND SIGNAL INTRODUCTION TO THE TAP WEIGHT CAPACITORS

In this section, the linearity of MOS capacitors to be used for the tap weights will be discussed. The method of inputting the analog information to these capacitors is one of key concern and is also

Fig. 3.26. The effect of a continuous feedback loop is shown here. The top trace is the input to the operational amplifier (2V/div). The second trace is the input to the inverting input of the op. amplifier (2V/div). The third trace is the output of the sampler (node 1; 5V/div) and bottom trace is the output of the op. amplifier (5V/div). Horizontal sensitivity is 20μsec/div. All ground levels are on grid lines immediately below the traces.

Fig. 3.27. The effect of pulsing the outer MOST is shown here. The traces (from top) are ϕ_2 (10V/div); INPUT (2V/div); inverting input of op. amplifier (2V/div); op. amplifier output (10V/div) ... Horizontal sensitivity is 50μsec/div, with all ground levels being immediately below the traces on the grid. Note when ϕ_2 is off, the inverting input to the amplifier slowly discharges (through input impedance of op. amplifier and MOS junction diffusion) and the op. amplifier output jumps to saturation levels.

Fig. 3.28. The effect of sampling on the inner MOS device is shown here. Everything else is identical to the situation in the last figure.

Fig. 3.29. A completely sampled system is shown here. The traces are as shown in the last figure.

Fig. 3.30. A sinusoidal input is used here. The traces are (from top) ϕ_2 (10V/div); INPUT (2V/div); output of source follower (2V/div); op. amplifier output (10V/div). Horizontal sensitivity is 50 sec/div. The system is working at its Nyquist limit.

Fig. 3.31. Actual schematic used in the filter chip to linearize the source follower input stage.

discussed here. Finally, the factor that determines the dimensions and layout of these capacitors is discussed.

3.4.1 Linearity of MOS Gate Oxide Capacitance

This section will consider the linearity achievable by using MOS gate oxide capacitors as the tap weights in the filter.

For this purpose, an experiment was set up in which the semiconductor surface was modulated by a sinusoidal voltage source and the gate was floated by a MOSFET working in the saturation region of operation. The experimental setup and results obtained are shown in Figs. 3.32a and b. The results show that under strong inversion conditions (high gate voltage) and moderate substrate bias (to prevent any thick oxide field inversion, if any) excellent linearity may be obtained from these capacitors.

3.4.2 Introduction of Analog Information to Capacitor Banks

The only other real time electrically programmable correlator that has been presented to date⁽¹⁾ also uses MOS capacitors to achieve its tap weights. The tap weights in their structure were not analog (1 bit binary) and the input method was different. Fig. 3.33 illustrates the relevant equivalent circuit used to calculate the output of their filter. The analysis of this circuit yields the output voltage ΔV_r as seen by:

$$\Delta V_r = \sum_{j=1}^N \frac{Q_j \phi_j C_{oj}}{(C_L + C_T)(C_{sj} + C_{oj}) + C_{oj} C_{sj}} \quad (3.4)$$

Fig. 3.32a. Linearity measurements on the basic multiplying structure used in the filter.

Fig. 3.33. The equivalent circuit used to calculate the output voltage when charge from several cells are transferred under a single floating electrode for the existing 1-bit tap weight correlator.

where Q_j represents the charge available for transfer in cell j and δ_j is one of the elements of the transfer vector which may take on the values of 0 or 1. C_T is the total cell capacitance and is given by

$$C_T = \sum_{i=1}^N \frac{C_{oi} C_{si}}{C_{oi} + C_{si}} \quad i \neq j$$

Now, due to differing surface potentials in the reservoirs C_{si} could vary from cell to cell and the resultant output (Eqn. 3.4) will not be a true superposition of all the individual inputs Q_i . The disadvantages of this structure may be summarized as follows⁽¹⁾:

- i) The relationship between the charge stored and the signal voltage applied to the input diffusion is non-linear because of the voltage dependence of the depletion capacitance of the storage reservoirs.
- ii) The relationship between the output voltage and the transferred charge is also non-linear because of the voltage variation of the depletion capacitance.
- iii) Intermodulation or crosstalk between cell signals occurs by virtue of the complex relation between the final voltage on the receiver electrodes and the total charge transferred.

The entire problem can be by-passed if one works with voltage sources (instead of injecting charge) as the analog information. This is the approach adopted for the proposed processor. Figs. 3.34 and 3.35 show the basic equivalent circuit proposed. It is to be noted that, at

Fig. 3.34. Actual structure required to implement each unit of Fig. 3.35.

Fig. 3.35. Basic structure of the filter using constrained voltage sources to drive the semiconductor surface of the capacitors.

all times, the semiconductor side of the gate oxide capacitance is either held at a reference voltage (say ground) or at the information voltage level (by source follower voltage buffer amplifiers). V_R is a reference voltage (say ground), SW , $\overline{SW}$ and SR are switches, and V_{dd} is a fixed dc voltage. The circuit operation may be described as follows:

- i). The switch $\overline{SW}$ is close circuited to set the bottom plate (semiconductor side) of the capacitor to reference potential; at the same time, SR is close circuited to constrain the sensing node at V_{dd} volts. This is the reset mode.
- ii) For a "0" tap weight, SW remains open and $\overline{SW}$ remains closed circuited. For a "1", SW is closed circuited and $\overline{SW}$ is open circuited. The sensing node voltage for a "1" in the i th tap (with "0"'s in others) becomes:

$$V_{out} = V_{dd} + (V_S - V_R) \frac{C_i}{C_T}$$

where

$$C_T = \sum_{i=0}^{N-1} C_i$$

C_T the total capacitance to ground remains the same. Hence there are no interactions between the taps.

Summation of individual outputs from each tap position is achieved simply by hardwiring the output sense electrodes of all the tap positions.

Fig. 3.36 shows a schematic of the proposed filter. C_{hi} , $i=0$ to $N-1$ are gate oxide tap weight capacitors and C_{si} is the semiconductor depletion capacitance under the tap weight capacitors. ϕ_1 and ϕ_2 represents the 2 separate channels of the filter. When one channel has its semiconductor surface grounded, the other one is operative. If the i th tap weight is switched in, $\delta_i=1$ and V_i is connected to the semiconductor surface. Otherwise, the semiconductor surface is grounded and $\delta_i=0$.

We assume that C_{hi} , $i=0$ and $N-1$ are all linear capacitors. The output voltage for the i th tap location assuming all other voltage sources are not switched in is:

$$V_{out} = \frac{V_i C_{hi}}{\sum_{i=0}^{N-1} C_{hi} + C_L}$$

where C_L is the loading on the structure.

In general, for an arbitrary number of taps switched in,

$$V_{out} = \frac{\sum_{i=0}^{N-1} \frac{V_i C_{hi} \delta_i}{\sum_{j=0}^{N-1} C_{hj} + C_L}}{\sum_{i=0}^{N-1} \frac{V_i C_{hi} \delta_i}{C_T + C_L}} = \frac{\sum_{i=0}^{N-1} V_i C_{hi} \delta_i}{C_T + C_L}$$

where C_T is the total oxide tap weight capacitance existing on the chip. The output voltage is a linear superposition of the output signals from each individual cell.

Fig. 3.36. C_{h_i} , $i=0, N-1$ represents the capacitance of each tap weight (ϕ_1) , (ϕ_2) represents the two channels in the proposed multiplexed structure. When the (ϕ_2) channel is working, the semiconductor surface under all the (ϕ_1) electrodes are grounded. C_L represents the capacitive loading, if any, on the electrodes. If a "1" is present, the shift register for the i th tap location, V_i , is switched in and $\delta_i=1$. Otherwise, the surface under the i th tap electrode is grounded and $\delta_i=0$.

3.4.3 Layout and Dimensions of the Capacitors

The time response of the MOS capacitors is the time taken by the charge to transfer from under the electrode. The situation is similar to the discussion in Section 3.2.3. The time response of the capacitors is shown in Figs. 3.12 to 3.13. In order to keep the response time short, the length L of the oxide electrodes must be kept small (see Fig. 3.6).

The next important consideration is the size and geometry of the smallest significant binary area ratioed capacitor. The size of this smallest capacitor will ultimately determine the size (area) of the chip since all other capacitors will be multiples of it. Thus, in order to design for a small chip area, very small dimensions should be chosen for this capacitor. However, this dimension should not be so small that the output from it is buried in chip noise and errors (resulting from non-ideal definition of the thin oxide boundary due to variation in mask aligning, etching and non-uniform gate oxide thickness). Unfortunately, no concrete data in this regard is available in the literature but work is going on in this area⁽¹¹⁾. The accuracy with which one can define a capacitor is another important consideration as errors would appear as tap weight errors and would cause errors in the transfer function of the filter.

The logic in the chip was designed for 10MHz. Using this number as a basis and Fig. 3.12; the length of the electrode (L) was chosen to

be 40μ for all the capacitors except the smallest (LSB) which was kept at 20μ . This reduces the sizes of all subsequent capacitors by a factor of 2, which results in significant reduction in the area of the chip. The width of the LSB bit was arbitrarily kept at 8μ ; thus, the sizes of the capacitor were (starting with the LSB) 20×8 , 40×8 , 40×16 , 40×32 , 40×64 , 40×128 and 40×256 .

A common centroid layout for the binary ratioed capacitors⁽¹¹⁾ was not adopted since it makes the actual layout of the chip extremely complicated and thus not readily realizable.

3.5 CONCLUSION

The actual circuitry used to realize one tap position of the filter is shown in Fig. 3.37. In total, 16 such taps were included in the chip (8 taps per channel). The computer printout of the filter multi-level mask layout is shown in Fig. 3.38. The chip measures 120 mils x 125 mils and Fig. 3.39 shows its photomicrograph. An n channel silicon gate process was used for its implementation.

FIG 3.38. Chip layout

Fig. 3.39. Photomicrograph of the chip which measures 120 x 125 mils.

CHAPTER 4

INPUT OUTPUT INTERFACE WITH THE PROCESSOR

4.1 INTRODUCTION

This chapter will discuss the methods of introducing the tap weight data into the filter and the processing required, by off-chip circuitry, of the signals appearing at the output of the filter (sense electrodes).

4.2 TAP FEEDIN METHODS

The basic scheme of introducing the tap weight data into the filter has been shown in Fig. 4.1. The tap weight shift registers may be thought of as switches which are close circuited during the on-time of (say) phase clock ϕ_2 (see Fig. 3.5) at both the input and the output of the shift registers. Information may be loaded in from the external world during the ϕ_2 on-time by closing the "LOAD SWITCHES" and open circuiting the "RECIRCULATING SWITCHES". Alternatively, information may be recirculated in the shift register by activating the "RECIRCULATING SWITCHES" and disabling the "LOAD SWITCHES". The information is fed in with reference to the ring counter input. For a N tap filter, there are N bit delays for one period of the ring counter. Each bit delay is assigned as an address for the tap weights. For example, the tap introduced immediately after the ring counter "1" is h_0 (see Fig. 2.7). h_0 may be thought to consist of its content (binary equivalent) and its

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Fig. 4.1. A possible interface for the filter.

address (number of bit delays after the occurrence of the ring counter "1"). The interface therefore has 2 buffer registers which contain the address and the contents of the tap to be introduced into the filter. An output from a counter (from which the ring counter input is developed) is used to compare the address contained in the register and the bit count sequence of the counter. When the two outputs match (filter is in the correct bit position for the tap weight to be introduced), a trigger is developed and the machine is ready to load. On a command "GO" (with the trigger ON), the "LOAD SWITCHES" are activated ("RECIRCULATE SWITCHES" are deactivated) and the tap loading operation is complete. It should be noted that whenever taps are not loaded the RECIRCULATE SWITCHES are activated so that data, once loaded, is retained on-chip.

Three systems of controlling the processor were studied where the taps could be keyed in manually by switches, or automatically using memories or under the control of a microprocessor.

In one system to be called "MANUAL", the Address and Content Buffer Register inputs were connected to physical switches. The GO line was also connected to a physical switch. The address of the tap was first set on the switches; the content of the tap was also set on the other switches; then, the GO signal was given by switching the GO to a high logic level voltage. After this load was completed, the GO line was made to go to a low logic level and a new set of contents and addresses was set up for the next tap to be fed into the filter. The

"MANUAL" system of keying in the taps was found very useful in characterizing the filter.

Another system was developed which uses PROM's (Programmable Read Only Memory). The tap contents were stored in the PROM (8x256). Each 7-bit tap was assigned one 8-bit byte (1 bit being superfluous), and arranged in order of their addresses. The counter used to develop the ring counter input drives the address lines of the memory whose output is then fed into the filter. This enables multiple filter functions/correlation functions stored in memory to be accessed under program control.

Another method where the filter is under the control of a microprocessor interface has been studied. The system architecture is similar to that shown in Fig. 4.1, except now the input lines and the GO switch are under control of the microprocessor data bus.

4.3 OUTPUT SIGNAL SENSING TECHNIQUES

The information processed in the filter has to be recovered from a noisy environment and requires special sensing methods.

A sensing technique, called "VOLTAGE SENSING", was developed which senses the voltage difference between the signal voltage and the reference voltage without sensing the capacitive kicks from the switches gating the voltages onto the sensing surface. These kicks cause decreased signal swing at the output and give rise to fixed pattern noise (and is discussed in Chapter 5).

4.3.1 Voltage Sensing

Fig. 4.2 shows the relevant circuitry needed to explain the sensing mechanism. The signal voltage V_s will be called state 1 and is gated onto the sensing surface by SW going high, while the reference voltage (ground), to be called state 2, is gated onto the sensing surface by $\overline{SW}$ going high. $\overline{SW}$ is the conditional output strobe from the tap weight shift registers and $\overline{SW}$ is logically derived from it using dynamic inverters.

Voltage sensing can be implemented in two ways:

- 1) The reset FET constrains the sensing electrode to a fixed voltage (V_{dd}) while SW turns on and sets the sensing surface to state 1 voltage. The sensing electrode is allowed to float BEFORE SW goes off. Then SW goes low and kicks the sensing surface. However, the effect of this kick is eliminated when $\overline{SW}$ goes high to apply state 2 voltage on the sensing surface. The sensing electrode senses the difference between state 1 and 2 voltage levels and the capacitive kick from SW going off is eliminated by a correlated sampling procedure, since the kick is felt on both sides of the sensing capacitor. This procedure is called "NEGATIVE VOLTAGE SENSING".
- 2) The reset FET constrains the sensing electrode to a fixed voltage (V_{dd}) while $\overline{SW}$ turns high and sets the sensing surface to state 2 voltage. The sensing electrode is allowed to float BEFORE $\overline{SW}$ goes low. Then SW goes high and sets the sensing surface to state 1 voltage and the

Fig. 4.2. Circuitry needed to refer to the sensing scheme.

sensing electrode senses the transition from state 2 to state 1. The effect of the capacitive kick (by $\overline{SW}$ going low) is again eliminated since both plates of the sensing capacitor respond to it and the application of state 1 voltage removes its effect. Only the difference between the state levels are sensed and any noise present in the transition between the state levels do not matter. This procedure is called "POSITIVE VOLTAGE SENSING".

Both these techniques are discussed in specific detail in the succeeding sections.

4.3.2 Positive Voltage Sensing

The transition from ground (state 2) to a positive voltage (state 1 signal level) is a positive voltage increment at the output; therefore, this method is called a Positive Voltage Sensing technique.

The necessary clocks are shown in Fig. 4.3. This method of sensing suffers from the fact that the sensing electrode is a high impedance line when it is floating and picks up capacitive kicks directly from off-chip or on-chip. Good operational amplifiers (in MOS realizations) were not available at the time when the chip was designed and hence the sensing electrode had to be brought off-chip at a high impedance level. Most of the on-chip circuits have logic level transitions during the ϕ_1 and ϕ_2 on-times, the time when the sensing electrode is at a high impedance level. This feedthrough directly onto the sensing electrode (not

Fig. 4.3. Relevant clocks and circuitry required to explain the positive voltage sensing process.

the sensing surface, since that feedthrough is removed by using the voltage sensing method) becomes serious when more chips are cascaded to build larger filters. In general, this noise is not filterable.

In order to isolate the causes of the feedthrough noise, the clocking scheme was altered to that shown in Fig. 4.4. Here, the rising and falling edges of ϕ_1 and ϕ_2 do not have ϕ_R and ϕ_g (ϕ_g is a clock applied to the gate of the MOSFET used to float the sense lines) coinciding with them. Fig. 4.4 also shows an amplifier and a sample and hold circuit which processes the information on the output sense electrode. The amplifier is discussed in more detail in Section 4.4. Fig. 4.5 shows some results obtained with the setup shown in Fig. 4.4. A single tap (in a '96 tap filter) was introduced (all 1's in the 7 tap weight shift registers for that tap position). The analog information was 0 volts. The output voltage should have been flat, but trace 3 in Fig. 4.5 shows the effect of a feedthrough. Fig. 4.6 shows the results on the same experiment as above, but here all the 96 time slots are shown. Fig. 4.7 is the situation for an arbitrary tap input. The feedthrough can be ascribed to the fact that the rising edge of ϕ_1 and ϕ_2 (logic and clocks) feeds through to the floating sense electrode.

Fig. 4.4. Amplifier and sample and hold circuitry which processes the output of the filter, with the clocking scheme shown below it. This clocking scheme was especially designed to study clock noise feedthrough and is not used elsewhere.

Fig. 4. 5. The analog information input is 0V. All 7 tap weight shift registers have a single "1" recirculating in one tap position for a 96 tap filter. The positive and negative sense lines are connected together. Line 1 shows the tap in a shift register (10V/div). Line 2 shows the output of the op. amplifier (.1V/div). Note, as the tap weight voltage goes up, the op. amplifier output goes down (due to phase reversal; see Eqn. 4.1). This is sampled (every alternate sample is sampled, i.e. we are looking at only 1 channel) and the results are shown on Trace 3 (.05V/div). Feedthrough effects are clearly evident (ideally trace 3 should have been flat) in trace 3 which cover only 8 time slots (of the 96 available).

Fig. 4.6. The situation here is identical to that of the last figure except that all 96 time slots are shown here. The 96 tap (per channel) filter was built by cascading 12 chips. It is noted that 12 distinct feedthroughs are evident during the 96 time slots available - 1 for every time the tap weights come off chip and then goes into the next chip.

Fig. 4.7. Feedthrough effect for an arbitrary number of taps. (trace 1) is shown here. Trace 2 is the op. amplifier output and trace 3 is the sampled output. All 96 time slots are covered. Sensitivity is the same as above.

4.3.3 Negative Voltage Sensing

An alternative sensing scheme called "NEGATIVE VOLTAGE SENSING" was developed to solve the feedthrough problem mentioned in the previous section. This method essentially constrains the sensing electrode voltage to a fixed value and allows charge transfer under the sensing electrodes to take place. Charge transfer takes place during the ϕ_1 or ϕ_2 on-times. After this is completed, the sensing electrodes are allowed to float and the reset clock restores the sensing surface to the reference voltage. This allows the sensing electrodes to sense a voltage which is the inverse of the original signal voltage. The clocks required are shown in Fig. 4.8. The circuitry required is that shown in the top part of Fig. 4.8. ϕ_g must remain on long enough during the ϕ_1 on-time to ensure complete charge transfer in the channel.

The "Negative Voltage Sensing" scheme was developed after the "Positive Voltage Sensing" was found to have noise problems. Essentially, in "Negative Voltage Sensing", sensing is possible at a time when no significant feedthrough occurs and hence the better noise performance. For "Negative Voltage Sensing", ϕ_g (as in Fig. 4.8) is required on the gate of the reset FET. However, ϕ_R is still required for operation of other circuitry as shown in Fig. 3.37.

Fig. 4. 8. Clock waveforms needed to implement the negative voltage sensing technique. ϕ_s is the output sampling clock. If the dashed ϕ_s pulse is retained, both channels would be sampled.

Fig. 4.9. Voltage changes on digital lines between chips are shown to change during the rise time of ϕ_1 , ϕ_2 only.

Using the negative voltage sensing techniques, no significant feedthrough was observed. This is attributed to the fact that during the rise times of ϕ_1 and ϕ_2 our sensing system is disabled, and this is precisely the time when most of the feedthrough occurs. This point is further illustrated by looking at Fig. 4.9. The lines that traverse from chip to chip (for cascading) are the tap weight shift register lines, the ring counter lines and the sense lines (the other lines being clock lines or dc voltage lines). Most of the feedthrough (see Figs. 4.6 and 4.7) occurs at the interface between the chips. The only time where the voltage at the interface changes is during the rise time of ϕ_1 or ϕ_2 . Thus, since (in the negative voltage sensing scheme) the signal is not allowed to appear on the output sensing electrode at this time, the feedthrough is eliminated. The wiring requirements (isolating sense lines completely) are not so stringent for this sensing method compared to the positive voltage sensing scheme.

The reset action on the sensing electrode achieved by ϕ_R (positive voltage sensing) or ϕ_g (negative voltage sensing), may alternatively be achieved by connecting V_{dd} to both the gate and drain of the reset FET (Fig. 4.2).

Essentially, during the on-time of ϕ_R , the sensing surface is set to reference voltage (ground). At this time, the sense electrode is sitting at 1 threshold below V_{dd} and is floating. Then ϕ_R goes off and ϕ_1 or ϕ_2 turns on and sets the sensing surface to the signal voltage.

This is detected as a positive increment on the floating sense line voltage. The sense lines return to V_{dd} when the sensing surface is returned to ground. This method would work provided the impedance level of the sensing electrode is lowered before coming off-chip. Use of V_{dd} on the reset transistor gate has the advantage that it eliminates reset noise⁽¹²⁾. However, for this particular design, its use was not successful due to capacitive pickups onto the sensing electrode as is shown in Figs. 4.10 and 4.11.

Fig. 4.10. This figure shows the convolution (trace 3: .2V/div) of 2 rectangles. One rectangle is the tap weight input (trace 2; 10V/div) and the other is the analog input (not shown). Trace 1 shows ϕ_2 (20V/div). V_{dd} is applied to the gate of MOSN1 (see Fig. 4.3). Note the pickup by the sense electrode of the change in voltage of trace 2. This causes changes in the reset level and hence errors in the output. ϕ_R is 100kHz here.

Fig. 4.11. The situation is identical to that in Fig. 4.10 except that ϕ_R is now used instead of V_{dd} on the gate of MOSN1 (the reset FET). Note that the reset level does not change due to pickups on the sensing electrodes. The experiment used 1 chip only and no output amplifiers were used. Relevant clocks are shown in Fig. 4.3.

4.4 CHARGE SENSITIVE AMPLIFIERS

The output information voltage on the sense electrode is small and is especially so when most of the tap weights are small. Hence, it becomes necessary to amplify the signal immediately after it comes out of the chip and before any other processing on it introduces additional noise (and brings down the signal to noise ratio). The amplifier also converts a high impedance input line to a low impedance output line, making it much less susceptible to capacitive noise pickup. In addition, the signal is valid only during the on-time of ϕ_1 (for one channel) and ϕ_2 (for the other channel) and must be sampled out at this time. This section will deal with the circuitry needed to do this.

4.4.1 Non-Differential Configuration

The basic amplifier configuration^(10c) is shown in Fig. 4.12. A high gain operational amplifier with capacitance feedback working in the inverting mode^(10b) is used.

The following discussion gives a qualitative understanding of the operation of the amplifier. It will be followed by a more quantitative analysis.

Let C_{in} be the gate oxide capacitance through which the analog signal appears on the sense electrode and C_L the loading on the electrode to ground. ΔV_s modulates charge on C_1 . The total charge on the inverting node of the operational amplifier cannot change, it merely redistributes itself between the capacitors. Thus, C_{in} draws whatever charge

Fig. 4.12. Basic charge sense amplifier.

Fig. 4.13. Actual configuration required for the filter using "negative sensing".

Fig. 4.14. Configuration used to calculate frequency gain characteristics of amplifier.

ΔV_s requires it to take. An opposite amount of charge appears on C_{FB} (the plate connected to the inverting input of the operational amplifier). The other plate of C_{FB} is charged up by the output of the operational amplifier to equalize the charge on both plates of C_{FB} . Thus,

$$\Delta q = \Delta V_s C_{in}$$

is the charge taken up by C_{in} . This is also the amount of charge needed on C_{FB} . Thus, the voltage across C_{FB} is

$$\Delta V_{FB} = - \frac{\Delta q}{C_{FB}} = - \frac{\Delta V_s C_{in}}{C_{FB}}$$

Therefore,

$$\frac{\Delta V_{FB}}{\Delta V_s} = - \frac{C_{in}}{C_{FB}}$$

Now, the voltage across C_{FB} is also the output voltage since the inverting input node is a virtual ground (10d). Thus, the gain, G , of the amplifier is

$$G = \frac{\Delta V_{out}}{\Delta V_s} = - \frac{C_{in}}{C_{FB}} \quad (4.1)$$

It is necessary to insert a resistor across C_{FB} since the operational amplifier requires a dc path from each input to common for bias current flow. The actual amplifier configuration needed for the filter has

been shown in Fig. 4.13 which uses the negative voltage sensing scheme. The MOS switch shorts out C_{FB} during the on-time of ϕ_g , and thus disables the amplifier and resets (discharges) the capacitor C_{FB} . Then, ϕ_R shorts the semiconductor sensing surface from the analog signal voltage level to ground and this signal appears on the floating sense electrode and is amplified by the charge sensitive amplifier. If we wish to use positive voltage sensing, ϕ_g should be replaced by ϕ_R in Fig. 4.13. Using the amplifier of Fig. 4.13, Fig. 4.15 shows the circuitry required for differential amplification of two signals.

A more quantitative analysis will now be carried out to determine the gain characteristics of the amplifier configuration of Fig. 4.13. Fig. 4.14 shows the amplifier configuration with R_2 representing the off resistance of the MOSFET connected across C_{FB} . R_1 is any resistance in series with C_{in} .

We have, assuming that there is a negligible current flow into the inverting input of the amplifier,

$$\frac{\Delta V_s - V_i}{R_1 + \frac{1}{SC_{in}}} = \frac{V_i - V_{out}}{R_2 / (1 + SC_{FB} R_2)}$$

or

$$\frac{\Delta V_s SC_{in}}{1 + SC_{in} R_1} = V_i \left[\frac{1}{R_1 + 1/SC_{in}} + \frac{1 + SC_{FB} R_2}{R_2} \right] - V_{out} \frac{(1 + SC_{FB} R_2)}{R_2}$$

Now, if the amplifier has a very high gain, $V_i \rightarrow 0$.

Then,

Fig. 4.15. One possible scheme of obtaining differential amplification of two signals from the sense electrodes.

$$G = \frac{V_{out}}{\Delta V_s} = - \frac{R_2}{1+SC_{FB}R_2} \frac{SC_{in}}{1+SC_{in}R_1} = - \frac{SC_{in}R_2}{(1+SC_{FB}R_2)(1+SC_{in}R_1)}$$

$$= \frac{-j \frac{\omega}{\omega_1}}{\left(1+j \frac{\omega}{\omega_2}\right)\left(1+j \frac{\omega}{\omega_3}\right)}$$

where

$$\omega_1 = \frac{1}{C_{in}R_2}$$

$$\omega_2 = \frac{1}{C_{FB}R_2}$$

$$\omega_3 = \frac{1}{C_{in}R_1}$$

Fig. 4.16 shows the transfer function of the filter as derived above.

If $1 \gg SC_{in}R_1$ and $1 \ll SC_{FB}R_2$, then

$$G \approx - \frac{SC_{in}R_2}{SC_{FB}R_2} = - \frac{C_{in}}{C_{FB}}$$

which is the value derived earlier. The amplifier actually behaves like a bandpass filter. The lower cut-off frequency should be taken to as near zero frequency as possible by having $C_{FB}R_2$ as large as possible and $C_{in}R_2$ as large as possible. C_{in} is actually the capacitance of on-chip capacitors and hence cannot be made arbitrarily large. Similarly, C_{FB} controls the gain of the amplifier and also cannot be

Fig. 4.16. Transfer function of amplifier.

made arbitrarily large. Thus, it is imperative that R_2 , the off resistance of a MOSFET, be very large.

Operational amplifiers with FET input stages are preferred because of their high input impedance, low bias current and high bandwidth.

The scheme presented in Fig. 4.15 to recover the output signal from the transversal filter has some disadvantages:

- i) Since the output is derived by subtracting the signals from two electrodes, the actual output is smaller than the signal on the electrodes. Thus, each operational amplifier assigned to the two electrodes has to slew through a much larger voltage (compared to the difference signal), and imposes slew rate constraints on the amplifier.
- ii) Uncorrelated amplifier noise is introduced before the subtraction takes place; this requires the use of low noise operational amplifiers.
- iii) Three operational amplifiers are required to achieve the amplification and subtraction.

The scheme, however, has the advantage that the output voltage is not dependent on the capacitive loading to ground of the sense electrodes.

Some experimental results obtained using the configuration shown in Fig. 4.17 will now be presented.

Fig. 4.17. Amplifier configuration used to obtain experimental data presented in this section.

A sinusoid was fed to an active lowpass filter (with 24dB/octave roll-off in the stop band) to deliver a pure sinusoid to the MOSFET network MOSN2 and MOSN3. The MOSFET network allows the sinusoid to appear at the input when ϕ_g is low and grounds it when ϕ_g is high. This procedure is necessary since the amplifier is capable of amplifying only changes in the signal. R_1 is a small resistance which is used to limit current input to the operational amplifier and is thus a protective feature in the amplifier. MOSN1 is a MOSFET whose off resistance is high (several tens of $M\Omega$). This is essential since, otherwise, a roll-off in the gain frequency characteristics is introduced as shown in Fig. 4.16. Initially, CMOS switches (RCA CD4066) were used for MOSN1. However, their off-resistance was found to be quite low, such that even at 20kHz the amplifier was operating on the 20dB/decade slope of the gain frequency curve of Fig. 4.16. Low leakage MOSFETs (Motorola 3N170, experimental MOSFET's fabricated at BNR) were found to be suitable. However, the off-resistance should not be so high that the amplifier input cannot get its input bias current and as a result go off into saturation. A high resistance (tens of $M\Omega$) R_2 can be introduced across MOSN1 to allow the flow of the necessary bias current (if the off-resistance is very high). The dc voltage V_{dd} connected to the non-inverting input controls the dc level of the output. C_c is a coupling capacitor which eliminates any dc input into the Krohn Hite active filter (whose input is limited to a few volts total of ac and dc voltage).

Fig. 4.18 shows qualitatively some of the results obtained with the amplifier. From the pictures, it becomes evident that although a

Fig. 4.18a. Trace 1 shows the envelope of the sinusoidal input at point A (see Fig. 4.17).

Trace 2 shows the envelope of the output voltage with the input as in trace 1.

Trace 3 shows the output voltage with a grounded input at point A. An overlap kick delivered by ϕ_g through the overlap capacitance of MOSN1 is amplified and seen at the output.

Trace 4 shows ϕ_g .

The sensitivity of the top 3 traces are identical.

$C_{FB} = 120\text{pf}$.

Fig. 4.18b. This is identical to the above except $C_{FB} = 390\text{pf}$. The overlap kick effect at the output is reduced as a result.

Fig. 4.18c. Trace 1 shows the input voltage at point A (see Fig. 4.17). Trace 2 shows the output voltage at point B. Note the offset in the output voltage. Trace 3 shows the clock ϕ_g . $C_{FB}=120\text{pf}$.

Fig. 4.18d. This figure is identical to the above except $C_{FB}=390\text{pf}$. Note that the offset effect has become negligible. Trace 3 is a low pass filtered (with cut-off at Nyquist) version of the output.

faithful amplification is obtained, an offset is present in the output voltage. With no sinusoidal input, the output voltage should not change. However, the overlap capacitance of MOSN1 introduces a signal (ϕ_g going low) on the inverting node of the amplifier. This is then also amplified and appears as an offset voltage on the output. The amplification factor is given by $C_{\text{overlap}}/C_{\text{FB}}$. Tables 4.1 and 4.2 show some results obtained with a breadboarded version of the amplifier without any major shielding to reduce noise. Hence, the results give only an estimate of the performance of the amplifier.

4.4.2 Differential Input Configuration

Another configuration will now be presented⁽¹³⁾ where the subtraction and amplification is achieved using only one operational amplifier. The circuitry is shown in Fig. 4.19.

The operation of the circuit using the negative voltage sensing scheme ϕ_g (same waveform as in positive voltage sensing) resets the sensing electrodes and disables the operational amplifier. Then ϕ_g goes off and the signal from both electrodes are introduced into the two inputs of the amplifier. The high gain of the operational amplifier forces the voltage on the two inputs to equalize by slewing the difference signal through C_{FB} . The discussion below gives a physical feeling of the operation of the amplifier.

Let the switches be open circuited and let C_n be a capacitor on the negative sense electrode. Similarly, C_p is a capacitor on the posi-

TABLE 4.1. Gain-Noise Trade-Off.

C_{in} (pf)	C_{FB} (pf)	Gain, G	rms Noise LPF @ 200kHz (Nyquist) at Point B (mV)	Noise Gain Ratio
390	390	1	1.48	1.48
390	185	2.11	3.18	1.51
390	80	4.87	6.8	1.39
390	39	10	12.4	1.24
390	10	39	24.4	0.64

TABLE 4.2. Linearity-S/N Ratio Trade-Off.

AMP GAIN G	INPUT SIGNAL PT. A V(rms)	INPUT SIGNAL/NOISE RATIO (dB) 200kHz LPF	INPUT SIGNAL SECOND HARMONIC CON- TENT RELATIVE TO FUND (dB)	O/P S/N RATIO AT POINT B 200kHz LPF (dB)	O/P SIGNAL SHC REL. TO FUND. (dB)
1	.225	66	-75	43	-70
1	.500	73	-68	50	-61
1	.795	77	-67	54	-60
2	.400	71	-67	50	-60
2	.600	75	-65	51	-50
2	.800	77	?	54	-44

Fig. 4.19. A charge sense differential amplifier.

tive sense electrode. C_{L_1} is the total capacitive loading to ground as seen by C_n and C_{L_2} is the total capacitive loading to ground as seen by C_p . C_{FB} is an off-chip capacitance connected around the amplifier.

i) Let us consider the situation when $V_n=0$ and V_p has a finite value. The voltage V_+ at the non-inverting input of the operational amplifier is

$$V_+ = \frac{V_p C_p}{C_p + C_{L_2} + C_{FB}}$$

The amplifier forces the voltage at the inverting input of the operational amplifier to this voltage.

The charge on one plate of C_{FB} (the plate connected to C_n and C_{L_1}) must balance the charge on C_n and C_{L_1} . Charge on C_n and C_{L_1} is $(C_n + C_{L_1})V_+$. Hence, the voltage across C_{FB} is $(V_+)(C_n + C_{L_1})/C_{FB}$. Hence, the output voltage V_{out} is

V_{out} = voltage across C_{FB} + voltage on non-inverting input of op. amplifier

$$= \frac{V_+ (C_n + C_{L_1})}{C_{FB}} + V_+ = \frac{V_+ (C_n + C_{L_1} + C_{FB})}{C_{FB}}$$

$$= \frac{V_p C_p (C_n + C_{L_1} + C_{FB})}{C_{FB} (C_p + C_{L_2} + C_{FB})}$$

ii) Now, let $V_p=0$ and V_n be finite.

This case has already been considered (see Eqn. 4.1). V_n modulates charge on C_n and forces V_{out} to charge up C_{FB} . For this case,

$$V_{out} = - \frac{C_n V_n}{C_{FB}}$$

C_{L1} does not affect the analysis since the inverting input of the operational amplifier is a virtual ground.

Now, applying the Superposition Theorem⁽²⁵⁾, the actual output with both V_n and V_p present is

$$V_{out} = \frac{V_p C_p}{C_{FB}} \frac{(C_n + C_{L1} + C_{FB})}{(C_p + C_{L2} + C_{FB})} - \frac{V_n C_n}{C_{FB}}$$

Now, $C_n + C_{L1}$ is the total capacitance (including strays) of the negative sense electrode and $C_p + C_{L2}$ is the total capacitance to ground (including strays) of the positive sense electrode. Hence,

$$V_{out} = \frac{V_p C_p}{C_{FB}} \frac{(C_{nSENSE} + C_{FB})}{(C_{pSENSE} + C_{FB})} - \frac{V_n C_n}{C_{FB}} \quad (4.2)$$

where C_{nSENSE} and C_{pSENSE} are the capacitance to ground of the negative and positive sense electrodes.

Hence, a true differential amplification is obtained provided C_{nSENSE} , C_{pSENSE} have the same value.

The gain frequency characteristics of the amplifier will now be discussed using Fig. 4.20.

$$e_p = \frac{I_2 R_2}{1 + S(C_B + C_{L2})R_2} = \frac{V_p \cdot \frac{R_2}{1 + S(C_B + C_{L2})R_2}}{\frac{1}{SC_p} + R_1 + \frac{R_2}{1 + S(C_B + C_{L2})R_2}} \quad (4.3)$$

Fig. 4.20. Circuit schematic used to calculate gain-frequency behaviour of the amplifier.

$$\frac{V_n - e_n}{R_1 + 1/SC_n} = \frac{e_n - V_{out}}{R_2 / 1 + SC_{FB} R_2} + \frac{e_n}{1/SC_{L_1}}$$

or

$$e_n \left\{ \frac{(1 + SC_{FB} R_2)(R_1 + 1/SC_n)}{R_2} + SC_{L_1}(R_1 + 1/SC_n) + 1 \right\}$$

$$= V_n + \frac{V_{out}}{R_2} (1 + SC_{FB} R_2)(R_1 + 1/SC_n) \quad (4.4)$$

Now, assuming $A \rightarrow \infty$

$$e_p = e_n$$

Using (4.3) in (4.4)

$$\left[\frac{\frac{V_p R_2}{1 + S(C_B + C_{L_2} R_2)}}{1/SC_p + R_1 + R_2 / 1 + S(C_B + C_{L_2} R_2)} \right] \left[\frac{(1 + SC_{FB} R_2)(1 + SC_n R_1)}{R_2 SC_n} + \frac{SC_{L_1}(1 + SR_1 C_n) + 1}{SC_n} \right]$$

$$= V_n + V_{out} \frac{(1 + SC_{FB} R_2)(R_1 + 1/SC_n)}{R_2}$$

or rearranging

$$V_{out} = \frac{V_p C_p}{C_n} \frac{SC_n R_2}{(1 + SC_{FB} R_2)(1 + SC_n R_1)}$$

$$\left[\frac{(1 + SC_{FB} R_2)(1 + SC_n R_1) + SC_{L_1} R_2(1 + SR_1 C_n) + SC_n R_2}{1 + S(C_{FB} + C_{L_2}) R_2 + SC_n R_1 \{1 + S(C_B + C_{L_2} R_2)\} + SC_n R_2} \right]$$

$$- \frac{V_n SC_n R_2}{(1 + SC_{FB} R_2)(1 + SC_n R_1)}$$

$$= \frac{V_p C_p S C_n R_2}{C_n (1 + S C_{FB} R_2) (1 + S C_n R_1)} \left[\frac{1 + S (C_n R_1 + C_{FB} R_2 + C_{L_1} R_2 + C_n R_2) + S^2 (C_{FB} C_n + C_{L_1} C_n) R_1 R_2}{1 + S (C_B R_2 + C_{L_2} R_2 + C_p R_1 + C_p R_2) + S^2 (C_B C_p + C_{L_2} C_p) R_1 R_2} \right] - \frac{V_n S C_n R_2}{(1 + S C_{FB} R_2) (1 + S C_n R_1)} \quad (4.5)$$

Now, R_1 is of the order of $1k\Omega$ and R_2 is $10M\Omega$. Also, $C_n + C_{FB} + C_{L_1} = C_T = C_p + C_B + C_{L_2}$ so that the capacitive loading to ground in each electrode are equal.

Eqn. 4.5 under these conditions reduces to

$$V_{out} = \frac{V_p C_p S C_n R_2}{C_n (1 + S C_{FB} R_2) (1 + S C_n R_1)} \left[\frac{1 + S C_T R_2 + S^2 R_1 R_2 C_n (C_{FB} + C_{L_1})}{1 + S C_T R_2 + S^2 R_1 R_2 C_p (C_B + C_{L_2})} \right] - \frac{V_n S C_n R_2}{(1 + S C_{FB} R_2) (1 + S C_n R_1)} \quad (4.6)$$

where $C_n R_1$ and $C_p R_1$ are neglected in comparison with $C_T R_2$. Again, for $S^2 R_1 R_2 C_n (C_{FB} + C_{L_1})$ to be comparable to $S C_T R_2$, we have

$$S C_T R_2 = S^2 R_1 R_2 C_n (C_{FB} + C_{L_1})$$

$$S = \frac{C_T}{C_n (C_{FB} + C_{L_1}) R_1}$$

Now, C_n is of the order of .1 to 500pf for a 96 tap structure.

C_T is of the order of 600pf for a 96 tap structure.

$(C_{FB} + C_{L_1})$ is of the order of 10-600pf for a 96 tap structure.

Thus, if frequency exceeds tens of megahertz, the term $S^2 R_1 R_2 C_n (C_{FB} + C_{L1})$ becomes comparable to $SC_{T2} R_2$ in Eqn. 4.6.

Since, for our purposes, the bandwidth will not exceed the megahertz region for the transversal filter, the high frequency roll-off caused by $S^2 R_1 R_2 C_n (C_{FB} + C_{L1})$ may be neglected. Similar comments apply to $S^2 R_1 R_2 C_p (C_B + C_{L2})$ in the denominator of 4.6.

Using these approximations, Eqn. 4.6 is rewritten:

$$V_{out} = \frac{V_p C_p}{C_n} \frac{SC_n R_2}{(1 + SC_{FB2} R_2)(1 + SC_{n1} R_1)} - \frac{V_n SC_n R_2}{(1 + SC_{FB2} R_2)(1 + SC_{n1} R_1)}$$

Now, when $SC_{FB2} R_2 \gg 1$, then $SC_{n1} R_1 \ll 1$.

$$\begin{aligned} V_{out} &= \frac{V_p C_p SC_n R_2}{C_n SC_{FB2} R_2} - \frac{V_n SC_n R_2}{SC_{FB2} R_2} \\ &= \frac{V_p C_p}{C_{FB}} - V_n \frac{C_n}{C_{FB}} \end{aligned}$$

and is the true differential amplifier action obtained earlier qualitatively. The transfer function obtained is similar to that derived for the non-differential input charge sense amplifier in Section 4.4.1.

The advantage of this particular configuration is that it does not impose severe restrictions on the amplifier. A relatively slow slew rate operational amplifier may be used as now the amplifier slews through only the difference signal. Also, uncorrelated noise is not

introduced before the subtraction (thus a low noise amplifier may not be needed), and the setup requires only one operational amplifier. Correlated noise on the two electrodes is also cancelled using this configuration.

Table 4.3 presents some experimental data on signal to noise ratio vs linearity obtained on a breadboarded version of the amplifier of Fig. 4.20a. The actual setup used is shown in Fig. 4.20b. The sample and hold unit used is discussed in the next section.

4.5 SAMPLE AND HOLD CIRCUITRY AT THE OUTPUT

The output of the charge sensitive amplifier has to be sampled and held at the appropriate time.

Commercially produced sample and hold modules are available and one such device (Harris HA2425) was tested and found to be unsuitable for this application. The module was a precision sample and hold suitable for low frequency application. The minimum sample time was large (1msec for a sample to hold offset error voltage of 100mV, 10msec for a sample to hold offset error voltage of 1mV, for 0.1% accuracy in the samples).

The sample and hold unit finally adopted is shown in Fig. 4.21. R_1 and C_1 low pass filters the signal with a cut-off frequency at $0.5f_c$, f_c being the clocking frequency. MOSM1 samples the information during the on-time of ϕ_s and stores it on C_s . C_s is a small capacitor (equivalent in size to the overlap capacitance from gate to diffusion of

TABLE 4.3. Linearity vs S/N Ratio for Differential Input Charge Amplifier.

INPUT SIGNAL (mV)	SHC OF INPUT SIGNAL (dB)	SIGNAL O/P (V)	SHC OF O/P SIGNAL (dB)	RMS NOISE AT O/P (mV)	SIGNAL/ NOISE @ O/P (dB)
37	<<-72	.287	-62	.4	57
50	<<-72	.390	-56	.4	59.75
61.5	<<-72	.478	-50	.4	61.5
76.8	-69	.595	-45	.4	63.45
87	-61	.655	-40	.4	64.28

Experimental Conditions: $V_{dd} = 7.25$; $V_{SUB} = -4$; SIGNAL FREQ = 20kHz ; NYQ FREQ = 200kHz .

Fig. 4.20b. Experimental setup used for measurements shown in Table 4.3.

Fig. 4.21a. Sample and hold unit used at the output.

Fig. 4.21b. Sample and hold unit with buffer amplifier and low pass filtering at the output.

MOSN1). $\overline{\phi_s}$ is required to deliver charge to C_s to cancel the charge C_s obtained (when ϕ_s went low) through the overlap capacitance of MOSN1. A bleeder resistance is connected to the source of MOSN2.

The linearity of this circuit has already been treated in Section 3.3.2. For best results, the bias on the input signal should be kept high, and low doped MOSFET's are preferable. Also, the input ac signal swing should be kept small. The clock voltages needed are high since the input information voltage level is high. This requires the use of a substrate bias to prevent field inversion.

Measurements on the linearity and signal to noise ratios obtained on the circuit are shown in Fig. 4.22. The circuit was breadboarded and no special shielding was done to reduce noise pickups.

Fig. 4.22. Linearly and signal to noise ratio measurements for the circuit of Fig. 4.21b.

CHAPTER 5

EXPERIMENTAL RESULTS & DISCUSSION

5.1 INTRODUCTION

In this chapter, some experimental results obtained with the filter chip will be presented.

5.2 CONVOLUTION OF RECTANGLES

The time domain output of the filter is the convolution of the tap weights with the analog signal input.

Figs. 5.1 and 5.2 show the result of such a convolution, obtained with a 96 tap filter. The charge sense amplifier configuration of Fig. 4.8 was used using the negative voltage sensing scheme described in Section 4.3.3. The output of the filter was sampled and held. Only one channel of the filter was used for this experiment.

5.3 FILTER DESIGN EXAMPLES

The frequency response of any filter which is periodic in frequency can be expanded in an infinite Fourier series. For a FIR realization, the Fourier series has to be truncated. This gives rise to overshoots and ripples at discontinuities in the frequency response (Gibbs phenomena). A way around this is to use a finite weighting sequence $h(n)$, called a window to modify the Fourier coefficients to control the convergence of the Fourier series. This windowing technique

Fig. 5.1. Convolution of two rectangles. Top trace shows the ring counter output. The second trace shows the analog information input and the third trace shows the tap weights. The bottom trace is the sense output. ϕ_R is 100kHz.

Fig. 5.2. Same as above except the two rectangles are of similar width.

has been used successfully^(3a) to design FIR filters. There are many types of windows possible, but the Hamming window is one of the most popular ones used. In order to obtain FIR filters with high stop band attenuation, the tap weights of that filter can be weighted with a suitable window (say a Hamming window). Thus, as a first example, a 96 tap Hamming window (which gives a low pass filter action) was designed. The tap weights for the window are given by:

$$h(n) = 0.54 + 0.46 \cos \frac{2\pi n}{N-1}, \quad 0 \leq n \leq N-1 \quad (5.1)$$

Since the output of the transversal filter is sampled and held, an additional sinc function roll-off is introduced on top of the frequency response expected from Eqn. (5.1). The roll-off in the frequency domain is given by (see Figs. 2.4 and 2.5) $\tau \text{sinc } \pi f \tau$ where τ is the hold time. Since a 100% hold is used, $\tau=1$ and the roll-off becomes sincf . Thus, the expected transfer function for the filter becomes:

$$\begin{aligned} H(e^{j\omega}) &= \text{sincf} \sum_{n=0}^{N-1} h(n) e^{-j\omega n} \\ &= \frac{\text{sincf}}{\pi f} \sum_{n=0}^{N-1} h(n) e^{-j\omega n} \end{aligned} \quad (5.2)$$

A computer program was written to compute the above tap weights. This was then digitized to the appropriate number of bits and the bit pattern was programmed in a ROM.

Fig. 5.3 shows the theoretical transfer function for the filter as given by Eqn. (5.2) for quantized and unquantized tap weights and compares it with the experimentally obtained transfer function. The charge sense differential amplifier of Fig. 4.19 was used. The tap weight coefficients were all positive, hence the MSBX2 of the tap weights (see Fig. 2.11) were all zero. Fig. 5.4 compares the theoretical and experimental transfer functions obtained using all 7 bits for the positive tap weight (all tap weights are positive). In this case, a non-differential amplifier negative voltage sensing method was used. Comparing Fig. 5.3 to Fig. 5.4, it is seen that the 6-bit experimental Hamming window performs better than the 7-bit experimental window. This may be ascribed to the fact that for the 6-bit window a differential amplification was used which cancels out correlated noise and transients common to the positive and negative sense electrodes.

Fig. 5.5 compares the theoretical and experimental transfer function for the 6-bit Hamming window, using a differential input charge sense amplifier, with the feedback linearizing circuitry in operation.

Next, a filter was attempted which gives a bandpass action. An intuitive procedure was used to design the filter. If $f(t)$ has a Fourier transform $F(\omega)$, then

$$f(t) \longleftrightarrow F(\omega)$$

and

$$f(t)e^{j\omega_0 t} \longleftrightarrow F(\omega - \omega_0)$$

Fig. 5.3. Experimental results obtained on a 96 tap Hamming window is compared to the theoretically expected results. Differential charge sensing was used.

Fig. 5.4. Results obtained for a 7bit Hamming window (all tap weights positive). A non-differential charge sense amplifier was used.

RELATIVE RESPONSE (dB)

Fig. 5.5. Theoretical and experimental results (using the linearizing feedback mechanism) on a 96 tap Hamming window. Differential charge sensing was used.

Signal spectra can be translated in frequency by suitable multiplication in the time domain. Specifically, a low pass action can be transformed into a bandpass action, as shown below:

$$f(t) \cos \omega_0 t = \frac{1}{2} \left[f(t) e^{j\omega_0 t} + f(t) e^{-j\omega_0 t} \right]$$

and if

$$f(t) \longleftrightarrow F(\omega)$$

then

$$f(t) \cos \omega_0 t \longleftrightarrow \frac{1}{2} \left[F(\omega + \omega_0) + F(\omega - \omega_0) \right]$$

$f(t)$ was chosen as the Hamming window previously described and the cosine function was $\cos \frac{4\pi n}{N-1}$.

Thus, the impulse response of the filter becomes:

$$h(n) = (0.54 - 0.46 \cos \frac{2\pi n}{N-1}) \cos \frac{4\pi n}{N-1}, \quad 0 \leq n \leq N-1$$

This would translate the Hamming window spectra by $\frac{2}{N-1}$ (normalized frequency of $\cos \frac{4\pi n}{N-1}$) and a bandpass action would be obtained with the passband maxima at $2/(N-1)$.

Fig. 5.6 compares the theoretically expected transfer function (with sinc function roll-off due to sample and hold accounted for) using quantized and unquantized tap weights and the experimentally obtained transfer function. A differential input charge sense amplifier was used with the linearizing circuitry being inoperative.

In all the filters presented, the fit is quite good in the pass band but errors are clearly present in the stop band of the filter.

Fig. 5.6. Bandpass spectra obtained by translating a Hamming window. Charge sensing was used.

This is expected as the sensitivity of the filter is inversely proportional to the transfer function as shown below.

$$S_{h_i}^{H(Z)} = \frac{\partial H(Z)}{\partial h_i} \frac{h_i}{H(Z)} = \frac{h_i Z^{-i}}{H(Z)}$$

or

$$\left| S_{h_i}^{H(Z)} \right| = \frac{h_i}{|H(Z)|}$$

Hence, the transfer function is most sensitive to errors in the coefficients where the magnitude of $H(Z)$ is small i.e. in the stop band.

The negative tap weights are more prone to errors since they are obtained by subtracting the largest negative bit from the six smaller positive bits; this is a consequence of the use of two's complement coding to achieve the tap weights. As a result, the Hamming window (see Fig. 5.3) an all positive tap weight filter has a better accuracy than a filter with both positive and negative tap weights (see Fig. 5.6).

Tap weight accuracy and hence transfer function accuracy is also influenced by the rotating nature of the taps. This is discussed in detail in Section 5.6.

5.4 EXPERIMENTAL RESULTS ON LINEARITY

In this section, results obtained using the linearizing scheme of Section 3.3.3 will be presented. The results were obtained using the 96 tap Hamming window low pass filter described in the last section. A single frequency sinusoid was introduced into the pass band of the filter. The second harmonic was measured relative to the fundamental after accounting for the roll-off in the transfer function (ΔH dB is added to the measured second harmonic where ΔH is the change in transfer function between the fundamental and the second harmonic).

Fig. 5.7 shows the second harmonic content of the filter with respect to the fundamental vs the d.c. bias as the input of the operational amplifier, for different sinusoidal amplitude inputs. These results were obtained on a 3.5-4.5 μ m substrate chip. As the d.c. bias is increased, the second harmonic content goes down (see Fig. 3.20) as expected. Fig. 5.8 shows the results without the use of the feedback mechanism. As the input voltage increases, the harmonic content eventually increases due to the fact that the MOSFET (with RING STROBE on its gate) begins to operate in the saturation region. Fig. 5.9 shows the second harmonic content relative to the fundamental vs the a.c. voltage at the operational amplifier input. An important source of non-linearity (using the feedback linearization scheme) is due to the kicks on node N1 (see Figs. 5.19 and 5.20) which is signal dependent - the non-linearity increasing with input signal amplitude as seen in Fig. 5.7.

Fig. 5.7: Non-linearity at filter output using the feedback mechanism.

Fig. 5.8. Non-linearity at filter output without using the feedback linearizing mechanism.

Fig. 5.9. Non-linearity at filter output using the feedback mechanism as a function of dc bias and ac input amplitude.

5.5 GENERATION-RECOMBINATION EFFECTS (LEAKAGE CURRENT)

Loss of signal information due to charge leakage is an important factor affecting the filter characteristics, especially at low clock rate operations.

The analog input signal is sampled and held on a reverse biased p-n junction (node A, Fig. 5.10a). As long as the correct information is available on node A, the correct voltages would appear on the semiconductor sensing surfaces through buffer amplifiers and correct transversal filtering would take place. The information (charge) is stored on node A for nT seconds where n can vary from 0 to N (the total number of taps in the filter) and T is the time period for 1 bit delay of the filter. Depending on T , considerable amount of charge may be lost due to recombination - generation processes inside and on the surface of the semiconductor.

In order to study the time constants of this leakage processes, an experiment was set up as shown in Fig. 5.10(a). A 96 tap filter was set up to convolve rectangles (see Section 5.2). With the time base of the oscilloscope set up for large times (say 100msec/div), the

Fig. 5.10a. Experimental setup implemented to study the leakage characteristics of the device.

envelope of the output becomes visible. Now, if the ring counter pulses are stopped, the input sample and hold nodes are no longer refreshed and the information stored starts leaking away. The output of the filter will reflect this change in input voltage and a decrease in output voltage will be observed. The normal ring counter input is a "1" every 96 time periods. Using logic circuitry, this normal rate is allowed for a certain time and then interrupted for a certain period during which the time rate of decay of the charge can be observed and is shown in Figs. 5.10b and 5.10c. When the capacitor control switch is turned on, some additional oxide capacitance is switched on to node A, as is additional junction capacitance from the capacitor control MOSFET's source diffusion and inversion channel. This changes the time constants somewhat from that with the extra capacitance switched out.

The time constant was experimentally found to be of the order of 100msecs for the chips tested (3.5-4.5 Ω cm doping) and variation of the order of 50% of this figure was observed for different chips.

Assuming a 100 tap filter is available on which 1% distortion (due to leakage) is acceptable, the sample and hold stage servicing the 100th tap weight would have to hold the information for 100·T sec. Further assuming 1% leakage takes place in 1msec, T becomes 10^{-5} secs. Hence, the minimum clocking frequency for the transversal filter would be $1/T=100\text{kHz}$, to keep the leakage distortion at 1% or lower.

Alternatively, if low frequency (below 100kHz for the above filter) operation is desirable, the tap weights of the filter may be

Fig. 5.10b. Envelope of the filter output showing leakage after ring counter input is turned off. Horizontal sensitivity 50msec/div. Capacitor control is off (see Fig. 3.16) for the top waveform and is on the bottom waveform.

Fig. 5.10c. Same as above; top waveform with capacitor control on; bottom waveform with capacitor control off. Horizontal sensitivity .1sec/div.

programmed to compensate for the above leakage. This is possible since tap weight h_k is always serviced by a sample and hold stage which has information on it stored for KT seconds. Thus, h_k may be increased such that the product of the original voltage (sampled) and h_k (original) is equal to the product of the decayed voltage and the new h_k .

(An important effect of leakage is that non-identical leakage characteristics of the different input sample and hold sites can cause fixed pattern noise which will be discussed in Section 5.7.1).

5.6 CONSIDERATIONS FOR DETERMINING TAP LENGTH OF THE FILTER

The structure of the filter is modular and hence, in principle, any number of taps can be implemented. In this section, considerations that determine the optimum length of a filter will be discussed.

In general, accurate implementation of a transfer function requires accurate approximation of the impulse response of the filter. Ideally, this requires the use of a large number of tap weights. For example, a rectangular low pass filter has an impulse response that is a sinc waveform. Thus, to approximate it theoretically, one would require an infinite tap length filter.

Practical considerations limit the actual filter length achievable. These considerations come from:

- i) leakage considerations
- ii) tap weight error considerations
- iii) insertion loss and chip area considerations
- iv) improvement in tap accuracy due to averaging.

i) Leakage Considerations

The analog information is sampled and held at fixed sites on the chip. The analog information which multiplies the k^{th} tap weight is held isolated at a storage node for period KT , where T is the time period of the shift registers propagating the tap weights. Thus, for a N tap filter, the maximum storage time of an analog signal input is NT . Since leakage degrades this signal amplitude (with varying amounts

of leakage for different tap locations), the maximum length of the filter, N , has to be limited such that leakage in time NT is acceptable. Effects of small leakage can be compensated for by predistorting the ideal tap weights.

ii) Tap Weight Error Considerations

Pragmatically, it is desirable to minimize the number of taps as much as possible (without sacrificing the filter performance) since this requires less area on chip.

Ideally, greater stop band attenuation and smaller pass band ripple requires a larger number of tap weights compared to the case where these requirements are not as stiff. Efficient algorithms exist for the design of FIR filters⁽²⁷⁾. Essentially given the filter specifications, the program optimizes the tap weights (for a given tap length) for the best stop band attenuation. If the result is not acceptable and filter specifications are not to be compromised, the length of the filter may be increased to get better performance. The filter length, however, can only be increased to a point beyond which no further gains can be obtained, due to tap weight errors.

In general, the tap weights of frequency selective filters tend to zero at both ends of the filter (for a linear phase design). For minimum phase design, the largest tap weights are located at the beginning and tap weights become smaller and smaller towards the end. For example,

an idealized low pass transversal filter has tap weights given by

$$h_n = \frac{\sin 2\pi n F_p / F_c}{2\pi n F_p / F_c}$$

where

F_p = passband edge

F_c = clock (sampling) frequency

$-\infty < n < \infty$

The smallest tap weight that can be realized is, however, limited by the number of bits used for the tap weight coding. The number of bits that code the tap weights will have to be finite due to chip area constraints. Device process variations such as non-uniform etching, etc. will result in random tap weight error and will put an effective lower limit on the tap weight size.

Tap weight error studies have been done by Puckette et al⁽¹⁹⁾; Fig. 5.11a (reproduced from their work) shows the average stop band attenuation as a function of tap weight tolerance for various filter lengths for a low pass filter. From the figure, it is clear that, for instance, in order to achieve a -70dB stop band attenuation, tap weight tolerance of better than 0.01% is required for a 63 tap filter. With similar tolerance, a 47 tap filter gives -60dB stop band attenuation and a 31 tap filter gives -50dB stop band attenuation. However, if the tolerance is only 1%, only -40dB of attenuation is obtainable, regardless of how long (31, 47, 63 taps) the filter is. It is evident that for a given tap weight tolerance, it is not possible to continuously improve

Fig. 5.11a Average stopband attenuation of a linear phase transversal filter.

the stop band characteristics by simply using more taps. Better stop band attenuation is achievable only by cascading two filters. The optimum filter length is obtained by studying the Monte Carlo simulation of the filter response for different filter lengths (and quantization of the tap weights), for tap weight tolerances representative of the process and layout geometry used to fabricate the device.

iii) Insertion Loss Considerations

As mentioned before, the tap weights of a general frequency selective filter tend to become smaller and smaller towards the end of the filter. By adding more taps, one is merely adding small values at the ends of the filter. Thus, the summed signal charge gets negligibly larger while the total electrode capacity continues to increase, resulting in a net decrease of signal voltage and a loss in signal to noise ratio. This insertion loss impacts the acceptable length of the filter.

iv) Improvement in Tap Weight Errors Due to Effective Averaging

Fig. 5.11(a) showed that in order to obtain stop band attenuation of -40dB a tolerance of better than 1% is required for a linear phase low pass filter. The programmable filter chip as designed had 8 taps/channel and requires cascading of chips to build larger filters. The precision components in each chip, the binary area ratioed capacitors, are defined with relatively good accuracy and tolerance. However, when another chip is cascaded with this, the relative accuracy of the entire array suffers due to variations in oxide thickness from chip to chip and

etching variations across the wafer. These factors can bring the tolerance up to as much as 7% for the silicon gate process used. This brings the expected value of the stop band attenuation achievable to about -23dB (see Fig. 5.11a) regardless of how large the tap length is, if more than 1 chip is used to implement the filter. Fig. 5.11(b) shows the results of a Monte Carlo simulation⁽¹⁹⁾ for a Blackman window.

$$\left[h(n) = 0.42 - 0.5 \cos \left(\frac{2\pi n}{N-1} \right) + 0.08 \cos \left(\frac{4\pi n}{N-1} \right) \right] \quad 0 \leq n \leq N-1$$

The simulation further showed that 4% tolerance yields -45dB, 4% yields -40dB, 1% yields -34dB, 3% yields -25dB and 5% yields -20dB of stop band minimum attenuation for a Blackman window. Fig. 5.11(c) shows the experimentally obtained results. The tap weight accuracy obtained is surprising. The argument presented is certainly valid for fixed tap transversal filters, but may not be extendable for programmable filters where the tap weights are not fixed on chip.

Let the error describing h_k , when h_k is at position m (fixed on chip), be e_k^m . We will assume the error statistics to have zero mean and variance σ^2 . Now, h_k propagates to N different locations on the chip (for a N tap filter). If the output of the filter is introduced into an integrator (averager) which averages over N samples, the resulting error variance associated with h_k over one time frame (NT secs) is (assuming errors are uncorrelated):

$$\begin{aligned} \text{var} \left[\frac{1}{N} \sum_{i=1}^N e_k^i \right] &= \frac{1}{N^2} (N \text{ var } e_k^i) \\ &= \frac{\sigma^2}{N} \end{aligned}$$

Fig. 5.11(b). Results of a Monte Carlo simulation on a Blackman window.

Fig. 5.11(c). Experimentally obtained results on a Blackman window.

Thus, the larger the value of N , the better the tap accuracy (over that expected if the filter had fixed taps on chip). However, this argument hinges on the assumption made that the errors are uncorrelated. In actual fact, some degree of correlation is expected and the actual improvement will be less than the factor of N . Such an averaging effect is expected in the transfer function measurement process due to the slow response time (greater than NT secs) of the high Q bandpass filter in the spectrum analyzer and due to the averaging responding meters in the spectrum or wave analyzer.

5.7 FIXED PATTERN NOISE

The most important mechanism that limits the dynamic range of the transversal filter is fixed pattern noise. The spectra of the filter with only a d.c. bias input consists of energy concentrated at $1/N$ and its multiples (normalized frequency) for an N tap filter. The noise mechanism that gives rise to such a spectra will be called fixed pattern noise (FPN).

Fig. 5.12a shows the transfer function of the bandpass filter discussed earlier (in Section 5.2). The figure is a X-Y plotter output driven from a spectrum analyzer. The lower curve is the spectrum with a d.c. input to the filter (and is the fixed pattern noise) and the upper curve is the transfer function with a sinusoidal input to the filter. The filter was 96 taps long and the FPN was located at multiples of $1/96$ normalized frequency.

The FPN was greatly determined by the programmed filter function as shown by the time domain FPN output for two similar bandpass filters (with different passband frequencies, hence different tap weights) in Fig. 5.12b. These effects will be studied in this section.

Fig. 12a. The transfer function of the filter is shown here with the feedback linearizing circuitry operative. The lower curve is the output of the filter for a dc bias input only and represents the lower dynamic range of the filter.

Fig. 5.12b. FPN is transfer function/tap weight dependent. The FPN in the time domain repeats with the ring counter repetition rate. Trace 1 shows the ring counter output. Trace 2 shows the FPN for a bandpass filter with passband at .02 normalized frequency. Trace 3 shows the FPN for another bandpass filter with passband at .25 normalized frequency. Feedback linearization was not used here. ϕ_1, ϕ_2 were 200kHz and the scales are uncalibrated.

5.7.1 FPN Analysis

Fixed pattern noise can be caused by a number of factors which are listed with reference to Fig. 5.13.

- 1) Gain variation of the source follower buffer amplifiers at the input;
- 2) Variation of overlap kicks from MOSN1 gate onto the input sampling node N1;
- 3) Variation in overlap kicks from MOSN2 gate onto node S1 (when using a non-optimum sensing technique);
- 4) Tap weight errors (not referable to Fig. 5.13);
- 5) Capacitive feedthrough onto the output electrodes; ground loops.

Each of these factors will now be separately discussed.

1) FPN caused by gain variation of individual channels

An N tap filter can be considered to be an N channel "multiplexed" structure with each channel being clocked at f_c/N , where f_c is the overall system clocking rate as shown in Fig. 5.14.

If a d.c. bias is presented to the analog bus, the input to each channel would be a series of impulses (one for every time that channel is sampled). This would appear as a train of impulses in the frequency domain at multiples of f_c/N . Thus, for arbitrary gain G and tap weights $\{h\}$, a fixed pattern would be expected at the output at multiples of $1/N$ ($f_c=1$). Every channel may be characterized for our purposes by

Fig. 5.13. The relevant filter circuitry showing sources of FPN.

Fig. 5.14. A N tap filter can be modelled as an N channel multiplexed device with the channel clocks shown as above. The input signal is sampled and held; then it is multiplied by the gain of the sample and hold buffer amplifiers. The resultant is convolved with the programmed tap weights and the result of all channels are summed up.

$$V_{out_i} = K_i + M_i V_{in}$$

where

$$\frac{V_{out_i}}{V_{in}} = G_i \text{ is the gain of the channel}$$

and K_i is an offset associated with the channel. The following derivation will model the FPN caused by variation of offsets and gains. Use of feedback linearization corrects for gain variations in the source followers, but capacitive kick variations on the input sampling nodes (which can be treated as an effective offset variation) are not corrected by feedback linearization.

Fig. 5.14 shows the block diagram of the filter. The k th channel has gain G_k . The signal in each channel is convolved with the tap weights and the result of all channels are summed up. Both convolution and summation are linear processes and are interchanged in the analysis following and has been shown in Fig. 5.15.

Let T be the time period for one channel of an N tap filter. Let $\omega_0 = 2\pi/T$ for each channel. Also, $\Delta t = T/N(k-1)$, $1 \leq k \leq N$ where k is an integer and Δt is the time delay of the k th channel with respect to the first channel as shown in Fig. 5.14.

Assuming impulse sampling, the signal after the input sampling

$f_{s_1}^*(t)$ for the first channel is

$$f_{s_1}^*(t) = f_{s_1} \delta_T(t)$$

Fig. 5.15. For purposes of analysis, the convolution and summation operations have been interchanged.

where

$$\delta_T(t) = \sum_{n=-\infty}^{\infty} \delta(t-nT)$$

and

$$F[\delta_T(t)] = \omega_0 \sum_{n=-\infty}^{\infty} \delta(\omega - n\omega_0)$$

In general, for the k th channel,

$$f_{sk}^*(t) = f_s(t) \sum_{n=-\infty}^{\infty} \delta(t - (nT + (k-1)/N)T)$$

The Fourier transform of the impulse train in the k th channel is:

$$\omega_0 \sum_{n=-\infty}^{\infty} \delta(\omega - n\omega_0) e^{-j\omega_0 \frac{nT}{N} (k-1)}$$

$$= \omega_0 \sum_{n=-\infty}^{\infty} \delta(\omega - n\omega_0) W_{kn}$$

where

$$W_{kn} = e^{-j\omega_0 \frac{nT}{N} (k-1)} = e^{-j2\pi \frac{n(k-1)}{N}}$$

Now, $F_{sk}^*(\omega)$ is a convolution of $F_s(\omega)$ and $\omega_0 \sum_{n=-\infty}^{\infty} \delta(\omega - n\omega_0) W_{kn}$.

Hence,

$$F_{sk}^*(\omega) = \omega_0 \sum_{n=-\infty}^{\infty} W_{kn} F_s(\omega - n\omega_0)$$

Output of the summing unit is:

$$S(\omega) = \sum_{k=1}^N G_k F_{sk}^*(\omega)$$

$$= \omega_0 \sum_{k=1}^N \sum_{n=-\infty}^{\infty} F_s(\omega - n\omega_0) G_k W_{kn}$$

$$= \omega_0 \sum_{n=-\infty}^{\infty} F_s(\omega - n\omega_0) V_n$$

where

$$V_n = \sum_{k=1}^N G_k W_{kn}$$

= nth Discrete Fourier Transform (DFT) of the gain vectors.

The output of the filter is a convolution (in the time domain) of the tap weights $\{h\}$ with summed signals from the N channels. Thus,

$$O(\omega) = S(\omega)H(\omega),$$

$$\text{where } H(\omega) = F[\{h\}]$$

This is without the sample and hold at the output. The sample and hold will cause a further modification in the form of a sinc function rolloff in frequency.

The normalized response of the system neglecting sinc rolloff is:

$$O(\omega) = \left[\sum_{k=1}^N \sum_{n=-\infty}^{\infty} F_s(\omega - n\omega_0) G_k W_{kn} \right] H(\omega)$$

For a d.c. bias input only $F_s(\omega) = \delta(\omega)$, the height being unity to compute normalized response; hence,

$$S(\omega) = \omega_0 \sum_{n=-\infty}^{\infty} \delta(\omega - n\omega_0) V_n$$

and

$$O(\omega) = \left[\sum_{k=1}^N \sum_{n=-\infty}^{\infty} \delta(\omega - n\omega_0) G_k W_{kn} \right] H(\omega) \quad (5.3)$$

When $n=0$, the d.c. response of the multiplexed system is:

$$O(\omega) = \left[\sum_{k=1}^N G_k \delta(\omega) \right] H(\omega)$$

Thus, the individual channel responses add up and the resultant is multiplied by the transfer function of the filter.

When $n=2$, $1 \leq l \leq N-1$

$$O(\omega) = \left[\sum_{k=1}^N G_k \delta(\omega - l\omega_0) e^{-j\omega_0 \frac{lT}{N} (k-1)} \right] H(\omega)$$

Here, channel gains add vectorially, the channel gain vectors being displaced from each other by equal phase increments as shown in Fig. 5.16.

Thus, if all G_k 's were identical, the resultant output would be zero.

However, if gains of the channel vary, then the resultant output would have components at $l\omega_0$, l being an integer. These components, however, would be filtered by the transfer function of the filter $H(\omega)$.

When $n=N$,

$$\begin{aligned} O(\omega) &= \left[\sum_{k=1}^N G_k \delta(\omega - N\omega_0) e^{-j\omega_0 \frac{NT}{N} (k-1)} \right] H(\omega) \\ &= \sum_{k=1}^N G_k \delta(\omega - N\omega_0) \end{aligned}$$

The channel response again adds up. This can be expressed somewhat differently by saying that aliasing occurs at $n=N$, and the FPN components of interest are $n\omega_0$, $1 \leq n \leq N-1$.

This discussion shows that gain variation of the channels can give rise to FPN, which is filtered by the programmed filter transfer function. Further, non-identical channel characteristics (like leakage variation across the chip) can also cause FPN. This can also be modelled as a gain variation, but this variation is not corrected by the feedback linearization scheme.

Fig. 5.16. The output spectra of the filter (FPN) for a d.c. bias input is the vector summation of equiphase shifted channel gain vectors multiplied by the transfer function of the filter.

For a single frequency input (say a cosine $\cos \omega_s t$), $F_s(\omega) = \delta(\omega - \omega_s)$. Hence

$$O(\omega) = \left[\sum_{k=1}^N G_k (\omega - l\omega_0 \pm \omega_s) e^{-j\omega_0 \frac{lT}{N} (k-1)} \right] H(\omega)$$

where $1 \leq l \leq N-1$.

This will give rise to interaction products between the individual channel frequencies and the signal.

In order to obtain an estimate of the amount of gain variation that may be expected for the on-chip source follower buffer amplifiers, the large signal gain variation was studied to obtain worst case estimates. The large signal gain of the source followers can be determined by using the results of Section 3.3.2. The output voltage of the source follower, V_{out} , is

$$V_{out} = \frac{-B - \sqrt{B^2 - 4AC}}{2A}$$

where

$$A = 1$$

$$B = -2(V_{dc} - V_{TO} + K_1 \sqrt{2\phi_f}) - K_1^2$$

$$C = -K_1^2 (|V_{SUB}| + |2\phi_f|) + (V_{dc} - V_{TO} + K_1 \sqrt{2\phi_f})^2$$

where the symbols are as in Section 3.3.2.

$$\text{Gain } G = V_{out} / V_{dc}$$

The effect of varying the various parameters on the gain are shown in Figs. 5.17(a), (b), (c), (d). The effect of random gain variation on FPN is shown in Figs. 5.18(a), (b). An uniformly distributed random number RN is used to generate gain $G_k = 1 - RN \times TOL$, where TOL is tolerance. Eqn. 5.3 then yields the FPN normalized to the maximum output of the filter (1.1 h.l.).

Fig. 5.17(a). Change in gain as a function of V_{dc} and substrate doping is shown here.

Fig. 5.17(b). Change in gain for various doping and oxide thickness profiles is shown here. The profiles are assumed to vary linearly across the tap location.

$$N = 10^6 \left(1 + \frac{.15}{96} K\right) \quad V_{SUB} = -5.0$$

$$T_{ox} = 10^{-5} \left(1 + \frac{.075}{96} K\right)$$

Fig. 5.17(c). Gain variation as a function of V_{dc} , the doping profile and the oxide thickness. Since the oxide thickness and doping profile vary in the same direction, this is a worst case estimate:-

$$V_{dc} = 5$$

$$\tau_{ox} = 10^{-5} \left(1 + \frac{.075}{96} K \right)$$

$$V_{SUB} = -5$$

Fig. 5.17(d). Gain variation for two different starting substrate doping density is compared here.

Fig. 5.18(a). The maximum value of FPN (before being modified by the transfer function, $H(\omega)$ in Eqn. 5.3) is shown as a function of tolerance, Tol. The variance in the data was ≤ 10 dB. The reference output of the filter (k_{ω_1} , h_k) was taken to be 30.0 for a 96 tap filter, with tap weights being normalized to unity.

Fig. 5.18(b). The expected height of the FPN (before being modified by the transfer function, $H(\omega)$) is shown as a function of tolerance, Tol. The variance in the data was ≤ 27 dB. The reference output of the filter was taken to be 30.0 for a 96 tap filter.

V_{out}

Fig. 5.19. The operating point of the input stage is non-linear (in spite of feedback linearization) due to the varying kicks on node N1. In addition to introducing non-linearity which increases with input signal amplitude (see Fig. 5.20), it also

Fig. 5.20. The signal dependence of the kick on node N1 is shown here.

2) FPN caused by overlap capacitance kicks at node N1

Fixed pattern noise can also be caused by the variation of error voltage injected onto node N1, in the different channels by the capacitive kicks of sampling clocks going off as in 2 of Fig. 5.13. This error is not corrected by the feedback linearization scheme, since that linearization is effective only during the on-time of the sampling clock. The error voltage seen on node N1 can be modelled as an effective offset variation of the channel and the resulting FPN can be treated in a manner described in the last section. Again, for this case, the FPN is filtered by the transfer function of the filter. Fig. 5.19 shows the effect of the kick on node N1. The kick is signal dependent (as shown in Fig. 5.20) and thus a potential source of FPN. The kick ΔV is proportional to the empty channel potential of MOSN1 (hence the signal dependence), i.e.

$$\Delta V \propto \frac{C_{\text{overlap}}}{C_{\text{overlap}} + C_L} (V_{\text{in}} + V_{\text{TO}} + k_1 (\sqrt{V_{\text{in}} + V_{\text{SUB}}} + |2\phi_f| - \sqrt{2\phi_f}))$$

In order to reduce the FPN caused by this effect, provision was made to switch in a large capacitor onto node N1 as shown in Figs. 5.13, 5.19. This capacitor increases signal swing (by reducing the negative kick from MOSN1 gate) and reduces FPN.

3) FPN caused by overlap capacitive kicks onto the sensing surface

It is possible, by improper time control of the resetting of the sense electrode (with clock ϕ_g), to pick up noise (FPN) contributions by overlap kicks from switches adjacent to the sensing surface, i.e. capacitive kicks from the gate of MOSN2 onto node S1 (3 in Fig. 5.13). This component of FPN is present if ϕ_g is on (sense electrode not floating) when SW goes low in negative voltage sensing, and if ϕ_R is high when SW goes low in positive voltage sensing. The error voltage on the sensing surface due to a V volt clock on the gate is

$$\frac{VC_1}{C_1 + C_L} = \frac{V}{1 + \frac{C_L}{C_1}}$$

where C_L is the effective loading on S_1 and C_1 is the effective capacitance between the gate of MOSN2 and S_1 . C_1/C_L was designed to be constant for all bits at all locations. If the error kick is constant across the chip, its effect is a net offset and no fixed pattern is created. However, due to random variation of C_1/C_L and signal dependence of the kick, a variation of the error is expected across the chip, which will create FPN.

At any 1 tap location, the net error voltage is

$$-2^0 \frac{C_1}{C_1 + C_L} (B1 \times V) + 2^{-1} \frac{C_1}{C_1 + C_L} (B2 \times V) + \dots 2^{-6} \frac{C_1}{C_1 + C_L} (B7 \times V)$$

where B1, B2 and B7 are 1's or 0's.

V is the height of the 1's (voltage V on the gate of MOSN2); the error voltage is

$$\frac{C_1}{C_1 + C_L} V \{h_k\}$$

where

$$h_k = -2^0 (B1) + 2^{-1} (B2) + 2^{-2} (B3) + \dots 2^{-6} (B7).$$

$$\text{Let } \frac{C_1}{C_1 + C_L} V = e_1$$

for the 1st storage location

$$= e_k$$

for the kth storage location.

If we assume C_1/C_L is constant at any 1 location but varies from location to location, and further assume that the analog signal is also held constant across all locations, then the output voltage due to a V_{DC} bias input becomes at time n ,

$$V_{out}(m) = (V_{DC} + e_1 h_1) h_1 + (V_{DC} + e_2 h_2) h_2 + \dots (V_{DC} + e_k h_k) h_k$$

and, in general,

$$V_{out}(t) = \{V_{DC}\} * \{h_k\} + \{e_k\} * \{h_k^2\}$$

or

$$V_{out}(\omega) = F[\{V_{DC}\}] H(\omega) + E(\omega) H'(\omega)$$

where

$$H(\omega) = F\{h_k\}$$

$$E(\omega) = F\{e_k\}$$

$$H'(\omega) = F\{h_k^2\}$$

i.e. the output voltage caused by the error kicks, $\{e_k\}$, is a convolution in time domain with the set $\{h_k^2\}$. The FPN caused by this effect is not filtered by the filter function, but by a modified filter function, whose stop band attenuation may not be as small as that of the programmed filter function. The use of a proper voltage sensing technique eliminates this component of FPN and improvements of up to

10dB in the FPN are measured (as will be shown later) for typical filters.

4) FPN caused by tap weight errors

In the time domain, the periodic repetition of the output (with d.c. input only) with frequency f_c/N (period T), f_c being the clocking rate of the filter, gives rise to FPN.

Let us consider a N tap filter with a single tap weight h_1 rotating in it, all other taps being 0. We will assume that a constant bias voltage is available at all sites and no overlap error kicks occur. Now, when h_1 is in position 1, it has tap weight error e_1 associated with it, and the time domain output reflects this. When h_1 goes to position k after time T/N , this error becomes e_k . Thus, over the time frame T , h_1 has covered all locations and the time domain output would show an error waveform representative of the tap weight errors in h_1 as it traverses all the chip locations. The waveform would be periodic and would give rise to FPN.

If we make the assumption that e_1 at the i^{th} location is constant for all time but different from e_j , then $V_{\text{out}}(n) = \sum_{i=1}^N \{V_{\text{DC}} + e(i)\} h(n-i)$

and $V_{\text{out}}(\omega) = E(\omega)H(\omega)$; $E(\omega) = F\{e_i\}$; $H(\omega) = F\{h_i\}$

The FPN is thus filtered by the programmed filter function.

5) FPN caused by capacitive feedthrough and ground loops

The sense electrodes are high impedance lines when they come off-chip in the chip as designed here. Hence, they are susceptible to capacitive feedthrough from the ring counter and tap weight shift register. This feedthrough can be minimized by using the negative voltage sensing scheme. However, this feedthrough, if it exists, will cause FPN since the spectra of the ring counters, tap weight registers have

energies at $\frac{f_c}{N}$ and its multiples. In addition, on-chip feedthroughs to the sensing electrode from the changing edges of clocks also cause FPN.

Another factor that could cause FPN is transient current rushes through a ground line shared by the digital shift registers/ring counters/off-chip T²L circuitry and the analog information processing section of the filter. Ground loops are eliminated by using independent ground lines going to a common grounded plane. All d.c. power supplies should also be decoupled with large capacitors to suppress any FPN in them.

5.7.2 Experimental Observations

In this section, experimental results will be presented which correlate the theoretical predictions made in the last section.

1) Effects of gain variation in the input buffer amplifiers

Fig. 5.21 shows the time domain output of the filter (transfer function shown in Fig. 5.6), with and without the use of the feedback linearizing circuitry. It is noted that most of the large variations in the time domain output are eliminated using the feedback linearizing circuitry, which corrects for the gain variation of the different stages. The resulting FPN spectra for the two cases discussed here are shown in Fig. 5.22a. The use of the linearizing circuitry suppresses the FPN components in the passband of the filter. Also, it is noted that the FPN components in the passband are larger than in the stop band,

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Fig. 5.21. The figure shows the time domain FPN output with and without the use of the feedback linearizing circuitry. The top trace shows the ring counter pulses. The middle trace shows the FPN output of the filter without the use of the linearizing circuitry (.1V/div.). The lower trace shows the output using the input linearizing circuitry (.1V/div.). It should be noted that variations in the output have been reduced using the feedback linearizing circuitry, which also corrects for gain variation of the buffers.

Fig. 5.22a. Transfer function and fixed pattern noise of a filter with and without the use of the feedback linearizing circuitry using the negative voltage sensing scheme.

which is in conformity with predictions that FPN caused by gain variation is filtered by the transfer function of the filter. Interaction products described previously are shown in Fig. 5.22b. Here, a single frequency sinusoid (with a d.c. bias) was used to determine the interaction products, which occur at frequencies corresponding to $(n\omega_0 \pm \omega_s)$. This has been compared with the transfer function of the filter. Feedback linearization was used here.

2) Effects of overlap kicks on FPN (from MOSN1 of Fig. 5:13)

FPN caused by kicks delivered through MOSN1 onto node N1 was studied and results are shown in Figs. 5.23 and 5.24. In Fig. 5.23, it appears apparently that when the capacitor is switched in onto N1, the FPN increases since the relative size of the output increases compared with that for the case where the capacitor is not switched in. However, quite the opposite should be true, since the amount of capacitive kick through the "overlap" capacitance will decrease with the capacitor switched in.

This apparent increase in FPN will now be explained. When the capacitor is switched in, the input signal (i.e. d.c. bias) increases since the capacitive kick reduces the signal on node N1. This increased bias level multiplies the vector summation of the gains (that cause FPN as described previously) and hence FPN increases. However, switching on the capacitor also increases the desired signal swing (by about 3dB) and the FPN relative to the increased passband is reduced by up to 4dB if

Fig. 5.22b. The transfer function of the filter is compared to the interaction product, between the signal frequency and the individual channel clock frequencies. A single frequency sinusoidal on a dc bias is used to obtain the lower curve (in red). Feedback linearization is used here.

RED: Interaction products (due to single frequency input on a dc bias)

BLUE: Transfer function of filter FPN (due to a dc bias only)

Fig. 5.23. The time domain FPN is shown here with and without the use of the extra capacitance that is switchable onto node N1. No linearizing feedback is used. The first trace is the ring counter pulse; the next trace is the output without the capacitor switched in and the bottom trace is with the capacitor switched in. Sensitivity of bottom traces is .1V/div.

Fig. 5.24. The time domain FPN is shown here with and without the use of the extra switchable capacitance onto node N1. Linearizing feedback is used here. The top trace is the ring counter; the middle trace is the output FPN without the capacitor; the lower trace is with the capacitor. Sensitivity of bottom traces is .1V/div.

the bias levels are adjusted (to compensate for the increased bias level caused by the capacitor being switched in).

The above hypothesis was tested and results are shown in Fig. 5.25. The capacitor was not switched in for this experiment. In one case, no feedback linearization was used for two input d.c. bias levels. It is observed that the FPN is larger for the larger d.c. bias. The same thing was also done for the case where input feedback linearization was used.

3) FPN due to overlap kick from MOSN2 (see Fig. 5.13)

Fig. 5.26 compares the FPN spectrum obtained using the negative voltage sensing and that using a modified scheme (where the sense electrode is not allowed to float before SW goes low, See Section 4.3).

Significant reductions in FPN result in the use of the proper negative voltage sensing schemes, specially in the FPN component corresponding to the periodicity of the chips (12/96 normalized frequency for a 12 chip realization of a 96 tap filter). This is consistent with the argument that FPN is caused by variation of the kick across the filter, and the kicks are expected to be relatively constant across one chip, but would vary from chip to chip. Further, the FPN is not filtered by the programmed filter function as predicted previously.

Fig. 5.25. Top trace shows the ring counter pulse. The next two traces are for V_{DC} (input dc bias) of 4 and 5 volts respectively (using feedback linearization). The next 2 traces are for V_{DC} of 4 and 5 volts respectively (without the use of feedback linearization). Sensitivity is .1V/div for the bottom four traces. Clearly increasing V_{DC} causes increased FPN. In all the four cases, the capacitor on node N1 (see Fig. A) was not switched in..

Fig. 5.26. By improper clock time control, it is possible to pick up FPN components caused by kicks from switches adjacent to the sensing surface. Significant increases in FPN result from such kicks as is seen here.

4) FPN due to tap weight errors

An experiment was set up to isolate the noise from the input stage by disabling the ring counters. The signal input in this case becomes the reference voltage (ground). Trace 1 of Fig. 5.27 shows the FPN (over one period of the ring counter repetition rate) for this case. The ring counter was then enabled (without using feedback linearization) and trace 2 shows the resulting FPN. Trace 3 shows the FPN with the ring counter enabled and the feedback linearization operative.

FPN in Trace 1 is attributed to capacitive feedthrough and ground loops. FPN in Trace 3 is attributed to tap weight errors and overlap kicks from MOSN1 in addition to those causes of FPN mentioned in Trace 1. Since the capacitor control was operative, it is believed that the increase in FPN in Trace 3 over that in Trace 1 is mostly due to tap weight errors.

5) FPN due to feedthrough onto sensing electrode and ground loops

An experiment was set up such that the tap weight inputs were all 1's for the largest capacitor bank and were all 0's for the smaller capacitor banks. This is a rectangular window in the time domain and is a sinc window in the frequency domain with nodes at multiples of $1/N$. Thus, this filter suppresses the effect of FPN from the input stage of the device. Further, since all the tap inputs are identical, the effects of FPN caused by tap weight errors are minimized and factor 5 is the only significant source of FPN left in the device.

Fig. 5.27. Trace 1 shows the FPN with the ring counter off (i.e. FPN caused by capacitive feedthrough and ground loops). Trace 3 shows the FPN with ring on and the feedback linearizing on (i.e. FPN caused by tap weight errors and overlap capacitive kicks in addition to those in trace 1). Trace 2 shows the FPN as in trace 3 but with feedback linearization off (FPN caused by gain variation in addition to reason present in trace 3). Increase in FPN in trace 3 over that in trace 1 is attributed mostly to tap weight errors. Increase in FPN in trace 2 over that in trace 3 is attributed to gain variation of the source followers.

Fig. 5.28 shows the FPN obtained from the experimental setup. Next, the tap inputs into the largest capacitor bank were made 0, but the input into all other banks was made 1. The resultant filter is similar to the one just discussed; however, larger feedthrough noise is expected for this case due to the larger number of capacitor banks involved. The experiment showed an increase in FPN by about 6dB over that obtained in Fig. 5.28.

5.7.3 Inference from Experimental Data

The FPN caused by gain variation in the input stage is filtered by the transfer function. This is clear from Fig. 5.22a, where the use of feedback linearization reduces FPN only in the passband but does not affect the stop band at all (since even without the use of the feedback linearization, the FPN caused by gain variation is filtered by the stop band of the filter). FPN caused by component 3 in Section 5.7.1 is completely eliminated by use of a proper voltage sensing technique as shown in Fig. 5.26. The remaining sources of FPN are therefore as in factors 2, 4 and 5. The evidence shown in Fig. 5.27 strongly suggests that factors 4 and 5 are the major remaining sources of FPN in the device. Fig. 5.28 shows the effect of factor 5 on FPN separately.

At present, a 45dB dynamic range has been achieved with less than 1% harmonic distortion at the output for 3.5-4.5 Ω -cm substrate material.

Fig. 5.28. FPN for a rectangular window (all 1's in the time domain). Only capacitive feedthrough and ground loops are the important sources of FPN for this case.

5.7.4 Reduction in FPN Using Dual Channels

The programmable filter was designed to have two interleaved separate filters programmed with one operating during ϕ_1 , the other during ϕ_2 . This two-way multiplexing is specific to this particular case and is additional to the N-way multiplexing discussed earlier which is general for this type of structure. The FPN was monitored in each filter and some degree of correlation was observed in the time domain FPN. The FPN waveforms from the two filters were introduced into the two inputs of a differential amplifier and the results are shown in Fig. 5.29. It should be noted that complete cancellation of the FPN (even with complete correlation of waveforms in the filters) is not possible since there is a phase delay between the two filters. This phase delay is small for the smaller harmonics and becomes significant for the higher harmonics.

Methods to Reduce FPN

From the previous discussion, it is apparent that several things could be done to reduce the FPN effects in programmable filters of this kind. These are listed below:

- 1) Use of low doped (high resistivity) substrate so that gain variation of the source followers is small. Also, this permits a larger signal swing (for a given linearity) and hence results in a larger dynamic range.
- 2) Use of feedback linearization to correct for gain variation of the source followers.

Fig. 5.29. Reduction of FPN by introduction of identical bias levels in each filter and their subtraction in a differential amplifier. No feedback linearization was used in the experiment.

- 3) Use of a large capacitor on node N1 (Fig. 5.13). This will increase signal swing and decrease FPN.
- 4). Use of a proper sensing scheme to eliminate effects of overlap capacitive kicks from switches.
- 5) Conversion of the impedance level of the sensing electrode before coming off-chip. This would reduce FPN caused by feed-through onto the sensing electrode.
- 5) Use of larger capacitors as tap weights to reduce FPN in the filter by reducing tap weight errors.
- 7) Use of a differential sensing scheme to reduce clock transients and common node noise (see Fig. 5.9) in the two sensing electrodes.
- 8) Use of a dummy channel could be made. Both channels carry identical bias voltages but complementary signals as discussed previously.

5.8 FILTER CASCADING

The magnitude of the stop band attainable in a filter is limited by quantization errors in the tap weight coefficients and by errors associated with the tap weights themselves. A practical method of obtaining high stop band attenuation is by cascading filters.

The filter chip was designed to have two interleaved filters programmed with the identical transfer function. One filter works during ϕ_1 and the other during ϕ_2 . The analog bus is common to both

filters. The input analog signal is introduced to the analog bus during ϕ_1 for one filter (filter A) and its output is introduced onto the analog bus during ϕ_2 (for filter B) as shown in Fig. 5.30. The transfer function obtained is shown in Fig. 5.31. However, for this technique to be meaningful, the fixed pattern noise would have to be reduced below the stop band attenuation level.

5.9 CONCLUSIONS

The implementation of a real time programmable transversal filter with analog tap weight capability and with acceptable performance has been shown to be feasible in MOS/LSI technology. This opens the door to applications in adaptive filtering for equalization, spectral analysis, in applications requiring cross-correlation of arbitrary signals and in matched filtering. It is believed that this approach will be superior in performance and cost over all digital processor implementations. Work is being done at Bell-Northern Research, Ottawa, Ontario on this filter (which has been interfaced to a microprocessor) to explore these possibilities.

The following are the principal contributions of this work:

- 1) The design of a programmable transversal filter, which is voltage controlled (as opposed to charge controlled) has been successfully demonstrated with all its attendant benefits.
- 2) Analog tap weights have been successfully implemented using binary coded capacitor banks.

Fig. 5.30. Circuitry needed to cascade two on chip multiplexed filters.

Fig. 5.31. Transfer function obtained by cascading two filters with identical tap weight inputs.

- 3) A single level Si-gate N-channel MOS/LSI process has been shown to be sufficient to implement the filter. The principle of modularity (i.e. increasing the filter size by cascading more chips) has been demonstrated to yield acceptable results (in spite of variations of parameters from chip to chip) without the need to adjust parameters in each chip separately.*
- 4) A novel circuit technique to linearize and correct the gain variation of the input source follower buffer amplifiers has been successfully demonstrated. This circuit was inspired by the use of operational amplifiers to correct for non-linearity in the input stage of a CCD.
- 5) Optimum sensing schemes were developed capable of sensing the true difference of voltage levels on the sensing surface without sensing the errors caused by capacitive kicks from switches gating in the voltage levels. Such kicks reduce the desired signal swing and increase FPN significantly. In addition, a differential sensing scheme was shown to be necessary (to eliminate correlated noise on the sensing electrodes) to yield a larger dynamic range.

* A recent attempt to build a filter with 4-bit tap weights (1 chip for each bit) using the charge sloshing correlator⁽¹⁾ showed that every chip required separate adjustment of the substrate bias and gain of the chip⁽²⁸⁾.

- 6) FPN is the primary limitation of these programmable filters. A major effort was made to isolate the causes and establish means of reducing the FPN. Experimental results have been shown to corroborate the model suggested.
- 7) It was shown that the rotation of the tap weights yield increased tap weight accuracy.

It is believed that further improvement in device performance will be obtained by doing the following:

- 1) The accuracy of the negative tap weights suffer from the use of 2's complement coding, since they are obtained by subtraction of a large capacitor from a bank of smaller capacitors. Instead, use of a sign bit with switches which allow the sensing of the signal or its complement is feasible and will result in better tap weight accuracy. However, to retain a differential sensing scheme, another channel is required.
- 2) The impedance of the sense electrodes should be lowered before coming off-chip.
- 3) The capacitor used in the input sampling stage should be increased, the size of the tap weight capacitor should also be increased.
- 4) The filter should be designed to reduce feedthrough by proper layout and timing control in the design.
- 5) Analog and digital grounds and supply voltages should be separate.

- 6) Low doping substrate material should be used.
- 7) Inclusion of operational amplifiers on-chip required for the signal recovery is highly desirable.

LIST OF REFERENCES

1. "A Surface Charge Correlator", Tiemann, J.J., Engeler, W.E., Baertsch, R.D., IEEE Journal of Solid State Circuits, Vol. SC-9, pp. 403-410, Dec. 1974.
2. "Theory and Application of Digital Signal Processing", Rabiner, L.R., Gold, B., Prentice Hall Inc., 1975, pp. 47.
3. "Digital Signal Processing", Oppenheim, A.V., Schafer, R.W., Prentice Hall, Inc., 1975, pp. 554.
- 3a. Ibid, pp. 239.
4. Berglund, C.N., Thornber, K.K., "Incomplete Transfer in Charge Transfer Devices", IEEE Journal of Solid State Circuits, Vol. SC-8, No. 2, April 1973, pp. 108-116.
5. Peatman, J.B., "The Design of Digital Systems", McGraw-Hill Book Company.
6. Haque, Y.A., "An investigation of MOS bootstrapped logic circuits", M.Eng. Thesis, Carleton University, Ottawa, Ont. Canada, 1974.
- 6a. Ibid, pp. 35.
- 6b. Ibid, pp. 53.
- 6c. Ibid, pp. 15.
- 6d. Ibid, pp. 30.
7. Joynson, R.E, Mundy, J.L., Burgess, I.F. and Neugebauer, C., "Eliminating Threshold Losses in MOS Circuits by Boot Strapping Using Varactor Coupling", IEEE Journal of Solid State Circuits, Vol. SC-7, No. 3, June 1972, pp. 217-224.
8. The Engineering Staff of American Micro-Systems Inc., "MOS Integrated Circuits", Van Nostrand Reinhold Co., New York, 1972.
- 8a. Ibid, pp. 186-239.
9. MacLennan, D.J., Mavor, J., "Linearization of the Charge Coupled Device Transfer Function", 1975 CCD Applications Conference, San Diego, pp. 291-294.

- 10a. Application and Engineering Staff of Burr-Brown Research Corp., "Operational Amplifiers", McGraw Hill Book Co., pp. 430.
- 10b. Ibid, pp. 428.
- 10c. Ibid, pp. 234.
- 10d. Ibid, pp. 429.
11. Albarran, J.F., Hodges, D.A., "A Charge Transfer Multiplying Digital to Analog Converter", 1976 IEEE International Solid State Circuits Conference, Feb. 1976, pp. 202.
12. Carnes, J.E., Kosonocky, W.F., "Noise Sources in Charge Coupled Devices", RCA Rev., Vol. 33, pp. 327-343, 1972.
13. Baertsch, R.D., Engeler, W.E., Goldberg, H.S., Puckette, C.M., Tiemann, J.J., "The Design and Operation of Practical Charge Transfer Transversal Filters", IEEE Journal of Solid State Circuits, Vol. SC-11, No. 1, Feb. 1976, pp. 65-73.
14. Foxhall, T.G., "CCD Transversal Filters", Master of Applied Science Thesis, University of Ottawa, Ottawa, Canada, 1975, pp. 43.
15. Sangster, F.L.J., "The Bucket Brigade Delay Line, A Shift Register for Analogue Signals", Philips Tech. Review, 31, 1970, pp. 97-110.
16. Collins, D.R., Bailey, W.H., Gosney, W.M., Buss, D.D., "Charge Coupled Device Analogue Matched Filters", Electronics Letters 8, 29 June 1972, pp. 328-329.
17. Buss, D.D., Collins, D.R., Bailey, W.H., Reeves, C.R., "Transversal Filtering Using Charge Transfer Devices", IEEE Journal of Solid State Circuits, SC-8, No. 2, 1973, pp. 138-146.
18. Whitehouse, H.J., "Signal Processing with Charge Transfer Devices", IEEE Journal of Solid State Circuits, Vol. SC-11, No. 1, Feb. 1976, pp. 64-65.
19. Puckette, C.M., Butler, W.J., Smith, D.A., "Bucket Brigade Transversal Filters", IEEE Trans. on Communications, COM-22, No. 7, July 1974, pp. 926-934.
20. Buss, D.D., Bailey, W.H., Tasch, A.F., "Signal Processing Applications of Charge Coupled Devices", CCD 74 Int. Conf. Edinburgh, Proc., pp. 179-197.

21. Buss, D.D., Bailey, W.H., Holmes, J.D., Hite, L.R., "Charge Transfer Devices: A New Semiconductor Technology Applied to Communication Systems", submitted to IEEE Transactions on Communications.
22. White, M.H., Lampe, D.R., Fagan, J.L., "CCD and MNOS Devices for Programmable Analog Signal Processing and Digital Non-Volatile Memory", EDM, Washington, D.C., Tech. Digest, 1973, pp. 130-133.
23. Haque, Y.A., Copeland, M.A., "An Electrically Programmable Transversal Filter", IEEE, IEDM, Dec. 1976, pp. 27-30.
24. Sze, S.M., "Physics of Semiconductor Devices", John Wiley and Sons, 1969, pp. 517.
25. Cheng, D.K., "Analysis of Linear Systems", Addison Wesley Publishing Company, Inc., 1966, pp. 6.
26. Carlson, A.B., "Communication Systems", McGraw Hill Book Co., 2nd Edition, pp. 73.
27. McClellan, J.H., Parks, T.W., Rabiner, L.R., "A Computer Program for Designing Optimum FIR Linear Phase Digital Filters", IEEE Transactions on Audio and Electroacoustics, Vol. AU-21, No. 6, Dec. 1973, pp. 506-526.
28. Evans, N.E., Gamble, H.S., "Intracell CCD Programmable Correlator", Electronics Letters, 3 Feb 1977, Vol. 13, No. 3, pp. 69-71.

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