Fine Resolution 20 GHz DCO

by

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Abstract

In this thesis a digitally controlled oscillator at 20 GHz is designed to have very fine tuning resolution. This high resolution enables the oscillator to change its frequency by a tiny fraction and in doing so improves the noise performance of a PLL, hence improving radio link quality. Following an introduction to the topic, and background study three designs were investigated to achieve fine resolution. The first design involves using the smallest kit varactor in the 130 μm CMOS technology in use available from IBM. This design achieves a measured resolution of about 30 MHz. Secondly a design involving the use of a small fixed capacitor in series with a larger varactor is used. In schematic simulation, this device achieved a resolution of 5 kHz. However due to the large size of the resonator covering digital tuning from 5 kHz to 2 GHz, the amount of interconnect greatly reduced the quality factor of the resonator and so the extracted view did not oscillate. Finally, in the third design, the same concept of the second design was used but this time only fine tuning was done digitally. This greatly reduced the size of the resonator and so the extracted view worked achieving a resolution of about 120 kHz at 20 GHz. After detailed simulation it became clear that the open loop gain in the oscillator was not sufficiently high enough and so any processing variations could lead to a further reduction of gain which would result in oscillations not starting up. For future designs, it is recommended that at such high frequencies, all passives in a circuit pass EM simulations before fabrication to obtain a better estimate of the expected on chip performance. Moreover, designs should pass slow corner simulations in order to make sure there is plenty of open loop gain, and in case there is not, measures should be taken to increase it.

Acknowledgement

Firstly, I would like to thank Dr. Calvin Plett for his non relenting support and patience with my research. He has been my guide and mentor in technical and motivational aspects throughout my thesis work.

I would also like to thank the many graduate students that helped me out of their own personal time through the many stages of my design and testing. Special thanks to Yasser Soliman, Jerry Lam, Kimia Ansari, William Knisely and Nathan Jess. Special acknowledgement also goes to Nagui Mikhail and the rest of the Department of Electronics at Carleton University for their continuous support.

Finally, I would like to thank my family for being there for me and providing me with their continuous support through the many hours of work I spent on this research.

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List of Acronyms

ADPLL	- All Digital Phase Locked Loop
CMOS	- Complementary Metal Oxide Semiconductor
DCO	- Digitally Controlled Oscillator
EM	- Electro-magnetic
FCW	- Frequency Control Word
MIMCAP	- Metal Insulator Metal Capacitor
MOSFET	- Metal Oxide Semiconductor Field Effect Transistor
NMOS	- n-channel MOSFET
PCB	- Printed Circuit Board
PLL	- Phase Locked Loop
PMOS	- p-channel Metal Oxide Semiconductor
Q	- Quality Factor
TDC	- Time to Digital Converter
RF	- Radio Frequency
VCO	- Voltage Controlled Oscillator

Chapter 1: Introduction

1.1 Wireless Communication and Radios

With the advance of electronics, wireless systems have become increasingly in high demand. This has triggered research into the many ways to improve such wireless systems. From having higher power efficiency, to being less susceptible to noise while maintaining wireless range, wireless research has become a major topic in analog and RF sub-genres of electrical engineering.

Wireless communication has many advantages. The absence of wires to carry signals means that data can be transferred for long distances without the use of expensive cables. In order to transmit or receive data wirelessly, devices use radios. Radios are complex components composed of several stages that prepare a signal either to be sent wirelessly or be processed and demodulated to translate it into a bit stream at baseband, corresponding to the data initially sent. The main stages of a radio include frequency generation to generate a carrier signal, filtering to remove unwanted out of band signals, amplification to boost signal level and mixing to either change the carrier frequency to RF band in a transmitter or an RF carrier to base band in a receiver.

This thesis focuses on an important aspect in the frequency generation stage of a radio. There are some certain criteria that this stage has to meet. For example the required RF signal needs to be of a certain minimum power, minimum noise level and stable enough to not drift with variations in temperature.

1.2 All Digital Phase Locked Phase Locked Loops (ADPLL)

Frequency is generated (synthesized) in most modern high performance wireless system by means of a phase locked loop [1]. A phase locked loop guarantees the quality and stability of the local oscillator signal needed for modulation or demodulation. Using a feedback loop, phase locked loops ensure that the frequency and phase do not drift due to temperature or noise affecting the circuit. The output of the system is fed into a comparator which compares the input phase with the loop phase generating an error signal, V_e. The error signal is then converted into a voltage to control the frequency of the oscillator. This is shown in Figure 1.1.

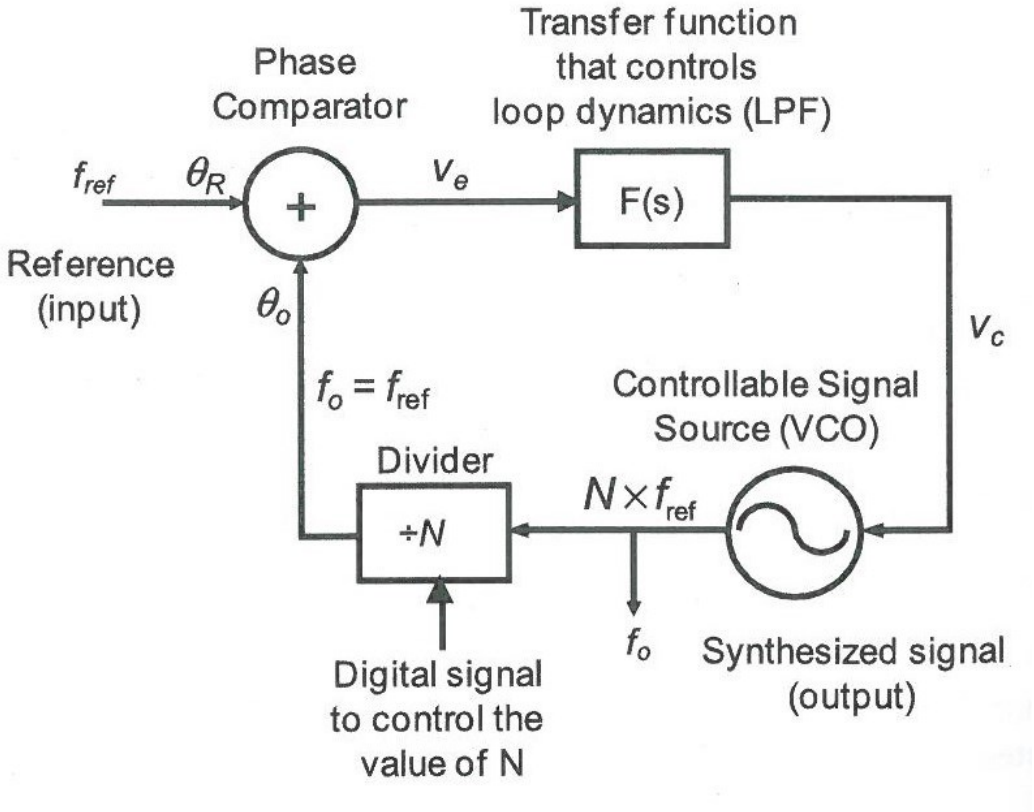


Figure 1.1: Phase Locked Loop [2]

However, there are challenges in implementing synthesizers in sub-micron CMOS, and often components like resistors and capacitors for the loop filter are implemented off chip thus making it difficult to integrate the PLL [2].

In recent times, analog PLLs have been frequently replaced by all digital PLLs in order to avoid the problems mentioned above. However, in many cases, components in a digital PLL are not simple translations of their analog counterparts. For example, a digital loop filter is used instead of the analog loop filter. The divider can also be replaced by a time-to-digital converter (TDC), which compares the edges of the output wave of the oscillator to a reference crystal. The input phase would also be substituted with a frequency control word (FCW). The frequency control word is then digitally compared with the output of the TDC and the output converted to a signal to control the oscillator. Finally, the voltage controlled oscillator (VCO) is converted to a digitally controlled oscillator (DCO). This is demonstrated in Figure 1.2.

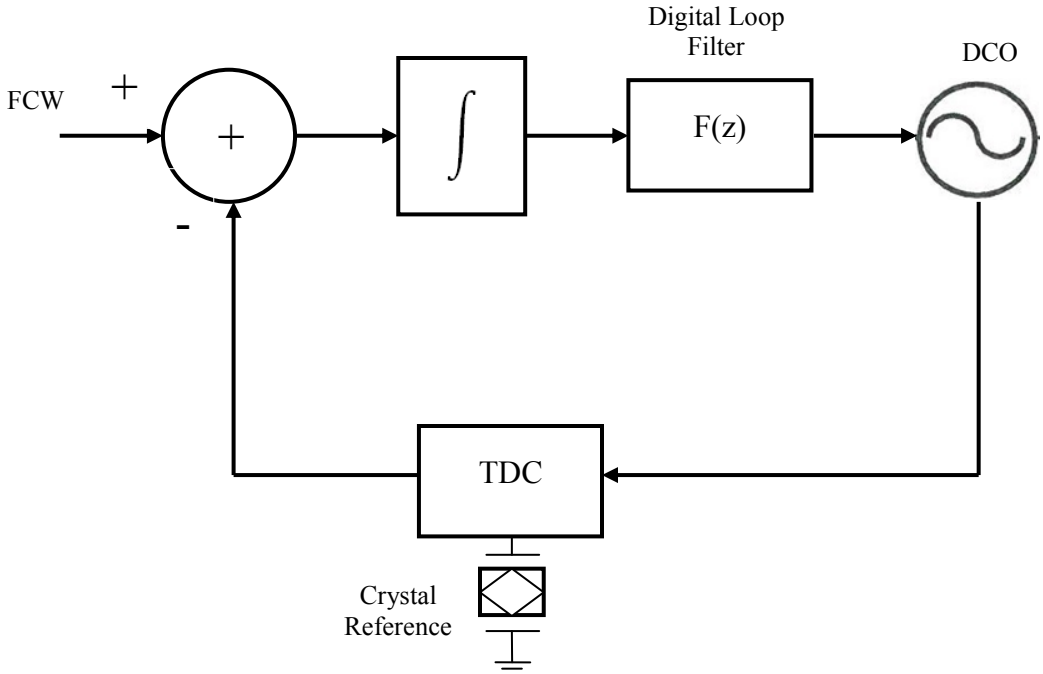


Figure 1.2: All Digital Phase Locked Loop [2]

1.3 Motivation of Research

One of the important parameters that determine the performance of an ADPLL is the phase noise in the output of the ADPLL. This describes how much the output frequency/phase would jitter due to noise from the circuit. In order to determine the phase noise, *L*, due to the resolution of the DCO, the following formula [2] is used:

$$L(s)|_{f_{res}} = 10\log\left[\frac{1}{12}\cdot\frac{f_{res}^2}{F_{ref}^3}\right] \quad \textbf{(1.1)}$$

Where f_{res} is the resolution of the DCO, (the smallest possible step in frequency) and F_{ref} is the sampling frequency.

As seen, the phase noise in an ADPLL increases with a higher resolution frequency. As the resolution improves (ie: finer resolution), the phase noise decreases and thus the spectral purity of the ADPLL improves. This research aims to explore how far the resolution of the DCO can be increased in order to produce high performance ADPLLs. The DCO designed is aimed to work at 20 GHz using 0.13 µm CMOS technology. This high frequency is used in many satellite uplinks, fiber links, and backplane data links.

1.4 Thesis Organization

This thesis describes the research involved in the design, implementation and testing of a 50 kHz resolution DCO at the 20 GHz band. Starting with Chapter 2, a background on the design of DCOs is given along with a literature review of previous research tackling the same problem. After that Chapter 3 explains the design stages of the DCO to be implemented while Chapter 4 discusses the testing procedure and the obtained results. Finally Chapter 5 discusses the results and draws conclusions on the successfulness of the design.

Chapter 2: RF Oscillator Fundamentals

This thesis focuses on the design of a digitally controlled oscillator at the 20 GHz band. Therefore, in this chapter, details of oscillator design will be provided. Firstly oscillator principles are discussed followed by detailed design steps required for a cross coupled RF oscillator, which is the topology used in this project.

2.1 Oscillator System Overview

2.1.1 System Blocks

Put in simple terms an oscillator is a device that takes power from a DC supply and converts it into an RF of a certain frequency of choice, depending on the design of the circuit [3].

In circuit terms an oscillator can be described as an amplifier that has positive feedback. This positive feedback, with enough gain, can sustain a certain frequency tone and prevent it from dying out. A system diagram for an oscillator is shown below in Figure 2.1:

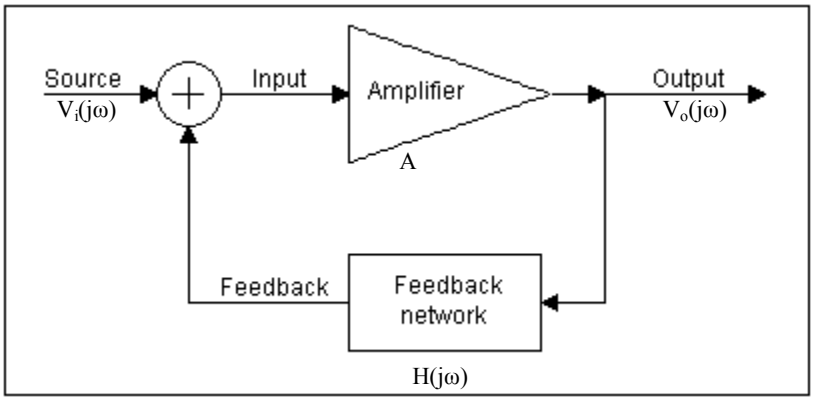


Figure 2.1: System Overview of an Oscillator

The positive feedback shown makes the loop unstable. If this feedback is frequency selective (for example by means of a high Q filter), a certain tone from the source will be allowed to increase in amplitude over time as the signal goes through the loop and gets re-amplified. Theoretically, this amplification could go on forever. However, in practice, many factors will eventually limit the amplitude of the output such as supply rails and linearity of the transistor(s) in the amplifier.

Although a source is shown in the conceptual block diagram, in reality, oscillators are not designed with a real 'source'. The circuit however does have broadband noise as an input which can ensure that the oscillations start up.

Another way to start-up an oscillator is to introduce a disturbance (or initial condition). This represents a large step voltage, which in the frequency domain is represented by a wideband input.

2.1.2 The Barkhausen Criterion

Referring back to Figure 2.1, a system with an amplifier of gain A, feedback network of response $H(j\omega)$, input voltage $V_i(j\omega)$ and output voltage $V_o(j\omega)$, can be shown to have the response [3]:

$$V_o(j\omega) = AV_i(j\omega) + H(j\omega)AV_o(j\omega) \tag{2.1}$$

Rearranging terms would then result in:

$$V_o(j\omega) = \frac{A}{1 - AH(j\omega)} V_i(j\omega) \tag{2.2}$$

The output of the oscillator would be 'infinite' when the denominator of (2.2) is equal to zero. This is known as the Barkhausen Criterion [3]. The frequency ω that would make the equation $1 - AH(j\omega) = 0$ true is the frequency at which oscillation would occur, since at this frequency, the output would effectively keep increasing in amplitude in the closed loop until bound by physical limits such as supply or transistor linearity. At this frequency the input and output of the amplifier must be adding in phase at the input of the amplifier.

2.2 Cross-coupled Oscillators

There are many ways to achieve the Barkhausen Criterion for oscillation. One of the most prominent ways to produce a differential oscillator is by using the cross-coupled topology, also sometimes referred to as $-G_m$ oscillator. This is particularly useful when driving a Gilbert cell mixer which requires a differential input.

A typical cross coupled topology is showed in Figure 2.2. The analysis in this chapter are done using bipolar transistor (to quote the sources), although they could easily be repeated using CMOS devices with the same analysis.

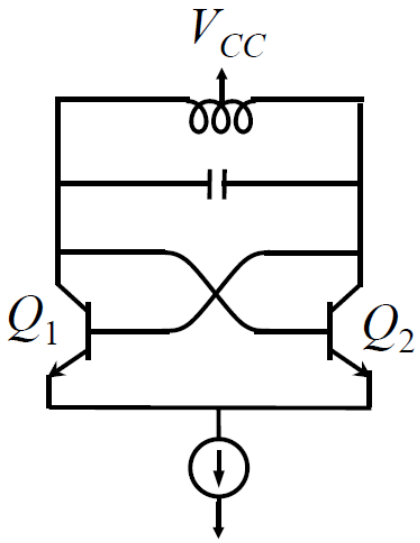
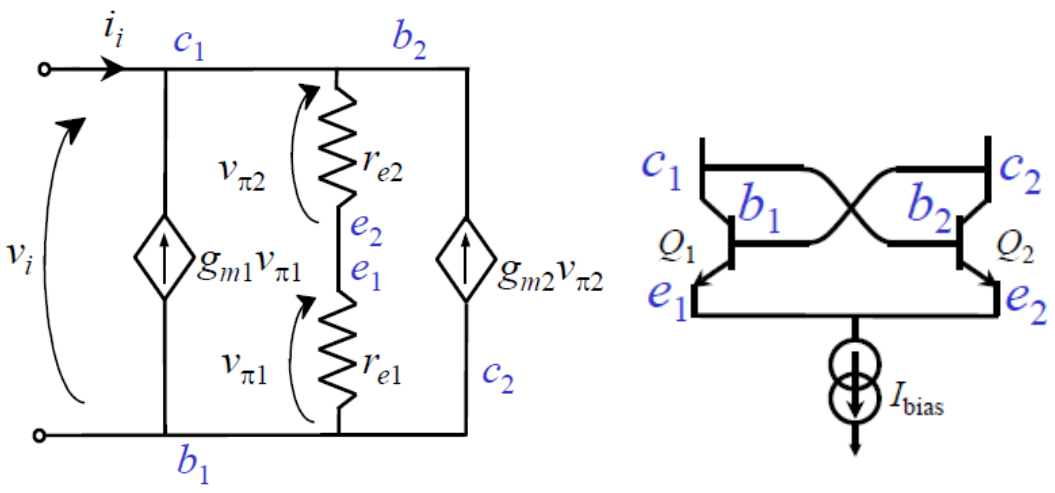


Figure 2.2: Cross-coupled Oscillator Topology

As seen, this looks like two parallel common emitter amplifiers connected together. The input of transistor Q_1 is inverted at the output (collector), due to the inverting property of common emitter amplifiers. This inverted output is then fed into the input of Q_2 which is in turn amplified and inverted again at the output of Q_2. When fed back again to the input of Q_1, the input is now in phase with the original input since it got inverted twice. This satisfies the property of being in phase required for the Barkhausen criterion.

Mathematically, the operation of the oscillator can be studied as follows. First of all, the small signal models for the transistors is used to analyse the cross coupled oscillator circuit. This is shown in Figure 2.3a, alongside with the origin of the subscripts used [4]:



(a) **(b)**

Figure 2.3 Small Signal Model and Subscript Explanation

Summing the currents in the top node we obtain:

$$i_i = \frac{v_i}{r_{e1} + r_{e2}} - g_{m1}v_{\pi 1} - g_{m2}v_{\pi 2} \tag{2.3}$$

where g_m is the transconductance of the transistor and r_e is the emitter resistor. Assuming both transistors are identical and biased in the same way, and solving for the input impedance (input voltage divided by input current), we obtain the following:

$$Z_i = \frac{-2}{g_m} \tag{2.3}$$

The negative resistance implies the instability of the amplifier and the fact that it can oscillate at a certain tuned frequency. After adding the parallel resistance of the resonator, R_p, the total resistance of the oscillator must remain negative in order for oscillations to occur. This is described in (2.4).

$$\frac{1}{\frac{1}{R_p} + \frac{g_m}{-2}} < 0 \tag{2.4}$$

Solving the equation for a condition for g_m, we obtain the biasing condition required for the transistor in order for oscillations to occur:

$$g_m > \frac{2}{R_p} \tag{2.5}$$

2.3 Frequency of Oscillation and Frequency Tuning

After setting the condition for oscillation in the amplifier, the frequency of oscillation must be set. In some microwave oscillators, the positive feedback condition is already frequency dependent due to depending on s-parameters of the transistor, which in turn depend on the transistor configuration and biasing [3]. However in the cases of Colpitts or cross-coupled oscillators, a high Q frequency selective circuit is required to make sure only the required frequency propagates in the oscillator.

2.3.1 LC Tank Circuit

As seen in a typical cross-coupled pair in Figure 2.2, an LC resonator circuit is added in parallel to the transistors. This creates a high Q filter which allows only the required frequency to be the frequency of oscillation. The frequency of resonance of the LC circuit is given by [4]:

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{2.6}$$

where L is the inductance and C is the capacitance of the tank circuit. It must be noted that at lower frequencies this model is sufficient. However at higher frequencies such as at RF and microwave frequencies, other important factors are significant too. For example on integrated circuits, the interconnect between the circuit components (especially near the LC tank) will affect the inductance of the resonance frequency. Moreover, the parasitic capacitance of the transistors has a significant effect on the value of capacitance in the circuit [4]. Other important factors also include the parasitics of the inductor and capacitors being used in the resonator. As a result, performance of RF circuits is never calculated in details beforehand. Instead a rough estimation of performance is done on paper, after which simulation is done to determine the actual performance of the circuit [4].

2.3.2 *Frequency Tuning*

Most oscillators are built such that their frequency can be adjusted. This is important because even after extensive simulations, many factors can affect the value of the resonance frequency of the tank circuit. These include temperature variations that can affect the value of capacitance or g_m of the transistor and variations in the power supply that could change the biasing of the circuit. Another perhaps more significant factor is process variation. During the chip fabrication process, a thicker (or thinner) layer of metal may be deposited which can greatly affect the value of capacitance or inductance of an on chip capacitor or inductor. As a result, it is important to be able to control the frequency of oscillations after integrated oscillators are fabricated to compensate for any unwanted frequency shifts. =

Moreover, for RF applications, oscillators need to be tunable in order to be able to select the channel frequency in an RF transceiver. Channels are usually a few megahertz apart and so the tuning also has to be relatively fine.

There are quite a few methods employed to tune frequencies in oscillators. Perhaps the most common method is using varactors. Put in simple terms, varactors are capacitors whose capacitance value changes depending on the bias on it.

One type of varactor is called MOS varactors. MOS varactors are formed by connecting the source and drain of a MOSFET together as one terminal of a capacitor and using the gate of the MOSFET as the other terminal. This is shown below in Figure 2.4.

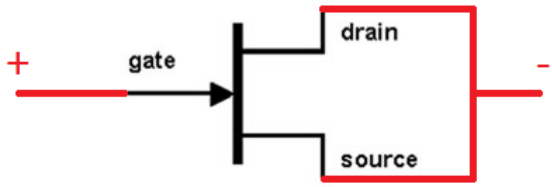


Figure 2.4: A MOS Varactor

The capacitance between the drain/source connection and the gate connection is affected by the depletion region formed beneath the gate oxide, and hence this becomes a voltage dependent capacitance [4].

Another alternative is the AMOS varactor where N+ regions, make connections to an n-well instead of forming the source and drain of an NMOS transistor. Because the structure looks similar to a MOS transistor, the substrate connections are still commonly labeled as source and drain. This is illustrated in Figure 2.5:

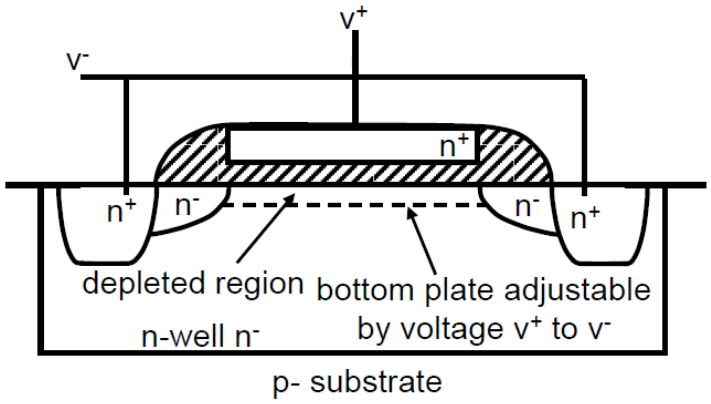


Figure 2.5: AMOS Varactor in a P-Substrate Process [4]

Depending on the voltage applied between the gate and the well, the depleted region's thickness can change, thus changing the capacitance of the varactor. This is explained in Figure 2.6.

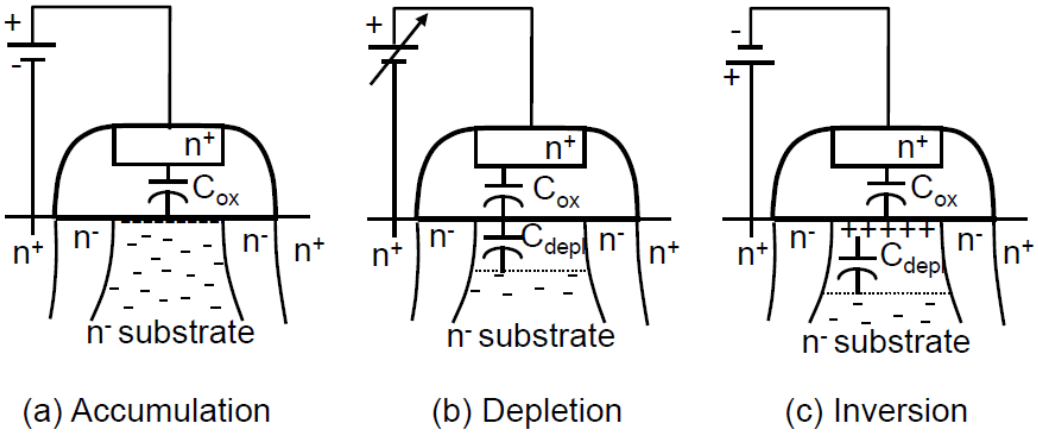


Figure 2.6: States of AMOS Varactor [4]

The varactor is made of two capacitors in series: C_{ox}, the capacitance due to the gate oxide, in addition to C_{depl}, the capacitance due to the depleted region. The capacitance due to the deplet-

ed region can be modelled using a parallel plate capacitor model. This is given by the following formula:

$$C = \frac{\varepsilon A}{d} \tag{2.7}$$

C is the capacitance, ε is the permittivity of the material (in this case, doped silicon), while A represents the area of the capacitor, which in the varactor example is the area of the gate and d is the distance between the two plates of the capacitor, in this case the distance between the substrate and the gate, or in other words the thickness of the depleted region. As suggested by the formula, when the depleted region is at its largest thickness, the capacitance is at a minimum value, while when the depleted region is at a minimum, the capacitance is at the largest value.

As shown in Figure 2.6, at maximum positive voltage (accumulation), there is no depleted region since the negative carriers from the n-substrate are attracted to the gate. This results in the maximum capacitance, equal to C_{ox}, the oxide capacitance. However as the gate to drain voltage decreases, the gate starts attracting positive carriers (holes) near it. This creates the depleted region which keeps increasing in size as more holes gather beneath the gate. The state at which maximum holes are gathered beneath the gate oxide is called inversion [4].

2.4 Noise in Transistors

Transistors have a several types of noise associated with them. The first type of noise is thermal noise [4]. This is simply present due to the fact that conductive channels in a transistor have a resistance associated with them. This results in a noise voltage source of a value that is simply 4kTR, where R is the channel resistance, T is the Kelvin temperature and k is the Boltzmann constant.

Another noise source associated with CMOS devices is called induced gate noise [4]. This is noise that is present due to the distributed nature of the transistor and is most prominent at frequencies past about one tenth of f_T of the transistor. It is given by a current source whose value can be calculated as follows:

$$i_{ng}^2 = \frac{4kT\delta\omega^2 {C_{gs}}^2}{5g_m} \tag{2.8}$$

Here, δ is a parameter related to the short channel modulation of the transistor while C_{gs} is the gate-source capacitance of the MOSFET.

Finally, another important source of noise is called 1/f noise (also known as flicker noise) [4]. This noise is more prominent at lower frequencies and weakens as the frequency increases. In most RF applications, 1/f noise can be ignored due to its dominance at lower frequencies. However, in the case of oscillators, this kind of noise affects the output at low frequency offsets from the main tone and so it plays an important role in determining the phase noise of the oscillator, especially at lower frequency offsets. In a MOSFET, 1/f noise is given by

$$v_{nf}^2 = \frac{K_f}{WLC_{ox}f} \tag{2.9}$$

In this equation, K_f is a process constant, W and L are the transistor dimensions and C_{ox} is the oxide capacitance at the gate.

2.5 Phase Noise in RF Oscillators

The Leeson formula [4] can be used to calculate the phase noise of an oscillator and is given by:

$$L = \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2 \left(\frac{FkT}{2P_s}\right) \tag{2.10}$$

In (2.10), ω_0 is the oscillator (centre) frequency, Q is the effective quality factor of the tank circuit, $\Delta\omega$ is the frequency deviation away from the center frequency. F is the noise factor of the oscillator, k is the Boltzmann constant, T is the Kelvin temperature while P_s is the output power of the oscillator.

Oscillator phase noise directly affects the phase noise in a phase locked loop and so it is essential that the oscillator being designed have a low phase noise. Moreover for design purposes, if the phase noise of the oscillator is too high, the high resolution changes of the frequency will not be noticeable since there will be too much jitter on the frequency.

Chapter 3: Current Work on High Resolution DCOs

As explained in Chapter 1, high performance DCOs are important for obtaining better phase locked loops. In this chapter a summary of previous work on DCOs is provided explaining the different techniques used and the results obtained.

3.1 Source-Gate Transformation to Realize Smaller Capacitor Values

In order to obtain higher resolution, one method is to be able to switch very small values of capacitance. According to [5], one way to achieve this is to use capacitive degeneration. If one were to move the tank varactors from where they are to the source of the cross-coupled pair, one can use the multiplication (or division in this case) factor of looking at the source from the gate of the transistor. Results from [5] suggest that multiplication factor of about 500 could be achieved and so using a varactor of value 5 fF can effectively be a switchable 10 aF varactor. Figure 3.1 shows the circuit used order to achieve this:

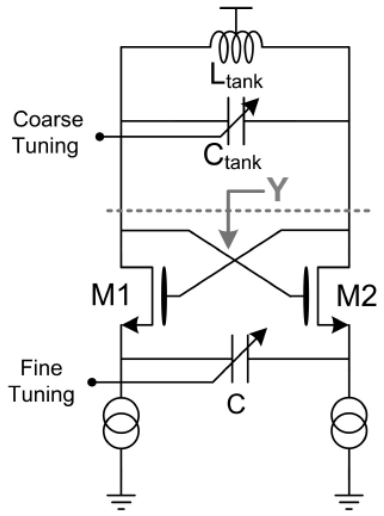


Figure 3.1: Capacitive Degeneration [5]

This circuit achieved a tuning resolution of 150 Hz, with a phase noise of -127.5 dBc/Hz at 1 MHz offset, equivalent to a figure of merit of 183 dBc/Hz. The center frequency is 3.0 GHz though which is quite lower than the required band for this research. In principle though, it should still work at higher frequency since source transformation occurs at all frequencies, but

perhaps working with a smaller multiplication factor since the g_m of the transistor drops at higher frequencies. However in order to achieve kilohertz resolution at 20 GHz, one requires less than 10 aF of switchable capacitance. Therefore more methods are investigated.

3.2 Difference in Switched Values between PMOS and NMOS Varactors

Another method for obtaining resolution that depends on capacitance values is explained in [6]. This method relies on the fact that in fully switched minimum sized varactors, PMOS and NMOS varactors have a small difference in values. This is illustrated in Figure 3.2:

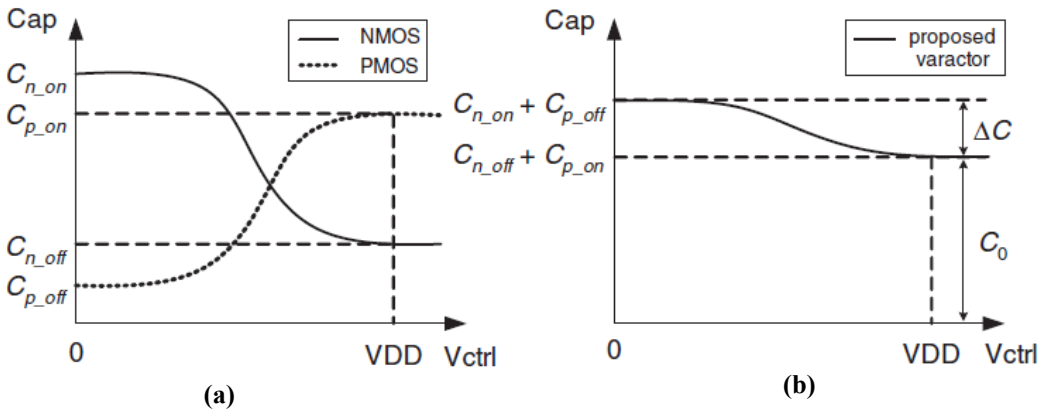


Figure 3.2: Switching PMOS and NMOS Varactors [6]

In Figure 3.2 (a), the individual C-V characteristic curves of PMOS and NMOS varactors are displayed. However if both varactors are connected in parallel with the same control voltage applied to them (see Figure 3.3), one can obtain the graph in Figure 3.2 (b).

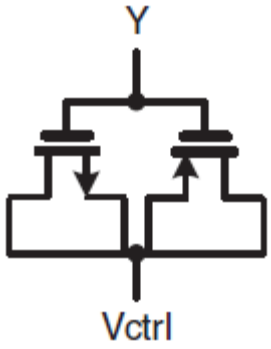


Figure 3.3: PMOS and NMOS Connection

This method results in a difference in capacitance, ΔC equal to 0.8 aF corresponding to 1.4 kHz of resolution. This DCO has a phase noise of -118 dBc/Hz at 1 MHz offset, centered at 5.0 GHz. However at 20 GHz, carefully controlling the ΔC required in this design would be very tough. This is due to the significant effect of parasitics and process variations on circuits operating at such high frequency.

3.3 Difference in Capacitance of PMOS Varactor Modes

According to [7], the implementation explained in [6] has a problem that could affect performance. It is suggested that NMOS varactor would run into the problem of well isolation which would result in more flicker noise leading to a worse phase noise performance for the oscillator at lower frequency offsets. As a result, an improvement is suggested by using two PMOS differential varactor pairs in parallel, with one pair connected at the gate while the other at the substrate. Moreover the control signal would be the opposite of the other. With increasing control voltage, this leads to one pair switching from depletion to inversion while the other switches accumulation to depletion. The small difference in varactor value between accumulation and inversion modes of the opposite varactors gives the required small capacitance change, as explained in Figure 3.4.

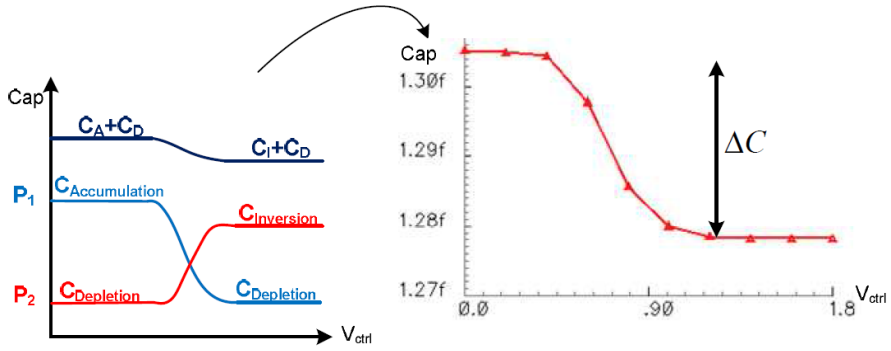


Figure 3.4: Performance of Two Oppositely Connected PMOS Varactor Pairs [7]

Figure 3.5 demonstrates how the connection is done between the PMOS pairs:

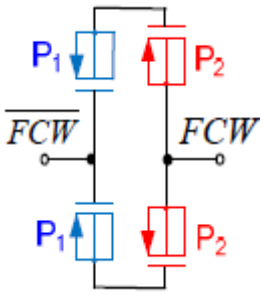


Figure 3.5: Schematic Connection (FCW is the Frequency Control Word)

This method yields a switchable capacitance of 3.5 aF. At 5.6 GHz, this corresponds to 14 kHz of frequency resolution. The DCO has a phase noise of -117 dBc/Hz at 1 MHz offset. This method provides a good technique to achieve a fine resolution DCO.

3.4 *ΣΔ* Dithering

One common method of achieving high resolution in oscillators is using high speed ΣΔ dithering [8]. Dithering involves the rapid switching of varactors on and off at a certain rate and so on average, the effective value of the capacitors would seem to be only a fractional number between the two varactors being switched to and from, resulting in better resolution. The technique is also used in fractional PLLs in order to achieve a non integer divider ratio [1]. This technique can achieve very high resolutions such as 14 kHz [9]. This resolution was obtained by combining the technique explained in section 3.3 in addition to dithering.

Dithering however requires high speed switching circuits at the input, a complication that would use up a lot of power and would make the circuit more complicated and more expensive to produce.

3.5 Connecting Varactors in Series with a Fixed Capacitor

Another method used to obtain fine tuning is to connect the varactors being switched in series with a small capacitor [10]. The suggested topology is shown in Figure 3.6.

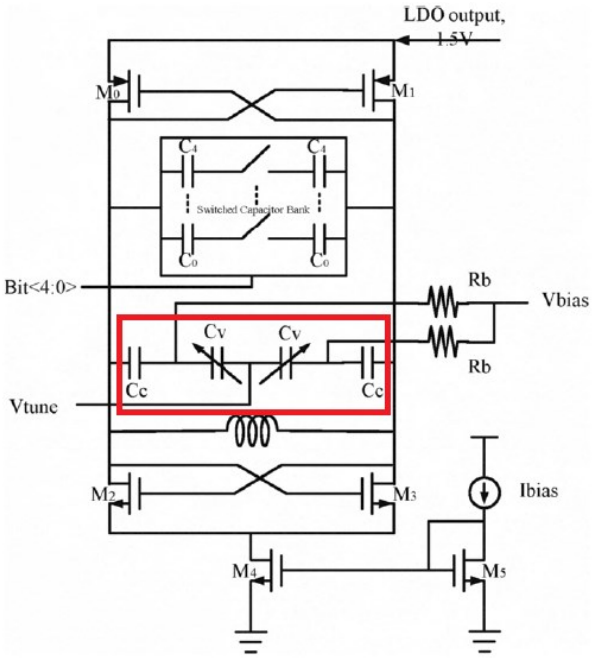


Figure 3.6: Using a Varactor and Capacitor in Series [10]

The small fixed capacitor in series with the varactor diminishes the effect of the change in capacitance of the varactor. This means that a much smaller switched capacitance can be achieved.

Unfortunately, the paper focussed on this topology did not publish results for the resolution of the VCO since it was more directed at it being a wideband VCO with a low tuning sensitivity. However this idea seemed like it could be exploited more for the topic of higher tuning resolution. As a result, the last chip designed for this thesis is focussed on this technique.

3.6 Other Methods in Literature

There are more methods that have been investigated to achieve fine resolution DCOs that have not been described in this chapter. Reference [11] discusses the manipulation of frequency control words in a purely digital fashion to achieve fractional switching of the varactors. More

digital solutions are also presented in [12] using binary controlled pass transistors and low power Schmitt triggers. Varying delay-line lengths in a ring oscillator is also discussed as a possible manner to change the phase and thus eventually the frequency of an oscillator [13]. Reference [14] uses the Miller multiplication effect of series to parallel conversion of capacitance along with delay elements in a ring oscillator to achieve fine resolution. Perhaps one of the most interesting methods discussed was research done to influence the inductance of an inductor by adding metal strips beneath it [15]. By configuring these metal strips with MOS switches, the capacitive loading of the tank circuit can be changed minutely and thus introducing a small change in frequency.

All of the techniques mentioned in this chapter are worth further investigation. However due to the time constraints of the master's degree and the delay of the fabrication cycle from the available foundry, only one method was investigated. This method was based on the technique discussed in Section 3.5.

Chapter 4: On-chip High Resolution DCO Design

After investigating previous attempts at obtaining high resolution in oscillators, the next step was to investigate novel ways to push the limit of resolution based on the literature. It can be noted that almost all the papers reviewed that covered resolution were concerned with much lower frequencies (<10 GHz), mainly for commercial applications such as Bluetooth, Zigbee and WiFi applications. Little research has been done into obtaining resolution at 20 GHz, which was more incentive to attempt to achieve higher resolution at such a high frequency. 20 GHz was also the frequency required by a local company investigating ADPLLs that were looking for oscillators with superior resolution.

In this section three main designs will be discussed, with the final having the finest theoretical resolution. In each case, the design theory is discussed in the beginning followed by simulation and implementation in a 0.13 µm CMOS process. Post layout simulation is then done followed by experimental results obtained from testing the chip (except for the second design). Chapter 5 will include a commentary on the results obtained.

4.1 Using the Smallest Available Varactor

The first attempt at achieving high resolution was by "brute force". That is, knowing that the smaller the varactor, the smaller the change in capacitance, this design was focussed on using the smallest possible varactor available in the design kit. This had a value of around 1 fF, which theoretically is much less than the parasitic capacitance added to the lines after layout. However the idea under investigation was that this capacitance would still be switchable and should display a difference in frequency of oscillation when switched.

4.1.1 Design

The change in frequency in an oscillator is related to the change of capacitance over the overall value of capacitance given by $\Delta C/C_{total}$. Therefore to achieve a smaller change in frequency, it is required to maximize the denominator (C_{total}) while minimizing the change in capacitance. Therefore, in a resonator tank circuit to achieve a certain center frequency, one must minimize the inductance in order to afford using a larger value of capacitance (see (2.6)). It must be

noted, however, that decreasing inductance will decrease the tank resistance in the circuit and thus result in smaller oscillator amplitude.

In the kit provided, the minimum value of inductance provided by a spiral inductor is about 101 pH at 20 GHz with a Q close to 20. However a characterized RF transmission line can provide about half of this inductance at a slightly higher Q, which means near 100 pH, the RF line would also have better Q than the spiral inductor (as shown in Figure 4.1). As a result, for this design, characterized RF transmission lines are used instead of spiral inductors.

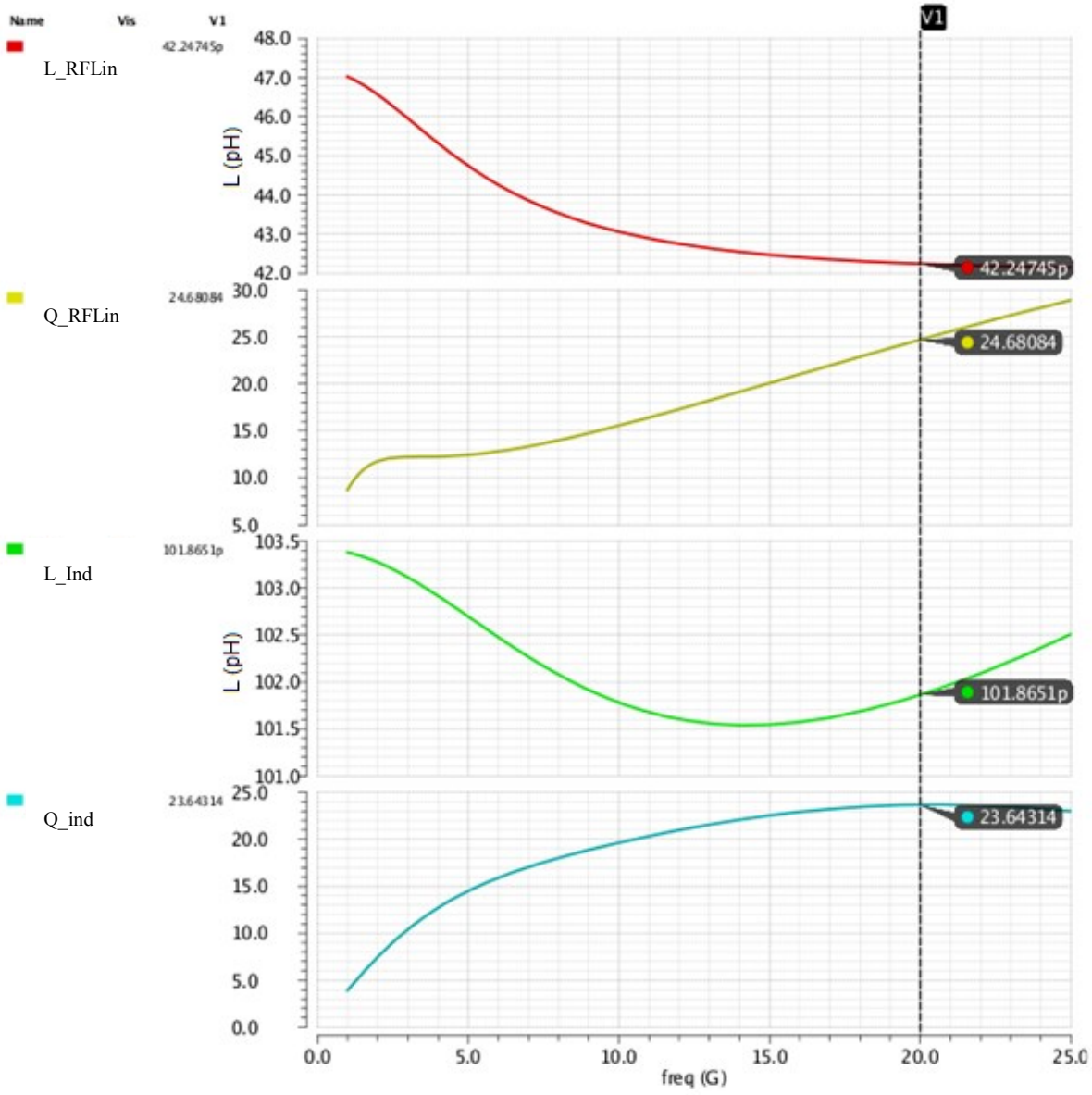


Figure 4.1: Characterization of Smallest Possible Inductor and RF Lines

A characterized transmission line of 56 pF is chosen at 20 GHz. The slight increase from the minimum value will help against process variation. At such a high frequency, the smallest change in length will greatly affect the inductance and thus throw off the center frequency of the oscillator.

After choosing the RF transmission lines, the varactors were then studied. Figure 4.2 shows the characterization circuit for the smallest n-type varactors.

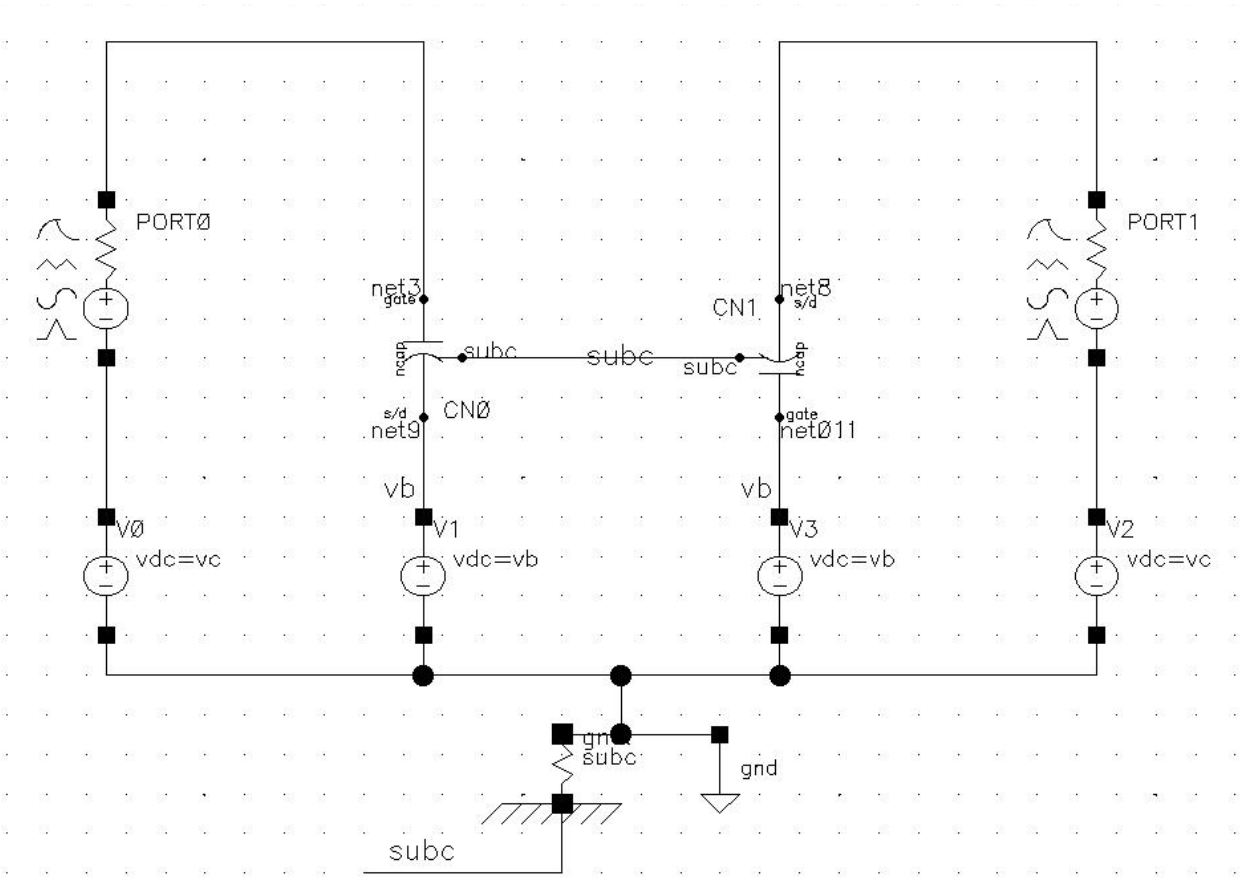


Figure 4.2: Varactor Characterization Circuit

In order to avoid having a significant effect of parasitics on the capacitance of the varactor, the channel length is set to 290 nm rather than the minimum 240 nm and the size of the varactor was increased to 2 gates instead of 1 (the latter is also done to improve the Q, since it decreases the channel resistance and hence provides less loss). The varactor was then simulated applying the control voltage to the gate once and then to the substrate. The bias voltage *vb* was kept at the rail (1.2 V), since this is how it would be in the proposed $-G_m$ cross coupled oscillator. Figure 4.3 shows the obtained capacitance and Q while changing the control voltage at 20 GHz.

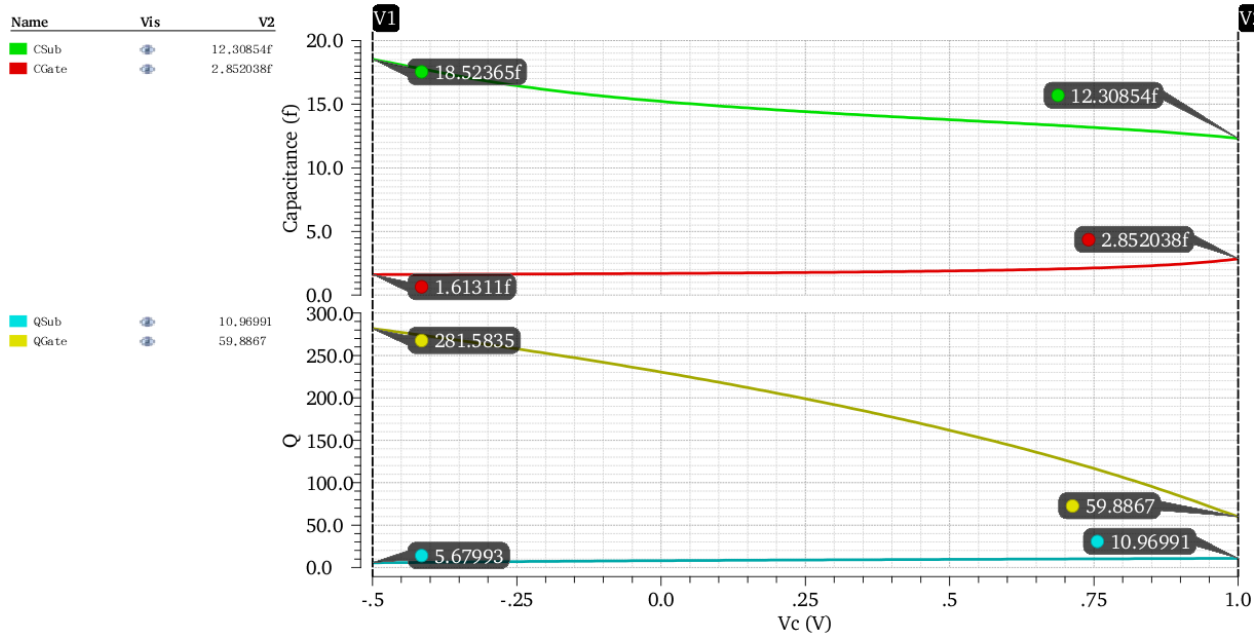


Figure 4.3: Varactor Characterization

As seen above, measuring the capacitance from the gate results in a significantly higher Q and in less capacitance. This would be useful to the oscillator since the higher Q will mean a less lossy resonator and higher output amplitude. Moreover the smaller capacitance is also desired to help achieve the finer resolution as per the technique described earlier. As a result, the first topology is chosen for the set of varactors. A total of 7 sets of varactors will be used to change the frequency, each set being controlled digitally.

Referring to (2.6) to obtain the capacitance of the circuit:

$$C_{total} = \frac{1}{\omega^2 L} = \frac{1}{(2\pi \times 22 \times 10^9)^2 \times 56 \times 10^{-12}} = 935 \text{ fF} \quad \textbf{(4.1)}$$

In this design, a target frequency of 22 GHz was set in the hope that after layout and fabrication the frequency would be approximately 20 GHz. The gate capacitance at this frequency is approximately estimated at about 100 fF, so subtracting this along with the varactor capacitance from the total capacitance yields the amount of fixed capacitance required:

$$C_{fixed} = C_{total} - \left(C_{gate} + C_{varactor}\right) = 935 - (100 + 7 \times 1.61)$$
$$C_{fixed} = 823 \text{ fF} \quad \textbf{(4.2)}$$

This capacitance will be provided by dualmimcap capacitors which have a compact size for such a capacitance. Even though their value of Q is not as good as that of vertical capacitors at

that frequency, their smaller size makes them a good choice since the parasitics from interconnect play an important role at 20 GHz. However the small size of dual mimcaps makes the effect of parasitics on their value more prominent since with the smaller size, the same fringe capacitance will translate to more parasitic capacitance. Ideally, this extra capacitance should be modelled by the kit when running higher frequency simulations.

The expected frequency resolution can be given by the following formula: (derived from (2.6))

$$\frac{f_{min}}{f_{max}} = \sqrt{\left(\frac{C_{min}}{C_{max}}\right)} \tag{4.3}$$

Solving:

$$f_{min} = \sqrt{\left(\frac{C_{min}}{C_{max}}\right)} \cdot f_{max} = \sqrt{\left(\frac{821 + 100 + 7 \times 1.61}{821 + 100 + 7 \times 2.85}\right)} \cdot 22\ \text{GHz}$$

$$f_{min} = 21.89829\ \text{GHz}$$

As a result, assuming monotonic steps in frequency, and having 8 steps, the frequency resolution of the oscillator is given as:

$$\Delta f = \frac{f_{max} - f_{min}}{N} = \frac{22\ \text{GHz} - 21.89829\ \text{GHz}}{8} = 12.7\ \text{MHz} \tag{4.4}$$

After characterizing the passives, the transistor was then sized and characterized. As suggested by (2.5), the g_m of the oscillator needs to be greater than $2/R_p$, R_p being the equivalent lossy component of the resonator. Determining R_p is also necessary for calculating the phase noise of the circuit.

The parallel lossy resistance is composed of two main components. The first component is due to the transmission line used as an inductor. Its resistance per side can be calculated as follows using the numbers obtained from the characterization of the inductor:

$$R_L = \omega L Q = 2\pi \times 22\ \text{G} \times 56.1\ \text{p} \times 32.9 = 255.1\ \Omega \tag{4.5}$$

Similarly capacitive component of the parallel resistance can be calculated as follows. It is composed of the loss due to the fixed vertical capacitor in addition to the loss due to the varactor. The loss of the varactor is calculated in (4.6) using values obtained from Figure 4.3.

$$R_{var} = \frac{Q}{\omega C} = \frac{282}{2\pi \times 22\ \text{G} \times 1.61\ \text{f}} = 1.27\ \text{M}\Omega \tag{4.6}$$

In a similar manner, the fixed capacitor is characterized and its equivalent loss resistance is calculated. A fixed 821 fF dualmimcap capacitor has a Q of about 11.4 at 22 GHz. Using (4.6), this yields an equivalent loss resistance R_{fixed} of 100.2 Ω.

The overall resistance of the tank circuit can now be calculated by finding the parallel equivalent of seven varactors, a fixed capacitor and a transmission line connected in parallel as shown in (4.7). Note the factor of two beside each resistor to convert from single ended parallel resistance to differential parallel resistance.

$$R_p = \frac{1}{\frac{7}{2R_{var}} + \frac{1}{2R_{fixed}} + \frac{1}{2R_L}}$$

$$R_p = \frac{1}{\frac{7}{2.54\ \text{M}\Omega} + \frac{1}{200.8\ \Omega} + \frac{1}{510.2\ \Omega}} = 144\ \Omega \tag{4.7}$$

It is assumed in this design that by using lower metal layers, the inductance is reduced to a minimum and so as a result their parallel resistance was not taken into account.

The minimum g_m of the transistor required can now be calculated as:

$$g_m > \frac{2}{144} = 13.9\ \text{mS} \tag{4.8}$$

A 50 µm transistor is chosen to achieve such g_m. 25 fingers of 2 microns length each is used to achieve the required gain. Moreover the length is kept at a minimum (120 nm) to achieve the best frequency response and noise performance. This is because the more the higher the channel length, the higher the channel resistance is and the higher the gate capacitance of the transistor is. The larger capacitance worsens the frequency response, while the larger resistance introduces more channel noise to the circuit.

This transistor is then characterized to see its current and g_m response for different bias conditions. The results are shown in Figure 4.4. The graph for g_m is obtained by taking the derivative of the I_D graph with respect to the gate-source voltage.

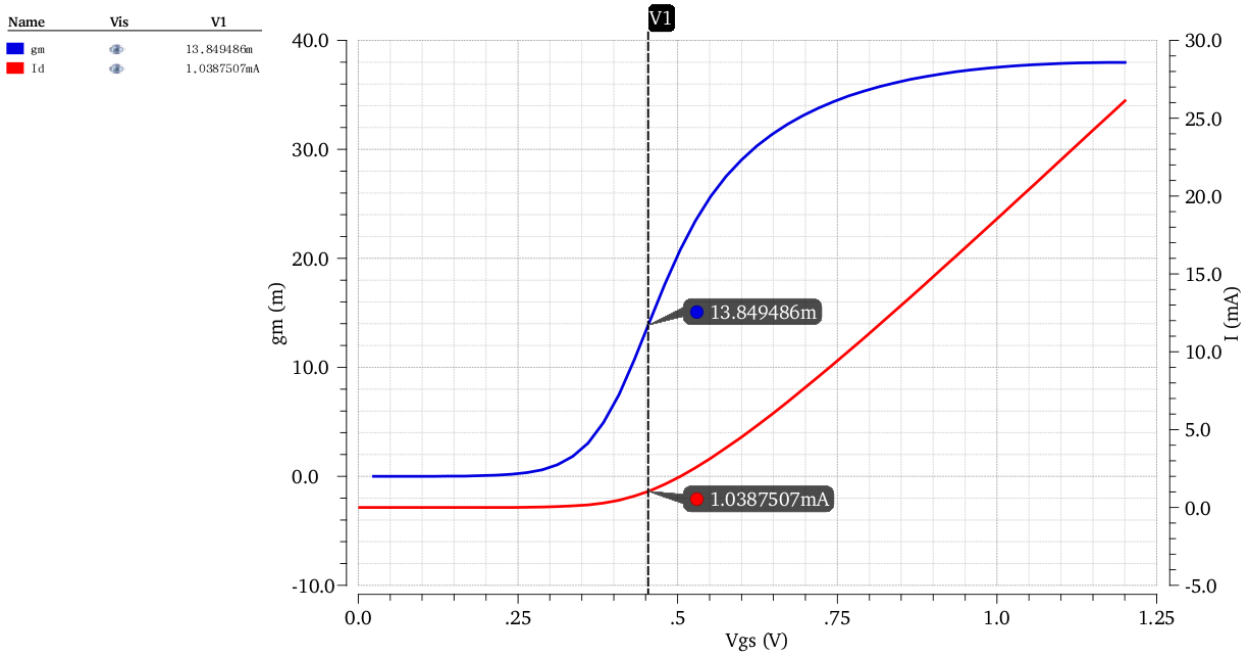


Figure 4.4: Transistor DC Characterization

The graph shown above demonstrates how the transconductance of the transistor behaves with varying bias current. At the minimum required g_m (see (4.8)), the bias current is roughly 1 mA. As a result to guarantee oscillation, the bias current is initially set at 4 mA for the transistor. A higher current is needed since at 20 GHz, the g_m of the transistor will be slightly less due to the parasitic components drawing current and thus decreasing the overall g_m for the same current. However, this will need to be optimized based on performance. (Note that this number is slightly too high compared to the minimum required minimum current, due to an error in calculating the parallel resistance during the design process – the conversion between single ended and differential parallel resistance was missed leading to a minimum current of about 2.7 mA).

For biasing the transistors, a current mirror of 1µm length transistors is chosen to increase the output resistance of the current mirror. Moreover, a source follower buffer was chosen to isolate the output from the tank circuit and prevent loading. The buffer also boosts the signal power from the output of the tank.

Finally, the phase noise of the circuit can be calculated using Leeson's Formula as demonstrated in (2.8). Firstly, the Q of the tank circuit can be calculated using the following formula.

$$Q = R\sqrt{\frac{C}{L}} = 144\sqrt{\frac{935 \times 10^{-15}}{56 \times 10^{-12}}} = 18.7 \tag{4.9}$$

The noise figure can also be calculated using (4.10) [4]. The short channel modulation, γ, is estimated to be 2 since at 4 mA of bias, short channel effects become more apparent. The fraction at which the transistors are turned on, ρ, is also estimated to be 0.8.

$$F = 1 + 4\gamma g_m R_p(1-\rho) = 1 + 4 \cdot 2 \cdot 27\text{m} \cdot 144 \cdot 0.20 = 7.22 \tag{4.10}$$

In order to calculate the power dissipated in the tank, the tank voltage swing needs to be calculated. This is given by [4]:

$$V_{tank} = \frac{2}{\pi} I_{tank} R_p = \frac{2}{\pi}(2 \times 4\ m) \cdot 144 = 0.732\ \text{V} \tag{4.11}$$

Therefore, the power dissipated is equal to:

$$P_S = \frac{{V_{tank}}^2}{2R_P} = \frac{0.732^2}{2 \cdot 144} = 1.86\ \text{mW} \tag{4.12}$$

Finally all the components can be plugged into Leeson's Formula to calculate the phase noise at 1 MHz offset as follows:

$$L = \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2 \left(\frac{FkT}{2P_s}\right)$$

$$L = \left(\frac{(2\pi \times 20 \times 10^9)}{2 \cdot 18.7\ \times 2\pi \times 10^6}\right)^2 \left(\frac{7.22 \cdot 1.38 \times 10^{-23} \cdot 298}{2 \times 1.86 \times 10^{-3}}\right)$$

$$L = 2.28 \times 10^{-12} = -116.4\ \text{dBc/Hz} \tag{4.13}$$

4.1.2 Implementation and Simulation

After characterizing the passives and actives the next step was to implement the circuit in Virtuoso Schematic Editor in Cadence. Figure 4.5 shows the circuit used. (See Appendix for a table of values of components used).

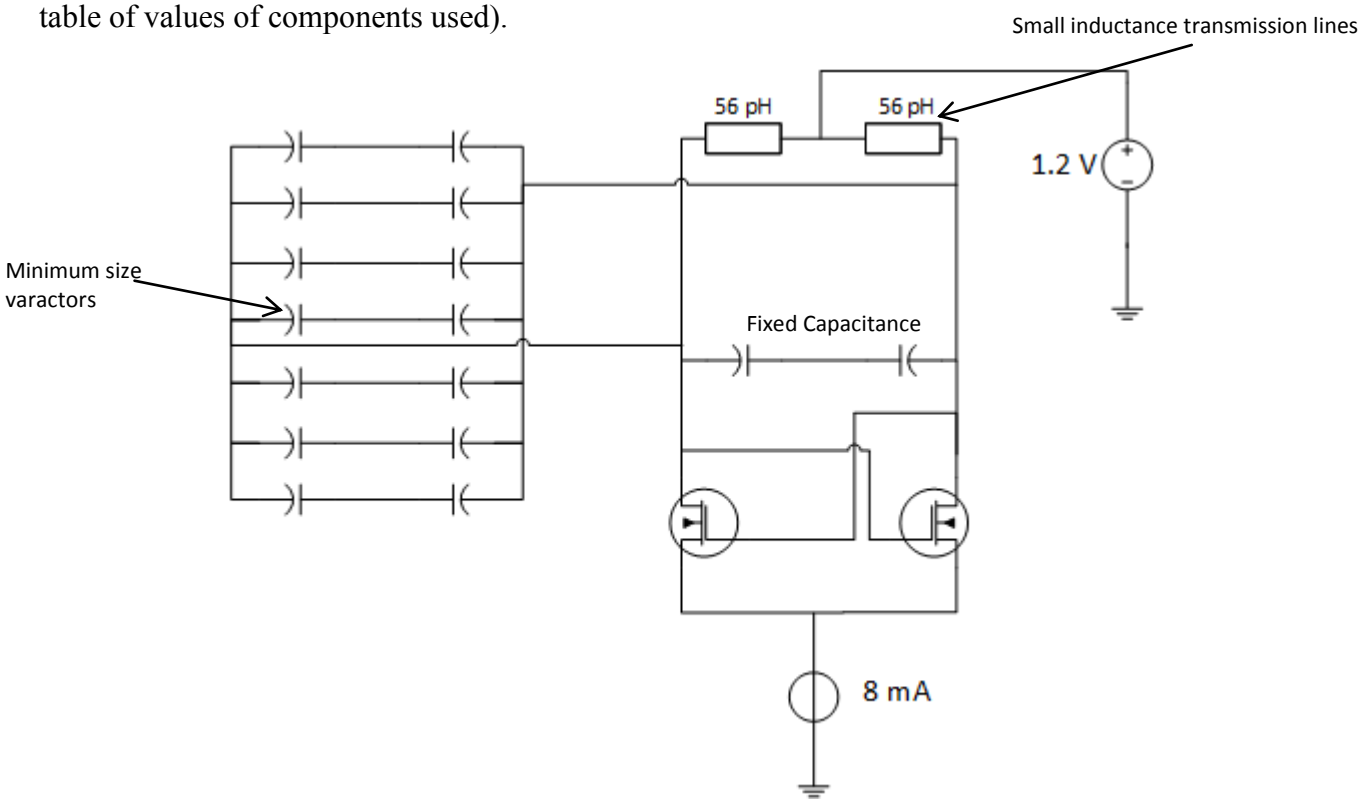


Figure 4.5: Initial Simulation Circuit

Transient simulation is performed to make sure the oscillator oscillates and to figure out the stabilization time. Figure 4.6 shows the transient results obtained at the oscillator core (before the buffer stage). An initial condition of 1 V is set on one side of the tank to get the oscillations starting. This would create a small transient signal due to the steady state value of the rail being at 1.2 V and thus induce oscillation. In a real circuit, ambient noise would be enough to get the oscillations started.

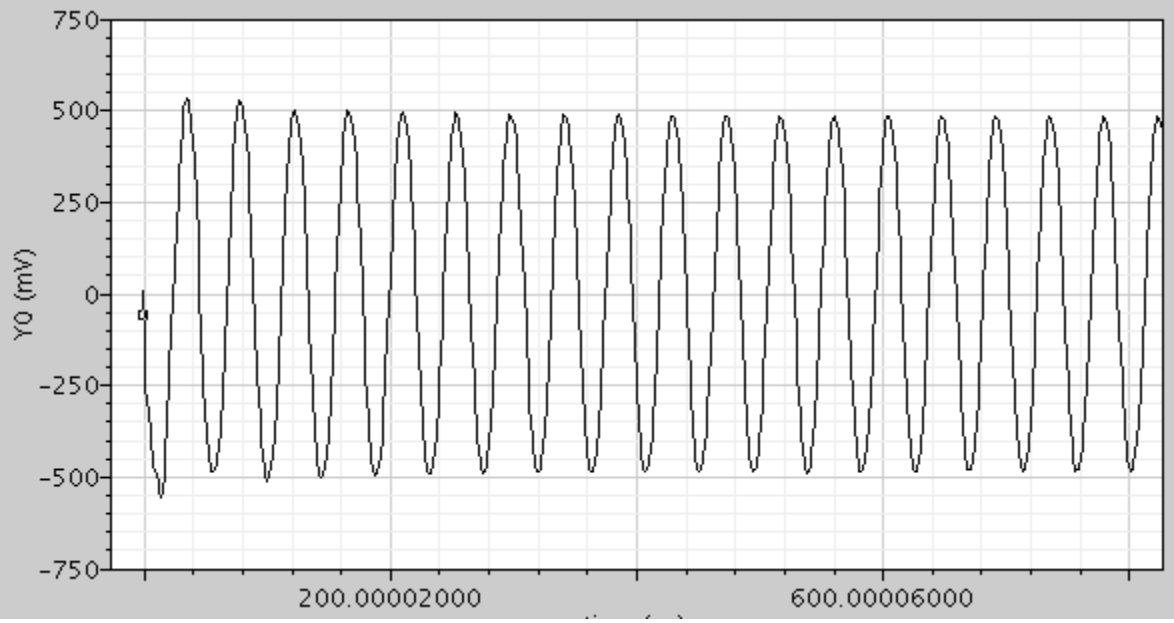


Figure 4.6: Transient Simulation

As seen above, the oscillator almost starts immediately due to the initial kick it is given. The amplitude is also slightly higher due to the unstable conditions from the initial kick. The peak voltage swing on the drain is about 500 mV (compared to the 732 mV predicted by calculation). This difference can be explained by the large signal operation that is unaccounted for in calculation. The g_m of the transistor is slightly less at 20 GHz than that predicted at DC charecterization. Periodic steady state analysis (PSS) is then performed in order to determine the output frequency and noise performance and a 'tstab' of 50 ns is chosen in order to make sure steady state is reached. Figure 4.7 shows the obtained results for this simulation:

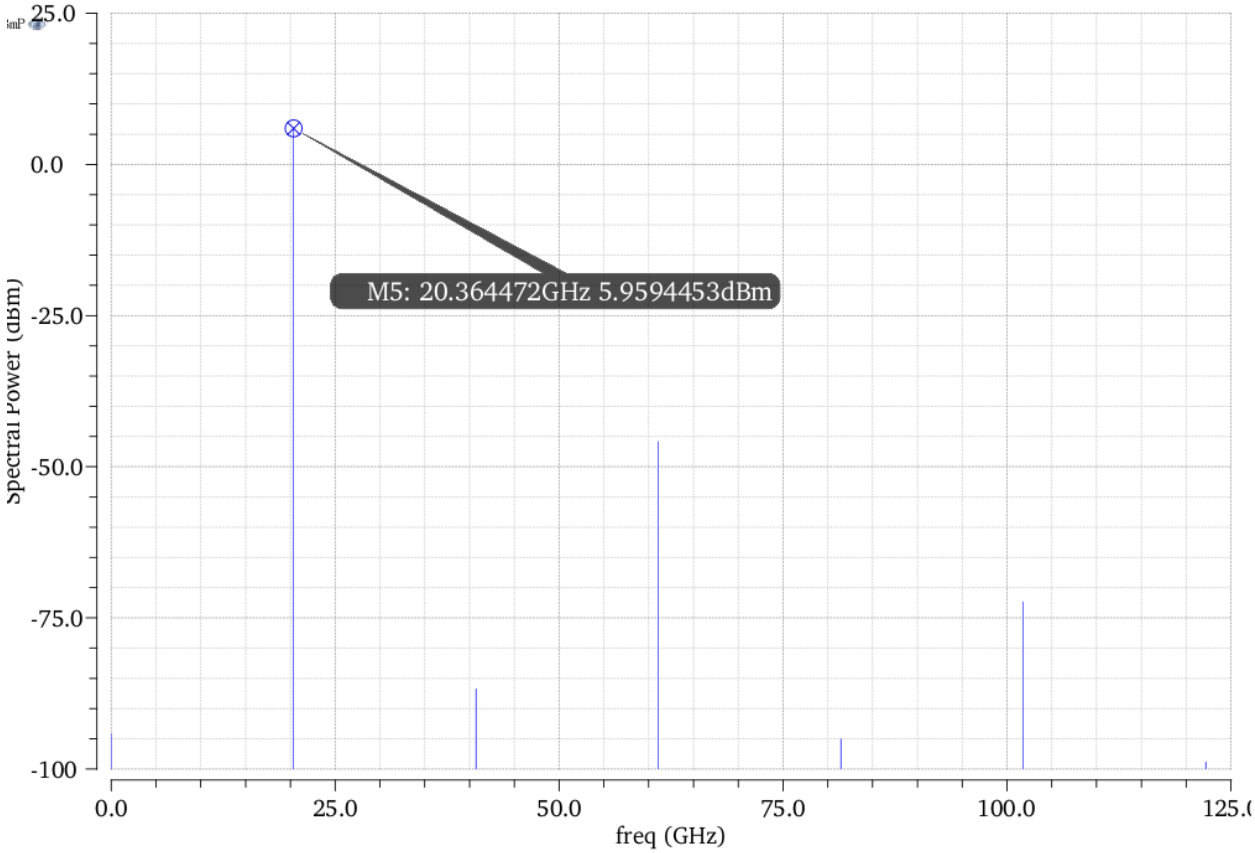


Figure 4.7: PSS Analysis Results

As seen in the spectrum response, the output of the oscillator is at about 20 GHz rather than the intended 22 GHz. This offset is mainly due to extra parasitic capacitance in the transistor model that was not accounted for in the calculation. Moreover, all the characterizations for the devices were done for small signal periodic steady state. The equations governing these characteristics become less accurate in a device such as an oscillator which is a large signal non-linear circuit.

Another observation in the results is the much lower amplitudes of the even harmonics. This is an advantage of differential circuits where even harmonics tend to cancel out.

In order to set the oscillator back to 22 GHz, the fixed capacitor value is decreased to 304 pF to drive the frequency up. In doing so, the capacitor is also changed from being a dual mimcap to a vertical capacitor in order to obtain the required low value. A comparison between the two capacitors is run in Figure 4.8:

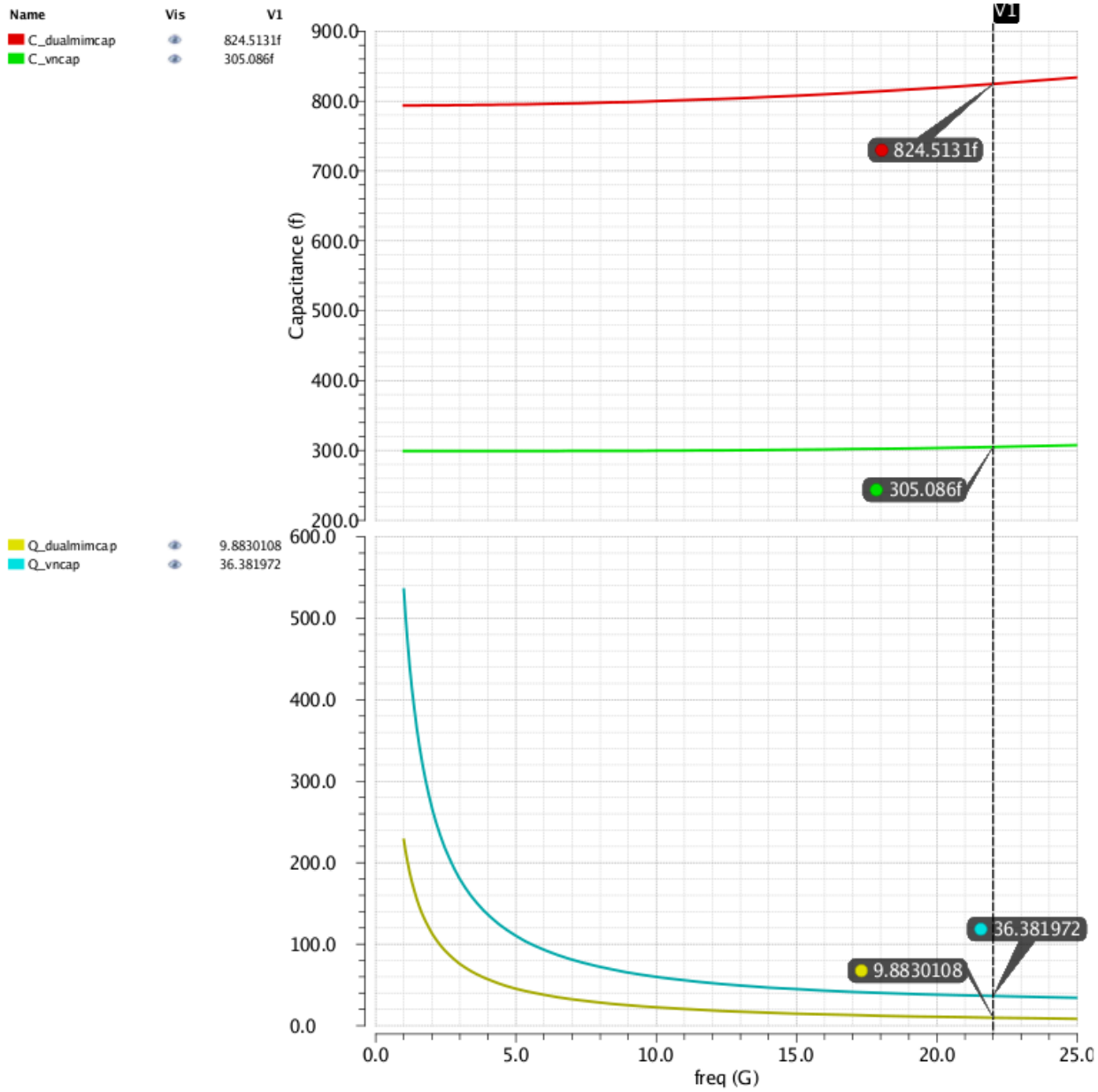


Figure 4.8 Comparing Dualmimcap and Vertical cap

As suggested above, the vertical capacitor can provide higher Q and thus decreasing the loss and phase noise of the circuit. Plugging the Q and capacitance values into (4.7) through (4.13) yields a new tank resistance of 243 Ω, a Q of 21.9 and a phase noise of -122 dBc/Hz (roughly a 6 dB improvement).

PSS analysis is performed again along with noise analysis to simulate the phase noise of the oscillator. Figure 4.9 shows the obtained results for all varactors switched off (maximum possible frequency):

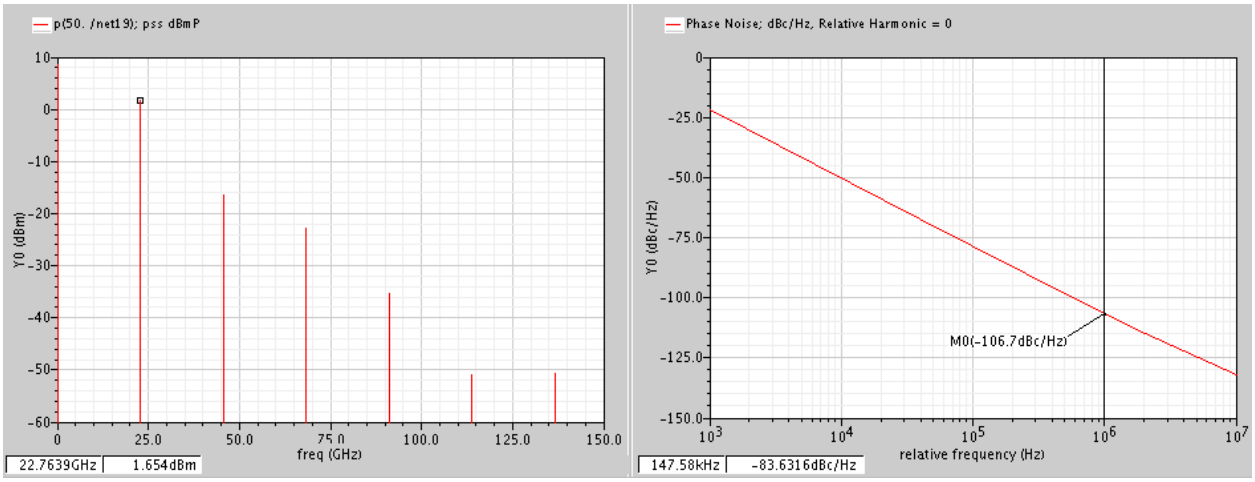


Figure 4.9: Obtained PSS and Noise Analysis Results

The frequency is now near the intended 22 GHz. The phase noise obtained is -106.7 dBc/Hz at 1 MHz offset. In order to determine the main sources of the noise, a noise summary is carried out to investigate the sources of the phase noise measured by the simulator. Figure 4.10 shows the results of the noise summary obtained:

Device	Param	Noise Contribution	% Of Total
/IO/T3	fn	1.808e-11	23.43
/IO/T9	fn	1.65855e-11	21.50
/IO/T0	fn	1.08774e-11	14.10
/IO/T1	fn	1.08598e-11	14.07
/IO/T14	fn	7.30299e-12	9.46
/IO/T4	fn	7.29599e-12	9.46
/IO/T8	fn	7.91781e-13	1.03
/IO/T0	id	6.71952e-13	0.87
/IO/T1	id	6.71787e-13	0.87
/IO/T3	id	6.43327e-13	0.83

Spot Noise Summary (in V^2/Hz) at 1M Hz Sorted By Noise Contributors
Total Summarized Noise = 7.71584e-11
No input referred noise available
The above noise summary info is for pnoise data

Figure 4.10: Noise Summary

As seen, the main sources of noise in the circuit are due to 1/f noise in the buffer transistors mainly followed by the cross coupled pair. Unfortunately this kind of noise is dependent on the process and is hard to limit or control. Moreover, the formula used in (4.13) does not take into account 1/f noise. T9 and T3 in the noise summary also refer to the current mirror transistors, whose noise performance is not taken into account and thus the extra 6 dB in noise given by simulation.

The varactors were then switched on one after the other to see the change in frequency. The graph below shows the obtained results.

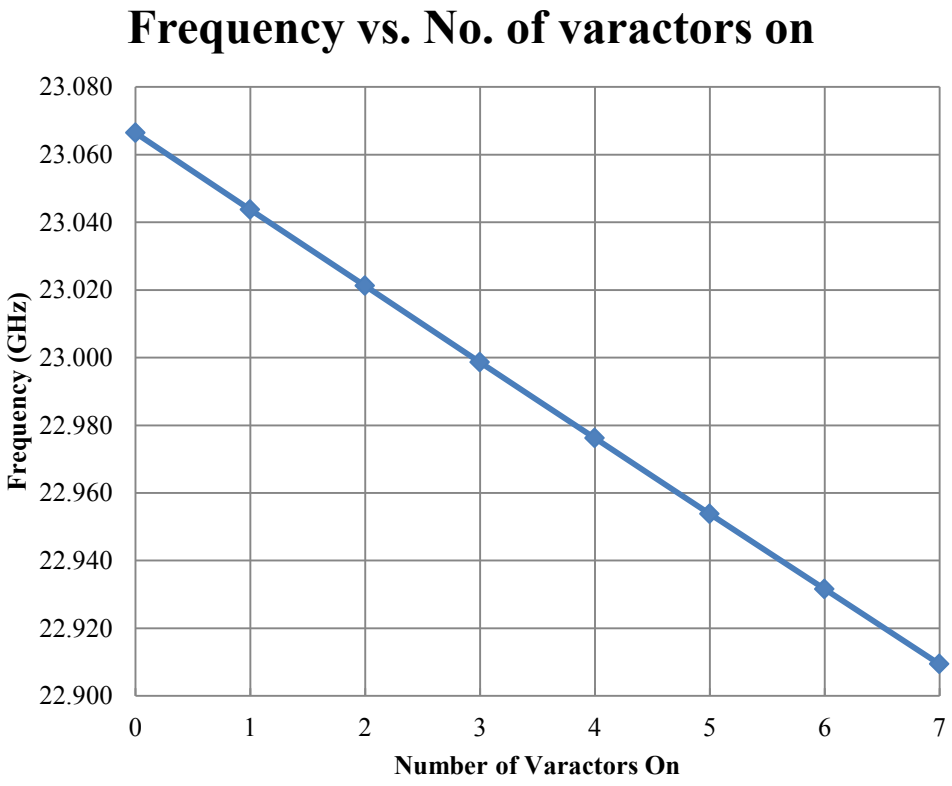


Figure 4.12: Simulated Frequency with Varactor Switching

The results show a fairly monotonic stepping of the frequency which is a good sign. As expected, the frequency decreases with increasing number of varactors turned on. This complies with what is shown in the varactor characterization plot (Figure 4.3) since turning on the varactor while using the gate topology increases the capacitance and hence drops the frequency. The frequency change is roughly 24 MHz between each step rather than the calculated 13 MHz. The main reason for this was the parasitic inductance added due to the interconnect. This extra inductance could only be compensated by decreasing the capacitance of the circuit since the RF line used for inductance was already at a minimum value. This decrease in total capacitance increased the $\Delta C/C$ fraction, hence resulting in a less fine resolution.

Seeing that the simulation results were satisfactory, the circuit was implemented in lay out. Figure 4.13 shows a picture of the laid out chip (measuring 1.332 mm x 0.750 mm).

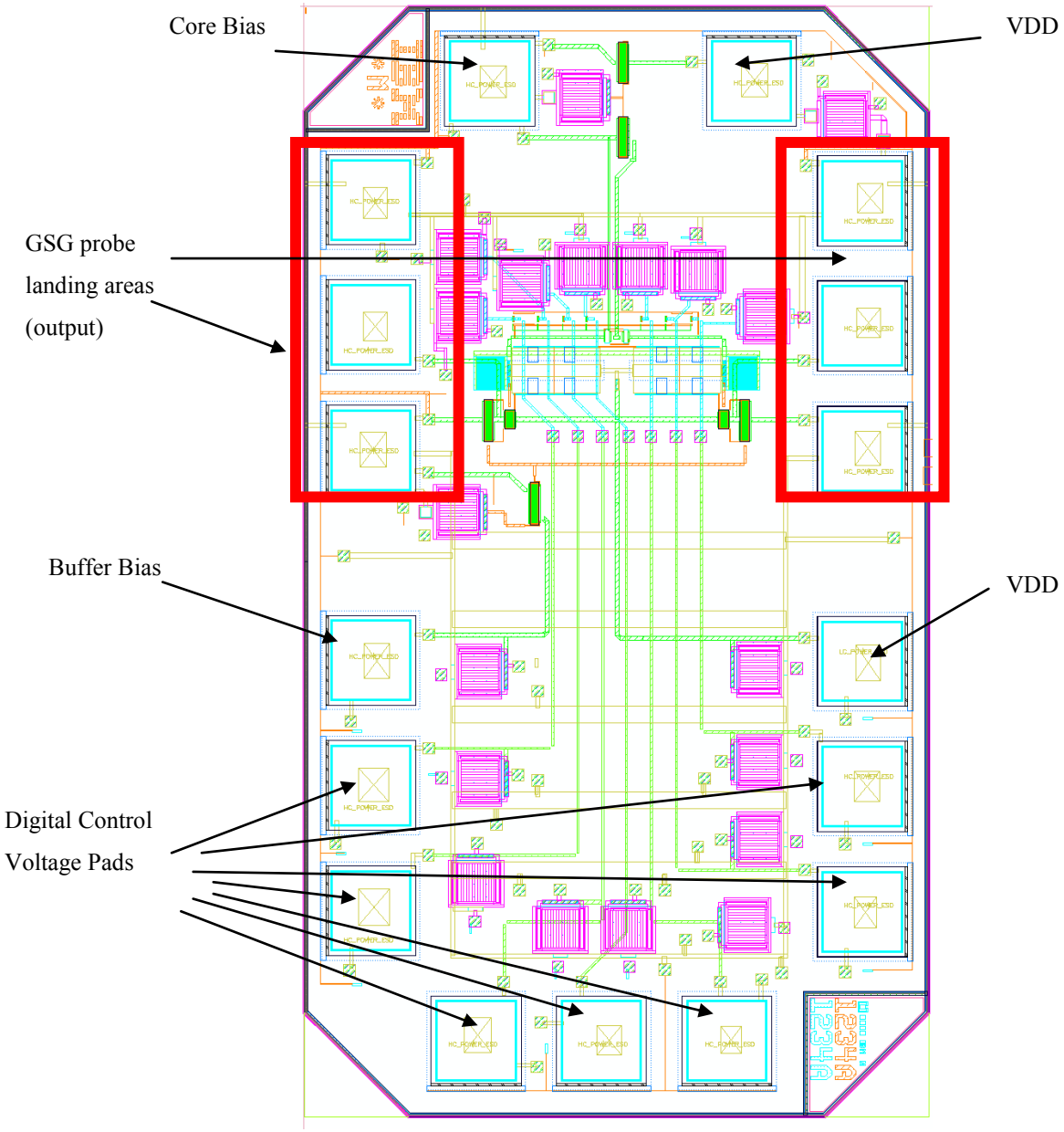


Figure 4.13: Chip Layout

In implementing the layout, care was taken to make sure there were no sharp (90 degree) turns since that can cause reflection loss due to radiation, especially at such a high frequency. Moreover, lines were kept to a minimum to avoid adding extra inductance, since the smallest extra length can be a source of significant inductance that can bring down the frequency greatly; an effect which is amplified at higher frequency. Moreover, since the circuit is differential, care was taken to make sure that the circuit was symmetrical at the core and from the core to the output

pads. The only unsymmetrical aspect perhaps would be the position of the noise decoupling capacitors at the varactor gates. However RF paths were kept as symmetrical as possible.

Figure 4.14 shows a zoomed in view at the core of the oscillator to show the components and symmetry.

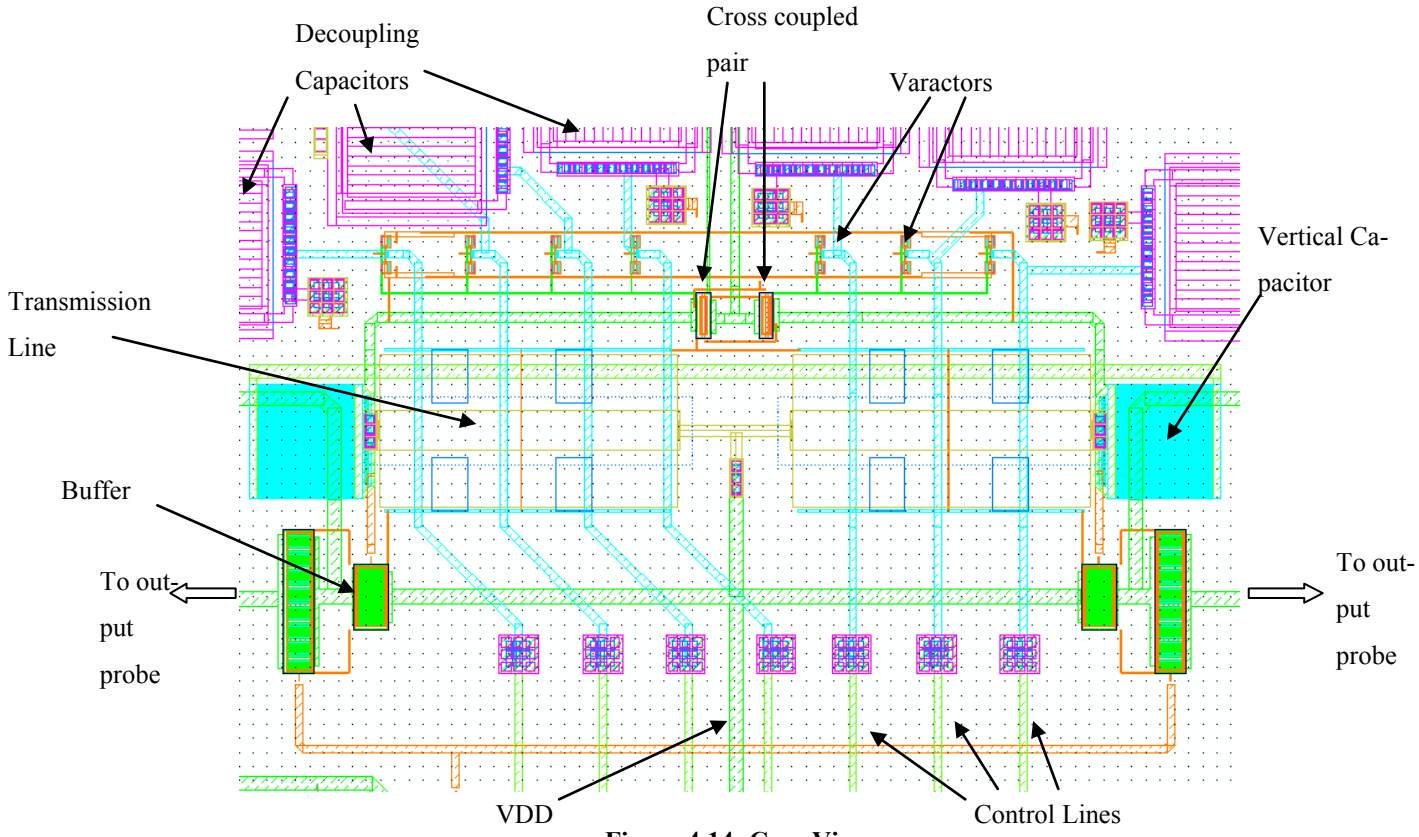


Figure 4.14: Core View

At all the power and control pads, large decoupling capacitors (10 pF) were added to ground the noise from the incoming DC signals. This acts as an on chip decoupling method to be used along with the microfarad capacitors added off chip near the pad. In addition, 10 pF capacitors were added at the gates of the varactors in order to decouple any possible noise signal that could have been generated as the control voltage signal passed through the long line connecting the pads to the varactors. This ensures that there is no noise signal that could modulate the control voltage on the gate causing an unstable varactor capacitance, adding to the variation in frequency and hence the phase noise.

In designing the layout, care was taken to design the layout stepwise in order to easily tackle the errors resulting from the design rule checks (DRC) and layout vs. schematic checks (LVS).

Once the whole chip was clear of any DRC and LVS errors, the design was extracted using RLC extraction to reflect the parasitic resistance, inductance and capacitance in the layout. This was followed by post-layout simulation. Figure 4.15 shows the obtained results for PSS and noise post layout simulation with all varactors switched off (maximum possible frequency).

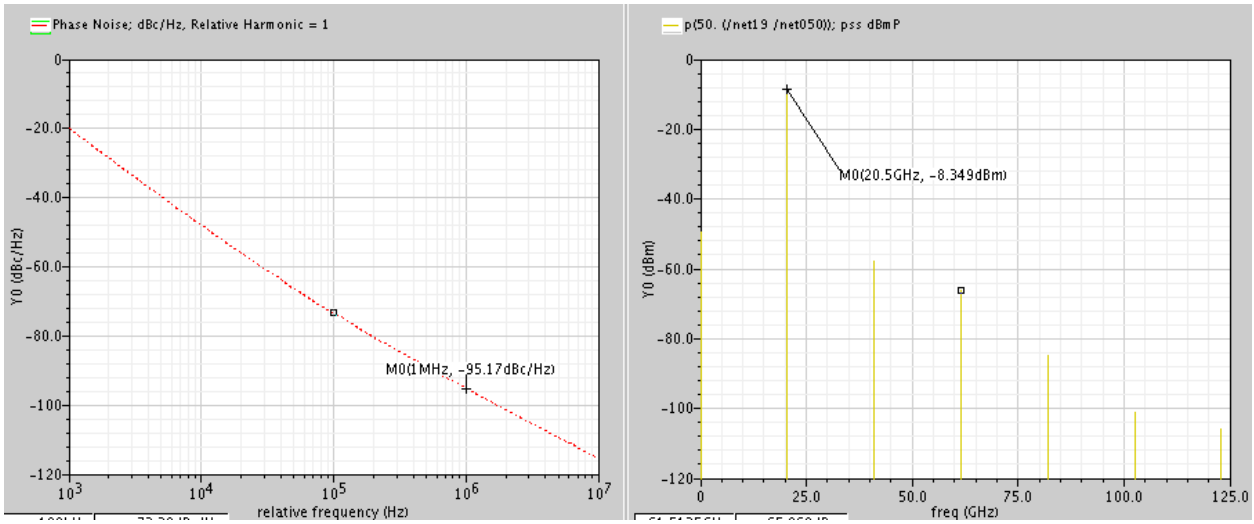


Figure 4.15: Post layout PSS and Noise Simulation Results

As seen in the results, the frequency of post layout simulation was just over 20 GHz which means the oscillator is working at the required band of 20 GHz. The output power has decreased significantly to about -8 dBm. This is expected since most of the losses have not been accounted for in the schematic view. These include resistive losses in addition to signal coupling to sub-strate and hence to ground. Moreover, the phase noise is about -95 dBc/Hz. This is slightly worse than the one obtained in schematic simulation. This is expected since adding all the connections to the devices brings in more sources of parasitic resistance which add more noise. A noise summary is performed to explore the sources of noise. Figure 4.16 shows the results:

Device	Param	Noise Contribution	% Of Total
/I24/T0	id	4.03305e-13	18.15
/I24/T1	id	3.19529e-13	14.38
/R0	rn	8.08267e-14	3.64
/I24/rh3033	rn	7.04631e-14	3.17
/I24/rj_1_1898	rn	6.71047e-14	3.02
/I24/T14	id	5.80954e-14	2.61
/I24/T15	id	5.61461e-14	2.53
/I24/rj_1_2058	rn	5.58227e-14	2.51
/I24/T14	fn	5.5104e-14	2.48
/I24/T8	fn	5.31803e-14	2.39

Spot Noise Summary (in V^2/Hz) at 1M Hz Sorted By Noise Contributors
Total Summarized Noise = 2.22257e-12
No input referred noise available
The above noise summary info is for pnoise data

Figure 4.16: Post Layout Simulation Noise Summary

The major source of noise is now thermal noise in the core transistors due to channel resistance. This can be reduced by decreasing the bias current in the transistors or by

The number of varactors switched on was then swept to see the frequency resolution of the oscillator. The results are shown below in Figure 4.17:

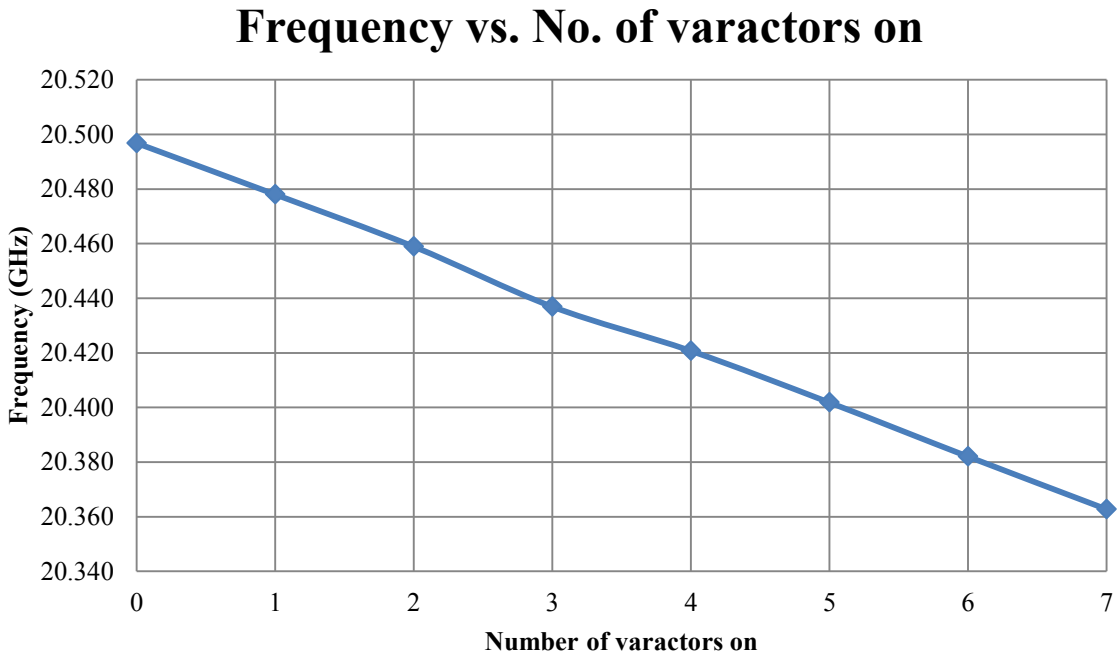


Figure 4.17: Post Layout Simulation Of Resolution

The frequency resolution showed by the simulation has an average of about 19 MHz, which is better than the schematic simulation results. One possible reason for this is the addition of the parasitic capacitances which increase overall capacitance, and thus make the switching of a 6 fF seem less significant in the layout than in the schematic; hence causing a smaller change in frequency and so improving the resolution.

4.1.3 Testing

Since the post layout simulations (including R,L and C parasitics) proved that the circuit works, the design was sent out for fabrication. A low frequency PCB was needed to manage the low frequency power and control signals to the chip. A 1 layer board was designed and sent out for fabrication. Figure 4.18 shows a diagram of the designed PCB.

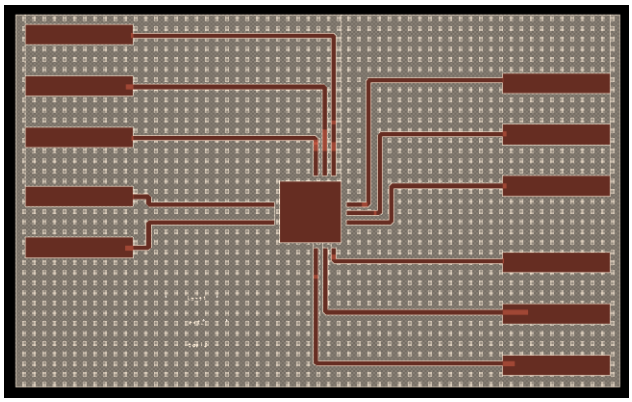


Figure 4.18: PCB for Testing Chip

The board is a single conductor layer board that provides surface mount spots for female headers to be soldered on and a central square to fix the die on. The bond pads on the chip would then be connected to the trails leading to the headers by means of wirebonding. Finally, wires connected to the female headers would lead to the breadboard where the power is managed and varactor switches are toggled. Wirebonding and soldering the headers had to be done very carefully with a grounding wrist band as the smallest build up of charge can burn the chip. Figure 4.19 shows the board with the chip and the headers where the power and control signals are connected.

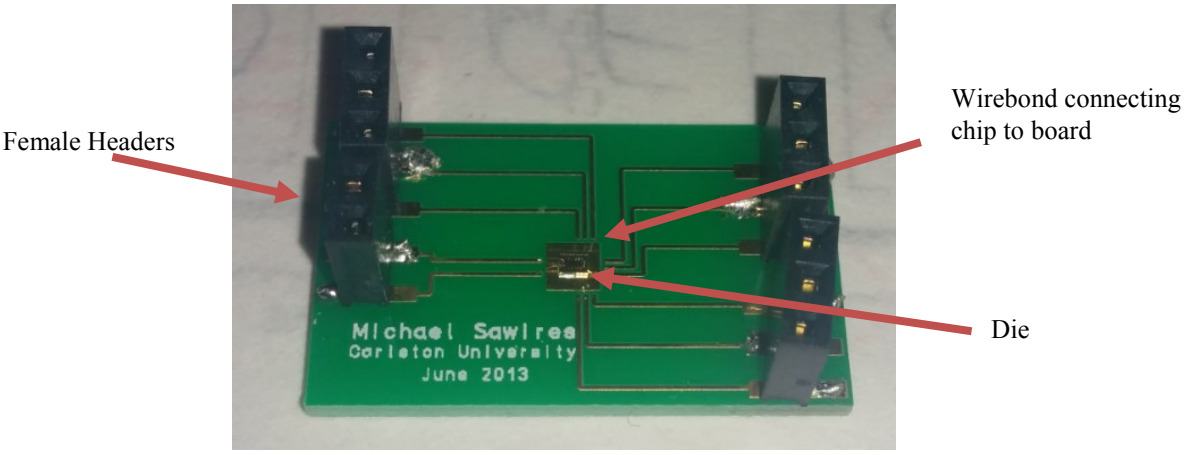
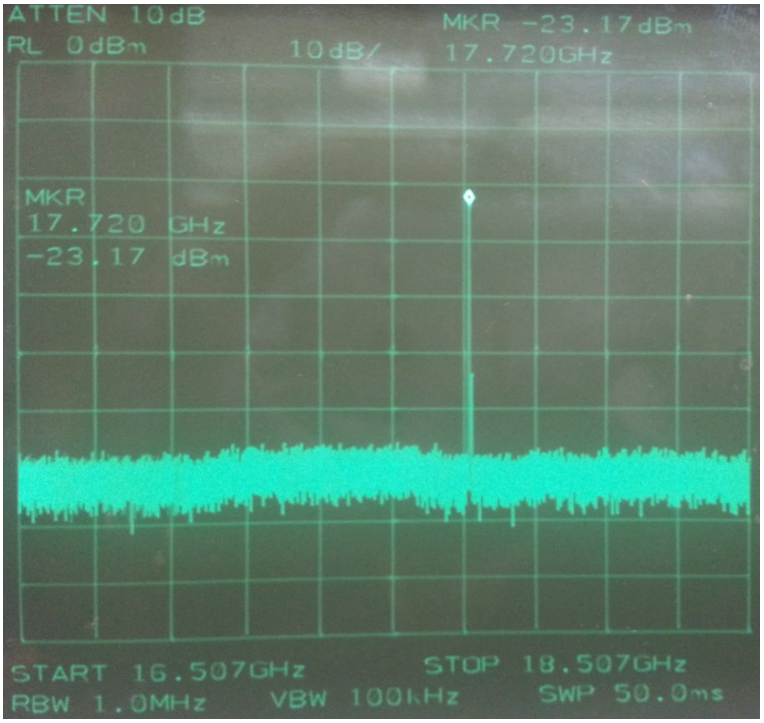


Figure 4.19: Chip, Board and Headers

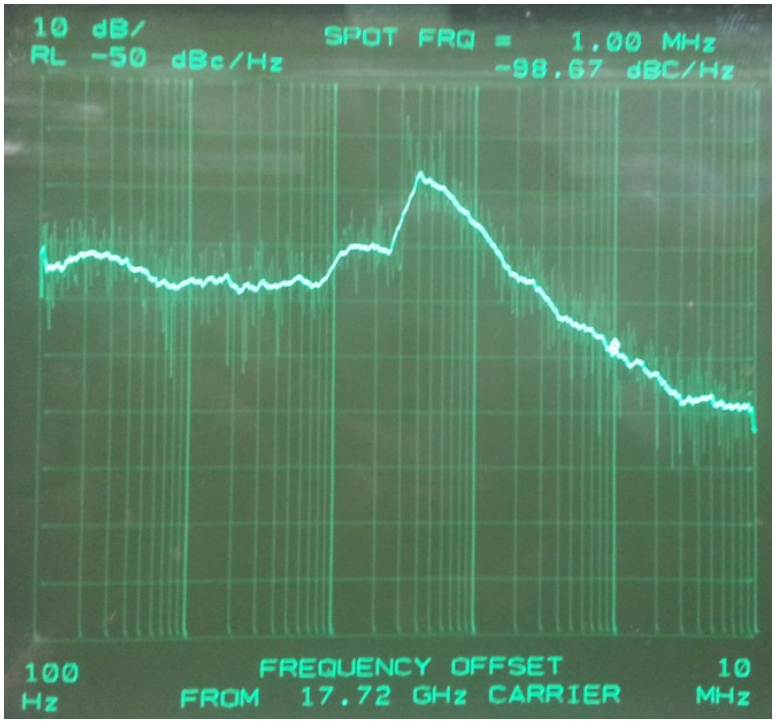
In biasing the circuit, care had to be taken not to burn the chip in case one of the connections was shorted. As a result a power supply with a current limit was used. The current flowing in the schematic is equal to 8 mA x 2 (from the core biasing) + 6 mA x 3 (from the buffer biasing). This results in 34 mA of power being used. Therefore, the current limiter is set at 40 mA. In order to achieve the desired current from the current source, a variable resistor is connected to the rail supply and the voltage across a 100 Ω resistor in series is measured to figure out the current. These two resistors are connected to the pads for I_{bias} and I_{buffer}. The resistor was tuned until the current in the test resistor reached the required value. The circuit draws 31.8 mA, which is close to what is expected. The slight offset is due to current not being mirrored perfectly in the current mirror.

After figuring out bias, the board is fixed to the probing chuck with the means of a vacuum pump. Two GSG probes are landed in the areas described in Figure 4.13 above (both outputs of the differential oscillator). Great care was taken while handling and landing the probes as they are easy to break. Moreover, the RF coax cable used to measure the oscillator output was characterized to have about 13 dB of loss at 20 GHz.

Finally, the output of one probe was connected to a spectrum analyzer while the other was connected to a 50 Ω termination. Figure 4.20 shows screenshots obtained from the spectrum analyzer for measuring the single ended output of the oscillator.



(a)



(b)

Figure 4.20: Spectrum Analyzer Results for All Varactors Switched Off – (a): Frequency Spectrum, (b): Phase Noise Measurement

As seen in Figure 4.20, the oscillator chip has an output of 17.720 GHz with a power of about -10 dBm (-23 dBm + 13 dB of cable attenuation). However in order to compare this to the simulated results, extracted view simulation is repeated using single ended measurement. Figure 4.21 shows the simulated single ended results for the extracted view and with all varactors turned off:

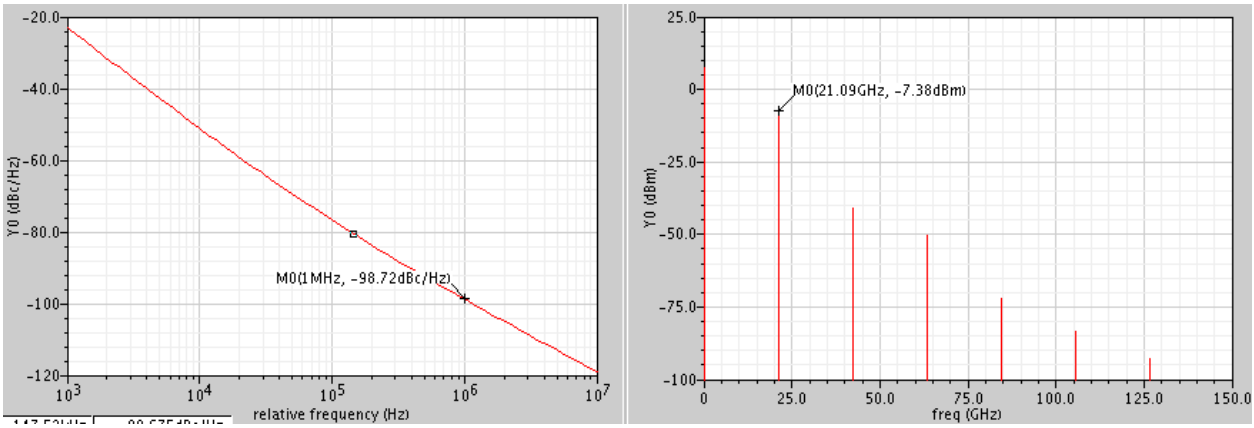


Figure 4.21: Single Ended Simulation for Extracted View, All Varactors Off

As seen, there is not much difference in performance between single ended and differential. Moreover, the frequency stepping with switching varactors is more or less the same (graph not shown).

Compared to the simulated results, the obtained measured results are about 2.4 dB lower in power and with a phase noise that is more or less the same. A possible reason for this is unlike in simulation, there is no failsafe way to guarantee that the current flowing in each transistor is the designed 4 mA. This causes the g_m of the transistor to drop slightly and hence the weaker output. Of course this can be easily fixed by slightly increasing the current from the current source biasing the core in the chip. The oscillation frequency is also roughly 3 GHz lower possibly due to EM characteristics of the resonator that was not accounted for by simple RLC extraction. Moreover it must be remembered that such high frequency is pushing the limits of the technology to the limits of obtaining reliable output.

However, the main concern is the frequency resolution. Figure 4.22 shows the stepping of frequency by switching on varactors (voltage on varactor gates changed from -0.5 V to 1 V).

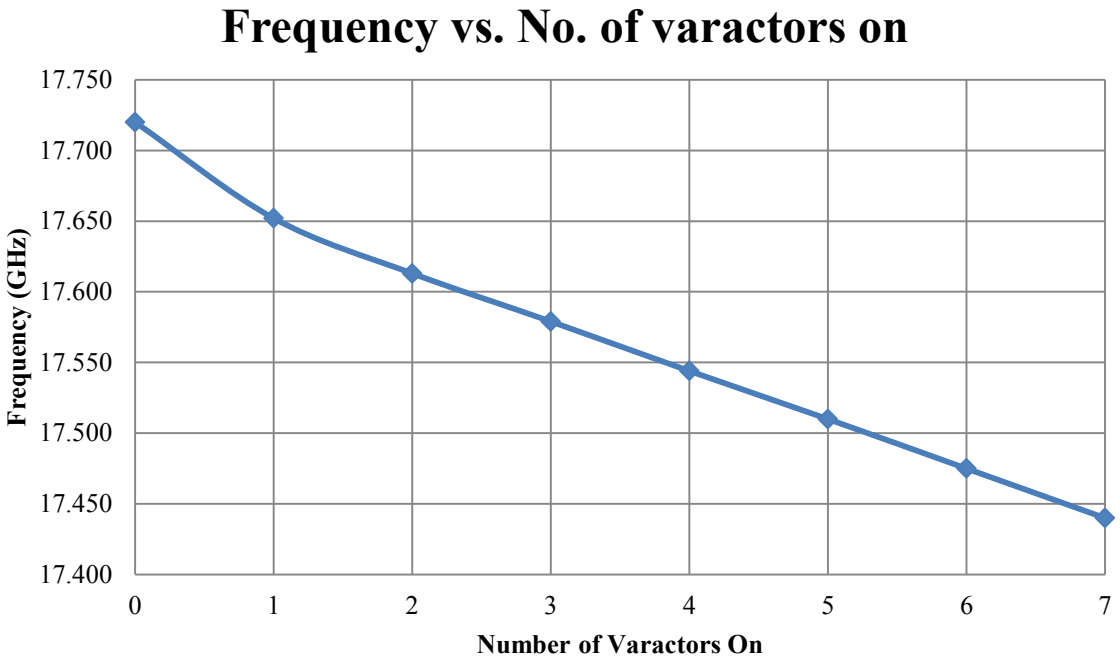


Figure 4.22: Measured Frequency Resolution of First Chip

The resolution of the oscillator chip is about 30 MHz. This is about one and half times the extracted resolution of 19 MHz. A possible explanation for this is the fact that the since output is a few dBs lower than that simulated in extraction view, the swing on the oscillator core is smaller. This means that the swing simulated on the varactors is also smaller than 0.5 V. Since the capacitance of the varactors depends on the bias, if the bias does swing as low as projected, the varactor is expected to achieve a higher capacitance change. This is reflected by a higher change in frequency in oscillations.

This method managed to achieve a few tens of megahertz of resolution. The results suggest that the limit of using the smallest possible kit varactor cannot achieve much better resolution. This is mainly due to the limit of how small of a capacitance is switchable in the smallest kit varactor available. In order to achieve kilohertz of resolution, another technique needs to be investigated.

4.2 Small Series Capacitor

As seen above, the previous method described can only achieve tens of megahertz of resolution. The oscillator required for the ADPLL application requires kilohertz resolution and so a new approach to achieving high resolution is needed. The last paper covered in Chapter 3 discusses adding a series capacitor to the varactor in the tank circuit. This decreases the effective change in capacitance during varactor switching and hence increases the resolution of the oscillator. In this section this method will be investigated to see whether better resolution can be achieved.

4.2.1 Design

A small capacitor connected in series to a much larger one will result in the smaller capacitor being much more dominant in terms of equivalent capacitance. This can be exploited by making the small capacitor fixed while varying the bigger capacitor for a reduced effect of capacitance change. For example a varactor switching between 700 fF and 1.3 pF put in series with a 2 fF vertical cap will have the following equivalent capacitance:

At maximum capacitance:

$$C_{max} = \frac{1}{\frac{1}{C_{cap}} + \frac{1}{C_{var,max}}} = \frac{1}{\frac{1}{2\text{ fF}} + \frac{1}{1.3\text{ pF}}} = 1.99693\text{ fF} \tag{4.14}$$

Similarly, at minimum capacitance:

$$C_{min} = \frac{1}{\frac{1}{C_{cap}} + \frac{1}{C_{var,min}}} = \frac{1}{\frac{1}{2\text{ fF}} + \frac{1}{700\text{ fF}}} = 1.99430\text{ fF} \tag{4.15}$$

This gives a capacitance resolution of roughly 2.63 aF, which is a significantly smaller number than the one obtained by the previous method. In order to approximate that in frequency terms, (assuming same bias conditions, total inductance and a capacitance of 935 fF), the new capacitance figures can be replaced in (4.3):

$$\frac{f_{min}}{f_{max}} = \sqrt{\left(\frac{C_{min}}{C_{max}}\right)} \tag{4.3}$$

Solving this yields:

$$f_{min} = \sqrt{\left(\frac{C_{min}}{C_{max}}\right)} \cdot f_{max} = \sqrt{\left(\frac{935\ \text{fF}}{935\ \text{fF} + 2.63\ \text{aF}}\right)} \cdot 20\ \text{GHz}$$
$$f_{min} = 19.99997187\ \text{GHz} \quad \textbf{(4.16)}$$

Thus the new resolution is theoretically about 28 kHz, which is significantly better than the one suggested by the first method discussed. Thus with fine tuning, and taking into account the extra capacitances added by the transistor and fringe capacitance of the varactor and transmission lines, this can be tuned to about 25 kHz.

$$\Delta C = 28\ \text{kHz}$$

4.2.2 Implementation and Simulation

In order to achieve a 10% tuning range (1 GHz), the frequency had to be controlled starting from small kHz steps all the way to hundreds of megahertz. In order to achieve this, stepping for 5 kHz, 25 kHz, 100 kHz, 1 MHz, 10 MHz and 100 MHz was designed based on the same method discussed of connecting a small fixed capacitor in series with a varactor. In the 100 MHz stepping however, simple varactors with no series capacitors were used since the frequency change is large enough at this point and adding a smaller capacitor in series would take up unnecessary space.

Figure 4.23 shows the structure of a typical row in the varactor-capacitor bank.

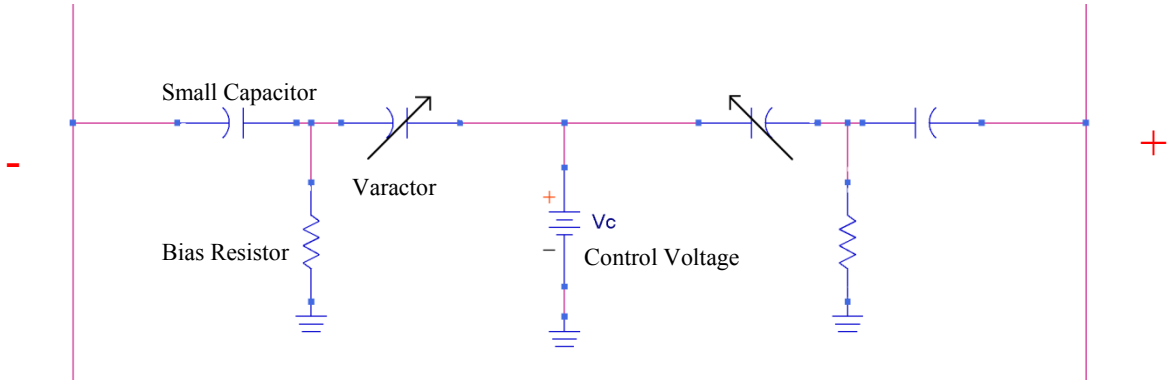


Figure 4.23: Varactor Row Design

A bias resistor is required to set the varactor substrate voltage to zero. This is necessary since all characterization on the varactor is done with a set substrate voltage (zero in this case). In order to implement that, a 1 kΩ resistor is connected between the capacitor-varactor net and ground. The resistor is necessary because it would prevent the RF signal from being grounded at the capacitor-varactor net.

With 5 rows of 5 kHz resolution varactors, 3 rows of 25 kHz, 9 rows of 100 kHz, 1 MHz, 10 MHz and 100 MHz each, there was a total of 44 varactor rows requiring a control voltage. In order to control all these rows it would be impractical to assign a pad for each of those control voltages as was done in section 4.1. Therefore it was necessary to devise a new method to deliver the control voltages to the varactor rows.

Figure 4.24 shows the method used to transmit the bias bits to the varactors. In this design, a shift register was used to shift a bit sequence from an input pad from row #1 all the way to row #44. In addition, a latch was connected at the output of every shift register flip flop to prevent the bit being transferred from directly biasing the control voltage at the varactor. Thus, once all 44 bits have been read, the latch would receive an enable signal allowing it to be transparent and therefore transmitting the bits to the varactor gates. In digital terms, this acts as a "READ" signal to make sure the varactors are biased only when the bits are in place.

The fact that the control voltages are of digital nature (either fully switched off at -0.5 V or fully switched on at 1 V) meant that an inverter biased at V_{DD} = 1 V and V_{SS} = -0.5 V could be used to deliver the control voltages.

Note that noise from the digital circuit was insignificant due to two reasons. Firstly, the circuit is set to by very slow compared to the 20 GHz oscillator. That means clock noise would not be a significant factor. Secondly the bias voltage reaching the varactor reaches the circuit at a virtual ground point, meaning that there it will ideally have no effect on the circuit in RF terms. Moreover, a noise decoupling capacitor is installed on each varactor gate to make sure that in case noise is present, it would be filtered out by the large capacitor at the gate.

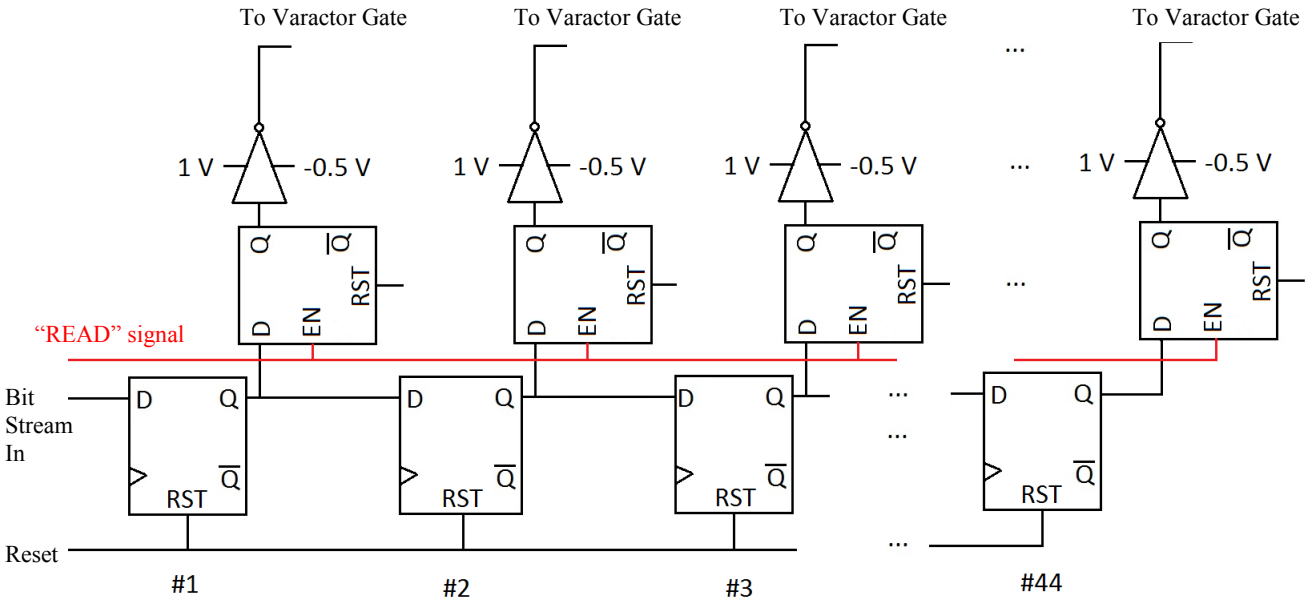


Figure 4.24: Shift Register to Bias Varactors

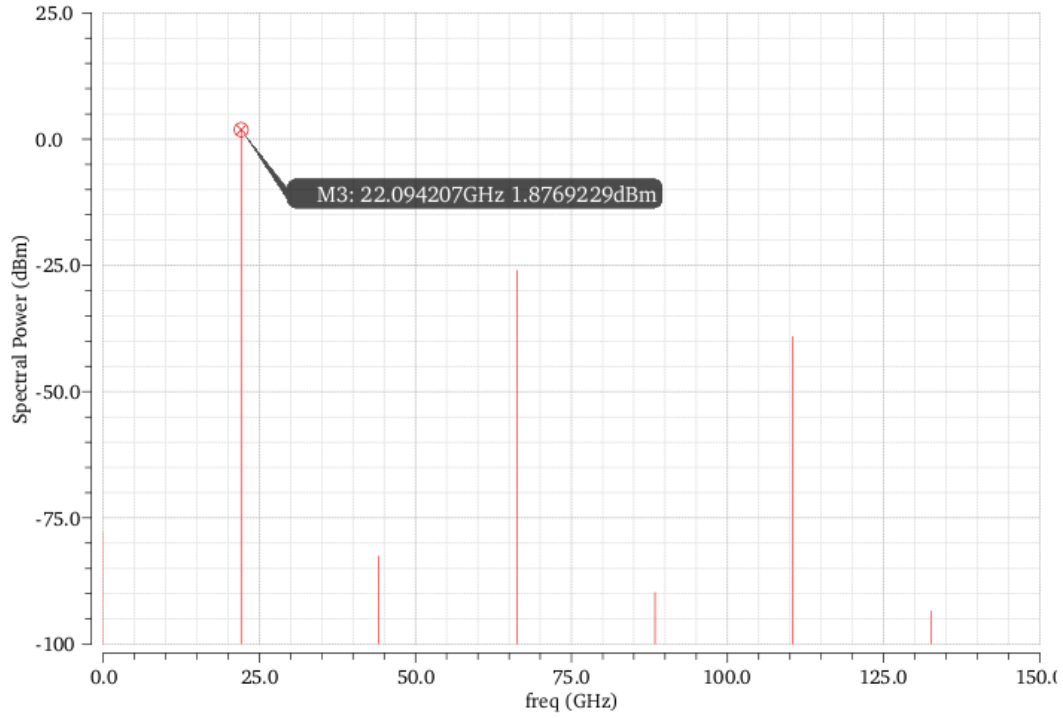
This arrangement would require six extra pads for the digital transmission of varactor biases – a pad for the read signal, reset, bit stream in, inverter V_{DD} and V_{SS}, and a bit stream out. The bit stream out is only for validation purposes; to make sure that the bits have been transmitted correctly throughout the shift register by reading them out again.

Simulating the whole oscillator with different bias bit combinations would be quite difficult since it would require waiting until the bits have propagated through, enabling the read signal and then running a PSS analysis. As a result the design and simulation of the different varactor rows was done without the shift register in a manner similar to that demonstrated above in (4.15). Different varactors with small capacitors were characterized, implemented and tuned to achieve the required frequency change. Similarly, the shift register/latch/inverter circuit was tested using a time domain simulation to make sure it functioned as expected. After both subcircuits were confirmed working, simulation was done using a default 44 zero bit combination (achieved by triggering "reset").

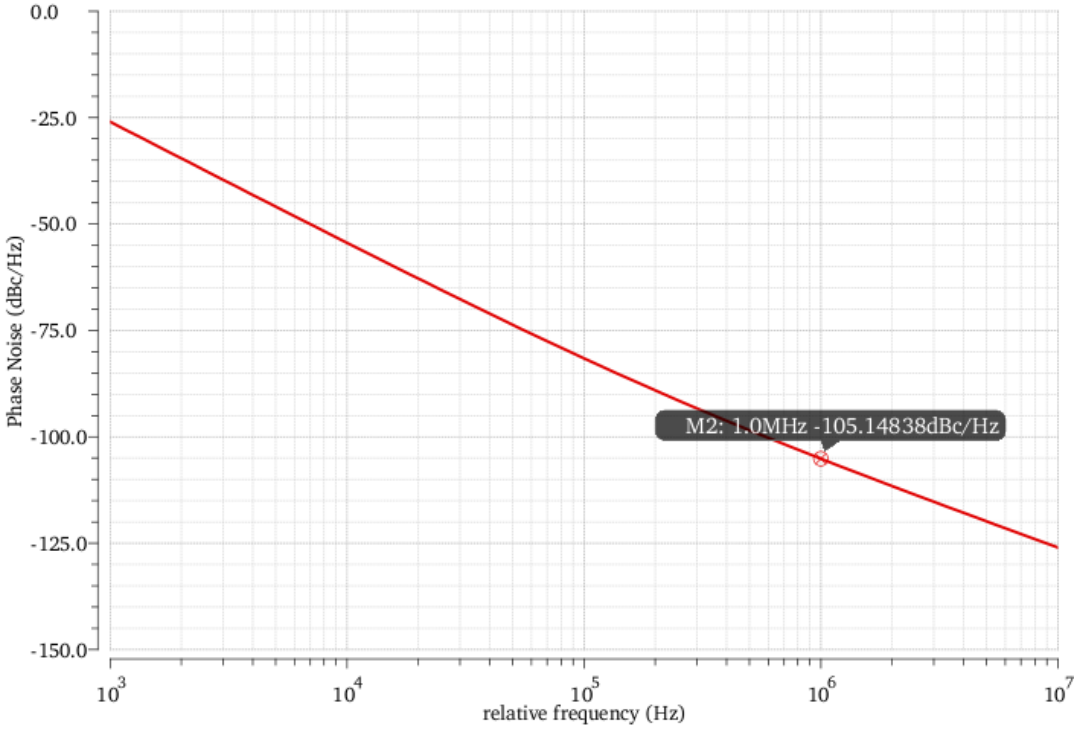
In order to be able to distinguish kilohertz difference in frequency in a gigahertz oscillator, the simulator tolerances had to be changed to be much stricter than default. The parameter "reltol" was reduced to "5e-6" instead of the default value of "1e-3". Similarly, "vabstol" (which is the error tolerance for the steady state voltage) was reduced to "3e-11" from an initial "1e-6". It should be noted that this increased the simulation time significantly, though yielding results.

However before convergence could be achieved, the “tstab” parameter in PSS analysis had to be increased to 50 ns instead of the default 20 ns used in the previous design. This is necessary since before 50 ns, there was still some small transient change from the start of the oscillator and so convergence was impossible, especially at such tightened conditions for the simulator. Each high accuracy simulation lasted roughly 4 hours. The step in resolution was close to the expected 5 kHz

Figure 4.25 shows the periodic steady state results obtained for the schematic view:



(a)



(b)

Figure 4.25: Schematic PSS Analysis Results for Second Design – All Varactors Off/Maximum Frequency – (a): Spectral Power, (b): Phase Noise

This oscillator has a tuning range from 21 to 22 GHz in the hope that post fabrication the frequency tuning would be in the 20 GHz range. It is also producing about 1 dBm of power which is an improvement from the -6 dBm from the previous design. The phase noise however is about the same as that of the first design.

The chip was then laid out as follows (Figure 4.26).

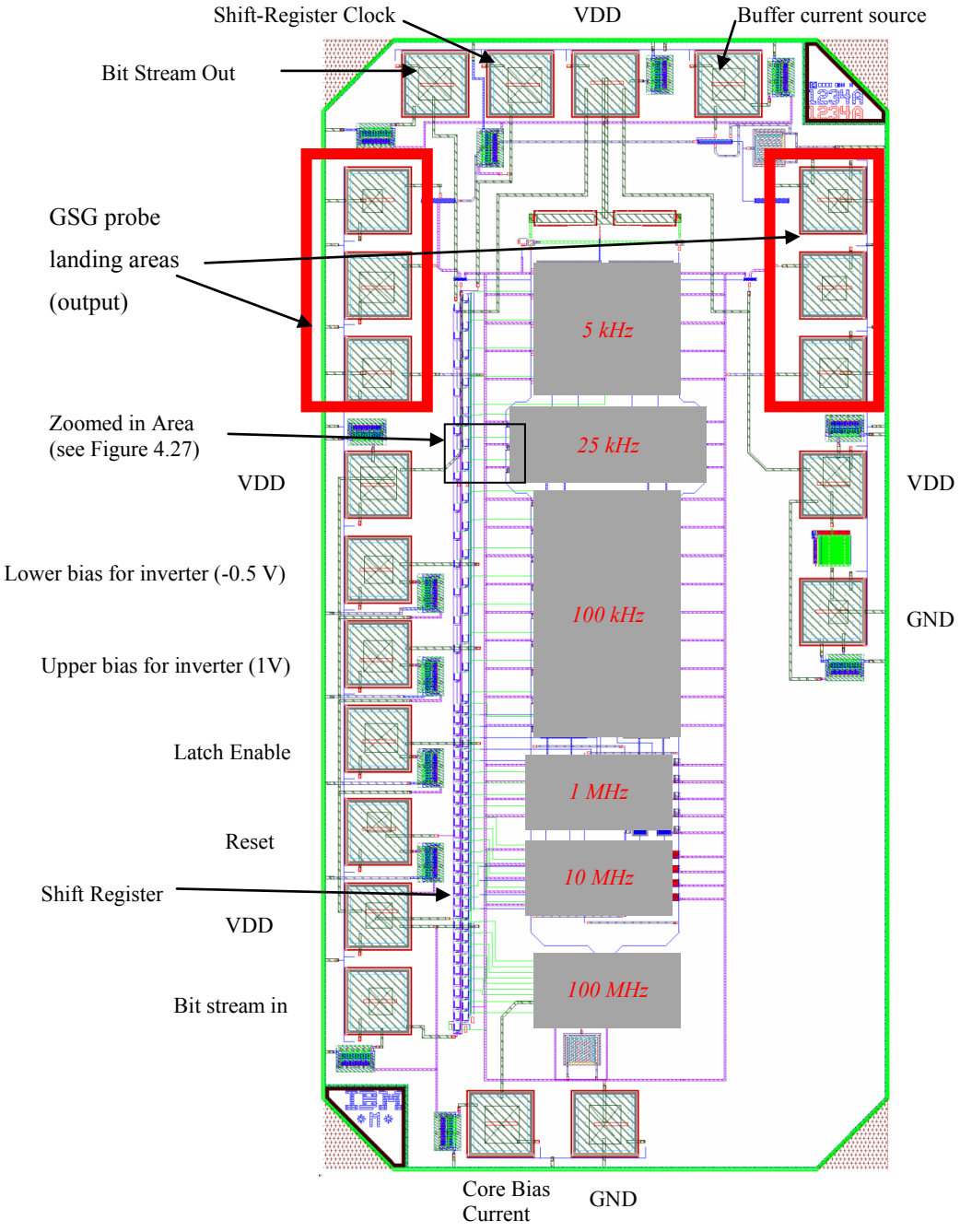


Figure 4.26: Second Design Layout – Measuring 2.00 mm x 1.00 mm

In connecting the different varactors together, lower metal layers (M1 & M2) were used rather than the conventional routing layers such as MA. This is because as explained in the first design, the method used employs using the least possible inductance, and so any additional inductance (which is present more in higher metal layers) will throw off the frequency. However in lower layers, the parasitic capacitance through the substrate to ground is increased, and the series resistance of lower level metal is much higher. Due to the high sensitivity to parasitic inductance in this design, it was felt that parasitic capacitance would be preferred over parasitic inductance. However, it was discovered later that the negatives far outweighed the positives for such an approach

Figure 4.27 shows a zoomed in view over the digital structure along with a varactor row.

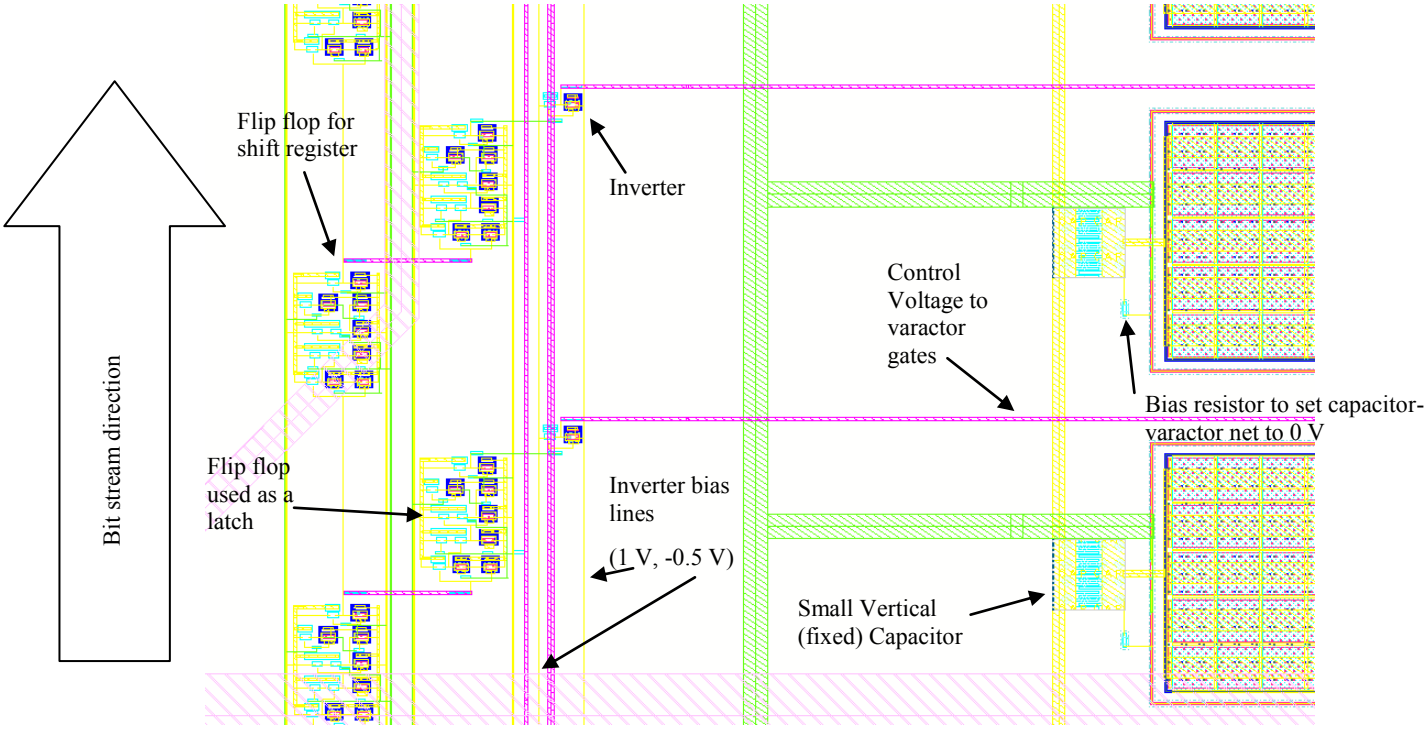


Figure 4.27: Control Voltage Transmission

The layout was made sure to match the schematic using LVS checks and was also ensured to have no design rule errors according to technology rules. It was then extracted to include parasitics. Simulation was then run again. Unfortunately oscillation never occurred. In order to investigate, a parasitics analysis is launched on the extracted view to find possible reasons why the oscillator did not start up. Each side of the oscillator reported about 1 nH of parasitic inductance. For a targeted 60 pH this is almost 20 times more inductance. By referring to Figure 4.26, it can

also be seen that the connecting lines connecting the transmission lines at the top and the oscillator core at the bottom are roughly 1.5 mm long (knowing that the layout is roughly 2 mm). As a result, it makes sense that they would have such high inductance. This inductance was not reflected in the schematic and so the oscillator oscillated normally. Moreover, the very high number of varactor rows loaded the tank circuit and brought down the Q. Combined with the effect of the parasitic capacitance by the lines connecting the components in addition to other parasitic inductances, this oscillator did not work.

Methods were implemented to try to reduce the damage from the very high loading of the varactors and the nanohenry inductance added but to no avail. Varactors were taken out and the lines were widened to reduce the inductance but the oscillator still did not work. In principle the idea seemed to work in schematic level but failed once implemented due to a lot of parasitic components. Therefore major changes were needed. However, the experience gained from the two designs done was fundamental in helping designing the final oscillator circuit explained in section 4.3.

4.3 The Simplified "Small Capacitor" Approach – Final Design

Even though both designs until now have not reached satisfactory performance, there was a lot to learn in the quest to achieve superior frequency resolution. Connecting lines should be as small as possible and the amount of capacitance change achievable from the smallest varactor is too large to achieve the required resolution. Therefore in this design, the concept of using a small fixed capacitor in series with a varactor is expanded on while maintaining the use of a much smaller number of varactors.

4.3.1 Design

This design will use the same principle used in the second design to achieve resolution. That is connecting a small capacitor in series with a varactor to achieve the high resolution required. However, except for the smallest frequency step, coarse frequency tuning was implemented by continuous varactor bias. That is the varactors can be biased using any voltage ranging from -0.5 V to 1 V. Even though this is not a strictly digitally controlled oscillator for those frequencies, it could be argued that this analog frequency control can be converted to a digital one simply by adding a DAC for the coarse tuning. That way, from the outside a frequency control word can be

sent to the oscillator-DAC system where the DAC converts the bits into a set of control voltages for the analog varactors. However, the frequency stepping responsible for the frequency resolution (fine tuning) was left in its previous state.

4.3.2 Implementation and Simulation

Figure 4.28 shows the schematic of the varactor arrangement used:

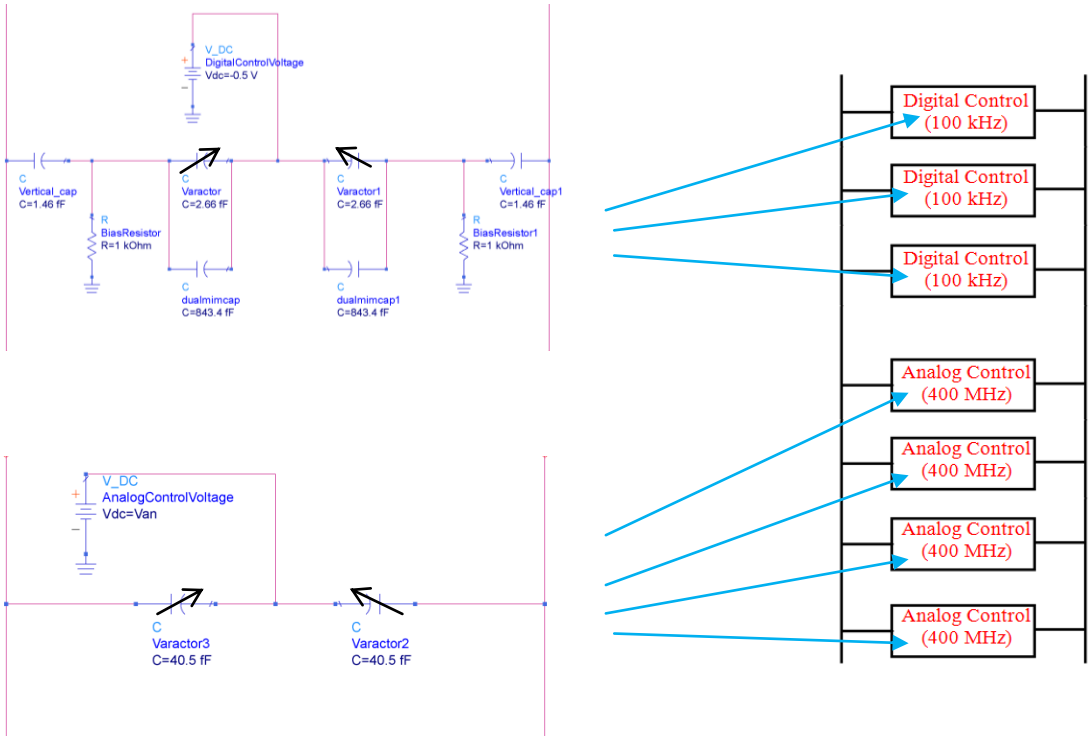


Figure 4.28: Final DCO Circuit

The oscillator core and buffer transistors were kept at the same size. Current however was increased to 5 mA to account for the lower Q of the resonator. The resolution was set at 100 kHz rather than 5 kHz since the varactors for them require significantly less space to build, which in turn requires less length of interconnect and hence less inductance. In principle however if it could work for 100 kHz, further research can be done later to try to reduce the physical size of the required capacitors. In this design, a large mimcap capacitor is also connected in parallel with the varactor. This has two effects. The first is by adding fixed capacitance in parallel with the varactor, the overall change in capacitance of the varactor-mimcap combination becomes less apparent. This results in a smaller change in total capacitance from the row, resulting in a finer resolution. Moreover, it prevents having to use a very large varactor to achieve the desired

change in capacitance. Using larger varactors leads to having a lower overall parallel resistance, resulting in less gain and voltage swing.

The transmission lines in this circuit were not kept at minimum size. In fact, the inductance was chosen to be about 200 pH so that after extraction, there would be space for adjustment and reducing of inductance to account for the parasitic inductance of the connecting lines. The lines were again kept at lower metal levels for a somewhat lower parasitic inductance (but unfortunately with a much higher parasitic capacitance).

5 mA were chosen for each of the core transistors and the buffer bias was also set at 5 mA. These numbers are slightly over the minimum number (as explained in the first design), providing just a little bit of extra current to improve phase noise performance and compensate for the lower tank resistance.

After schematic simulations proved to have the required resolution (100 kHz) at 20 GHz, The chip was laid out and parasitic extraction was performed. As expected, there was about 100 pH of parasitic inductance on each side of the oscillator which brought down the frequency to about 13 GHz. Therefore, the inductance of the used transmission line was cut down to account for the extra parasitic inductance of the interconnect. The final chip layout is shown below in Figure 4.29.

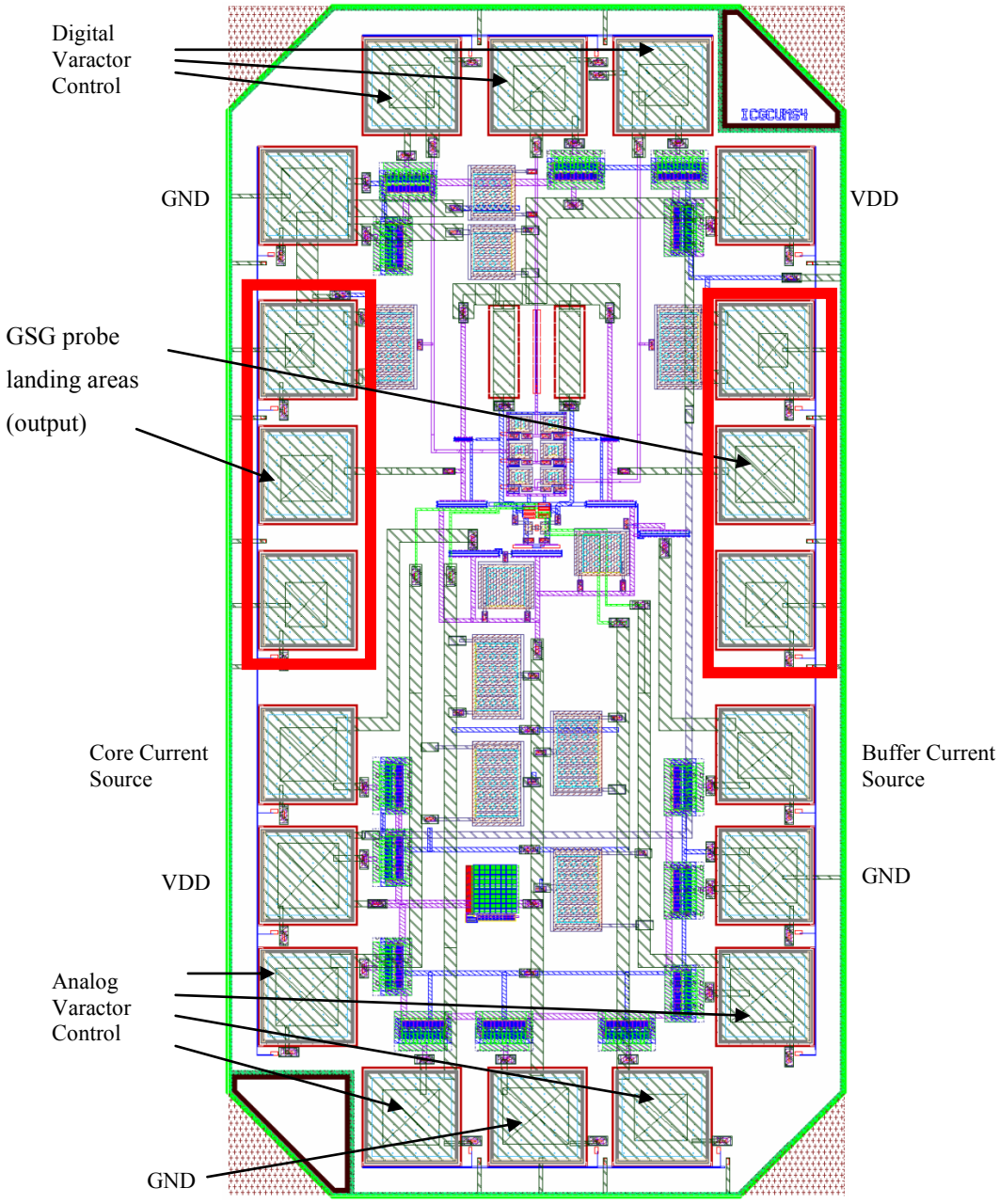


Figure 4.29: Final DCO Chip Layout, Measuring 1.426 mm x 0.737 mm

Figure 4.30 shows a zoomed in view on the core of the DCO to see the components involved.

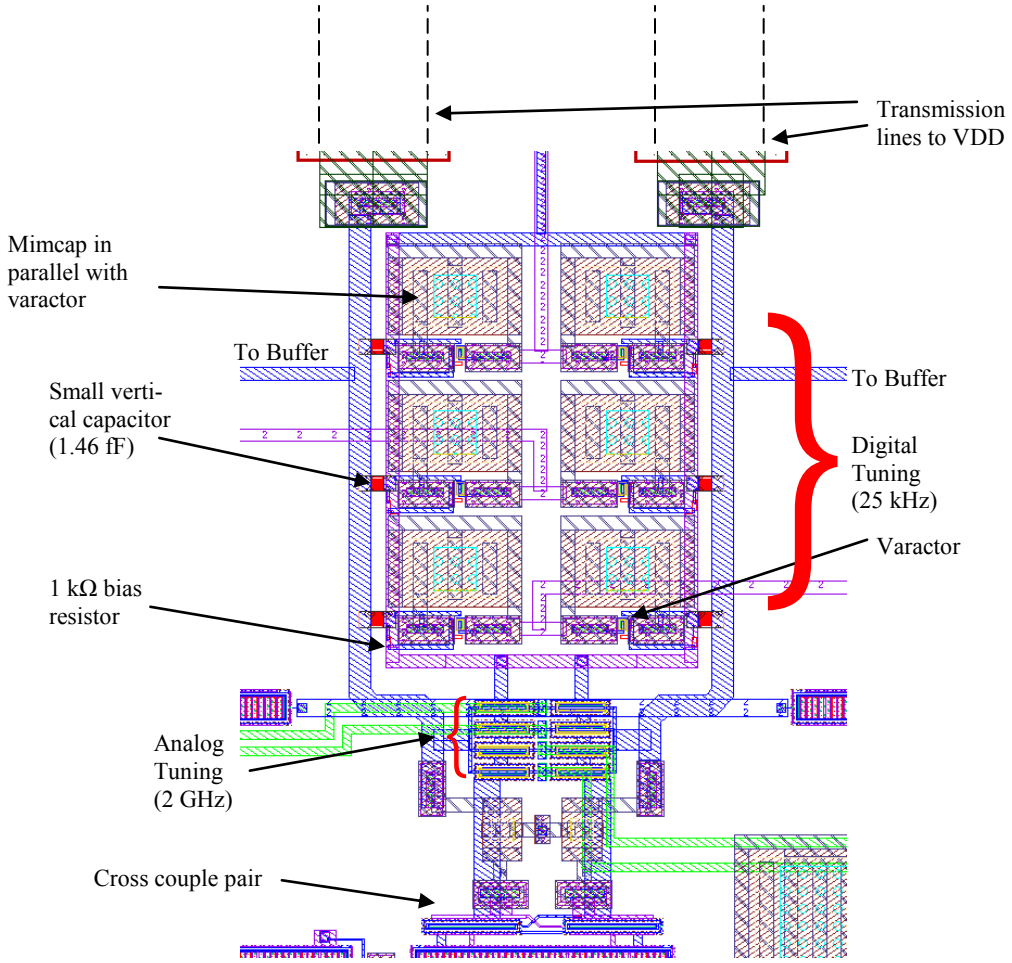
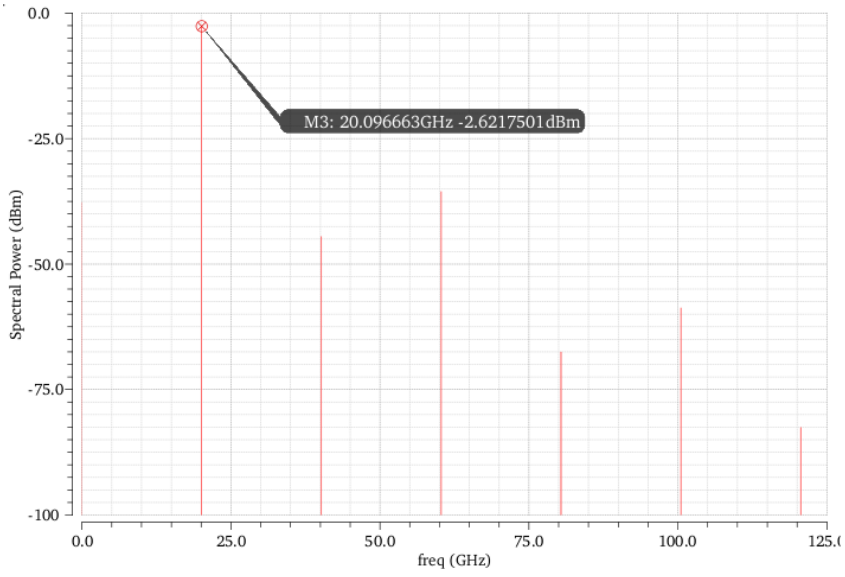


Figure 4.30: Final DCO Core Layout

Figure 4.31 shows the results of the periodic steady state and noise analysis performed on the extracted view of this layout with all varactors switched off for maximum frequency.



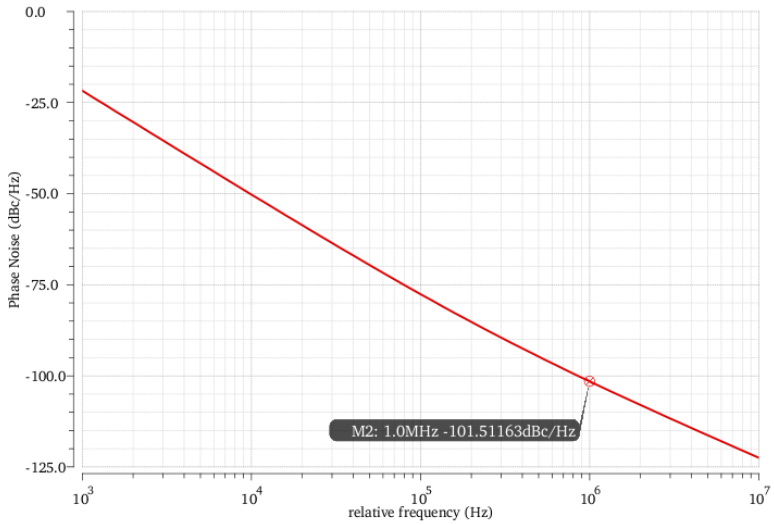


Figure 4.31: PSS and Noise Analysis on Final Extracted DCO – All Varactors Off

There is good power (about -2.3 dBm) coming out at the required frequency. Therefore, the results were deemed satisfactory. Finally the varactors were switched on (voltage on varactor gates changed from -0.5 V to 1 V) to show the frequency stepping in order to measure the resolution. This is plotted below in Figure 4.32:

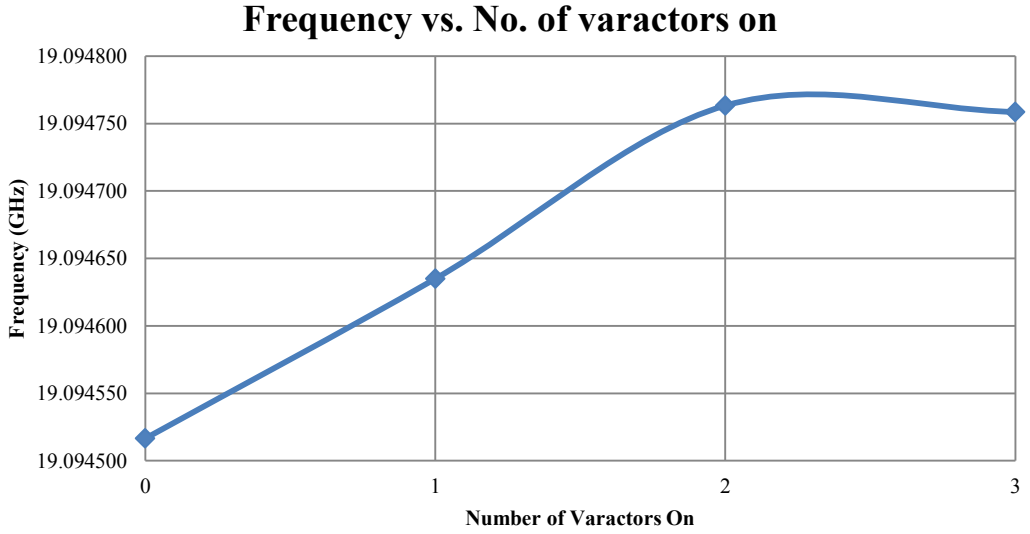


Figure 4.32: Frequency Resolution

The graph shows about 120 kHz of frequency change between the first three samples. However when the fourth varactor is switched on, there's a very small change in frequency. After try-

ing different center frequencies and obtaining the same non-monotonic anomaly while switching the fourth varactor, it was decided that this behaviour should be investigated more through actual testing on chip.

4.3.3 Testing

In a similar manner as in the first design in this thesis, the chip was manufactured and bonded to a PCB with female headers where the DC connections were made. This is shown in Figure 4.33:

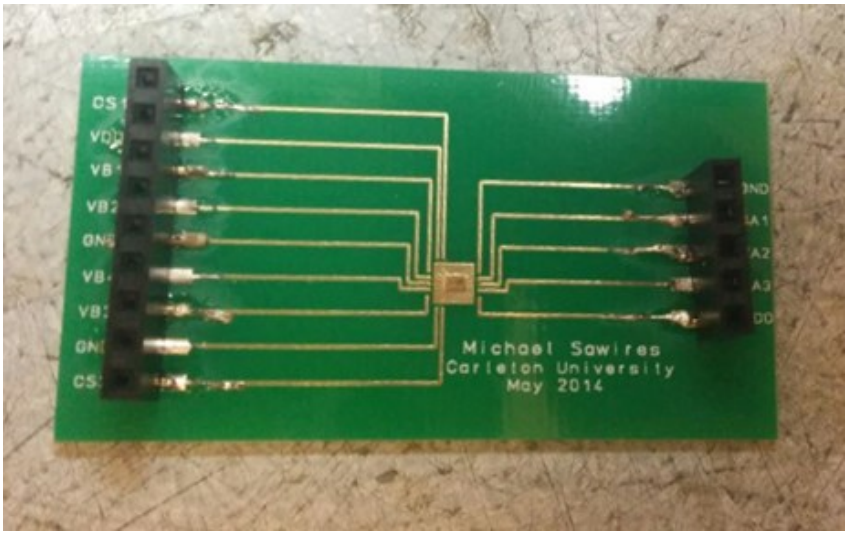


Figure 4.33: Chip Bonded to PCB

However the kind of wires used to make the DC connections were changed. It was noticed while making the measurements on the first design that the wires used were too thick and rigid and so when many of them were connected to the PCB, they exerted a lift on the PCB which caused a risk of them hitting the GSG probes and damaging them. As a result, for this measurement, much thinner (softer) telephone wires were bonded to male headers and then inserted directly to the female headers on the PCB. Not only was this safer for the probes, it also meant that substituting the chip under test was much quicker and convenient, since it only involved the unplugging of the set of male headers on both sides, substituting the board and then plugging them again.

The test setup is shown in Figure 4.34.

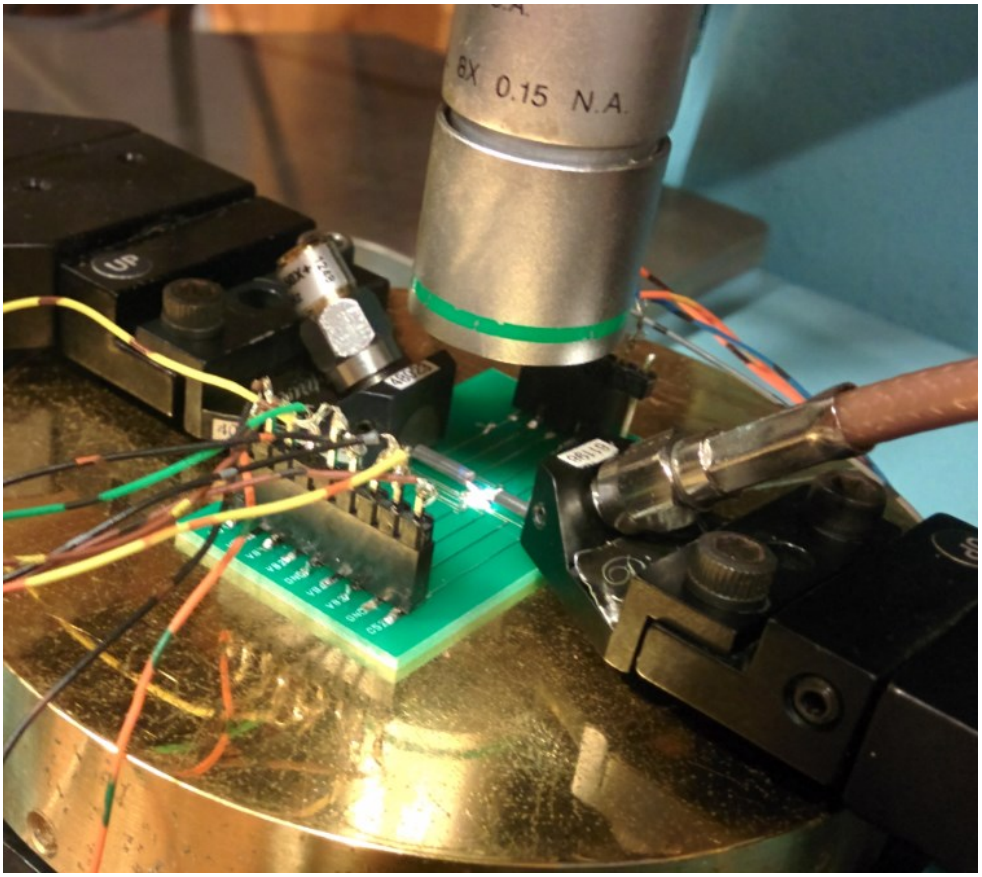


Figure 4.34: Test Setup

The setup shows the telephone lines carrying the signal to the PCB from the two sides of the PCB. From the other two sides, two GSG probes probe the bond pads of the chip. One of them has a 50 Ω termination while the other carries the output signal to the spectrum analyzer. The PCB is held in place with means of a vacuum pump. Figure 4.35 shows the chip view under the microscope along with the bonding and the probes.

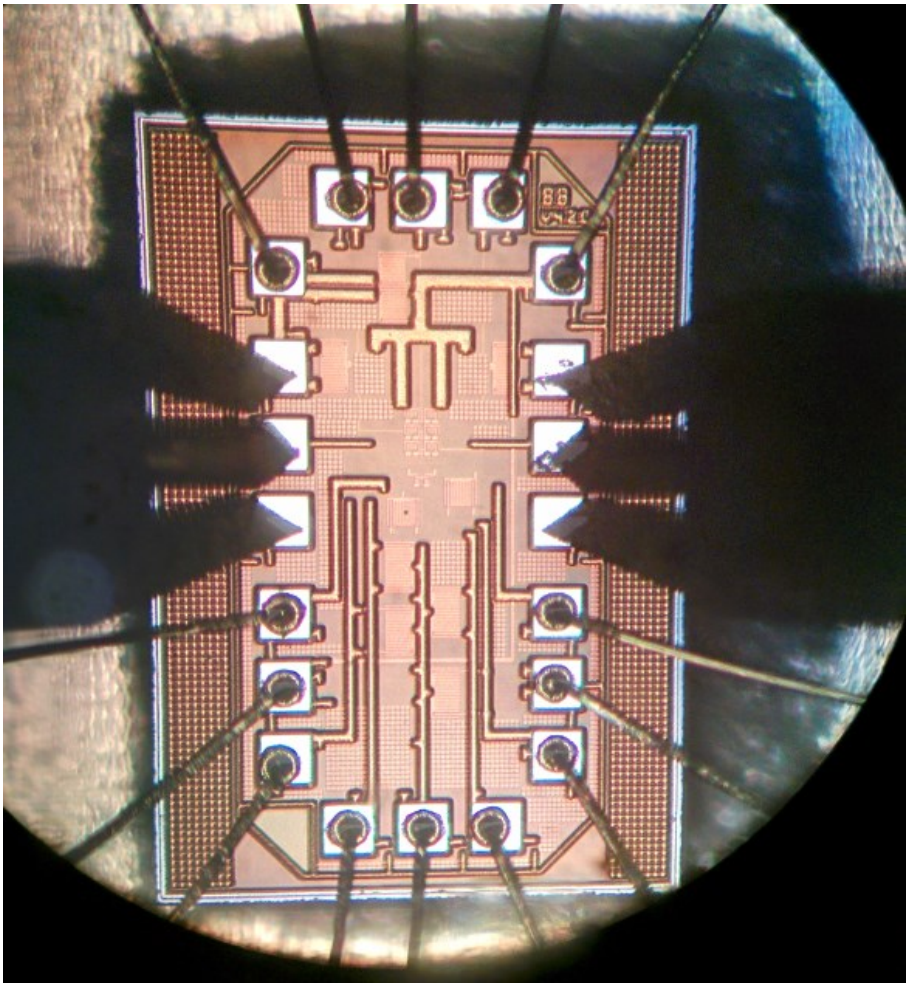


Figure 4.35: Probing the Final Design

After turning on the power, the current was adjusted to make sure the core and buffer were biased according to the simulation. Unfortunately the chip did not register any output on the spectrum analyzer. The voltages at different nodes were checked and found to match the simulation node voltages, though with no oscillations detected. Currents in the core and buffer were increased until the core current was roughly 13 mA per pair but still to no avail.

In order to rule out problems in the PCB or wiring, testing was done again on the individual dies but after gluing them to a glass slide. Figure 4.36 shows the arrangement made:

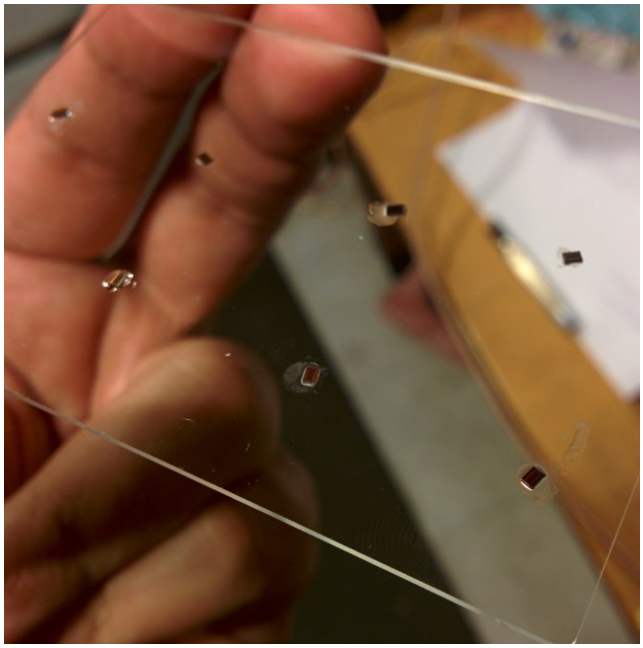


Figure 4.36: Dies on Microscope Slide

The slide was then mounted on the chuck directly and probed. However, only the necessary pads were proved. These were VDD, core bias, buffer bias and ground. Varactor biases were left floating however since that would not prevent the oscillator from starting. Figure 4.37 shows the chip probing (compare with Figure 4.29).

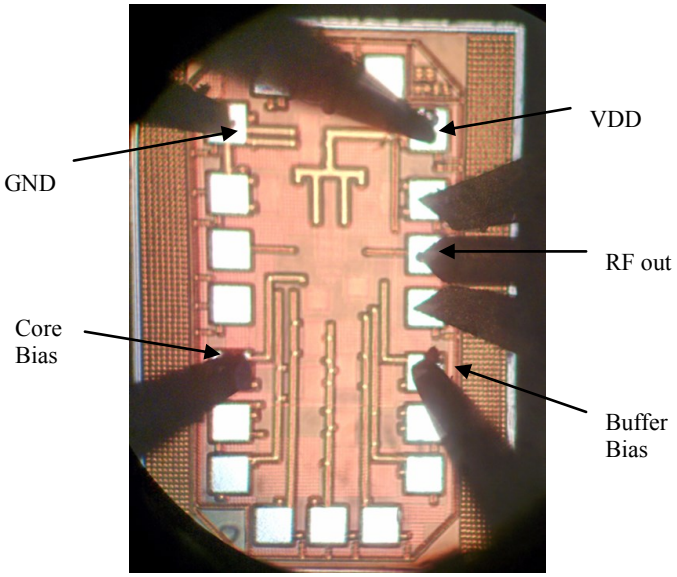
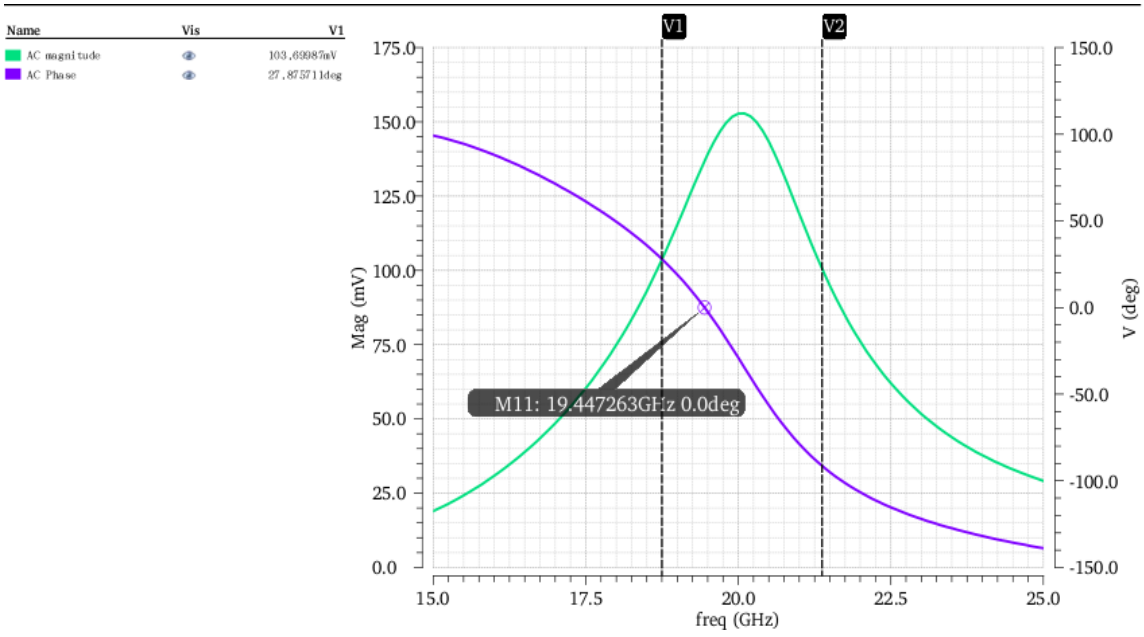
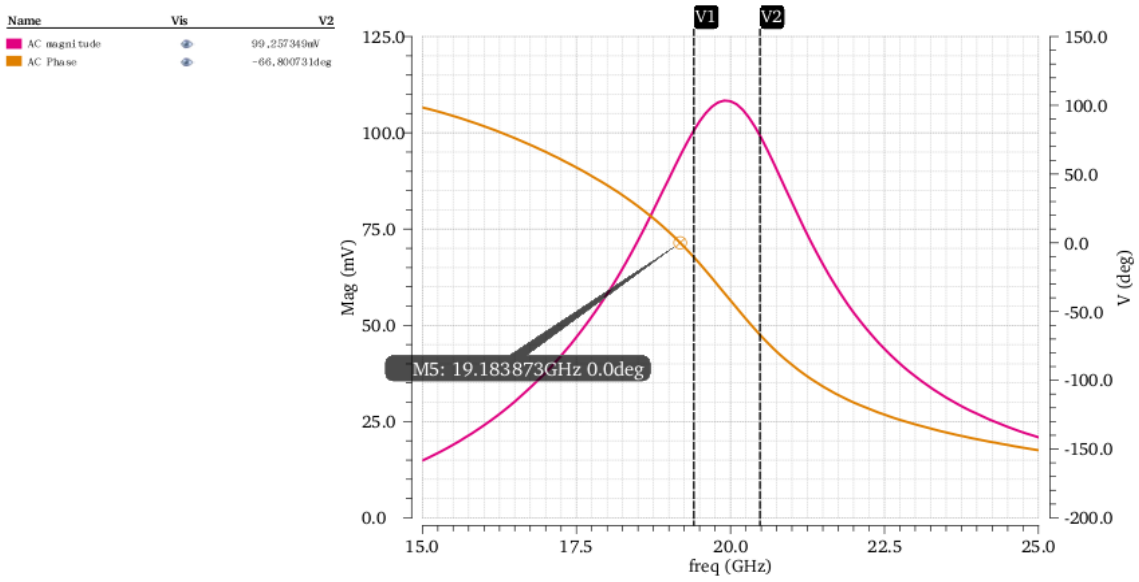


Figure 4.37: DC Probing

Unfortunately, results were still not obtained. A total of 12 dies were tested without obtaining any results. Therefore it was concluded that the design did not work successfully on chip. In order to investigate possible reasons why that is the case, further simulations were run on the RLC extracted view. Open loop analysis was performed by opening the loop near the gate of the first transistor, making sure the loading was still correct, then measuring open loop gain and phase. Loading was adjusted by means of a 50 fF capacitor to ground to simulate the gate capacitance in closed loop conditions. Analysis was then run for both typical and slow processes as shown in Figure 4.38. A signal of 100 mV was input at the gate and the magnitude and phase of the output around loop was plotted as shown below. Note the region where the signal is higher than 100 mV signifying positive gain.



(a)



(b)

Figure 4.38: Open Loop AC Analysis – (a): Typical Process, (b): Slow Process

It was noticed that when slower processes were used for the simulation, the oscillator stopped working completely (in pss analysis), even when increasing the bias current. This is because as demonstrated in Figure 4.38, the Barkhausen Criterion is never met for the slow process (refer to Section 2.1.2 on Barkhausen Criterion). In other words, there is no frequency for which the loop has both a positive gain and a phase difference of zero degrees. As a result the slow process oscillator never oscillates. However, when the first oscillator design is tested using slow corner process, the oscillator works fine though at an amplitude about 4 dB less. Open loop analysis also shows a zero degree phase difference point in a region with strong gain. This implies that the final design pushes the oscillator to the limits of stability preventing it from starting up oscillations. At these high frequencies where design is already more marginal, a process change is more likely to cause the circuit to fail.

Finally, the small amount of inductance being used also decreases the parallel resistance of the resonator hence lowering the loop gain. The Q of the resonator of the final oscillator is investigated to compare it with the first circuit. The capacitive part has a Q of 6.4 with a total capacitance of 227 fF. The inductance in the circuit is 278 pH (taking into account parasitic inductance) and has a Q of 24.9. A transmission line was simulated for the inductance in order to obtain this value of Q. Thus using equations (4.5) through (4.9), the equivalent tank resistance of the parallel resonator is 178.3 Ω and the Q of the resonator is equal to 5.09. Compared to the updated cal-

culations in Section 4.1.3 (using the vertical capacitors instead of dual mimcaps), the first design's Q and R_p values were 21.9 and 243 Ω respectively. This tank Q is about four times less than the Q of the resonator in the first oscillator. The complicated varactor arrangement in the final design added more loss to the resonator and hence decreased the gain of the oscillator making it easier to be stable and not oscillate.

In retrospect it the slow process corner should have been checked before getting the oscillator fabricated to make sure the gain in the loop is enough to withstand any unexpected problems in processing. That is, allowing more gain margin to overcome possible circuit deterioration during fabrication.

Chapter 5: Conclusion

In this thesis, the design of a high resolution DCO was investigated. After investigating previous work in the field, three attempts at designing a fine resolution DCO were made. Although only the first design produced measurable results, the other designs theoretically achieved better results.

In the first design, the smallest possible kit varactor was used while minimizing the inductance in the circuit. Minimizing the inductance leads to having more capacitance in order to achieve the same frequency, thus resulting in a smaller $\Delta C/C$ ratio and hence a smaller $\Delta f/f$ which is equivalent to a finer resolution. This design yielded a measured resolution of about 30 MHz at 17.700 GHz. This is quite close to the estimated 24 MHz obtained through extracted view simulation, although the centre frequency also dropped by about 1 GHz.

This method therefore achieves satisfactory results although only in the tens of megahertz resolution. With more careful characterizing (such as including EM simulations), one can achieve slightly better performance by possibly decreasing spacing between components and thus using less interconnect and so reducing parasitic capacitance and inductance. Parasitic capacitance plays a significant role especially with the use of lower metal layers.

In the second design, a small fixed capacitor was used in series with a varactor thus minimizing the effective change of capacitance due to the switching of the varactor. Theoretically a resolution of 5 kHz was achieved. However due to the number of varactor banks in the design and the complexity and size of the circuit (especially the resonator), there was a lot of parasitic components extracted by the simulator and so the circuit did not work at all in extracted layout view. Therefore, it seems that the more tuning range covered by incremental digital stepping, the harder it becomes to realize a design. This is due to the fact that the interconnect adds more parasitic inductance than the designed inductance and adds resistive loss to the resonator.

Finally, the final design was created learning from the previous two design experiences. While using minimum interconnect for minimizing inductance, and using the principle in the second design of connecting a small fixed capacitor in series with the varactor being switched, a 100 kHz resolution DCO was designed, laid out and extracted successfully and found to be working well at the required center frequency. However, the design failed to work on a real sili-

con die. The main reason for this discrepancy between the simulated and obtained results could be due to the much lower gain margin (as demonstrated in the end of Chapter 4) that was adequate for the chip to just work at a nominal process. The increased complexity of the resonator design added too much loss and moved the oscillator closer to the stability boundary. Hence the oscillator did not need much process irregularity to force it to not oscillate. That is, it was noticed that when the simulation was repeated at any slower process, the oscillator stopped working (unlike in the first oscillator, which passed slow corner testing). This suggests that there might have been a performance problem due to the process being too slow.

Overall, it could be argued that in order to achieve a working DCO at 20 GHz (especially using the technology used in this design), one must make sure that there is enough open loop gain margin in the oscillator and so functionality should be tested over slower process corners. This would involve using larger transistors than 20 μm to achieve better transistor g_m and thus better gain. Simpler, more compact structures to achieve the high resolution would also be recommended because as mentioned earlier, it is very easy to add parasitic capacitance and inductance at 20 GHz. The results could be as adverse as preventing the oscillator from functioning at all.

The use of lower metals for interconnect also seems to produce more harm than benefit since it is associated with a lot more parasitic capacitance which can kill the oscillator completely (in the case of the two final oscillators). Even though much less inductance was achieved in the three designs in this thesis, the parasitic capacitance (and inductance in the case for the second design) was critical to the DCO performance.

Another possible adjustment is to use differential probes which would guarantee making use of the differential advantage of an oscillator. In case a differential spectrum analyzer is not available, the differential probes can be used alongside a balun to convert the differential measurement from the two single ended probes into a single ended output for spectrum analyzer. If differential measurement is not available, one could resolve to a single ended approach to the design from the first step instead. Even though this would get rid of the common mode noise cancellation advantage that differential circuits have (assuming differential measurement is carried out), it would be more reliable to test. A Colpitts, Hartley or even a single ended negative resistance microwave oscillator topology could be used. The last involves a purely microwave de-

sign where s-parameters are analyzed and the oscillator is made sure to be unstable at the required frequency, possibly with the help of distributed components.

The technology used (0.13 μm CMOS) also seemed to hinder how much performance could be obtained at 20 GHz, especially when the boundaries were pushed in the final design with a slightly more complex topology for the resonator. A more recent bipolar or HBT process with higher f_T transistors would be able to provide better gain for the oscillator at the same frequency and bias, thus avoiding the problem that happened in the last oscillator.

At 20 GHz, the use of EM simulation to characterize passives components in the circuit would help in guaranteeing design reliability. This is particularly important for the resonator since it would take into account the EM wave reflections due to bends in the shape. It would also better characterize the interconnect lines, especially the ones nearer to the substrate where effects like substrate inductive coupling and parasitic capacitance to substrate can be taken into account better. This would help prevent the failure that happened particularly in the third design where there were multiple bends and complex geometries in the resonator.

Overall, this thesis successfully pushed the boundaries of creating a fine resolution DCO at 20 GHz using a 0.13 μm CMOS process. Even though in practice the final design did not work on a fabricated die, it came close since it did work in extracted view adding in all the parasitics. With more investigation and building on the work done in this thesis, achieving a successful kHz resolution DCO at 20 GHz seems within grasp.

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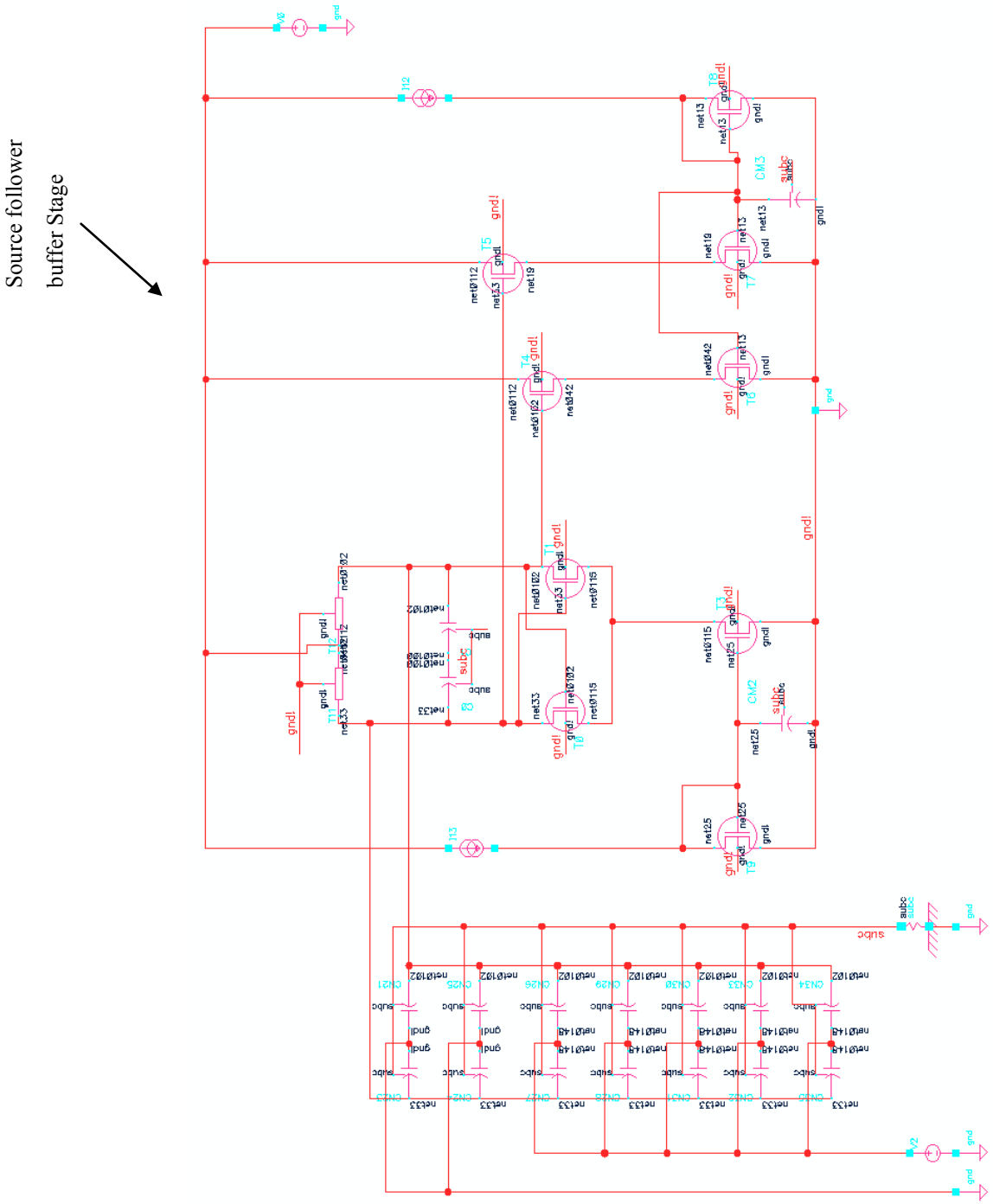
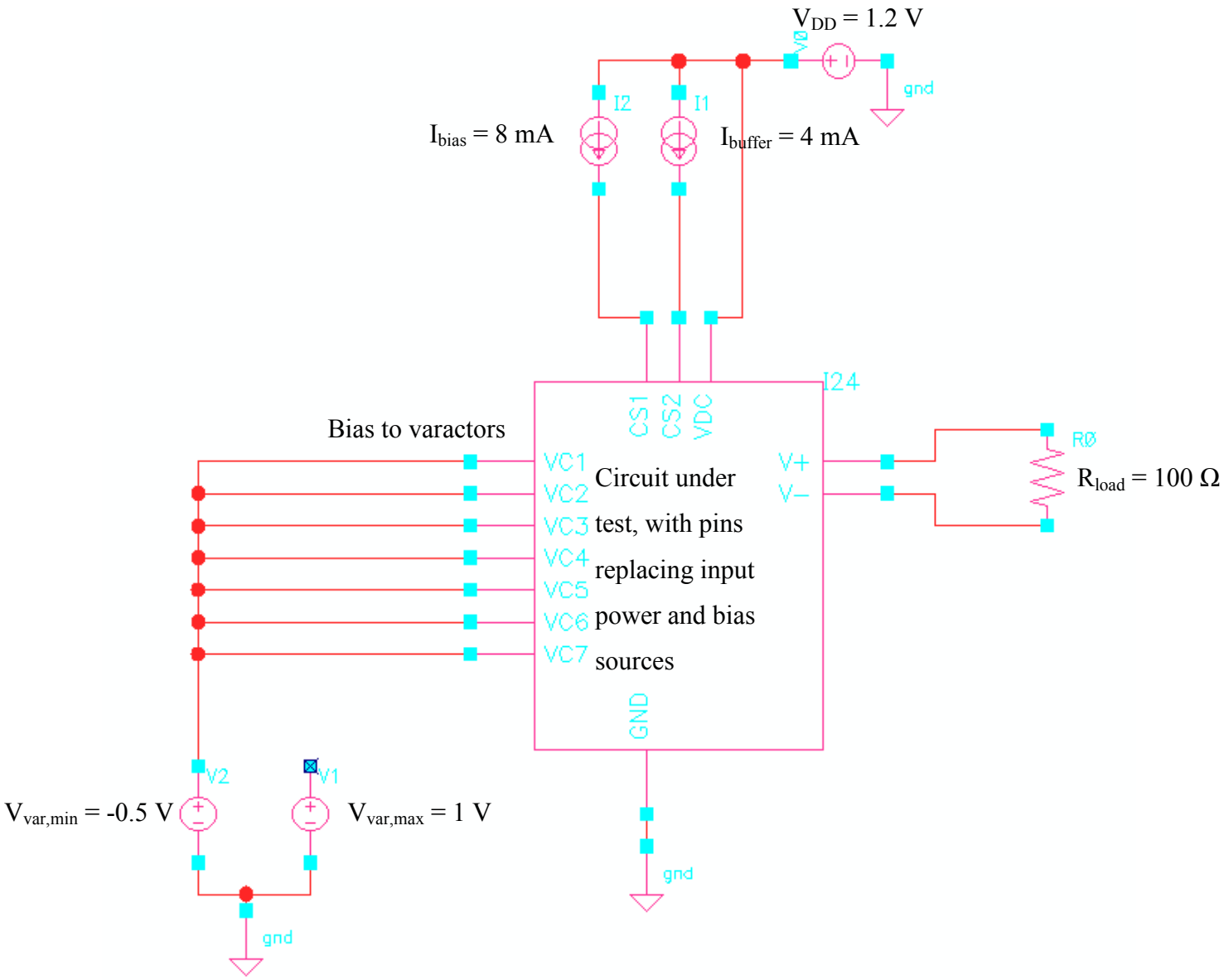
APPENDIX

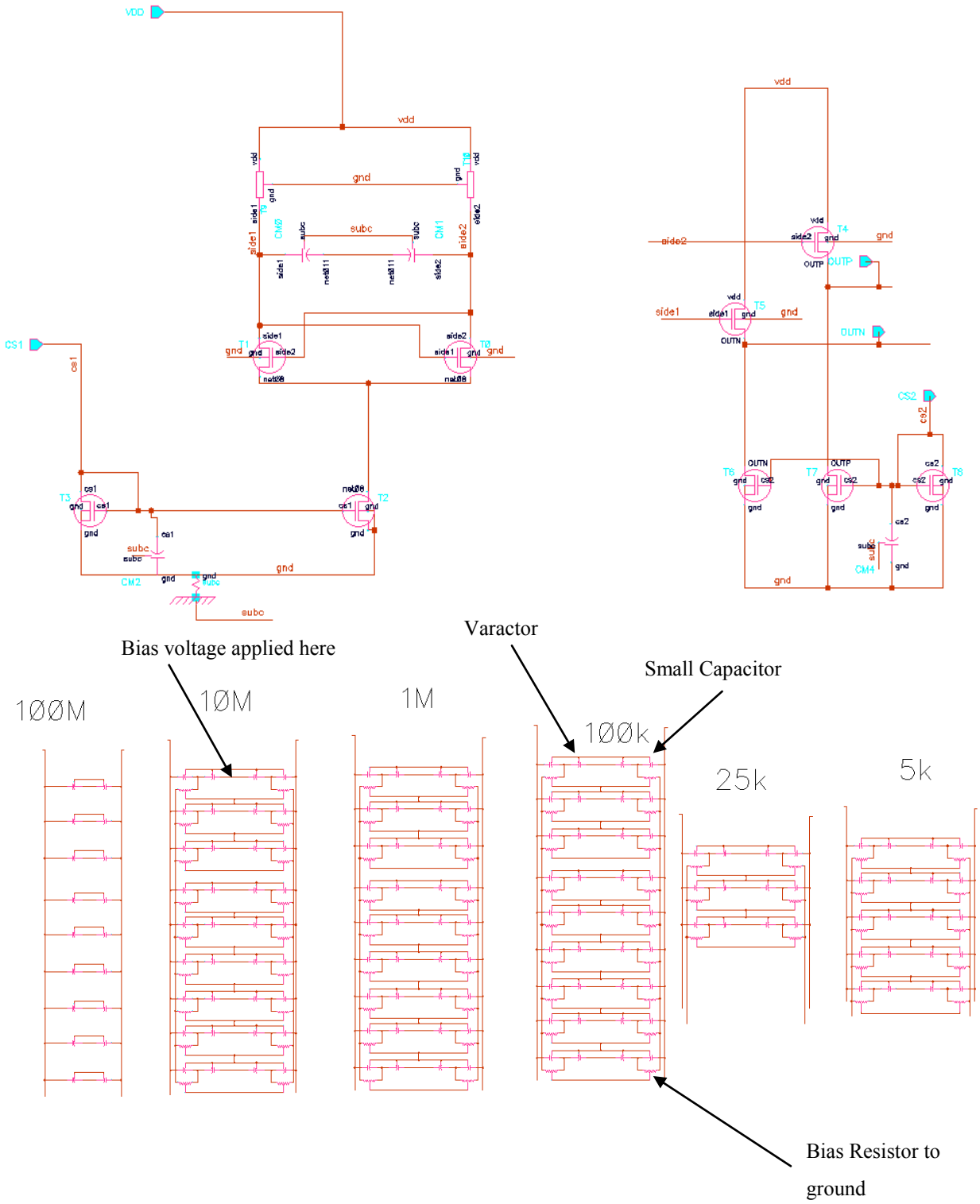
First Design Schematic:



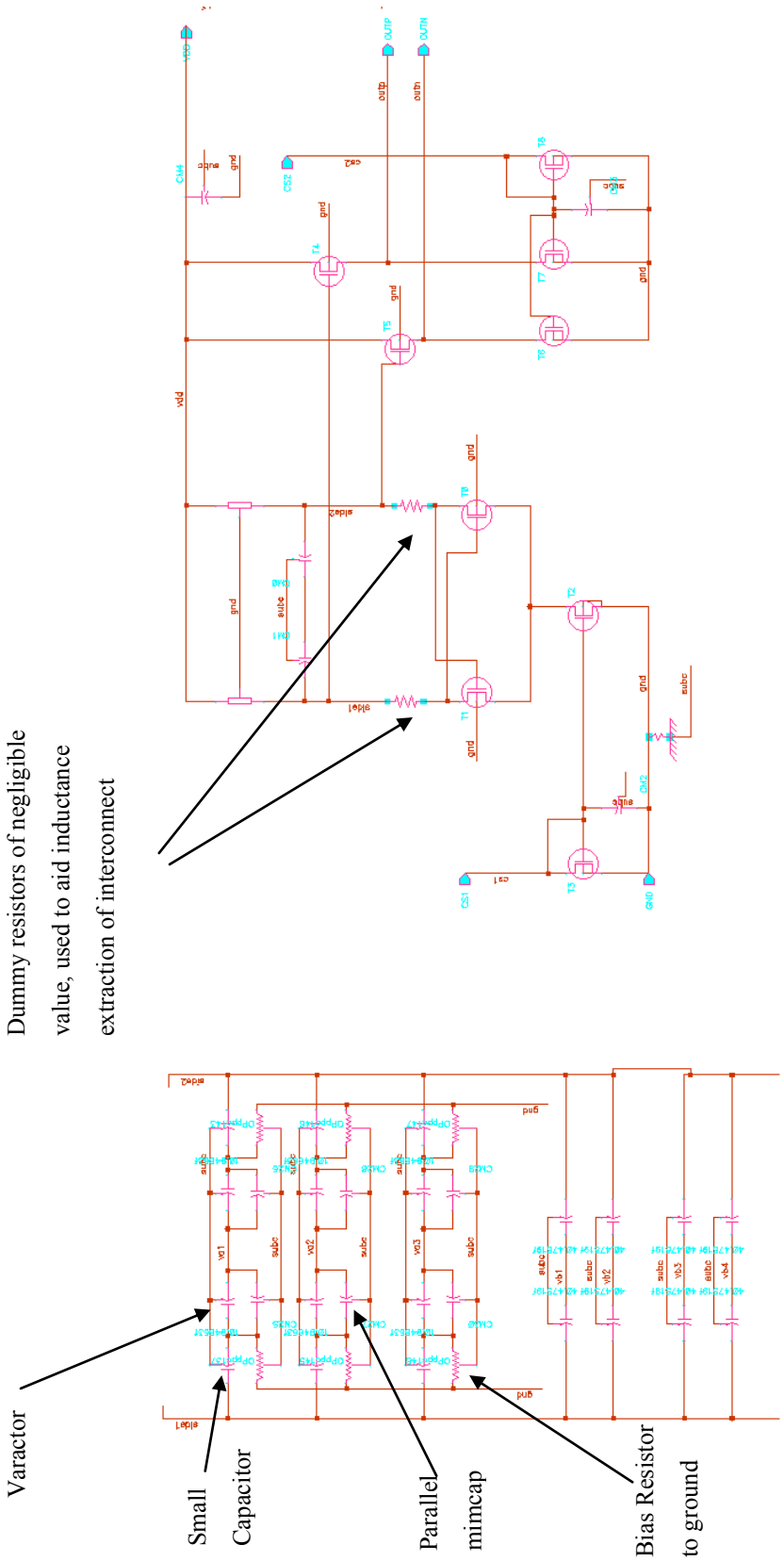
Test Bench: (used after circuit is made sure to start up properly)



Second Design Schematic: (refer to Figure 4.24 for the digital control section)



Third Design Schematic:



Component values for First Design:

Component	Cell Name	Parameters			
Core Transistor	nfet_rf	Width Single Finger = 2 um	Width All Fingers = 50 uM	Length = 120 nm	No. of Fingers = 25
Buffer Transistor	nfet_rf	Width Single Finger = 9.37 um	Width All Fingers = 281 uM	Length = 200 nm	No. of Fingers = 30
Inductor	rf_line	Metal Width = 13.9 um	Metal Length = 105 um		
Fixed Capacitor	vncap	Length = 40 um	Width = 40.12um		
Varactor	ncap	RX Width = 1um	PC Length = 290 nm	No. of gates = 2	RX Repetition = 1

Component values for Second Design:

Component	Cell Name	Parameters			
Core Transistor	nfet_rf	Width Single Finger = 2 um	Width All Fingers = 50 uM	Length = 120 nm	No. of Fingers = 25
Buffer Transistor	nfet_rf	Width Single Finger = 9.37 um	Width All Fingers = 281 uM	Length = 200 nm	No. of Fingers = 30
Inductor	rf_line	Metal Width = 15 um	Metal Length = 100 um		
Fixed Capacitor	mimcap	Length = 5.24 um	Width = 5.24 um		
Bias Resistor	opppcres	Width = 400 nm	Length =800 nm	No. of series bars = 1	
Small Capacitor (5 kHz tuning)	vncap	Length = 8.76 um	Width = 3.64 um		
Varactor (5 kHz tuning)	ncap	RX Width = 5um	PC Length = 5 um	No. of gates = 20	RX Repetition = 5
Small Capacitor (25 kHz tuning)	vncap	Length = 8.76 um	Width = 8.44 um		
Varactor (25 kHz tuning)	ncap	RX Width = 5um	PC Length = 5 um	No. of gates = 27	RX Repetition = 5
Small Capacitor (100 kHz tuning)	vncap	Length = 10 um	Width = 9.4 um		

Varactor (100 kHz tuning)	ncap	RX Width = 5um	PC Length = 5 um	No. of gates = 14	RX Repetition = 5
Small Capacitor (1 MHz tuning)	vncap	Length = 11 um	Width = 12.28 um		
Varactor (1 MHz tuning)	ncap	RX Width = 3 um	PC Length = 5 um	No. of gates = 4	RX Repetition = 5
Small Capacitor (10 MHz tuning)	vncap	Length = 16.4 um	Width = 13.24 um		
Varactor (10 MHz tuning)	ncap	RX Width = 3um	PC Length = 1.8 um	No. of gates = 5	RX Repetition = 4
Varactor (100 MHz tuning)	ncap	RX Width = 1um	PC Length = 240 nm	No. of gates = 10	RX Repetition = 1

Component values for Third Design:

Component	**Cell Name**	**Parameters**			
Core Transistor	nfet_rf	Width Single Finger = 2 um	Width All Fingers = 50 uM	Length = 120 nm	No. of Fingers = 25
Buffer Transistor	nfet_rf	Width Single Finger = 9.37 um	Width All Fingers = 281 uM	Length = 200 nm	No. of Fingers = 30
Inductor	rf_line	Metal Width = 25 um	Metal Length = 100 um		
Fixed Capacitor	mimcap	Length = 5.24 um	Width = 5.24 um		
Bias Resistor	opppcres	Width = 400 nm	Length =800 nm	No. of series bars = 1	
Small Capacitor (100 kHz tuning) ***(in series with varactor)***	vncap	Length = 16.4 um	Width = 13.24 um		
Varactor (100 kHz tuning)	ncap	RX Width = 1 um	PC Length = 1 um	No. of gates = 1	RX Repetition = 1
Large Capacitor (100 kHz tuning) ***(in parallel with varactor)***	dualmimcap	Length = 10 um	Width = 10 um		
Varactor (1 GHz tuning)	ncap	RX Width = 1um	PC Length = 290 nm	No. of gates = 2	RX Repetition = 1