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**6 GHz INDUCTOR-LESS TUNED LOW NOISE AMPLIFIER
INCORPORATING AN ARTIFICIAL TANK CIRCUIT**

by

ABDULHAKIM AHMED

B. ENG. (ELECTRICAL ENGINEERING)

A thesis submitted to the Faculty of Graduate Studies and Research in partial fulfillment of the
requirements for the degree of

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ABSTRACT

This thesis presents a novel design of a 6 GHz Low Noise Amplifier (LNA) incorporating a damped ring oscillator, which is used as the the tuning circuit to replace the LC-tank in the LNA. Algebraic equations necessary to describe the behaviour of the ring oscillator as an artificial tank were developed and derived. The simulated design of the LNA gave a power gain of 9 dB. The LNA was fabricated in CMOS 0.18 micron technology, mounted and bondwired to a glass printed circuit board (PCB) and its S-parameters were tested. The test results obtained were different from the simulated ones mainly because of process variation, but demonstrated the operation of the artificial tank.

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LIST OF SYMBOLS

A	Small Signal Gain of an Inverter.
ADS	Advanced Design Systems.
AI	Artificial Inductor.
AT	Artificial Tank.
BB	Base-Band.
C _{gs}	Gate to Drain Capacitance in CMOS.
CMC	Canadian Microelectronics Corporation.
CMOS	Complimentary Metal Oxide Semiconductor.
dB	Decibels.
DRO	Differential Ring Oscillator
ESD	Electro-Static Discharge.
GHz	Gigahertz.
g_m	Small Signal Transconductance of a Transistor.
HD2	2nd order Harmonic Distortion.
IC	Integrated Circuit.
ICFCULMV	Name of Circuit Die.
ID	Inter-Digitated.
IF	Intermediate Frequency.
IM3	The 3rd Order Inter-Modulation Product.
In	Noise Current resulting from Noise Voltages.
IP3	3rd order intercept Point.
k	1/RC time constant.
K	Boltzmann constant.
LC-tank	Inductor and Capacitor in parallel that forms the output impedance of a tuned circuit.
LMX	LNA-Mixer.
LNA	Low Noise Amplifier.
LO	Local Oscillator.
MHz	Megahertz.

NDP	NMOS Differential Pair.
NF	Noise Figure.
P-1dB	One dB Compression Point.
PCB	Printed Circuit Board.
PLS	Post Layout Simulation.
PSS	Periodic Steady State.
Q	Quality Factor.
RB	Rectangular Balun.
RF	Radio Frequency.
r_o	Output Resistance of an Inverter.
RO	Ring Oscillator.
R_S	Series Resistance.
SNR	Signal to Noise Ratio.
VPWL	Piece-Wise Linear Voltage Source.
VNA	Vector Network Analyzer.
V_{n1}	Noise Voltage due to Gate Resistance R_{g1} .
V_{n2}	Noise Voltage due to Gate Resistance R_{g2} .
V_{no1}	Noise Voltage due to Output resistance r_{o1} .
V_{ns1}	Noise Voltage due to Interanal Source Resistance R_{s1} .
V_{ns2}	Noise Voltage due to Interanal Source Resistance R_{s2} .
V_x	Voltage at Source of the Amplifying Transistor next to the Channel.
V_y	Voltage at Source of the Load Transistor next to the Channel.
Z_{out}	Output Impedance.
δ	Dirac Delta Function.
τ_d	Time Delay in seconds.
ω	Angular Frequency in Radians per Second.
ω_o	Center Angular Frequency of the Ring Oscillator
∞	Infinity.

1.0 INTRODUCTION

The function of a Low Noise Amplifier (LNA) is to minimize the noise produced by the amplifier at the input to a Radio Frequency (RF) receiver. The low noise figure of the LNA ensures that the following circuit components do not have to minimize noise in their circuits because of the cascading Noise Figure effect (discussed in the section 2.3 of this Thesis) [4.1].

Noise in electrical circuits, which is mainly caused by the nature of the semiconductors used, is a hindrance to the incoming signals because it interferes in the demodulation of the signals in the back-end of a radio. Since the noise is a natural phenomena, it is not easy to minimize, except by filtering out the part of the incoming electro-magnetic spectrum that is not occupied by the signal, and by ensuring that maximum power transfer occurs between the antenna and the input of the front-end of a radio. Noise can be further minimized by filtering the output of the amplifier so that those frequencies not within the signal bandwidth are attenuated rather than amplified. This circuit is called a tuned amplifier, or a tuned low-noise amplifier (LNA). The LNA is biased in such a way as to minimize its own noise contribution which arises from its components [4.1].

The maximum power transfer, which is required at the input to achieve the highest possible Signal-to-Noise Ratio (SNR), is obtained using a “matching network” which tunes the input of the radio to the incoming signal frequency, while attenuating all other frequencies. Since the exact input impedance of the LNA after manufacturing is not known and is subject to manufacturing variations, the input matching network can be put off-chip, for low volume fabrication. However, if the chip is mass-produced, the matching network is often put on-chip to ensure complete

integration and reduce costs. At high frequencies, between 1 to 6 GHz, many of these matching networks include high-Q inductors which not only occupy large chip areas (from 100um x 100um to 400um x 400um) but also have large variations in performance from chip to chip [4.3]. In addition, these inductors exhibit large capacitances to ground and thus behave like capacitances at higher frequencies. There has been extensive research on this topic, and active inductors are used to replace the passive elements for input matching at low frequencies. However, at higher frequencies, the Quality (Q) factor of these active inductors is reduced and the maximum Q available in the 5 to 6 GHz band from an active inductor is about 8 [1]. This implies that the equivalent input matching inductor would have an equivalent series resistor equal to [2]:

$$R_s = \frac{\omega L_s}{Q}. \quad (1)$$

This in turn introduces noise to the LNA, since the lower the Q, the higher the series resistance. Thus it is not desirable to use active inductors for input matching networks [4.4].

Inductors are also used to tune the output of the LNA. This kind of an inductor is used in an LC-tank and thus called a “tank-inductor”. Here the source of noise in the inductor is less of a concern, as the Gain of the LNA causes the output SNR to be high as long as the input noise is kept low by minimizing the thermal noise contributed by the resistive elements of the input matching network and the amplifier itself. This minimizes the effective Noise Figure, given by equation (2) [3.10].

$$NF = \frac{SNR_{in}}{SNR_{out}}. \quad (2)$$

However, the Q of the active inductors that are used to miniaturize the circuits are also low at higher frequencies, and thus the resulting Q of the LC-tank is low (Q s add like resistors in parallel for Q_C and Q_L). For a high gain, which is required to keep the NF in the system low, a high- Q output tank is required to provide a large output impedance to the amplifier. Another technique, developed as part of this Thesis, is introduced to achieve this requirement. This new technique is discussed and described in Sections 3.6 to 3.9, and can be used not only for an LNA, but for any tuned circuit.

Another tuned circuit in which the high- Q tank developed in this Thesis can be used is a Mixer which is used to up or down convert the message signal from a mixture of the carrier and the message signal [3.0]. The Mixer in an RFIC receiver is a non-linear circuit used to down-convert the high frequency modulated carrier signal to a lower frequency modulated signal. The carrier signal is usually a few orders of magnitude greater than the intermediate frequency (IF) signal. Before the signal is demodulated, it has to be first converted to its original message frequency, usually in the range of hundreds of MHz. This down-conversion usually results in a high NF because the LO signal, which is used to frequency shift the modulated carrier, is generated and supplied to the Gilbert cell [3.1] mixer at the gates of the upper-quad transistors without a matching network that would ensure maximum power transfer. A matching network is not desirable for the LO signal because a switching behaviour is required from the LO signal to provide the “mixing” effect. Hence the upper-quad is a source of high noise in the Mixer, which is down-converted to the IF signal and added to the modulated signal. The basic building blocks of a Mixer are described in the many RFIC design books [3.2].

The main objective of this Thesis is to create an LNA in CMOS IC technology, with acceptable parameters for the 802.11a wireless LAN standards, without the use of inductors on the IC by substituting other circuit(s) to replace the inductor or the whole LC-tank. Chapter 2.0 describes the basic and general issues involved in LNA design. Exactly how this LNA circuit was conceived is discussed in Chapter 3.0. Not using inductors reduces the chip-area, thus minimizing the cost of a potential commercial chip. Once the simulated circuit met the acceptable parameters using the Spectre schematic simulator in Cadence, layouts were created for the circuit, the circuit was extracted, and post layout simulations were performed to ensure that the circuit would work once manufactured. These simulations are discussed and the results are shown in Chapter 4.0.

Finally, an evaluation board was created to test the chip. When the fabricated chip was returned from CMC, the chip was mounted and bondwired to the evaluation board and test results were recorded. This is described in Chapter 5.0. The Conclusion deduced from these test results, together with the future work that can be done to improve the LNA design and test method, is discussed in Chapter 6.0.

2.0 BACKGROUND

2.1 Amplification

The LNA is supposed to have high Gain (defined as the ratio of output small-signal Voltage or Power to the input small-signal Voltage or Power) because this renders the noise effect caused by the following circuit components to be negligible [3.4].

Gain is obtained when a small input voltage signal is “converted” to a large output signal (current, voltage or power) using components such as Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). The gate of the MOSFET is separated from the bulk of the semiconductor by a thin layer of silicon oxide. A Voltage applied to the gate creates a “channel” in the bulk through which electrons or holes can flow between the Source and the Drain. It is important to keep the Drain to Source Voltage (V_{ds}) greater than the difference between the Gate to Source Voltage (V_{gs}) and the Threshold Voltage (V_t), which is the minimum voltage at which the channel is formed, so that the transistor remains in the saturation region of operation. This minimizes the 2nd and 3rd order inter-modulation product frequencies (explained in Section 2.4) by ensuring that the transistor behaves as a linear amplifier and provides a larger voltage gain. The basic MOSFET equations are given in Appendix B. The current flow through the channel can be passed through a resistor to give a high voltage gain. The power gain is the product of the current gain and the voltage gain. Gain and matching are discussed in detail in Section 2.2 next.

2.2 Voltage and Power Gain

When one talks of voltage gain, one refers to V_{out}/V_{in} . However, when one talks of instantaneous power gain, P_{out}/P_{in} , where:

$$P_{in} = V_{in} \times I_{in}, \text{ and } P_{out} = V_{out} \times I_{out}.$$

$$\text{Now: } I_{out} = V_{out} / R_{out}, \text{ and } I_{in} = V_{in} / R_{in}$$

Here, R_{in} is the small-signal input impedance of the circuit and the R_{out} is the small-signal output impedance of the circuit. Unless R_{out} and R_{in} are exactly the same, the maximum voltage gain is not going to be obtained at the same frequency as the maximum power gain. Thus there is a definite need for both input and output matching.

Since most Test Equipment has input and output terminals of 50 Ω impedance, it is important that both input and output impedances of the amplifying circuits are matched to 50 Ω for maximum input and output power transfer from and to the measurement devices.

2.3 Noise Figure

The first circuit to receive the incoming Radio Frequency (RF) signal from the antenna is a Low Noise Amplifier (LNA). An LNA is a circuit that amplifies an input signal within a specified Band-Width (BW), while contributing a Noise Figure (NF) small enough so that the Noise Power (P_n) at its output does not affect the rest of the circuit in the RF receiver chain.

Electronic Noise (referred from now on as simply noise) is caused by the thermal vibration of electrons in all the materials that comprise the circuit. It is caused by the random movement of electrons in the materials. This is called Thermal Noise and represented by $4KTRB$ (in V^2/Hz).

Another type of noise that occurs in electronic circuits is Shot Noise which is caused by the quantum values of the currents flowing through the P-N junctions in circuits. This is represented by $2qIB$ in (A^2/Hz) [3.5]. However, since the LNA in this Thesis uses only MOSFETs, there are no P-N junctions through which the main drain current (I_D) flows when the MOSFETs are in Saturation region of operation. Therefore there is no need to consider this type of noise source for this LNA.

It is important to suppress all noise sources at the beginning or the input of the receiver-chain so that the noise does not get amplified by the first circuit which is the LNA. The LNA should also have high Gain as discussed above, since this renders the noise contributions of the following circuits to be negligible.

The NF of a number of components in series is given by [3.6]:

$$NFT \text{ (linear)} = NF1 + (NF2 - 1)/G1 + (NF3 - 1)/G1*G2 + (NF4 - 1)/G1*G2*G3 + \dots \quad (3)$$

From equation (3), we can see that as long as the Gain of the first circuit component ($G1$) is high and its NF ($NF1$) is low, then the effect of the NF of the second circuit component adds little to the total NF (NFT).

2.4 Harmonics and Inter-Modulation Products

In addition to providing a low NF, the LNA suppresses the 2nd order harmonic distortions and 3rd order inter-modulation product frequencies not only in order to meet the specifications required for the design of the LNA, but also in order to provide a “clean” output signal to the rest of the components in the Receiver-chain [4.6].

The 2nd order harmonic distortion (HD2) frequencies are caused by the multiplication in the time-domain (convolution in the frequency domain) of two signals with relatively high amplitudes at the input to the LNA. Although the HD2 frequencies are out of band and can be filtered-out, the HD2 frequencies can also be converted to, and interfere with, the Base-band (BB) frequencies (the frequencies of the message) by a direct down conversion mixer which follows the LNA in a direct conversion receiver [3.7].

The 3rd order inter-modulation product (IM3) frequencies are caused by the addition of frequencies like $(2f_{in1} - f_{in2})$ or $(2f_{in2} - f_{in1})$. These products fall within the BW of an LNA and will be amplified. They cannot be filtered out, and therefore will interfere with the main input signal (f_{in1}) that is to be amplified. Furthermore, the IM3 frequencies will be down-converted by the mixer to BB frequencies and thus will interfere with the message to be demodulated by the Receiver-chain. The only way to get rid of these frequencies is to ensure that all the devices in the LNA work in the Saturation region and thus retain linearity [4]. This means that D.C. bias characteristics of the MOSFETS at the operating point have to be linear (not to be confused with the linear or triode region of MOSFET operation). A linear characteristic is one in which the region of a graph of I_{ds} verses V_{ds} , or V_{in} verses V_{out} shows an almost straight line.

There are some components that can be adjusted in the LNA to improve linearity. This will be discussed later in Section 3.13.

2.5 IP3 and 1dB Compression point

At some point, when the input signal is too large, the change in input power is not equal to the change in output power, i.e.:

$$\Delta P_{out}[f_{in1}] \neq \Delta P_{in}[f_{in1}]. \quad (4)$$

At some power level P_{out} decreases by 1dB below the regular straight line input-output gain characteristic given in equation (5):

$$\Delta P_{out}([f_{in1}] = \Delta P_{in}[f_{in1}]) \quad (5)$$

This point is called the 1-dB Compression point. It is normally advised to have the P_{in} 10dB lower than the 1-dB Compression point value, thus ensuring that the output does not begin to distort [4].

It is known that during amplification, the output power level of the IM3 frequencies increases three times as fast as the input power level (P_{in}) for the frequencies that are meant to be amplified within the BW. This information can be shown graphically in IP3-plots of P_{out} verses P_{in} [3.8].

In a similar way for the 1 dB compression, when the P_{in} of $[2f_{in1} - f_{in2}]$ reaches a certain level, the change in P_{out} is no longer 3 times change in P_{in} . The output power level of the $[2f_{in1} - f_{in2}]$ never exceeds that of f_{in} . However, when the straight lines obtained by the plots of output power

of the fundamental frequency and the third order intermodulation frequency are projected beyond the point where the lines are no longer straight, the lines meet at a point of intersection called IP3. The values obtained from these points are the input IP3 (IIP3) power level and the output IP3 (OIP3) power level. The graph of Figure 2.1 shows how the IP3 point is obtained.

Therefore the measure of power of the IM3 frequencies at the output is a measure of the linearity of the LNA. The lower the output power of the IM3 frequencies, the more linear the LNA. The reason is that we do not want the IM3 frequencies to interfere with the output signal of the LNA. These non-linearities become excessive when P_{in} exceeds the 1-dB Compression point because the output is no longer sinusoidal.

Figure 2.1: Demonstration of the IP3 Point.

Thus a high input referred 1-dB Compression point of about -18 dBm and a high input referred IP3 of about -5 dBm or greater is preferred. The 1-dB compression of greater than -18 dBm ensure

that the output will remain linear as long as the input voltage from a 50 ohm line does not exceed 22.36mV

2.6 Two Port S-Parameters

These are variables named S11, S22, S21 and S12 that represent the complex input and output reflection coefficients, the power gain, and the reverse isolation respectively [5].

2.7 Stability and Phase

The insertion phase of a circuit determines how stable the circuit is. This is because there is always a feedback path from the output back into the input of the circuit via the Gate-to-Drain capacitance, Cgd. If the phase is close to 180° , then positive feedback occurs because the output of the Common-Source amplifier configuration is inverting (i.e. $180^\circ - 180^\circ = 0^\circ = 360^\circ$), thus the output voltage adds to the input, giving a greater output voltage. This continues until the circuit currents saturate, making the circuit unstable. An unstable circuit would oscillate when given a "kick" by a high-frequency noise pulse. The stability is measured using S-parameter measurements in Cadence and is denoted by Kf. As long as Kf greater than 1, then the circuit is deemed to be unconditionally stable. Also, a phase margin greater than 45° at the unity gain frequency ensures that the circuit is stable for the operational frequencies [6].

3.0 DESIGN & SIMULATION RESULTS

There were two designs created using the same concept: an LNA and an LNA-Mixer. Only the LNA is discussed in this Thesis since it was the design that was integrated on CMOS, tested and found to be working in principle. The target specifications of the LNA are discussed in the next section, then the technology used and the selection of the design frequency is discussed. Sections 3.5 to 3.9 explain in detail the derivation of the equations describing the functioning of the new circuit used in the LNA and the development of the tuned amplifier. Other important features of the LNA design such as matching, noise equations, linearity and LNA architecture are discussed in sections 3.10 to 3.15. Finally, the full LNA circuit, design procedure, its functioning, trade-offs, and simulation results are discussed in sections 3.16 to 3.20.

3.1 TARGET SPECIFICATIONS

Before designing a circuit, its target specifications must be selected in order to obtain the correct parameters for the design. This LNA design is based on the 802.11a standard which the 100 MHz BW segment from 5.725 to 5.825 GHz. Table 1 shows the target specifications for the LNA design [7].

Table 1: LNA SPECIFICATIONS

Specification Type	Value range
Center Frequency	5.9 GHz to 6 GHz
Bandwidth	150MHz
Power Gain (S21)	8.5 dB
Current Consumption	< 3mA
Voltage supply	1.8V
1dB Compression Point	> -20dBm
Input referred IP3	> -14dBm
Noise Figure	< 4dB
S11	< -10dB
S22	< -10dB

3.2 Technology Used

The technology used for the LNA design in this thesis has the smallest MOSFET gate length required for good performance at the high operating frequencies. The smallest gate length MOSFET technology available at Carleton University that has well-defined simulation models is the TSMC CMOS 0.18-micrometer (micron) process. This technology requires a minimum grid spacing of 0.005 microns (μm). The documentation provided from CMC shows that the unity gain frequency for this technology is about 70 GHz and the minimum NF for a minimum-sized NMOS transistor is about 0.0005 dB.

The circuit was made using only using NMOS transistors since the electron mobility is about three times higher than that of holes [4]. Thus smaller NMOS transistors obtain the same operational frequency compared to a circuit with PMOS transistors, or both NMOS and PMOS transistors. This minimizes the size of the LNA on the layout. Also, the NMOS transistors provide a lower NF for the circuit.

3.3 Design Frequency

Although the bluetooth 802.11a wireless LAN, UNI 3 band specifications say that the center frequency of this LNA is supposed to cover 5.725 - 5.825 GHz [7], the schematic simulations were intentionally designed for a frequency band 80 to 100 MHz higher so that $f_C \approx 6\text{GHz}$.

This was done because of the original misunderstanding that parasitic capacitances and resistances were known to bring the operational frequency of an RF-circuit down by about 80 to 100MHz [4.5] after the layout of the circuit is completed. This was a mistake since the variation is up to 10% of the operational frequency [14], which means the design frequency should have been centered at 6.6 GHz instead of 6 GHz. The post layout simulations in Section 4.0 and test results in Section 5.0 clearly show this.

3.4 Identifying the Problem

The idea of replacing the inductor in the LC-tank with an Artificial or Active Inductor is not a new one. There have been several designs made using Gyrators, and active inductors [3.0]. This is usually done to replace the High-Q inductors which are large in size and difficult to implement on Integrated Circuits (ICs). Reducing silicon chip area is one of the most cost-saving goals of IC

design. Some of the main uses of inductors are in LC tank circuits. There have been many papers published on designing active-inductors which work relatively better at frequencies up to 10 GHz [15-21]. However, even these active inductors break down at frequencies higher than 10 GHz because of the parasitic capacitances intrinsic to active devices like MOSFETs and BJTs [8]. At lower frequencies, the capacitor in the LC-tank is usually too large to be put on an IC, so that it has to be put off-chip.

The main purpose of the LC tank is to store energy obtained from the current and voltage swings produced by the amplifying transistors. This energy cannot be stored perfectly because of the series and parallel resistances in the inductor and capacitor in the tank [2]. Thus there is an effect of loss in the stored energy. However the storage results in a large voltage swing required for amplification. The LC-tank in this case also acts as a resonator in the sense that the inductor produces the voltage from the change in the current swing provided by the amplifying transistor. This voltage change in turn produces the current through the capacitor in the tank, which in turn adds to the initial current through the inductor which would be quite small. The extra current produces a further voltage drop across the inductor, which in turn increases the total amplification of the amplifier without adding resistive noise in the circuit. A detailed account of the functioning of the LC-tank in the tuned amplifier is given in Section 3.5.

The above technique of using the LC-tank is useful for circuits where the size of the chip is not a concern. However, as the RF circuits become faster and require better performances from the on-chip inductors, the inductors get larger in size for better performances because they have a lower

series resistance and therefore a higher Q , and thus there is a need to reduce the size of the inductor, or to replace the LC-tank altogether.

The initial thought was to replace the inductor with passive components. Circuits were designed to test this theory but they only partially worked. The circuits did not have the drive capability of an inductor because of the parasitics, and were limited in performance due to the D.C. biasing required in MOSFETs. Appendix A describes the circuits created in these attempts to replace the inductor using passive circuit elements. The next sub-section describes the functioning of the LC-tank, the understanding of which leads to the design of the artificial tank.

3.5 The Functioning of the LC-tank in a Tuned Amplifier

In order to study and understand the currents through the capacitor and inductor in an LC-tank, and the voltages across the LC-tank, a simple common source amplifying circuit consisting of an NMOS transistor and an ideal inductor was entered into a Cadence schematic and simulated. Figure 3.1 shows the circuit, and Figure 3.2 shows the output waveforms obtained from the circuit simulation.

Figure 3.1: Simple amplifier circuit with an LC-tank.

Figure 3.2: Output wave forms of the circuit in Figure 3.1

As can be seen from the waveforms in Figure 3.2, the voltage at V_{out} reaches its minimum when the current into the Drain of transistor M2 is increasing, and the voltage at V_{out} reaches its maximum when the current through the Drain of transistor M2 is decreasing. The transient waveforms show that: $I_d = \sin\theta$, $V_{out} = -\cos\theta$ which means the current lags behind the voltage as expected. Figure 3.3 shows the flow-diagram of the current and voltages in the LC-tank in the circuit in Figure3.1.

1. $V_{in} = 0$.
2. $I_d = \text{minimum}$.
3. $V_{out} = V_{dd}$.
4. V_{in} increases
5. Channel forms
6. Current ' I_d ' flows into drain of the NMOS transistor
7. V_{out} decreases
8. when dI_d/dt is max, the voltage across L is max.
9. thus V_{out} is min @ $dI_d/dt = \text{max}$
10. dI_d/dt now decreases as I_d approaches a constant max value.
11. V_{out} now increases as voltage across L decreases due to (8).
12. dV_{out}/dt reaches max.
13. this means dV_c/dt reaches minimum, where V_c is the voltage across the capacitor.
14. the current I_c , going out of the bottom terminal of C, reaches max due to (9)
15. I_c "adds" to the value of I_d increasing it further.
16. I_d reaches max, $dI_d/dt = 0$.
17. V_c , the voltage across the capacitor, decreases as V_{out} increases to V_{dd} .
18. As V_{out} increases to maximum, dV_{out}/dt decreases, which decreases I_c into C.
19. this makes I_d to decrease as V_{out} reaches max.
20. as $dI_d/dt = \text{min}$, $V_{out} = \text{max} > V_{dd}$.
21. Now if V_{in} decreases to 0, I_d decreases to its minimum.
22. As I_d decreases, dI_d/dt approaches 0 from the negative.
23. When $I_d = \text{min}$, $V_{out} = V_{dd}$ again.
24. If V_{in} increases again, this cycle continues to repeat from #1.

Figure 3.3: List showing the functioning of an LC-tank in an common source amplifier.

The list in Figure 3.3 shows how the LC-tank works. It also shows that in step #24, if V_{in} is “in phase” with the LC-tank resonating frequency, then V_{in} would increase when I_d is minimum and $V_{out} = V_{dd}$. If V_{in} is “out-of-phase”, then V_{in} would increase at another point in time, increasing I_d before it actually reaches the minimum, thus interrupting the resonance response of the LC-tank, and therefore decreases the total power gain of the amplifying circuit. So it is important to note that this “in” or “out” of phase response is the classic behaviour of a tuned circuit. This behaviour is easily explained in the frequency domain, but not so easily explained in the time domain. This time domain explanation will be used to describe the working of the Artificial Tank.

3.6 The Artificial Tank

The requirement for the Artificial Tank was mainly driven by the need to reduce chip-area and maintain a high-Q tank circuit. There were definite costs involved, namely: a lower IP3, worse Noise performance, and higher current usage.

The perfect ideal LC-tank behaves like an oscillator or a resonator because it oscillates indefinitely once a certain amount of energy is put into it via an initial current or voltage. Real LC-resonators do not store energy indefinitely: they have loss through parallel and series parasitic resistances in the inductor and the capacitor [2]. The equivalent resistance parallel to the LC-tank is the result of two parallel resistances: the intrinsic parallel resistance of the LC-tank and the output resistance of the amplifying transistor. This is what causes the loss in the energy of the tank. In short, an LC-tank used as the load impedance for an amplifying transistor oscillates at a particular frequency when an input signal is present, and does not oscillate when there is no input signal (a requirement for stability).

Using a similar concept for the Artificial Tank, a device is required that is an oscillator by nature but does not oscillate without an input signal, for stability purposes. In electronics such a device is available: a loaded ring oscillator (RO) [9]. However, an unloaded RO oscillates “forever” like a perfect LC-tank, and this is not really desirable if it is to be used as the output impedance of a tuned circuit. So an important concept is to “stabilize” the RO by introducing a loss in the RO by connecting a resistor from one of the nodes of the RO to ground. The value of the resistor is then varied until the RO is “made stable”. Although this concept is intuitive, the equations required to represent the Artificial Tank are not simple. There are two main factors of difficulty. First, the RO is a non-linear device as it oscillates indefinitely. Second, the tuned amplifier needs a linear impedance in parallel with its transconductance, g_m , to in order to obtain the linearized amplification (e.g. $A = g_m(r_o \parallel Z_{RO})$). It is therefore imperative to describe the RO as a linear device, and as an impedance.

3.7 Ring-Oscillator (RO) as an Impedance

Starting with the original idea of the LC-tank as a resonator, it is well known that the perfect LC-tank can be represented as an impedance:

$$Z_{out} = \frac{j\omega L}{1 - \omega^2 LC} \text{ which reaches infinity as } \omega \rightarrow \frac{1}{\sqrt{LC}}. \quad (6)$$

We need to represent the RO as an impedance that will reach infinity as ω reaches its resonance frequency. Starting with the simple 1-inverter RO, the RO can be seen as an impedance in the following way. A small pulse of test current can be applied into the input/output node (since they are the same). The output voltage obtained immediately after the pulse ends is then measured. The

impedance of the RO is then simply $Z_{out} = \frac{V_{out}}{I_{in}}$. Figure 3.4 shows the idea of how the RO is represented as an impedance.

Figure 3.4: The Ring Oscillator as an impedance and Simple Small Signal MOSFET model.

Now, when the test current I_{in} is applied, a voltage is formed across the Gate to Source capacitance C_{gs} at the input of the first inverter in the RO. This voltage is determined by the input impedance of the RO, which, ignoring other the gate-to-drain and drain-to-source capacitances, is:

$$Z_{in} = \frac{1}{\frac{1}{r_o} + j\omega C_{gs}} = \frac{r_o}{1 + j\omega r_o C_{gs}}. \quad (7)$$

Here r_o is the total output resistance of the inverter. The input voltage is now $V_{in} = I_{in}Z_{in}$. The output voltage now generated depends on “A”, the amplification of the inverter which is negative. We will assume, for now, that A is frequency independant, and we will also ignore the fact that V_{out} is delayed by a time τ_d . So now V_{out} can be expressed in terms of I_{in} , Z_{out} and A as follows [4.10]:

$$V_{out} = V_{in}(-A) = I_{in}Z_{in}(-A). \quad (8)$$

$$Z_{out}(j\omega) = \frac{V_{out}}{I_{in}} = \frac{-Ar_o}{1 + j\omega r_o C_{gs}} \quad (9)$$

The resistor needed to introduce the loss in order to stabilize the RO can be connected as shown in Figure 3.5.

Figure 3.5: Damped Ring Oscillator as an impedance.

The new output impedance becomes $Z'_{out} = Z_{out} || R_L$. Calculating this gives:

$$Z'_{out}(j\omega) = \frac{1}{\frac{1}{\frac{-Ar_o}{1 + j\omega r_o C_{gs}}} + \frac{1}{R_L}} \quad (10)$$

$$= \frac{-Ar_o R_L}{R_L - Ar_o + j\omega r_o R_L C_{gs}} \quad (11)$$

$$= \frac{\frac{A}{C_{gs}}}{\frac{Ar_o - R_L}{r_o R_L C_{gs}} + j\omega} \quad (12)$$

This is in the frequency or ω domain. In the time domain, this equation becomes:

$$Z'_{out}(t) = u(t) \frac{A}{C_{gs}} \left[e^{-t \left(\frac{Ar_o - R_L}{r_o R_L C_{gs}} \right)} \right]. \quad (13)$$

Equation (12) clearly shows that if R_L is greater than Ar_o , then the exponential part of the new impedance becomes infinite, and thus the $RO \parallel R_L$ circuit is unstable. However, if R_L is less than Ar_o , then $Z'_{out}(t)$ decreases to zero with time, showing that the $RO \parallel R_L$ circuit is stable. How quickly the circuit stabilizes depends on how large the value of $r_o R_L C_{gs}$ is.

It was originally assumed that the amplification of the inverter is independent of frequency or ω and that there was no time-delay τ_d between V_{out} and I_{in} . These assumptions are very “crude” and are insufficient for proper calculations or understanding. The actual amplification can only be derived in the frequency domain if the RO response can be linearized and its impedance calculated using the linear characterization, and then calculating the new impedance $Z_{RO} \parallel R_L$.

The most difficult part of this theory is to “linearize” a non-linear device for the purpose of calculating its frequency response to a small signal input. Once this is done, the linear-model can be used to quickly hand-calculate the parameters needed to design the tuned amplifier.

3.8 Linearization of the Ring Oscillator

3.8.1 The Discrete frequency response of the RO

By nature, the RO is non-linear and continuously oscillates at its resonance frequency which is

given by $\omega_o = \frac{2\pi}{2\tau_d} = \frac{\pi}{\tau_d}$ where τ_d (in seconds) is the time delay between the input and

output of the inverter(s) in the RO. The waveform can be approximated as unit-steps multiplied by a decaying exponential as shown in the equations (14-18) used in Mathematica below. Here, “m” is the total time of the simulation, and “y” is the output voltage of the RO. Figure 3.6 shows one period of the waveform obtained from these equations.

$$m=2; \quad (14)$$

$$\tau_d = 1; \quad (15)$$

$$k = 5; \quad (16)$$

$$y = \sum_{n=0}^m (-1)^n \text{UnitStep}[t - n\tau_d](1 - \text{Exp}[-k(t - n\tau_d)]) \quad (17)$$

$$\text{Plot}[y, \{t, 0, m\}]; \quad (18)$$

Here $k = \frac{1}{RC}$, and RC is the time constant formed by the output resistance of the RO and the

total capacitance formed by $C_{gs}||C_{ds}$. Also, u(t) is the unit-step function.

Figure 3.6: One period of the resulting waveform from equation (17).

This continuous waveform can be represented in the frequency or ω domain by representing the continuous wave as a fourier series as shown in equation (19) below:

$$V_{out} = c_o + c_n \sum_{n=-\infty}^{\infty} e^{jn\omega_o t}. \quad (19)$$

Here, $c_n = c_{n1} + c_{n2}$ and $c_o = c_{o1} + c_{o2}$.

Calculating the first constant:

$$c_{n1} = \frac{1}{2\tau_d} \int_0^{\tau_d} (1 - e^{-kt}) e^{-jn\omega_o t} dt \quad (20)$$

$$= \frac{1}{2\tau_d} \left(\int_0^{\tau_d} e^{-jn\omega_o t} dt - \int_0^{\tau_d} e^{-t(k+jn\omega_o)} dt \right) \quad (21)$$

Integrating, we get:

$$c_{n1} = \frac{1}{2\tau_d} \left(\frac{e^{-jn\omega_o t}}{-jn\omega_o} \Big|_0^{\tau_d} - \frac{e^{-t(k+jn\omega_o)}}{k+jn\omega_o} \Big|_0^{\tau_d} \right) \quad (22)$$

Substituting the limits, we get:

$$c_{n1} = \frac{1}{2\tau_d} \left(\frac{e^{-jn\omega_o \tau_d}}{-jn\omega_o} - \frac{1}{-jn\omega_o} - \left(\frac{e^{-\tau_d(k+jn\omega_o)}}{k+jn\omega_o} - \frac{1}{k+jn\omega_o} \right) \right) \quad (23)$$

$$= \frac{1}{2\tau_d} \left(\frac{1 - e^{-jn\omega_o \tau_d}}{jn\omega_o} + \frac{1 - e^{-\tau_d(k+jn\omega_o)}}{k+jn\omega_o} \right). \quad (24)$$

Calculating the second constant:

$$c_{n2} = \frac{1}{2\tau_d} \int_{\tau_d}^{2\tau_d} (e^{-k(t-\tau_d)}) e^{-jn\omega_o t} dt \quad (25)$$

$$= \frac{e^{k\tau_d}}{2\tau_d} \int_{\tau_d}^{2\tau_d} e^{-t(jn\omega_o + k)} dt \quad (26)$$

Integrating we get:

$$c_{n2} = \frac{e^{k\tau_d}}{2\tau_d} \left[\frac{e^{-t(jn\omega_o + k)}}{-(jn\omega_o + k)} \right] \Bigg|_{\tau_d}^{2\tau_d} \quad (27)$$

$$= \frac{e^{k\tau_d}}{2\tau_d} \left[\frac{e^{-2\tau_d(jn\omega_o + k)} - e^{-\tau_d(jn\omega_o + k)}}{-(jn\omega_o + k)} \right] \quad (28)$$

$$= \frac{1}{2\tau_d} \left[\frac{e^{-k\tau_d} - e^{-jn\omega_o\tau_d}}{-(jn\omega_o + k)} \right]. \quad (29)$$

Now the D.C. components are:

$$c_{o1} = \frac{1}{2\tau_d} \int_0^{\tau_d} [1 - e^{-kt}] dt \quad (30)$$

$$= \frac{1}{2\tau_d} \left[t + \frac{e^{-kt}}{k} \right] \Bigg|_0^{\tau_d} \quad (31)$$

$$= \left(\frac{1}{2} + \frac{e^{-k\tau_d}}{2k\tau_d} \right) \quad (32)$$

and

$$c_{o2} = \frac{1}{2\tau_d} \int_{\tau_d}^{2\tau_d} e^{-k(t-\tau_d)} dt \quad (33)$$

$$= \frac{e^{k\tau_d}}{2\tau_d} \left[-\frac{e^{-kt}}{k} \right] \bigg|_{\tau_d}^{2\tau_d} \quad (34)$$

$$= \frac{1 - e^{-k\tau_d}}{2k\tau_d} \quad (35)$$

$$\therefore c_o = c_{o1} + c_{o2} \quad (36)$$

$$= \left(\frac{1}{2} + \frac{1}{2k\tau_d} \right) \quad (37)$$

At $t = 2\tau_d$, $V_{out} = c_o + c_n$, which is entirely in the $n\omega_o$ domain, i.e. the frequency domain, and this series can be plotted using the following Matlab program:

```
k=5; td=1; w=pi/td;
%co=0.5 + (0.5)*(1/k*td);
n=[0:100];
cn1=((1-exp(-i*pi.*n))./(i*w.*n) + (1-exp(-td*(k+(i*pi.*n))))./(k + i*w*n))/(2*td);
cn2=(((-exp(-td*(k+(2*i*pi.*n)))+exp(-i*pi.*n))./(k + i*w*n))/(2*td);
y=abs(co+cn1 + cn2);
stem(n,y); grid %gives magnitude of Cn = Cn1 + Cn2
r=real(cn1 + cn2);
x=imag(cn1 + cn2);
d=360*(1/(2*pi))*atan(x./r);
stem(n,d); grid %gives phase of Cn = Cn1 + Cn2
```

The plots generated from the program above are shown below. Ignoring the D.C. component c_0 , the program above generates the plot in frequency component magnitude shown in Figure 3.7 and the phase component shown in Figure 3.8.

Figure 3.7: Plot for the magnitude of the frequencies.

The plot in Figure 3.7 shows the discrete nature of the spectrum generated by the Fourier Series, with the first harmonic = ω_o at $n=1$, which has the highest amplitude. Thus ω_o is the natural resonant frequency of the RO.

Figure 3.8: The plot generated by the program shows the Phase of the Fourier Series

The plot in Figure 3.8 shows how all the $n = \text{even}$ harmonic frequencies have different phases because they need to cancel each other as “ n ” increases. On the other hand, the $n = \text{odd}$ are all in phase so the amplitudes add up to give the characteristic output waveform of a Ring Oscillator.

The plots in Figure 3.7 and 3.8 show the discrete nature of the spectrum. The discrete spectrum in frequency implies it is piece-wise continuous in time, and therefore non-linear. This non-linear nature arises from the fact that this waveform is piece-wise continuous and does not begin or end at any point in time. As a result, the Fourier series representation having a discrete spectrum of

V_{out} is not sufficient to describe the behaviour of the RO as an impedance, or to obtain the linear representation of the RO's output waveform in the frequency domain that would show its function as an artificial tank.

However, it is known that the RO does not begin to oscillate unless there is a small disturbance or variation in the output or input current of the inverter(s). This means that there is a specific moment in time that the RO begins to oscillate when there is a small variation in the current or voltage at its input or output node (which may be the same if an RO with only one inverter is used). This fact can now be used to obtain a continuous frequency response of the RO.

3.8.2 The Continuous Frequency response of the RO

The method used to “linearize” the RO output waveform is done in the following way: instead of characterizing the output waveform as a Fourier series of a single period of the waveform, the waveform is characterized as an infinite sum of time-delayed unit-step functions multiplied by the waveform shape, with each time delay equal to τ_d , and the Fourier transform of the resulting function is taken to give a continuous linear spectrum. This characterization implies that the waveform begins or starts at a specific point in time: $t = 0$. Before this, the output is assumed to be $V_{out} = 0$. This assumption is more realistic than the assumption of a continuous waveform that begins at negative infinity and continues to positive infinity.

The equation (38) best represents the waveform characterization (here $u(t)$ = unit-step function):

$$V_{out} = u(t)[1 - e^{-kt}] - u(t - \tau_d)[1 - e^{-k(t - \tau_d)}] + u(t - 2\tau_d)[1 - e^{-k(t - 2\tau_d)}] - \dots \quad (38)$$

$$= \sum_{n=0}^{\infty} (-1)^n u(t - n\tau_d) [1 - e^{-k(t - n\tau_d)}] \quad (39)$$

$$= \left(\sum_{n=0}^{\infty} (-1)^n u(t - n\tau_d) - \sum_{n=0}^{\infty} (-1)^n u(t - n\tau_d) (-e^{-k(t - n\tau_d)}) \right). \quad (40)$$

Now the Fourier Transform of the above sum gives the following equation:

$$V_{out}(j\omega) = \sum_{n=0}^{\infty} (-1)^n \left[\pi\delta(\omega) + \frac{1}{j\omega} \right] e^{-j\omega n\tau_d} - \sum_{n=0}^{\infty} (-1)^n \left[\frac{e^{-j\omega n\tau_d}}{j\omega + k} \right] \quad (41)$$

It can be seen, by intuition, that the representation above does not give the highest amplitude at the resonant frequency of ω_o . However, there is a “hidden” variable in the above equation, that can be used to provide the necessary “frequency shift” required to give the highest amplitude at the resonant frequency. This is $(-1)^n$ which can be represented as $e^{-jn\pi}$ as can be seen in the equations below:

$$V_{out}(j\omega) = \sum_{n=0}^{\infty} \left[\pi\delta(\omega) + \frac{1}{j\omega} \right] e^{-j\omega n\tau_d - jn\pi} - \sum_{n=0}^{\infty} \left[\frac{e^{-j\omega n\tau_d - jn\pi}}{j\omega + k} \right] \quad (42)$$

But we know that:

$$\omega_o = \frac{2\pi}{2\tau_d} = \frac{\pi}{\tau_d}. \quad (43)$$

$$\tau_d = \frac{\pi}{\omega_o} \quad (44)$$

Hence:

$$V_{out}(j\omega) = \sum_{n=0}^{\infty} \left[\pi\delta(\omega) + \frac{1}{j\omega} \right] e^{-\frac{j\omega n\pi}{\omega_o} - jn\pi} - \sum_{n=0}^{\infty} \left[\frac{e^{-\frac{j\omega n\pi}{\omega_o} - jn\pi}}{j\omega + k} \right] \quad (45)$$

$$= \sum_{n=0}^{\infty} \left[\pi\delta(\omega) + \frac{1}{j\omega} \right] e^{-jn\pi \left(\frac{\omega}{\omega_o} + 1 \right)} - \sum_{n=0}^{\infty} \left[\frac{e^{-jn\pi \left(\frac{\omega}{\omega_o} + 1 \right)}}{j\omega + k} \right] \quad (46)$$

$$= \sum_{n=0}^{\infty} \left[\pi\delta(\omega) + \frac{1}{j\omega} \right] e^{-jn\pi \left(\frac{\omega + \omega_o}{\omega_o} \right)} - \sum_{n=0}^{\infty} \left[\frac{e^{-jn\pi \left(\frac{\omega + \omega_o}{\omega_o} \right)}}{j\omega + k} \right] \quad (47)$$

From here it can be seen that the magnitude of $e^{-jn\pi \left(\frac{\omega + \omega_o}{\omega_o} \right)}$ reaches a maximum when

$\omega = \omega_o$. Furthermore, the infinite series in the above equation can be represented analytically

because of the following mathematical property: (48)

$$\sum_{n=0}^{\infty} x^n = 1 + x + x^2 + x^3 + x^4 + \dots = \frac{1}{1-x}. \quad (49)$$

Hence:

$$V_{out}(j\omega) = \left[\pi\delta(\omega) + \frac{1}{j\omega} \right] \sum_{n=0}^{\infty} e^{-jn\pi\left(\frac{\omega+\omega_o}{\omega_o}\right)} - \frac{1}{j\omega+k} \sum_{n=0}^{\infty} e^{-jn\pi\left(\frac{\omega+\omega_o}{\omega_o}\right)} \quad (50)$$

$$= \left[\pi\delta(\omega) + \frac{1}{j\omega} - \frac{1}{j\omega+k} \right] \sum_{n=0}^{\infty} e^{-jn\pi\left(\frac{\omega+\omega_o}{\omega_o}\right)} \quad (51)$$

$$= \left[\pi\delta(\omega) + \frac{1}{j\omega} - \frac{1}{j\omega+k} \right] \left(\frac{1}{1 - e^{-j\pi\left(\frac{\omega+\omega_o}{\omega_o}\right)}} \right) \quad (52)$$

$$= \left[\pi\delta(\omega) + \frac{k}{j\omega(j\omega+k)} \right] \left(\frac{e^{j\pi\left(\frac{\omega+\omega_o}{\omega_o}\right)}}{e^{j\pi\left(\frac{\omega+\omega_o}{\omega_o}\right)} - 1} \right). \quad (53)$$

It can now be seen that as $\omega \rightarrow \omega_o$,

$$V_{out} \rightarrow \infty, \text{ because the denominator } \left(e^{j\pi\left(\frac{\omega+\omega_o}{\omega_o}\right)} - 1 \right) \rightarrow 0.$$

However, equation (53) is not entirely true, since the RO is non-linear, and $V_{out} \leq V_{dd}$ instead of infinity at the resonance frequency ω_o . So, the “linearized” form of the RO can now be represented as an impedance in the following manner:

$$Z_{out}(j\omega) = \frac{V_{out}(j\omega)}{I_{in}(j\omega)} \quad (54)$$

where $Z_{out}(j\omega)$ is the impedance of the RO and $I_{in}(j\omega)$ is a small pulse of test current that is inserted into the gate of the inverter to obtain V_{out} . This pulse can be represented in the frequency domain as the Fourier Transform of $u(t) - u(t - t_d)$ in time domain, which would be:

$$I_{in}(j\omega) = \left[\pi\delta(\omega) + \frac{1}{j\omega} \right] - \left(\pi\delta(\omega) + \frac{1}{j\omega} \right) e^{-j\omega\tau_d}. \quad (55)$$

Now the output impedance $Z_{out}(j\omega)$ can be plotted using a program like Matlab or Mathematica.

The equations shown in Figure 3.9 on the next page were entered into Mathematica to plot $Z_{out}(j\omega)$ and the Voltage Gain. These are shown in Figure 3.10 and Figure 3.11 respectively. The plot in Figure 3.11 was obtained using $g_m = 0.004 = 4\text{mS}$


```

w = 2 π 6 × 109
m =  $\frac{\omega}{w} + 1$ 
k = 2 π 6 × 109
ro = 1000
Zamp =  $\frac{ro}{i \frac{\omega}{k} + 1}$ 

theVoutRO =  $\left( \pi \text{DiracDelta}[\omega] + \frac{k}{(i \omega + k)(i \omega)} \right) \left( \frac{e^{i \pi m}}{(e^{i \pi m} - 1)} \right)$ 

theIinRO =  $\pi \text{DiracDelta}[w] + \frac{1}{i \omega} - \left( \pi \text{DiracDelta}[w] + \frac{1}{i \omega} \right) e^{-i \omega / (w)}$ 

ZoutRO =  $-\frac{\text{theVoutRO}}{0.1 \text{theIinRO}}$ 

z =  $\left( \frac{Zamp ZoutRO}{Zamp + ZoutRO} \right)$ 

Plot[Abs[z], {w, w - 0.01 w, w + 0.01 w}]
Plot[20 Log[0.004 Abs[z]], {w, w - 0.01 w, w + 0.01 w}]

```

Figure 3.9: Equations in Mathematica.

Note that only $0.1 \times$ “theIinRO” is used to “start” the RO. This means the RO has a D.C. gain of

$\frac{1}{0.1} = 10$. Also note that the resistor is now replaced by the output impedance of the MOSFET

connected in its place, Zamp. Here “z” is the total impedance, i.e. Zamp||ZoutRO.

Figure 3.10: Plot showing $|Z_{out}(j\omega)|$ at 6 GHz frequency within a 120 MHz BW.

Figure 3.11: Plot showing $\text{Gain} = 20 \text{ Log}\{g_m Z_{out}(j\omega)\}$ at 6 GHz frequency, BW=120 MHz.

3.9 The Single-Ended Tuned Amplifier

The resistor R_L (shown in Figure 3.5) is now replaced by a NMOS transistor (call it M1) biased in saturation with R_{ds} equal to the resistor value, to provide the same amount of stability in the RO. Finally a signal is applied to the gate of M1 and the result is a tuned amplifier with a voltage gain of about 18 dB. Figure 3.12 shows the schematic of a tuned amplifier using an AT. Figure 3.13 shows the small signal voltage gain of the tuned amplifier.

Figure 3.12: Tuned Amplifier.

Figure 3.13: Small-Signal Gain of the Tuned Amplifier shown in Figure 3.12

It is now clearly seen how the RO acts like a AT for this transistor. With proper input matching in order to provide the lowest noise figure (NF), this circuit can be converted into a Low Noise Amplifier (LNA).

3.10 Noise Figure and Input Matching

There is a direct contradiction between the trying to match a circuit for maximum power transfer and for the minimum noise figure [4.8]. The reason is that when a circuit's input is matched for the maximum power transfer from a 50-ohm load, the input impedance looks like 50-ohms, reducing the small-signal input voltage. This reduces the Voltage Gain of the LNA because the small-signal output voltage (v_o) is a square function of the input voltage (v_i), according to the NMOS current equations described in Appendix B. This also increases the noise figure of the circuit, since the NF is a ratio of the input and output Signal to Noise Ratios (SNR_i/SNR_o), and the SNR_i is lower when the input voltage is lower. Thus the maximum gain and minimum NF is obtained when the input impedance is much higher [4.9]. Therefore it is almost impossible to obtain both perfect input matching and the minimum NF at the same time.

On the other hand, it is possible to obtain both perfect input matching and the minimum NF at the same time by using two circuits: the first one to provide perfect input matching, and the second one to provide the best Gain, NF and output matching. This was not done in this design in order to reduce the current consumption and thus reduce D.C. power consumption.

It is important to note that unlike the LNA using an LC-tank at its output, the input impedance of the LNA using an Artificial Tank does not “see” a negative resistance [4.10], and thus there is no

need to use the source or emitter inductor (L_s or L_e) in order to provide a positive match-able impedance. The reason is that in the LNA using an LC-tank, the amplifying transistor provides extra energy to increase the equivalent parallel resistance of the tank, while in the LNA using the Artificial Tank, the amplifying transistor provides the energy loss so that the tank does not oscillate indefinitely.

Also, in the case of the LNA with the LC-tank, there is high-energy output because of the large currents that flow through the inductor during the voltage swings at the drain or collector of the amplifying transistor, thus causing the LC-tank to store more energy than required by the voltage swing at the output. This extra stored energy in the LC-tank causes a feedback through the C_{gd} of M_2 shown in Figure 3.1, making the input look like a negative resistance. However, because the Artificial Tank is voltage driven, and has no excess energy stored in it during the oscillations, the feedback through C_{gd} does not occur. This, then facilitates the LNA using the AT to have no need for an L_e or L_s for positive impedance matching.

3.11 General Noise Equations

Some of the equations describing the Noise Figure of a NMOS transistor are shown below:

The equation (56) shows how increasing the unity gain frequency ω_T reduces the NF [4].

$$NF_{min} = 1 + 2 \sqrt{\frac{\delta\gamma}{5}(1 - |c|^2)} \left(\frac{\omega}{\omega_T} \right) \quad (56)$$

The equation (57) shows how increasing g_m and decreasing C_{gs} decreases NF. The only way to increase g_m is to increase the W/L ratio of the input diff-pair transistors. However, doing this also

increases C_{gs} because $C_{gs} = (2/3)WLC_{ox}$. This in turn increases the NF. Thus, there is a balance between increasing the widths of input diff-pair transistors and the increasing g_m .

$$NF_{min} = 1 + \frac{2\gamma R_s \omega_o^2 C_{gs}^2}{g_m} \quad (57)$$

The equation (58) shows how the minimum NF is obtained when G_{opt} and B_{opt} , which are part of the optimal admittance of the input diff-pair ($Y_{opt} = G_{opt} + jB_{opt}$), are equal to the source admittance $Y_s = G_s + jB_s$:

$$NF = NF_{min} + \frac{R_s}{G_s} [(G_s - G_{opt})^2 + (B_s - B_{opt})^2] \quad (58)$$

where:

$$G_{opt} = \alpha \omega C_{gs} \sqrt{\frac{\delta\gamma}{5} (1 - |c|^2)} \quad (59)$$

and:

$$B_{opt} = \omega C_{gs} \left(1 + \alpha \sqrt{\frac{\delta\gamma}{5}} |c| \right) \quad (60)$$

Here, $|c|$ is the noise correlation coefficient, and γ is the excess MOSFET noise factor. These equations show how G_{opt} and B_{opt} can be obtained, and how these values are related to C_{gs} .

3.12 Noise Sources in the RO Amplifier

3.12.1 Derivation of output Noise Figure

The total noise generated by an LNA with an active load is extremely complicated to describe. However, in order to show the complexity of derivation of the equations, the Noise Equations for

the active load circuit shown in the small-signal diagram of Figure 3.14 were derived. Here the load of the amplifying transistor(s) is the RO consisting of active loads in a feedback configuration. Figure 3.14 shows the small signal (SS) diagram of the Common Source Differential-Pair with a diode-connected active-load having some of the noise sources in the circuit.

Here the Thermal Noise is caused by the vibration of electrons in resistive materials [4], and the Shot Noise is caused by the random movement of electrons in PN-junctions when the channel is not completely formed in the NMOS transistor. From the small signal diagram shown above, the noise in the circuit can be reduced by reducing the gate resistance R_g , the output resistance of the input diff-pair, r_{o1} , the equivalent series resistance which can be part of the source inductor, and finally the output resistance of the output diff-pair r_{o2} .

Figure 3.14: Small Signal diagram of the Common Source Differential-Pair with an active-load.

The Noise Equations derived from the Figure 3.14 are shown below:

Let the Input Resistance be represented by R_{g1}' :

$$R_{g1}' = R_{g1} + \frac{1}{j\omega C_{gs1}} + R_s \quad (61)$$

V_{n1} can be given as:

$$V_{n1} = \sqrt{4KTB R_{g1}'} \quad (62)$$

The Input Current to the amplifying transistor gives:

$$\frac{V_{gs1}}{1/j\omega C_{gs1}} = \frac{V_{n1} - V_x}{R_{g1}'} \quad (63)$$

Hence:

$$V_{gs1} = \frac{V_{n1} - V_x}{j\omega C_{gs1} R_{g1}'} \quad (64)$$

The Input Current to the active load gate gives:

$$\frac{V_{gs2}}{1/(j\omega C_{gs2})} = \frac{V_y}{R_{g2} + (1/(j\omega C_{gs2}))} \quad (65)$$

Hence:

$$V_{gs2} = \frac{V_y}{1 + j\omega R_{g2} C_{gs2}} \quad (66)$$

Kirchoffs Current Laws at node V_y gives:

$$\frac{V_{out} - V_y}{R_{s2}} = \frac{V_y j\omega C_{gs2}}{1 + j\omega R_{g2} C_{gs2}} + g_{m2} V_{gs2} + \frac{V_y}{r_{o2}} \quad (67)$$

$$= V_y \left[\frac{j\omega C_{gs2}}{1 + j\omega R_{g2} C_{gs2}} + \frac{g_{m2}}{1 + j\omega R_{g2} C_{gs2}} + \frac{1}{r_{o2}} \right] \quad (68)$$

or:

$$\therefore V_y = \frac{V_{out}}{1 + R_{s2} \left[\frac{g_{m2} + j\omega C_{gs2}}{1 + j\omega R_{g2} C_{gs2}} + \frac{1}{r_{o2}} \right]} \quad (69)$$

$$\approx \frac{V_{out}}{1 + g_{m2} R_{s2}} \quad (70)$$

$$\text{since } j\omega C_{gs2} \approx 0 \text{ and } \frac{1}{r_{o2}} \approx 0. \quad (71)$$

Substituting (64) for V_{gs1} and calculating the KCL at node V_x gives:

$$\frac{V_x}{R_{s1}} = \frac{g_{m1}(V_{n1} - V_x)}{j\omega C_{gs1} R_{g1}'} + \frac{V_{out} - V_x}{r_{o1}} + \frac{V_{n1} - V_x}{R_{g1}'} \quad (72)$$

Hence:

$$V_x = \frac{\frac{V_{n1}}{R_{g1}'} + \frac{g_{m1} V_{n1}}{j\omega C_{gs1} R_{g1}'} + \frac{V_{out}}{r_{o1}}}{\frac{1}{R_{s1}} + \frac{1}{R_{g1}'} + \frac{g_{m1}}{j\omega C_{gs1} R_{g1}'} + \frac{1}{r_{o1}}} \quad (73)$$

$$= \frac{V_{n1} \left(\frac{g_{m1} + j\omega C_{gs1}}{j\omega C_{gs1} R_{g1}'} \right) + \frac{V_{out}}{r_{o1}}}{k_o} \quad (74)$$

$$\approx \frac{\frac{g_{m1} V_{n1}}{j\omega C_{gs1} R_{g1}'} + \frac{V_{out}}{r_{o1}}}{k_o} \quad (75)$$

where:

$$k_o = \frac{1}{R_{s1}} + \frac{j\omega C_{gs1} + g_{m1}}{j\omega C_{gs1} R_{g1}'} + \frac{1}{r_{o1}} \quad (76)$$

$$\approx \frac{1}{R_{s1}} + \frac{g_{m1}}{j\omega C_{gs1} R_{g1}'} \quad (77)$$

since:

$$\frac{1}{r_{o1}} \approx 0 \text{ and } j\omega C_{gs1} \approx 0. \quad (78)$$

Now substituting (75) into (64), we get:

$$V_{gs1} = \frac{V_{n1} k_o - \left(\frac{V_{n1} (j\omega C_{gs1} + g_{m1})}{j\omega C_{gs1} R_{g1}'} + \frac{V_{out}}{r_{o1}} \right)}{j\omega C_{gs1} R_{g1}' \left(\frac{1}{R_{s1}} + \frac{g_{m1}}{j\omega C_{gs1} R_{g1}'} \right)} \quad (79)$$

$$= \frac{V_{n1} \left(k_o - \frac{j\omega C_{gs1} + g_{m1}}{j\omega C_{gs1} R_{g1}'} \right) - \frac{V_{out}}{r_{o1}}}{\frac{j\omega C_{gs1} R_{g1}'}{R_{s1}} + g_{m1}} \quad (80)$$

$$\frac{\frac{V_{n1}}{R_{s1}} - \frac{V_{out}}{r_{o1}}}{g_{m1}} \quad (81)$$

KCL at V_{out} gives:

$$g_{m1}V_{gs1} + \frac{V_{out} - V_x}{r_{o1}} = \frac{V_{out} - V_y}{R_{s2}} \quad (82)$$

$$\frac{V_{n1}}{R_{s1}} - \frac{V_{out}}{r_{o1}} + \frac{V_{out} - \left(\frac{g_{m1}V_{n1}}{j\omega C_{gs1}R_{g1}'} + \frac{V_{out}}{r_{o1}} \right)}{\frac{1}{R_{s1}} + \frac{g_{m1}}{j\omega C_{gs1}R_{g1}'}} = \frac{V_{out} - \frac{V_{out}}{1 + g_{m2}R_{s2}}}{R_{s2}} \quad (83)$$

$$\frac{V_{n1}}{R_{s1}} - \frac{\left(\frac{g_{m1}V_{n1}}{j\omega C_{gs1}R_{g1}'} + \frac{V_{out}}{r_{o1}} \right)}{r_{o1} \left(\frac{1}{R_{s1}} + \frac{g_{m1}}{j\omega C_{gs1}R_{g1}'} \right)} = \frac{V_{out} - \frac{V_{out}}{1 + g_{m2}R_{s2}}}{R_{s2}} \quad (84)$$

$$V_{out} = \frac{\frac{V_{n1}}{R_{s1}} - \frac{\frac{g_{m1}V_{n1}}{j\omega C_{gs1}R_{g1}'}}{r_{o1} \left(\frac{1}{R_{s1}} + \frac{g_{m1}}{j\omega C_{gs1}R_{g1}'} \right)}}{\frac{1}{r_{o1}^2 \left(\frac{1}{R_{s1}} + \frac{g_{m1}}{j\omega C_{gs1}R_{g1}'} \right)} + \frac{1 - \frac{1}{1 + g_{m2}R_{s2}}}{R_{s2}}} \quad (85)$$

$$\frac{V_{n1}}{R_{s1}} - \frac{\frac{g_{m1} V_{n1}}{j\omega C_{gs1} R_{g1}'}}{r_{o1} \left(\frac{1}{R_{s1}} + \frac{g_{m1}}{j\omega C_{gs1} R_{g1}'} \right)} \approx \frac{1}{\frac{1}{R_{s2}}} \quad (86)$$

since:

$$\frac{1}{\frac{2}{r_{o1}}} \approx 0 \text{ and } \frac{1}{j\omega C_{gs1}} \approx \infty, \text{ and } 1 - \frac{1}{1 + g_{m2} R_{s2}} = \frac{g_{m2} R_{s2}}{1 + g_{m2} R_{s2}} \approx 1 \quad (87)$$

$$V_{out} = V_{n1} \left(\frac{R_{s2} r_{o1} \left(\frac{1}{R_{s1}} + \frac{g_{m1}}{j\omega C_{gs1} R_{g1}'} \right) - \frac{R_{s2} R_{s1} g_{m1}}{j\omega C_{gs1} R_{g1}'}}{R_{s1} r_{o1} \left(\frac{1}{R_{s1}} + \frac{g_{m1}}{j\omega C_{gs1} R_{g1}'} \right)} \right) \quad (88)$$

$$= V_{n1} \left(\frac{j\omega C_{gs1} R_{g1}' R_{s2} r_{o1} + (r_{o1} - R_{s1}) R_{s2} R_{s1} g_{m1}}{r_{o1} R_{s1} (j\omega C_{gs1} R_{g1}' + R_{s1} g_{m1})} \right) \quad (89)$$

$$\approx V_{n1} \left(\frac{j\omega C_{gs1} R_{g1}' R_{s2} r_{o1} + (r_{o1} - R_{s1}) R_{s2} R_{s1} g_{m1}}{r_{o1} R_{s1}^2 g_{m1}} \right) \quad (90)$$

$$\approx V_{n1} \left(\frac{j\omega C_{gs1} R_{g1}' R_{s2}}{R_{s1}^2 g_{m1}} + \frac{R_{s2}}{R_{s1}} \right) \quad (91)$$

since:

$$j\omega C_{gs1} R_{g1}' \approx 0 \text{ and } (r_{o1} - R_{s1}) \approx r_{o1} \text{ because } r_{o1} \gg R_{s1}. \quad (92)$$

This shows the direct dependency of the output noise voltage to C_{gs1} , the input impedance R'_{g1} , and inverse dependency to the amplifying transistor's transconductance g_{m1} . This V_{out} is equivalent to V_{on1} which is the output noise voltage caused by the thermal noise of R_{g1} .

Now the output noise voltage caused by source resistance, R_s , is:

$$V_{ons} = \frac{V_{out}}{V_{n1}} \times V_{ns} \quad (93)$$

where: (94)

$$V_{ns} = \sqrt{4KTBR_s} \quad (95)$$

Now use super-position to calculate V_{ons1} , the output noise voltage due to R_{s1} , by setting V_{n1} and V_{ns} equal to zero:

$$-V_{gs1} = \frac{V_{ns1}}{j\omega C_{gs1} R_{g1}}, \quad (96)$$

KCL at V_x gives:

$$\frac{V_{ons1} - V_{ns1}}{r_{o1}} + g_{m1} V_{gs1} = \frac{V_{ns1}}{R_{s1}} \quad (97)$$

$$\frac{V_{ons1} - V_{ns1}}{r_{o1}} - \frac{g_{m1} V_{ns1}}{j\omega C_{gs1} R_{g1}} = \frac{V_{ns1}}{R_{s1}} \quad (98)$$

Hence:

$$V_{ons1} = V_{ns1} r_{o1} \left(\frac{1}{r_{o1}} + \frac{g_{m1}}{j\omega C_{gs1} R_{g1}} + \frac{1}{R_{s1}} \right) \quad (99)$$

where:

$$V_{ns1} = \sqrt{4KTB R_{s1}} \quad (100)$$

Again, use super-position to calculate V_{on2} , the output noise voltage due to R_{g2} , setting V_{n1} , V_{ns} , and V_{ns1} equal to zero, the noise voltage at V_y due to R_{g2} is given by the voltage divider:

$$\frac{V_y R_{g2}}{R_{g2} + (1/j\omega C_{gs2})} = V_{n2} \quad (101)$$

$$V_y - V_{n2} = V_{n2} \left(\frac{1}{j\omega C_{gs2} R_{g2}} \right) \quad (102)$$

Hence:

$$V_y = \frac{V_{n2}}{R_{g2}} \left(R_{g2} + \frac{1}{j\omega C_{gs2}} \right) \quad (103)$$

where:

$$V_{n2} = \sqrt{4KTB R_{g2}}. \quad (104)$$

Now KCL at V_y gives:

$$\frac{V_{on2} - V_y}{R_{s2}} = \frac{V_y - V_{n2}}{(1/j\omega C_{gs2})} + \frac{V_y}{r_{o2}} + g_{m2}(V_y - V_{n2}) \quad (105)$$

Substituting (103) into (105) gives:

$$\frac{V_{on2} - V_{n2} \left(1 + \frac{1}{j\omega R_{g2} C_{gs2}} \right)}{R_{s2}} = \frac{V_{n2} \left(\frac{1}{j\omega C_{gs2} R_{g2}} \right)}{(1/j\omega C_{gs2})} + \frac{V_{n2} \left(1 + \frac{1}{j\omega R_{g2} C_{gs2}} \right)}{r_{o2}} + g_{m2} V_{n2} \left(\frac{1}{j\omega C_{gs2} R_{g2}} \right) \quad (106)$$

$$\frac{V_{on2} - V_{n2} \left(1 + \frac{1}{j\omega R_{g2} C_{gs2}} \right)}{R_{s2}} = \frac{V_{n2}}{R_{g2}} + \left(\frac{V_{n2}}{r_{o2}} + g_{m2} V_{n2} \right) \left(\frac{1}{j\omega R_{g2} C_{gs2}} \right) + \frac{V_{n2}}{r_{o2}} \quad (107)$$

Hence:

$$V_{on2} = V_{n2}R_{s2} \left(\frac{1}{R_{g2}} + \left(\frac{1}{r_{o2}} + g_{m2} \right) \left(\frac{1}{j\omega R_{g2}C_{gs2}} \right) + \frac{1}{r_{o2}} + \frac{\left(1 + \frac{1}{j\omega R_{g2}C_{gs2}} \right)}{R_{s2}} \right) \quad (108)$$

Now, since $\frac{1}{r_{o1}} \approx 0$:

$$V_{on2} \approx V_{n2}R_{s2} \left(\frac{1}{R_{g2}} + \frac{g_{m2}}{j\omega R_{g2}C_{gs2}} + \frac{1}{R_{s2}} \left(1 + \frac{1}{j\omega R_{g2}C_{gs2}} \right) \right) \quad (109)$$

Finally, neglecting the noise voltages from r_{o1} , r_{o2} and R_{s2} , (because these are not amplified) the total output noise power becomes:

$$V_{on}^2 = V_{on1}^2 + V_{on2}^2 + V_{ons1}^2 \quad (110)$$

and the Noise Figure of the amplifier is:

$$NF = \frac{V_{on}^2}{V_{ons}^2}. \quad (111)$$

where:

$$V_{ons}^2 = \frac{V_{on1}^2}{V_{n1}^2} \times \sqrt{4KTBR_s} \quad (112)$$

3.12.2 Phase Noise

Phase Noise generally occurs in Ring Oscillators when amplitude noise is added to the circuit by thermal, shot, and/or flicker noise during the transition of the signal voltage or current from Vdd to Ground or vice-versa. The amplitude noise makes the transition either faster or slower than it

should be without the noise input. This in turn makes the successive transitions faster and/or slower depending on the noise inputs during earlier transitions. Thus this time shift in the transitions creates phase noise, since the exact moment of the transitions becomes random. The transitions accumulate over time because each previous noise input affects the present time of transition and the future time as well [10]. However, phase noise in a Tuned RO Amplifier such as this LNA is not extremely significant because:

1. the RO is used at the output of the amplifier.
2. the transitions of the signal at the output is directly controlled by the input signal at the amplifying transistor, unlike a RO which runs freely without any external or independant input signal.
3. external noise sources have already been reduced by the input matching and the high output SNR of the amplifier.

Thus, the phase noise should not be a great concern for the LNA design discussed in this Thesis.

3.13 Linearity

The classic way to improve linearity of the LNA or Mixer is to put source resistances R_s or source inductor L_s . This increases the source voltage of the input transistor when the current I_d increases as a result of the increase in input gate voltage, V_g . This in turn reduces V_{gs} and thus I_d , therefore providing the negative feedback needed to maintain a linear circuit. However, in this LNA, this technique was not used since the goal of the Thesis is to minimize the chip area and design the LNA without the use of inductors. Therefore another technique was used. Instead of making the input transistors linear, the artificial tank (AT) that was created for the tuned LNA was made linear by putting source resistors in the Differential Ring Oscillator (DRO) artificial tank (the differential

architecture is discussed in section 3.15). The result was that even though the drain current of the input differential pair transistors was increased, the current through the Artificial Tank remained relatively constant for a limited input power level, thus increasing the circuits' 1-dB compression points. Thus linearity was maintained up to an input power of -20 dBm.

3.14 Output Matching

This was accomplished using appropriate current sources and source follower buffers so that the output impedance seen would be $1/g_m = 50$ ohms.

3.15 Differential Architecture

The small-signal current flow (i_d) in a single ended amplifier can be expanded by its non-linear components [3]:

$$i_d = i_{d1} + i_{d2}^2 + i_{d3}^3 + i_{d4}^4 + i_{d5}^5 + \dots \quad (113)$$

In a differential amplifier, the current flows between the input diff-pair transistors, thus the total current through the diff-pair is:

$$+i_d - (-i_d) = i_{d1} + i_{d2}^2 + i_{d3}^3 + i_{d4}^4 + i_{d5}^5 + \dots - (-i_{d1} + i_{d2}^2 - i_{d3}^3 + i_{d4}^4 - i_{d5}^5 + \dots) \quad (114)$$

$$= (i_{d1} + i_{d3}^3 + i_{d5}^5 + \dots) \quad (115)$$

This means that the even-order harmonics are cancelled out by the differential architecture. This result is very important because by using the Differential RO, the output waveform is no longer in the shape of decaying exponentials, but in the shape of hyperbolic sines and hyperbolic cosines. This is because the capacitors of the positive and negative inputs of the amplifying transistors

charge and discharge in a quarter of a cycle rather than half a cycle of the input waveform. This makes the Artificial Tank even more linear. Thus a differential architecture was chosen in order to minimize the 2nd order harmonics for the LNA circuit. Also, the differential architecture enables operation at higher frequencies than single ended designs because parasitic capacitances to ground are “halved” in value [4].

3.16 Differential RO (DRO) LNA

The RO LNA was made differential by connecting the outputs of the amplifying transistors forming a differential pair to the output nodes of a differential ring oscillator (DRO). This increases the frequency response because the differential structure makes some of the parasitic capacitances in the NMOS devices which are connected to ground to be divided by two. This doubles the frequency of operation. There is a disadvantage of using the differential structure in that the DRO LNA requires a constant current ($3 \times 250 \text{ uA}$) supply. This is due to the current sources used in the differential structure, thus producing a need for static power. In the single ended structure, the static power is almost zero because under the static condition, the RO power consumption is almost zero, which prolongs battery life. However, the advantage of added linearity is much more desirable.

In order to reduce the size of the DRO, which was used as the load for the differential LNA, the resistive loads in the DRO were replaced by active loads composed of diode-connected NMOS transistors. Adjustments were made in the sizes of the active load transistors and the sizes of the input differential pair transistors to obtain damped oscillations at the correct frequency for a short voltage pulse input at the gates of the input differential pair transistors.

3.17 Design Procedure

The following procedure was used to design the DRO LNA. First a DRO was designed using three identical differential inverters with a oscillation frequency of 6 GHz. The current sources of the DRO inverters were increased to give the correct oscillation frequency. Then the diode connected NMOS transistors were used to replace the load resistors of the inverters in the DRO. After that, D.C. simulations were run while varying the widths of the diode connected NMOS transistors and the differential inverter transistors to ensure 0.9 volts at the output of the DRO inverters and maximum voltage swing at the output of the LNA.

An NMOS differential pair (NDP), accompanied with the appropriate current source, was designed as the amplifier in the DRO LNA. The drains of the NDP transistors were connected to the output of the DRO (i.e. to two of the diode connected NMOS transistors of one of the differential inverters in the DRO). Since more current flowed through the NDP transistors, these diode connected NMOS transistors, which were connected to the differential inverter in the DRO, were replaced by smaller resistors so that the voltage at the drains of NDP transistors remained at 0.9 volts. A piece-wise linear voltage source (VPWL) was connected to the gates of the NDP transistors. The VPWL was configured so that it would give a short pulse and then maintained zero volts after the pulse.

Transient simulations were run and the widths of the NDP transistors were increased until damped oscillations were obtained from the DRO at 6 GHz. The width of the current source transistor was also increased to give the appropriate 1-dB compression and IP3 points.

Finally, the widths of the NDP transistors chosen were the ones closest to $2.5\mu\text{m} \times 4, 8, 16, 32, 64, \text{ or } 128$ due to the limitations of the RF models provided by Cadence and CMC. Off-chip input matching components were inserted to give the highest power transfer and power gain at 6 GHz. A buffer with an output impedance of $1/g_m = 50 \text{ ohms}$ was made to provide output matching for the LNA.

3.18 Time Domain Analysis of the Functioning of the Artificial Tank

In section 3.5 the time step-by-step time-domain analysis of the LC-tank was discussed. Here the time domain analysis of the functioning of an Artificial Tank shown in Figure 3.12 is discussed. This analysis is shown in Figure 3.15, where the mentioned transistor M1 is the amplifying NMOS transistor, and Vout is the voltage output at the drain of M1.

It is easily seen from Figure 3.15 how the storage of the energy in the Artificial Tank is “virtual” and not real because the electrical-energy is time-delayed in the RO to provide the illusion of energy-storage, therefore having the same effect as having an LC-tank.

1. the gate voltage of M1 shown in Figure 3.12 is increased.
2. the current through M1 increases.
3. this decreases V_{out} as the voltage across the load resistors increases, causing a signal (call it signal#1) to be transmitted throughout the inverter(s) of the RO.
4. the gate voltage of M1 is now decreased.
5. the current through M1 decreases.
6. this increases V_{out} as the voltage across the load resistors decreases. This sends another signal (call it signal#2) to be transmitted through the inverter(s) of the RO.
7. Now, if the frequency of the input signal is the same as the resonant frequency of the RO, which means that the response of the RO to signal#1 is “in-phase” with the incoming signal, then V_{out} increases further than normal, as the PMOS transistor of the RO provides lower resistance for the current/charge to flow out of the V_{out} node into V_{dd} .
8. When the gate voltage of M1 is increased again, yet another signal propagates through the inverter(s) of the RO.
9. V_{out} now drops further than normal if the frequency of the input signal is the same as the resonant frequency of the RO, which means that the response of the RO to signal#2 is “in-phase” with the incoming signal, because the NMOS transistor of the RO provides lower resistance for the current/charge to flow out of the V_{out} node into V_{ss} .
10. The cycle repeats back to step #4.

Figure 3.15: Time Domain Analysis of the Artificial Tank

3.19 Trade-Offs

3.19.1 *Reasons why linearity is a problem*

The RO does not have the same “drive capability” as the LC resonator because the Energy stored is “virtual”, a result of the feedback in the RO, and not real like in an LC-tank where energy is stored in electric and magnetic fields in the capacitor and inductor respectively. The result is that when the input power is increased, the output quickly saturates due to the transistors in the RO, and not due to the input differential pair transistors. One way to overcome this problem would be to use more current in the input differential pair transistors, but doing so might decrease the oscillation frequency of the RO because the input differential pair transistors' C_{gs} would increase, thereby increasing the load capacitance to the RO. The other way, which does not require current increase in the input differential pair transistors is to make the DRO more linear as discussed in Section 3.13.

3.19.2 *Choosing Transistor Widths*

The DRO inverter transistors widths were chosen to give the correct oscillation frequency. Damped oscillations were obtained by just increasing the active load width to 1.4 μ m. This gives a frequency of 10GHz. As the widths of the load is decreased, the amplitude of the oscillation increases, and the frequency of the oscillation decreases to 6GHz. After the adjustments of the desired widths, the closest size was chosen for 2.5 μ m x 4, 8, 16, 32, 64, or 128.

To improve linearity, the current of the input differential pair transistors was increased by 4 and the Load by 4. This increases the 1dB compression point to -27dBm with a power gain of 9dB while keeping the NF less than 2dB at 6GHz. This is achieved with matching elements $L_1 = 5$ nH,

and $C1 = 51\text{fF}$, and with the input differential pair transistors biased at 0.9V for the gate voltage V_g .

3.19.3 Choosing Gate Biasing Resistors

In order to increase the IP3 and/or the P-1dB point of the LNA, the biasing resistor (R_{bias}) values would have to be decreased from 100Kohms to less than 10Kohms (to decrease compression due to the input components). This would result in a P-1dB = -15dBm for a Current Source of $64 \times 2.5\mu\text{m}$, and with $L1 = 6.17\text{nH}$ and $C1 = 30\text{fF}$ arranged at the input for off-chip matching. However, this results in a low voltage gain of 10dB , a S_{21} of 0dB , and a NF of 5dB (approx). It is not appropriate to sacrifice the voltage gain and NF for a higher compression point, therefore this was not done.

In order to reduce the number of components used for input matching, the values of the R_{bias} resistors used to set the gate voltage of the input differential pairs were swept so that Z_{in} (real) is 50 ohms . Hence no $C1$ is required, and therefore the input did not oscillate or compress as much as before. This value was obtained to be 42.9Kohms for $CS = 128 \times 2.5\mu\text{m}$. The $L1$ off-chip matching inductor was swept and found to be 13.18nH for a minimal S_{11} . The D.C. current of the LNA was now reduced to 2mA .

3.20 Initial Simulation Results

The schematic of the DRO LNA that was used to obtain the simulation results is shown in Figure 3.16. Figure 3.17 shows the S-parameter plots obtained from simulations in Cadence. The S-parameters show that the DRO LNA circuit has its input and output matched to 50 ohms ($|S_{11}|$

and $|S_{22}| < -10$ dB), and has a power gain of 9.25 dB, and a Noise Figure of 2.3 dB. Figure 3.19 shows the 1-dB compression point of the DRO LNA without a the buffer to be 18.9 dBm, while Figure 3.18 shows the 1-dB compression point of the DRO LNA after the buffer to be 20.9 dBm, yielding a 1-dB increase in compression due to the buffer.

The frequencies used for the IP3 simulations were 5.9 GHz and 6 GHz. Before the buffer was added, the IP3 point obtained from extrapolating the 3rd order output power of 5.8 GHz was -12.1 dBm as shown by Figure 3.22, while Figure 3.23 shows the IP3 point obtained from extrapolating the 3rd order output power of 6.1 GHz at -11.1 dBm.

Figure 3.20 shows the IP3 point obtained from extrapolating the 3rd order output power of 5.8 GHz at -13.2dBm after the buffer was added, while Figure 3.21 shows the IP3 point obtained from extrapolating the 3rd order output power of 6.1 GHz at -11.6 dBm. The plot in Figure 3.20 shows that the P-1dB point at the output is 2dB lower because the buffer increases compression.

Figure 3.17: RO LNA S-parameter plot.

Figure 3.18: The P-1dB plot of the RO LNA at the output port (which is after the buffer).

Figure 3.19: The P-1dB plot of the RO LNA at the output nets (before the buffer).

Figure 3.20: RO LNA IP3 plot @ output port with 3rd order frequency = 5.8 GHz.

Figure 3.21: RO LNA IP3 plot @ output port with 3rd order frequency = 6.1 GHz

Figure 3.22: RO LNA IP3 plot @ output nets (before the buffer) with 3rd order freq = 5.8 GHz.

Figure 3.23: RO LNA IP3 plot @ output nets (before the buffer) with 3rd order freq = 6.1 GHz.

4.0 POST LAYOUT SIMULATION

A layout of the LNA was created and the layout was extracted in order to simulate the performance of the extracted circuit. The following section describes the special procedures that were taken in order to extract the proper transistors from the layout. Section 4.2 describes the design of the Electrical Discharge Protection (ESD) circuit and its layout. Section 4.3 shows the post layout simulation (PLS) results of the LNA with ESD protection. Finally, section 4.4 gives the PLS results using resistive extraction only.

4.1 Special Procedures

The following procedures had to be performed for every simulation: i.e. S-parameter, Periodic Steady State (PSS),... etc.

The extraction process in Cadence produces only “nch” type devices in the layout. The “nch” type transistor model is used for frequencies under 1 GHz. The “nch_rf” type transistor model is used for frequencies between 1 and 6 GHz.

In the post layout simulation (PLS) a new netlist was created in Analog Artist using: simulation-->netlist-->recreate. Then the “input.scs” file was opened using the text editor and all the “nch” were converted to “nch_rf” using: Edit-->Find/Change.

Later on, a method was discovered to extract the “nch_rf” transistors directly from the layout. This was done by copying the “divaEXT.rul” file into /home/aahmed directory, and changing the

saveProperty(nmos "model" "nch") function to saveProperty(nmos "model" "nch_rf"). The word "extracted" was added to the Setup-->Environment page. Then the simulation was run without netlisting, using the "yellow" button in Spectre. It is found that the input matching inductor L1 was 11.1nH for an S11 match.

Figure 4.1: RO LNA PLS: The P-1dB plot.

The Power Gain S21 was 7.5dB. This is a 1.5dB drop from the schematic simulation shown in Figure 3.17. The NF and P-1dB point remained almost the same as shown in Figure 4.1 above. The interconnect metal lines were made smaller in RO_LNA_Diff9_rf_layout2, but the PLS did not give better results. Two pins named Vout1_plus and Vout1_minus were put in the layout just before the buffer, and the S-parameter and PSS PLSs were run. The PLSs results show that the

differential Voltage gain at the 2 pins before the buffer was 17.2dB. This should give an equivalent power gain of 8.5dB, but the actual power gain obtained was 7.5dB. This means there was a 1 dB loss in power gain through the buffer. Thus the original layout named RO_LNA_Diff9_rf_layout was going to be used in the actual layout to be submitted for fabrication.

4.2 ESD Protection

The ESD protection circuit was created using three diodes. The ESD protection circuit shown in Figure 4.2. All the diodes were set in the reverse bias position. The ESD protection circuit works in the following way. If the voltage at the Vdd exceeds the diode breakdown voltage (V_{bkd}), then the current would flow to the ground through D1 instead of flowing through the circuit. If the signal line voltage exceeds V_{bkd} , then the current flows to ground through D3. Finally, if the signal line voltage exceeds $V_{dd} + 0.7V$, then current flows to Vdd through D2 instead of affecting the gates of the transistor.

Figure 4.2: ESD schematic.

Figure 4.3 below shows the layout of the ESD protection circuit. There were significant simulation differences before ESD protection was added and after.

Figure 4.3: The layout of the ESD circuit.

4.3 LNA: PLS Results with ESD Protection

Due to the ESD protection circuit, the NF increased to 3.3dB, and the power gain decreased to 6.98dB. Also the voltage gain decreased to 16dB. The new matching component values were: $L1 = 4.365\text{nH}$ and $C1 = 1.4\text{pF}$ for $Z_{M1}(\text{real}) < 50\text{ ohms}$. Figure 4.4 shows the LNA layout. Figure 4.5 shows little difference in the 1-dB compression point of the LNA after adding the ESD protection. However Figure 4.6 and 4.7 show that the power gain of the LNA is now reduced to about 7dB due to ESD protection.

Figure 4.4: LNA Layout.

Figure 4.5: LNA PLS with ESD Protection P-1dB plot.

Figure 4.6: LNA PLS with ESD Protection PSS power Gain @ 6GHz

Figure 4.7: LNA PLS with ESD Protection PSS S-parameter plots.

4.4 LNA PLS Results with Resistive Extraction

The cmop18 “divaEXT.rul.” only allows the extraction of “parasitic resistors” or “parasitic caps” but not both. In order to get more realistic PLS values, the connections on the layout were overlaid with m5res, m4res... etc, depending upon the connection metal layer. This resulted in the extraction of the connections as resistors when the switch for “parasitic caps” was used. This design was not submitted, but was used for simulation only.

Resistive extraction S-Parameter simulation is shown in Figure 4.8. Here, the NF increased to 2.95dB and S21 decreased to 5.4dB but the voltage gain remained approximately the same (15

dB). Figure 4.9 shows that since the gain decreased due to the resistances extracted, the 1-dB compression point increased to -17.7 dBm from -19.5 dBm. Figure 4.10 shows the full circuit layout that was submitted to CMC for manufacture.

Figure 4.8: LNA with ESD Protection PLS with Resistive Extraction: S-Parameters.

Figure 4.9: LNA with ESD Protection PLS with Resistive Extraction: P-1dB plot.

Figure 4.10: ICFCULMV Layout

5.0 EVALUATION BOARD DESIGN, AND CHIP PERFORMANCE

5.1 General Design Issues

The dimensions of the final chip layout were measured in microns and converted into mils which is the unit that the PCB layouts use. Advance Design Systems (ADS) software was used to design the PCB for the LNA. Microstrip line characteristics of the traces on the glass PCB were used to replace inductors that were originally used for input matching for the LNA. There were some iterations performed to achieve realistical lengths and widths of the microstrip lines. Simulated values were obtained from LineCalc and ADS schematic simulations. The PCB layout size for the LNA was limited to a 2 inch x 2 inch glass slide substrate.

There were several attempts to convert the Cadence Netlist/Schematic into ADS netlist/schematic so that the circuits with the PCB components could be simulated with the ADS cmosp18 models provided by CMC. The schematic was not successfully converted since the license “OASIS RFDE” was not available for use in Cadence at Carleton University. As a result only netlist files were successfully converted. The ADS simulation results were drastically different from the Cadence simulation results. Hence the default Cadence simulation results were chosen in preference because cmosp18 files were originally created and designed for Cadence.

In order to use the Cadence simulation results, the LNA Cadence S-parameter simulation results were saved to “.s2p” data files. These “.s2p” files were re-formatted to the ADS data file formats. Careful simulations were done in ADS using the “.s2p” files in order to obtain the proper values

for input and output matching. Just for simulation purposes, perfect baluns were used to convert the single-ended inputs/outputs in the “.s2p” files to differential inputs and outputs.

Because the testing of the LNA was done using single-ended inputs/outputs available from the Network Analyzers, real baluns were needed to provide the differential input/output signals for the circuits. An internet search was performed to obtain baluns for the 6 GHz operating frequency. This was not successful so a ring-balun design was considered for the PCB.

5.2 Design of the Rectangular-Balun (RB)

This is how the RB works. A ring consisting of $6 \frac{\lambda}{4}$ long segments is made. The input voltage V_{in} and the reference or ground are kept a distance of $\frac{\lambda}{2}$ apart. The differential outputs are now taped as follows. V_+ is taped between V_{in} and Gnd, $\frac{\lambda}{4}$ away from each, and V_- is taped $\frac{\lambda}{4}$ away from the Gnd. This ensures that the 2 voltages V_+ and V_- are exactly 180° apart because the positions from which they are taped are exactly $\frac{\lambda}{2}$ apart in distance [11-13].

The main problem being faced was the PCB size limitations. As a result, the Ring-Balun was “converted” into a Rectangular-balun using exactly the same concept. The schematic of the Rectangular-balun is shown in Figure 5.1. Figure 5.2 shows the balun layout. Symbols were created from the schematic and connected for testing the baluns as shown in Figure 5.3. The results of the 2-port S-parameter simulation performed in ADS on the Rectangular-Balun are

Figure 5.2: Rectangular-Balun Layout.

Figure 5.3: Rectangular-Balun Test Schematic.

Figure 5.4: Rectangular-Balun Test S-Parameter Simulation Results.

The balun was used for the RO LNA input and output. Ideal inductors of value 1 nH were used to emulate the inductance that would be presented by the bond-wires [4.2] which connect the pads of the ICFCULMV die to the PCB pads.

5.3 Full PCB Design

The Balun discussed in Section 5.2 was used to provide a truly differential input to the LNA at 6 GHz. The “.s2p” files were connected to ideal baluns to convert the single-ended input/output into differential inputs/outputs. The size of the pads used for bondwires were made to be 5 mil square. Gaps between the PCB traces were kept for soldering off-chip components such as D.C. coupling and matching capacitors. However, it should be noted that the soldered capacitors could not be “modelled” properly because solder properties and sizes vary from one solder joint to another, so only ideal capacitors were used in their place.

The Schematic of the LNA PCB that was used in ADS simulation is shown in Figure 5.5. The layout of the LNA PCB is shown in Figure 5.6 and the S-parameter Simulation results of the LNA PCB together with the LNA as the S2P file block is given in Figure 5.7. This S-parameters simulation result shows the S21 should be about 6dB, but it does not consider the resistance of the baluns and the loss-tangent of the Soda-Lime Glass PCB material.

Figure 5.6: LNA PCB Layout.

Figure 5.7: S-parameter PLS results of the RO-LNA together with the LNA-PCB.

5.4 Component Mounting Difficulties and PCB Re-design

Two PCBs were fabricated. On the first PCB, the matching capacitors available in the High Speed Lab (5128ME) at Carleton University were used. The test results were not acceptable. No significant gain could be measured at the output. On the second PCB ceramic matching capacitors from Johanson Technologies were used. Mounting these capacitors presented great difficulty because of their size and structure. An attempt was made to mount the capacitors. However, the

the measured results did not give any significant output. It was determined, by looking through a microscope, that even though it seemed to the naked eye that the connections with the PCB traces were made, in reality the connections were not made.

It was then decided to test the LNA alone in order to prove the concept. The LNA-PCB was designed using inter-digitated capacitors (ID caps). It is well known that the ID caps are non-linear in the way their capacitance is related to their structure because the capacitance is due to the electromagnetic fields in air/space rather than within the substrate alone. Thus the size of the capacitors was determined purely by trial and error to get the best performance of the LNA at 5.98 GHz. Also, for the simulations, the $\epsilon_r = 6.0$ was used instead of 6.7, since it was determined that the glass substrate material was Soda-Lime Glass instead of Boro-silicate glass. Figure 5.8 shows the picture of the ID cap used for input matching, while Figure 5.9 shows the picture of the ID cap used for output matching. Figure 5.10 shows the layout of the input balun with the ID cap, while Figure 5.11 shows the layout of the output Balun with the ID cap. Figure 5.12 shows the final glass PCB in ADS layout. Figure 5.13 shows the ADS schematic used to simulate the final LNA PCB, after considering the loss tangent of 0.03 for the Soda-Lime Glass material. The S-parameter simulation results shown in Figure 5.14 shows that the input and output are matched, and a power gain of 2.4 dB is obtained from this circuit. However, this simulation did not consider the resistive losses due to the traces on the die that connected the LNA to pads on the ICFCULMV die.

Figure 5.8: Inter-digitated capacitor used for input matching.

Figure 5.9: Inter-digitated capacitor used for output matching.

Figure 5.10: Re-designed Balun + ID cap for LNA input

Figure 5.11: Re-designed Balun + ID cap for LNA output

Figure 5.12: Final PCB design

Figure 5.13: ADS Simulation Schematic

Figure 5.14: Re-designed PCB ADS Simulation Result

5.5 Test Results

SMA connectors were soldered to the PCB to enable connection to the Vector Network Analyzer (VNA). Figure 5.15 to 5.19 show the first S-parameters measured for the LNA. Figure 5.15 shows that the input is matched at 4.78 GHz instead of 5.98 GHz as the ADS simulations had indicated.

This is probably due to following causes:

- the ADS simulations did not give accurate modeling of ID caps.
- there were minor deformations in the ID caps that were not visible.

- the input impedances of the LNA was different from that which was predicted from simulations due to process variation.

Figure 5.16 shows there is no output signal when the circuit is OFF. When the LNA is turned ON, Figure 5.17 is obtained showing a S21 (power gain) of -23 dB at the matched frequency of 4.78 GHz and a power gain of -18 dB at 5.98 GHz where the circuit is not matched. Figure 5.18 shows that the output is not matched over the measured frequencies. Figure 5.19 shows that there is a -33 dB isolation between the input and the output as seen by the VNA. The Figures 5.16 and 5.17 show that the circuit is not working at 5.98 GHz as designed for, rather it is working at about 5.4 GHz.

Figure 5.15: Original S11.

Figure 5.16: Original S21 with circuit OFF

Figure 5.17: Original S21 with circuit ON

Figure 5.18: Original S22

Figure 5.19: Original S12

An aluminium foil was delicately put on the PCB traces to alter the impedances of the matching network so that the circuit becomes matched at 5.4 GHz. This resulted in the following S-parameters shown in Figures 5.20 to 5.24. Figure 5.20 shows that the input is well matched at 5.4 GHz. Figure 5.21 shows there signal power is -28 dB when the circuit is OFF. Figure 5.22 shows the signal power is -9 dB at 5.4 GHz when the circuit is ON. This frequency shift from 5.98 GHz to 5.4 GHz can be explained as the result of about a 10% process variation [14]. The low power gain at first seems to indicate the circuit is not working. However, when certain losses are considered, which will be discussed in sub-section 5.6, it is realized that the LNA does in fact

work in principle. Figure 5.23 shows that the output is well matched at 5.4 GHz. Figure 5.24 shows the circuit has a good isolation of -26 dB at 5.4 GHz.

Figure 5.20: S11 with Aluminium Foil

Figure 5.21: S21 with Aluminium Foil with circuit OFF

Figure 5.22: S21 with Aluminium Foil with circuit ON

Figure 5.23: S22 with Aluminium Foil

Figure 5.24: S12 with Aluminium Foil

5.6 Discussion of Measured vs Simulated Results

The Gain of -9 dB is not impressive for any amplifier. The expected gain, after considering the losses due to the PCB traces was 2.4 dB. This is a 11.4 dB difference. There are some losses associated with the metal 5 paths from the LNA circuit in the chip to the pads of the chip that were

not considered. It was impossible to consider these resistances during the design of the PCB because Cadence crashed every time the LNA resistance extraction was run. These paths had to be extracted separately in a new cellview. The resulting resistances from the paths are shown in the Figure 5.25. Also, resistance of the solder joint for the SMA connectors was measured to be 0.4 ohms and 1 ohms for the input and output respectively. These resistances were entered into the ADS simulator to account for the losses, and the loss tangent was increased to a maximum of 0.05 instead the average 0.03 value. The resulting ADS schematic is shown in the Figure 5.26. The S-parameter plot obtained from simulating the ADS schematic after considering the resistive losses is shown in Figure 5.27. The new power gain is now -2.5dB. This still leaves 6.5 dB loss unaccounted for.

Considering the fact that the baluns were designed for the operation frequencies from 5.8 GHz to 6.0 GHz, and the fact that the LNA seems to be working at 5.425 GHz instead of 5.98GHz (due to process variation), then the input signals to the LNA are no longer 180 degrees out of phase. This can cause a loss of about 6 dB (1/4 power loss about 50% from each balun) because now the LNA is no longer truly differential and there may be radiation losses from the rectangular baluns that were not simulated. Add another 0.5 dB loss due to the cables, and the S21 measured from the Vector Network Analyzer shown in Figure 5.22 is now accounted for.

Figure 5.25: Resistances of LNA METAL 5 PATHS

Figure 5.27: PCB Simulation considering losses

6.0 CONCLUSION

6.1 The Conclusion

A new use of the Ring Oscillator as an artificial tuning tank for an amplifier has been introduced. A differential LNA was designed in Cadence using 0.18 micron CMOS technology incorporating an artificial tank circuit. Post Layout Simulations were performed to ensure proper operation. The circuit was manufactured by TSMC via Carleton University's contract with CMC in 0.18-micron CMOS on a 1.5mm by 0.5mm die. Several unsuccessful attempts were made to assemble capacitors on the gold traces of the glass PCB to measure the LNA. A final solution using interdigitated capacitors enabled the measurement of the LNA.

The original Gain of the LNA, without the losses of the metal 5 paths leading up the pads was simulated to be 9 dB with a NF of 2.3 dB. After adding ESD protection diodes, the Gain was reduced to 7dB. When the losses of the transmission lines on the PCB are considered, and the losses due to the metal 5 paths leading up to the pads are taken into account, the gain of the LNA reduces to -2.5dB. The LNA was measured and found to be working at 5.4 GHz instead of 5.98 GHz (due to process variation). This accounts for about 6 dB loss due to the fact that the signal going into and out of the LNA is no longer differential (since the Rectangular baluns on the PCB were designed to work between 5.8 and 6 GHz). Due to the process variation that could not be foreseen, which made the LNA work at 5.4 GHz instead of 5.98 GHz, and the radiation losses that were have not been simulated and could not be measured, and because of the metal line resistances that could not be extraced in Cadence, the LNA loss can be accounted for. Thus it can

be concluded that the LNA incorporating an artificial tank circuit works in principle. The measured performance is given in Table 2.

Table 2: LNA MEASUREMENTS

Measurement	Simulated Value	Measured Value
Center Frequency	5.98 GHz	5.435 GHz
Bandwidth	200 MHz	350 MHz
Gain with PCB losses	-2.5 dB	-9 dB
Current Consumption	9.0 mA	9.5 mA
Voltage supply	1.8V	1.8V
S11	-15 dB	-22 dB
S22	-20 dB	-25 dB
Noise Figure (Simulated)	7.9 dB	

It should be noted that if a gain of about -2.5 dB was measured from the PCB when connected to the Network Analyzer, then this would imply that the LNA on the die worked almost exactly as simulated. However, the measured gain was -9 dB, which means that the gain of the LNA on the die was $9 \text{ dB} - (-2.5 \text{ dB}) + (-9 \text{ dB}) = 2.5 \text{ dB}$, ignoring any radiation losses from the rectangular baluns. Therefore it can be concluded that the LNA on the die did work as an amplifier with a low gain.

6.2 Future Work

The models used for the circuits in this Thesis were from CMC's "rf018.scs" files, which are valid up to 6 GHz for a fixed width of 2.5 microns. Therefore the models are not accurate for a whole

range of widths which would have enabled a better design and performance. More accurate models should be developed.

Control voltages could be added to control the resonant frequency of the artificial tank and the output resistance of the input differential pair transistors, instead of supplying fixed voltages through an internal current mirror. Other features that could be added are on-chip active input and output matching networks with yet another control voltage that would enable the circuit to be tested using probes instead of a PCB. The output buffers were not well designed, thus an improvement could be made by using current sources instead of the resistances that were used. An output active matching network (which does not necessarily emulate inductors) could replace the buffers.

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APPENDIX A

A.1 System Solution to an Inductor

The idea is to create a circuit which will do the same thing an inductor does. The main properties of an inductor are:

- it increases the voltage across it when the rate of change of current through it increases.
- it provides a short circuit for D.C. currents.
- it provides a short circuit for D.C. voltages.

The circuit shown in Figure A1 was developed to obtain inductive behaviour of the inductor at V_2 as the current through it is altered:

Figure A1: Artificial Inductor circuit

The main question is how would one increase the voltage given a change in the rate of current flow without using an inductor? The answer is to use a resistor (R_1) to create a change in voltage for a small amount of current flowing through it, and in parallel with the resistor, put a capacitor (C) through which current will flow due to the changing voltage on top of the capacitor which is a result of changing input current. Another resistor (R_2) is put in series with the capacitor across which the voltage increases or decreases, depending on whether the rate of change of voltage is

increasing or decreases across R_1 . This voltage across R_2 can be amplified and fed back to the point of the input current.

Normally, the A.C. voltage across R_2 is:

$$v_2 = i_{in} R_1 \left(\frac{R_2}{R_2 + \frac{1}{j\omega C} + R_1} \right). \quad (A.1)$$

But if R_1 and R_2 are small enough compared to the impedance of the capacitance $\frac{1}{j\omega C}$, then

$v_2 \approx i_{in} R_1 R_2 (j\omega C)$ which in time domain approximates to $v_2 \approx \frac{di_{in}}{dt} R_1 R_2 C$. The time

domain response of an inductor is: $v = L \frac{di_{in}}{dt}$. If v_2 is amplified by a factor K and fed back to

node “A”, then the equivalent inductance of the circuit composed of R_1 , R_2 , C and the amplifier

would be $L \approx K R_1 R_2 C$. The value of “L” obtained in this way would be mostly dependant on

the value of K , R_1 and C , since the value of R_2 would be relatively small. The simulation result of

the circuit in Figure A1 above is shown in Figure A2 in the next section, proving that the voltage

at V_2 is indeed “similar” to what one would expect from an inductor, i.e. it is “lagging” behind the

input current by 90 degrees, however, it is very small, and thus the need for amplification.

A.2 Major Problems

A major problem was creating the “virtual short”. This was attempted by creating the circuit shown in Figure A3. This circuit also provides the necessary isolation between the feedback

voltage output and the input current. However, there are problems in using this kind of a circuit and will be discussed in Section A.4.

Another problem was applying the feedback voltage at the input without increasing the current through the Artificial Inductor (AI) and not resulting in a positive feedback. This would result in non-inductive behaviour. An apparent solution to this was to use a Charge Pump to provide the necessary current through R_1 to provide the voltage greater than V_{dd} or less than V_{ss} at Node “A” shown in Figure A1. However, this in turn changed the phase of the circuit, giving a non-inductive response.

Making the inductor bi-directional (so it behaves the same, whichever way it is connected) seemed to be overcome with the virtual short circuit shown in Figure A3. This could not be obtained by the circuit used in Figure A1. However, this characteristic could be specific to the application depending on whether the inductor is to be used in input or output matching circuit, or in an L-C tank. The D.C. current consumption of the AI had to be minimized to prevent excessive power usage. Also, the “series resistance” of the AI had to be reduced in order to achieve a high Q. A novel “virtual short” (VS) circuit is shown in Figure A3 below. The explanation of how this circuit works is given in the following section.

Figure A2: The plot of the “inductive” behaviour of the AI shown in Figure A1

Figure A3: Virtual Short Circuit

A.3 Explanation of the Virtual Short Circuit shown in Figure A3

As the voltage at node C is increased, the current in M1 increases, which is mirrored to M2 and M3, which is again mirrored to M4, where M5 acts as the load. Thus the voltage at node D is approximately the same as the voltage at node C. Similarly, when the voltage at node D is increased, the current through M5 increases, which is mirrored to M6 and M7, which is again mirrored to M8, where M1 acts as the load. Again, the voltage at node C is approximately the same as the voltage at node D. By inspection, the circuit can be seen to be “symmetrical”.

The simulation shown on the next page shows how the voltage at node D is almost the same as at node C till the voltage at node C reaches 1.1V. After this point they are different because the PMOS transistor M4 needs 0.6V to stay “on” ($1.8 - 0.6 = 1.2\text{V}$). The short circuit voltage characteristic of the virtual short circuit can be increased by increasing the Vdd to 3.6V instead of 1.8V; then the voltage at node C and D are the same for the range from 0 to 2.6V.

A.4 Problems with the Virtual Short Circuit

Even though the virtual short circuit acts as a good “voltage short”, it does not act as a good “current short”. To improve its performance as a “current short”, the widths of the NMOS transistors were increased from $6\mu\text{m} \times 1$ to $12\mu\text{m} \times 20$, and the PMOS transistors from $18\mu\text{m} \times 1$ to $36\mu\text{m} \times 20$. This results in the circuit behaving like a “current short” with a “series resistance” of only 8 ohms, as well as a “voltage short”, with one major disadvantage: the D.C. current flow is 400mA instead of 4mA for the original transistor widths.

An advantage of using the above Virtual Short circuit is that the node “A” of “circuit A” can be attached to the node “A” of the VS circuit, enabling R_1 to tap the current from the drain of M2. The output at V_2 from “circuit A” can then be amplified and fed back to node C of the VS circuit. This would in turn result in an “inductive behaviour” where the feedback path is actually within the virtual short circuit, negating the need for isolation.

The disadvantage of this circuit is that there is a limitation in the voltage swing due to the threshold voltages of the PMOS and NMOS transistors. This is clearly shown in Figure A4. Furthermore, when the voltage at Node C/D is increased within the operating range, the voltage at Node D/C increases as well. However, if the voltage at Node C/D is held initially at a certain voltage, and the voltage at Node D/C is decreased, the voltage at Node C/D does not decrease. Thus this circuit does not behave as an applicable virtual short.

Figure A4: The voltage ranges at which the Virtual Short circuit in Figure A3 can operate.

APPENDIX B: NMOS Equations

NMOS EQUATIONS [4]:

Threshold Voltage equations:

$$V_{TH} = V_{THO} + \gamma(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}) \quad (B.1)$$

where:

$$V_{THO} = \Phi_{MS} + 2\Phi_F + \frac{Q_{dep}}{C_{ox}}, \quad (B.2)$$

$$Q_{dep} = \sqrt{4q\epsilon_{Si}|Q_F|N_{sub}}, \quad (B.3)$$

$$\gamma = \frac{\sqrt{2q\epsilon_{Si}N_{sub}}}{C_{ox}}, \quad (B.4)$$

and:

$$\Phi_F = \frac{kT}{q} \ln\left(\frac{N_{sub}}{n_i}\right) \quad (B.5)$$

Velocity Saturation equation:

$$I_D = \mu_{crit} C_{ox} 'W (V_{GS} - V_T) \quad (B.6)$$

Saturation Current:

$$I_D = \frac{1}{2} \mu_n C_{ox} 'W (V_{GS} - V_T)^2 (1 + \lambda(V_{DS} - V_{DS,sat})) \quad (B.7)$$

Saturation Current condition:

$$V_{DS} > V_{GS} - V_T \quad (B.8)$$

and:

$$V_{GS} > V_T \quad (B.9)$$

Triode Current:

$$I_D = \mu_n C_{ox} 'W \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] \quad (B.10)$$

Triode Current condition:

$$V_{DS} < V_{GS} - V_T \quad (B.11)$$

and:

$$V_{GS} > V_T \quad (B.12)$$

Subthreshold Current:

$$i_{DS} = I_{DS0} \frac{W}{L} \exp\left(\frac{v_{GS}}{nkT/q}\right) \quad (B.13)$$

Subthreshold Current condition:

$$V_{GS} < V_T \quad (B.14)$$