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LOW TEMPERATURE COFIRED CERAMICS FOR LMCS/LMDS APPLICATIONS

Alex Panther

**A Thesis Submitted to the School of Graduate Studies in Partial
Fulfillment of the Requirements for the Degree
Master of Engineering**

**Carleton University
2001**

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the Faculty of Graduate Studies and Research
acceptance of the thesis**

**Low Temperature Cofired Ceramics
for LMCS/LMDS Applications**

**Submitted by
Alex Panther, B.A.Sc**

**In partial fulfillment of the requirements for the degree of
Master of Engineering**

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Abstract

This thesis demonstrates that Low Temperature Cofired Ceramic packages can be used for LMCD/LMDS (Local Multipoint Communications System / Local Multipoint Distribution System) applications, provided that parasitic radiation sources are accounted for. Three planar transitions (microstrip to stripline, coplanar waveguide (CPW) to coplanar waveguide and coplanar waveguide to stripline) and four vertical transitions (stripline to stripline, stripline to CPW, CPW to CPW, and CPW to microstrip) are considered and analyzed. A potential radiation problem at high frequencies is discovered and methods of eliminating this radiation are discussed.

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Table of Contents

Chapter One: Introduction	1
1.1 <i>Trends in Data Transmission</i>	1
1.2 <i>Objectives</i>	7
Chapter Two: Low Temperature Co-fired Ceramics	9
2.1 <i>Current Microwave Packaging</i>	9
2.2 <i>The History of Low Temperature Co-fired Ceramics</i>	12
2.3 <i>The Manufacture of MCM-C</i>	14
2.4 <i>LTCC vs. HTCC</i>	15
2.5 <i>Challenges with Low Temperature Co-fired Ceramics</i>	16
2.6 <i>Advantages of Low Temperature Co-fired Ceramics</i>	19
2.2 <i>LTCC Packages</i>	25
2.3 <i>The Need for Research into Vertical Transitions</i>	29
Chapter Three: Transmission Line Theory	30
3.1 <i>Transmission Lines for a 3D Environment</i>	30
3.2 <i>Microstrip</i>	32
3.3 <i>Stripline</i>	35
3.4 <i>Coplanar Waveguide</i>	38
Chapter Four: Feedthrough Simulations	43
4.1 <i>The Need To Study Feedthroughs</i>	43
4.2 <i>Electromagnetic Simulations</i>	43
4.3 <i>Simulations Included in this Thesis</i>	44
4.4 <i>Design Rules</i>	46
4.5 <i>Entering and Exiting the Package</i>	47
4.5.1 <i>Microstrip to Stripline Feedthrough</i>	49
4.5.2 <i>CPW to CPW Hermetic Feedthrough</i>	53
4.5.3 <i>CPW to Stripline Hermetic Feedthrough</i>	55
Chapter Five: Simulations of Vertical Transitions	59
5.1 <i>Vertical Transitions – Direct vs. Coupled</i>	59
5.2 <i>Stripline to Stripline Vertical Transition</i>	61
5.2.1 <i>General Effects of the Connecting Via and Via Pad</i>	64
5.2.2 <i>The Capacitive Effect of the Via Pad</i>	66
5.2.3 <i>The Effect of the Via Diameter</i>	68
5.2.4 <i>The Effects of Varying the Hole in the Ground Plane</i>	70
5.2.5 <i>Parallel Plate Modes Launched By This Transition</i>	73
5.2.6 <i>Grounding the Stripline to Stripline Transition</i>	74
5.3 <i>Stripline to CPW Vertical Transition</i>	78
5.3.1 <i>Transition Properties</i>	81
5.3.2 <i>Effect of the Via Diameter and Via Pad Size</i>	82
5.3.3 <i>Effect of the CPW Open Circuit</i>	83
5.3.4 <i>Variations with the DiPak and VTT Simulations</i>	84

5.3.5 <i>Grounding Schemes</i>	85
5.3.6 <i>Tuning the Transition</i>	88
5.4 <i>CPW to CPW Vertical Transition</i>	92
5.5 <i>Coplanar Waveguide to Microstrip Vertical Transition</i>	96
5.6 <i>Other Vertical Transitions</i>	100
Chapter Six: Transition Modeling	101
6.1 <i>Stripline to Stripline Vertical Transition</i>	101
6.1.1 <i>Comparison</i>	111
6.2 <i>Stripline to CPW Vertical Transition</i>	113
6.3 <i>CPW to CPW Vertical Transition</i>	116
6.4 <i>CPW to Microstrip Vertical Transition</i>	120
6.5 <i>Comparison of Circuit Model Values</i>	122
Chapter Seven: Measurements	124
7.1 <i>Finished Package</i>	124
7.2 <i>Microstrip Test Circuits</i>	129
7.2.1 <i>Measurements</i>	135
7.2.2 <i>Agreement with Simulation</i>	140
7.3 <i>Coplanar Test Circuits</i>	143
7.3.1 <i>Measurements</i>	149
7.3.2 <i>Agreement with Simulation</i>	160
Chapter Eight: Radiation	165
8.1 <i>Radiation in the Coplanar Test Circuits</i>	165
Chapter Nine: Discussion and Conclusion	186
9.1 <i>Conclusion</i>	186
9.2 <i>Future Work</i>	187
Bibliography	189

List of Tables

1.1 Data rate for various video qualities (Standard Resolution)	2
1.2 LMCS Frequency bands in Canada	4
1.3 LMDS Frequency bands in the USA	4
2.1 Comparing packaging technologies	21
2.2 Characteristics of different LTCC types	23
3.1 Transmission line attenuation	42

List of Illustrations

1.1 <i>An LMCS Configuration</i>	3
1.2 <i>Attenuation vs. Frequency</i>	6
2.1 <i>Packaging Levels</i>	9
2.2 <i>Custom metal microwave package</i>	10
2.3 <i>BGA MMIC package</i>	11
2.4 <i>The Creation of an MCM-C package</i>	15
2.5 <i>Via Posting</i>	18
2.6 <i>An LTCC-M Package with several active devices</i>	19
2.7 <i>Loss Tangent of several materials versus frequency</i>	24
2.8 <i>Attenuation versus frequency for several different materials</i>	24
2.9 <i>LTCC-M amplifier</i>	26
2.10 <i>Phased array design</i>	27
2.11 <i>LTCC Stripline package</i>	28
2.12 <i>LTCC Stripline coupler</i>	29
3.1 <i>A microstrip line</i>	32
3.2 <i>Stripline</i>	35
3.3 <i>The E field of the CPW mode</i>	39
3.4 <i>The E field of the slotline mode</i>	39
3.5 <i>The E field of the parallel plate mode</i>	40
3.6 <i>The E field of the microstrip mode</i>	40
4.1 <i>Typical DiPak package structure</i>	47
4.2 <i>Two types of feedthrough</i>	48
4.3 <i>Microstrip to Stripline Feedthrough</i>	49
4.4 <i>D1 Microstrip to stripline feedthrough</i>	50
4.5 <i>D1 Microstrip to stripline feedthrough simulation results</i>	50
4.6 <i>VTT Microstrip to stripline feedthrough</i>	51
4.7 <i>VTT Microstrip to stripline feedthrough simulation results</i>	52
4.8 <i>VTT CPW to CPW feedthrough</i>	54
4.9 <i>VTT CPW to CPW feedthrough simulation results</i>	54
4.10 <i>D2 CPW to stripline feedthrough</i>	55
4.11 <i>D2 CPW to stripline feedthrough simulation results</i>	56
4.12 <i>A CPWG line one layer above a ground plane (DiPak)</i>	56
4.13 <i>A CPWG line one layer above a ground plane (VTT)</i>	57
4.14a <i>DiPak Feedthrough</i>	57
4.14b <i>Feedthrough modified for VTT</i>	57
5.1 <i>Side view of stripline to stripline vertical transition</i>	62
5.2 <i>3D view of stripline to stripline vertical transition</i>	62
5.3 <i>Stripline to stripline vertical transition (Gipprich)</i>	63
5.4 <i>Return loss curves for different via and pad sizes in the DiPak stripline to stripline vertical transition</i>	65

5.5 Smith chart comparison of S_{11} for DiPak stripline to stripline vertical transition (effect of via pad).	67
5.6 Smith chart comparison of S_{11} for DiPak stripline to stripline vertical transitions (effect of via diameter).	69
5.7 Return loss comparison of two DiPak stripline to stripline vertical transitions (effect of ground plane hole).	70
5.8 Smith chart comparison of two DiPak stripline to stripline vertical transitions (effect of ground plane hole).	71
5.9 Representation of electric fields in a stripline to stripline vertical transition	72
5.10 Representation of electric fields in a stripline to stripline vertical transition with a large ground plane hole	72
5.11 Representation of parallel plate modes that can propagate near a stripline to stripline vertical transition	73
5.12 A via fence used to connect two ground planes	75
5.13 D1 return loss comparison of stripline to stripline vertical transition with via fence and PAB	76
5.14 3D view of D1 stripline to stripline vertical transition showing PABs	76
5.15 3D view of D2 stripline to stripline vertical transition showing PAB	77
5.16 Lack of improvement realized by using PABs in D2 stripline to stripline vertical transition	77
5.17 Simplified 3D diagram of a stripline to CPW vertical transition	79
5.18 3D view of a D2 stripline to CPW vertical transition	80
5.19 3D view of VTT stripline to CPW vertical transition	81
5.20 Comparison of return loss for D1 and D2 simulation results for the stripline to CPW vertical transition	82
5.21 Simulations demonstrating return loss variation in a stripline to CPW vertical transition with CPW gap size	84
5.22 Return loss of VTT stripline to CPW vertical transition	84
5.23 A CPWG line with a pseudo air-bridge	86
5.24 Improvements in D1 stripline to CPW vertical transition from PAB	86
5.25 Lack of improvement realized by using PABs in D2 stripline to CPW vertical transition	87
5.26 S_{11} of the D2 stripline to CPW vertical transition	89
5.27 3D view of a quarter-wave transformer added to the D2 stripline to CPW vertical transition	90
5.28 Return loss of D2 stripline to CPW vertical transition using a quarter-wave tuning section	90
5.29 3D view of stripline to shorted CPW vertical transition (D2)	91
5.30 Return loss of stripline to shorted CPW vertical transition (D2)	92
5.31 3D view of a CPW to CPW vertical transition	93
5.32 3D view of the VTT CPW to CPW vertical transition	94
5.33 Simulation results for the VTT CPW to CPW vertical transition	94
5.34 S_{11} Smith chart plot of VTT CPW to CPW vertical transition	95
5.35 3D view of a CPW to microstrip vertical transition	97
5.36 3D view of the VTT CPW to microstrip vertical transition	98

5.37 Simulation results for the VTT CPW to microstrip vertical transition	98
5.38 S11 Smith chart plot of VTT CPW to microstrip vertical transition	99
6.1 S11 Smith chart plot of D2 stripline to stripline vertical transition	102
6.2 Circuit model of stripline to stripline vertical transition	102
6.3 Comparison of simulated and modeled return loss for case a)	104
6.4 Comparison of simulated and modeled return loss for case b)	105
6.5 Comparison of simulated and modeled S11 for case b)	105
6.6 Comparison of simulated and modeled return loss for case c)	106
6.7 Comparison of simulated and modeled S11 for case c)	107
6.8 Comparison of simulated and modeled return loss for case d)	108
6.9 Comparison of simulated and modeled S11 for case d)	109
6.10 S11 Smith chart of VTT stripline to CPW vertical transition	113
6.11 Circuit model of stripline to CPW vertical transition	114
6.12 Comparison of return loss for circuit model and simulation for VTT stripline to CPW vertical transition	114
6.13 Comparison of S11 for circuit model and simulation for VTT stripline to CPW vertical transition	115
6.14 S11 Smith chart of VTT CPW to CPW Vertical Transition	117
6.15 Lumped element model of VTT CPW to CPW Vertical Transition	117
6.16 Circuit model versus HFSS simulation of Return Loss of VTT CPW to CPW Vertical Transition	118
6.17 Circuit model versus HFSS simulation of S11 of VTT CPW to CPW Vertical Transition	118
6.18 Smith chart plot of S11 for VTT CPW to Microstrip transition	120
6.19 Circuit model of VTT CPW to Microstrip Transition	120
6.20 Circuit model versus HFSS simulation of Return Loss of VTT CPW to Microstrip Vertical Transition	121
6.21 Circuit model versus HFSS simulation of S11 of VTT CPW to Microstrip Vertical Transition	121
7.1 Microscope photograph of Microstrip change in width	125
7.2 Microscope photograph of CPW line becoming embedded	125
7.3 Microscope photograph of CPW short circuit	126
7.4 Microscope photograph of Microstrip line	127
7.5 Microscope photograph of grounding via	128
7.6 Microscope photograph of via pad	128
7.7 Microstrip TRL Standards	130
7.8 Back-to-back microstrip quarter-wave transformers and TRL lines	131
7.9 Microstrip to stripline feedthroughs and TRL standards	132
7.10 Stripline to CPW Vertical Transitions	134
7.11 Measured results for a 1.3 mm microstrip through line	135
7.12 Measured results for a 2.4 mm microstrip delay line	135
7.13 Measured results for a back-to-back microstrip quarter-wave transformer (TRL calibrated)	136

7.14 Measured results for a back-to-back microstrip to stripline feedthrough	137
7.15 Measured results for a back-to-back stripline to CPW vertical transition	138
7.16 Measured results for a back-to-back stripline to CPW vertical transition with posting vias	138
7.17 Measured results for a back-to-back stripline to CPW vertical transition with posting vias and PAB grounding	139
7.18 Measured results for a back-to-back stripline to CPW vertical transition after SOLT calibration	140
7.19 Comparison of measurement and simulation for microstrip to stripline feedthrough	141
7.20 Comparison of measurement and simulation for stripline to CPW vertical transition	142
7.21 Ground plane arrangements for coplanar circuits	143
7.22 Pseudo air-bridge use with microstrip lines and ground planes	144
7.23 PAB use with coplanar line	144
7.24 CPW TRL standards, dimensions in mm	145
7.25 CPW to CPW feedthroughs, dimensions in mm	146
7.26 CPW to microstrip vertical transitions, dimensions in mm	147
7.27 CPW to CPW vertical transitions, dimensions in mm	148
7.28 Measured S-Parameters of 1.5 mm CPWG through line	150
7.29 Measured S-Parameters of 2.7 mm CPWG line	150
7.30 Measured S-Parameters of 5 mm CPW to CPW feedthrough	151
7.31 Measured S-Parameters of 6 mm CPW to CPW feedthrough	152
7.32 Measured S-Parameters of CPW to microstrip vertical transition (circuit 7a)	153
7.33 Measured S-Parameters of CPW to microstrip vertical transition (circuit 7b)	153
7.34 Measured S-Parameters of CPW to microstrip vertical transition (circuit 7c)	154
7.35 Measured S-Parameters of CPW to microstrip vertical transition (circuit 7d)	154
7.36 Measured S-Parameters of CPW to CPW vertical transition (circuit 8a)	155
7.37 Measured S-Parameters of CPW to CPW vertical transition (circuit 8b)	156
7.38 Measured S-Parameters of CPW to CPW vertical transition (circuit 8c)	156
7.39 Measured S-Parameters of CPW to CPW vertical transition (circuit 8d)	157
7.40 The scraped exposed conductor. The vertical transition is on the left side of the picture. The probes touched down on the right-hand side.	158
7.41 Measured S-Parameters of half of circuit 8a, cut as in Figure 7.40.	159
7.42 Measured S-Parameters of half of circuit 8c, cut as in Figure 7.40	159

8.1 One-Port measurement of 1.5mm CPWG line	166
8.2 One-Port measurement of 2.7 mm CPWG line	166
8.3 Comparison of Momentum simulation and measured data for 1.5 mm CPWG line (1 port).	168
8.4 Comparison of Momentum simulation and measured data for 2.7 mm CPWG line (1 port).	168
8.5 HFSS 3D view of 1.5 mm line	170
8.6 HFSS 3D view of 2.7 mm line	171
8.7 HFSS simulation versus measurement for CPWG lines	172
8.8 S-Parameters of Ground-Reduced CPW lines	174
8.9 S-Parameters of Ground-Reduced CPW lines	174
8.10 Original: CPW sides overhand intermediate ground plane	175
8.11 Cut: CPW sides same length as intermediate ground plane	175
8.12 Silver paint increasing the width of a CPW ground plane. The dotted line indicates the area where the silver paint was used to extend the length as well as the width.	176
8.13 Comparison S11 of different CPW grounds in One-Port measurement of 1.5 mm CPW through line.	177
8.14 Comparison S11 of different CPW grounds in One-Port measurement of 2.7 mm CPW delay line.	177
8.15 Comparison S11 of different CPW grounds in One-Port measurement of 1.5 mm CPW through line.	178
8.16 Comparison S11 of different CPW grounds in One-Port measurement of 2.7 mm CPW delay line.	178
8.17 Silver paint extensions for CPW to CPW vertical transitions	179
8.18 Comparison of S-Parameters for two different ground extensions on the CPW to CPW vertical transition.	180
8.19 Comparison of S-Parameters for two different ground extensions on the CPW to CPW with PAB vertical transition.	180
8.20 CPW to microstrip vertical transition with different ground extensions.	181
8.21 Comparison of S-Parameters for two different ground extensions on the CPW to Microstrip vertical transition.	182
8.22 Comparison of S-Parameters for two different ground extensions on the CPW to microstrip with PAB vertical transition.	182
8.23 Leaky waves (after [34])	184

I: Introduction

1.1: Trends in Data Transmission

Over the last decade the Internet has grown dramatically, from 1,313,000 domains in Jan 1993 to 93,047,785 domains currently [Internet Software Consortium: www.isc.org]. As a result of such enormous growth, existing Internet applications are seeking to expand their services while new organizations seek to provide services in this growing market. With few exceptions, new proposed Internet services are all high bandwidth applications, such as video-on-demand, online gaming, television broadcasting, tele-conferencing, and tele-medicine. These applications are being proposed to operate over the current Internet infrastructure. For these applications to be successful a high-speed data connection is essential.

Initially, all Internet accesses were achieved using conventional modems over telephone lines. These modems connected the user to Internet Service Providers (ISP) who connect to the Internet backbone. As the Internet grew, phone line modems increased in speed, from 300 baud initially to 56 kbit/s currently. Other organizations recognize the need for high-speed connections: cable television companies offer Internet connections via coaxial cable and telecommunications companies offer high-speed

Digital Subscriber Loops (DSLs). These connections are significantly faster than existing phone-line modems, DSL fastest, with speeds up to 6.1 Megabits/s out of a theoretical 8.448 Megabits/s. Typically, individual DSL lines operate at 1.544 Megabits/s downstream and 128 kbits/s upstream.

The following table illustrates the needed connection speed required for transmission of different video qualities (video can be used as a comparative measure since most new Internet applications involve video).

Table 1.1: Data rate for various video qualities (Standard Resolution) (After [1]).

Video Quality	Data Rate (Mb/s)
Studio	200
Perfect domestic reception	8
High quality domestic reception	5
Acceptable for movies	2

In order to implement these large bandwidth applications a high-speed data connection must meet the specifications listed above. This connection must also provide the needed bandwidth at a reasonable cost. Unfortunately, the existing high-speed data connections (DSL and cable) cannot approach the high data speeds required.

A direct fiber-optic connection to the home or business has been proposed to provide a high-speed connection. This plan has extremely fast data transfer, but it is very expensive. The one-time costs in deploying the fiber (roadwork and other construction)

are enormous, and maintenance costs due to broken fibers will continue to keep costs high.

A wireless connection is a possibility that is being explored. This connection could be deployed quickly, with participating homes simply attaching antennas to their roofs, keeping infrastructure costs minimal.

Figure 1.1: An LMCS Configuration

A wireless connection would be a viable option if high data speeds could be achieved. High speeds are possible, but require a large bandwidth, and the very high speeds that are discussed here will require an enormous bandwidth.

Policy makers in North America and Europe have decided that the strengths of such a wireless system overcome their weaknesses, and have allocated large blocks of spectrum for wireless data communication systems. The United States has allocated 1300 MHz for Local Multipoint Distribution Systems (LMDS) and Canada has allocated 3 GHz for its equivalent system Local Multipoint Communications Systems (LMCS). This wide bandwidth was not available at lower frequencies, so it has been allocated in

the high microwave / low millimetre-wave range. LMCS/LMDS applications have been allocated in the 25-31 GHz range.

Table 1.2: LMCS Frequency Bands in Canada (After [1])

Band	Frequency Range (GHz)	Bandwidth (MHz)
A	27.85-28.35	500
B	27.35-27.85	500
C	26.85-27.35	500
D	26.35-26.85	500
E	25.85-26.35	500
F	25.35-25.85	500

Table 1.3: LMDS bands in the USA (after [1])

Block	Bands (GHz)	Bandwidth (MHz)
A (1150 MHz)	27.50-28.35	850
	29.10-29.25	150
	31.075-31.225	150
B (150 MHz)	31.000-31.075	75
	31.225-31.300	75

The previous tables indicate only North American spectrum allocations, and to be complete it must be stated that there have been LMCS/LMDS spectrum allocations worldwide. Many nations allocate at least 1 GHz of spectrum in the frequency range of 20 GHz – 40 GHz.

Consider the 850 MHz of unrestricted bandwidth of the US implementation. This can potentially provide (depending on modulation, frequency re-use, and polarization choices) 51.84 – 155.52 Megabits/s downstream and 1.544 Megabits/s upstream per cell. Mm Tech Inc. states that, with 1 GHz of spectrum, “an all-video system could provide up to 288 channels of digital broadcast quality television plus on-demand video services. Fast data, Internet access, PCS backhaul, local loop bypass, digital video, digital radio, work at home, and tele-medicine are all possible. In fact, they are all possible within the same cell” [www.mm-tech.com]. Canada has allocated 2.5 times the spectrum of the US, and will be able to provide increased services as a result.

However, the high microwave frequencies allocated for LMCS/LMDS have a difficult propagation problem since at such high frequencies, atmospheric attenuation is high. Figure 1.2 shows attenuation vs. frequency, including the molecular absorption bands, and the effect of fog and rain on wireless transmission (note that foliage can also increase signal attenuation).

Figure 1.2: Attenuation vs. Frequency (after [1])

From the graph shown above, at 30 GHz, attenuation can vary from 0.2 dB/km to 20 dB/km, depending on the environmental conditions. With such high attenuation, LMCS/LMDS systems require line-of-sight propagation paths (maximum 1-3 km in length) simply to function. To achieve a reliable system, circuits for LMCS/LMDS networks must be high gain to account for the losses in the transmission. However, LMCS/LMDS systems are also required to be low-cost, if the technology is to be available to residential customers.

Volume production will lower costs, but may not lower costs to the point where a residential customer can afford the technology. Decreasing the number of components is vital. To this end, research is conducted to increase the integration of on-chip components, to build the “system on a chip”. However, this research has difficulty integrating filters, as well as large values of capacitance and inductance.

Low Temperature Co-fired Ceramics (LTCC) is a promising packaging technology that, through vertical stacking, can integrate passive components into the package substrate. This feature could eliminate the need to purchase off-chip components, lowering system cost. This reduces total circuit size, another important cost factor, and can improve system performance by eliminating line discontinuities encountered from multiple packages. This thesis investigates the possibilities and difficulties in changing the circuit package from a structural necessity to an essential part of a microwave system.

1.2: Objectives

The objective of this thesis is to determine if Low Temperature Co-fired Ceramic packages can be used for the packaging of LMCS/LMDS circuitry. For LTCC packages to achieve the levels of integration required to lower costs there must be a library of well-mapped, repeatable, and simple planar and vertical transitions for designers to use. To this end, transitions and interconnects that would allow high integration are simulated, measured, and discussed.

This thesis is arranged as follows: Chapter Two details the manufacture of LTCC packages, and reviews published work in this area. Chapter Three examines transmission lines from a theoretical point of view, and examines their usefulness as 3D circuitry. Chapter Four presents simulated results of three different transmission line feedthroughs, and Chapter Five presents simulated results of four vertical transitions. Chapter Six details a circuit model for the vertical transitions of chapter Five and uses the model to

understand transition behaviour. Chapter Seven contains measured results and comparisons to simulation. Chapter Eight investigates differences between measurement and simulation, and finally conclusions and future work are described in chapter Nine.

II: Low Temperature Co-fired Ceramics

2.1: Current Microwave Packaging

A circuit package is no longer simply the receptacle in which a previously designed circuit is placed. At high frequencies, package effects can radically change the operation of the circuit within. Surface modes can excite cavity resonances, which interfere with circuit operation. Add hermeticity requirements to this already difficult endeavor, and packaging becomes an issue that must be considered from the beginning of the circuit design cycle.

Figure 2.1: Levels of Packaging (after [2])

Currently, many RF (RFICs – Radio Frequency Integrated Circuits) and microwave circuits (MMICs – Monolithic Microwave Integrated Circuits) are packaged in custom metal cases and attached to coaxial or SMA connectors.

Figure 2.2: Custom metal microwave package (1.8 – 26.0 GHz Amplifier from Atlantic Microwave Ltd.)

Custom metal packages can hold multiple chips or chip sized packages as well as planar lines and passive components such as couplers. This approach is well-suited for microwave packages because unwanted resonances are suppressed by metal trenches that short circuit the package lid to the package bottom. However, these packages are expensive, usually custom made, and heavy.

Some microwave circuits can be packaged on ceramic substrates as surface mount (SMT) or ball-grid array (BGA) packages. Typically, there are conductive traces printed on the package substrate that are wire-bonded or ribbon-bonded (or flip-chip mounted) to the Si/SiGe or GaAs MMIC being packaged. These packages are then affixed to carrier boards or into custom packages as described above through metal pads (surface mount)

or solder bumps (BGA). Each package typically holds one active chip and, potentially, several off-chip capacitors.

Figure 2.3: BGA MMIC package (from www.hdcom.com)

Microwave substrates typically contain little more than bare MMIC dice. Custom metal packages have the ability to hold components that cannot be integrated as MMICs, but these contribute to large sizes and weights. SMT or BGA packages can fit some off-chip capacitors into the package, but rarely anything else. Other components, such as high Q inductors or ceramic filters, are placed outside the ceramic package. This causes a discontinuity in the path from circuit to off-package component. Complex paths introduce loss and can degrade performance. The higher the operating frequency the more detrimental these effects become.

One method to reduce these parasitics is to increase integration. If all the components were in the same package then the distance traveled would decrease as well as the line discontinuities. Low Temperature Cofired Ceramics, a more integrated packaging technology, can potentially solve this problem.

2.2: The History of Low Temperature Co-fired Ceramics

The problem with lossy connection paths was originally encountered by the computer industry except, instead of losses, the problem was line delay.

Computer speeds were limited by long path delays found in through-hole technology (THT) packages. Out of this problem surface mount technology (SMT) developed to reduce these transit times. SMT packages again became the bottleneck, due to the time required for signals to propagate from one package to the next. Realizing that speeds could increase if the chips were closer together, multi-chip modules (MCM) were introduced. MCMs reduce transit time by providing a medium that can integrate several bare circuit dies on the same substrate. Since the bare chips are much closer together, the travel time from one to another is significantly reduced. The substrate in a multi-chip module supports the dies as well as provides the interconnections between them.

There are several different versions of MCMs available. They are usually categorized by substrate type and have been defined by the Institute for Interconnecting and Packaging Electronic Circuits (IPC) (from [2]).

- **MCM-L: (Laminated) Substrates based on laminated multilayer PCB technology.**
- **MCM-C: (Ceramic) Substrates based on co-fired ceramic or glass ceramic technology.**
- **MCM-D (Deposition) Interconnection pattern formed by the deposition of dielectrics and conductors, on a base substrate, typically by thin film process.**

MCM-L packages are low-cost, low-performance packages. They are typically made from FR4 epoxy-glass with copper foil conductors. They are mainly used for high volume, low cost applications, and are not suited for microwave applications due to the lossy nature of the FR4 substrate and the lack of precise conductor definitions.

On the other end of the spectrum is MCM-D. This high-cost, high performance technology is similar to IC design. "MCM-D uses a naked die on a silicon or aluminum base structure that supports a multi-layer, high density metal-polyamide interconnection structure" [2]. The interconnection patterns are formed by depositing dielectrics and conductors on a base substrate, typically by a thin film process. The complete fabrication process involves using deposition or thermal growth to create materials on the wafer, followed by photolithography for pattern definition. The wafers are then etched; this process is repeated for each mask. The process is expensive and difficult and MCM-D programs typically have volume problems [2]. However, the packages that do work have excellent RF/microwave properties, such as low-loss conductors and high Q components (1.6 nH inductor with a Q of 107 at 10 GHz [3]). Unfortunately for MCM-D, commercial markets operate on the principle of lowest cost rather than on best performance. An application such as LMCS/LMDS requires low-cost and repeatable packages to achieve market success. Therefore, in between these two MCM processes is MCM-C.

MCM-C packages have substrates based on cofired ceramic or glass ceramic technology, and have been around for more than 25 years [2]. Initially, this ceramic technology was used to make chip capacitors, followed by single-chip packages. Sherwani [2] claims that IBM was the first to make breakthroughs with this technology,

using alumina substrates for mainframes. There are several types of MCM-Cs: LTCC, HTCC (High Temperature Cofired Ceramic), and Aluminum Nitride (AlN) [2].

2.3: The Manufacture of MCM-C

Regardless of the MCM-C type, the fabrication procedure is the same (see figure 2.4). “First, a liquid slurry is formed from ceramic particles and organic binders and cast into a solid sheet called green tape. Via holes are drilled or punched on to the green tape sheets. A conductive ink is applied to each sheet to form the conductive pattern by using a screen printing process while a vacuum is applied to the other side of the punched green sheet to pull the ink into the via holes to coat the side walls of the holes or to fill the holes completely. Screen printing refers to a thick film process in which a paste or ink is squeezed through open areas of a screen and transferred to the surface of the green tape sheet to form geometric patterns such as signal paths” [2]. If the holes are filled completely with conductive ink they are referred to as solid vias, and have the advantage of being able to be stacked directly on top of each other. Finally, all the green tapes with conductive patterns on them are stacked and cofired to form a complete structure of interconnections. The green tapes of HTCC materials are fired at 1500 degree Celsius, while the green tapes of LTCC materials are fired at temperatures about 800 degrees. A well known type of MCM-C is alumina, a form of HTCC popular in the microwave industry.

Figure 2.4: The creation of an MCM-C package (after [4])

2.4: LTCC vs. HTCC

There are two main reasons why LTCC is being investigated in this thesis as opposed to HTCC.

Metal Conductivity: The low firing temperature of LTCC allows low-loss conductors such as gold and silver to be used as conducting strips. Brown et al [5] write that “low loss conductors necessary for acceptable performance of many microwave systems had limited the use of high temperature ceramics which require the use of lossy tungsten metallization due to the high firing temperatures required”. In packages designed for the microwave and millimeter wave market, it is extremely important to minimize both conductor and dielectric losses, which can seriously hamper circuit

performance. Gold and silver tracks help reduce conductor loss by increasing the conductivity of the metal (tungsten has half the conductivity of silver and gold).

Embedded Passives: Figure 2.4 shows the construction of an LTCC package, explicitly indicating the firing of several layers, each with conducting tracks and vias. Typically with HTCC packages, such as alumina, embedded conductors are not used. Either lossy conductors are used before firing as previously described, or low-loss metals are added to a post fired piece of ceramic. The advantages of LTCC result from the embedding of high-conductivity conducting tracks. HTCC can provide either embedded tungsten conductors, or single layer gold conductors, but not both.

2.5: Challenges with Low Temperature Co-fired Ceramics

LTCC can be separated into two sub-categories: LTCC, and LTCC-M (LTCC on Metal). A disadvantage of LTCC is that it shrinks in the x, y, and z directions upon firing. Sarnoff Corporation solved this problem by developing LTCC-M (LTCC on Metal). LTCC-M is fabricated by cofiring the ceramic sheets on a metal core formed from Copper-Molybdenum-Copper (CoMoCo). The ceramic layers attach to the metal and prevent the ceramic from shrinking in the x and y directions. The metal core also has a secondary function as a heat sink. This process was licensed by Sarnoff to Dielectric Laboratories, and commercialized as “DiPak”. Currently the most common manufacturing process is LTCC, with LTCC-M being used only by Sarnoff Corp. and Dielectric Labs.

In LTCC foundries, manufacturers can predict the level of 'xy' shrinkage ($\pm 0.3\%$) and use this knowledge to ensure that the appropriate final design is reached. However, because of this shrinkage, solid ground planes (in the 'xy' plane) are not possible, because the ceramic layers and the metal conductors do not shrink at the same rate. Therefore, in LTCC packages, meshes of conductor strips approximate large ground planes. These meshes perform worse than unbroken ground planes, and this has been discussed in the literature [6]. Because of the lack of 'xy' shrinkage in LTCC-M packages, solid ground planes can be fabricated without problems. In both LTCC and LTCC-M, however, complete ground planes are not possible, as space must always be left to allow the ceramic layers to bond together. Thus, LTCC package ground planes are limited by ceramic shrinkage while LTCC-M ground planes are limited by ceramic bonding. As a result of the CuMoCu former in LTCC-M, shrinkage and uncertainty in 'z' is much larger. DuPont 943, a brand of LTCC, has 'z' shrinkage of $12.3 \pm 0.3\%$ versus $30 \pm 10\%$ for the DiPak LTCC-M process.

Shrinkage in 'z' can lead to some defects, such as 'posting', where a via remains the same height but the layer through which it passes shrinks, causing the pads that meet the vias on the layers above and below to be pushed out of their optimum position. This is due to the fact that the vias are filled (referred to as solid vias), and the conductive ink that fills the via does not shrink along with the ceramic.

Figure 2.5: Via posting

The longer the via, the worse the posting problem. Posting is prevented by avoiding large stacks of vias.

A key factor in package design is the ability of the package to manage heat dissipation. For a transmit module with a large power amplifier, it becomes crucial to carry the heat away from the MMICs performing the amplification. Generally speaking, LTCC packages are poor conductors of heat. However, thermal conductivity can be improved by using thermal vias to carry heat from hot microwave semiconductor devices to a metal core or a heat sink mounted on top of the package. Also, the coefficient of thermal expansion (CTE) of the package material becomes critical. The CTE of a material is defined as the fractional increase in length per unit rise in temperature. Ideally, the CTE should be matched to GaAs (or Si, depending on the application) so that the active device remains attached to the package. The CTE of most commercial brands of LTCC and LTCC-M is set to match closely with GaAs.

2.6: Advantages of Low Temperature Cofired Ceramics

In the most basic terms, Low Temperature Cofired Ceramics provide multi-level packages. These packages can reserve levels for DC routing, levels for RF and microwave signals, and several layers for buried lumped elements. Several active chips can be mounted in the package, from RF amplifiers and downconverters to DC tuning elements such as varactors (see Figure 2.6 for an example). By allowing multiple active circuits to be mounted on the same package substrate along with all their attendant off-chip components, LTCCs can not only create complete systems in a package, but also eliminate the need to go off-package for any components and hence improve circuit performance.

Figure 2.6: An LTCC-M package with several active devices (after [7]).

As frequencies go up, the industry is faced with another conflicting trend – falling prices. The cost of a design that includes many off-package components is more expensive than one with all integrated components. Amey et al reported that if 25% of passives in a cellular phone handset could be embedded into the substrate as in an LTCC package, a \$4.00 per unit savings would result [8]. These studies have interested industry in LTCC technology, and a consortium of six companies (CTS Microelectronics, DuPont Microcircuit Materials, Heraeus Cermalloy, Kyocera, Motorola, and National Semiconductor) have formed the Ceramic Interconnect Initiative (CII) to promote the advantages of ceramic-based packaging. These industries are interested in the cost-reduction and performance-enhancing capabilities of LTCC packages.

In the following table, the manufacturers of DiPak have compared different packaging techniques. Note that they assume HTCC to be used with post-fired high-conductivity metal.

Table 2.1: Comparing packaging technologies - from www.dipak.com

	HTCC	MCM-L	MCM-D	LTCC	DIPAK
Ruggedness	High	High	Poor	Poor	High
Component Assembly Flexibility	Fair	Fair	Fair	Fair	Good
Buried Passives	No	Resistors Only – Limited Expensive	Resistors & Decoupling Capacitors - Expensive	Resistors and Capacitors - Poor Yield	Resistors and Capacitors *
Flip Chip Capability	Good	Good with Underfill	Good	Good	Good
Cost	Medium	Low	High	Medium	Low
Wiring Density (cm/cm²)	300	200	800	300	300-600
Thermal Conductivity (% of Cu)	.05	.01	20	.1	50
Large Format Processing	Yes (Shrinkage)	Yes	No	Yes (Shrinkage)	Yes

TCE Matched To GaAs/Si	Poor/Fair	Poor	Good	Fair	Good
Applicability to High Frequency Applications	Good	Good to 2 GHz	Yes (Materials Dependent)	Good / Excellent	Excellent

* papers have demonstrated inductors in DIPAK as well, see [9].

This table demonstrates that the last two columns (representing LTCC and LTCC-M) have advantages over the other packaging techniques. Only HTCC and MCM-D have good applicability to high frequency applications, and HTCC does not allow buried passives and MCM-D is very expensive. This points to LTCC and LTCC-M as excellent packaging technologies.

There are several types of LTCC on the market currently. The main types are: DuPont 951, DuPont 943, Ferro A6, and DiPak. DuPont 951 is DuPont's standard Green Tape process, and DuPont 943 is their high-performance Green Tape for high frequency applications. Each of these technologies has slightly different dielectric constants, layer thicknesses, and loss tangents.

Table 2.2: Characteristics of different LTCC types.

Characteristic	DuPont 951	DuPont 943	Ferro A6	DiPak
Dielectric Constant	7.8 (at 3GHz)	7.5 at 10 MHz 7.1 at 20 GHz [10]	5.9 (at 3 GHz)	5.67 (at 12.5 GHz)
Layer Thickness	114 μm (4.5 mil) 165 μm (6.5 mil) 254 μm (10 mil) all +/- 7%	107 μm fired	1.5 mil 3.7 mil 7.3 mil	5 or 6.5 mils +/- 10%
Loss Tangent	0.0043 (at 3GHz)	0.001 (at 1 MHz)	0.002 (at 3 GHz)	0.003 (at 12.5 GHz)

These loss tangents and dielectric constants are not constant with frequency.

These following graphs characterize DuPont 943 over a range of frequencies. Figure 2.7 shows the relationship between loss tangent and frequency. Figure 2.8 plots attenuation vs. frequency.

Figure 2.7: Loss tangent of several materials versus frequency (after [10])

Figure 2.8: Attenuation versus frequency for several different materials (after [10])

Note that these curves contain no information about line roughness or line widths, crucial parameters when measuring line attenuation. Nor is it known if all lines were manufactured by the same company. As LTCC is a new technology, foundries have not yet determined the limits of their processes, making many design rules flexible.

However, research into LTCC and LTCC-M has produced several prototype packages to verify the advantages and potentials in this material.

2.7 LTCC Packages

There have been packages produced in LTCC that use passive elements alongside mounted active elements. Michael O'Hearn [11] designed a frequency synthesizer module that contains a BiCMOS PLL, a VCO and the loop filter. This package utilized a 10 layer LTCC package from National Semiconductor, with 4 capacitors and two inductors buried in the ceramic. In fact, the entire loop filter was buried in the ceramic. This package was designed for the North American AMPS cellular standard (869 MHz – 894 MHz), and the author claims that the module “can reduce printed circuit board real estate requirements by as much as 400%”[11].

Consolazio et al [12] mount three MMIC amplifiers in cavities in a three layer LTCC package to produce a broadband high gain circuit from 2 – 18 GHz. The LTCC used was DiPak from Dielectric Laboratories. Figure 2.9 shows the multilayer nature of the amplifier package. Notice that there are no RF vertical connections; the lines start on layer 2 and proceed straight through the package, most likely being wire bonded to the MMIC amplifiers. The embedded passives are resistors (2k) and capacitors (200 pF), all located on layer 2.

Figure 2.9: LTCC-M amplifier (after [12])

Kopp and Axness [13] have developed a wide-bandwidth X-band (7-10 GHz) receive module in an LTCC package. This package includes four GaAs MMICs for RF functions and silicon ICs for control functions. All RF lines were created in microstrip and attached to the MMICs with gold ribbon. This design did not use the multilayer features of LTCC packages, but illustrates their suitability for multi-chip modules and mixed analog-digital environments.

There have also been several designs in the 20 GHz range. Sturzbecher et al [14] use an LTCC package that has no bottom ground plane to create a 20 GHz phased array module, with the radiating elements on one side (the 'bottom') with the phase shifters and amplifiers on the other (the 'top'). The authors describe the packaging effort as follows: "The development of high-performance, solid-state, phased array antennas relies directly on the ability to integrate and operate a large amount of complex circuitry in a small physical volume. This packaging challenge is increasingly difficult as operating frequencies move into the K and Ka-bands, where radiating element spacing decreases to

fractions of a centimeter and the available space behind the radiators approaches the size of the MMIC devices alone. Furthermore, the packaging is further constrained by the requirements that each MMIC be individually controlled, electrically isolated, and protected from environmental hazards". [14]

To meet the specifications detailed above, the devices that drive the array elements are placed behind the elements (see Figure 2.10).

Figure 2.10: Phased array design (after [14])

The RF design is done in microstrip and (presumably) wire-bonded or connected by ribbon to the phase shifters and amplifiers. The radiating elements are probe fed by vias that descend from the 'top' through the LTCC substrate. The only RF vertical connections in this circuit are the probes that feed the radiating elements. All other RF connections are strictly planar.

Also at 20 GHz, Lester et al [15] developed a downconverter in an LTCC package that includes a buried stripline filter (bandpass at 1.55 GHz). The LTCC used is DuPont 851 fired ceramic, fabricated by CTS Corporation. Although this implementation uses stripline, there are no vertical RF connections. In Figure 2.11, it can be seen that the

stripline converts to microstrip simply by emerging into a cavity. The top ground plane of the stripline disappears and the line continues as microstrip.

Figure 2.11: LTCC Stripline package (after [15])

This design also uses the top layers for DC routing, and vias are used to bring the MMIC biasing voltages down into the cavity.

Gipprich et al [16-18] have developed a coupling circuit that is fabricated in LTCC, using many of the features that are discussed in this thesis. The LTCC used is Ferro type A6 LTCC. Their paper discusses the creation of a compact coupler network for combining six high efficiency HBT power MMICs in the frequency range of 8-14 GHz. In their design, stripline was used as the transmission line of choice, and was used in 3 dB and 4.77 dB couplers as well as vertical transitions. The vertical transition used in this paper was a stripline to stripline transition and will be discussed further. An interesting design was used in the creation of the couplers. The 3 dB coupler was formed by completely overlapping the two stripline elements, and used capacitive tuning to optimize the insertion and return losses. This capacitive tuning was implemented using

metal pads connected with vias to the top and bottom stripline ground planes. This coupler design can be seen below:

Figure 2.12: LTCC Stripline coupler (after [18])

2.8: The Need for Research on Vertical Transitions

There has yet to be a package produced that truly exploits the multilayer capabilities of Low Temperature Cofired Ceramics in the microwave/millimetre-wave range. This lacuna is due to the lack of adequate vertical transitions available to the package designer. If a library of suitable transitions were available then LTCC packages could be used much more often. Examples have demonstrated planar microwave circuits and transmission lines, with one notable exception (Gipprich et al: [16-18]). Since multilevel circuits are possible and highly beneficial for low frequency applications ([8], [11]), now is the time to produce full 3D microwave packages.

III: Transmission Line Theory

3.1: Transmission Lines for a 3D Environment

A key consideration for any design is the choice of transmission line. LTCC packages offer the designer a choice of transmission lines, and indeed, a package designer can switch from one type of line to another to best suit the application at hand.

A designer will encounter the following two design environments:

- 1) The transmission line is encased in the ceramic;
- 2) The transmission line is open to air.

If the transmission line is open to air, it is likely to be either on the top of the package or in a cavity. Here the choice of transmission lines is limited, as these lines are used primarily to interface with other equipment. The lines that are likely to be used on top of the package or in a cavity are usually used to connect to MMICs or other devices. These lines are also used to connect the LTCC package to a carrier board. Microstrip is commonly used to interface with MMICs and to connect to carrier lines. Coplanar waveguide can also be used in both these circumstances, especially with flip-chip

mounted MMICs. The choice between these two different transmission lines will largely be made for the package designer by the active devices that must be included in the package.

Loss in transmission lines comes from the following:

- 1) Dielectric loss
- 2) Conductor loss
- 3) Radiation loss

Dielectric loss in LTCC packages occurs when an electric field partially or entirely passes through a dielectric material. When comparing microstrip and coplanar waveguide, for instance, the CPW line will have lower dielectric loss, as the fields in CPW are mostly split between air and ceramic, as opposed to a microstrip line, where the fields are almost entirely contained within the dielectric below the microstrip line.

Conductor loss is a function of the conductivity of the conducting metal, as well as the geometrical arrangement of the conductor. In LTCC packages, high conductivity metals are used for both exposed and embedded conductors.

Radiation loss can be defined as power lost into unwanted modes. These unwanted modes can be radiating modes, such as leaky surface waves, or they can be substrate and parallel plate modes that cause power loss. The unwanted modes for each transmission line will be discussed.

3.2: Microstrip

Microstrip lines are formed by placing a strip conductor over a ground plane as illustrated in figure 3.1. In the dominant mode, the E field lines stretch from the conductor to the ground plane, and are concentrated mostly below the conductor. However, since not all the E field is located within the dielectric, microstrip is not a TEM transmission line, rather it is a quasi-TEM line.

Figure 3.1: A microstrip line

Most of the E field lines pass through the dielectric, and this results in dielectric loss. This loss is difficult to reduce in LTCC packages. Current crowding adds to conductor loss and begins to take effect if the conductor is very thin with respect to the height above the ground plane.

Surface Modes:

“For any nonzero thickness slab, with a permittivity greater than unity, there is at least one propagating TM mode, which we call the TM_0 mode. This is the dominant mode of the dielectric slab waveguide, and has a zero cutoff frequency” [19]. Therefore,

at microstrip discontinuities, there is a risk of exciting the TM_0 mode. The next higher order mode for the dielectric slab is the TM_1 mode, with cutoff frequency given by Pozar [19] as:

$$f_c = \frac{c}{2d\sqrt{\epsilon_r - 1}}$$

With a slab height of $d = 107 \mu\text{m}$, and $\epsilon_r = 7.1$, $f_c = 567 \text{ GHz}$. Therefore this mode is not a concern for a microstrip line fabricated in the DuPont 943 process. There is, however, also the TE_1 mode that can be excited. The cutoff frequency for this mode is given by:

$$f_c = \frac{c}{4d\sqrt{\epsilon_r - 1}}$$

With the same parameters as before, $f_c = 283 \text{ GHz}$. Hence at the frequencies that this thesis examines (25.5 to 30.5 GHz), it can be concluded that, beyond the TM_0 mode, there are no higher order surface modes to be excited by microstrip discontinuities.

Theoretical Losses in Microstrip on DuPont 943:

One can calculate, based on formulas found in [19], theoretical dielectric and conductor losses for a microstrip line. For a 50Ω Ag line at 30 GHz, the physical parameters are: substrate thickness = $107 \mu\text{m}$, conductor thickness = $10 \mu\text{m}$, conductor width = $150 \mu\text{m}$, metal conductivity (σ) = $6.173 \times 10^7 \text{ S}$. From [3] the loss tangent at 30 GHz is 0.002. The formula for dielectric loss is:

$$\alpha_d = \frac{k_o \epsilon_r (\epsilon_e - 1) \tan \delta}{2 (\epsilon_r - 1) \sqrt{\epsilon_e}} \text{ Np / m}$$

where k_o is the free space wavenumber and ϵ_e is the effective dielectric constant (4.942, from [19]). This yields $\alpha_d = 1.2968 \text{ Np / m}$. Conductor loss is given by [19] as:

$$\alpha_c = \frac{R_s}{Z_o W} \text{ Np / m}$$

where R_s is the skin depth and W is the conductor width. This yields $\alpha_c = 8.185 \text{ Np/m}$ for $Z_o = 50 \Omega$. The total losses are given by the sum of the dielectric and conductor losses,

$$\alpha = 9.482 \text{ Np / m} = -82.36 \text{ dB / m} = -0.08236 \text{ dB / mm}.$$

This number will be used in comparison to the measured results.

Suitability for 3D Environments:

Microstrip, due to the exposed upper half, is suitable for use on the top of LTCC packages and for connecting to MMICs and other mounted components. It is possible to make vertical transitions from a microstrip line, but since the currents in a microstrip line are predominantly on the underside of the line and the ground plane, the transitions will likely have better performance if made downwards. Microstrip can be used as an

embedded transmission line, and this will cause the dielectric loss to increase, as more of the fields will be contained within the dielectric.

It is likely that microstrip will continue to be the transmission line of choice of most microwave designers, due to its simple geometry and well-characterized behaviour.

3.3: Stripline

Stripline is formed by sandwiching a conductor in-between two ground planes. This embeds the conductor in dielectric, creating a pure TEM mode. A picture of stripline and the fundamental mode is shown in Figure 3.2.

Figure 3.2: Stripline

Dielectric loss in stripline is higher than that of microstrip, due to the fact that all the E field lines are inside dielectric. There is one unwanted stripline mode: the parallel plate mode. If there are vias acting as shields for the stripline, these vias can form side walls and the structure can behave as a rectangular waveguide. These modes will be considered in turn.

The parallel plate mode:

Two parallel plates can support a TEM wave, and this mode has no cutoff frequency. Therefore, any stripline circuit is in danger of exciting this mode at discontinuities. There are also higher order parallel plate modes, and two of these are the TE_1 and TM_1 modes. Both of these modes have the same cutoff frequency, and it is given by [19] as:

$$f_c = \frac{1}{2 d \sqrt{\mu\epsilon}}$$

where d is the parallel plate spacing. For $d = 214 \mu\text{m}$, and $\epsilon_r = 7.1$, $f_c = 263 \text{ GHz}$, and hence these modes are not excited.

The waveguide mode:

With shielding vias, a stripline can act as a rectangular waveguide. In the structures simulated in this thesis, a shielding wall of vias was formed beside a stripline creates what appears to be a waveguide with width of 1 mm and height of $214 \mu\text{m}$. The first propagating mode in a rectangular waveguide is the TE_{10} mode, and the cutoff frequency is given by [19] as:

$$f_c = \frac{1}{2 a \sqrt{\mu\epsilon}}$$

where the width $a = 1$ mm. This yields a cutoff frequency $f_c = 56$ GHz. This is higher than the LMCS/LMDS band.

Theoretical Losses in Stripline:

The formula for losses due to the dielectric in stripline is given by [19] as:

$$\alpha_d = \frac{k \tan \delta}{2}$$

where k is the wavenumber in the dielectric. This yields $\alpha_d = 1.674$ Np /m ($\tan \delta = 0.002$). For a characteristic impedance of 30Ω , $Z_0 \sqrt{\epsilon_r} < 120$, the formula for conductor loss is given by [19] as:

$$\alpha_c = \frac{R_s \epsilon_r Z_0 A 2.7 \times 10^{-3}}{30 \pi (b - t)}$$

where R_s is the skin depth of the conductor (the metal is silver, $\sigma = 6.173 \times 10^7$ S, so $R_s = 0.04379 \Omega$ at 30 GHz), b is the ground-to-ground spacing (214 μm), and t is the conductor thickness (10 μm). The value of A is given by [19] as:

$$A = 1 + \frac{2W}{b-t} + \frac{1}{\pi} \frac{b+t}{b-t} \ln \left(\frac{2b-t}{t} \right)$$

where $W = 150 \mu\text{m}$ is the conductor width necessary to achieve a characteristic impedance of 30Ω . This formula yields $\alpha_c = 4.945 \text{ Np /m}$. When the losses due to dielectric and due to conductors are added together, and normalized with respect to wavelength, we find that:

$\alpha = 6.619 \text{ Np/m}$, or $-57.5 \text{ dB/m} = -0.0575 \text{ dB/mm}$. Again, this will be compared to the measured results.

Suitability for 3D Environments:

Stripline is ideally suited for 3D environments. With both upper and lower ground planes it has excellent isolation from other transmission lines. With the currents evenly distributed on the top and bottom of the line it is suited for making vertical transitions either up or down, and the pure TEM mode eliminates dispersion losses.

3.4: Coplanar Waveguide

Coplanar waveguide is a planar transmission line with a single conductor flanked by two ground planes. If there is a ground plane below the CPW it is referred to as conductor-backed coplanar waveguide (CPWG). Traditional CPW/CPWG has dielectric only below the conductors and air above. In a 3D environment, CPW lines can be embedded within the package. Embedding the CPW will increase the dielectric loss, but will make the transmission line more of a TEM line (as opposed to quasi-TEM), as the

fields will be completely in the dielectric rather than split. The characteristic impedance of embedded CPW/CPWG can be found using formulas found in [20] and [21]. CPW and CPWG can both suffer from the onset of the slotline mode depicted in Figure 3.4. CPWG also suffers from the parallel plate mode (like stripline) and the microstrip mode (Figures 3.5 and 3.6). LTCC-M packages are always built on a metal core, and so will always have a lower ground. LTCC packages that do not have any ground planes will not suffer losses from either the parallel plate mode or the microstrip mode.

Figure 3.3: The E field of the CPW mode

Figure 3.4: The E field of the slotline mode

The slotline mode is excited by asymmetrical discontinuities such as right-angle bends.

It is suppressed in MMICs by using bridges to connect the planar grounds. LTCC has the ability to form a type of bridge, and this will be discussed in Chapter 4.

Figure 3.5: The E field of the parallel plate mode

The parallel plate mode is suppressed by connecting the planar grounds to the lower ground plane with vias.

Figure 3.6: E field of the microstrip mode

The microstrip mode is prevented by ensuring that the distance from the centre conductor to the side grounds is less than the distance from the centre conductor to the lower ground plane.

Theoretical Losses in Coplanar Waveguide:

Conductor loss is computed using formulas derived for traditional CPWG lines, with air above the transmission line. There are many formulas included in [20], which have been included in the computer program "Linecalc". Linecalc yields conductor losses of 0.038 dB/mm. Dielectric losses can be calculated according to [20], as:

$$\alpha_d = \frac{(2.73)\epsilon_r(\epsilon_r - 1)\tan \delta}{\sqrt{\epsilon_r(\epsilon_r - 1)}\lambda_0}$$

where ϵ_{re} represents the effective dielectric constant of the coplanar line. This constant is given by Linecalc as 4.411 for a line with $\epsilon_r = 7.1$ and dielectric thickness = 214 μm . This yields 1.032 dB per metre, or 0.001032 dB / mm. Total loss is therefore $\alpha = 0.039032$ dB / mm.

Suitability for a 3D Environment:

CPW is well suited for a 3D environment, provided the conductor-ground spacing is small. This contains the E fields in the gap between conductor and ground, reducing interference between adjacent lines. If embedded CPW is used then it becomes more like a TEM line, and dispersion will decrease. CPW is also quite flexible, and good for vertical transitions, both up and down.

From the calculations made in this chapter, it is apparent that CPW has the lowest line loss of the three types of transmission line. The following is a rough comparison of transmission line losses. However, transmission line losses depend on line impedance, and the stripline in this case was computed at 30 Ω . Also, the CPW impedance could change depending on conductor configuration. This table is presented to estimate theoretical losses of transmission lines in the configuration that they are most likely to be used.

Table 3.1: Transmission Line Attenuation

Transmission Line	Attenuation
Microstrip	82.36 dB / m
Stripline	57.5 dB / m
CPW	39.032 dB / m

A package designer should be well-acquainted with these figures, as line lengths can occasionally run long, accruing large losses.

Chapter IV presents these three types of transmission lines used in package feedthrough structures.

IV: Feedthrough Simulations

4.1: The Need To Study Feedthroughs

A feedthrough is a transition that connects an exposed transmission line to an embedded transmission line. This is important to study, as, at high frequencies, feedthroughs can have a negative effect on circuit behaviour. These transitions will allow not only interaction between embedded passives and exposed circuitry, but also provide a means of connecting the LTCC package to external components, such as antennas. Also, packages with lids require feedthroughs.

4.2: Electromagnetic Simulations

To predict the performance of LTCC transitions, electromagnetic (EM) simulators were used. Simulations were mostly conducted in HP's (now Agilent) High Frequency Structure Simulator (HFSS), with some simulations also being done in Momentum, another Agilent product.

HFSS is a full-wave 3D solver that uses the finite element method (FEM) to solve Maxwell's equations and generate S-Parameters. The solver discretizes a volume and solves for the E and H fields inside a small section of that volume. The solutions from this section are forced to agree on all boundaries, yielding a continuous field solution. HFSS forces the volume under consideration to be surrounded by a box of potential zero, to give a point of reference. These simulations consumed much computational power, as well as time. Simulation time ranged from 3 to 30 hours on an Ultra 60, and used from 100 Mbytes to 2 Gbytes of memory. To speed up the simulation process, infinitely thin perfect conductors were used, dielectrics were lossless, and intermediate ground planes were treated as perfect grounds.

Momentum is a 2.5D solver that uses the method of moments (MoM) to solve Maxwell's equations. Momentum allows for multilevel circuits, but, as it forces the dielectric levels to extend to infinity in all directions, is not always applicable to LTCC transitions.

4.3: Simulations Included in This Thesis

The feedthroughs and transitions examined in this thesis were originally intended for manufacture using the DiPak process of Dielectric Laboratories (note that Dielectric Labs is an American company, and hence uses imperial measurements. 1 mil = 1 thousand of an inch). The structures were simulated with 5 mil diameter vias and no via catch-pads, from Dielectric Labs design rules (literature and website). However, consultation with Dielectric Labs revealed that these specifications could not be met, and

that their design rules were in error. As a result, the layout was modified to use 6 mil diameter vias and 10 mil square via pads, and re-simulated. After learning that the DiPak process was having difficulty ensuring that vias would connect to the CuMoCu core, the design was sent to the Technical Research Centre of Finland (VTT). VTT uses a different LTCC process (DuPont 943) with different design rules. The layout was modified and re-simulated following the new design rules.

As a result of all these different manufacturing methods, there exist three separate simulation sets: the original DiPak, the modified DiPak, and the VTT simulations. In this thesis it is often necessary to discuss some features of all these sets. Therefore, the following convention will be used: for simulations from the original DiPak simulation, the notation D1 will be used. For simulations from the second round of DiPak simulations the notation D2 will be used. Finally, simulations from the VTT round will be referred to as VTT.

Some CAD drawings of conductor structures appear as only one half of the structure. This is due to the fact that, due to the symmetry in some transitions, a magnetic wall was used. This feature reduced simulation time. Provided that the structure was symmetrical, the magnetic wall does not affect the accuracy of the simulation.

4.4: Design Rules

Both DiPak and VTT had design rules that constrained the design.

DiPak

- Fired Layer Thickness: 6.5 mils (172.5 μm).
- Minimum conductor width: 5 mils (125 μm).
- Minimum conductor to conductor spacing: 5 mils (125 μm).
- Minimum Via Diameter: 6 mils (150 μm) with via pad 2 mils on all sides for D2 and 5 mils with no pad for D1.
- Minimum Via to Via Spacing: 3X Via Diameter: 18 mils (450 μm).

VTT (DuPont 943)

- Fired Layer Thickness: ~4 mils (107 μm).
- Minimum conductor width: 6 mils (150 μm).
- Minimum conductor to conductor spacing: 6 mils (150 μm).
- Minimum Via Diameter: 6 mils with Via Pad 2 mils (50 μm) on all sides.
- Minimum Via to Via Spacing: 3X Via Diameter: 18 mils.

4.5: Entering and exiting the package

Many applications require hermetically sealed packages that can be guaranteed to form a tight seal and keep impurities (dirt, moisture) away from the package contents. Most packages containing active circuits have lids, and both the DiPak and VTT processes allow for lids.

[typical DiPak™ package structure]

Figure 4.1: Typical DiPak package structure (after [www.dipak.com]).

The addition of a lid requires a feedthrough from an external transmission line. The feedthrough characteristics must match the two lines being joined.

Figure 4.2: Two types of feedthrough.

Several papers have been published on the subject of hermetic feedthroughs [22] [23] [24]. The principle of hermetic transitions is to match the fields and impedance of the exposed line to those of the embedded line.

The transmission line to be embedded is most likely microstrip or coplanar waveguide (with or without a lower ground plane) because this geometry is most likely used to interface with other circuitry outside the package such as MMICs.

This chapter describes simulation results of three different feedthrough geometries:

- Microstrip to Stripline
- CPW to CPW
- CPW to Stripline

These feedthroughs are examined in both the Dielectric Labs and VTT processes, where appropriate.

4.5.1: Microstrip to Stripline Feedthrough

Yook [23], Rittweger [22], and Ni [24] examined microstrip to stripline transitions (see Figure 4.3) as a method to enter the package. Adding a ground plane above the microstrip line converts the microstrip into stripline. To convert back to microstrip, the upper ground plane is removed. Rittweger et al [22] claim that the transition causes unwanted spikes in return loss. This thesis claims that the ripples seen in [22] are specific to some designs, and not general to all microstrip to stripline feedthroughs. This thesis demonstrates that ripple-free feedthroughs of this type are possible, and postulates the causes of the Rittweger ripple.

Figure 4.3: Microstrip to Stripline feedthrough (after [51])

An acceptable measured return loss is taken as $S_{11} < -10$ dB, or $|S_{11}| < 0.3$. Simulations should show $S_{11} < -15$ dB, to allow for unsimulated occurrences. By this standard, the transition seen in Figure 4.3 is unacceptable.

Simulations were conducted with both the DiPak and VTT design rules, and both simulations showed that this feedthrough was operational past 30 GHz (Figure 4.5). In the DiPak case, for 50 Ω , the microstrip has a width of 10 mils, the stripline has a width of 5 mils, the layers are 6.5 mils thick, and the metal thickness is 0.5 mils, as below.

Figure 4.4: Microstrip to stripline feedthrough (D1).

Figure 4.5: S-Parameters of D1 microstrip to stripline feedthrough.

This transition was also simulated in the VTT process. In the VTT process the layers are thinner ($107\text{ }\mu\text{m}$ fired) thus making it easier to maintain the same potentials on different ground planes. However, due to these thinner layers, generating high impedance in two-level stripline (one level above the conductor, on level below, for a $214\text{ }\mu\text{m}$ ground plane spacing) is difficult. With a minimum conductor width of $150\text{ }\mu\text{m}$, the highest possible impedance is $30\text{ }\Omega$. Therefore, this feedthrough was simulated as a $30\text{ }\Omega$ microstrip to $30\text{ }\Omega$ stripline transition. Vias were used to connect the top and bottom ground planes, and these vias were located $500\text{ }\mu\text{m}$ from the centre of the conductor. The conductor was $10\text{ }\mu\text{m}$ thick, and is shown in Figure 4.6.

Figure 4.6: Microstrip to stripline feedthrough (VTT).

Figure 4.7: S-Parameters of VTT microstrip to stripline feedthrough

The results for the VTT microstrip to stripline feedthrough (Figure 4.7) show a transition that has good performance up to 30 GHz. The transition has a similar curve shape to the D1 simulation, with slightly worse millimetre-wave performance. The degradation in return loss comes from the fact that the VTT case has a greater step change in width from microstrip to stripline, creating a greater discontinuity.

There are several parameters that could be used to explain the discrepancies between the results simulated in this thesis (Figures 4.5 and 4.7) and those of Rittweger et al. (Figure 4.3). First, since the current in the microstrip line is predominantly located on the underside of the line, to make a good transition to stripline this current must redistribute itself evenly over the whole conductor surface. For this to happen, there must be a strong ground connection that can carry half the ground currents from the bottom ground plane to the top ground plane. Without these connections it is possible for parallel plate mode resonances to occur. With the ground connection being a 6 mil diameter via in VTT and 8 mil diameter in DiPak, the width of the connection is almost

as great as the height. This creates a solid ground connection, the lack of which could certainly cause the ripples seen in the results of Rittweger [51] (Figure 4.3).

Secondly, the transitions simulated in this thesis make a correction in the width of the conductor so as to maintain a constant 50Ω (or 30Ω) impedance throughout. Without such a correction, as in the Rittweger transition, reflections will occur, degrading return and insertion losses.

One final explanation for the Rittweger ripples is in the finite length of the stripline. The resonances could be caused by a half wavelength section of stripline upper ground and a resonance in the parallel plate mode of the stripline. These effects are not seen in the DiPak or VTT case because the stripline continues into the package. This transition is quite useful for LTCC packages, as microstrip is a common external line and stripline is a useful transmission line to embed.

4.5.2: CPW to CPW Feedthrough

Rittweger et al [22] also propose a strictly coplanar feedthrough. In this feedthrough, both exposed and embedded transmission lines are CPW. This design matches the EM fields of the lines, making the response less dependent of the field discontinuity and more dependent on the impedance discontinuity. It is not proposed in [22], but it is also possible to vary the width of the embedded CPW to provide a good impedance match.

This feedthrough was simulated in both D1 and VTT cases (VTT case shown in Figure 4.8). Both simulations demonstrate a wideband transition that extends into the

millimetre wave range. Even if the impedance is not compensated for [22], the transition still shows (Figure 4.9) excellent performance.

Figure 4.8: CPW to CPW feedthrough (VTT).

Figure 4.9: S-Parameters of VTT CPW to CPW feedthrough.

The CPW to CPW feedthrough curve has a similar shape to that of the microstrip to stripline feedthrough. The return loss is improved due to a better field match.

4.5.3: CPW to Stripline Feedthrough

This feedthrough uses a CPW to CPW transition to enter the ceramic, followed by a transition from embedded CPW to stripline. The transition is made by curving the two ground planes of the coplanar line away from the centre conductor, while an upper ground plane is introduced. Vias connect the coplanar grounds to the upper ground plane, and carry ground current. The transition is shown below:

Figure 4.10: CPW to stripline feedthrough (D2).

This transition takes into account the EM fields of both transmission lines. As the two planar grounds of the CPW become increasingly removed from the centre coplanar conductor, the stripline upper ground plane is introduced. This allows the transition to take place over a distance, rather than abruptly. The transition shows good results up to 40 GHz, as in Figure 4.11.

Figure 4.11: S-Parameters of D2 CPW to stripline feedthrough.

This transition allows the use of CPW as the exposed transmission medium, for flip-chip mounting, while enjoying the isolation achieved by using stripline as the embedded transmission medium.

However, this transition is difficult to make in the VTT process. The thicker layers of the DiPak process allow a coplanar line to be located only one layer above a lower ground plane, as in Figure 4.12 (because the conductor gap spacing (5 mils) is smaller than the conductor to lower ground spacing (6.5 mils)).

Figure 4.12: A CPWG line one layer above a ground plane in the DiPak process.

The dimensions in Figure 4.12 are quite similar, but simulations suggest that, even with such a small difference between grounds, the CPW will still propagate correctly.

This spacing means that the E fields will stretch from the centre conductor to the CPW planar grounds more than to the lower ground plane. In the VTT process, the situation is reversed, as below:

Figure 4.13: A CPWG line one layer above a ground plane in the VTT process.

In the VTT process, the layers are thinner than the minimum conductor-ground spacing of the CPW line. This means that, in a similar transition, the fields of the CPW line would exist also in what is referred to as the microstrip mode, where the fields of the centre conductor extend to the lower ground plane as well as the coplanar grounds. To avoid this, the CPW would have to be placed two layers above the lower ground plane, as in Figure 4.14. Note that ECPWG stands for Embded CPWG.

Figure 4.14a: DiPak Feedthrough

Figure 4.14b: Modified for VTT

The stripline conductor would then also have to be placed on the second layer. With the stripline conductor on the second layer, this can either be a part of a three layer offset stripline, with the grounds on layers three and zero and the conductor on layer two, or a four layer stripline. Both three-layer and four-layer striplines are difficult to use: a four layer stripline vertical transition would require a via at least 2 layers tall, and offset stripline is not widely used. However, there are benefits, for instance an offset stripline could realize impedances that cannot be realized in two-level stripline, and possibly implement novel coupler geometries. Despite these potential advantages, in this thesis, only two-level stripline is used.

Some vertical transitions (such as microstrip to CPW) can be considered a type of feedthrough. These vertical transitions are considered separately from planar feedthroughs, in Chapter 5.

V: Simulations of Vertical Transitions

5.1: Vertical Transitions – Direct vs. Coupled

There are two choices of vertical transitions: the first is a direct transition, and the second method is that of aperture coupled transitions. A direct connection is made through vias or vertical metal sections (examples: [25],[26]). These connections work at DC, and typically have low pass behaviour. Aperture coupled transitions (see [27]) involve vertically separated conductors and rely on radiated electric and magnetic fields to make a transition. These connections provide a DC block and exhibit a bandpass response. Generally, direct connections have a wider bandwidth than coupled transitions.

As direct connections are typically lowpass and coupled connections typically bandpass, it can be speculated that after a certain frequency point, all transitions will need to be coupled transitions. However, since the limiting factor in directly coupled transitions is the discontinuity presented by the connecting via, this discontinuity can be tuned out. Unfortunately, these tuning methods can be difficult to implement at high frequencies. By comparison, coupled transitions always require tuning and simulations to ensure that the transition is centered on the appropriate frequency. Therefore coupled transitions have a set level of difficulty in design, regardless of frequency. As

frequencies increase, the difficulties in tuning directly connected transitions will become larger than the difficulties encountered in design of aperture coupled transitions, making coupled transitions more desirable. The goal of this chapter is to determine at which frequency directly connected transitions begin to require difficult tuning methods and hence become less feasible than coupled transitions.

For LTCC packages to achieve the levels of integration required to lower costs and be usable for the LMCS/LMDS applications discussed in Chapter I, there must be a library of well-mapped, repeatable, and simple vertical transitions for a designer to use. Forcing package designers to continually resort to lengthy 3D EM simulations will not encourage acceptance of this technology. If directly connected vertical transitions can function in the microwave and lower millimetre-wave range then LTCC multilevel microwave packages can be designed more easily and cheaply.

Another justification in choosing to analyze directly connected transitions comes from problems involved with aperture-coupled transitions. By definition, coupled transitions radiate, which can cause problems with cross-talk and other interference in a multilevel environment such as LTCC. These transitions can also have difficulties with manufacturing, since they typically depend on stubs and frequency dependent lengths to set the operating frequency of the transition. If a stub changes dimensions in manufacturing, then the operating bandwidth of the transition can change.

For these reasons, only directly connected transitions are considered. The types of directly connected transitions examined in this thesis are:

- Stripline to stripline vertical transition.
- Coplanar waveguide to stripline transition.
- Coplanar waveguide to coplanar waveguide transition.
- Microstrip to coplanar waveguide transition.

5.2: Stripline to Stripline Vertical Transition

As mentioned in section 3.3, stripline is a very useful transmission line for LTCC packages, and there have been all-stripline packages [16-18]. To best enhance the multilayer features of LTCC, a stripline to stripline transition is necessary. The transition studied involves two separate three-layer striplines with a common ground. The lower stripline has the CuMoCu core (if LTCC-M) or another ground plane (if LTCC) as its bottom ground plane and has its top ground plane on layer two, with the centre conductor sandwiched between them on layer 1. The upper stripline has its ground planes on layers two and four, with the centre conductor on layer three. Therefore, the connection will be a via that spans two layers, connecting the conductor on layer 1 to that on layer 3. This via will pass through a hole in the ground plane located on layer 2. The transition is shown in Figures 5.1 and 5.2.

Figure 5.1: Side view of generic stripline to stripline vertical transition.

Figure 5.2: 3D view of generic stripline to stripline transition.

Typically, two layer transitions are made, as this keeps the connecting via (the source of the discontinuity) as small as possible. However, if offset stripline is desired, or if the package design calls for longer transitions, these can be made by simply stacking more vias. However, increasing the length of the via increases the discontinuity of the junction.

This transition has been demonstrated in the literature, by Gipprich et al [18], with an all-stripline LTCC package that functioned at frequencies up to 14 GHz, depicted below:

Figure 5.3: Stripline to stripline transition (after [18])

The Gipprich transition involves two interesting features: a brief tuning section demonstrated by the narrowing of the stripline and a wall of vias to provide grounding. The large numbers of vias indicate the necessity of maintaining proper ground potentials in an LTCC package. The tuning method will be discussed further as the properties of the transition are discussed. The transition shown in Figure 5.3 indicates the feasibility of this transition, and this thesis will extend the operating frequency.

5.2.1: General Effects of the Connecting Via and Via Pad

Interestingly, the transition depends most on the size and dimensions of the via pad, rather than the properties of the via itself. Traditionally, vias are modeled as inductances, but in this case the shunt capacitance of the via pad dominates the transition behaviour. In both the VTT and DiPak processes, a via catch-pad is required and must be 2 mils (50 μm) larger than the via on all sides. Therefore, for a 6 mil diameter via, the pad must be a circle of diameter 10 mils, or a square 10 mils on a side. This pad is often quite large with respect to the line that it connects to: e.g. in the DiPak process a 50 Ω stripline with a ground plane spacing of 13 mils has a width of 5 mils, meaning that the line must double in width at the via pad. This change in width will add to the parasitics of the transition. The tuning method of the Gippich transition is the introduction of a short section of high impedance stripline, used to counteract the capacitive behaviour of the transition.

In order to determine the effects of different via diameters and via pad sizes, several simulations were performed in following the DiPak design rules. A stripline to stripline transition was designed, and the connection was made with:

- a) A 5 mil diameter via with no via pad;
- b) A 5 mil diameter via with a 10 mil square via pad;
- c) A 6 mil diameter via with a 10 mil square via pad;
- d) An 8 mil diameter via with a 12 mil square via pad.

Each of these cases was simulated in HFSS, and S-Parameters were calculated.

The curves for return loss are shown below:

Figure 5.4: Return loss curves for different via and pad sizes in a DiPak stripline to stripline vertical transition.

The curves for return loss indicate a correlation between via pad size and transition performance. The first case, with no via pad, has an S11 of -25 dB at 30 GHz. The introduction of a 10 mil square via pad reduces this to an S11 of -18 dB at 30 GHz. The change in via size (i.e. from case b) to c)) affects the return loss only marginally, as the difference between the 5 mil diameter and the 6 mil diameter vias with the same pad size is only approximately 2 or 3 dB at 30 GHz. Worst is case d), the 8 mil diameter via with the 12 mil via pad (12 mils = 8 mil via plus 2 mils on either side). This transition has an S11 of -11 dB at 30 GHz. This makes a change of 14 dB between the best (a) and worst (d) cases. The first case provides a baseline for comparison, but is not realistic as via pads are required in all current LTCC processes. However, comparing cases c) and d)

allows the comparison between a 6 mil process and an 8 mil process. The difference is 5 dB. If a 5 mil via process were available, then the pads would be 9 mil square (or diameter) which would result in additional improvement, most likely 4 or 5 dB better than a 6 mil via process.

These simulations allow two different parameters to be compared. Examining a) and b) allows for the determination of the effect of a via pad. Comparing b) and c) exposes the effect of the via diameter. Case d) demonstrates how both of these trends, taken to a larger degree, degrades performance.

5.2.2: The Capacitive Effect of the Via Pad

Examining cases a) and b) we see that the via pad has an enormous effect on the transition response. Both cases tend to work up to approximately 30 GHz, and both cases have the same effects after 30 GHz. However, before 30 GHz, the differences are dramatic. An increase in shunt capacitance due to the increase in via pad area causes this degradation in performance. The S_{11} of both cases has been plotted on a Smith chart, and is labeled Figure 5.5.

Figure 5.5: Smith chart comparison of S_{11} for DiPak stripline to stripline vertical transitions, to determine the effect of the via pad (comparing cases a) and b)). Reference planes were located $1000\ \mu\text{m}$ away from the transition on both ports.

The curves demonstrate an increase in capacitance associated with increased via pad size. It can be noted that both curves have a similar spiral pattern, but in the case of the transition with no via pad the spiral is held tightly to the centre of the chart. In the case with the 10 mil square pad (case b)) the spiral is now rotating further from the $50\ \Omega$ point, pushed towards low impedance by this increase in shunt capacitance. An interesting phenomenon, that the responses are initially capacitive, is observed here. This is intriguing because most via analysis assumes that the inductive nature of the via dominates. This response, although not standard, is in no way unbelievable. This transition has many areas of shunt capacitance, such as:

- from below the via pads to (any) ground;
- the open end effect of the striplines;
- the capacitance between the connecting via and the hole in the ground plane.

Since the transition behaviour is initially capacitive, it stands to reason that an increase in shunt capacitance would do little to improve performance, and would in fact degrade the transition behaviour. This is the reaction that one sees in Figure 5.5.

5.2.3: The Effect of the Via Diameter

By comparing cases b) and c) (case b) has 5 mil diameter via with 10 mil via pad; case c) has 6 mil diameter via with 10 mil via pad) the effect of a small change of the via diameter can be claimed to be quite small. In both the return loss (Figure 5.4) and the Smith chart (Figure 5.6) curves, we see little to indicate that a change from 6 mil diameter vias to 5 mil diameter vias will result in any great improvement (provided the vias pad size remains constant).

Figure 5.6: Smith chart comparison of S_{11} for DiPak stripline to stripline vertical transitions, to determine the effect of the via diameter (comparing cases a) and b)). Reference planes were located $1000\ \mu\text{m}$ away from the transition on both ports.

Some improvement is seen with the thinner via, but this improvement is small; on the order of two or three dBs. However, any LTCC design should use the smallest vias possible. The most important reason to switch from 6 mil vias to 5 mil vias is that the via pads will be smaller. Typical design rules state that there must be 2 mils clearance from the edge of the via to the edge of the pad. This means that a 6 mil diameter via will have a 10 mil square pad, while a 5 mil diameter via will have only a 9 mil square pad. This is a 19% reduction in area, and would improve the performance of the transition.

5.2.4: The Effects of Varying the Hole in the Ground Plane

Another factor that effects the transition is the radius of the hole in the ground plane through which the connecting via passes. This hole must be a certain size in order to not interfere with the EM fields as they pass through the hole. Consider the following two sets of results (Figures 5.7 and 5.8) – the first represents the transition with a ground plane hole of 10 mil diameter, the second with a 15 mil diameter.

Figure 5.7: Return loss comparison of two DiPak stripline to stripline vertical transitions with identical vias and via pads, to determine the effect of the hole in the ground plane.

Figure 5.8: Smith chart comparison of two DiPak stripline to stripline vertical transitions with identical vias and via pads, to determine the effect of the hole in the ground plane. Reference planes were located 1000 μm away from the transition on both ports.

These results demonstrate that the size of the hole in the ground plane plays a significant role in this transition. If the hole is too small, then the fields are interfered with as they make a vertical transition. Conversely, if the hole is too large, this will affect the striplines as they approach the via; the E fields of the stripline will no longer stretch from the centre conductor to the upper ground plane, as there will be no upper ground plane. This will cause most of the fields to point to the lower ground, making the stripline behave like a microstrip line and causing difficulties in making the vertical transition. The difficulties come from the fact that the transition is made by allowing currents to flow up the via. If the line that approaches the via is a microstrip line, then most of the current is located on the bottom of the line, furthest from the via. The

transition is best served by having currents on the top of the line which can easily flow onto (and up) the via.

Figure 5.9: Representation of electric fields in a generic stripline to stripline vertical transition.

Figure 5.9 depicts a side view of the stripline to stripline vertical transition, clearly showing the hole in the level-2 ground plane. The E fields of the stripline on both sides of the transition are depicted with arrows.

Figure 5.10: Representation of electric fields in a generic stripline to stripline vertical transition with a large ground plane hole.

Figure 5.10 depicts the changes in the fields of the striplines if the radius of the hole in ground plane number two is increased. The striplines will start to behave more like microstrip lines and this will force the E fields away from the via, and degrade the transition performance. Therefore the ideal hole in the ground plane will be large enough to allow the fields to pass through unimpeded, but avoid affecting the striplines on either side of the via.

5.2.5: Parallel Plate Modes Launched By This Transition

A parallel plate mode can be excited by line discontinuities. In this transition, this mode is excited by unequal charge distributions created by the vertical via [28], and can propagate in many different directions away from the via, as shown in Figure 5.11.

Figure 5.11: Representation of parallel plate modes that can propagate near a generic stripline to stripline vertical transition.

Unwanted power can be reflected back as parallel plate modes from either port, as well as being lost in between the area under the level 2 ground on the bottom right section of the figure. Power can also be lost in lateral parallel plate modes. These modes are prevented by connecting the two plates in some way such that they are forced to maintain the same potential. In LTCC, vias make this connection. The two plates are connected by a via two layers tall (13 mils in Dipak, 8.5 mils in VTT). However, as frequency increases, the inductance of the grounding vias increases, and their ability to keep the two ground planes at the same potential decreases.

5.2.6: Grounding the Stripline to Stripline Transition

The top and bottom ground planes of the stripline must be connected together with vias in order to ensure that the proper mode is launched on the stripline. The vias need to be a certain distance away from the stripline conductor (4 times the ground plane separation) in order to avoid interfering with the fundamental TEM mode of the line [29][30]. It is also noted that the line performs better when the vias are regularly spaced along the line, rather than placed only in potentially troublesome locations [29].

The area under the level 3 stripline must also be well grounded. Vias must connect level 2 to the metal core of the package. In this section, the vias can be placed at the designer's discretion, and can be arranged to form a "fence". For instance, three vias can be placed in a row, to block EM transmission, as depicted in Figure 5.12.

Figure 5.12: A via fence used to connect two ground planes.

An improvement on this fence is a structure that uses the intermediate layer between the top ground and the core to connect the three vias together. This grounding structure is referred to as a via fence with pseudo air-bridge (PAB). The structure was named for its similarity to air-bridges used in MMICs. This structure aims to decrease the inductance of the ground connection by using three vias in parallel. Ponchak et al demonstrate the use of via connecting lines (like the PAB) to improve microstrip lines (see [29]).

This fence with PAB was found to have mixed results, depending on the simulation set. In the D1 simulations, the addition of a via fence with PAB over the use of two-level grounding vias caused a large improvement in performance, shown in Figure 5.13. A 3D view of the transition is shown in Figure 5.14.

Figure 5.13: D1 return loss comparison of stripline to stripline vertical transitions with via fence and PAB.

Figure 5.14: 3D view of D1 stripline to stripline vertical transition showing PABs.

However, in the D2 set (3D view shown in Figure 5.15, S-Parameters shown in Figure 5.16) of simulations it was found that the addition of the PAB no longer caused such a large improvement.

Figure 5.15: 3D view of D2 stripline to stripline vertical transition showing use of PAB.

Figure 5.16: D2 return loss comparison of stripline to stripline vertical transitions with via fence and PAB.

The reason for this lack of improvement is the following: in the D1 case, the transition performed well into the millimetre-wave range, and the improvements were realized at 45 GHz, where a resonance was eliminated. In the D2 case, the addition of the large via pad has already deteriorated the results to have an upper frequency limit of just

above 30 GHz, and so any improvements from the PAB were cancelled out by the deterioration caused by the large via pad. These suggest that as LTCC manufacturing improves and via diameters and pads get smaller, the PAB can play a prominent role in extending the bandwidth of vertical transitions. Although Figure 5.15 only shows 1 PAB, simulations demonstrated a similar lack of improvement with two PABs, as in Figure 5.14.

The via fence with PAB was not simulated in the VTT stripline to stripline transition.

5.3: Stripline to Coplanar Waveguide Vertical Transition

This transition is useful for package designers who wish to use more than one type of transmission line in an LTCC package. The different transmission line sections can be used for different circuit functions.

The transition is formed by connecting a stripline conductor to the centre conductor of a CPW line through a vertical via. The CPW ground planes are formed from the top ground plane of the stripline. The connecting via is one layer in height. A generic transition is depicted in Figure 5.17.

Figure 5.17: Simplified 3D diagram of a generic stripline to CPW vertical transition.

This transition was simulated in all of the simulation sets, D1, D2, and VTT. In the D1 case, the stripline width was 5 mils, and met a 5 mil diameter vertical via with no via pad. The via connected to the end of the CPW centre conductor, which had a width of 7.5 mils. The via height was 6.5 mils, and the CPW ground plane spacing was 5 mils.

In the D2 case, the dimensions of all the lines were almost the same, except for the addition of a 10 mil square via pad on both the stripline and CPW. Also, the via diameter was changed to 6 mils from 5, as in Figure 5.18.

Figure 5.18: 3D view of a D2 stripline to CPW vertical transition.

In the VTT case, the transition was changed somewhat. Due to the increased dielectric constant and thinner layers of the DuPont 943, the line widths had to be increased. Due to the $30\ \Omega$ restriction on the stripline impedance, the CPW line was also made $30\ \Omega$. The minimum spacing was larger in the VTT process necessitating the use of 6 mil ($150\ \mu\text{m}$) CPW ground plane gaps. Also in the VTT process, a circular via pad was used instead of a square one, and the curve of the ground plane has changed from a square to a triangle, to try and make a smoother transition. The transition is shown in Figure 5.19.

Figure 5.19: 3D view of VTT stripline to CPW vertical transition.

5.3.1: Transition Properties

There are several key features that are responsible for the behaviour of this transition. The first of these is the connecting via and via pad, whose importance was emphasized in the stripline to stripline transition. The second is the capacitance of the CPW open circuit. The third is the geometry of the CPW line. Typically in microwave applications the lower ground plane is not so close to the CPW line. The distance from the CPW centre conductor to the coplanar grounds is slightly greater than the distance from the centre conductor to the lower ground plane. This will make the microstrip mode of CPW much easier to launch, and will likely add to losses in this transition. The fourth key feature is not so easily quantifiable. The goal of this transition is to allow a smooth transition from the fields of stripline to a CPW configuration, so that propagation is not

unduly affected. However, it is difficult to force the E fields that stretch from the bottom of the stripline to the lower ground plane to follow the currents up the via into the CPW line. This reticence has a significant effect.

5.3.2: Effect of the via diameter and via pad size

By comparing the results of the D1 and D2 simulations, the effect of moving from a 5 mil via with no pad to a 6 mil via with a 10 mil square via pad can be observed. As the following results demonstrate, the effects are dramatic. As in the stripline to stripline transition, the introduction of the larger via and large via pad causes a significant degradation in performance, as shown below:

Figure 5.20: Comparison of return loss for D1 & D2 simulation results for the stripline to coplanar waveguide vertical transition.

This is similar to the effects seen in the stripline to stripline transition, and the reasons for the degradation also similar. Again, this transition is dominated by shunt capacitances, from the stripline open-end effect to the CPW open circuit, so the addition of more shunt capacitance in the form of a larger via pad degrades the transition performance.

5.3.3: Effect of the CPW open circuit

Unlike the stripline open circuit, the CPW open provides a tuning opportunity, as the distance from the CPW centre conductor to the CPW ground plane is a variable controlled by the package designer. Simulations conducted in Momentum (and plotted as Figure 5.21) demonstrate the effect (on the D1 case) of varying this dimension (the CPW open was square in these simulations).

Figure 5.21: Simulations demonstrating return loss variation in a stripline to CPW vertical transition with CPW gap size.

5.3.4: Variations with the DiPak and VTT simulations

Figure 5.22: Return loss of VTT stripline to CPW vertical transition.

Both the D1 and D2 simulations for this transition show similar behaviour, although with some performance loss caused by the large via and via pad in the D2 case. In the VTT case, the transition shows excellent performance (Figure 5.22 shows $S_{11} < -15$ up to 40 GHz), which is better than both the DiPak versions. This improvement can be attributed to the thinner layers, making the connecting via shorter.

5.3.5: Grounding Schemes

As in the stripline to stripline transition, different grounding schemes were examined in order to minimize the parallel plate noise introduced by the via discontinuity. A pseudo air-bridge (PAB) was used in an effort to keep the two CPW ground planes at the same potential as the lower ground plane. Initially, this grounding was done with two vias, one from each CPW ground down two layers to the bottom ground. With the PAB, these two vias are connected with a conducting strip on the layer below the CPW (Figure 5.23). This allows the connection of this conducting strip to the bottom ground plane to be done with three vias in parallel, reducing the inductance of the ground connection.

Figure 5.23: A CPWG line with a pseudo air-bridge (PAB).

This grounding structure was used in all three simulation sets with mixed results. The D1 case was the first to demonstrate the promise of such a structure, demonstrating results that increased the bandwidth of the transition and improved the return loss and insertion loss of the transition. The addition demonstrated an improvement (shown in Figure 5.24) that worked in the high frequency regions (30 GHz +).

Figure 5.24: D1 Insertion Loss improvement resulting from PAB usage.

When the structure was used in the D2 case these improvements disappeared. This seems akin to the problem that faced the stripline to stripline transition: the benefits of the lowered inductance were erased by the loss in performance caused by the large vias and via pads. As a result, the transition showed no difference in results for both with and without the PAB, as below:

Figure 5.25: The addition of a PAB to the D2 simulation has little effect.

When the structure was used with the VTT case, the transition behaviour deteriorated. This is a result of the VTT design rules. In the DiPak case, the CPW line could propagate the correct CPW mode despite the use of the PAB, as the CPW conductor-ground spacing is 5 mils and the PAB is located 6.5 mils below. Therefore, the CPW centre conductor is still closer to the appropriate grounds than to the bridge. In the VTT case, the CPW conductor-ground spacing is 6 mils, and the bridge is located on

the layer below which is approximately 4.25 mils away. Therefore the CPW line suffers a major discontinuity every time a PABs is used. The PABs could be used in a CPW line where there were three layers between the CPW and the lower ground plane, with the bridge two layers under the CPW. However, as was seen with the D2 simulations, the PABs would not likely have any effects due to the detrimental effects of the large vias and via pads required in the VTT process.

5.3.6: Tuning the transition

In the D2 case, the transition had a return loss less than -10 dB up to 30 GHz. This behaviour would normally be acceptable, but since this is a simulated result, a better transition response was desired to allow for the degradation of performance caused by non-simulated effects such as rough metals, posting, etc. It was also desired to see if the transition could be tuned to provide optimum behaviour in a certain band. Therefore, the transition was de-embedded, and plotted on the Smith chart, as below:

Figure 5.26: S11 of the D2 stripline to CPW vertical transition.

The Smith chart shows that the S11 curve crosses the real axis at 30 GHz. Therefore simple tuning methods can be used to improve the performance at 30 GHz. The impedance at 30 GHz was 25Ω. A quarter-wave transformer was used (40 mils in length, impedance of 35Ω), and placed directly before the transition (originally published in [31]). A 3D view is depicted in Figure 5.27.

Figure 5.27: 3D view of quarter-wave transformer added to the D2 simulation of a stripline to CPW vertical transition.

Figure 5.28: Return loss of D2 stripline to CPW vertical transition using a quarter-wave tuning section.

Figure 5.28 shows that this impedance transformation resulted in an improvement in return loss at 30 GHz. The bandwidth of a quarter-wave transformer is not large, but at 30 GHz, it was large enough to stretch across the whole LMCS/LMDS band with a return loss of less than -15 dB.

Another tuning method was also briefly examined. This method involves the addition of inductance to cancel the shunt capacitance that dominates the transition behaviour. Inductance was added with the use of a short circuit. The CPW line was shorted just after the transition. This tuning effort was made in the D2 process, and is shown below:

Figure 5.29: 3D view of shorted CPW to stripline vertical transition (D2).

This short provides two benefits to the transition. First, the inductance cancels some capacitance. Second, a CPW short has less radiation than a CPW open. The results (Figure 5.30) were encouraging:

Figure 5.30: Return loss of D2 shorted CPW to stripline vertical transition.

These results show how the transition now behaves like a high pass filter, with the pass band starting at 40 GHz. This was somewhat out of the range of the LMCS/LMDS band but, by varying the distance to the CPW short, the transition could be tuned to operate in the 30 GHz region. There is an effect that creates a ripple at 32 GHz that should be investigated.

5.4: CPW to CPW Vertical Transition

Another vertical transition examined in this thesis is the CPW to CPW transition. Connecting two CPW lines with vias forms this transition. The vias are one layer tall, and connect both the centre conductors and the coplanar grounds. A generic transition is given by Figure 5.31.

Figure 5.31: 3D View of a generic CPW to CPW vertical transition.

Ideally, the vertical vias would have the same widths and spacings as the initial lines, making the transition act like a right angle bend, but LTCC design rules make this impossible. Both the DiPak and VTT design rules state that vias must be separated by 3X the via diameter, and this spacing is too large to match the CPW spacing. Consider a D2 CPW line with a 7.5 mil centre conductor and 5 mil ground spacing. The via diameter is 6 mils. If the centre conductor stretches from $x = -3.75$ to $x = 3.75$, then the coplanar ground planes start at $x = -8.75$ and $x = 8.75$. The via connecting the centre conductors would be at $x = 0$, meaning that the two side vias would be placed at $x = -18$ and $x = 18$, far from their ideal location. Therefore, the vias are simply placed as close together as possible.

This transition has been simulated in the VTT simulation set, where it demonstrated excellent results into the millimetre-wave range. In the simulation a CPW line on layer three connected to a CPW line on layer two. A 3D view and the results of the VTT simulation are shown below:

Figure 5.32: 3D View of the VTT CPW to CPW vertical transition.

Figure 5.33: S-Parameter results of the VTT CPW to CPW vertical transition.

The transition features some overlap between the two lines: the length of the via pads. This means that the lines overlap by 10 mils (250 μm). It would be possible to try and tune this transition by varying this overlap, but this could increase open-end radiation. Ideally, the transition would appear as a right angle bend to the incoming line.

The VTT simulation has the following dimensions: the fired layer thickness is 4.25 mils, the conductor-ground gap is 6 mils, and the centre conductor width is 6 mils for the level two line and 12 mils for the level three line. These dimensions were found from the Linecalc program and verified to be 50 Ω with HFSS.

Unwanted parallel plate modes can be excited by this transition. Since there is a lower ground plane in the VTT layout, parallel plate modes can propagate between either CPW line and the lower ground. For this reason, the coplanar grounds of the CPW line are connected to this bottom ground plane with vias. The vias are spaced 500 μm away from the middle of the centre conductor.

If the S_{11} of the VTT result is plotted on the Smith chart, as in Figure 5.34, one can see that the behaviour of this transition is predominantly capacitive. This is a good result, as it agrees with the findings of a previous investigation into CPW-CPW transitions for flip-chip circuit transitions [32]. In fact, the curve seems to follow the spiral pattern of the transitions previously analyzed.

Figure 5.34: S_{11} Smith chart plot of VTT CPW to CPW vertical transition.

There are several reasons for this capacitive behaviour. First, the transition has two CPW open circuits. Second, the CPW line on level three is exposed to the air, and hence has an epsilon effective of less than 7.1. As the line turns vertical the conductors

are now completely embedded in the ceramic, giving an epsilon effective of exactly 7.1. This increase in effective dielectric constant lowers the impedance of the transition.

Simulations were performed to see the benefits of the pseudo air-bridge (PAB) on the CPW-CPW transition behaviour. Unfortunately, as the PAB could only be placed one level below the CPW lines, as mentioned in section 5.35, this caused a degradation in return loss.

5.5: Coplanar Waveguide to Microstrip Vertical Transition.

The stripline to stripline vertical transition is used to connect one embedded line to another. There is a need for transitions that connect embedded lines (such as stripline, ECPW) to exposed lines (such as microstrip and CPW). These transitions connect embedded circuitry to devices mounted on the top of the package. The CPW to CPW vertical transition could be used in this manner, as well as the stripline to CPW vertical transition. However, these result in an exposed CPW line. Since these exposed lines will be used to connect to active devices and to other components, it is important to note that while the popularity of CPW is growing, many active circuits are designed to be accessed with microstrip lines. Therefore it is necessary to have a transition that connects an embedded line to an exposed microstrip.

This transition has been in existence for many years, with reference to it being found in Houdart's 1979 paper "Various Excitations of Coplanar waveguide" [33]. The transition is made by forming a CPW line out of the ground plane of a microstrip line, as in Figure 5.35.

Figure 5.35: A generic CPW to microstrip vertical transition.

This transition allows for an easy transmission of ground currents, and can be expected to have excellent performance. The microstrip ground currents flow seamlessly into the CPW grounds. This transition behaves as a low-pass filter, created from the inductance of the connecting via and the CPW open circuit.

This transition was simulated in HFSS following the VTT design rules. The design had the following dimensions: microstrip width: 150 μm . Layer thickness: 107 μm . CPW spacing: 150-150-150, with a lower ground plane 214 μm below, connected to the coplanar grounds with vias. The via that connects the microstrip to the CPW is 150 μm in diameter and 107 μm (one layer) long. A 3D view and the results of the VTT simulation are shown below:

Figure 5.36: 3D view of a microstrip to CPW vertical transition (VTT).

Figure 5.37: S Parameter results of VTT CPW to microstrip vertical transition.

The excellent simulation results of Figure 5.37 show a return loss that remains below -20 dB from DC to 40 GHz. This high frequency performance is to be expected due to the fact that ground currents are relatively unaffected in this transition, unlike other vertical transitions which required ground currents to take via paths. The Smith chart (Figure 5.38) demonstrates a familiar response:

Figure 5.38: S11 representation of microstrip to CPW vertical transition.

The initial capacitance is due to the capacitance of the CPW and microstrip open circuits. The revolution about the Smith chart is due to the inductance of the connecting via as well increasing frequency. The curve has the appearance of an ideal low-impedance (lower than $50\ \Omega$) transmission line, with small variations due to the reactances of the via and CPW open circuit. However, the similarities in this response to that of an ideal transmission line suggest the excellent performance of this transition.

The response demonstrates real impedances at three distinct frequencies. At DC, the transition is exactly $50\ \Omega$. At 12 GHz, the transition appears as $42\ \Omega$. Finally, at 25 GHz the transition looks like $53\ \Omega$. These occurrences of real impedances allow for the use of quarter wave tuning as used in the stripline to CPW vertical transition. However, as the return loss remains below $-20\ \text{dB}$ from DC to 40 GHz, tuning is unnecessary for general applications.

5.6: Other Vertical Transitions

This chapter presented four directly connected vertical transitions and discussed their performance with regards to using them in LTCC packaging. Certainly, there are many more possible transitions that can be used for this purpose. The transitions examined herein, however, have one great asset: simplicity. For high integration in LTCC packages to become a reality, the transitions must easily interface with both passive components (which would become embedded) and active circuits (the chips mounted on the package). One broad class of transitions that deserves attention is the coupled transition, which can be used into the millimetre-wave range.

The transitions demonstrated a variety of effects that influenced their S-Parameters. To determine the source of these effects, the transition are modeled with circuit elements, and this is shown in Chapter Six.

VI: Transition Modeling

6.1: Stripline to Stripline Vertical Transition

The stripline to stripline vertical transition has many effects, from via inductances to open circuit capacitances. The return loss of this transition has been plotted in Figure 6.1. At low frequencies, the input impedance demonstrates capacitive behaviour, which develops into a spiral pattern similar to a lossy low impedance transmission line. The S_{11} curve begins at the centre of the Smith chart, and moves as a shunt capacitance as frequency increases (A). The impedance then begins to curve towards the real axis, appearing somewhat as a series inductor (B). Once the impedance is well into the inductive area of the Smith chart, the curve turns downward towards the real axis, and crosses at an impedance slightly greater than 50 ohms (C). At this point, the curve resembles most a low-impedance transmission line with characteristic impedance equal to the point where S_{11} first crosses the real axis. The curve, after crossing the real axis for the second time, again begins curling as if a shunt capacitance existed (D). After point D, the curve becomes difficult to model.

Figure 6.1: S11 Smith chart plot of D2 stripline to stripline vertical transition.

Based on this plot, a circuit model for the transition can be created. The transition is modeled by two series inductances and two shunt capacitances. This is an unsymmetrical model for a symmetric structure, meaning that the elements in the transition model do not correspond directly to structural elements. The model is shown below:

Figure 6.2: Circuit model of stripline to stripline transition

One of the assumptions made in this model is that all the ground planes are at the same potential. Since the top stripline ground planes are connected to the lower ground plane with vias, a more realistic assumption is that the ground planes for the top stripline have an inductive ground connection. Another simplification is in the modeling of the shunt capacitances. In reality, the shunt capacitance is split, half to the top ground and half to the bottom ground. This top shunt capacitance then has a connection to ground that includes distance traveled across the ground plan to a grounding via, and then down the inductive via.

This complicated transmission line transition requires many simplifications. With so many simplifications, the models will lack accuracy. However, this model is not being made to speed circuit development, since S-parameter blocks from 3D EM simulators can be used in circuit simulators to represent the transition. What this model provides is a means of determining in advance the effects of varying some of the major structural parameters. Since building a model is an attempt to match a curve with a fixed number of variables, it would always be possible to find a set of component values to represent any curve, provided there were enough variables. Therefore the simplest model possible was created, in order to limit this effect, and to obtain element values that somewhat represent effects that are seen in reality. If the model element values are related to the values that exist in reality then the model can be used with more confidence to predict structures not yet built.

To test the model, it was applied to the four cases of via and pad structural changes described in Section 5.2.1. The model includes the vertical transition and also 1 mm of transmission line on both ports. The results are:

Model a): stripline to stripline transition using a 5 mil connecting via with no via pad.

$L1 = 70 \text{ pH}$

$C1 = 115 \text{ fF}$

$L2 = 290 \text{ pH}$

$C2 = 90 \text{ fF}$

Figure 6.3: Comparison of simulated and modeled return loss for case a)

Model b): stripline to stripline transition using a 5 mil connecting via with 10 mil square via pad.

$L1 = 125 \text{ pH}$

$C1 = 160 \text{ fF}$

$L2 = 275 \text{ pH}$

$C2 = 125 \text{ fF}$

Figure 6.4: Comparison of simulated and modeled return loss for case b)

Figure 6.5: Comparison of simulation and model of S11 for case b)

Model c): stripline to stripline transition using a 6 mil connecting via with a 10 mil square via pad.

$L1 = 110 \text{ pH}$

$C1 = 145 \text{ fF}$

$L2 = 250 \text{ pH}$

$C2 = 115 \text{ fF}$

Figure 6.6: Comparison of simulated and modeled return loss (case c))

Figure 6.7: Comparison of simulated and modeled S11 (case c))

Model d): stripline to stripline transition using an 8 mil connecting via with a 12 mil square via pad.

L1 = 210 pH

C1 = 250 fF

L2 = 550 pH

C2 = 260 fF

Figure 6.8: Comparison of simulated and modeled return loss (case d))

Figure 6.9: Comparison of simulated and modeled S11 (case d))

In the first case (case a), Figure 6.3), the model does not predict the early resonance. This was a difficult case to model exactly, as the S11 curve held tightly to the centre of the Smith chart. It seems that the very ideality of the transition behaviour made low-frequency modeling difficult. The circuit model takes into account non-ideal circumstances, such as via pad capacitances, and the lack of these effects (due to the lack of via pads) in the first case makes the low-frequencies difficult to model. However, the model was able to track the transition behaviour well into the high frequency regions. This good high frequency agreement is likely due to the fact that, as this is an ideal case, the high-frequency non-modeled effects were less prominent. It will be shown in the following paragraphs how the non-ideality of other cases allows the modeling of low frequency operation and prohibits the modeling of the high (30 GHz +) frequency areas.

However, as both the model and HFSS simulation yield return losses less than -20 dB, the responses are not that dissimilar.

In the second case (case b), Figures 6.4 and 6.5), the model was not able to follow the small dimple in the Smith chart curve that causes the model to cross the real axis at a lower impedance than the simulated curve. Also, the behaviour for this transition showed a resonance, creating a small loop, near the centre of Figure 6.5. This loop is responsible for the two downward spikes on the S_{11} curve, just after 30 GHz (Figure 6.4). Without any parallel resonators in the circuit model, the transition behaviour could therefore only track the curve up to approximately 31 GHz.

In the third case (case c), Figures 6.6 and 6.7), the model was able to make a more accurate representation of the transition behaviour. Some small discrepancies in the curve make the modeled curve cross the real axis for the first time at a lower impedance than the simulated value (Figure 6.7). Also, this curve, like both before it, has a curling resonance that is not taken into account by the model. It is for this reason that the model is good up to only 31 GHz.

In the last case, case d): the case of the 8 mil diameter via and 12 mil square via pad, modeling was less useful. In this case the non-modeled effects of the transition dominate, making the existing model unsuitable. The transition was modeled up to 17 GHz, but at higher frequencies the circuit model was unable to track the graph (see Figures 6.8 and 6.9). Due to the unreliability of the model in this case, however, it is unlikely that the circuit values below 17 GHz are correct, as they seem unreasonable when compared to the preceeding cases. It is possible that these values are correct and

that they are large because they are including effects that are prominent in this transition and not prominent in the preceding transitions.

6.1.1: Comparison

To attempt to determine the veracity of the model, the modeled results can be compared to see if the model's behaviour corresponds to the structural changes that were made in the simulations.

If we compare the results of simulations a) and b) we see that as a via pad is added the following changes occur:

L1 changes from 70 pH to 125 pH.

C1 changes from 115 fF to 160 fF.

L2 changes from 290 pH to 275 pH.

C2 changes from 90 fF to 125 fF.

The effect that was expected with the addition of a via pad was an increase in shunt capacitance. This is seen with both C1 and C2 increasing. However, there are also some inductances that change. L1 increases in value while there is a reduction in L2. The most plausible explanation is that although L1 and L2 seem to represent the via inductance, they also include other effects that are being seen here. One consolation is that the change is quite small.

If the increase in via diameter is examined (simulations b) and c)), the following changes are observed:

L1 changes from 125 pH to 110 pH.

C1 changes from 160 fF to 145 fF.

L2 changes from 275 pH to 250 pH.

C2 changes from 125 fF to 115 fF.

The increase in via diameter does not cause serious effects because, due to the skin effect, the current carrying area is much the same. However, generally a via diameter increase is regarded as a decrease in inductance. A decrease in shunt capacitance is also observed. This decrease can be explained through the reduction of the open-end effect. In the first case, the via is 3 mils away from the pad edge on all sides. In the second simulation the via is only 2 mils away from the pad edge. The values do not change drastically because the open-end effect change is small.

The results from d) seem to be complicated by non-modeled effects that lead to parameter values not in the range of the other cases. This indicates the limits of the simple model to handle drastic parameter changes. However, with most of the simulations, the model does an adequate job of modeling structural changes in the stripline to stripline vertical transition.

6.2: CPW to Stripline Vertical Transition Model

The ladder network of two inductors and two capacitors used for the stripline to stripline transition model is also appropriate to use for the CPW to stripline model.

Consider the graph of S_{11} from the VTT simulation set shown below:

Figure 6.10: S_{11} of VTT CPW to stripline transition (normalized to $30\ \Omega$)

The graph shows the same spiral pattern seen in the stripline to stripline transition. This is because many of the effects are the same:

- The vertical via series inductance
- The stripline open end shunt capacitance
- The CPW open shunt capacitance

Therefore the same network is used, that of Figure 6.11.

Figure 6.11: Circuit model of stripline to CPW vertical transition.

Figure 6.12: Comparison of return loss for circuit model and simulation for VTT stripline to CPW vertical transition

Figure 6.13: Comparison of S11 for circuit model and simulation for VTT stripline to CPW vertical transition

The circuit model accurately represents the transition. The plot of S11 on the Smith chart (Figure 6.13) shows excellent agreement until the curves separate, at approximately 29 GHz. Likewise, the return loss graph (Figure 6.12) shows good agreement up to the same frequency. After 29 GHz, the transition is dominated by effects not included in this circuit model. In this respect, the model is faced with the same problem faced in the stripline to stripline case. It is likely that the effects which dominate the transitions are the same.

The parameter values are:

$$L1 = 85.6 \text{ pH}$$

$$L2 = 158.8 \text{ pH}$$

$$C1 = 179.5 \text{ fF}$$

$$C2 = 44.4 \text{ fF}$$

If these values are compared to that of the D2 stripline to stripline case (case c): appropriate, because of same via diameter, and via pad size), one would expect to see a reduction in inductance, due to the shorter via connection. Indeed, the inductance is reduced, L1 goes from 110 pH to 85.6 pH, L2 from 250 pH to 158.8 pH. One would also expect to see two capacitance changes, from the changed stripline geometry (the closer layers in the VTT process would increase capacitance) and from the CPW open (one would expect lower capacitance due to the triangular nature of the open). As expected, C1 increases (from 145 fF to 179.5 fF) and C2 decreases (from 115 fF to 44.4 fF).

6.3: CPW to CPW Vertical Transition Model

The similarity between the stripline to stripline and stripline to CPW vertical transitions seems to be that transmission line vertical interconnects can be modeled with the same ladder network of two inductors and two capacitors. Indeed, all the transitions examined so far have the same S11 spiral, and Figure 6.14 is no exception.

Figure 6.14: S11 of CPW to CPW vertical transition.

Therefore, the model was applied to this transition also, giving the results:

Figure 6.15: Lumped element model of CPW to CPW vertical transition.

The model shows excellent agreement with the HFSS simulation, and the comparisons are made in Figures 6.16 and 6.17.

Figure 6.16: Circuit model versus HFSS simulation of Return Loss of VTT CPW to CPW vertical transition.

Figure 6.17: Circuit model versus HFSS simulation of S11 of VTT CPW to CPW vertical transition.

This model agreed with the simulated results very well, because the CPW to CPW vertical transition does not curl around the centre of the Smith chart more than once (Figure 6.17). This is most likely due to the fact that the ground planes in this transition undergo the same discontinuity as the conducting metal. This indicates that although there is some field discontinuity, the potentials between conductor and ground are unchanged. In both previous cases there were direct ground connections (two striplines shared a ground plane, the CPWG line was formed from a stripline ground). In comparison to the VTT stripline to CPW transition, the inductance is expected to increase, as the vertical connection looks like a higher impedance CPW line (the two side grounds move away from the centre conductor). The capacitance is also expected to decrease slightly, as the CPW open from the stripline to CPW transition has been changed to a CPW overhang. Indeed, the inductance increases substantially, with $L1$ going from 85 to 100 pH, and $L2$ increasing to 250 pH from 158. The capacitance also decreases on the whole, with $C1$ changing from 179.5 fF in the CPW to stripline transition to 100 fF. $C2$ actually increases, from 44 fF to 85 fF, and this is likely due to the fact that the model is not completely representational.

However, the model follows the curve very well, and has comparable element values to the other transitions.

6.4: CPW to Microstrip Vertical Transition Model

The last transition analyzed was the CPW to microstrip vertical transition. This transition is analyzed using the same modeling network as the others. Again, it has the same spiraling S11, shown in Figure 6.19.

Figure 6.18: HFSS simulated S11 for the VTT CPW to microstrip transition

The network values were as below:

Figure 6.19: Network values for VTT CPW to microstrip model.

The results were good up to 25 GHz (see Figures 6.20 and 6.21).

Figure 6.20: Circuit model versus HFSS simulation of Return Loss of VTT CPW to Microstrip Vertical Transition

Figure 6.21: Circuit model versus HFSS simulation of S11 of VTT CPW to Microstrip Vertical Transition

This transition is most similar to the stripline to CPW vertical transition, except that the ground connection in this transition is the simplest. With the CPW being formed from the microstrip ground, currents can flow easily from one to another. The ease in which the ground connection is made is the reason that this transition behaves most like a section of low-impedance transmission line.

Note that the S11 Smith chart curves for all the vertical transitions resemble one another, with the same single spiral and the same extra curl that the model cannot follow. The values are similar, with two exceptions. L2 doubles from the stripline to CPW transition; from 158.8 pH to 350 pH, and so does C2, increasing to 110 fF from 44.4 fF. These large changes are difficult to explain, and are perhaps due to the fact that these components dominate the transition much more than other sources of inductance and capacitance.

6.5: Comparison of Model Results

An MMIC via with a 100 μm diameter and 50 μm length has an inductance between 20 and 30 pH. The vias in all but the stripline to stripline transition are 107 μm long, with the stripline to stripline case using a via of length 325 μm . The LTCC vias are all 150 μm in diameter. Given that the transitions are surrounded by 1000 μm of line on either side of the via, the model inductances of 80 pH to 350 pH are not unreasonable, especially since the model inductances do not represent the via inductance directly.

However, the fact that all the simulation results can be simulated with the same ladder network of two inductors and two capacitors, and that all the simulation results

have parameter values in the similar range is encouraging. These models are meant only for qualitative purposes, and serve mainly to demonstrate the unexpected amount of shunt capacitance that dominates the transitions.

This Chapter presented circuit models for four vertical transitions. These models of two inductors and two capacitors allow for a greater understanding of transition behaviour. In Chapter VII, the transitions are measured, and the results compared to the models and simulations.

VII: Measurements

7.1: Finished Package

The LTCC package was fabricated at the Technical Research Centre of Finland, in Oulu, Finland. The package measured 4.5 inches by 4.5 inches, and was cut into thirds, with the same test structures repeated three times on a single LTCC substrate. The test circuits could be divided into two groups: circuits with microstrip launches and circuits with CPW launches. The results are shown divided in this way. As measured by the manufacturers, the layer thickness varied from 107.5 μm to 108.3 μm . The line thickness was between 18 and 19 μm . The finished package also had very rough metal, as depicted in Figure 7.1.

Figure 7.1: Microscope photograph of microstrip change in width.

Figure 7.1 shows the roughness of the screen-printed conducting tracks that are used in this LTCC package. At microwave frequencies, currents are only flowing in the very outer edges of the conductor. With a very rough outer edge, this increases insertion loss.

Figure 7.2: Microscope photograph of a CPW line becoming embedded.

Figure 7.2 depicts a CPW to CPW feedthrough, with the exposed CPW on the left and the embedded CPW hidden by the ceramic on the right. The cavity wall is marked by the vertical line in the centre of the picture. This line is not straight, but meanders slightly. With a balanced line like CPW, it is important to keep both side grounds at the same potential. An effect which impacts one side differently from the other can potentially launch the slot-line mode.

Figure 7.3: Microscope photograph of a CPW short circuit.

Figure 7.3 demonstrates an asymmetrical ground connection on a CPW short circuit. The upper gap is 12 μm longer than the lower gap. This asymmetry can cause slotline moding problems with CPW lines. Also, the centre conductor curves as it makes the ground connection. This is a departure from the layout, where all lines were straight.

Figure 7.4: Microscope photograph of an open circuit quarter-wave transformer.

Another deviation from the design was the change in dimension of conducting tracks. All the lines were 20–40 μm smaller than designed. This applies to both length and width: i.e. a 1 mm long 150 μm wide microstrip line becomes 115 μm wide, and 970 μm long after manufacture. This is likely due to a shrinking feature of the silver paste used in construction. One explanation is that the paste curls up on all sides like a drop of water on a smooth surface. Alternately, it could be that the silver paste is shrinking during package firing. Whatever the reason, it can have drastic effects, especially in impedance transformation circuits like Figure 7.4. A change in length from 1 mm to 970 μm is not very problematic, but 150 to 115 μm is. This problem will most likely be corrected by VTT through further characterization of the silver paste.

Figure 7.5: Microscope photograph of a grounding via

Also, the vias tended to interact rather strongly with the metals they connected with. Figure 7.5 shows the crater-like connection that the via makes. A raised circle of metal followed by a depressed interior. This can (due to the fact that currents only flow in the very outer conductor edge) add to losses. Also, sometimes the vias were not positioned exactly, as shown below:

Figure 7.6: Microscope photograph of a misplaced via; the via should be in the centre of the via pad.

7.2: Microstrip Test Circuits

All the microstrip test circuits began with a microstrip line on level 4, 107 μm above an intermediate ground plane on level 3, which is connected to the bottom of the package through three-level vias. These circuits were built to measure microstrip to stripline feedthroughs and stripline to CPW vertical transitions. As the stripline maximum impedance was 30 Ω (see section 3.3), an impedance transformation was required in the form of a microstrip quarter-wave transformer. Circuits were designed to use a TRL calibration standard to exclude the effects of the cables, probe launch, and impedance transform. Therefore, the following standards were used:

- 1) 1.3 mm microstrip through line;
- 2) 2.4 mm microstrip delay line;
- 3) 0.65 mm microstrip open circuits.

Figure 7.7: Microstrip TRL standards, dimensions in mm.

To have a $50\ \Omega$ impedance, the width was $150\ \mu\text{m}$. Due to the manufacturing variations, this dimension was typically reduced to somewhere in between 115 and $125\ \mu\text{m}$. Likewise, the lengths typically lost $30\ \mu\text{m}$ from their designed lengths to become 1.27 mm, 2.37 mm, 0.620 mm, respectively.

These calibration standards advance the reference plane to 0.65 mm along a microstrip line. These standards were also used to measure some simple microstrip lines. The next standards that were used were the impedance transformation standards. These included:

- 4) Back to back microstrip quarter-wave transformers, 4.7 mm total length.
- 5) Back to back microstrip quarter-wave transformers, 5.8 mm total length.
- 6) Microstrip quarter-wave transformers terminated in open circuits, 2.35 mm total.

Figure 7.8: Back-to-back microstrip quarter-wave transformers and TRL standards, dimensions in mm.

The quarter-wave transformers used the following ideal impedances: $50\ \Omega$, $38.7\ \Omega$, $30\ \Omega$. This required the widths to be: $150\ \mu\text{m}$, $220\ \mu\text{m}$, $320\ \mu\text{m}$. From manufacture, these deviated to approximately 115 , 190 , $290\ (\mu\text{m})$. The length of the $38.7\ \Omega$ section was designed as a quarter-wavelength at $30\ \text{GHz}$, $1100\ \mu\text{m}$. The other sections (in circuit 6) were $750\ \mu\text{m}$ for the 50Ω , and $500\ \mu\text{m}$ for the 30Ω section. For the delay line, the $1000\ \mu\text{m}$ length of $30\ \Omega$ microstrip became $2100\ \mu\text{m}$. As before, these lengths decreased by approximately $30\ \mu\text{m}$.

These standards advance the reference plane to $2.35\ \text{mm}$ from the probe tips, and establish a $30\ \Omega$ reference plane. This allowed the measurement of $30\ \Omega$ microstrip to 30

Ω stripline feedthroughs, which also served as TRL calibrations themselves. The circuits are:

Figure 7.9: Microstrip to stripline feedthroughs / TRL calibrations, dimensions in mm.

These circuits (Figure 7.9) allow for the measuring of two feedthroughs (#7 and #8 – from a reference plane located in the 30 Ω microstrip) as well as to advance the reference plane to the reference plane 4.1 mm from the probe tips, to 30 Ω stripline. The stripline in circuit 7 has length 2500 μm , and is sandwiched between two sections of embedded microstrip. The embedded microstrip sections are necessary as the stripline ground cannot (due to VTT design Rules) touch a cavity. Therefore the embedded

microstrip sections involve a change in width to accommodate the change in dielectric. The stripline width is $150\text{ }\mu\text{m}$, and grounding vias (in white) are spaced $425\text{ }\mu\text{m}$ from the edge of the stripline. These vias are $214\text{ }\mu\text{m}$ (two layers) tall, spaced $950\text{ }\mu\text{m}$ apart, and connect the stripline upper ground plane to the intermediate ground plane. It is not possible to measure the embedded conductors, but it is likely that they have suffered the same shrinking effects as the other conductors.

Once the reference plane is advanced to the $30\text{ }\Omega$ stripline, a back to back stripline to CPW vertical transition can be measured. This transition has 4 variations: 10a: "normal", 10b: with posting via, 10c: with PAB under the CPW, and 10d: with PAB and posting via. These variations are shown in Figure 7.10. The CPW line is embedded, with one layer of ceramic above it, and has a gap width of $150\text{ }\mu\text{m}$ and a centre conductor with of $440\text{ }\mu\text{m}$. The centre conductor is $3250\text{ }\mu\text{m}$ in length, not including via pads. The grounding vias are now $275\text{ }\mu\text{m}$ from the edge of the ground plane, and are still $214\text{ }\mu\text{m}$ tall, connecting the coplanar grounds to the intermediate ground plane. The vias are spaced $850\text{ }\mu\text{m}$ apart.

Figure 7.10: Stripline to CPW Vertical Transitions, dimensions in mm.

The PAB lines are located $107\ \mu\text{m}$ below the CPW lines, and contain an extra central via, $107\ \mu\text{m}$ in height, to connect the PAB to the intermediate ground plane. The PAB is $1550\ \mu\text{m}$ wide, and $250\ \mu\text{m}$ long. The reference plane from the TRL calibration is $110\ \mu\text{m}$ from the stripline via pad, which is a circle $250\ \mu\text{m}$ in diameter. The hole in the stripline top ground, from point to point, is $4.2\ \text{mm}$ long. The dimensions should always be considered $30\ \mu\text{m}$ smaller in reality.

7.2.1: Measurements

The microstrip standards showed good measured results:

Figure 7.11: Measured Results for a 1.3 mm microstrip through line.

Figure 7.12: Measured Results for a 2.4 mm microstrip delay line.

The return loss is consistently under -20 dB, and up to 30 GHz the insertion loss is approximately -0.25 dB. From section 3.2, microstrip attenuation at 30 GHz is -0.08236 dB / mm, yielding -0.107 dB for 1.3 mm and -0.197 dB for 2.4 mm. The difference in the measured results from the theory is likely due to the roughness of the screen-printed silver conductor.

The previous measurements were made using an open-short-load calibration, as they were the most basic structures. The following measurements use those lines as part of a TRL calibration to remove the effects of the probe launch.

Figure 7.13: Measured Results for a back to back microstrip quarter-wave transformer.

The measured response for the back-to-back quarter-wave transformers (Figure 7.13) indicates a problem with the TRL calibration. The insertion loss of this passive structure demonstrates gain at above 31 GHz. It is likely that the calibration fails above 31 GHz due to small amounts of line radiation, which can be seen in the measured results of circuits 1 and 2 (Figures 7.11 and 7.12). The return loss shows an appropriate shape,

having a minimum at 30 GHz, and having a -15 dB bandwidth of 12 GHz, from 23 to 35 GHz.

Figure 7.14: Measured Results for back to back microstrip to stripline feedthroughs.

The microstrip to stripline feedthrough is usable up to 30 GHz before the performance degrades significantly (see Figure 7.14). Up to this range, however, the performance is excellent: $S_{11} < -20$ dB, $S_{21} > -0.5$ dB. The S_{21} peak at 27 GHz is perhaps due to a calibration problem. In any case, this feedthrough is definitely usable for LMCS/LMDS applications.

In the measurement of the vertical transitions, some results were expected. As simulated, the introduction of the PAB caused a degradation in performance. The posting vias had a minor effect.

Figure 7.15: Measured Results for back to back stripline to CPW vertical transition.

Figure 7.16: Measured results for back to back stripline to CPW vertical transition with posting vias.

Figure 7.17: Measured results for back to back stripline to CPW vertical transition with posting vias and PAB grounding.

Comparing the results for 10a) (Figure 7.15) and 10b) (Figure 7.16), one sees that the posting vias introduce a reflection which can be seen in the return loss curve. Otherwise, these vias do not seem to affect the results. The effect of the PAB (as seen above, Figure 7.17) is to render this transition useless above 20 GHz. This was expected, as the PAB cannot be low enough to not interfere with the CPW line. In the measurements without the PAB, this transition is excellent for LMCS applications: the return loss is very low ($S_{11} < -20$) and insertion loss does not go below -0.5 dB below 30 GHz. However, this transition quickly loses desirability as one continues into the millimetre-wave range. The line radiates heavily and shows gain due to radiation after 35 GHz.

To ensure that the calibration is not adversely affecting the measured results, the same structures were simulated following a SOLT calibration on a known substrate.

Figure 7.18: Measured results of back to back stripline to CPW vertical transition after SOLT calibration.

The measurement shown in Figure 7.18 includes the effects of: two probe launches, two microstrip to stripline feedthroughs, and two quarter-wave transformers. The quarter-wave transformers are responsible for the performance below 20 GHz, and the ripples are due to the large length of this structure (over 12 mm). Still, the transition shows a return loss less than -17 dB and insertion loss > -0.9 across the entire LMCS/LMDS band. It seems clear that the transition is well-matched and low loss.

7.2.2: Agreement With Simulation

The measured results did not always agree with the HFSS simulations done before manufacture. Consider the microstrip to stripline feedthrough results shown below:

Figure 7.19: Comparison of measurement and simulation for microstrip to stripline feedthrough.

In this comparison, the simulated return loss agrees in shape with the measured return loss, but predicts a response 10 dB better. This discrepancy is regrettable, but understandable, given the change in line dimensions due to manufacturing. The HFSS simulation could not predict the insertion loss measurement, and this is due to the fact that the HFSS simulation had infinitely thin metals, and avoided the intermediate ground plane that is responsible for radiation in the 30 GHz+ region.

Figure 7.20: Comparison of measurement and simulation for stripline to CPW vertical transition.

In Figure 7.20, the comparison of measurement and simulation for circuit 10a), good agreement is seen, with the exception of in the very high frequencies (above 35 GHz). In the 10 to 25 GHz range, the case is such that the measured results are better than the simulated results. This is not usually the case, but can possibly be attributed to the fact that some of the simulated impedances were not quite 50Ω , but perhaps 47, 48 Ω . With the real circuit, the conductors now have thickness which can push the impedance up to its correct value. Both the simulation and measurement show a low point for return loss at 27 GHz, and the behaviour from 27 to 35 GHz is quite closely matched. Again, the insertion loss is not modeled closely, as the simulation used infinitely thin lines with no conductor or dielectric losses.

The simulations suggest that HFSS could be used to predict the return loss quite comfortably. Predicting insertion loss with a 3D simulator is quite difficult, as

simulations with finite thicknesses and lossy conductors and dielectrics are very time consuming.

7.3: Coplanar Test Circuits

An exposed CPWG line had two sets of grounding vias: those that connected the coplanar grounds to the intermediate ground plane, and those that connected the intermediate ground plane to the ground at the bottom of the package. In future diagrams, the vias that connect the coplanar grounds to the intermediate ground are shaded white, while those that connect the intermediate ground to the bottom ground are shaded dark, as in Figure 7.21.

Figure 7.21: Ground plane arrangements for coplanar circuits.

When PABs are used with microstrip lines, they have the geometry shown below:

Fig 7.22: Pseudo air-bridge use with microstrip lines and ground planes.

When PABs are used with CPW lines, they have the geometry shown below:

Fig 7.23: PAB use with coplanar line.

There were 12 measurements that started and ended with CPW lines.

To calibrate out the effect of the probes and cables, the following calibration lines were used:

- 1) 0.75 mm exposed CPWG short circuits.
- 2) 1.5 mm exposed CPWG through line.
- 3) 2.7 mm exposed CPWG delay line.

Figure 7.24: CPW TRL standards, dimensions in mm.

To move the reference plane to an embedded CPWG line, the following standards were used:

- 4) 2.5 mm exposed CPWG feedthrough (as in Section 4.4.2) to embedded CPWG short circuit (1 mm exposed, 1.5 mm embedded).
- 5) 5 mm back to back CPWG feedthroughs (two sections of 1 mm long exposed CPWG lines separated by 3 mm of embedded CPWG line).
- 6) 6 mm back to back CPWG feedthroughs (two sections of 1 mm long exposed CPWG lines separated by 4 mm of embedded CPWG line).

Figure 7.25: CPW to CPW feedthroughs, dimensions in mm.

Once the reference planes were advanced to be within the ceramic, 2 vertical transitions were measured, each with four variations. These were:

- 7) CPW to microstrip vertical transition: 1 mm of exposed CPWG, CPW to CPW feedthrough, 1.6 mm of embedded CPWG, vertical via, 1.75 mm exposed microstrip, vertical via, 1.6 mm of embedded CPWG, CPW to CPW feedthrough, 1 mm of exposed CPWG.
- 8) CPW to CPW vertical transition: 1 mm of exposed CPWG, CPW to CPW feedthrough, 1.775 mm of embedded CPWG, vertical transition, 1.5 mm exposed CPW line, vertical connection, 1.775 mm embedded CPWG, CPW to CPW feedthrough, 1 mm of exposed CPWG.

Circuit 7a

Circuit 7c

Circuit 7b

Circuit 7d

Figure 7.26: CPW to microstrip vertical transitions, dimensions in mm.

Figure 7.27: CPW to CPW vertical transitions, dimensions in mm.

The parameter variations dealt with grounding: both transitions were repeated with extra floating ground vias as well as with PAB structures.

As shown in the diagrams, there are 4 possible variations on each of these transitions. The a) transitions are taken as “normal”. The b) transitions have extra grounding that connects the intermediate ground plane to the bottom ground plane. This tests for the presence (and impact) of posting (see section 1.6). The c) transitions are the same as a) except with a PAB used as per section 8.1. Finally, the d) transitions are a combination of b) and c), that is, with posting vias and PABs.

7.3.1: Coplanar Measurements

Originally, circuits 1-6 were to be used as TRL calibration standards to measure circuits 6,7,8. However, it was impossible to make a functioning TRL calibration. The calibration demonstrated gain. This was due to a radiation problem seen in circuits 1 and 2. Using a calibration substrate, the system was calibrated to the probe tips. This allowed two port measurements to be made.

Figure 7.28: Measured S-Parameters of 1.5 mm CPWG through line.

Clearly there is radiation happening in this CPWG line (see Figure 7.28). At 28.5 GHz, energy is being lost, as a return loss of -12 dB does not correspond to an insertion loss of -2.4 dB. In circuit two, this effect is distributed:

Figure 7.29: Measured S-Parameters of 2.7 mm CPWG line.

Here (Figure 7.29) radiation is seen at three distinct frequencies: 17.5 GHz, 21 GHz, and 35.5 GHz. This radiation adversely effects all of the measurements to come.

Figure 7.30: Measured S-Parameters of 5 mm CPW to CPW feedthrough.

In Figure 7.30 the 5 mm CPW to CPW feedthrough demonstrates excellent performance until struck by radiation at 28.5 GHz. Similarly, circuit 4, the longer CPW to CPW feedthrough, is also affected, and this is shown in Figure 7.31.

Figure 7.31: Measured S-Parameters of 6 mm CPW to CPW feedthrough.

In this longer circuit, the radiation points are now 26 GHz and 32.5 GHz. Therefore, despite having an excellent impedance match ($S_{11} < -20$ dB to 30 GHz), this feedthrough is unusable for LMCS/LMDS applications.

The vertical transitions fare better, but still show radiation. Figures 7.32 to 7.35 show the results for circuits 7, a) to d), in order:

Figure 7.32: Measured S-Parameters of CPW to microstrip vertical transition (circuit 7a)

Figure 7.33: Measured S-Parameters of CPW to microstrip vertical transition (circuit 7b)

Figure 7.34: Measured S-Parameters of CPW to microstrip vertical transition (circuit 7c)

Figure 7.35: Measured S-Parameters of CPW to microstrip vertical transition (circuit 7d)

These results show a transition with an excellent impedance match ($S_{11} < -10$ from DC to 40 GHz) but with a radiation problem at 27.7 GHz. All of the transitions

demonstrate a dip in S_{21} at this frequency. The radiation is worst in circuits 7a) (Figure 7.32) and 7b) (Figure 7.33), with S_{21} dipping to below -1.5 dB. Circuits 7c) (Figure 7.34) and d) (Figure 7.35) demonstrate an improvement, but not an elimination of the problem. It appears that the use of the PAB to ground the microstrip ground plane to the intermediate ground plane lessened the radiation, and changed S_{11} from worse than -1 dB to less than -1 dB (with no posting). The effect of the posting vias is to make this radiation very slightly worse.

The radiation also plays a role in the CPW to CPW vertical transitions. The results for circuits 8a to 8d are shown in Figures 7.36 to 7.39.

Figure 7.36: Measured S-Parameters of CPW to CPW vertical transition (circuit 8a)

Figure 7.37: Measured S-Parameters of CPW to CPW vertical transition (circuit 8b)

Figure 7.38: Measured S-Parameters of CPW to CPW vertical transition (circuit 8c)

Figure 7.39: Measured S-Parameters of CPW to CPW vertical transition (circuit 8d)

The CPW to CPW vertical transition does not vary much in cases a) through d). All cases radiate at 27 and 33 GHz, and all cases radiate near the same amount. The effect of the PAB and the posting vias seems negligible. All of the transitions demonstrate an excellent impedance match, with $S_{11} < -18$ from DC to 32 GHz. However, the unwanted radiation occurs directly in the LMCS/LMDS band, making these transitions useless for this area unless the radiation can be eliminated.

As the radiation prevented a TRL calibration from being made, these measurements include much line length, as well as two CPW to CPW feedthroughs. To make a measurement that reflected the CPW to CPW vertical transition more accurately, half of the exposed third level CPW line was removed via scraping, allowing for a measurement of half the structure, namely less line length and only one CPW to CPW feedthrough. A view of this is shown below:

Figure 7.40: The scraped exposed conductor. The vertical transition is on the left side of the picture. The probes touched down on the right-hand side.

The scraping was difficult to do precisely, so only two structures were altered, namely 8a) and 8c). The measurements were done to a higher frequency, 50 GHz, but with 40 GHz probes. The measurements cannot be considered as accurate after 47 GHz, where the probes begin to support other modes. The S-Parameters are depicted in Figures 7.41 and 7.42.

Figure 7.41: Measured S-Parameters of half of circuit 8a, cut as in Figure 7.40.

Figure 7.42: Measured S-Parameters of half of circuit 8c, cut as in Figure 7.40.

These results show dramatic differences between the two responses. The first, with regular grounding, no longer suffers from radiation at 27 GHz, but still has radiation at 33 GHz. The second response has a worse insertion loss in general, and keeps the 27

and 33 GHz radiation points seen in the OSL measurements. It is difficult to draw conclusions from these results, as the rough cut on the probe side will affect the results. If all the metal is not removed then the response will be unpredictable. This seems to be what has happened in Figure 7.42. Also, since the scraping is not exact, the two circuits have different cuts. However, the results demonstrate that, if there were no radiation, the transition would perform well up to 35 GHz. Indeed, this statement can be applied to all the CPW measurements made: if there had been no radiation, the feedthroughs and transitions would be ideally suited for microwave and even millimetre-wave packages. Chapter 8 looks at methods of stopping the radiation.

7.3.2: Agreement with Simulation

The main problem with the simulation of the CPW circuits is that the simulations that were made in Chapter V did not predict any of the CPW radiation problems. Chapter VIII looks at why this was the case, and how to make the simulator predict these resonances. However, the simulations were better at predicting return loss (note that the simulations did not take into account losses in the conductors or dielectrics, which explains the unnaturally good insertion loss curves). The main circuits of note were the feedthroughs and the vertical transitions.

Figure 7.43: Measured and simulated results for the 5 mm CPW to CPW feedthrough (circuit 6).

From Figure 7.43, the simulation predicts the rolling nature of the return loss curve, but is slightly off in frequency about where the nulls occur. This is due to the fact that, in the measurements, the probes touch down slightly into the circuit, making the length different. At 28 and 35 GHz, where the radiation occurs, the simulation shows nothing. The S11 curves do both finish at -20 dB at 40 GHz, however.

Figure 7.44: Measured and simulated results for cut-in-half CPW to CPW vertical transition.

For the vertical transition results of Figure 7.44, the comparison of measurement and simulation shows an excellent agreement, except for the occurrences of radiation. Again, the simulation does not take into account losses, explaining the low insertion loss in the simulated case. The measured results have a slightly better return loss, likely due to the fact that the simulation used infinitely thin metals, and the slight thickness of the manufactured conductors pushed the lines closer to 50Ω . The difference in impedance can be seen at the very low frequencies.

The CPW to microstrip line was also simulated (in section 5.5):

Figure 7.45: Measured and simulated results for the CPW to microstrip vertical transition of circuit 10a.

In Figure 7.45, the agreement is not good. Much of the disagreement stems from the radiation in the measured results. If the simulation is compared to circuit 10c, where a PAB is used to reduce radiation, better agreement is seen:

Figure 7.46: Measured and simulated results for the CPW to microstrip vertical transition of circuit 10c.

In Figure 7.46, the curves have a better agreement. This indicates that the simulation is assuming closer potentials on ground planes than exists in reality. The two curves still have some discrepancies, however, notably the differences near 10 GHz and near 23 GHz. The difference at 10 GHz can be explained through probe placement. The difference at 23 GHz corresponds to a reflection in the simulation that does not exist in the measurement. If the simulation did not have the low at 23 GHz, the curves would show excellent agreement, with the same rise after 10 GHz, and the same drop after 25 GHz. Both curves also increase in the same fashion after 30 GHz.

This agreement except for problems is very important. For LTCC packages to be used in commercial packages, the simulators must have the ability to predict areas of unwanted radiation. Chapter VIII explores the origin of this radiation as well as ways of making the simulators detect it.

VIII: Radiation

8.1: Radiation in the Coplanar Test Circuits

Measurements demonstrate a non-simulated occurrence that makes many CPW transitions and feedthroughs unusable for the LMCS/LMDS frequency band. Since the transitions generally have good performance other than these unwanted resonances, especially return loss, it is necessary to determine the cause of, and a method of eliminating these points of radiation. As the radiation occurs even in the simplest CPWG line, it stands to reason that the radiation is due to line geometry rather than being excited by a discontinuity. Circuit 1 (Figure 7.28) was measured as a one-port measurement. Ideally, this would show an open circuit, an S_{11} of zero across all frequencies. However, this is not the case:

Figure 8.1: One-Port measurement of 1.5mm CPWG line.

The response of Figure 8.1 shows a clear point of radiation at 28.5 GHz (as with the previous measurements, the response after 47 GHz cannot be considered valid). Circuit 2, the 2.7 mm CPWG line, also shows resonances in a one-port measurement, as below:

Figure 8.2: One-Port measurement of 2.7 mm CPWG line.

Circuit 2 (Figure 7.29) shows radiation at 17.25 GHz, 21.65 GHz, and most notably at 35.22 GHz. As the resonances have changed location from Circuit 1 to Circuit 2, it seems there must be some length dependency, as the widths of the lines and ground planes are the same. However, there does not seem to be a simple correlation between the two. This lack of a simple correlation is perhaps due to the grounding vias. In circuit 1, the intermediate ground plane is connected to the bottom ground plane with only two vias, located midway along the structure, at the edges of the ground plane. However, in circuit 2, the grounding was accomplished with four vias, this time located at the corners of the intermediate ground plane. There were never any vias in the centre of these structures.

It is likely that the resonances come from an improperly grounded intermediate ground plane, and that if (like the simulations) the intermediate ground plane was the bottom ground, that these resonances would not exist. To solve this problem, the first step is to find a simulator which can predict this resonance. Momentum, a 2.5D EM solver commonly used for antenna design, somewhat solves this problem.

Figure 8.3: Comparison of Momentum simulation and measured data for 1.5 mm CPWG line (1 port).

Figure 8.4: Comparison of Momentum simulation and measured data for 2.7 mm CPWG line (1 port).

The Momentum simulations of Figures 8.3 and 8.4 do show resonances, but tend to have the wrong frequency. In the comparison of 1.5 mm CPWG lines, the simulator predicts a resonance at 17 GHz, where the measurements only indicate a small loss. The simulator also does not predict the 28.5 GHz resonance measured. In the 2.7 mm CPWG delay line, where the 17 GHz resonance is more pronounced, the simulator predicts a loss of -4 dB, as opposed to the -1 dB measured. The simulator also predicts a resonance at 28.5 GHz, missing the measured resonance at 35 GHz.

To attempt to simulate the problem, more complete structures were drawn in HFSS. Speculating that the ports (which short circuit undefined modes) were the reason that the simulations of Chapters IV and V did not predict the resonance, simulations were performed involving finite-ground coplanar (FGCPW) feed lines. These lines served as the ports, and the area around the circuit was built with radiation boundaries. After the simulation was finished, the FGCPW lines were de-embedded up to the change in width. Two 3D views are shown below:

Figure 8.5: HFSS 3D view of 1.5 mm line. The finite ground coplanar lines are used to feed the structure, as it will not radiate if the CPW lines under test are touching the simulation box.

Figure 8.6: HFSS 3D view of 2.7 mm line. Simulations could be sped up if only half the structure was simulated, using a magnetic wall. Simulations determined that the use of the magnetic wall did not affect the results.

The simulation results now show radiation. However, the radiation is not always in the correct points, as evinced by Figure 8.7.

Figure 8.7: HFSS simulation versus measurement for CPWG lines.

In the 1.5 mm line, the simulation shows a point of radiation that did not exist in the measurements. In the 2.7 mm line the simulation does not show an existing radiation point. These inaccuracies mean that the simulations must be carefully considered, and

cannot be taken for granted as ideal. It is difficult to use HFSS simulations to remove the radiation as the results could not be completely trusted. It is likely that the simulator can predict the resonances, but the problem must be defined very carefully.

To gain insight into the resonances, more measurements were necessary. Using a Dremel tool, the bottom gridded ground plane was removed. This allowed a measurement (with the LTCC package mounted on top of an insulating glass slab) to determine if the resonances existed between the CPW and intermediate ground or between intermediate ground and lower gridded ground plane.

These measurements indicated that the resonance was occurring between the CPW lines and the intermediate ground plane, most likely the parallel plate / microstrip mode. There were some small changes in the resonances, but not substantial. The effects at 17 GHz did disappear in both lines, suggesting that this effect was related to the gridded ground plane. As the 1.5 mm line was wider than it was long, and the 2.7 mm line was longer than it was wide, it seemed as if the 1.5 mm line was resonating in width and the 2.7 mm line was radiating in length.

The epsilon effective of the parallel plate mode would be the epsilon of the ceramic, 7.1. In such a medium, at 28.5 GHz, a half-wavelength measures 1.94 mm, quite close to the width of the intermediate ground plane. At 22 GHz, a half-wavelength measures 2.558 mm, reasonably near 2.7 mm, the length of the delay line. It seems, therefore, that the radiation comes from a parallel plate resonance between the CPW line and the intermediate ground plane. To test this theory, the ground planes were shortened, also with the Dremel. The ground plane width was reduced by slightly less than half, making the total CPW width similar to the intermediate ground plane. This procedure

was performed on the CPW TRL standards, on a CPW to CPW feedthrough, and on a CPW to CPW vertical transition. On the CPW to CPW feedthrough, the ceramic was cut through in order to thin the entire line. The results are shown below:

Figures 8.8 and 8.9: S-Parameters of Ground-Reduced CPW lines.

The results of these measurements indicate an increase in the frequency of the resonance in all cases. The reason that the resonance only moves up in frequency slightly is that, since the resonance is between the CPW and the intermediate ground plane, and the CPW overhangs the intermediate ground plane on both sides, the resonant frequency is determined by the width of the intermediate ground plane. This is depicted graphically in Figures 8.10 and 8.11.

Figure 8.10: Original: CPW sides overhand intermediate ground plane

Figure 8.11: Cut: CPW sides same length as intermediate ground plane

Cutting the CPW ground planes changes the resonant length only slightly, by reducing the fringing fields. This has the effect of very slightly increasing the resonant frequency. In the 2.7 mm CPW delay line where the resonance is lengthwise, the resonances increase in the same way as a rectangular waveguide cavity, where the resonant frequency increases as width decreases.

Since the resonances were changed due to a decrease in the ground plane width, it was desired to see the effects of an increase. Using silver paint, the ground planes were

extended in two different ways: 1) only in width (black solid of Figure 8.12) and 2) in width and length (black solid plus dotted line area of Figure 8.12).

Figure 8.12: Silver paint increasing the width of a CPW ground plane. The dotted line indicates the area where the silver paint was used to extend the length as well as the width.

Both cases removed the radiation from the CPW TRL standards, as shown in Figures 8.13 through 8.16.

Figure 8.13: Comparison S11 of different CPW grounds in One-Port measurement of 1.5 mm CPW through line.

Figure 8.14: Comparison S11 of different CPW grounds in One-Port measurement of 2.7 mm CPW delay line.

Figure 8.15: Comparison S11 of different CPW grounds in One-Port measurement of 1.5 mm CPW through line.

Figure 8.16: Comparison S11 of different CPW grounds in One-Port measurement of 2.7 mm CPW delay line.

The responses are very similar up to 30 GHz. After 30 GHz, there appear some changes: in the 1.5 mm line the line with the extended sides introduces a small resonance at 32.5 GHz that the other does not. In the 2.7 mm line there are some dramatic differences between 35 and 45 GHz, but the two curves match up again after. As there are no differences between these two approaches in these two circuits, they both were used to alter the ground planes of the CPW to CPW and CPW to microstrip vertical transitions. Both cases (exposed conductor extended versus silver paint everywhere) are plotted for feedthroughs and vertical transitions. The silver paint extensions are shown in Figure 8.17 with the S-Parameters plotted in Figures 8.18 and 8.19.

Figure 8.17: Silver paint extensions for CPW to CPW vertical transitions

Figure 8.18: Comparison of S-Parameters for two different ground extensions on the CPW to CPW vertical transition. Thick lines represent the extended length and width.

Figure 8.19: Comparison of S-Parameters for two different ground extensions on the CPW to CPW with PAB vertical transition. Thick lines represent the extended length and width.

In the first case, the extended width only does not remove the persistent radiation at 28.5 GHz. The extensions of both length and width do, however. In the second case, the transition with the PAB, both grounding schemes prevent the emergence of the 28.5 GHz radiation. This suggests that, taken together, the extended ground plane and the PAB can eliminate this radiation. However, taken separately, the radiation continues. In either case the big silver ground extension eliminates the radiation. Unfortunately, the big silver is somewhat unrealistic, as it connects CPW ground planes that are on different levels. The insertion loss in all of these cases is very similar (apart from the radiation) to the original measured data. This indicates that the silver paint is not eliminating resonances due to its high attenuation, but rather preventing the radiation from occurring.

The silver paint was used on the CPW to microstrip vertical transition in both of these configurations also, as in Figure 8.20. The results are plotted in Figures 8.21 and 8.22.

Figure 8.20: CPW to microstrip vertical transition with different ground extensions.

Figure 8.21: Comparison of S-Parameters for two different ground extensions on the CPW to Microstrip vertical transition. Thick lines represent the extended length and width.

Figure 8.22: Comparison of S-Parameters for two different ground extensions on the CPW to microstrip with PAB vertical transition. Thick lines represent the extended length and width.

This case is similar to the CPW to CPW vertical transition, except that, as seen above, the PAB reduces radiation on its own. In both cases (with and without PAB) however, an extension of both length and width eliminates the radiation. Again the extension of both length and width is unrealistic, as the silver paint connects conductors on different levels.

The reason that the extension of width only does not fix the problem is that only exposed lines can have their ground planes extended. The use of large silver extensions effectively (through capacitive coupling) extends the ground planes of all the transmission lines. However, there are cases where the extended width, along with a PAB, eliminates a parasitic resonance.

Consider the CPW to CPW vertical transition. Since the extension of both length and width prevents radiation that the extended width-only does not, this implies some radiation in the same direction as the CPW line (denoted 'x'). If the radiation is at least somewhat in the 'x' direction, and between the CPW and the intermediate ground, then the extension of the CPW ground planes in the 'y' direction will not prevent said radiation. Unless the ground extension is coupled with a PAB. The intermediate ground could be radiating in both the 'x' and 'y' directions. The extension in length and width eliminates this radiation by stopping it in both the 'x' and 'y' directions. However, the radiation is only stopped otherwise when there is a PAB and extended 'y' ground planes. The extended 'y' ground planes stop the 'y' radiation, and the PABs stop the 'x' radiation.

In the case of the CPW to microstrip vertical transition, the same phenomenon occurs, except that in this case, the PABs ground the microstrip ground to the

intermediate ground much better than the PABs used in the CPW to CPW vertical transition, due to 1) the distance is shorter (2 levels versus 3) and 2) there are more grounding vias. Therefore the PABs reduce the radiation without the introduction of any ground extension at all. This hypothesis of multi-directional resonances is validated by the work of Oliner, who posits that a conductor-backed co-planar waveguide is a leaky line at all frequencies, and that power is lost at an angle to the CPWG direction of propagation.

Figure 8.23: Leaky waves (after [34])

Oliner notes that the CPWG line is leaky due to the fact that the parasitic wave (the parallel plate / microstrip mode) travels slower than the dominant wave, and claims that the radiation can be eliminated by slowing the CPW wave, by embedding the CPW line in dielectric. This can be likened to the stripline to CPW vertical transition, where the CPW line is embedded in 107 μm of ceramic. In this case, there is no unwanted radiation. This supports the theory that the CPW line is radiating due to its leaky nature, and that the power lost (at an angle) is resonating due to the finite width of the

intermediate ground plane and the CPW lines. This theory also explains the need for both 'x' and 'y' radiation blocks, and the fact that the two CPW TRL standards resonate in different directions.

The power lost to leaky waves is generally not large, and it is large only when there is a reason for it to bounce back into the circuit does the loss become large. Therefore, as the ground planes are extended a large distance, the line continues to leak, but the high attenuation of the silver paint means that there are no resonances set up within the circuit. However, if the ground planes had been extended with high-quality silver conductors, it is likely that the structures would still radiate, with the lowest mode at a lower frequency and higher-order modes (multiple standing waves) moving into the LMCS/LMDS bands.

This leaves one sure method of eliminating the unwanted resonances up to 30 GHz – reducing the CPW ground plane width. Of course, these unwanted modes can be removed (almost) entirely if the intermediate and bottom ground planes are removed, and the line can function in pure CPW mode. However, it is likely that a finite ground CPW (FGCPW) line, with a lower ground plane would be able to operate well above the 30 GHz area. The lack of the intermediate ground plane would make the parallel plate/microstrip mode much more difficult to excite. The use of finite ground planes would mean that any side-to-side resonances would be very high in frequency. However, this method would have an upper limit in that even regular CPW supports a leaky mode [39], but this mode should only occur at frequencies well above the LMCS/LMDS band.

IX: Discussion and Conclusion

9.1: Conclusion

The objective of this thesis was to determine if Low Temperature Co-fired Ceramic packages can be used for the packaging of LMCS/LMDS circuitry. To this end, transitions and interconnects that would allow high integration were simulated and measured.

The result of these simulations and measurements has shown that, yes, LTCC packages can be used for LMCS/LMDS circuitry, but with much greater difficulty than originally imagined. The difficulty of EM simulations to predict package resonances due to leaky modes is a problem, but one that, with careful planning, can be avoided. The measured data proves that (provided the resonances can be removed) the transitions and interconnects have acceptable levels of insertion loss and return loss to be used in the 25.5 – 30.5 GHz range. To make simulations that yield trustworthy results is a very important goal. Without such a simulator, LTCC designs will be forced to be either: 1) simple or 2) research oriented.

Also, as the transitions and interconnects tend to degrade in performance after 30 GHz, it is recommended that some elementary tuning be done to extend the transition

behaviour at the expense of the low-frequency match. This would centre the transition operation in the LMCS/LMDS band, and give some room for error.

The repeatability of the LTCC transitions was excellent, certainly good enough for research purposes, but perhaps not reliable enough (see errors in section 7.1) for production. However, these errors will most likely be removed through further characterization of the manufacturing process, an audit to be performed by the manufacturers.

With proper tuning and consideration for the EM effects of the transmission lines, it is likely that LTCC could be used quite far into the millimetre-wave range.

9.2: Future Work

If anything, this thesis has uncovered more questions than it has answered. The potential for future work in the area of LTCC packages is enormous, and spans a wide range of research activities, such as:

- 1) Research into numerical methods to predict package resonances, especially those derived from leaky waves.
- 2) Research into transmission line theory, to build transmission lines that are resistant to unwanted effects, such as finite ground coplanar waveguide (FGCPW) to extend the bandwidth of the line by reducing side-to-side-width; slotlines, to use a balanced approach and laminated waveguides to take advantage of years of EM theory in this area.

- 3) Prototype LMCS/LMDS packages, investigating wire-bond effects, thermal problems, mixed analog-digital packages, and integrated antennas.
- 4) Novel 3D circuitry, such as filters, couplers, baluns, and other passive components that can be miniaturized with the use of the third dimension.
- 5) Other multi-layered package techniques such as MCM-D.
- 6) Research into the restrictions on LTCC packages, such as layer height, minimum conductor spacing, via diameters, different metallizations, and conductor width restrictions.

The research done in this thesis is but a small part in the investigation into the use of multi-layer circuitry. The discoveries made in this thesis are applicable to other multi-layered packaging techniques such as MCM-L and MCM-D, to future multi-level MMICs, and to flip-chip packaging methods. Being aware of the previously hidden danger of package radiation will aid in the development of further packages.

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