A Compact Electronic Dispersion Compensation Solution for 10Gb/s Optical Links

by

Matthew Hagman

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January 7, 2009

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Abstract

Electronic Dispersion Compensation (EDC) is an equalization technique used to correct for the transmission impairments of an optical signal in the electrical domain. In this work, an alternative to the traditional feed-forward/decision feedback equalizer (FFE/DFE) is analyzed at the system level, and implemented in an integrated circuit (IC) design. The target application is medium reach optical links at 10Gb/s employing non-return to zero (NRZ) modulation and direct detection. A unique infinite impulse response (IIR) filter is designed which exploits the properties of chromatic dispersion in order to approximate the behaviour of the commonly used FIR filter. Given the simplicity of this single delay element filter, a 10Gb/s EDC solution is presented which draws only 75mW in 0.13μm CMOS with an approximate 1.5mm x1mm chip real estate. Simulation results and field measurements on a 100km optical link show that the proposed filter offers comparable performance to a baud-spaced FFE/DFE approach at less than half the power dissipation and one third the chip length. This is a multi-disciplinary thesis, incorporating elements of adaptive filter theory, digital communications, circuit design and photonic components.

Acknowledgements

There are many people who have encouraged and supported me during my graduate studies. I would like to express my gratitude to Dr. Tadeusz Kwasniewski for his guidance and mentorship during my graduate studies at Carleton – especially for keeping me from re-inventing the wheel, which at times, I am wont to do.

I would also like to thank my friends at Bookham Inc. for their support and understanding during my two year hiatus in order to pursue graduate studies, especially Paul Davis, Michael Vitic and Sameer Chandani for letting me use the 10Gig optical link test equipment for my research. I also like to thank Andre van Schyndel, a pioneer in EDC and DSP, for giving me his time for detailed EDC discussions – this help was truly inspiring.

I would also like to thank my mother, Marilyn Marrone for always offering moral support and guidance during my studies. And also a special thanks to my father for explaining to me how a capacitor filters the low frequencies out of a tweeter, and why the "damping factor" in a woofer enclosure is important... all when I was 12 years old.

And finally, I'd like to dedicate this thesis to my fiancée Jodi for her love and support throughout the many late evening classes, and time spent locked up in my office reading papers and running simulations.

Statement of Intellectual Property

The information used in this thesis comes in part from the research program of Dr. Tad Kwasniewski and his associates in the VLSI Communications group. The research results appearing in this thesis represent an integral part of the ongoing research program. All research results in this thesis including tables, graphs and figures but excluding the narrative portions of the thesis are effectively incorporated into the research program and can be used by Dr. Kwasniewski and his associates for educational and research purposes, including publication in open literature with appropriate credits. The matters of intellectual property may be pursued cooperatively with Carleton University and Dr. Kwasniewski, where and when appropriate.

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List of Acronyms

ADC Analog to Digital Converter
AGC Automatic Gain Control
BER Bit Error Rate (or ratio)
BERT Bit Error Rate Tester
CDR Clock and Data Recovery
CML Current Mode Logic
CMOS Complementary Metal Oxide Semiconductor
DEMUX De-multiplexer
DFE Decision Feedback Equalizer
DML Directly Modulated Laser
EDC Electronic Dispersion Compensation
EML Electro-absorption modulated laser
FFE Feed-forward Equalizer
FIR Finite Impulse Response
IC Integrated Circuit
IIR Infinite Impulse Response
ISDN Integrated Services Digital Network
ISI Inter-symbol interference
MLSE Maximum Likelihood Sequence Estimation
MODEM Modulator-Demodulators
MUX Multiplexer
MZ Mach-Zehnder (modulator)
NRZ Non-return to zero
PCB Printed Circuit Board
PRBS Pseudo Random Bit Sequence
QPSK Quadrature Phase Shift Keying
SONET Synchronous Optical Network
TIA Trans-impedance amplifier
XFP 10Gb/s Small Form-factor Pluggable

1 Introduction

With the widespread acceptance of 10Gb/s fibre optic networks, systems providers are faced with a need to increase channel counts and replace legacy 2.5Gb/s links with faster, lower cost 10Gb/s links. As the cost pressure continues and the commoditization of optical transmitters and receivers becomes a reality, the recent developments in electronics has made electronic dispersion compensation (EDC) schemes attractive as a means of increasing the reach of 10Gb/s optical links. Since the 1990s, the primary methods for combating the impairments of fibre optic links was the use of dispersion compensating fibre and other optical methods such as distributed Bragg grating devices and optical FIR filters. These optical methods for impairment mitigation are costly – both in the financial sense as well as gain budget, power consumption and system equipment real estate perspectives. At present, the optical solutions for dealing with chromatic dispersion are inherently non-adaptive. As complementary metal oxide semiconductors (CMOS) technologies evolve, it is now possible to reverse optical impairments after the signal has been detected. This is known as post-detection equalization.

One of the challenges of post-detection equalization in fibre optics is the fact that the impairment is highly non-linear. This means that some of the equalizer architectures that were developed for modulators/demodulators (MODEMs), integrated services digital networks (ISDN), and serial backplane environments may not be well suited for optical impairments. Since this application is at 10Gb/s using 2-level non-return to zero (NRZ)

formats, it is interesting to draw a comparison with serial backplanes which operate at 6.4Gb/s up to 10Gb/s. In the backplane environment, equalizers are capable of recovering signals which have suffered 10 to 30dB of loss at just 5GHz. In a long distance optical link, the loss at 5GHz may only be 3 to 6dB. However, there are spectral nulls that appear in the useful band. These are caused by the combination of chromatic dispersion and square-law photo-detection.

1.1 Scope of this Thesis

Given that fibre optic communications is a very broad topic, it was essential to focus on one particular type of optical link. EDC has the potential to be used in many areas of telecommunications. From the initial research work, and some key observations from the Optical Fiber Conference (OFC) in 2007 [1, 2, 3], it became apparent early on that long haul networks tend to use very sophisticated optical techniques such as optical quadrature phase shift keying (QPSK), coherent detection, and highly sophisticated MLSE coding. For this research, the best place on which to focus is the 10Gb/s direct detection links usually used in the metro arena where fibre lengths are typically between 40 and 120km. An optical network diagram is shown in Figure 1.1. The circled area indicates where this research is directed.

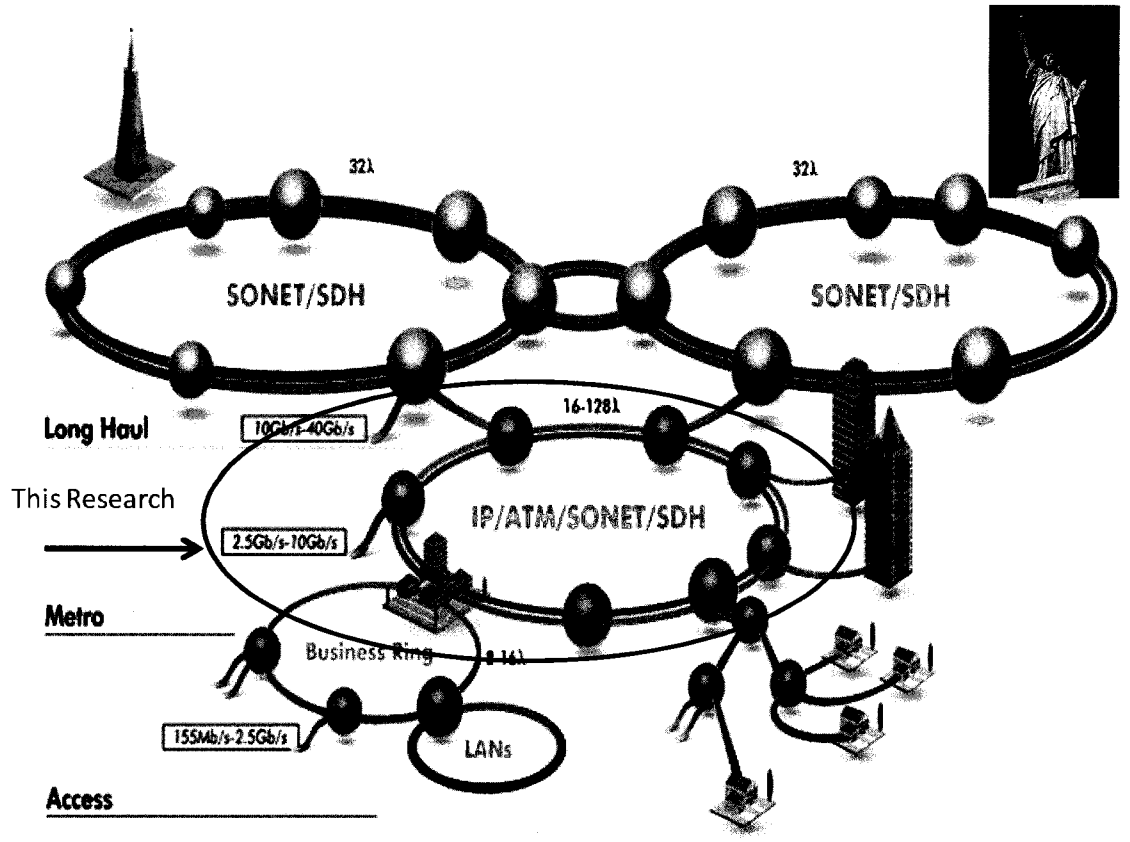

Figure 1.1: Optical Network Diagram[1]

Another important detail regarding the scope of this work is the type of physical hardware in which this EDC solution will fit. As metro links use NRZ data and direct detection, there are two popular small form-factor standards for these 10Gb/s optical modules. The industry standard 300-pin transponder has an optical transmitter and receiver as well as the pre-amplification and multiplexing/demultiplexing (MUX/DEMUX) circuitry. This is shown in Figure 1.2. The 10Gb/s small form factor

[1] Taken from customer training materials, Nortel Networks, November 2002.

pluggable (XFP) standard is a serial in/serial out device which is much smaller, typically lower reach, and lower cost. An example of this module is shown in Figure 1.3. For integration into these modules, the integrated circuit (IC) has to be low power dissipation (<200mW) and must not use too much internal printed circuit board (PCB) real-estate. To date, a typical XFP module consumes between 1W and 1.5W, and the transponder module is generally less than 10W. These figures include all of the power consumers in the module such as the transmitter laser bias, TEC cooler (for wavelength locked devices), MUX/DEMUX ICs, receiver module, and control electronics.

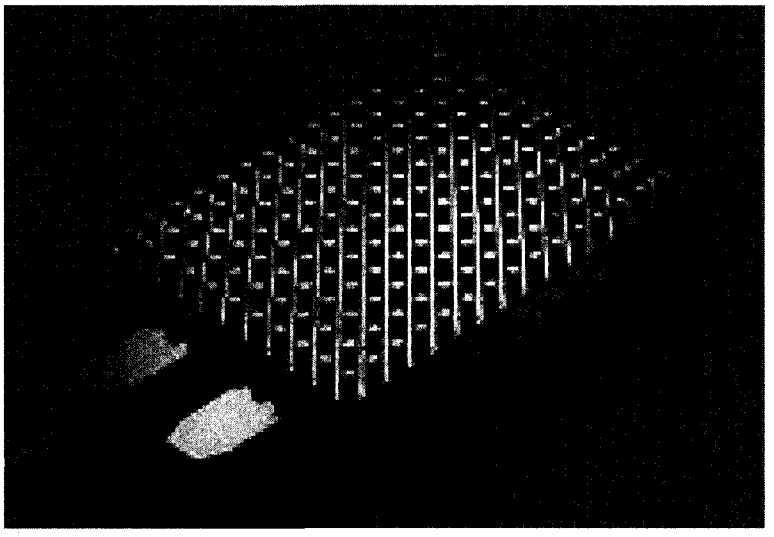

Figure 1.2: 300-pin 10Gb/s Transponder MSA[2]

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[2] Taken from internet promotional materials. NEC Corporation, http://www.eu.necel.com/products/optomodules/010_10g_300_PIN_msa_transponders/index.html, May 2008.

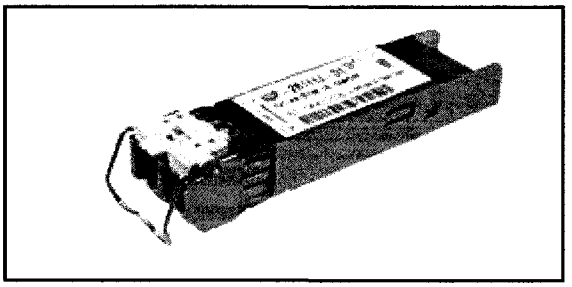

Figure 1.3: 10Gb/s XFP Transceiver[3]

1.2 Background on Metro-reach Optical Links

1.2.1 Modulation Techniques

For this specific metro optical network the only modulation technique used is on-off keying (OOK) and the NRZ format. This is necessary since the photo-diode in the receiver can only detect the intensity of the optical waveform [4]. The extinction ratio is defined as the ratio of the mean optical power in the "ones" level versus the mean optical power in the zeros level. Figure 1.4 shows the eye-diagram of a typical 10Gb/s optical signal where the extinction ratio is approximately 15:1 or 11.7dB.

[3] Taken from internet promotional materials. Bookham Inc,. http://www.bookham.com, May 2008

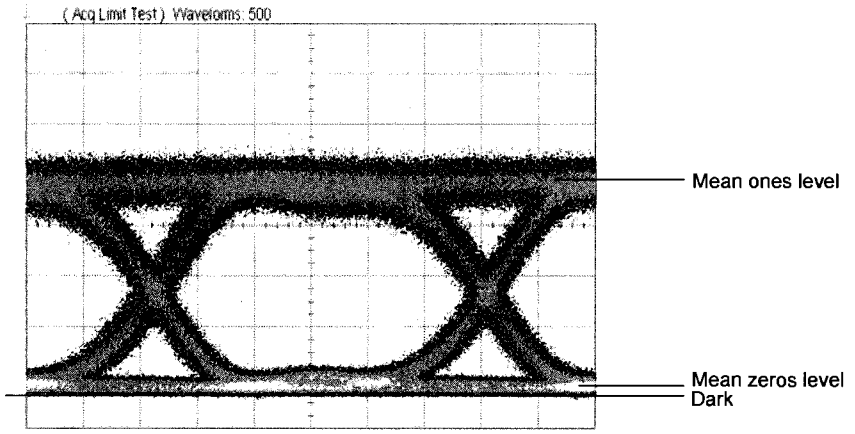

Figure 1.4: An eye-diagram showing a 10Gb/s optical signal

Other modulation techniques are generally reserved for long-haul and ultra long-haul links. Some examples are optical dual phase shift keying (DPSK) [5], dual-polarization quadrature phase shift keying (DP-QPSK) [6], OOK + return-to-zero (RZ), optical duo-binary [7], optical single-sideband [8], and others.

1.2.2 Transmitter Types

For this type of 10Gb/s metro link, the suitable optical transmitters are an electro-absorption modulated laser (EML) or a Mach-Zehnder (MZ) modulated laser. Both types of transmitters use a continuous wave Distributed Feedback (DFB) as the laser source. Some very short reach 10Gb/s modules use directly modulated laser (DML). However, DMLs have very limited reach due to their inherent adiabatic chirp characteristic. Adiabatic chirp causes the "ones" level to have a longer wavelength than the "zeros" level. For this reason, externally modulated sources are preferred for 10Gb/s as in the XFP, and 300-pin MSA transponder standards. By consulting the datasheets of

two top optical component suppliers (Bookham Inc. and Eudyna) and a valuable email exchange with an Engineer at Bookham Inc. [9], it was determined that the 10Gb/s EML transmitter will have slightly positive chirp, 10dB extinction ratio and 29ps rise/fall times. Additional electro-optical characteristics are given in Table 1-1. Later on, this data will be used for numerical simulations.

Parameter	**EML-Transmitter**	**MZ Transmitter (zero-chirp variant)**
Rise/Fall Time	29ps	25ps
Transient Chirp	$-0.2<\alpha<0.4$	$-0.2<\alpha<0.2$ $-4GHz<f_{chirp\ pk\text{-}pk}<4GHz$
Adiabatic Chirp	0GHz	0GHz
Extinction ratio	10dB	12dB
Uncompensated reach @ -2dB power penalty	70km	80km
Electrical drive requirements	2V peak-peak single ended	5V peak-peak differential (2.5V pk-pk on each arm)

Table 1-1: Transmitter performance data

1.3 State of the Art

Since chromatic dispersion is known to be the dominant source of inter-symbol interference in 10Gb/s uncompensated optical transmission, several papers have been published proposing solutions. In order to draw a fair comparison, the results presented here will be expressed as the fibre reach achieved with 2dB dispersion penalty. This is the industry accepted measure of dispersion tolerance.

Scintera™ introduced two 10Gb/s EDC solutions based on the feed-forward, decision feedback equalizer (FFE/DFE) architecture, one for single mode and one for multimode fibre links [10]. The single mode solution offers link extension up to 140km and it is fabricated in CMOS in the form of a 5mm by 5mm package. It consumes 700mW.

P. M. Watts [8], introduces three proposed schemes. Of these three, one is an FFE/DFE approach for intensity modulated/direct detection (IM/DD). Here, a 7-tap (T/2) FFE and 1-tap DFE filter gives a reach of 100km over single mode fibre.

Broadcom Semiconductor introduced an EDC solution with integrated clock and data recovery (CDR) and DEMUX for 10Gb/s optical links. The EDC offers a reach extension of up to 120km over single mode fibre. The IC was fabricated in 0.13μm CMOS, has a chip size of 15mm by 15mm, and consumes just under 1W.

Quake introduced an EDC chip with integrated CDR for 10Gb/s multimode [11] and single-mode [12] fibre links. The IC employs a 9-tap FFE and a 3-tap DFE filter. It was fabricated in 0.18μm SiGe BiCMOS technology and consumes 900mW in a 7mm by 7mm package.

In the work by Sven Otte [13], a modified DFE filter is designed. This example is of particular interest because it shows one of the few attempts to implement a second order filter where there are not only linear combinations of previous decisions, there are also second order terms: $Dd(k)d(k-1)+Ed(k)d(k-2)+Fd(k-1)d(k-2)$, etc where D, E and F are the non-linear decision feedback coefficients, and d(k) is the k^{th} decision. The schematic for this filter is shown in Figure 1.5. The linear filter coefficients are B and C, as one would find in a DFE with only single decision terms (d(k), d(k-1), d(k-2)...) The reported reach is 130km over single mode fibre. Given the flexible simulation set up, the author makes direct comparison with the standard first and second order DFE filters by simply setting coefficients F,D, and E (in Figure 1.5) to zero. The "squared equalizer" case offers a 1dB improvement over the standard two-tap DFE. Although this work is from 1999, it is frequently referenced in recent publications.

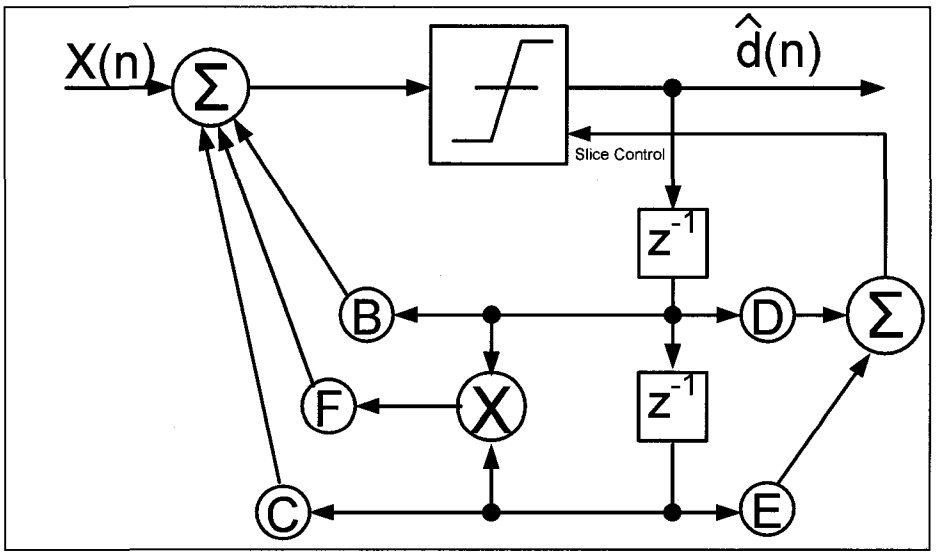

Figure 1.5: Model of the squared equalizer[4]

The work of Foster F. Dai et al. [14] discusses another half symbol period spaced, 7-tap FFE with 1-tap DFE. There is no discussion on reach extension, however, there are detailed eye diagrams showing significant reduction in inter-symbol interference (ISI) at 75km of single mode fibre. This paper is significant as there is a detailed discussion on blind adaptation of the FFE section using a decision directed approach and the sign-sign least mean squares (LMS) optimization method. Most references to date only treat blind adaptation of the DFE section. This EDC solution was implemented in 47GHz SiGe bipolar, featuring cascaded unity gain Cheery-Hooper amplifiers as the 50ps delay elements (circuit described in [15]). The fabricated IC draws 250mW and has an area of 1.2mm by 1.8mm.

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[4] "Squared DFE" Diagram similar to the one described in [13]

H. Wu et al. of IBM [16], designed and implemented a 7-tap half-baud-spaced FFE for 10Gb/s multimode fibre applications. It has been fabricated in 0.18μm SiGe BiCMOS with a chip area of 1.0mm by 2.5mm and a power dissipation of less than 45mW.

The work of S. Reynolds et al. of IBM [17] presents a 7-tap 75ps spaced FFE in 0.13μm CMOS for multi-mode fibre applications. The chip is 1.5mm x 4.8mm area and consumes 290mW.

1.3.1 Other EDC Solutions

There are many works which compare existing EDC techniques [10], [3], and [8]. As mentioned in the section defining the scope of this research, EDC solutions such as MLSE or fully digital FFE/DFE approaches have been ruled due to the significant power dissipation. It is worth mentioning that MLSE techniques are significantly more powerful in terms of reach extension. This is due to the fact that an MLSE filter is adaptive, non-linear, and it takes the sequence of several received bits and computes the likelihood of each possible transmitted bit sequences, selecting only the most likely one. One of the earliest 10.7Gb/s hardware implementations of MLSE was reported in [8]. This 4-state Viterbi equalizer was capable of extending the reach to 200km with a 5dB OSNR penalty.

Many papers on MLSE were researched [18, 19, 20 and others] to see if there was some available technique that was both powerful with low power dissipation. In [18], a

non-linear filter analysis using the Volterra series is discussed, resulting in a reach of 250km with only -3dB dispersion penalty. The work of Hyeon-Min Bae et al. [20] presents an MLSE solution in 0.18μm SiGe BiCMOS. This work describes a complete implementation and measurements showing error free performance at 2000ps/nm dispersion exceeding the SONET specifications for an OC-192 transponder application. The IC implementation consumes 4.5W. The most recent implementation of a 4-state Viterbi MLSD circuit [21] also consumes 4W. Given these high power dissipations, these solutions are deemed inappropriate for the XFP application.

The most impressive reported ultra-long haul EDC solution was reported by [6], where a reach of 3200km was achieved at 40Gb/s. This approach used a combination of transmitted pre-distortion, QPSK modulation and dual polarization modes. It is interesting to note that this method uses optical phase modulation, which preserves phase information in the detection scheme and thus increases the efficacy of linear finite impulse response (FIR) filters. This solution demonstrated by Nortel uses their proprietary ASIC for all of the transmit-side and receive-side DSP. Further technical detail on this technique will not be elaborated on here as it is outside of the scope of this research.

2 System Level Simulation of Optical Links

2.1 Method of Simulating Optical Links

The first step in EDC filter design is the development of a simulator in order to evaluate different filter approaches. The successful simulator needs to:

1. Generate a realistic transmitted optical signal waveform.
2. Apply the chromatic dispersion characteristic of SMF-28 in the wavelength range of 1525nm – 1605nm (C&L bands) taking into consideration the square-law and band-limiting effects of the photo-detector.
3. Model other important factors such as the frequency (or impulse) response of the trans-impedance amplifier.
4. Apply the FFE/DFE filter and adaptation algorithm.

In order to generate the transmitted waveform, it is important to determine how to model the transmitter. The other analysis tool that needed to be developed was a pseudo random bit sequence (PRBS) generator. An online source[5] was found which provided instructions for the generation of the standard PRBS bit streams. The code was entered into MATLAB to produce a 2^{11}-1 pattern. In future work, this will be increased to PRBS 2^{31}-1 as this is a more accurate spectral representation of 10Gb/s SONET data [22, 4].

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[5] Rob Lynch, Quinta Corporation, March 31, 1997

The next part of the development of this optical link simulator was the application of the distortion due to chromatic dispersion. Although chromatic dispersion is a particularly difficult impairment to equalize, it is quite accurately modelled mathematically. In an optical system, the transmitter carrier is 1550nm light, which has a frequency of 194THz. This carrier is intensity modulated and just like in AM radio, there are upper and lower sidebands. As the signal passes through the fibre, different wavelengths travel at different velocities. This is sometimes called group velocity variation. An expression for the wavelength dependent group velocity variation from [22] is given by:

$$\tau = \beta L(\lambda - \lambda_0) = -\beta L \frac{\lambda_0^2}{c}(f - f_0) \text{ for } f \approx f_0 \tag{1}$$

Where β is the dispersion constant of the fibre (typically 17ps/nm/km)

L is the fibre length (in km)

λ_0 is the centre wavelength (1550nm for this simulation) also represented in frequency by f_0. Given that the frequency of the light-wave carrier is extremely high compared to the modulation spectrum, a convenient representation of (1) is given by:

$$\tau = -\beta L \frac{\lambda_0^2}{2\pi c}(\omega - \omega_0) \tag{2}$$

Here, ω and ω_0 are the frequencies of the Fourier component of the transmitted signal, and the carrier frequency respectively. If a baseband representation[6] is considered, and making the appropriate change of variables $\omega - \omega_0 \Rightarrow \omega$ where ω is now the modulation frequency, the propagation through a dispersive medium can be expressed as a frequency dependant phase shift:

$$\phi = \frac{\omega^2 \beta L}{2} \tag{3}$$

Then, the baseband representation of the transmitted signal is given as:

$$E = A + Be^{-j(\omega t + \phi)} + B^{j(\omega t + \phi)} \tag{4}$$

Where A is the amplitude of the carrier and B is the amplitude of the sideband. After this optical signal is received via a square law detector, the resulting photocurrent is given by:

$$P_{received} \propto I_{ph} \propto |E|^2 = 2AB\cos\left(\frac{\omega^2 \beta L}{2}\right)\cos(\omega t) \tag{5}$$

Here it can be noted that there will be spectral nulls at $\omega^2 \beta L = (2n-1)\pi$. The nulls are due to the fact that one sideband has a shorter optical path than the other. The result is similar to comb-filtering except for the dependence on ω^2. A measured[7] frequency

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[6] This derivation approach is based on the method in [8]

[7] Measured at Bookham Inc. in Kanata, Ontario on March 15, 2007. Used with permission

response is given in Figure 2.1. This was taken using a Hewlett-Packard HP8703 light-wave component analyzer. The fibre length was 100km and the optical intensity modulation depth was approximately 15%. The first null appears at 5.8GHz which causes severe ISI when 10Gb/s NRZ data is sent down this length of fibre. This result helps to confirm the expression given in (5).

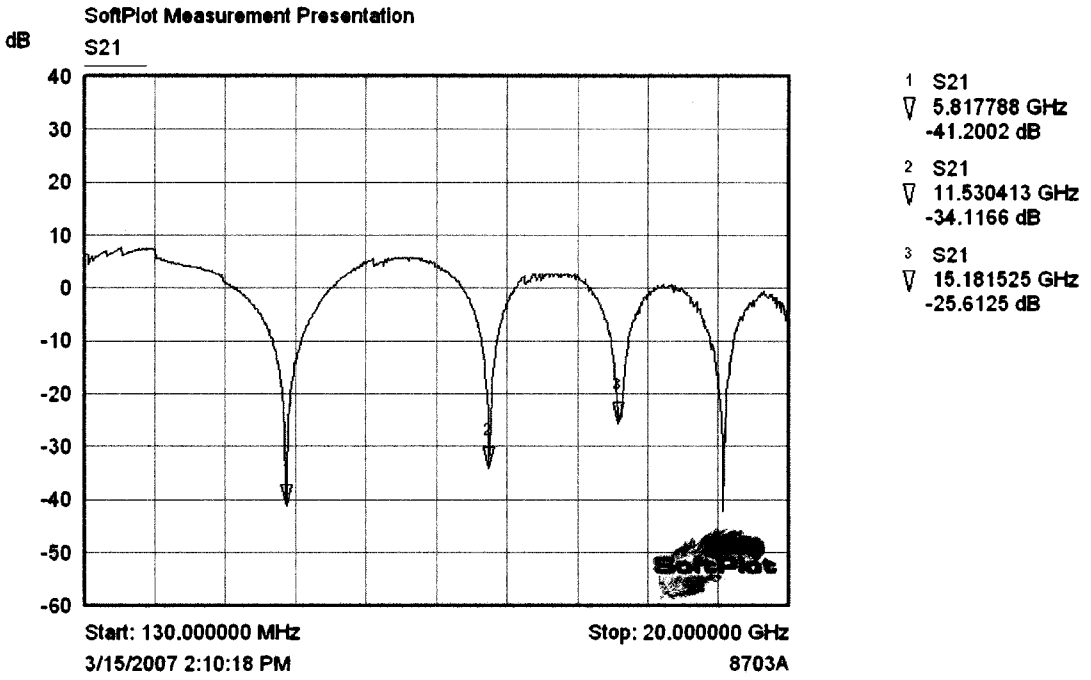

Figure 2.1: Frequency response of a modulated optical signal at 100km of fibre

2.2 Description of the Link Simulation in MATLAB

The MATLAB code in this research consisted of seven program files (or .m files) and explaining the details of each section is outside of the scope of this research[8]. The most important numerical calculations come from the application of chromatic dispersion to

[8] Some parts of the MATLAB code were developed at Bookham Technology, and these parts were used with permission.

an intensity modulated signal. The MATLAB program applies the dispersion equation to the transmitted waveform and stores it in another vector with units of milliwatts of optical intensity or milliamps of photocurrent. This is valid as most PIN photo-detectors have a conversion gain (responsivity) of 1A/W [4]. An oversampling of 40 samples per symbol period was used. The chromatic dispersion equations involve a fast-Fourier transform (FFT) of the transmitted signal, so that the chromatic dispersion can be easily applied in the frequency domain. The resulting distorted frequency domain signal is then brought back to the time domain by the inverse (IFFT) operation. The over-sampling greatly improves the accuracy of these operations. From trial and error, the minimum acceptable over-sampling was found to be 8 times.

The final step in the optical link simulation is the modeling of the photo-receiver. Many commercially available PIN based optical receivers for 10Gb/s operation have a bandwidth of 8GHz, and can be modeled as a 4^{th} order Bessel-Thompson filter. This has been verified by comparison with commercially available PIN receivers. An example is the PT10GC receiver from Bookham Technology which has a bandwidth of 8GHz and a gain of 1500mV/mW. It should be noted here, that for all EDC applications a linear optical receiver is required. There are several optical receivers on the market with an integrated limiting function. This type of receiver is not appropriate, and most vendors carry both linear and limiting versions. A pictorial model of the optical link simulator is shown in Figure 2.2 with some examples of the typical waveforms of each element. The signal shown at node "B" in Figure 2.2 is the unfiltered optical signal after 80km of single-mode optical fibre. The signal at node "C" is the point where amplifier input

referred noise is added for bit error ratio (BER) analyses. Node "D" shows the received signal where the pre-amplifier and photo-detector capacitance has applied a bandwidth limit of 7.5GHz. The eye appears opened in at "D" due to the fact that the noise bandwidth is reduced by the 7.5GHz Bessel filter, and the higher order effects of squaring the dispersed optical signal have been attenuated.

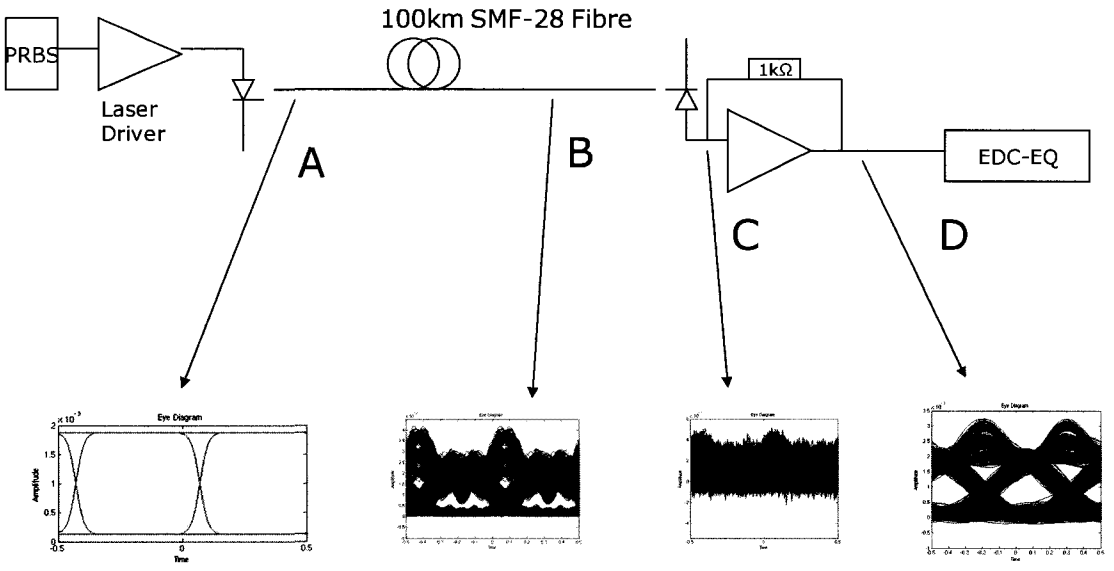

Figure 2.2: Pictorial representation of the simulated optical link

At this point, it is worth presenting some of the eye-diagrams of signals that have been distorted by chromatic dispersion. This will help the reader appreciate the unusual effects of square-law detection of a dispersed signal. The eye-diagrams in Figure 2.3

show the received signal after the low-pass filtering of the optical receiver has been applied. This filtering is important, and the un-filtered signal gives a closed eye due to the excessive high frequency content resulting from squaring a dispersed signal. The signals shown in Figure 2.3 will be referenced in later sections of this thesis. It is worth mentioning that there are numerical simulation packages from VPI™ which have built in models for chromatic dispersion, polarization mode dispersion, and other fibre optical link impairments. Distorted signals can be generated from VPI, and then imported into MATLAB to apply the FFE/DFE filters. An example of the MATLAB code developed in this research to apply FFE and DFE filters is given in Appendix D.

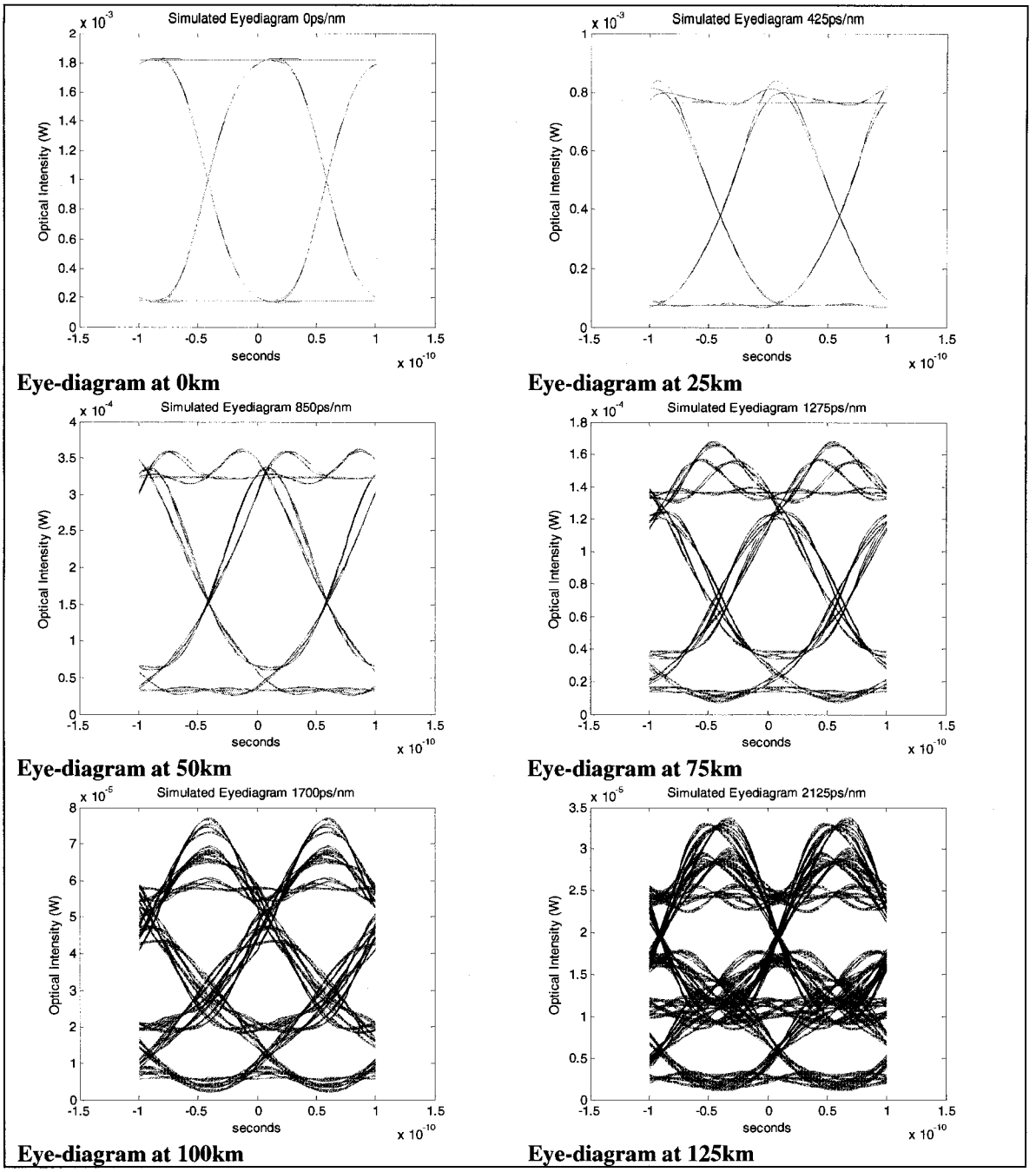

Figure 2.3: Optical eye-diagrams at various fibre distances simulated using MATLAB

2.3 Validation of Simulated Optical Signals

Given that a significant part of this research depends on the accuracy of numerical simulation, it is essential to include some simulated versus measured waveforms to prove

that the optical link simulator developed for this research is producing realistic results. Figure 2.4 shows the output of the simulator using a zero-chirped Mach-Zehnder transmitter, 100km of fibre, and a modelled PIN photodetector and transimpedance amplifier (TIA) based optical receiver. The image on the right of Figure 2.4 is the measured result[9] of the same scenario – using a Bookham™ "LMC10ZEG" zero-chirp Mach-Zehnder modulator, 100km of Corning™ single mode Fibre, and a Bookham™ PT10GC optical receiver. Since the receiver's frequency or impulse response has a significant effect on the simulation results, the frequency response phase and magnitude data for the PT10GC was used to improve the models in MATLAB. The result is clearly very good agreement from measured results to simulation.

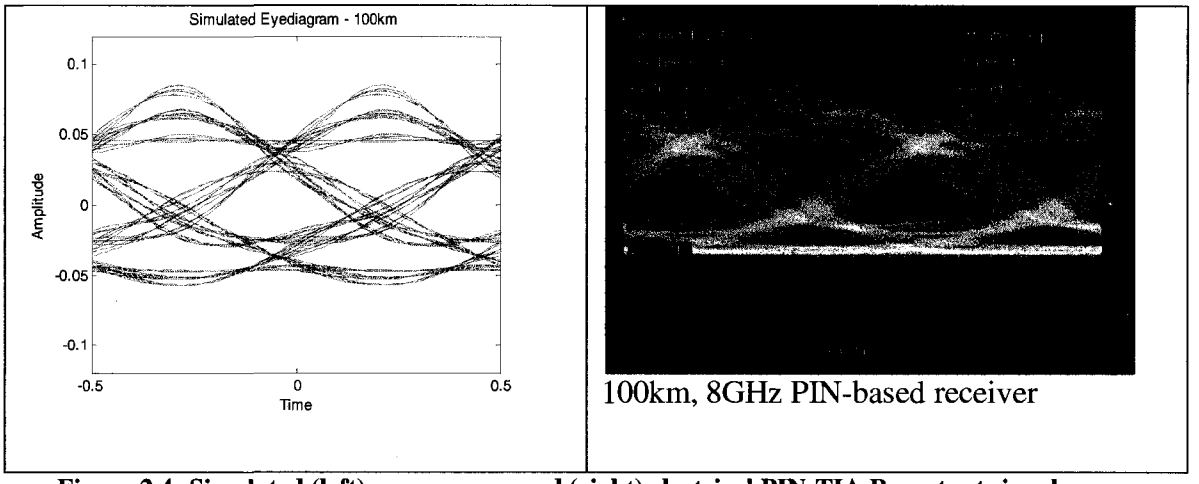

Figure 2.4: Simulated (left) versus measured (right) electrical PIN-TIA Rx output signal

Another validation of the simulation environment was carried out without any influence of the optical receiver. Figure 2.5 shows a simulated optical signal after 75km of fibre filtered by a 30GHz Bessel filter and displays it with the measured optical signal taken using a 30GHz optical scope module.

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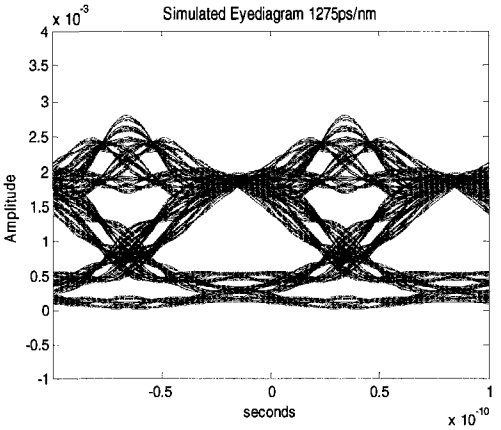
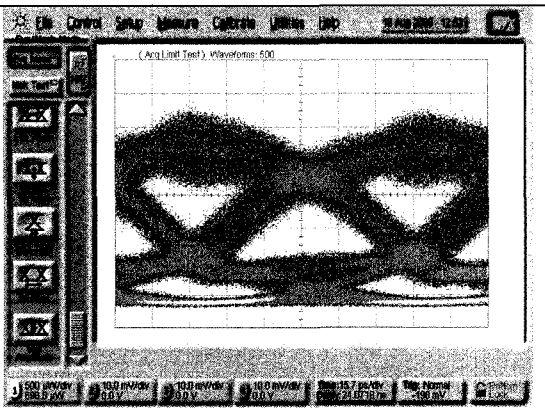
[9] Measurements taken at Bookham Inc. on August 7, 2008 in Kanata, Ontario. Used with permission.



Simulated 10Gb/s eye-diagram of 75km (1275ps/nm) of optical fibre



75km, 30GHz optical scope measurement

Figure 2.5: Simulated (left) versus measured (right) of an unfiltered, 75km, 10Gb/s optical signal

2.4 Notes on Applying Filters to Simulated Optical Signals

During the work with numerical simulations, several details were discovered which must be considered when working with the unusual effects of chromatic dispersion. For example, the ISI from chromatic dispersion has a high degree of temporal symmetry, meaning that the pre and post cursor ISI are virtual mirror images of one another. This has implications when applying the FFE. For example, if an FFE filter is 5-taps long, tap 3 needs to be set to the reference tap. This is achieved by applying the standard least mean squares (LMS) algorithm [23] with the desired signal delayed by 2 bits. Otherwise, the filter might converge to values of [1 -0.4 0.2 -0.1 0] instead of [0.2 -0.4 1 -0.4 0.2]. The latter case provides much better reduction in ISI.

2.4.1 Tuning FFE and DFE Filters using LMS

Although adaptation is not the focus of this research, it is essential to ensure that when a proposed filter is tuned via numerical simulation, that adaptation be performed correctly. The simulations presented here use the basic LMS or sign-sign LMS methods

to tune a filter and in all cases, the PRBS 2^{11}-1 pattern is used as the stimulus. At times, the pattern had to be repeated to ensure that the taps weights have fully converged. The easiest filter to tune from a convergence perspective is the baud period spaced equalizer. This is due to the fact that PRBS signal sources have a white power spectral density in the frequency range of $1/\tau_{pattern-length} < f < 1/2\tau_{baud-period}$ or, in the case of PRBS 2^{11}-1, between 4.885MHz and 5GHz. The result in this case is non-directional convergence which is the most rapid convergence trajectory for the LMS algorithm [23]. There is one challenge which comes with the baud-spaced equalizer, and that is the requirement for timing synchronization. In order for the LMS algorithm to be used effectively, there must be a reliable measure of error between the desired signal and the received signal. For numerical simulations, this means that some information is required regarding the mean edge position for the NRZ data stream. For practical purposes, this requires that the CDR be locked on the received signal such that the sampling point is close to the centre of the eye. Figure 2.6 shows an example of a 100km received optical signal with respect to sampling point and error signals.

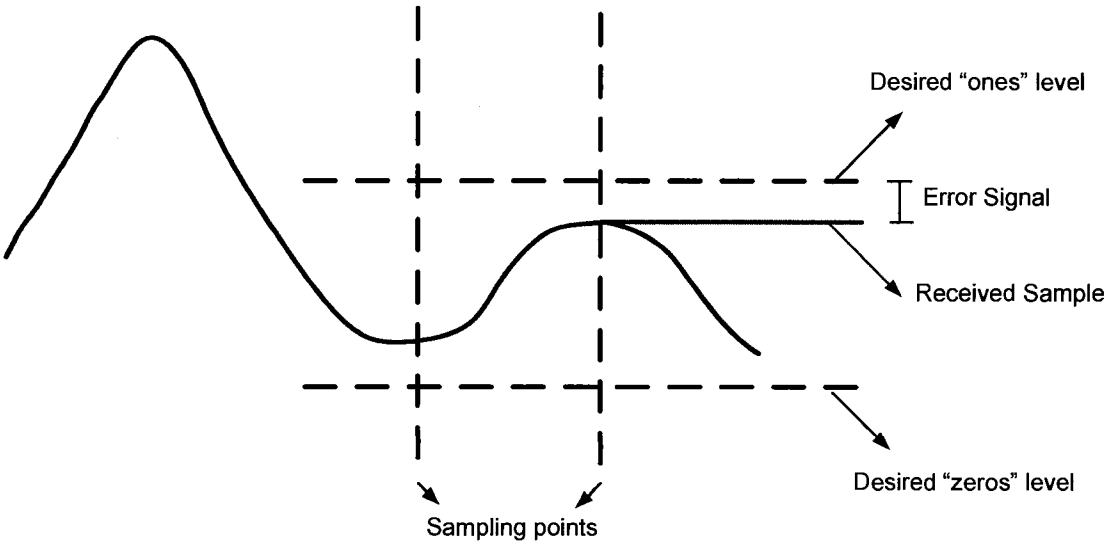


Figure 2.6: Diagram showing sampling points for LMS error estimation

During a numerical simulation, the received signal and the "desired" back to back signal is effectively down-sampled to the same sampling rate as the FFE. For example, in Figure 2.6, the receive signal shown is sampled at a rate of 40 samples per baud-period. However, only data from the sampling point is used to tune the FFE. This ensures that the filter is tuned such that the cost function is minimized when the eye is opened.

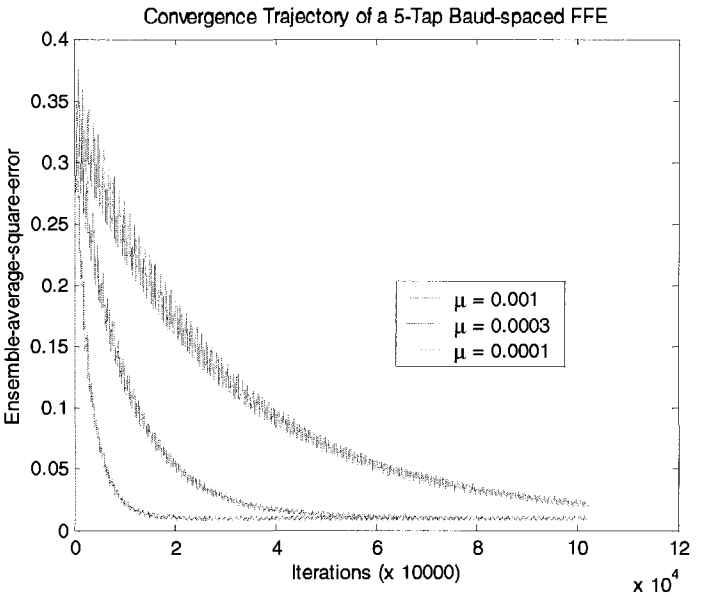


Figure 2.7: Convergence of the LMS for a 5-tap baud-spaced FFE

The next case that is considered is the fractionally spaced equalizer (FSE) where the tap spacing is at 50ps, or one half of the baud period. The sensitivity to timing synchronization discussed earlier is no longer quite as important. There are two new challenges which emerge. The first challenge is the fact that at every 50ps there is now some statistical correlation between each sample. This higher degree of correlation means that the convergence of taps weights is less reliable, and in some cases coefficient drift may occur [24]. The second challenge has to do with the treatment of error signals. If the reference clock from the CDR is used, it is possible to sample the signal at the centre of the eye and at the transitions. This reference clock from the CDR is reliable as the jitter at the input of the CDR is band-limited by the loop-bandwidth of the PLL. This is typically ~1MHz for a CDR designed to the SONET, 10G Ethernet and fibre-channel standards. If equal weight is given to both the eye-opening, and edge transitions (jitter

minimization) some interesting effects appear. For a reach of 115km over single mode fibre, Figure 2.8 shows the impact of changing the LMS tuning priority by weighting the transition errors and the eye opening errors. From this, it seems that in this non-linear system, vertical opening is traded off with horizontal opening. From a BER perspective, the vertical opening is more important as noise added to the amplitude of the signal experiences a much higher 7.5GHz bandwidth compared to noise added in the form of jitter. The topic of vertical eye opening versus horizontal eye opening is explored very closely in [25].

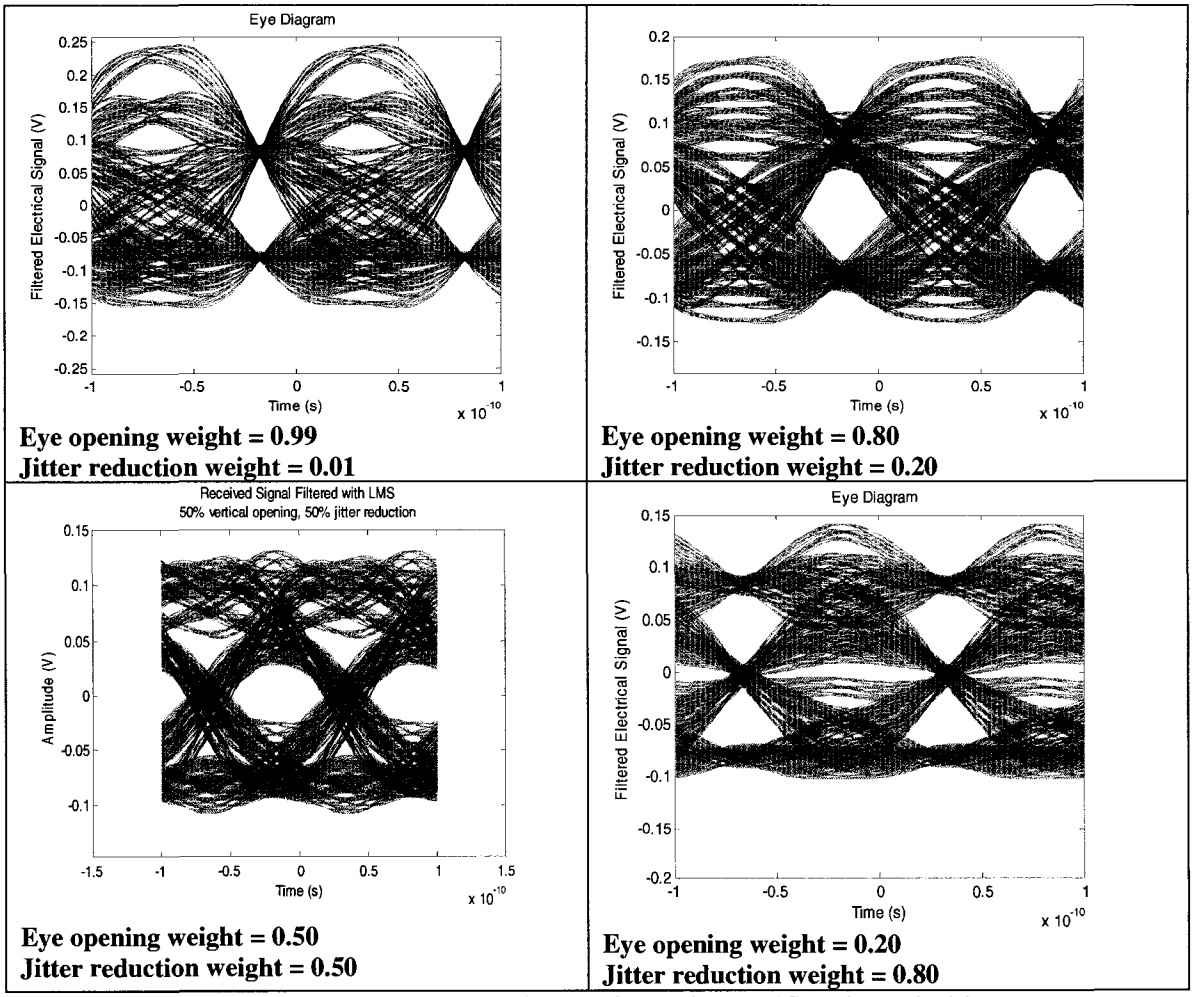


Figure 2.8: Half baud-spaced 9-tap FFE filters with various LMS tuning priorities

3 Design of a Suitable Filter

In this section, many of the approaches proposed in the literature are explored via numerical simulation. The purpose of this re-simulation is two-fold; the first goal is to prove relevance to this application and the second is to compare the merits of each filter design in a controlled environment.

3.1 Types of Feed-forward Equalizers

Throughout the last five years, there has been some ongoing debate about the performance differences between baud-spaced and fractionally spaced feed-forward equalizers. In section 1.3 the opinions from several sources found in the literature are stated. In this section, a direct comparison is made for the specific scope of this thesis: metro-reach optical links employing intensity modulation and direct detection.

3.1.1 Baud-spaced Feed-forward Equalizers

The obvious advantage favouring baud-spaced equalizers is the simplicity due to fewer taps for a given filter length. Another advantage of the baud-spaced equalizer illustrated in [24] is increased facility in coefficient adaptation due to the low correlation between received bits. It has been suggested that there are some implementation challenges. Since it is easy to show that baud-spaced equalizers are more sensitive to timing synchronization, it is not hard to demonstrate that variations as much as 20% can cause performance issues. The most popular implementation of the baud-spaced equalizer at 10Gb/s is the use of long inductor-capacitor ladders (LC-ladders) where the

taps are spaced every 100ps. With process variations as much as 20% on passive circuit elements, this invariably affects the effective tap spacing of the FFE filter. Using the simulation methods proposed in chapter 2, the received signal at 125km of optical fibre is shown in the last diagram in Figure 2.3. The equalized output signals are shown in Figure 3.1.

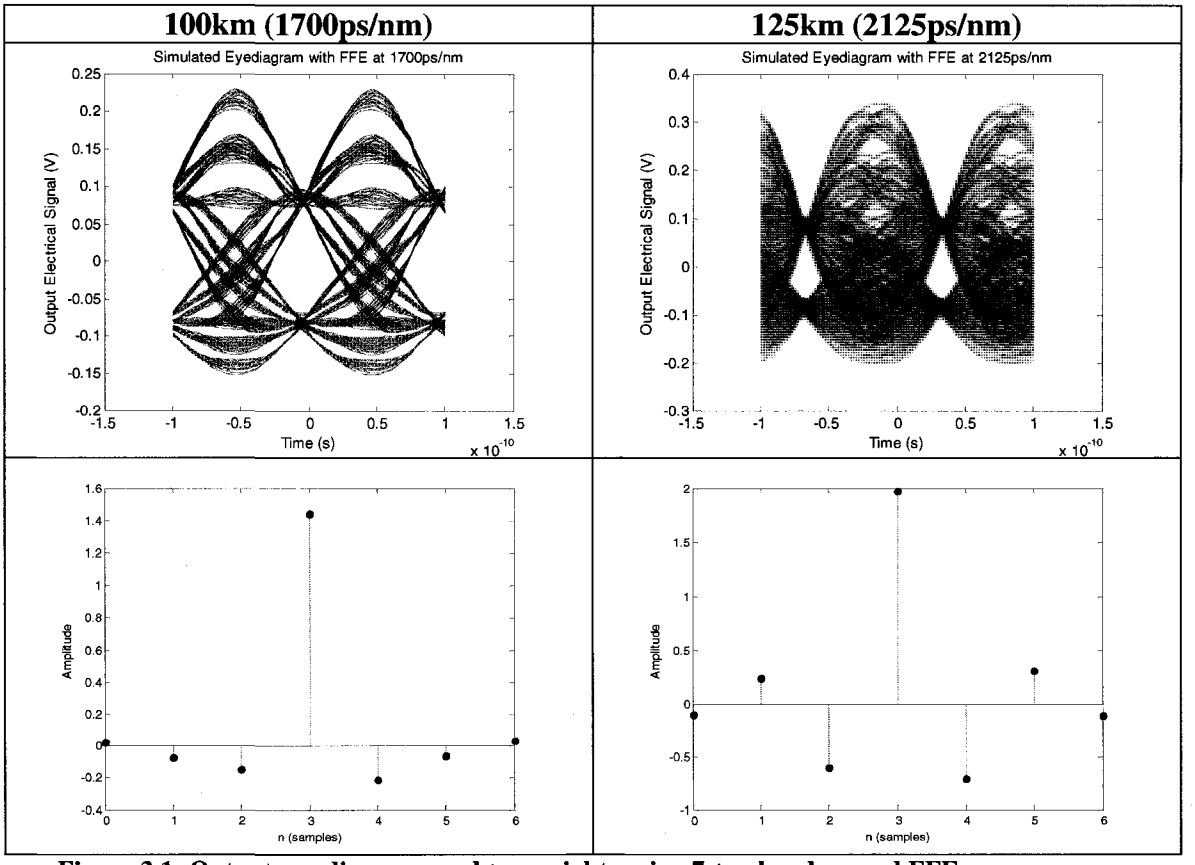


Figure 3.1: Output eye-diagrams and tap weights using 7-tap baud-spaced FFE

Apart from measuring the BER before and after an EDC filter, a good way to measure the performance of a linear filter is measure the eye-opening as a ratio with the average peak to peak signal. Provided the signal is sufficiently random, it has been shown that the vertical opening gives a good estimate of the power penalty due to ISI. Figure 3.2 shows the estimated dispersion penalty of baud-spaced FFEs of various lengths and it

suggests that the 5-tap equalizer is a good compromise between performance and complexity. Later, it will be clear that for practical reasons, shorter filters have performance advantages.

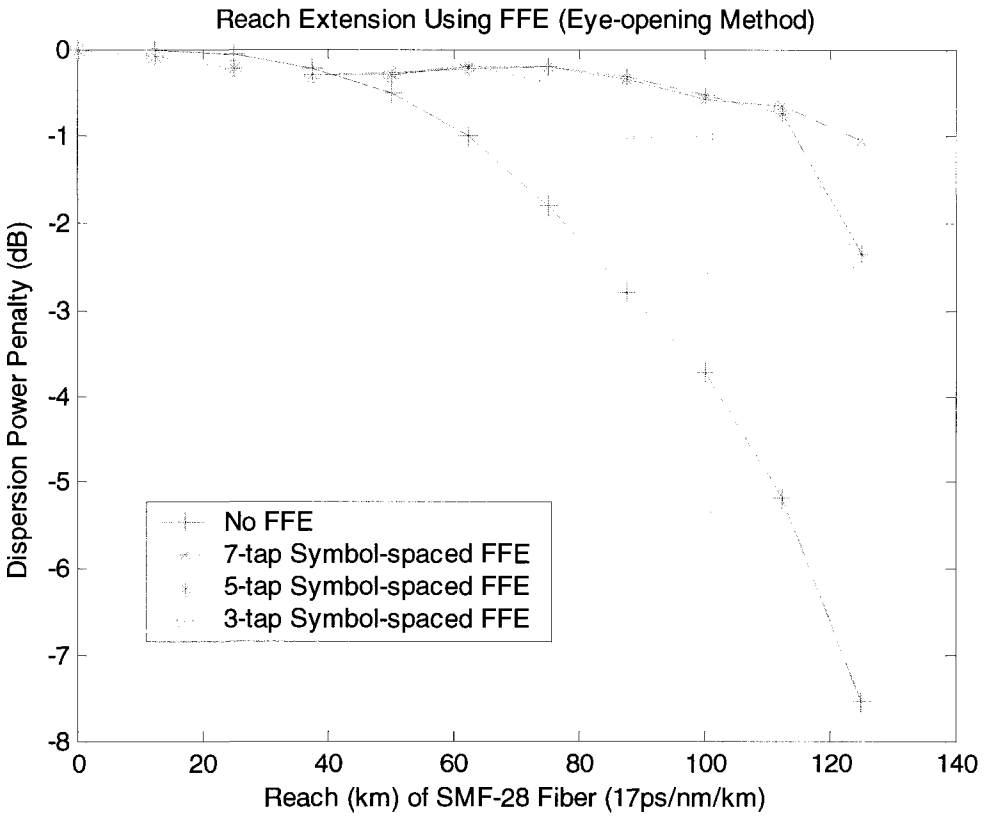


Figure 3.2: Simulated dispersion penalty of FFEs of various lengths

3.1.2 Noise Enhancement in Baud-spaced Feed-forward Equalizers

A well known issue in the feed-forward equalizer is the enhancement of noise. In links limited by chromatic dispersion, the frequency response shows attenuation in high frequencies, and even spectral nulls as seen earlier in Figure 2.1. An appropriately tuned FFE will attempt to counteract this effect by boosting the high frequencies. Since the noise is added after the dispersion, there is a component of noise that receives additional

gain. The amount of this noise enhancement is very easy to quantify by referring to the tap weights of an FFE filter. The resulting reduction in SNR of an N-tap filter is:

$$F_{ne} = \frac{\sum_{i=1}^{N} w_i}{\sqrt{\sum_{i=1}^{N} w_i^2}} \tag{6}$$

Where F_{ne} is the factor by which SNR is reduced, and w_i is the i-th tap weight. For the case of a 5-tap filter used to equalize 125km of fibre, the tap weights were found to be [0.15 -0.55 1.92 -0.65 0.21]. Using (6) this gives a loss of 0.51 or -3dB SNR. This effect is not included in Figure 3.2.

3.1.3 Fractionally-spaced Feed-forward Equalizers

Another class of feed-forward equalizers is the fractionally spaced FFE. In the literature there are many contradictory opinions regarding the performance enhancements involved in the use of fractionally-spaced equalizers. Intuitively, one might think that the fractionally-spaced equalizer offers equal or better performance when compared to the baud-spaced equalizer, especially since the fractionally spaced equalizer can always reduce to a baud-spaced one if the channel response so requires (ie. every other tap weight is set to ~0). The references focused on the back-plane channel [26-27] state that the fractionally spaced equalizer out performs the baud-spaced equalizer especially when jitter is considered. Several other works only discuss the baud-spaced equalizer as the only approach taken. In the papers by A. Carusone [24]

and [25] it is said that the fractionally-spaced equalizer may slightly out-perform the baud-spaced equalizer due to the fact that the filter serves as both the electronic dispersion compensation and the matched filter. It can also be shown that the higher resolution of the FSE is better at correcting for amplitude and phase response distortions if the optical receiver (PIN + TIA) has a less than ideal matched filter characteristic. In this work, the fractionally-spaced equalizer is considered with special attention being given to convergence and error measure during adaptation. However, as shown in section 2.3.1, the half baud-spaced equalizer offers only a slight improvement on the baud-spaced one which significantly more complicated convergence issues. For this reason, the baud-spaced filter is treated as the benchmark for this research.

3.2 DFE and FFE/DFE Filters

The popular Decision Feedback Equalizer (DFE) is often combined with the FFE. Only a few works mention the use of DFE on its own [13]. The main advantage of the DFE is the fact that it uses hard decisions on the sampled data and therefore does not suffer from the noise propagation issues discussed in section 3.1.2. A diagram from the DFE is given in Figure 3.3. Another benefit of the DFE is that, since the data is sampled, the delay can be achieved by the use of a simple D-latch or flip-flop. For practical purposes, this has a much simpler implementation as no analog delay elements are required.

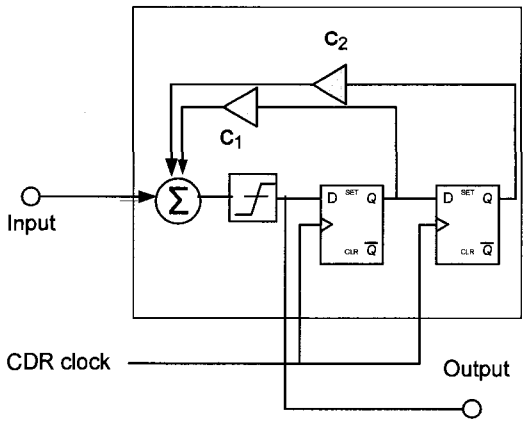


Figure 3.3: Functional block diagram of the DFE

One of the difficulties with the DFE is that fact that it can only treat post-cursor ISI. When combined with the FFE, this issue is reduced as the FFE equalizer can treat pre-cursor ISI provided that the reference tap is chosen in the middle of the filter. As it will be shown in a later section (Figure 3.9), the DFE on its own only achieves half of the electronic dispersion compensation than one that is paired with a suitable FFE. Several months of this research was dedicated to finding a variation on the DFE that will address pre-cursor interference. Accomplishing this means that the FFE section can be removed, which is valuable from the power consumption and chip real estate perspective as several references [15, 16, and 17] suggest that for this application a chip of between 3 to 5mm is required to achieve 500ps of total filter length. One approach that was considered during this work is shown in Figure 3.4. The element labelled "LC-ladder delay line" is simply a 100ps analog delay element, realized by an LC-ladder and appropriate signal buffering. This delay element feeds the "master" DFE. There is an un-delayed signal which comes from a second DFE used as a predictor. This is considered better than simply feeding forward an analog signal as it sampling an already opened eye. Another inherent simplicity in this design is the fact that there are only 2 "d" coefficients. This is

due to the temporal symmetry of the ISI due to chromatic dispersion. If this filter were used in multi-mode fibre, the 1-bit look ahead tap will need to be distinct as the temporal symmetry of SMF can no longer be exploited.

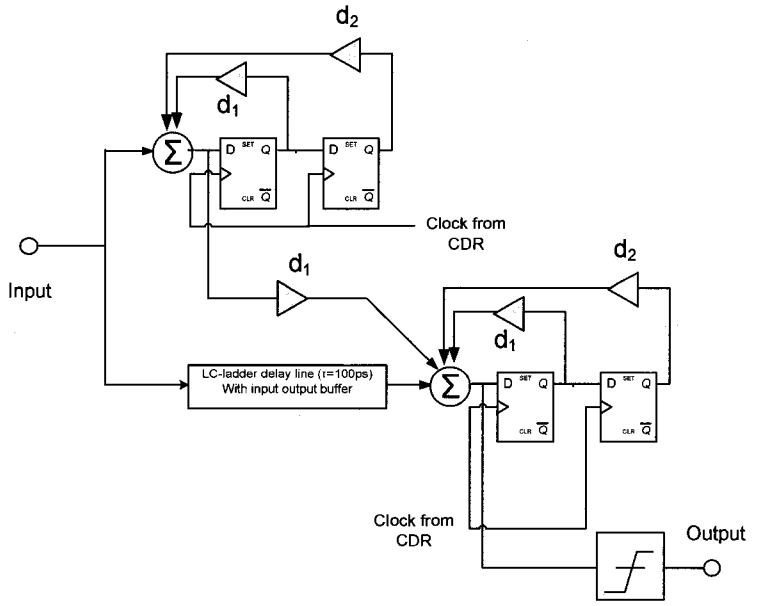
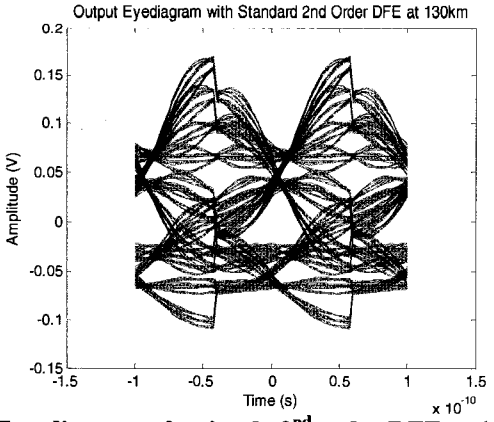


Figure 3.4: Functional block diagram of the 1-bit predictive DFE

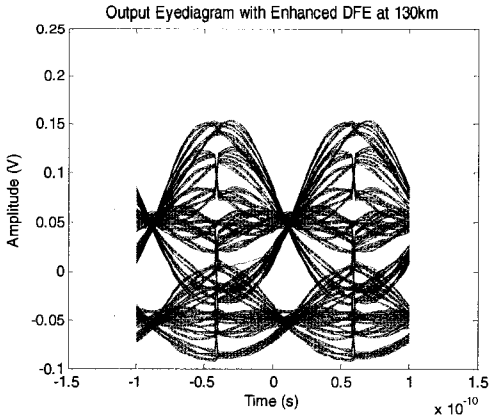
One complexity of comparing DFE equalizers comes from the fact that they are non-linear. This prevents one from using eye-diagrams or especially the measure of eye-opening as a performance metric. The problem with eye-opening analyses should be somewhat obvious – if any distorted signal is feed to a slicer, of course, the eye will be open. The received data might be incorrect. In order to properly analyze standard DFE filters and the proposed modified, 1-bit predictive DFE, an actual bit error ratio measurement is needed. This was carried out numerically by adding various levels of white Gaussian noise to the received signal, then applying the filter and measuring the bit error rate. The result of this work is shown later in Figure 3.9 where the conclusion is

that the 1-bit predictive DFE (called the digital 1-bit predictive) slightly out-performs the standard DFE and the 7-tap FFE and 2-tap DFE has the best overall BER performance.

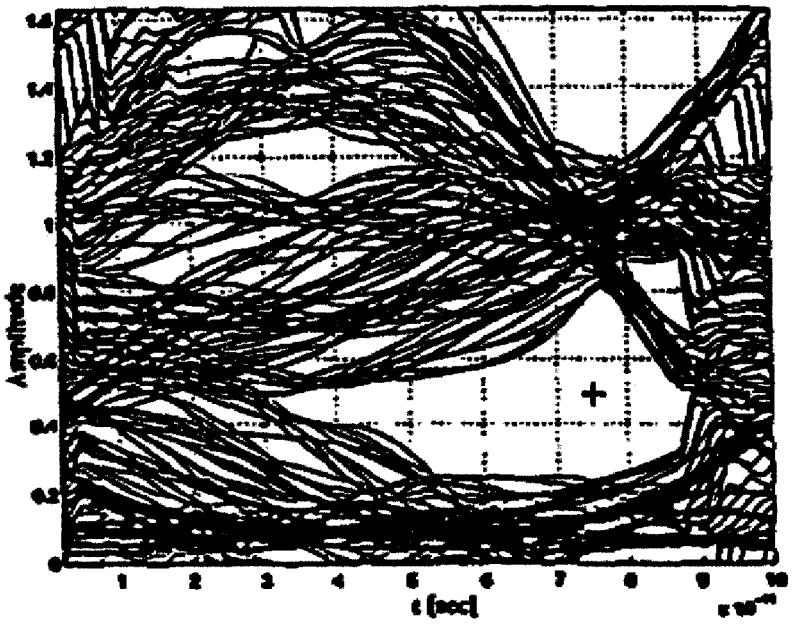
The eye-diagrams from the DFE filters discussed are given in Figure 3.5. One example is included from the early work of Sven Otte and Werner Rosenkranz [13]. This result shows very good agreement with the numerically simulated results from this research. The 1-bit predictive DFE developed in this research shows a much more symmetrical eye-diagram with almost 2dB better eye opening. The next section will describe another filter approach which offers better BER performance from 0 to 130km.



Eye-diagram of a simple 2nd order DFE at 130km



Eye-opening of a novel predictive DFE filter with 1-bit look ahead



Simulated eye opening plot taken from [13] after 130km using a 2nd order DFE

Figure 3.5: Various eye diagrams of decision feedback equalizers

3.3 IIR Filters – Interesting Observations

Apart from the characteristic of temporal symmetry observed in the tap weights resulting from a well-tuned FFE filter, there were also some other features observed. These additional features are:

1. Alternating sign starting from the reference (centre) tap

2. Decreasing tap weight for taps further from the reference tap.

These observations imply that one side of the impulse response of the FFE could be expressed as $1/w_{fb}^{i}$ and approximated with an infinite impulse response (IIR) filter where w_{fb} is one feedback tap. The only remaining issue is similar to what was observed with the DFE filter, and that is the treatment of pre-cursor ISI. One idea might be to handle this by one or more feed-forward taps. For example, a 5-tap FFE filter used in any single mode fibre, direct-detection system could be approximated by an IIR filter of the form:

$$H(z)=\frac{1-c_{ff}z^{-1}}{1-c_{fb}z^{-1}} \tag{7}$$

Where c_{ff} and c_{fb} are the filter coefficients for the feed-forward and feed-back terms respectively .This filter has the benefit of achieving similar ISI cancelation with only one delay element.

A proposed filter design is shown in Figure 3.6. More pre-cursor ISI cancellation may be achieved by adding additional feed-forward sections but in this work, the case of 1-tap fed-forward is explored in depth. Some numerical simulations were performed to show the performance comparison between the case of 100 and 125km. The output eye-diagrams and stem plots of the filter are given in Figure 3.7 and Figure 3.8 respectively.

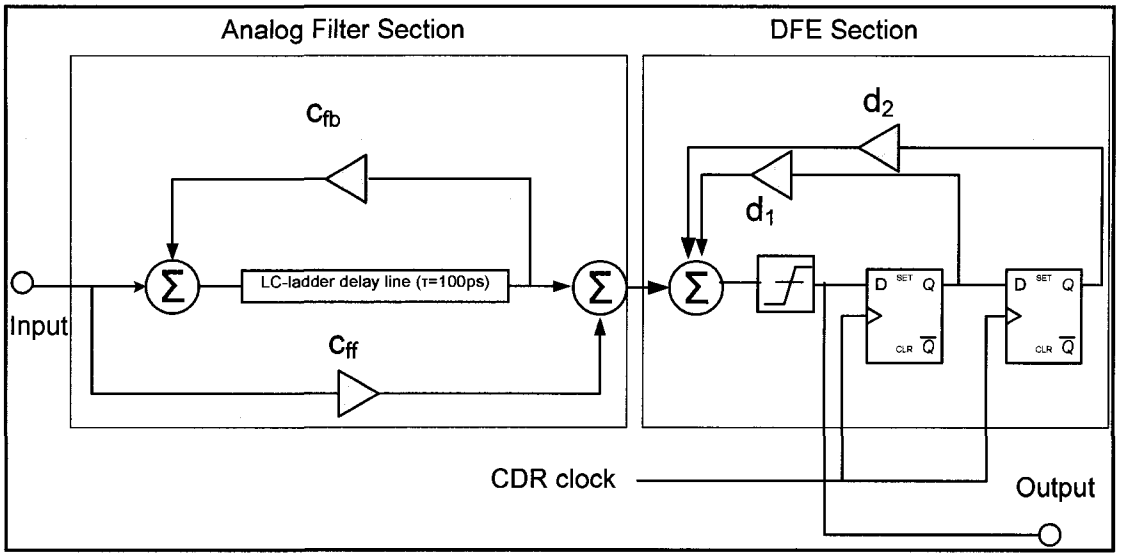


Figure 3.6: Diagram of the Proposed EDC Filter

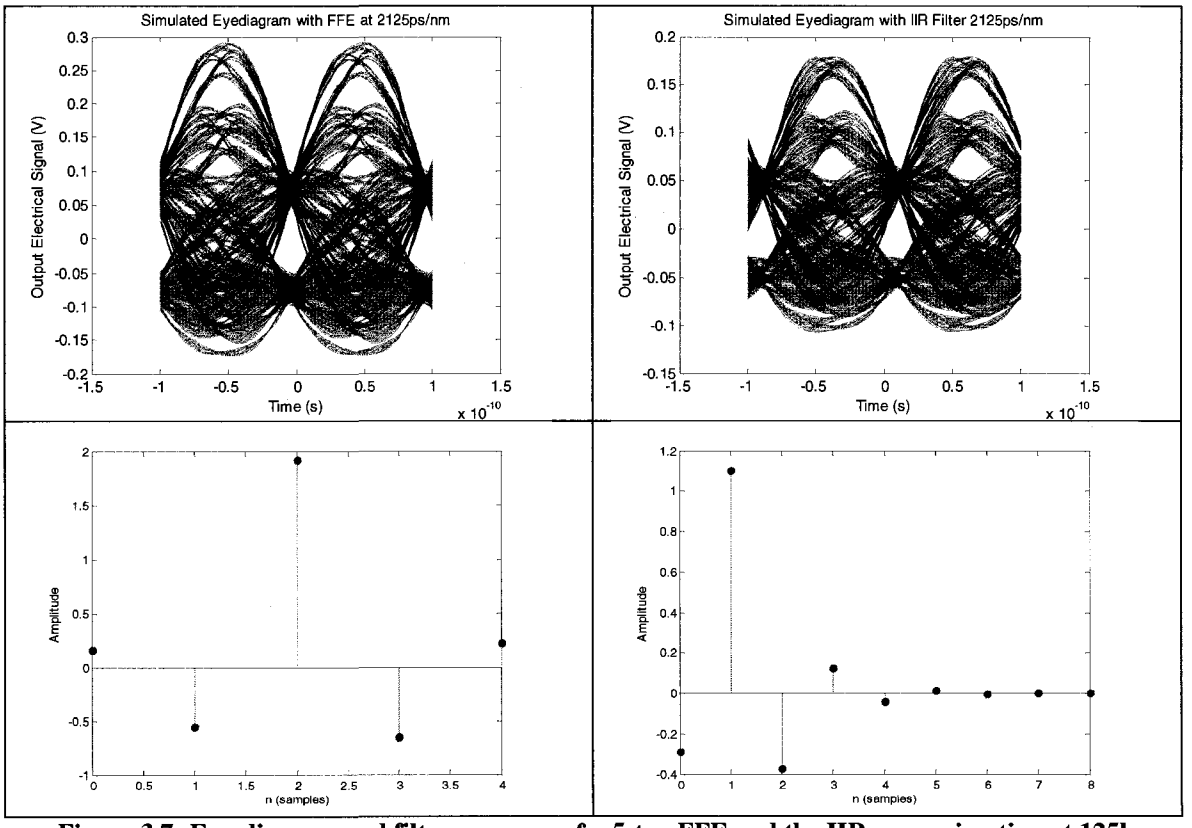


Figure 3.7: Eye-diagram and filter response of a 5-tap FFE and the IIR approximation at 125km

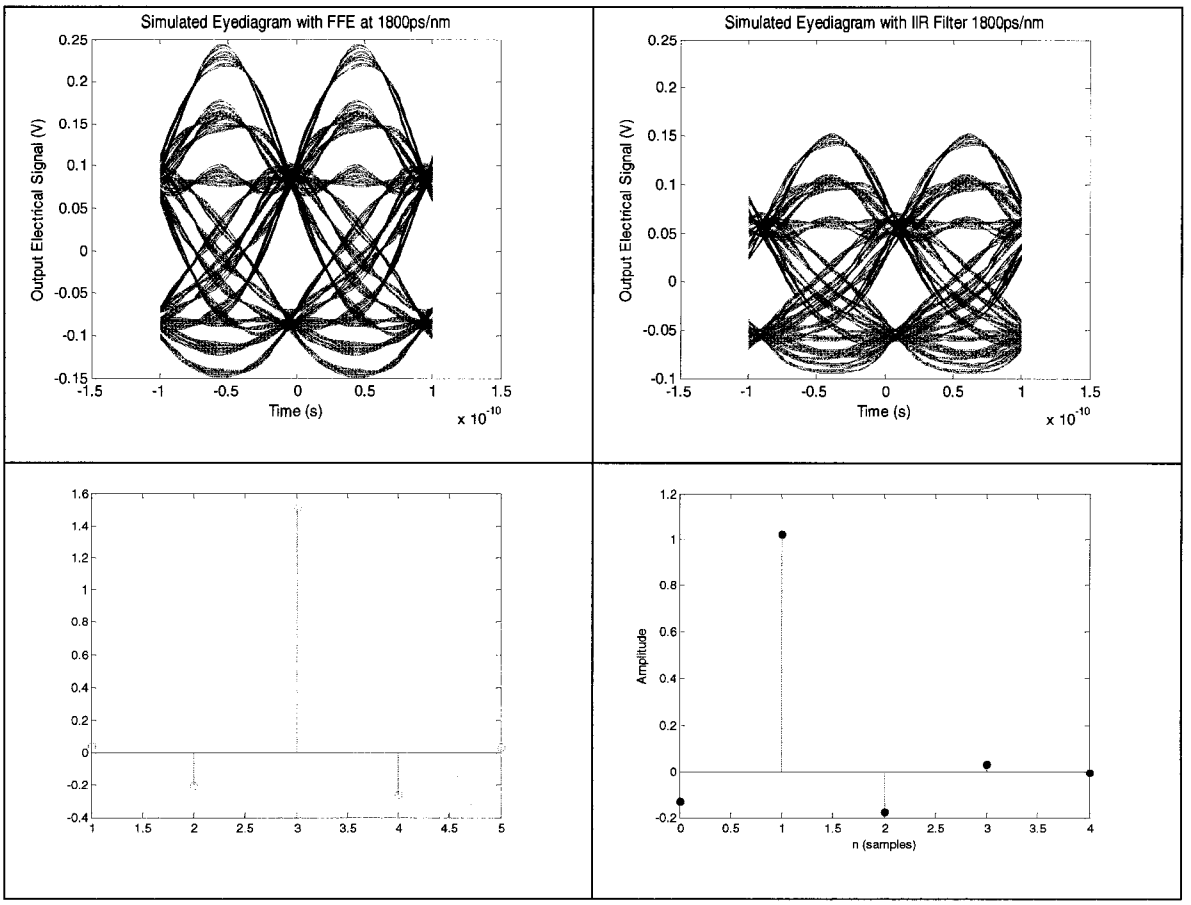


Figure 3.8: Comparison of the 5-tap FFE and the IIR approximation at 100km

As will be shown later, the practical consequences of reducing the number of taps and the delay line are significant. For this reason, the new "compact EDC solution" will be the focus of this research. In the next chapter, there is a BER analysis of the most significant filters reviewed in this research, and it is shown that this new approach gives comparable performance to the 7-tap FFE + 2-tap DFE equalizer.

3.4 Comparison of the Proposed Filter with Traditional Approaches

In order to conclude the survey of EDC filter topologies, a bit-error rate analysis was performed on the top two EDC solutions found in literature, and the two developed during this research. This noise analysis used some of the noise and sensitivity performance data on a commercially available 10Gb/s PIN optical receiver. The PT10GC receiver from Bookham has an input referred noise current of $15\,{}^{pA}/_{\sqrt{Hz}}$ and an input sensitivity of -18.5dBm with BER = 10^{-12}, measured with an ideal reference input signal at 10dB extinction ratio. This information and a sensitivity waterfall curve were used to develop a complete receiver model in MATLAB. Waveforms generated earlier were used and the appropriately scaled white Gaussian noise was added just before applying the EDC filter under test. This lengthy simulation takes approximately 4 hours to give a "waterfall" curve up to a BER = 10^{-9}. The addition of noise is the only proper way to carry out a BER analysis of a filter incorporating any form of DFE. This is to include the error propagation effects of incorrect decisions being made at the slicer. The output from this experiment is shown in Figure 3.9. Instead of white noise, coloured noise may also be used in the analysis. Some effort was made to add the effects of 1/f noise to the receiver model, however, very little difference in BER was observed. This is likely due to the fact that the PRBS signal as very little spectral content below 1MHz.

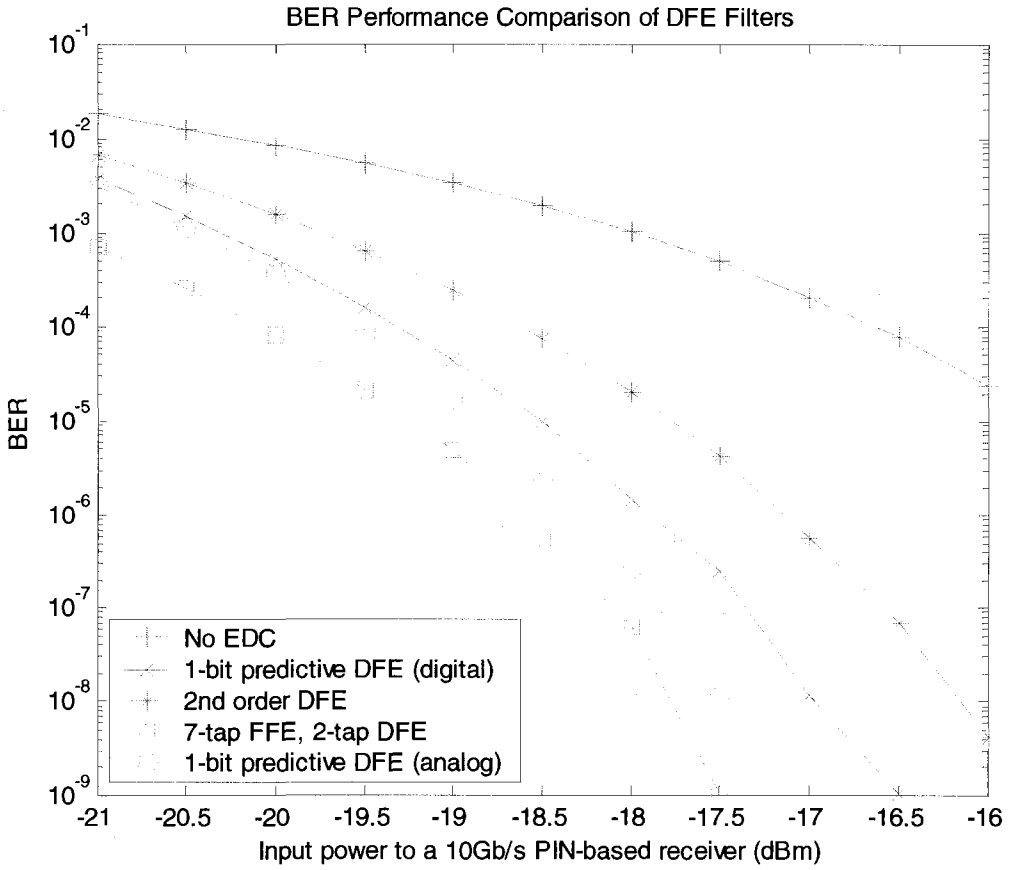


Figure 3.9: Bit rate performance of several filters at 130km

One of the conclusions from this simulation is that the traditional DFE needs to be coupled with an appropriate FFE section in order to compensate for the pre-cursor ISI. Given temporal symmetry, it is not surprising to observe that DFE on its own only offers half the EDC compensation as an FFE/DFE approach. The digital implementation of the 1-bit predictive DFE developed in this research offers some improvement. However, it suffers from the error-propagation effects of potential incorrect decisions being made at the slicer. The analog 1-bit predictive filter is the preferred approach as this filter may replace the FFE section of the traditional FFE/DFE technique as it offers both pre-cursor cancellation and the high-frequency boosted needed before slicing the signal. In the

numerical simulation environment, the traditional 7-tap FFE, 2-tap DFE appears to offer another 0.5dB improvement in BER performance compared to the equalizer proposed here. This advantage may disappear due to the practical difficulties of implementing a 600ps filter. As reported in [17], tap #6 had a -3dB bandwidth of only 4GHz. In the design section of this work, a total bandwidth of 10GHz is achieved in the entire filter.

4 Design of the 10Gb/s EDC Solution in 0.13μm CMOS

The first step in designing the filter shown in Figure 3.6 is the delay section. This has been cited by many references as being the single most challenging aspect of designing any continuous time FIR or IIR filter. An exhaustive search was carried out in order to determine the most appropriate method for introducing 100ps of delay to a 10Gb/s NRZ electrical signal. The most basic means of delaying a signal is the use of a long transmission line. The disadvantage of this approach is the physical size of such an element. In this application, a 100ps delay is required. If this were implemented by using a 50Ω transmission on a PCB with an effective dielectric constant of ε_r=3.3, the length of this element will be 16.5mm. Another approach is the "synthetic transmission line" or LC-ladder. This is very popular approach and it gives a significant reduction in length. The length reduction is often traded off bandwidth and signal quality as the size of each LC-element is adjusted. One of the earliest means of delaying a signal is the "charge bucket brigade" [28]. This method is fundamentally limited by the switching devices used in the sample and hold amplifiers to charge and discharge capacitors with each sample of the signal. The fastest reported bucket brigade was only capable of 400 MHz of bandwidth. Another method of achieving delay is digitizing the signal and storing samples in memory. With current CMOS electronics, this has been achieved with a 5-bit resolution and a sampling rate of 20GSa/s. The disadvantage of the all-digital approach to EDC is the power consumption required by the high-speed ADCs, DACs and memory/storage cells. A 10GSa/s ADC has been reported in [29]. It was designed in 0.18μm SiGe BiCMOS with a power dissipation of 3.6W. For this work, the

LC-ladder was selected as it offers the best compromise between signal quality, physical size, and power dissipation.

Later in the design process, it quickly becomes clear that aggregate bandwidth is a challenge in this filter design. Even with all tap weights set to zero, the received signal will pass through 2 summing nodes and 1 delay element before making its way to the slicer or DFE section. The first goal is to keep a bandwidth of 15GHz for all three sections to ensure that the total bandwidth is greater than 10GHz for the entire filter. This implies that the response of each element at 10GHz should be -1dB or better.

4.1 Design of the delay element

4.1.1 Theory of LC-ladder delay lines

A diagrammatic example of the LC-ladder delay line is shown in Figure 4.1. The characteristic impedance of this line is given by:

$$Z_{char} = \sqrt{\frac{L}{C}} \tag{8}$$

And the delay of each section is:

$$\tau = \sqrt{LC} \tag{9}$$

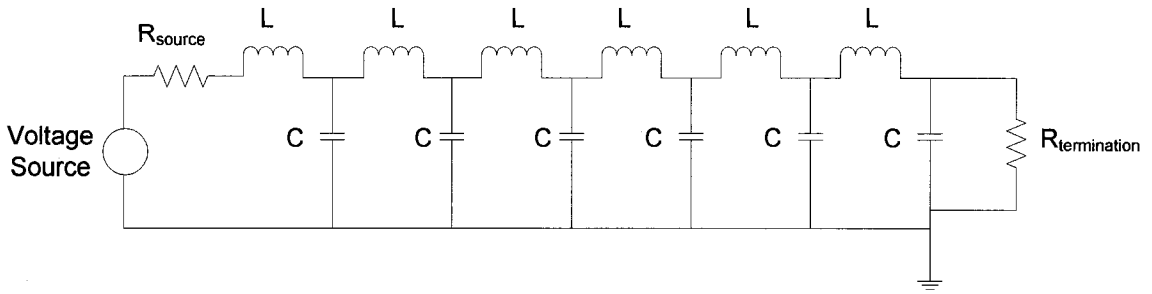


Figure 4.1: LC-ladder delay line

One of the most important design choices is the number of sections. If one assumes ideal L and C components (certainly not a safe assumption) there is a minimum number of elements required to have sufficient bandwidth for the application. With matched input and output terminations, the LC-ladder can be considered as analogous to a Butterworth filter. The minimum number of LC sections suggested by the derivation in [24] is given by:

$$M \geq \frac{W\tau_{total}}{\pi} \tag{10}$$

Where "W" is the bandwidth, τ_{total} is the total delay. With the design goal of 15GHz bandwidth for the delay section, this suggests that only a one section delay line is needed. Later, it becomes evident that more LC sections are needed to overcome the losses and effects of self-resonance in the inductors. For comparison purposes, a 6-section LC-ladder with ideal inductors, capacitors and termination resistors was simulated. This gives the theoretical limit for bandwidth (23GHz in this case) for this length of filter.

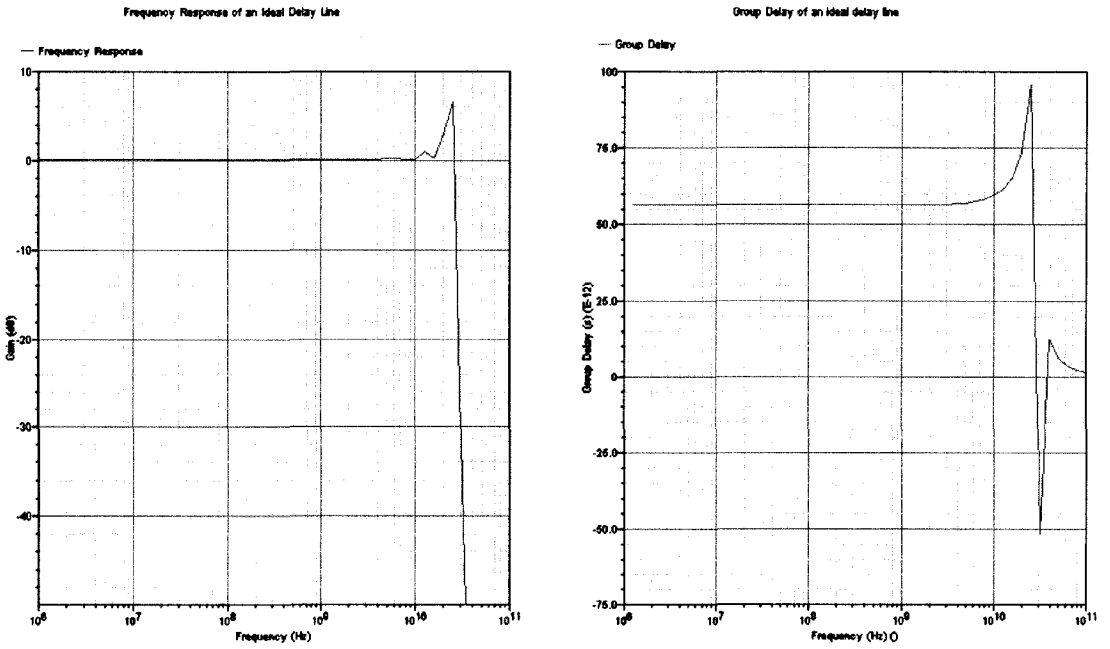


Figure 4.2: Frequency response and group delay of an ideal LC-ladder

4.1.2 Delay Element in 0.13μm CMOS

Before choosing the number of LC-sections, some important considerations had to be made regarding the much needed impedance matching at the input and output of the transmission line. Since the characteristic impedance will be relatively low (50Ω - 100Ω) there will be some form of buffer needed at the input to in order to minimize the load on the summing node. A brute force approach to this problem would be to use a low impedance environment for all three nodes in this filter. This is not a good idea since the power dissipation will be high. Instead, the low impedance environment is reserved in the delay line where it is needed. A few types of unity gain voltage buffers were considered for this design. A novel approach found in [30] was attempted in 0.13μm CMOS. The circuit diagram is shown in Figure 4.3. This follower had excellent linearity and gave a bandwidth of 18GHz with very little optimization. However,

simulations results confirmed that this buffer would not work well in this application as the output impedance was unpredictable and highly frequency dependent. The other issue is that this circuit works only with the simple feedback shown and thus, if matched to 50Ω, a -6dB loss of signal will result.

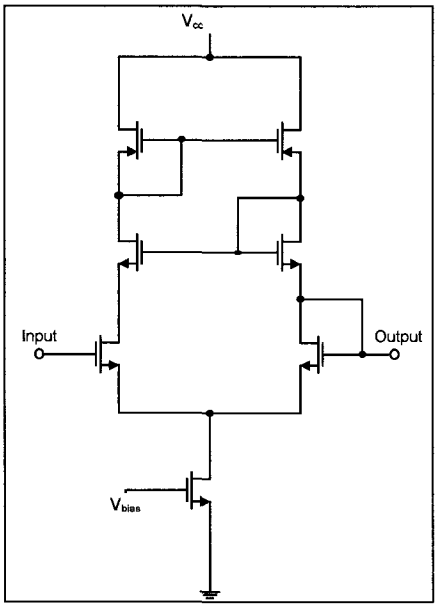


Figure 4.3: Unity gain amplifier[10]

Another type of unity gain buffer is the source-follower. There are two ways to design a source-follower such that it has a 50Ω output impedance. The first way it to make the follower with a high (W/L) and bias it with sufficient current so that the g_m is large. Since the output impedance is low ($1/g_m$) a series resistor can be added to ensure a good 50Ω match. Unfortunately, for this application, this transistor would have to have a gate width greater than 300um with a bias of tens of mA, and a series resistor of ~35Ω.

[10] Circuit suggested in [30]

Another means of reaching a 50Ω match was attempted by reducing the transistor size until the g_m is 20mA/mV (1/50Ω). This also did not meet the performance requirements because of the dependence of output impedance on frequency, and the -6dB loss. The only remaining options were the common-source amplifier or the current mode logic (CML) stage. The CML stage was chosen as it has two fundamental advantages – higher linearity, especially in the even-order terms and better power supply and common-mode rejection given that the input signal will come from a differential summing node. The final delay circuit is shown in Figure 4.6. Some effort was made to reduce the power dissipation by raising the characteristic impedance of the LC-ladder, and thus allowing the drain resistors, CML stage and bias current to be scaled down. It was found that increasing the characteristic impedance to 61Ω by adjusting the L/C ratio gave the best results. Increasing the L/C ratio even further resulted in a rapid reduction in bandwidth and signal integrity due to the larger value, lower Q inductors. The decreasing self resonance frequency with increasing inductance also prevented the target 100ps delay up to 10GHz from being achieved.

A basic CML stage works almost as well as the proposed cascode CML gain stage. However, the cascode stage was chosen due to lower input capacitance. From simulation, it was found that the input capacitance of the cascode stage was 25% lower due to reduction in the Miller effect. This is to be expected as gate to drain capacitance (C_{GD}) is roughly 1/3 of the gate to source capacitance (C_{GS}) in this process. Normally a low (unity) gain CML stage would not benefit much from the cascode configuration. Another interesting observation is the output impedance of the circuit. Since the output

impedance is defined by $R_D \parallel r_{DS}$, the basic CML stage required a load resistor of 115Ω to bring the total output impedance down to 61Ω. If a cascode stage is used, the output impedance of this node becomes $R_D \parallel r_{DS}^2 g_m$. Since $r_{DS}^2 g_m >> 61\Omega$ it contributes little to the output impedance seen by the LC-ladder.

The ideal number of LC-sections was determined by measuring the frequency response and group delay while adding and removing LC-sections keeping $N\sqrt{LC} = 90ps$ (allowing for 10ps of delay to be introduced by the summing nodes). Figure 4.4 shows that the 6-section LC-ladder gave a bandwidth of 12.5GHz and a group delay of 85ps. The 12-section LC-ladder gave a bandwidth of 15.8GHz and a delay of 70ps. Figure 4.5 presents the minimum acceptable 3-section delay element. The bandwidth was 10GHz but this was not chosen as the total bandwidth of the filter would be too low.

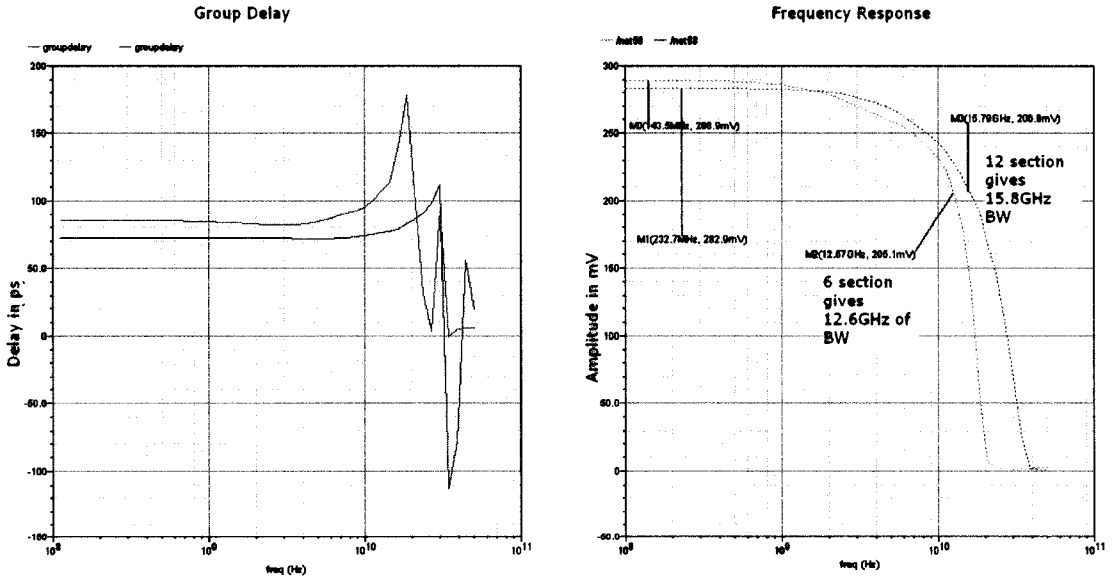


Figure 4.4: Frequency and group delay response of a 6-section and 12-section LC-ladder

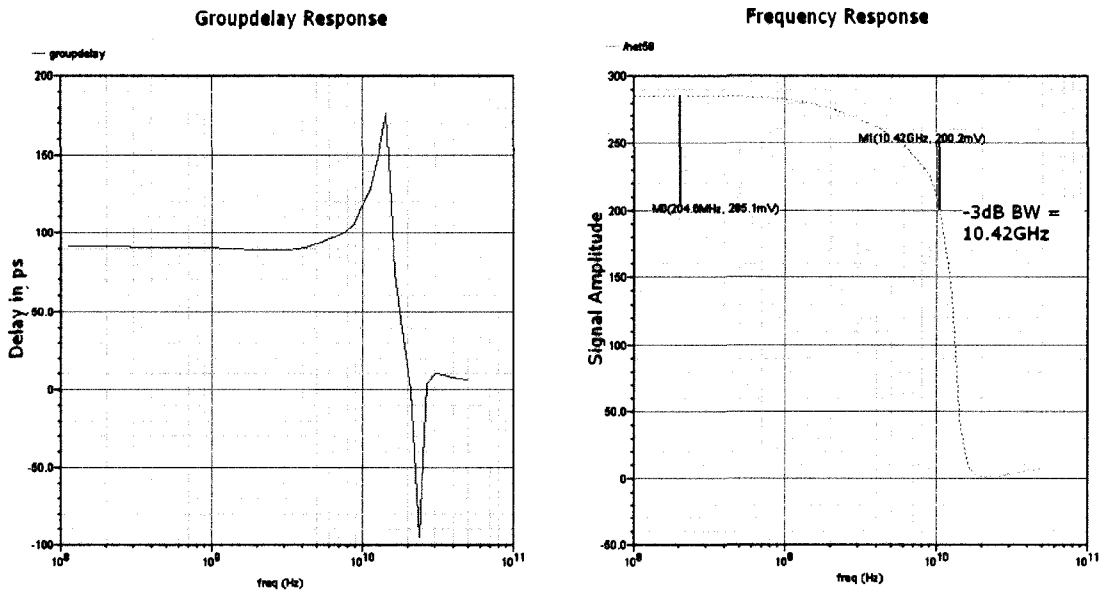


Figure 4.5: Frequency and group delay response of a 3-section LC-ladder

One of the major difficulties of the LC-ladder approach is the variation in the total group delay over process variation. One idea might be to use varactors as the capacitors in the delay line. This allows the total delay to be adjusted using a control voltage. In this case, a delay-locked loop may be used with a reference clock to determine the varactor voltage for the delay line. This option was not explored in this research. However, it is worth noting that the high frequency performance of the "ncap" varactors in the 0.13μm CMOS process is sufficient for the LC-ladder. There was a negligible reduction in bandwidth when varactors were used instead of metal-insulator metal (MIM) capacitors. This is to be expected as the inductors cause the greatest loss due to their inherent low-Q. The schematic and frequency domain performance of the finished delay element are given in Figure 4.6 and Figure 4.7 respectively.

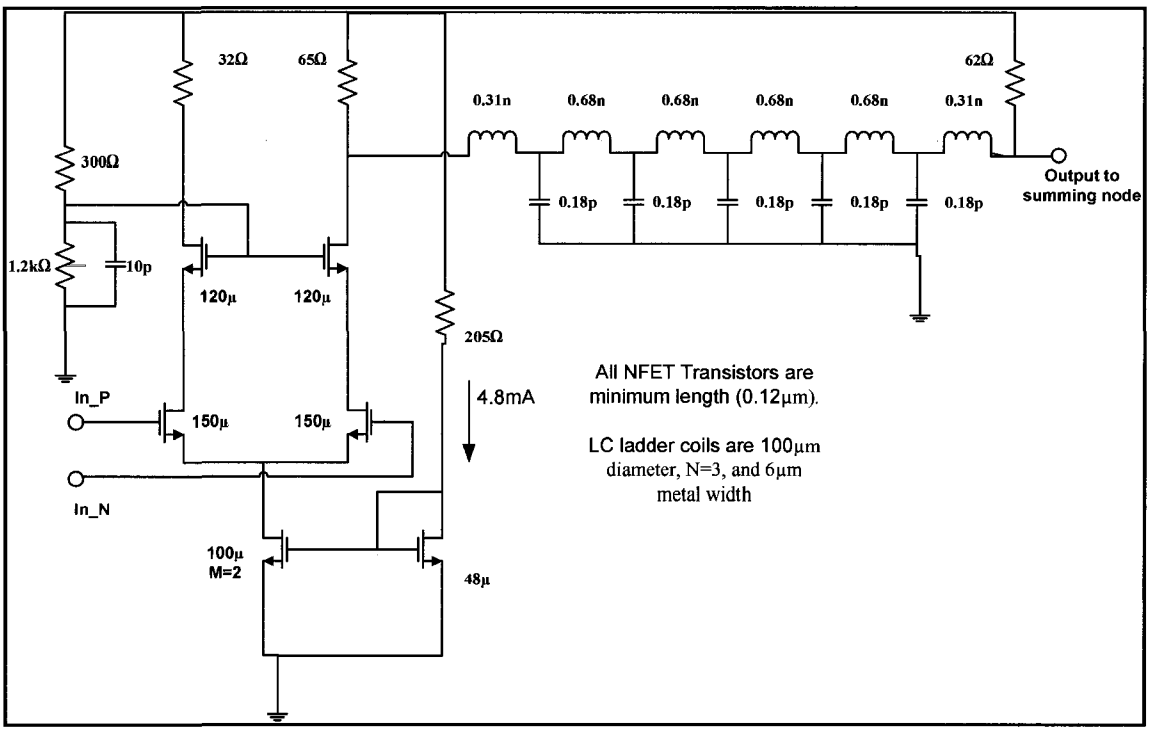


Figure 4.6: Schematic of the buffered 100ps delay element.

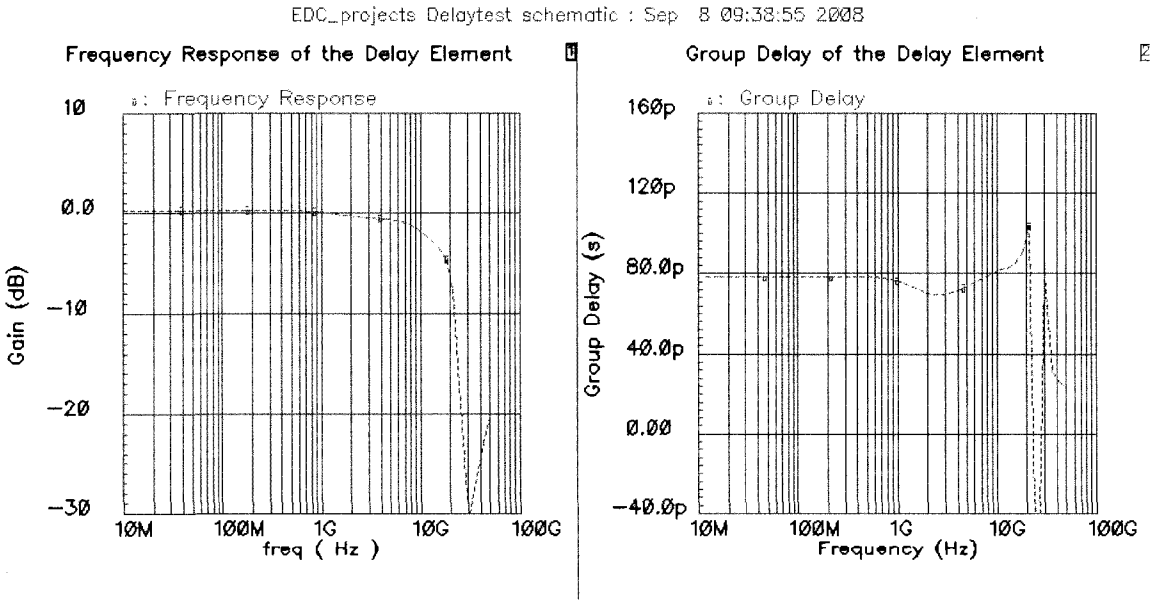


Figure 4.7: Frequency and group delay response of the buffered LC-delay element

In order to quantify the effects of process variation on the group delay and gain of the delay element, a Monte Carlo simulation was carried out and the values of group delay and gain at 1GHz were plotted in the histograms shown in Figure 4.8. The 3σ variations in group delay and gain were 4.08ps and 1.01dB respectively. This is considered acceptable for this design, as the effects of changes in gain can be compensated by adjusting the tap weights.

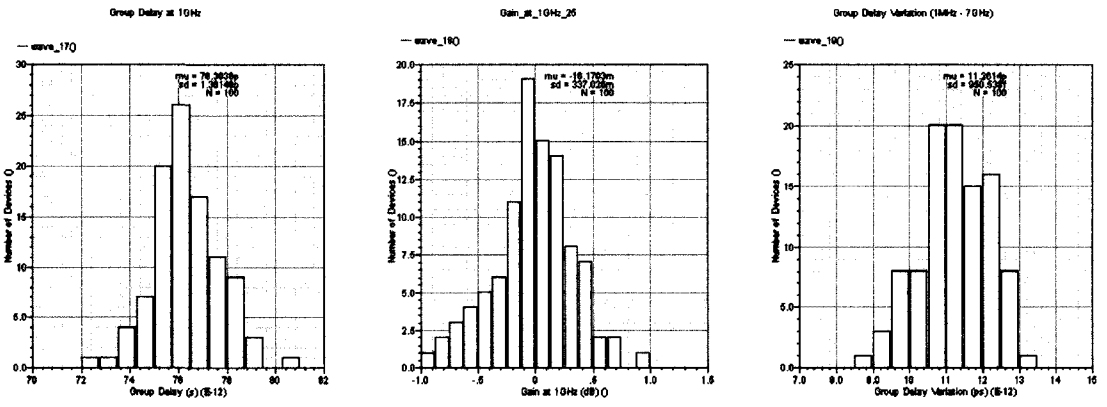


Figure 4.8: Monte Carlo simulation of the gain and delay over process variation

4.1.3 Dealing with the Single-Ended Output

The reader may have noticed that the delay line presented here is singled ended. This was done deliberately to save chip area. The first method used to couple the single ended outputs to both the summing nodes was a simple RC filter so only the DC portion of the signal is feed to the "inverting" input of the summation node. This approach had problems though. Since the data used in metro optical systems has spectral content down as low at 100kHz, there would be a requirement for a large 22nF external

capacitor. This is undesirable. To deal with this, a reliable DC reference must be generated on-chip to send to the unused differential input. The approach taken here is in the form of a scaled down "dummy stage" where the sum of the inputs to the delay element (with no AC component) are feed to a scaled down single ended version of the CML stage. This gives a reliable DC representation of the output signal with minimal dependence on process variation. This is certainly a better approach than a resistive divider. The circuit schematic is shown in Figure 4.9 and the Monte Carlo analysis showing a small variation in DC offset over process and mis-match is given in Figure 4.10.

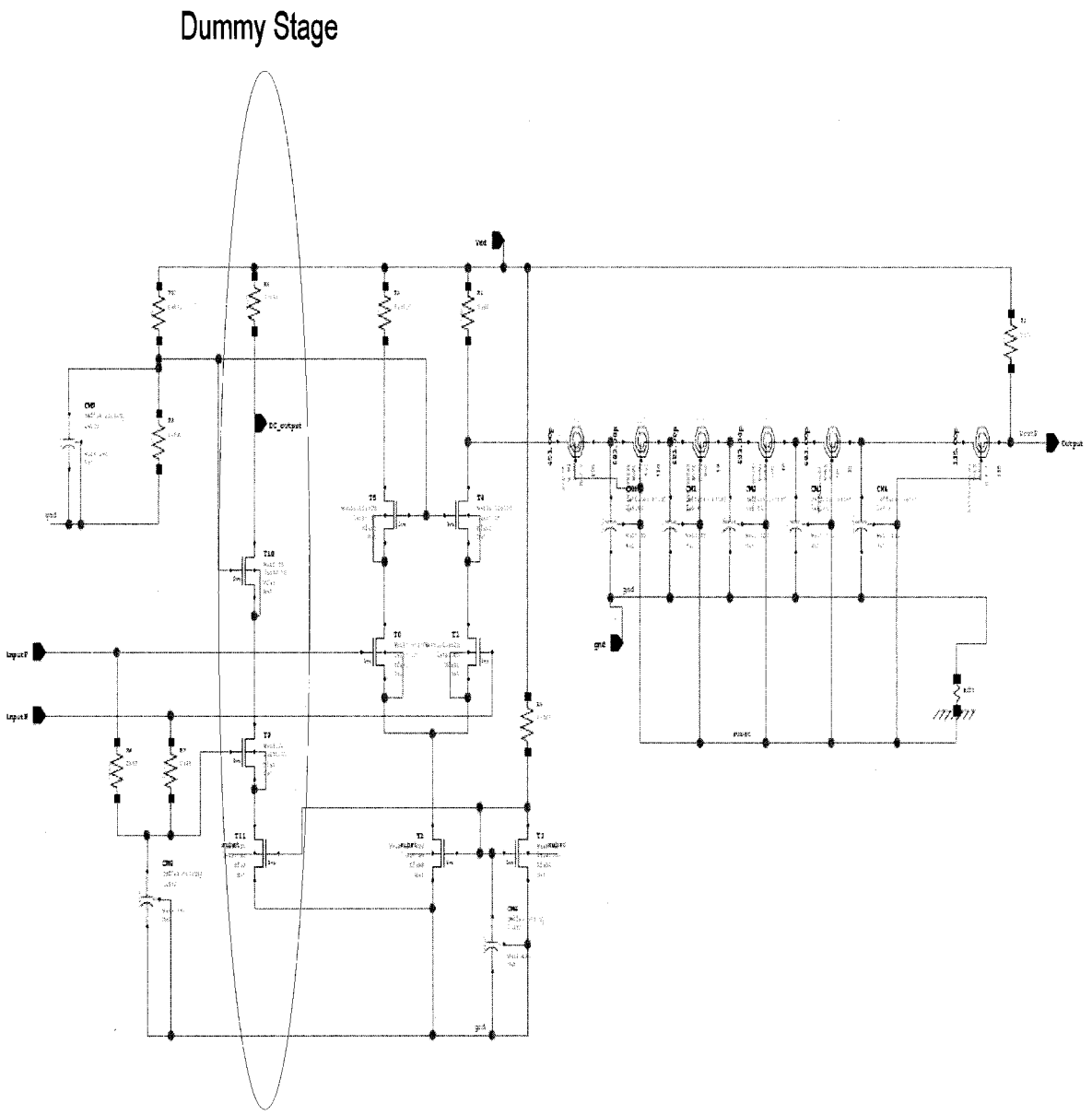


Figure 4.9: Schematic of the delay element showing the dummy stage

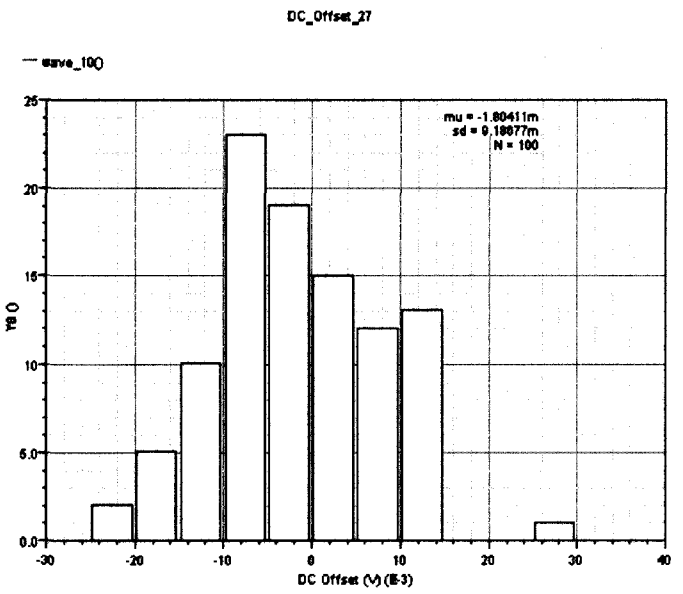


Figure 4.10: Monte Carlo simulation to verify DC-offset over process and mismatch

4.2 Design of Summing Nodes

Virtually all of the works surveyed for this research have some mention of the circuit topology of the summing nodes in the FFE section of an FFE/DFE filter. In all cases the summing node has the scaling amplifier or variable gain amplifiers integrated. The basic summing node is the CML stage shown in Figure 4.11. A modified version of this CML summing stage is presented in [31] and shown in Figure 4.12. This design has the advantage of dual polarity tap weights, a feature required in FIR equalizers. Both the basic and the cross-coupled summing nodes were designed and simulated in 0.13μm CMOS. However, there were issues discovered with this approach. The main one is variation in bandwidth with tap adjustment. This is due to the changing current densities in MOS transistors with each tap weight setting, and there is especially low bandwidth when a low tap weight is set. Since the proposed filter topology only uses negative tap weights, the dual polarity approach is not required.

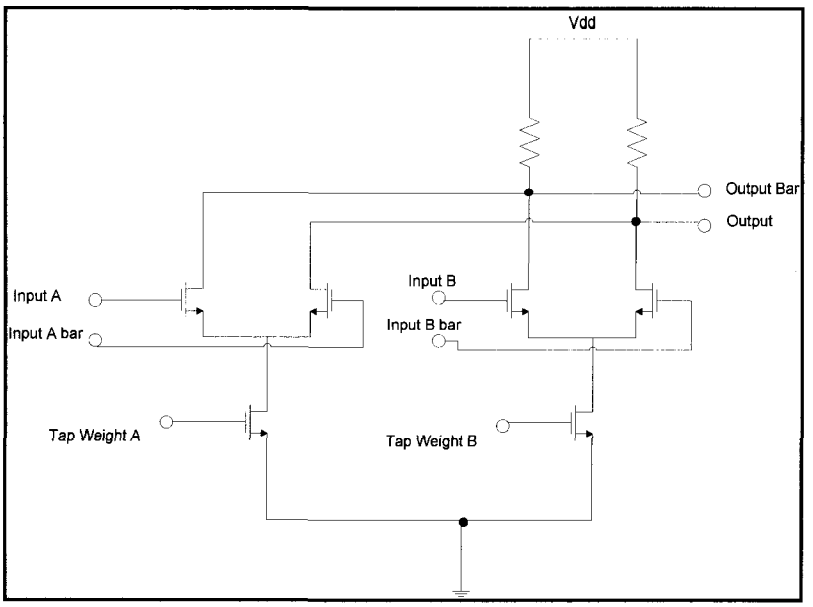


Figure 4.11: Basic CML summing node

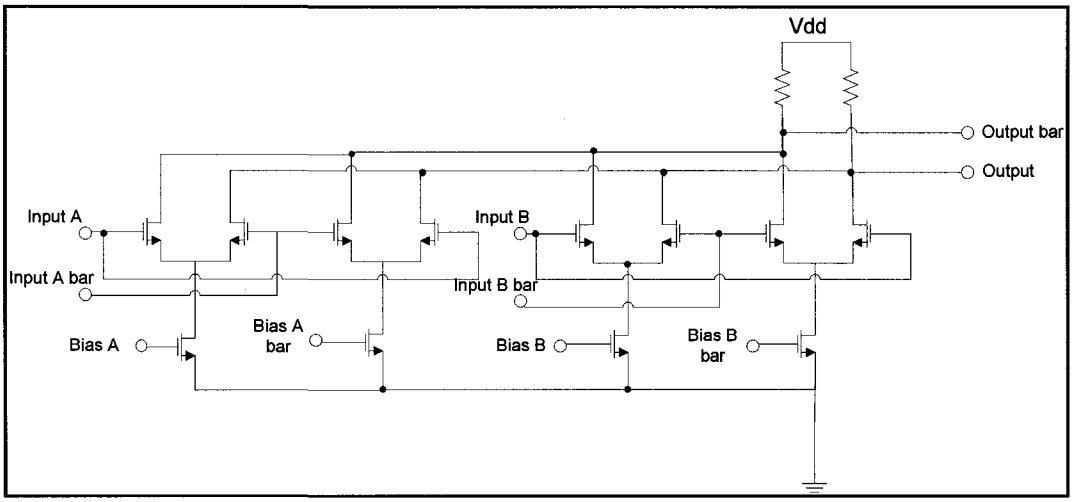


Figure 4.12: Cross-coupled dual polarity summing node

A new summing node topology is designed for this EDC solution which uses some of the ideas found [32] except with a few modifications. Instead of the low noise amplifier (LNA) approach, the signal and bias setting transistors are separate devices, and a CML biasing scheme is used. The circuit designed for this filter is shown in Figure 4.13.

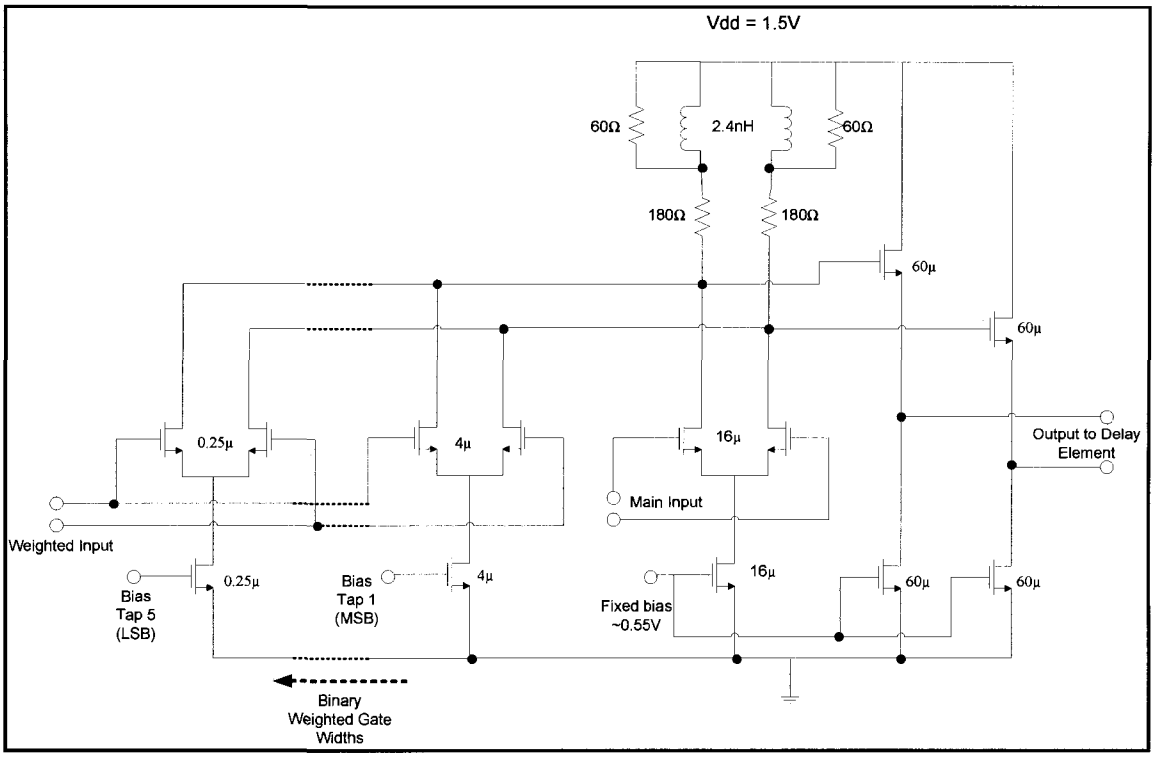


Figure 4.13: Schematic of the summing node

The main advantage of this design is the fact that it is digitally controllable and all CML stages carrying a signal are biased at the same current density. For both summing nodes in this design, a current density of 100µA/µm was used. This gives close to 80% of peak transition frequency (F_t) operation. Since F_t is a good measure of the fundamental bandwidth limit of a transistor this characteristic must be traded off with power dissipation. Figure A.3 of Appendix A shows the simulated F_t characteristics of this process. The range of the variable gain, expressed as a coefficient of the main input signal, is from 0 to -0.5. From the conclusions of chapter 3 this is a sufficient range for compensation up to 130km of single mode fibre. The digital control is achieved by turning biases 1 through 5 on and off. A simple CMOS inverter biased switch is used

provide buffering. One of the five switches for this design is shown in Figure 4.14. Another key aspect of the input summer is the broad-banding technique used at the summing node. An active load was attempted but this resulted in too much of a reduction in voltage headroom. Using a real inductor had some interesting effects. Since there is a scaling up which needs to occur between the summing nodes and the delay element, there is a significant capacitive load presented to the CML stage. The load inductors of 2.4nH produced a high-Q resonance at ~10GHz. To mitigate the impact on transient performance, these inductors were de-Qed with the use of the 60Ω shunt resistors. This gives a boost in bandwidth from about 10GHz to 15GHz. The inductors are not used in the output summation node as they are not necessary.

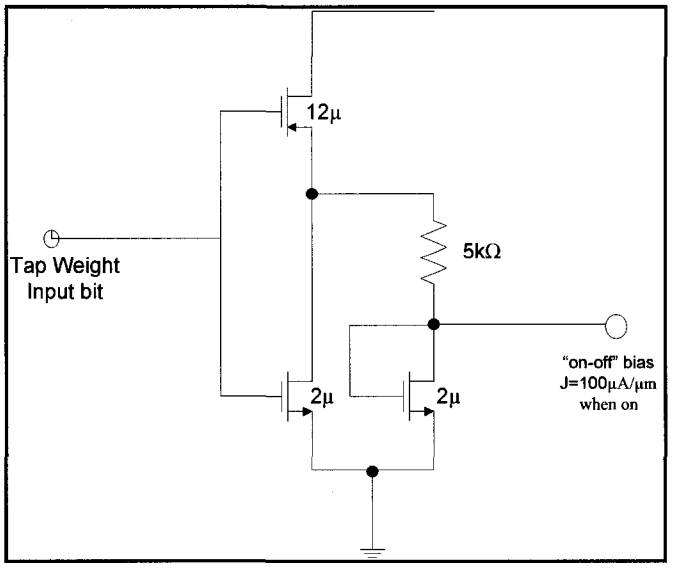


Figure 4.14: Digital control buffer for tap weight selection (5x)

4.2.1 A Note on Power Saving Measures

As mentioned in an earlier chapter, the delay element has relatively high power consumption and bias currents due to the fact that it has to operate with 10Gb/s signals up to $300mV_{pk-pk}$ in a 61Ω environment. In order to save power, the summation nodes are scaled back roughly ten times. This gives the added complexity of driving the 150μm NFETs of the delay line buffer with summing node FETs of only 16μm. The best approach to combat this potential bandwidth limitation is by the use of intermediately scaled source follower stages to serve as both level shifters and current buffering. A small signal alternating current (AC) simulation was carried out to size these transistors and, as shown in Figure 4.15, the optimum channel width is 60μm.

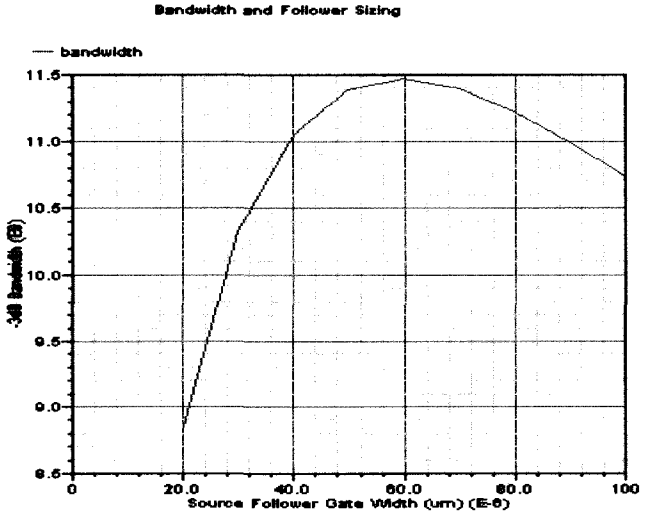


Figure 4.15: Scaling the source followers for maximum total bandwidth

4.2.2 Tests on the Summing Nodes in Isolation

Now that the summing nodes are designed, it was important to verify the performance with respect to bandwidth and linearity with various tap weight settings. The first simulation was carried out to ensure that the bandwidth and gain of the main, fixed input does not vary with the tap weight settings for the variable input. Figure 4.16 shows the frequency response of the main tap with a respectable 15GHz of bandwidth. The traces are not labelled since there is no difference in the frequency response while the tap weights are varied.

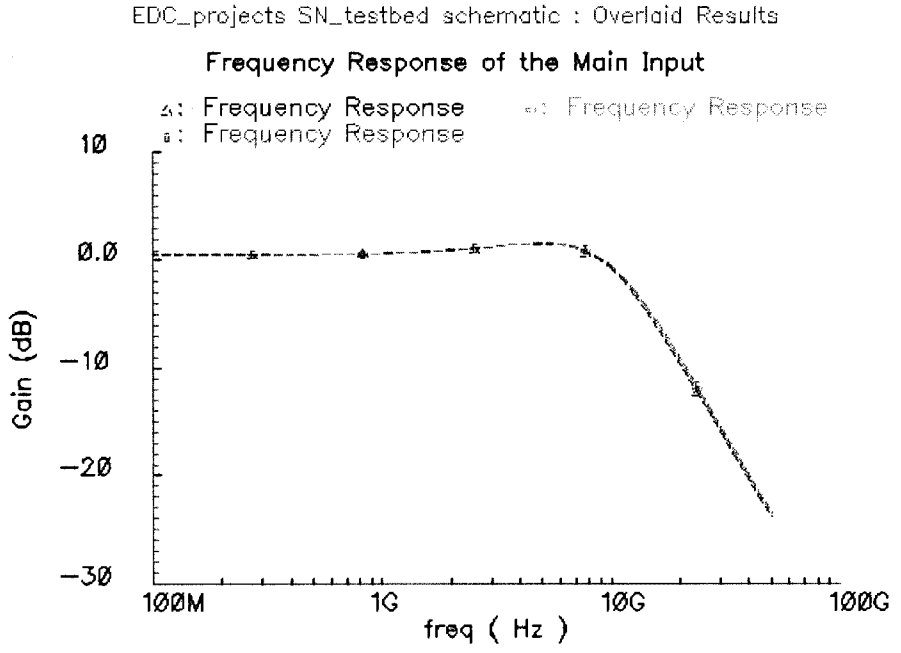


Figure 4.16: Frequency response of the main input

The next simulations were performed on the variable input. Figure 4.17 shows the frequency response with several different tap weights. Since this 5-bit weighted input

can have weights of 0 to -0.5, this corresponds to input binary words from 0 to 31. In the following plot, the highest gain is achieved with all bits high (ie. 31). The remaining curves are with weight values of 16, 8, 4, and 2. The linearity and monotonicity of this digitally programmable method was not verified as device scaling is similar to that of [31] and [32] which shows better than 2% non-linearity.

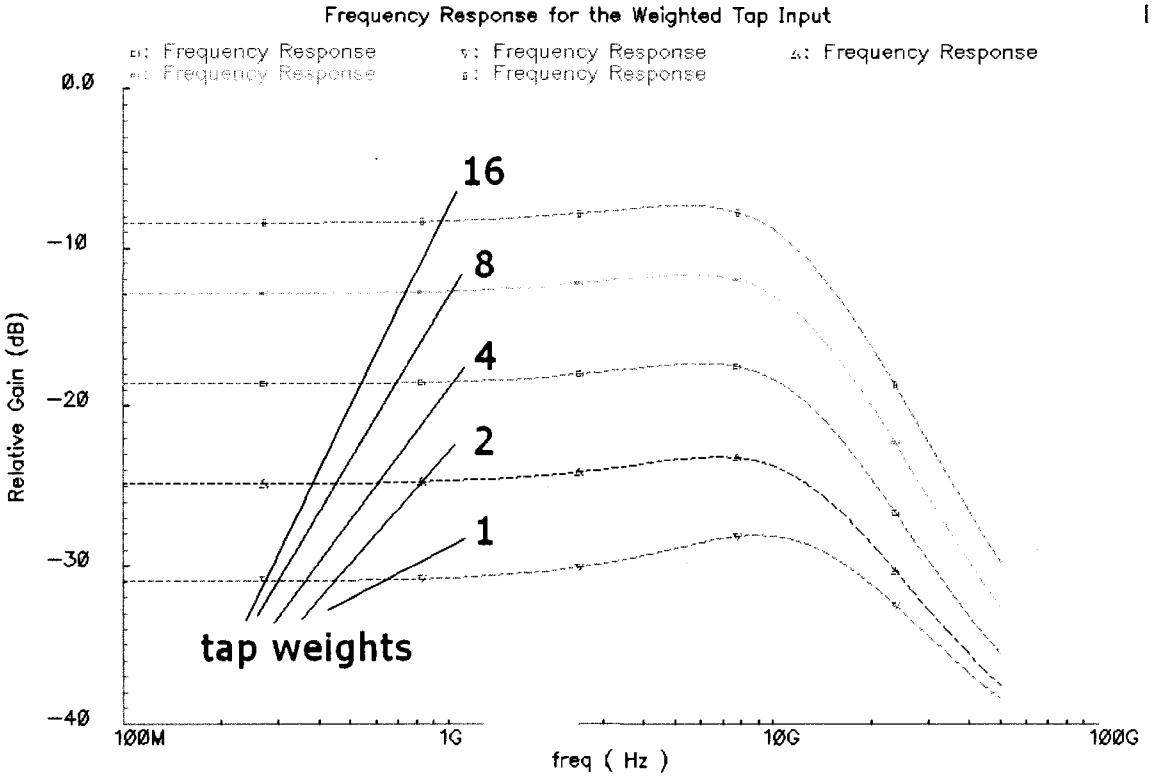


Figure 4.17: Family of frequency response curves of the variable input

One feature in the frequency response curves is the increasing bandwidth and peaking that occurs for low tap weight settings. Originally, it was thought that the "turned off" CML stages were capacitively coupled through the C_{GD}. If this were case, then there would be a resulting phase shift as the capacitive coupling is out of phase with the CML

stages inherent inverting property. After some work, it was confirmed that the 180° phase shift was present at the peak and thus capacitive coupling was the culprit. Whether a stage is turned on or off, the input capacitance at this node is equal to roughly $C_{GS}/2$ since the state of the current source has little impact on this capacitance (ignoring the r_{DS} of the current source and considering the C_{GS} of an NFET with width = $4\mu m + 2\mu m + 1\mu m + 0.5\mu m + 0.25\mu m \approx 8\mu m$). The peaking around 10GHz may have something to do with the reduction of Miller effect at the output node when low tap weights are set. Since the Miller effect depends on the drain voltage moving the opposite direction of the gate voltage, it seems plausible that reducing the circuit's gain by shutting off stages would reduce this effect. Since the peaking occurs at 10GHz and most of the spectrum of 10Gb/s NRZ data is below 7GHz, this effect should be negligible. This will be shown later by evaluating the entire equalizer circuit with various tap weights.

4.3 Overall filter performance

4.3.1 Impulse Response

Before applying the distorted waveforms to the designed filter, some tests were performed to ensure that the response is fit for purpose. The first test is a simulation of impulse response with all taps set to the maximum values. For the first test, a 100ps, $300mV_{pk\text{-}pk}$ pulse with 15ps rise times is used as the stimulus. The output of this simulation is shown in Figure 4.18.

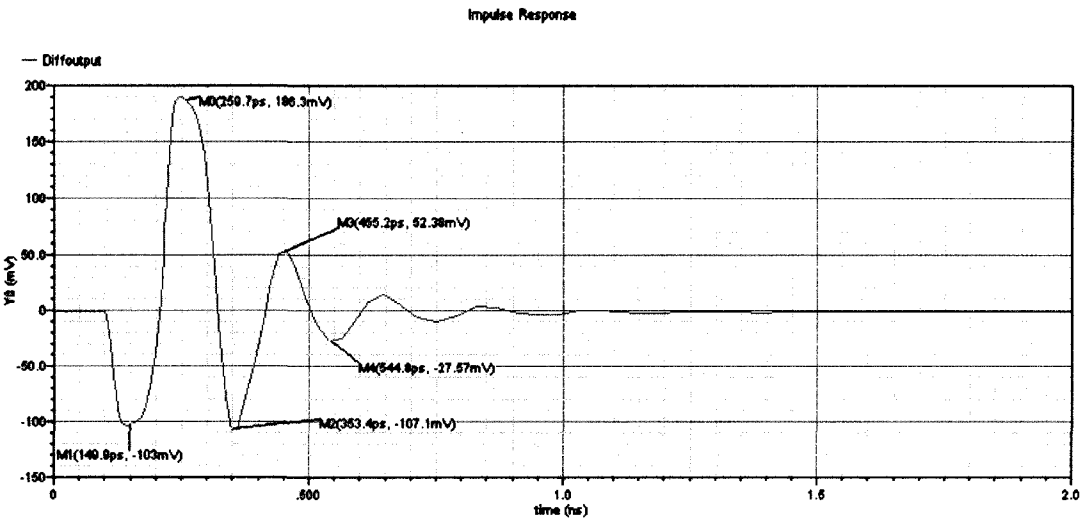


Figure 4.18: Impulse response of the IIR filter with taps set to the maximum

This result allows for some calibration of the tap weights with respect to the input digital control word. Table 2 serves as a look-up table for tap weights. It should be noted that this table is different for each device due to process variations. Especially since the gain of the buffers in the delay element are affected by process parameters as shown earlier. Figure 4.19 and Figure 4.20 are the simulated impulse responses with both taps set to -0.25 and 0 respectively.

Tap input (decimal)	FF Tap	FB Tap	Tap input (decimal)	FF Tap	FB Tap
31	-0.554	-0.575	15	-0.268	-0.278
30	-0.536	-0.556	14	-0.250	-0.260
29	-0.518	-0.538	13	-0.232	-0.241
28	-0.500	-0.519	12	-0.214	-0.223
27	-0.483	-0.501	11	-0.197	-0.204
26	-0.465	-0.482	10	-0.179	-0.185
25	-0.447	-0.464	9	-0.161	-0.167
24	-0.429	-0.445	8	-0.143	-0.148
23	-0.411	-0.427	7	-0.125	-0.130
22	-0.393	-0.408	6	-0.107	-0.111
21	-0.375	-0.390	5	-0.089	-0.093
20	-0.357	-0.371	4	-0.071	-0.074
19	-0.340	-0.352	3	-0.054	-0.056
18	-0.322	-0.334	2	-0.036	-0.037
17	-0.304	-0.315	1	-0.018	-0.019
16	-0.286	-0.297	0	0.000	0.000

Table 2: Table of tap weights and control words

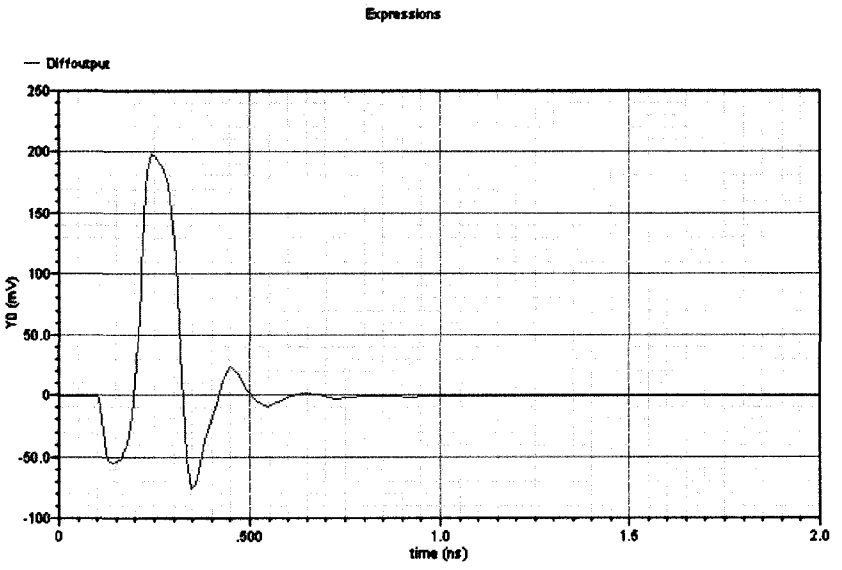


Figure 4.19: Impulse response with both tap weights set to -0.25

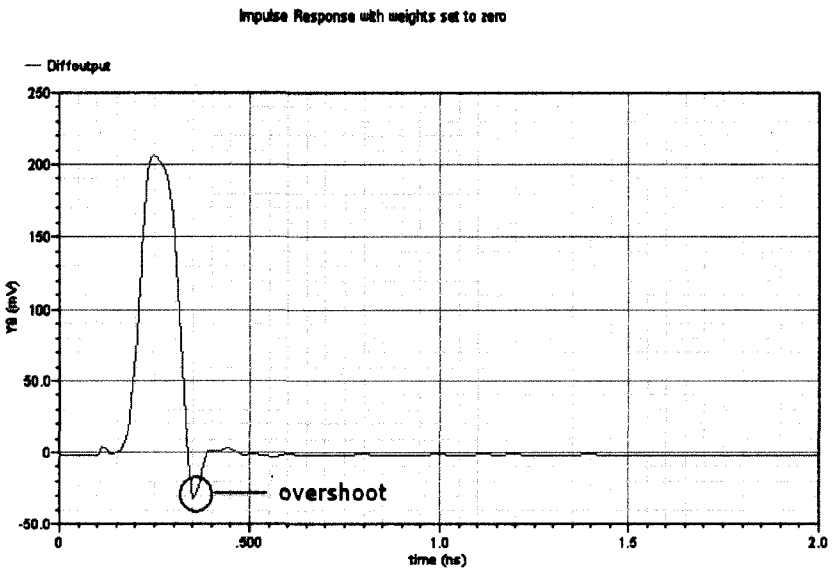


Figure 4.20: Impulse response with tap weights set to zero

The behaviour is considered to be close enough to the numerical simulations performed earlier with exception of the small overshoot seen in Figure 4.20. This overshoot disappears when the rise and fall times of the input pulse stimulus is increased from 15ps to 25ps.

4.3.2 Frequency response variation with tap weight adjustment

The next test on the analog filter is the frequency response with various tap weight settings. This is an important result and it shows the overall bandwidth of the summing nodes, buffers and delay lines in this process. This is shown in Figure 4.21. The clean response with taps set at zero shows exemplary performance with a total bandwidth of 10GHz. When the taps are set to non-zero values, the clear peak at 5GHz is exactly what is needed to equalize the unique ISI from single mode fibre as shown in earlier sections.

This agrees with the MATLAB simulation of an ideal IIR filter using the command "freqz([-0.25 1],[1 0.25])".

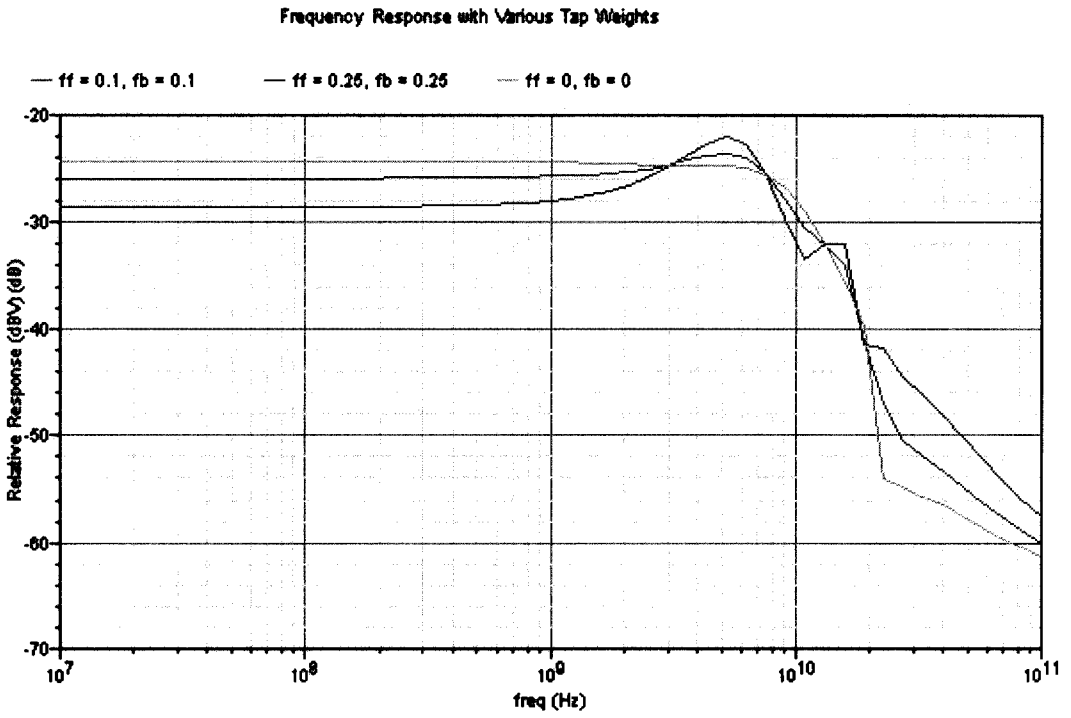


Figure 4.21: Frequency response of the filter with various tap weights

4.3.3 Linearity

The efficacy of any linear filter is strongly dependent on the achieved linearity of all of the components used. This was a challenge in this design given the number of CML buffers used. In early experiments, some simulations showed that higher bias currents give better overall linearity at the expense of headroom and gain. From the spectrum and total harmonic distortion measurements, it appears that this filter can work reliably with a 250mVp-p input signal. This will be shown later when measured signals are used as the stimulus. Figure 4.22 shows the spectrum of the output signal when a $250mV_{pk\text{-}pk}$

1GHz pure sinusoid is presented to the input. As hoped, the non-linearity is small and predominantly odd-order. With NRZ signalling, even order non-linearities cause issues with the slicing operation in later stages as the effective 50% slicing point changes when an even order distortion is added. Mathematically, a second order non-linearity has the same effect on slicing point as adding DC to the signal.

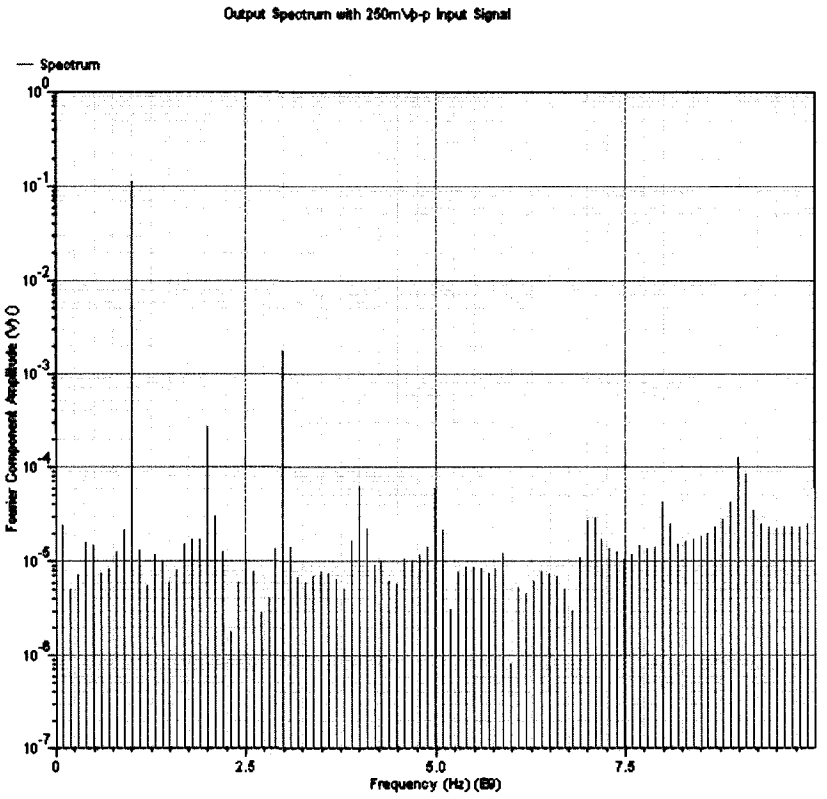


Figure 4.22: Output spectrum with a 1GHz sinusoidal input signal

Figure 4.23 gives a very important result. One of the weaknesses of this filter could be considered that any signal passed to the feed-back tap has to go through the summing nodes more than once. This may have the effect of multiplying the non-linearity by several times. Luckily, in the selected application, tap weights tend to be no larger than -0.35, and thus this effect is small. The family of curves in Figure 4.23 gives the total

harmonic distortion (THD) with three different tap weight settings. The ultimate test of linearity is determining whether the filter performs differently as the input signal amplitude is changed.

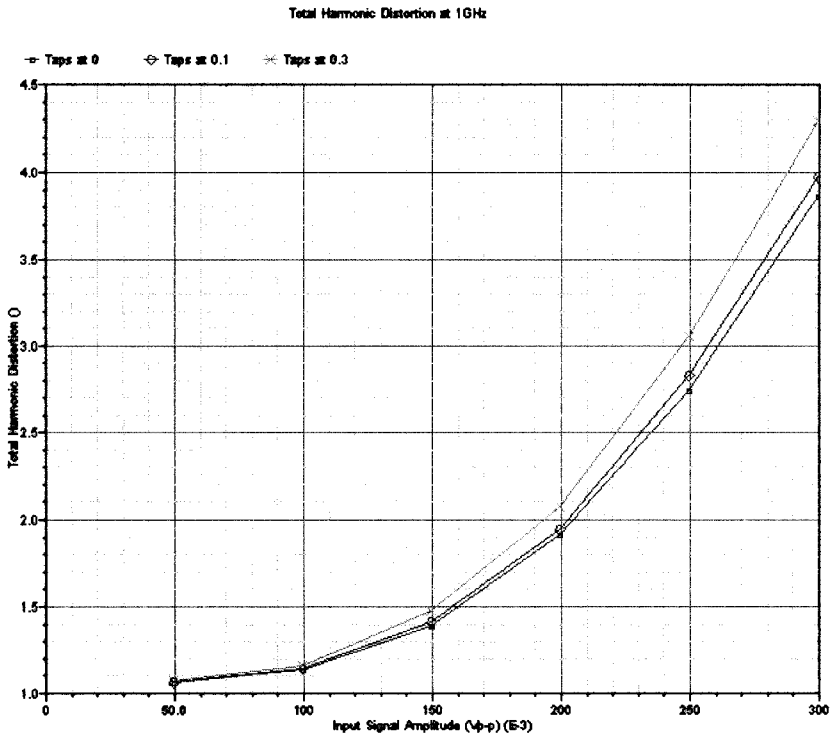


Figure 4.23: Total harmonic distortion as a function of input signal amplitude

4.3.4 Noise Performance

Given that there will always be a high sensitivity TIA in front of any EDC filter, noise performance of this component is not critical. In all optical receive chains, the TIA and photo-detector are the dominant sources of noise [4]. It is important to ensure that the noise contribution is at least a few times lower than that of the TIA. This is not difficult given that this filter is constructed with unity gain CML stages biased very close to the

current density for minimum noise figure (as in Appendix A). Figure 4.24 shows the simulated input referred noise of the proposed circuit. In optical transmission specifications, input referred noise seems to be the industry preferred measure of noise contribution rather than noise figure. As one can see, there is a significant amount of 1/f noise in this design. However, once the noise is integrated over frequency it comes out as $0.406mV_{RMS}$, the input sensitivity for BER = 10^{-10} will be $2.8mV_{pk-pk}$. It is interesting to note that the commercially available PIN-based optical receiver has an output signal of $20mV_{pk-pk}$ when it is operated at its BER = 10^{-12} sensitivity point of -18.5dBm input power. This shows that the EDC filter is not the dominant source of noise.

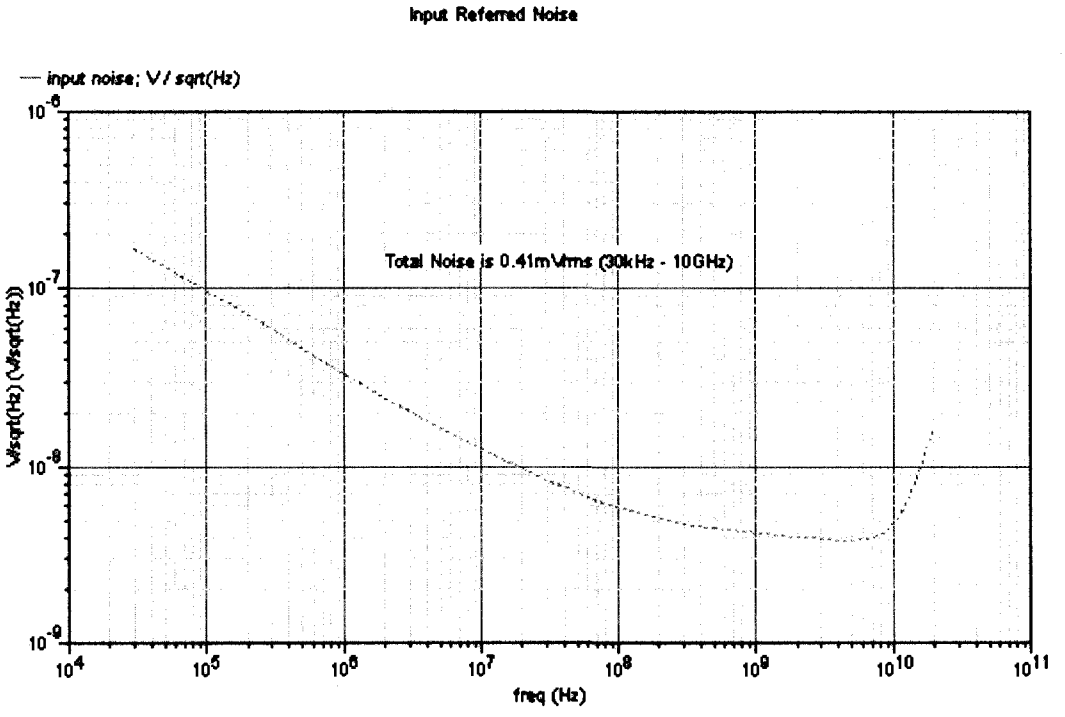


Figure 4.24: Input referred noise of the EDC filter

4.3.5 Power Dissipation

After all design revisions were made, the total power dissipation was found to be 75mW. 2/3 of the power is consumed in the delay element, and the remaining 25mW comes from the summation nodes. To the author's knowledge, this is 2-3 times lower than any other EDC solution with the exception of [16], however, this circuit compensates for ISI up to only 300ps and there is no input and output buffering at the LC-ladder delay lines.

5 Field Measurements and Performance Verification

The final step in this research is proving the proposed EDC solution. Although the focus of this research is minimizing the EDC chip area and power dissipation, the final design has a transistor count of 85, an estimated area of 1mm by 1.5mm, and 14 input and output pads. Another challenge is finding a suitable adaptation algorithm to interface with this adaptive filter. Even considering that this circuit is still approximately three times smaller than an EDC chip for the same application, the time required for layout, fabrication and measurements will exceed the time allotted for a master's thesis. It is prudent however, to address some of the natural variables which come into play when comparing a CAD simulation with a finished, packaged device. Since the proposed circuit is an electronic filter designed to reduce the effects of optical chromatic dispersion, the main differences, in order of severity between simulation and practice are:

1. RF interaction between the optical receiver module (PIN detector + TIA) and the EDC filter.
2. Deviation of RF performance, linearity and frequency/impulse response of a real optical receiver and transmitter compared to the receiver model used in numerical simulation.
3. Package parasitic such as bond-wire inductance and resistance, decoupling capacitors, etc.
4. Parasitics due to layout.
5. Mutual inductance of the on-chip inductors used in this design.

The proposed verification plan was designed to address most of these concerns. This will be discussed in the next section.

5.1 The Performance Verification Plan

In order to address concerns 1 and 2, the most efficient approach is to visit an optical link test laboratory[11] and measure the electrical output of a real optical receiver, receiving a signal after 50km to 150km of single mode fibre. The recorded data from this work will be in the form of long text files containing the time and voltage information measured using a digital communications analyser (DCA) for various reaches of fibre. This data can then be brought into Cadence Analog Artist for transient simulation of the EDC filter. Other data that can be collected are eye-diagrams of the transmitted optical signal and the received electrical signal for comparison with simulated results. This in fact was used in the earlier section entitled "Validation of Simulated Optical Signals" for purposes of verifying the dispersion models used in MATLAB.

To address concern 3, packaging parasitic, the test-bench used in Cadence simulated the packaging parasitics. For the power supply, 4 wire bonds were assumed with 0.5nH inductance each and 0.1Ω resistance. The chip was designed to have a total of 30pF of Vdd to ground capacitance between metal layers to mitigate ground and supply bounce. The schematics for the test bench and packaging parasitic can found in Appendix C.

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[11] The optical link test laboratory of Bookham Inc. of Kanata, Ontario was generously provided to contribute to this research. Measurements were carried out on May 20, 2008. Results used with permission.

The practical issues 4 and 5 are not directly addressed, however, since this design does not really stress the limits of the 0.13μm CMOS process there is little risk. For example, a unity gain CML stage biased at 100μA/μm current density gives a bandwidth of greater than 18GHz with no broad-banding techniques used. The proposed circuit design has a total simulated bandwidth (taps set to 0) of 10GHz which is approximately 30% higher than that which is required for this application.

5.2 Measurement setup

The measurements carried out in the optical link test laboratory were completed using the setup shown in Figure 5.1. The pattern generator of the Hewlett-Packard BERT system was set to provide 10Gb/s NRZ differential electrical signals with a PRBS 2^7-1. Longer patterns were available, however, it was necessary to keep the pattern short so that a complete pattern length was able to be recorded by the oscilloscope. The optical transmitter used was a zero-chirp device contained in an optical module with the biasing and drive electronics. The optical output signal from the transmitter is shown in Figure 5.3. The optical signal is then sent down lengths of 0, 50, 75, 100, and 150km of fibre using a network of splitters, attenuators and an optical switch. There were 2 erbium doped fibre (optical) amplifiers (EDFAs) in this set placed every 75km to compensate for losses. The optical noise generated at these reaches is insignificant compared to the electrical noise generated at low signal levels in the TIA. This was verified by checking the optical signal to noise ratio which was always greater than 35dB OSNR/0.1nm. The 10Gb/s optical receiver shown in the diagram was held onto a test PCB using a pressure jig, and the differential electrical output signals were brought to the digital oscilloscope

using high grade 50Ω cables and DC blocking capacitors. The input to the optical receiver was kept constant at -10dBm such that the output signals were 300mV$_{pk-pk}$. This PT10GC model receiver has a TIA gain of 1.5kΩ, 9GHz of bandwidth, and a photo-detector responsivity of 0.9mA/mW.

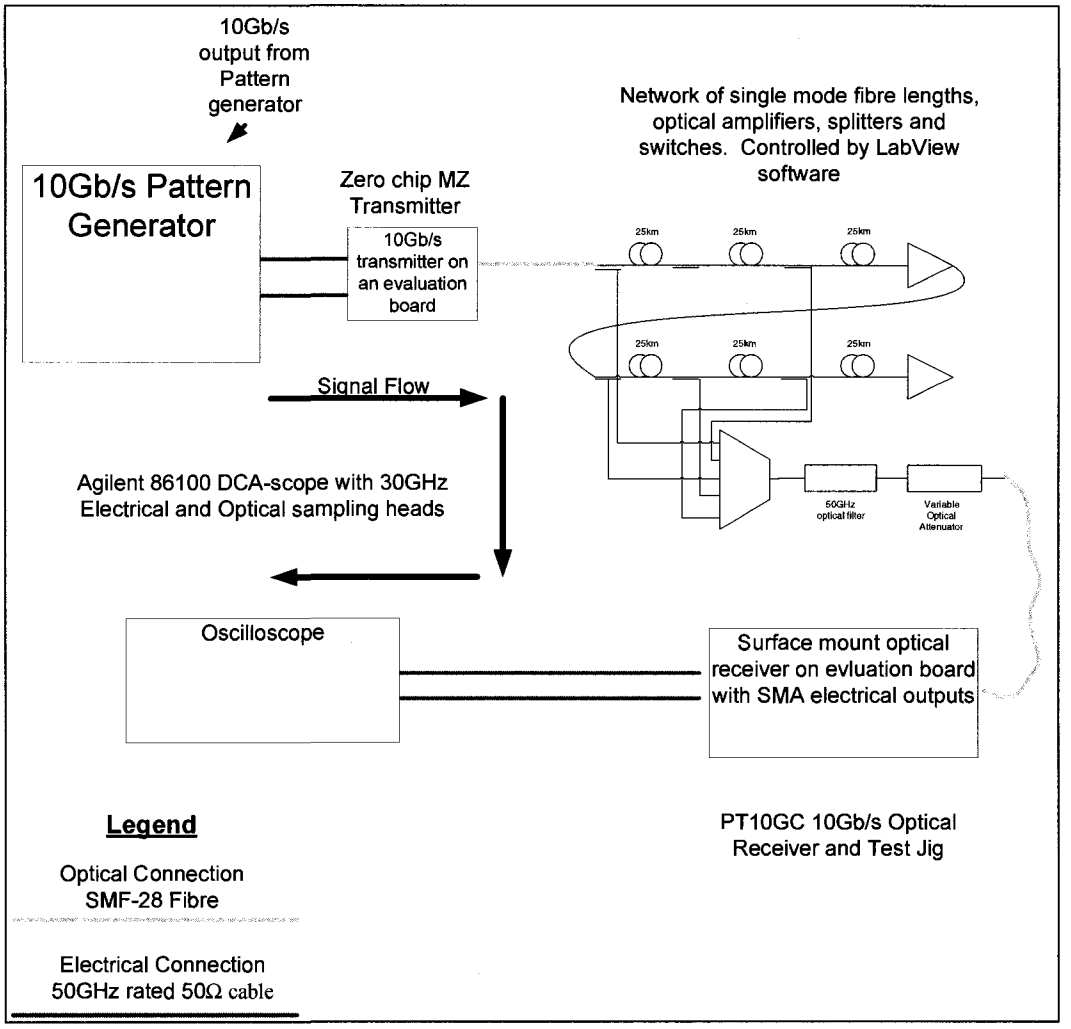


Figure 5.1: Block Diagram of optical test setup

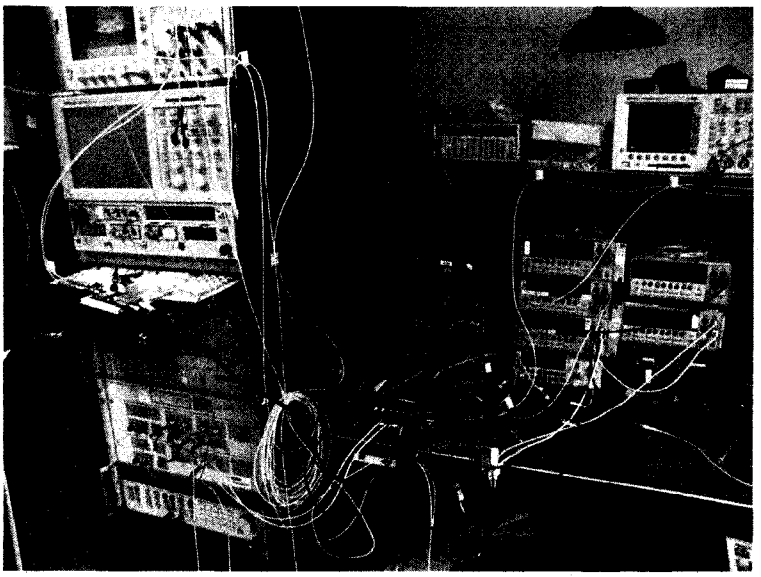


Figure 5.2: Optical link test facility - fibre spools not shown

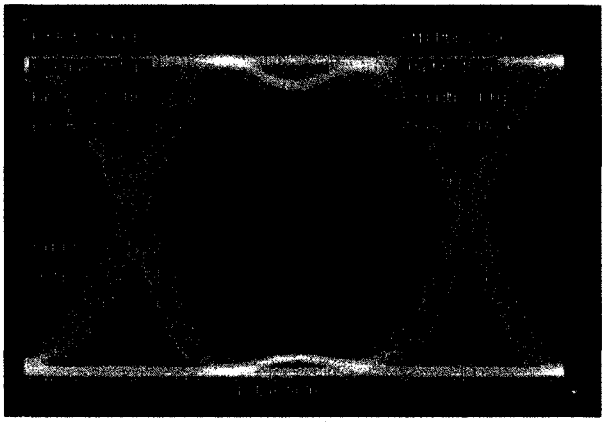


Figure 5.3: Optical output signal from the zero-chirp MZ modulator

Before storing the output electrical waveforms from the optical receiver, the eye-diagrams were captured on the oscilloscope. These are shown in Figure 5.4 and they can be compared with those simulated in Figure 2.3. The one exception is for the 125km reach. This test link did not have a tap at 125km, so the simulated signal needed to be used for this data point.

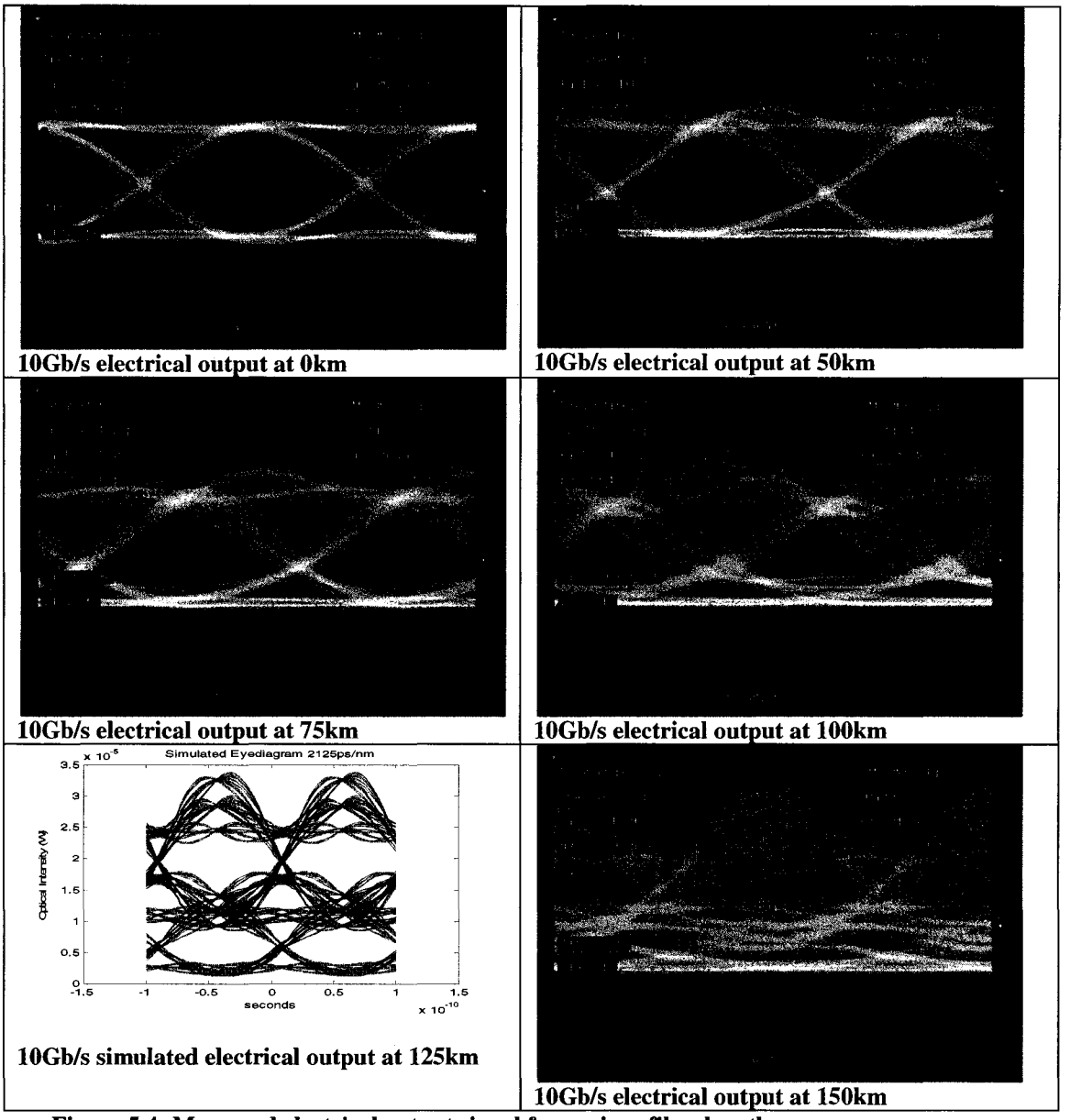


Figure 5.4: Measured electrical output signal for various fibre lengths

Now that the waveforms have been stored in text files, it is possible to load these signals into Cadence and run transient simulations. Before doing this, some significant work had to be done in MATLAB to determine the correct tap weights. The measured data needed to be up-sampled then the LMS algorithm was used to find the tap weights. There were only minor differences compared to the simulated tap weights. The eye-

diagrams from the input and output of the EDC filter were plotted and shown in Figure 5.5.

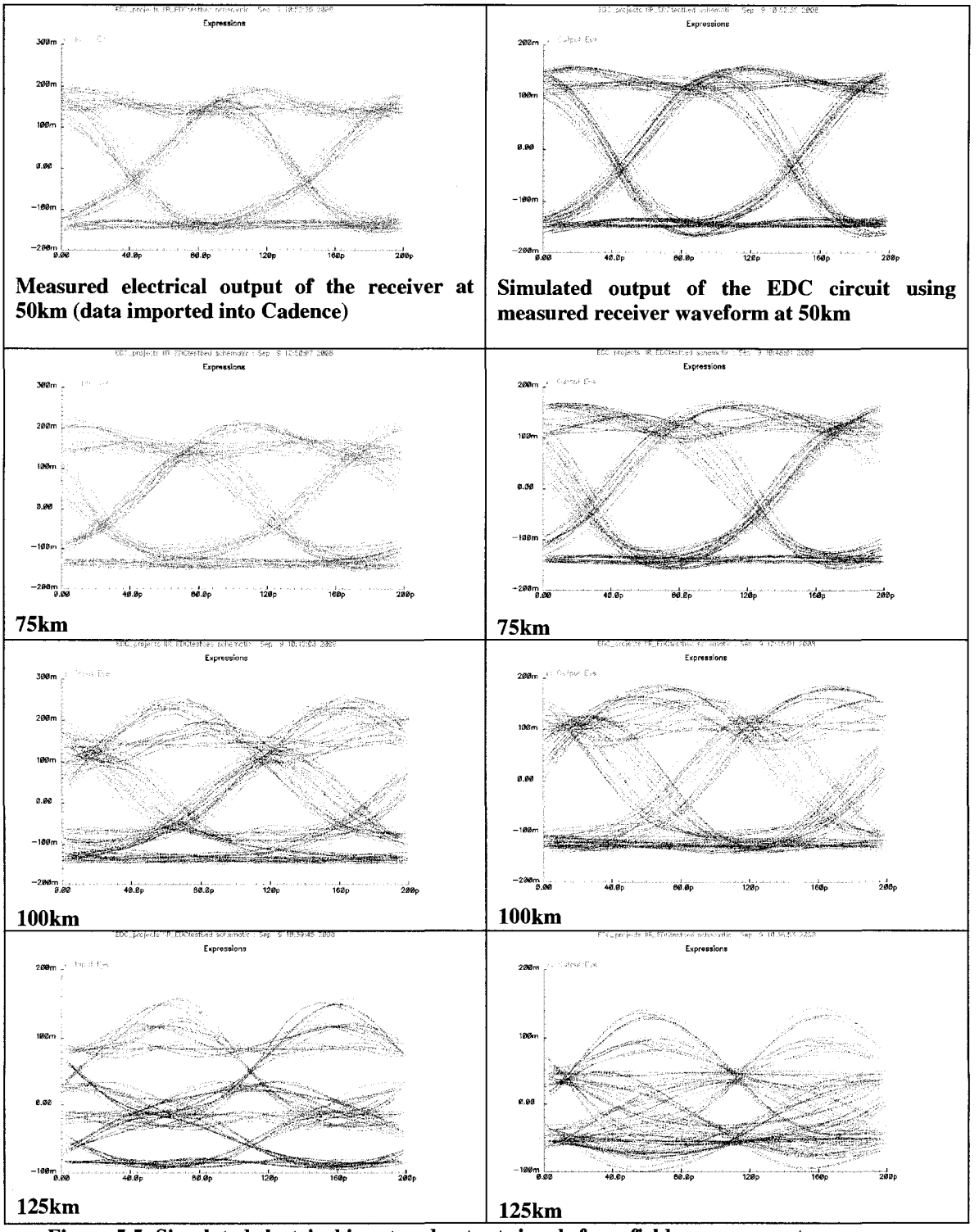


Figure 5.5: Simulated electrical input and output signals from field measurements

Since it is difficult to spot the increase in eye-openings in Figure 5.6, a graphical method was used and the eye openings were measured as a ratio of opening versus mean signal amplitude. The results of the simulated EDC solution with real inputs can now be compared with numerical simulations and in section 3.1.1. Figure 5.6 shows the dispersion penalty of the simulated EDC circuit with real measured input electrical signals. There is fairly good agreement, however, the measured signal shows slightly worse dispersion penalty. This variation might be due to the dispersion characteristic of the fibre used or the non-ideal behaviours of the optical receiver. At 100km, the 5-tap FFE filter has about 0.75dB advantage over the proposed design. This difference disappears at 125km.

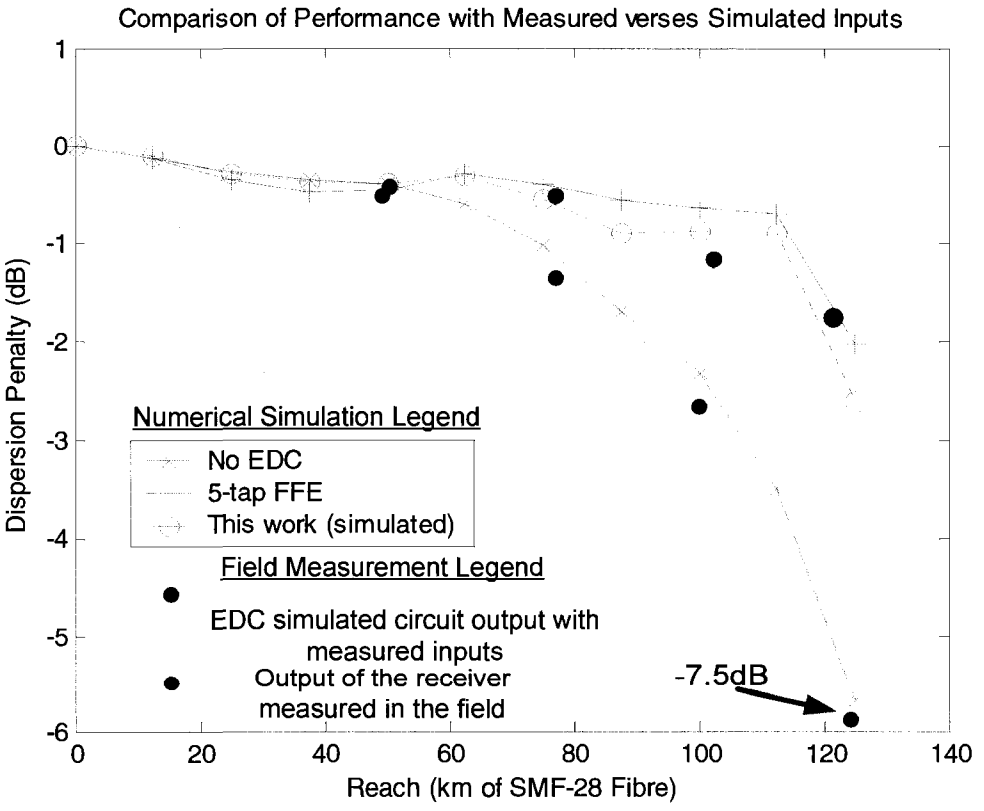


Figure 5.6: Comparison of EDC circuit with measured inputs versus the numerical simulation

6 Conclusion and Future Work

A new EDC solution has been developed and its feasibility was confirmed by both numerical simulation, and measured data. The design in 0.13μm CMOS was challenging, and this was due to some of the unique features of this filter topology. The next step to prove this design is to have it fabricated and tested in an optical link. This will be the focus of future work. There were no reported references in literature of IIR filters being used in this way to reduce the physical length, and power consumption for this unique application. The only disadvantage of this approach may be that it only works with single mode fibre – however, this question can be answered once the chip is manufactured and tested in a multimode link. This circuit design could be improved by building in some compensation for gain variation over process and supply voltage. Achieving the necessary speed for this application was surprising not difficult and therefore, a good extension of this research might be modifications to allow for operation up to 18Gb/s and even 40Gb/s as these links emerge.

Appendix A: NFET Characterization

The following plots were used during the circuit design to arrive at values for r_{DS}, g_m, and other critical operating parameters. Both standard nFET and low threshold voltage nFETs were used in this design.

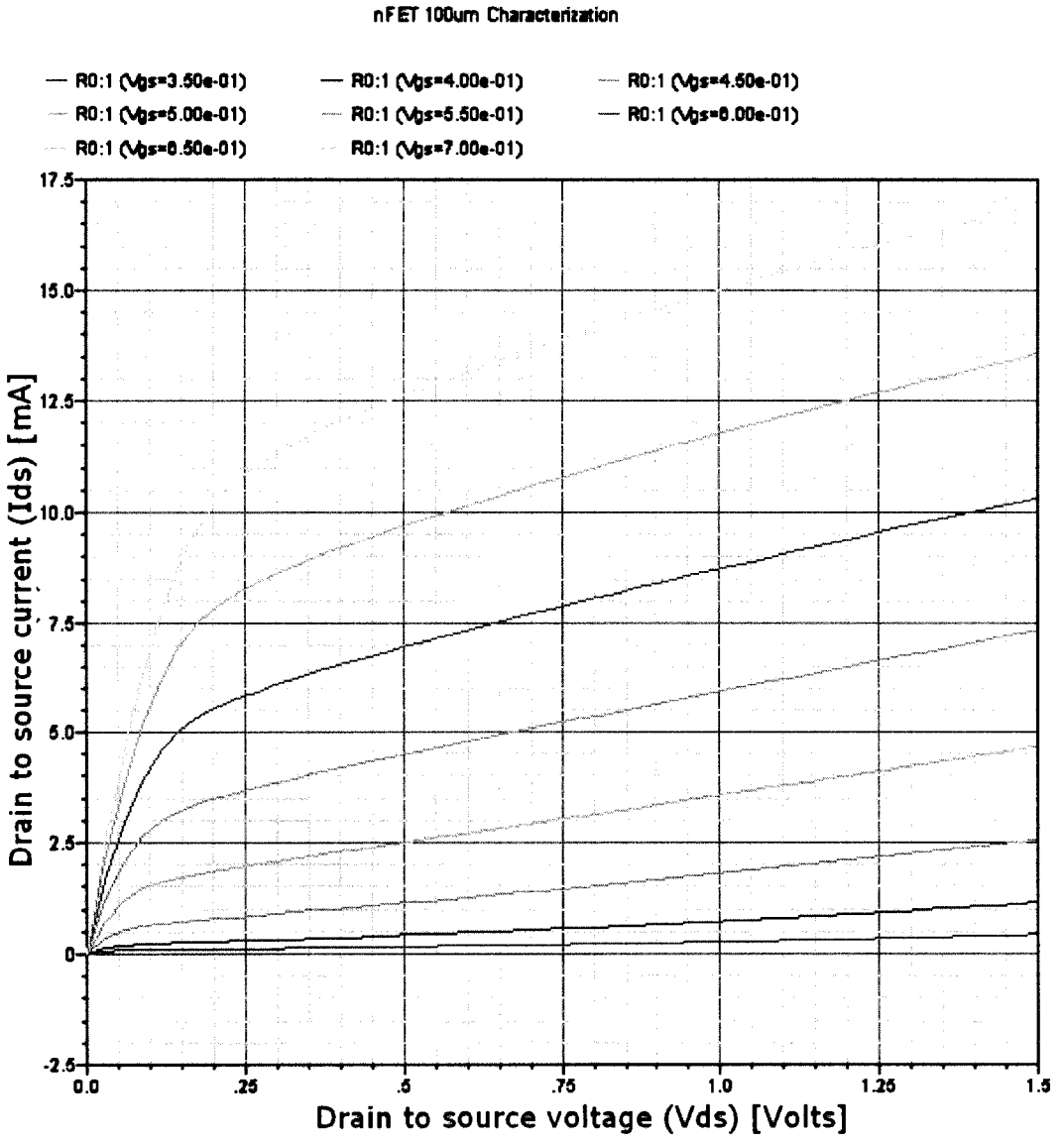


Figure A.1: I-V characteristic of the standard nFET transistor (W =100um, minimum length)

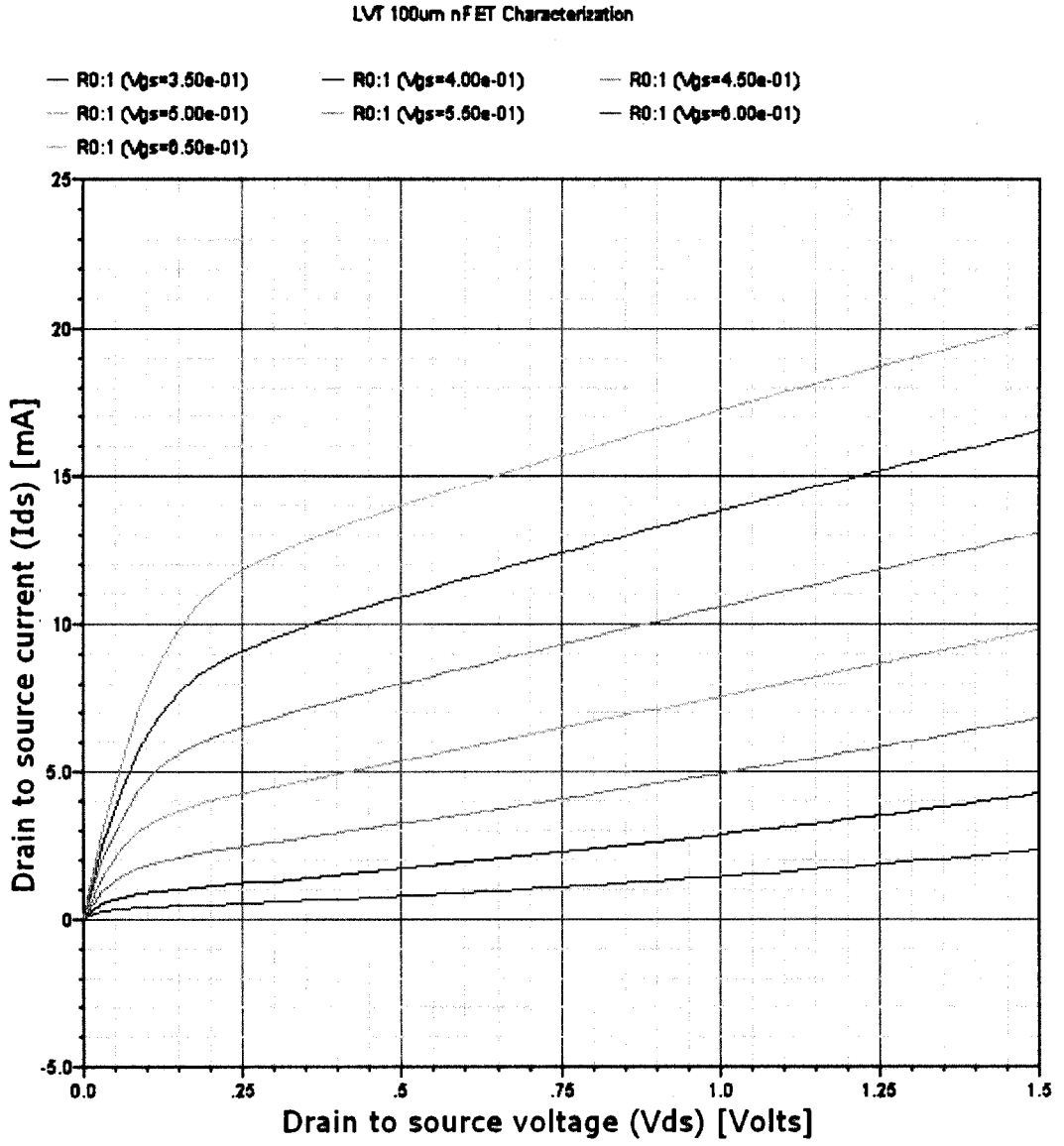


Figure A.1: I-V characteristic of the low threshold voltange nFET transistor (100um width)

The following plot was used to find the current densities and implications on transistor speed and noise figure.

Unity-Gain Transition Frequency (F_t) of an NFET Transistor

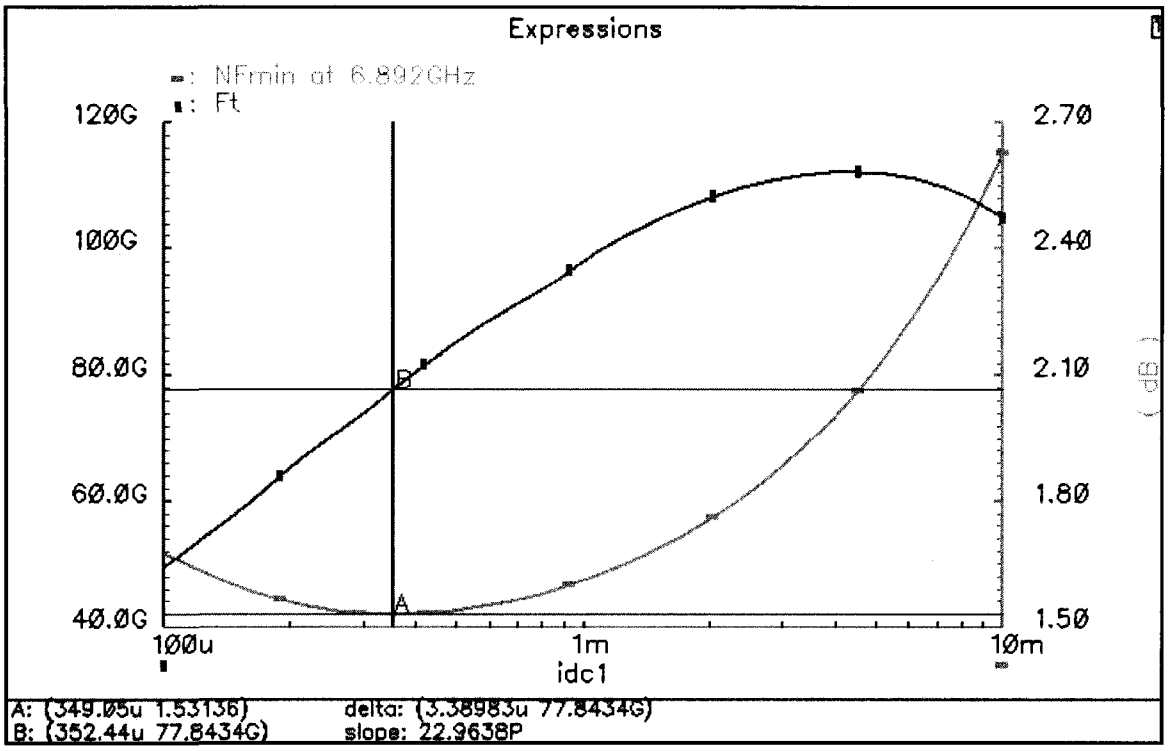


Figure A.3: Transition frequency (F_t) of the minimum length transistor

Appendix B: Characterization of Passives

In the figures below the Q factors are shown for 4 different inductor layouts. In Table 3 some of the inductor geometries are listed. The reference numbers in column 1 of table 3, line up with the traces in Figure B.1. From this work, it is concluded that fewer turns and wider geometries (wire and diameter) give the best Q factor.

Table 3: Q factors for various inductor configurations

Reference	Wire width	Gap	Diameter	Turns	Q factor at 7GHz
1	5um	5um	115um	3	13.2
2	5um	5um	160um	2	16.8
3	10um	5um	150um	3	14.8
4	10um	5um	190um	2	18.9

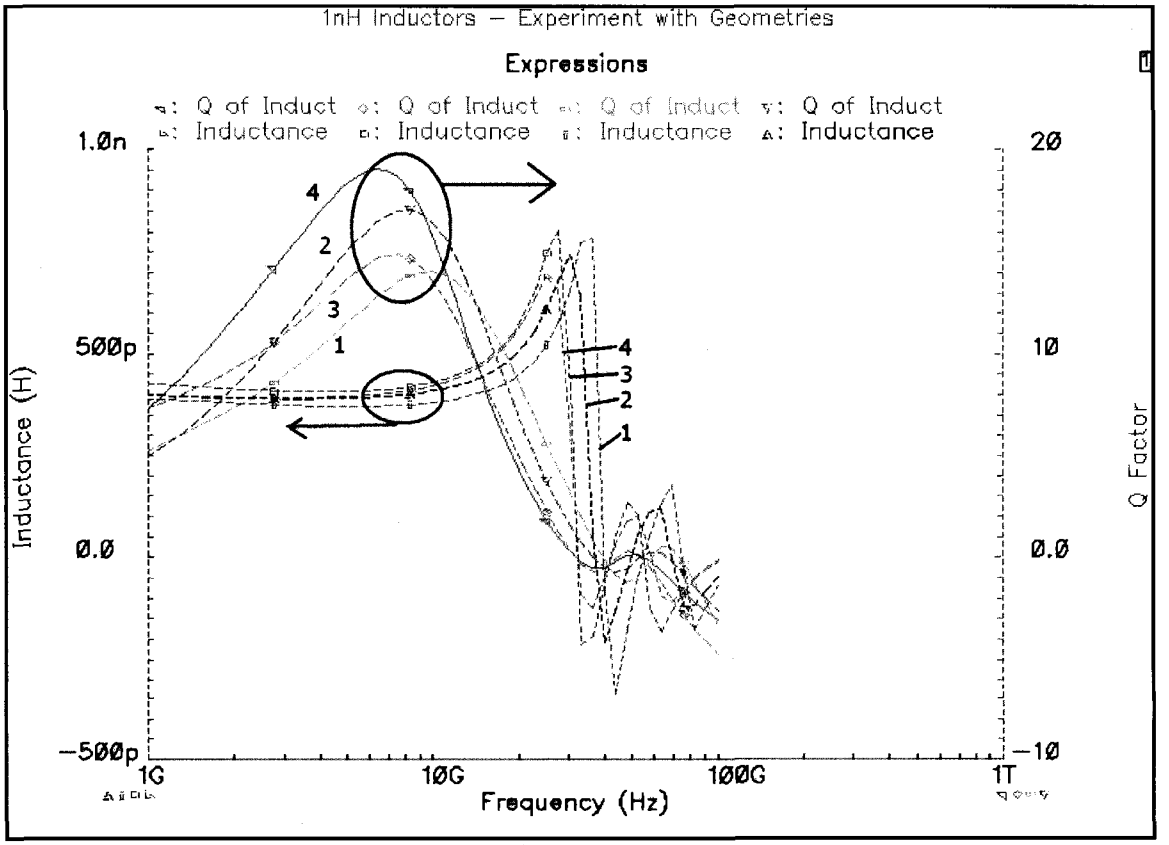
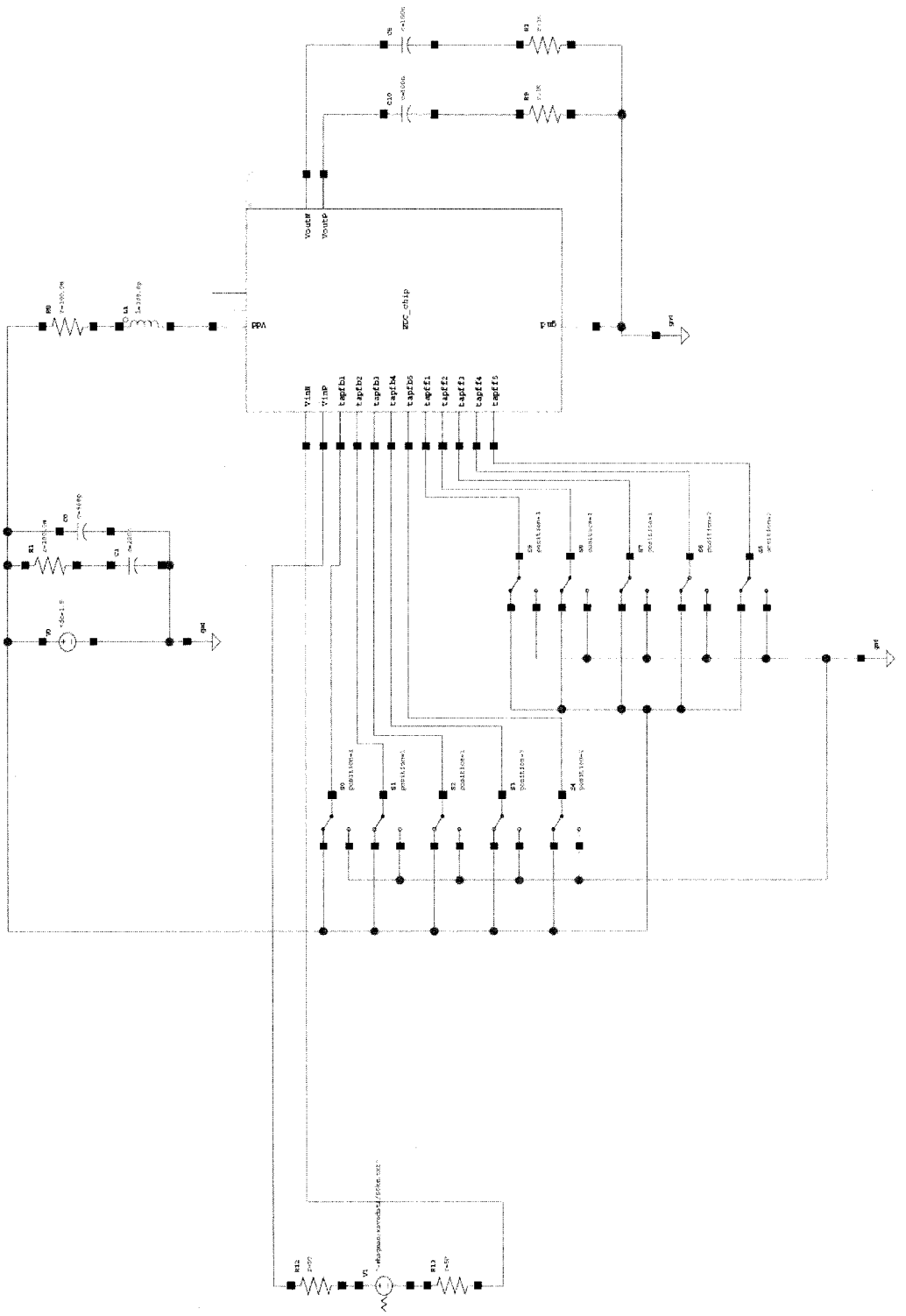


Figure B.1: Experiments on a 1nH inductor - various geometries

Appendix C: Test Bench Used for Simulations



Appendix D: Select MATLAB Code Examples

```
%Matlab code for apply FFE filters to distorted signals (M.
Hagman, Carleton University, 2008)

N = 7;%number of FFE taps
w = [zeros(1,N)]; %Initial conditions
index = (N+1)/2;  %reference tap
w(index) = 1;
tapsp =round(elsperbit);

%need to downsample for LMS optimization.  Note that an .m
file called refsamp was used to find the average edge
position.  This was set up to mimic the loop bandwidth and
response of a CDR.

x = Vout(refsamp+elsperbit/2:tapsp:length(Vout));%Vout is
the dispersed signal from the optical receiver - it is a
vector of voltages for each discrete time.
refsampd = edgefind(Vbk2bk,nts,elsperbit); %Vbk2bk is the
desired signal (no dispersion)
d = Vbk2bk(refsampd+elsperbit/2:tapsp:length(Vbk2bk));
d = filter(w,1,d); %delays the desired signal to force
symmetrical taps.  This makes sure the filter wants to tune
so that the middle tap is the "reference tap". Note that
initial conditions are [0 0 1 0 0] in this case.

w=fliplr(w);%need to flip the coefficients around because
of the order column matrices are treated properly...
%now w elements are backwards...
mu = 0.01;% this is the LMS "mu" parameter.
%LMS FFE tuning loop
for m=1:1000% pattern repeats 1000 times for convergence.
for n = N:length(x)%main loop - for one PRBS 2^11-1 pattern
    err = d(n) - w*x(n-N+1:n)'; %d(n) is the desired signal
                %x(n) is the downsampled dispersed signal.
    if mod(n,2) == 0
        err = 0*err;%opening weight
    else
        err = 1*err;%edge weight
    end
    w = w + mu*err*x(n-N+1:n);
    end
end
w=fliplr(w)%...now they are forwards.
```

```
Blong = [zeros(1,N*tapsp)];% this is done to up sample.
Each tap weight is zero padded so that the FFE filter can
be applied to the chromatic dispersed signal at the 40x
oversampling rate.
for n=1:N
    Blong(tapsp*n+10) = w(n);
end
%This code is used to apply the filter at the native
sampling rate, and store it in a vector "y1"
y1 = filter(Blong,1,Vout);
y1 = y1/sum(Blong);
eyediagram(y1(215:length(y1)),elsperbit*2,200e-12)%plot the
eyediagram.
axis auto
hold off
title(['Simulated Eyediagram with FFE at
',num2str(pspernm(idisper)),'ps/nm' ]);
xlabel('Time (s)');
ylabel('Output Electrical Signal (V)')

%Matlab code for apply DFE filters to distorted signals (M.
Hagman, Carleton University, 2008)

%dfeMH custom DFE Optimizer
%define wdfe as the weight vector
y2 = y1;  %the unfiltered input signal -> note, this must
be a DC cancelled signal - ie mean(y1) = 0.  Note, this
came from the FFE filter.
Ntaps = 3;
wdfe = [1 0 0];

%find edges
refsamp=edgefind(y2,length(y2),elsperbit); %routine to find
average edge position.


fprintf('Pre-DFE optimizer edge position %4.1f',refsamp)
Nbits = round(length(y2)/elsperbit);
%downsample the distorted signal
x = [];
d = [];
x = y2(refsamp+elsperbit/2:elsperbit:length(y2));
ERlinear = 10^(er/10);
modamp = Iave*100*(ERlinear-1)/(ERlinear+1);%estimate of
the modulation amplitude
```

```
mudfe = 0.0001;
%This is the standard way to optimize a DFE filter using
decision-directed methods.  Note that wdfe(1) is actually
the gain of the filter, "modamp" is the amplitude out of
the slicer - this is important.
d(1:Ntaps)=modamp*sign(x(1:Ntaps));
for m=1:20
x = y2(refsamp+elsperbit/2:elsperbit:length(y2));
for n = Ntaps:length(x)
    x(n) = x(n) + wdfe(2)*d(n-1) + wdfe(3)*d(n-2);
    d(n) = wdfe(1)*modamp*sign(x(n));
    err = d(n) - x(n);
    wdfe(1) = wdfe(1) - mudfe*sign(err)*sign(d(n));
    wdfe(2) = wdfe(2) + mudfe*sign(err)*sign(d(n-1));
    wdfe(3) = wdfe(3) + mudfe*sign(err)*sign(d(n-2));
end
end
wdfe
```

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