10-Gb/s CMOS Clock Recovery Circuit Building Blocks Using Dual Substrate Technique

by

Zoe W.Y. Hui, B.A.Sc., UBC

A thesis submitted to the Faculty of Graduate Studies and Research in partial fulfillment
of the requirements for the degree of

Master of Applied Science

in

Electrical and Computer Engineering

Ottawa-Carleton Institute for Electrical Engineering
Department of Electronics
Carleton University
Ottawa, Canada
January, 2004

© Copyright Z.W.Y.Hui 2004

National Library
of Canada

Bibliothèque nationale
du Canada

Acquisitions and
Bibliographic Services

Acquisitions et
services bibliographiques

395 Wellington Street
Ottawa ON K1A 0N4
Canada

395, rue Wellington
Ottawa ON K1A 0N4
Canada

Your file Votre référence

ISBN: 0-612-89844-X

Our file Notre référence

ISBN: 0-612-89844-X

The author has granted a non-exclusive licence allowing the National Library of Canada to reproduce, loan, distribute or sell copies of this thesis in microform, paper or electronic formats.

L'auteur a accordé une licence non exclusive permettant à la Bibliothèque nationale du Canada de reproduire, prêter, distribuer ou vendre des copies de cette thèse sous la forme de microfiche/film, de reproduction sur papier ou sur format électronique.

The author retains ownership of the copyright in this thesis. Neither the thesis nor substantial extracts from it may be printed or otherwise reproduced without the author's permission.

L'auteur conserve la propriété du droit d'auteur qui protège cette thèse. Ni la thèse ni des extraits substantiels de celle-ci ne doivent être imprimés ou autrement reproduits sans son autorisation.

In compliance with the Canadian Privacy Act some supporting forms may have been removed from this dissertation.

Conformément à la loi canadienne sur la protection de la vie privée, quelques formulaires secondaires ont été enlevés de ce manuscrit.

While these forms may be included in the document page count, their removal does not represent any loss of content from the dissertation.

Bien que ces formulaires aient inclus dans la pagination, il n'y aura aucun contenu manquant.

Canada

The information used in this thesis comes in part from the research program of Dr. T. A. Kwasniewski and his associates in the VLSI in Communications group. The research results appearing in this thesis represent an integral part of the ongoing research program. All research results in this thesis including tables, graphs and figures but excluding the narrative portions of the thesis are effectively incorporated into the research program and can be used by Dr. Kwasniewski and his associates for education and research purposes, including publication in the open literature with the appropriate credits. Matters of intellectual property may be pursued collaboratively with Carleton University and Dr. Kwasniewski where and as appropriate.

Abstract

In this thesis, design techniques for the phase-locked loop, phase detector and voltage controlled oscillator for clock and data recovery applications are studied.

A full-rate CMOS phase detector and the associated voltage controlled oscillator for Synchronous Optical Network (SONET) OC-192 systems were designed, implemented and tested. The two devices, implemented using a 0.18 μ m CMOS technology, consumed 14.9mW and 24.2mW respectively from a ± 1.6 V power supply. The power consumption of the output drivers is not included in this calculation.

A new dual-substrate technique was used to overcome the small rail-to-rail supply voltage headroom problem that is characteristic of short channel length technology. The measurement and simulation results showed that the performances of the sample-and-hold phase detector (with 10-Gb/s NRZ data) and the 10-GHz complementary LC voltage controlled oscillator are superior compared to other reported designs employing existing technologies such as GaAs and SiGe.

The feasibility of substituting a digital CMOS process for those technologies traditionally used in high speed mixed-signal System-On-Chip (SOC) systems has been demonstrated.

Acknowledgements

I would like to thank Professor Tad A. Kwasniewski, my supervisor, for his guidance and encouragement during my studies. His enthusiasm and curiosity in understanding how everything works have inspired me in many ways.

I would also like to thank Dr. Stephane Dallaire for his technical advices and friendship. His valuable help in testing the chips is highly appreciated.

The technical support and fabrication funding provided by CMC is gratefully acknowledged. Support from Bob Stevenson, Hui Xu and Jim Quinn are gratified.

Special thanks go to the people I met from Nortel, SiGe Semiconductor, Carleton, UBC, Bridge Camp and by other means, especially Wei An, Morgan Richmond, Professor John Knight, Fred Ma, Bob Lamont, Karen, Kenny, Volney and Wilson. Finally, I would like to thank my parents for their unconditional love and for always giving me the best they can provide.

Table of Contents

Abstract.....	iv
Acknowledgements	v
Table of Contents	vi
List of Figures and Tables.....	viii
Glossary	xi
Chapter 1: Introduction	1
1.1 Thesis Objectives	1
1.2 Thesis Outline	3
Chapter 2. PLL Overview	4
2.1 Basic PLL Structure	4
2.1.1 First-Order Type-I PLL	7
2.1.2 Second-Order Type-I PLL	9
2.1.3 Second-Order Type-I PLL With Phase Lead Correction	10
2.1.4 Type-II PLL	12
2.2 PLL Architectures	13
2.2.1 Full-Rate PLL Architecture.....	13
2.2.2 Integer-N Architecture	14
2.2.3 Fractional-N PLL.....	15
2.2.4 Sigma-Delta Modulation	16
2.2.5 Dual-Loop PLL	17
2.3 Design Issues	18
2.3.1 Phase Noise	19
2.3.2 Spur and Sideband Suppression.....	19
2.3.3 Settling Time	20
2.3.4 Acquisition Range.....	21
2.3.5 Jitter Accumulation	22
2.4 Conclusion.....	23
Chapter 3. Clock Recovery Circuit Building Blocks Overview	24
3.1 Phase Detectors.....	24
3.1.1 PD For Clock And RZ Data Signals	25
3.1.1.1 XOR PD (Gilbert Cell Mixer)	25
3.1.1.2 Two-State PD (R-S Latch)	27
3.1.1.3 Three-State PD (Phase Frequency Detector)	28
3.1.2 PD For NRZ Data	29
3.1.2.1 NRZ To RZ Data Conversion.....	30
3.1.2.2 Linear PD.....	32
3.1.2.2.1 Hogge PD.....	32
3.1.2.2.1.1 D Flip Flop	35
3.1.2.2.1.2 XOR	39
3.1.2.2.2 Conventional Sample-and-Hold PD	40
3.1.2.3 Non-linear PD.....	41
3.1.2.3.1 Conventional Bang-Bang PD	42
3.1.2.3.2 Modified Bang-Bang PD	43
3.1.2.3.3 Simplified Bang-Bang PD	45
3.1.3 Conclusion	47

3.2 Voltage-Controlled Oscillators.....	48
3.2.1 Resonatorless VCOs	48
3.2.1.1 Ring Oscillators	48
3.2.1.1.1 Three-Stage Ring Oscillator.....	49
3.2.1.1.2 Two-Stage Ring Oscillator	51
3.2.1.1.3 Coupled Two-Stage Ring Oscillator.....	54
3.2.1.2 Relaxation Oscillator	55
3.2.2 LC Oscillators	56
3.2.2.1 Passive Dividers (Colpitts and Hartley Oscillators)	57
3.2.2.2 Negative-Gm Oscillator.....	60
3.2.2.3 Phase Noise	61
3.2.3 Conclusion	69
Chapter 4: Design Methodology and Implementation	70
4.1 Dual-Substrate Technique.....	70
4.2 Sample-and-Hold Phase Detector	72
4.2.1 Design Methodology	72
4.2.2 Implementation.....	74
4.2.3 Floorplan and Layout.....	78
4.3 Complementary LC VCO	79
4.3.1 Design Methodology	79
4.3.1.1 Varactor Design.....	81
4.3.1.2 Inductor Design	82
4.3.2 Implementation.....	83
4.3.3 Floorplan and Layout.....	89
4.4 Driver Circuits.....	90
Chapter 5: Measurement Results.....	92
5.1 Phase Detector	92
5.2 VCO	97
5.2.1 Probe Damages.....	98
5.2.2 Melting of Gate Oxide	98
5.2.3 Inductor Pi Model Inaccuracy.....	99
5.2.4 Parasitic Resistances of Metal Lines	101
Chapter 6: Conclusion.....	102
6.1 Summary of Contributions	102
6.2 Future Work.....	104
6.2.1 VCO	104
6.2.2 Clock Recovery Circuits.....	105
Appendix A. Device Characteristics	106
Appendix B. Phase Detector Schematics and Testbench	108
Appendix C. VCO Schematics and Testbenches	113
Appendix D. VCO Open Loop Gain AC Simulation Schematic and Testbench	118
References.....	121

List of Figures and Tables

Figure 1.1: Clock and Data Recovery Block in OC-192 System	2
Figure 2.1: Basic Phase-Locked Loop	4
Figure 2.2: Characteristics of (a) PD and (b) VCO.....	6
Table 2.1: Polarities of Filter with Respect to the Slopes of the Characteristics of PD and VCO.....	6
Figure 2.3: First-Order PLL Filter Circuit and Bode Plots [4]	8
Figure 2.4: Second-Order PLL Filter Design and Bode Plots [5].....	9
Figure 2.5: Second-Order PLL With Phase Lead Correction Filter Designs and Bode Plots [5].....	10
Figure 2.6: Charge-Pump PLL [5]	12
Figure 2.7: Integer-N PLL [7].....	14
Figure 2.8: Fractional-N PLL Using a Dual-Modulus Divider [7].....	15
Figure 2.9: Noise Shaping in PLL by a Sigma-Delta Modulator [7]	16
Figure 2.10: Dual-Loop PLLs (a) Series Structure (b) Parallel Structure with SSB Mixer Outside the Loop (c) Parallel Structure with SSB Mixer Inside the Loop [7]	17
Figure 2.11: Phase Noise Power Spectrum	19
Figure 2.12: Carrier Signal With Sidebands in Frequency Spectrum.....	20
Figure 3.1: Clock Recovery on Clock and RZ Data Signals	25
Figure 3.2: XOR PD (a) Symbol (b) Waveforms (c) Characteristic.....	26
Figure 3.3: Gilbert Cell Mixer	26
Figure 3.4: Two-State PD (a) State Diagram (b) RS-Latch Implementation (c) Waveforms (d) Characteristic	27
Figure 3.5: Three-State PD (a) State Diagram (b) A Possible Implementation (c) Waveforms (d) Characteristic	28
Figure 3.6: Clock Recovery on NRZ Data	30
Figure 3.7: NRZ to RZ Data Conversion (a) Using Delay Cell and XOR (b) Using Differentiator and Squaring Circuit.....	31
Figure 3.8: Hogge Phase Detector [12].....	32
Figure 3.9: Hogge PD Waveforms [13]	33
Figure 3.10: Conversion Characteristic of the Hogge PD.....	34
Figure 3.11: Edge-Triggered D Flip Flop (a) Static Logic Circuit [15] (b) Dynamic Logic Circuit [16].....	36
Figure 3.12: Improved TSPC Dynamic D Flip Flop [17]	37
Figure 3.13: Differential CML (a) DFF (b) Implementation of Each Latch [7].....	38
Figure 3.14: 4-Transistor XOR Gate [20]	39
Figure 3.15: Conventional Sample-and-Hold PD (a) Circuit Concept (b) Waveforms [21]	40
Figure 3.16: Conventional Bang-Bang PD (a) Circuit Concept (b) PD Characteristics (c) Summary Table [24].....	42
Figure 3.17: Modified Bang-Bang PD (a) Schematic (b) PD Characteristics (c) Summary Table [26].....	44
Figure 3.18: Simplified Bang-Bang Phase Detector [27].....	46
Table 3.1: Performance Summary of Hogge, S&H and Bang-Bang PDs.....	47

Figure 3.19: (a) Ring Oscillator Feedback System (b) Ring Oscillator Circuit [7].....	49
Figure 3.20: (a) Linearized model of a three-stage ring oscillator (b) A simple implementation of one stage [25].....	49
Figure 3.21 (a) Varying the load impedance (b) Varying the bias current (c) Varying the delay [27]	50
Figure 3.22: (a) Linearized model of a two-stage ring oscillator (b) A simple implementation [25]	52
Figure 3.23: An implementation of a two-stage ring oscillator with an inductive load [27]	52
Figure 3.24: Linearized model of a coupled two-stage ring oscillator [25].....	54
Figure 3.25: (a) Circuit concept of the relaxation oscillator [28] (b) A simple implementation [7]	55
Figure 3.26: Frequency Selective Feedback System [7].....	56
Figure 3.27: LC Oscillator With One Active Device [7]	57
Figure 3.28: Common Base Approach: (a) Colpitts Oscillator (b) Hartley Oscillator [7]	58
Figure 3.29: Common Collector Approach: (a) Colpitts Oscillator (b) Hartley Oscillator [29]	58
Figure 3.30: Differential Approach: (a) Colpitts Oscillators (b) Hartley Oscillators [29]	59
Figure 3.31: Negative-Gm Oscillator: (a) Single-Ended (b) Differential [7].....	60
Figure 3.32: Noise Impulse Injected at (a) Peak of Waveform (b) Zero Crossing Point of Waveform [30].....	64
Figure 3.33: Phase Noise Spectrum of Linear Time-Invariant Equations [30].....	66
Figure 3.34: Up and Down Frequency Conversion of Noise into the Carrier Region [30]	67
Table 3.2: Performance Summary of Ring and LC Oscillators.....	69
Figure 4.1: Cross-Section View of Silicon with Deep NWELL Feature.....	71
Figure 4.2: Sample-and-Hold Phase Detector Circuit Structure	72
Figure 4.3: 10-Gb/s Sample-and-Hold Phase Detector Schematic [23].....	73
Figure 4.4: Phase Detector Post-Layout Transient Response.....	75
Figure 4.5: Phase Detector Post-Layout Characteristic	77
Figure 4.6: Floorplan and Layout of PD	78
Figure 4.7: Complementary LC VCO Circuit Concept.....	80
Figure 4.8: 10-GHz Complementary LC VCO [36]	80
Figure 4.9: Substrate Cross-Section View of an Inversion Mode PMOS Varactor [37]81	
Figure 4.10: S-Parameter Analysis of an Inversion Mode PMOS Varactor	83
Figure 4.11: VCO Steady State Response.....	85
Figure 4.12: VCO Post-Layout Tuning Range	86
Figure 4.13: Phase Noise of VCO at 1-MHz Frequency Offset with Various Control Voltages	87
Figure 4.14: Phase Noise of VCO vs. Control Voltage	88
Figure 4.15: Floorplan and Layout of VCO	89
Figure 4.16: Buffer Driver Structure For PD and VCO.....	90
Figure 5.1: Phase Detector Measurement Setup.....	92
Figure 5.2: Phase Detector Die Photograph.	93

Figure 5.3: Input Clock and Data Signals Waveforms on Oscilloscope.....	94
Figure 5.4: Output Signals of the Phase Detector.....	94
Figure 5.5: Phase Detector Characteristic with Simulated and Measured Results.	95
Figure 5.6: VCO Measurement Setup.	97
Figure 5.7: VCO Die Photograph.	98
Figure 5.8: Open Loop Gain AC Simulation Result With $R_0 = 1.07 \, \Omega$	100
Figure 5.9: Open Loop Gain AC Simulation Result With $R_0 = 1.3 \, \Omega$	100
Table 6.1: Comparison of Performances With Other PD Designs For CDR Applications	102
Table 6.2: Comparison of Performance With Others VCO Designs	103

Glossary

BERT	Bit Error Rate Test
CDR	Clock and Data Recovery
CMC	Canadian Microelectronics Corporation
CMFB	Common-Mode Feedback
CML	Current-Mode Logic
CP	Charge Pump
CPPLL	Charge-Pump Phase-Locked Loop
CRC	Clock Recovery Circuit
DFF	D Flip Flop
DLL	Delay-Locked Loop
DNW	Deep N-Well
EM	Electro Migration
f_t	Transition Frequency
FRPLL	Full-Rate Phase-Locked Loop
GaAs	Galium Arsenide
HRPLL	Half-Rate Phase-Locked Loop
IEEE	Institute of Electrical and Electronics Engineers
ISF	Impulse Sensitivity Function
ISI	Inter-Symbol Interference
LAN	Local Area Networks
LF	Loop Filter
LPF	Low Pass Filter
LTI	Linear Time-Invariant
NRZ	Non-Return to Zero
NW	N-Well
OLG	Open Loop Gain
PD	Phase Detector
PLL	Phase-Locked Loop
P-SUB	P-Substrate
PW	P-Well
Q-point	Quiescent Operating Point
QPD	Quadrature Phase Detector
RZ	Return to Zero
S&H	Sample-and-Hold
SiGe	Silicon Germanium
SNR	Signal to Noise Ratio
SOC	System-On-Chip
SONET	Synchronous Optical Network
SSB	Single-Sideband
TSPC	True Single-Phase Clocking
UIp-p	Unit Interval Peak to Peak
VCDL	Voltage Controlled Delay Line
VCO	Voltage-Controlled Oscillator
WAN	Wide Area Networks

Chapter 1: Introduction

Bandwidth demand in wide area networks (WAN) and local area networks (LAN) is growing quickly because of the proliferation of applications such as full-motion video, multimedia, e-commerce, and advanced digital services. This exponentially-growing need for bandwidth is placing a huge demand on the internet. Current generation Ethernet LANs are being deployed with 10/100-Mb/s connections to the desktop and 1-Gb/s on the WANs. Next generation networks will have 1-Gb/s to the desktop with 10-Gb/s backbones. This trend has stimulated research on high speed, low-cost and low-power integrated fiber-optic transmitters and receivers.

1.1 Thesis Objectives

A most challenging task is the design of the Clock and Data Recovery (CDR) block in the receiver of a gigabit optical communication system. Figure 1.1 shows a conventional Phase-Locked Loop (PLL) used as the clock recovery circuit in an OC-192 system. Here, a 10-GHz clock signal is recovered from a 10-Gb/s Non-Return to Zero (NRZ) data signal. The recovered clock is then used for synchronous data signal regeneration. In this thesis, critical clock recovery building blocks for 10-Gb/s data rate applications are developed with CMOS technology.

Figure 1.1: Clock and Data Recovery Block in OC-192 System

In CDR, the Phase Detector (PD) is a critical module that directly affects the structure and performance of the CDR. The difficulty lies in the fact that comparing the phase difference of a 10-GHz clock and a 10-Gb/s data signal severely challenges the speed capability of CMOS technology. Compared to other technologies, CMOS devices have relatively low Transition Frequencies (f_t) (and therefore relatively high Inter-Symbol Interference (ISI)). For instance, 0.25- μm SiGe offers a f_t of 47-GHz and 0.18- μm CMOS offers a f_t of only 23-GHz. In order to achieve very high-speed phase detection, PDs have been traditionally designed using GaAs or SiGe, or else a CDR using a half-rate structure or a frequency divider might be used. However, these designs suffer from high power consumption [1], and poor jitter performance with slow settling time [2], respectively.

The objective of this thesis is to establish a technology replacement for GaAs or SiGe by using a standard digital CMOS process in very high speed mixed signal SOC designs.

In this thesis, a full-rate 10-Gb/s CMOS phase detector with extremely low power consumption is presented. To the author's knowledge, no reviews of this type of circuit

have been published at the time of submission to fabrication [3]. Finally, a 10-GHz Voltage-Controlled Oscillator (VCO) implemented with the same 0.18- μm CMOS technology will be discussed in this thesis.

1.2 Thesis Outline

Chapter 2 of this thesis gives an overview of PLL architecture and Chapter 3 continues on with overviews of PD and VCO circuit structures. Chapter 4 describes the design methodologies and the implementations of the circuit building blocks. Measurement results are presented in Chapter 5. Finally, Chapter 6 summarizes the thesis.

Chapter 2. PLL Overview

A PLL is a negative feedback system that locks the phase and frequency of an internal VCO to the input signal – its use leads to a high degree of noise immunity in communication circuits. PLLs have applications in the following areas:

- Carrier, clock and code synchronization and regeneration
- Frequency synthesis and frequency translation
- Narrowband tracking filters
- FM modulation/demodulation and AM detection

PLLs can be classified into different types and orders. The type represents the number of integrators in the forward path and the order identifies the number of poles in the closed-loop transfer function. An overview of the PLL structures, architectures and design issues will be presented in this chapter.

2.1 Basic PLL Structure

A PLL consists of three major blocks: a Phase Detector (PD), a Loop Filter (LF) and a Voltage-Controlled Oscillator (VCO). Figure 2.1 shows the basic PLL structure.

Figure 2.1: Basic Phase-Locked Loop

An ideal PD produces an error signal, V_e , whose average value is linearly proportional to the phase difference between the two input signals, V_i and V_o :

$$V_i(t) = A_i \cos(\omega_i t + \phi_i(t)) \quad (2.1)$$

$$V_o(t) = A_o \cos(\omega_o t + \phi_o(t)) \quad (2.2)$$

For a multiplier PD, the PD output is the product of V_i and V_o , a product which can be written as a combination of sum and difference terms:

$$V_i(t) \cdot V_o(t) = A_i A_o \cos(\omega_i t + \phi_i(t)) \cos(\omega_o t + \phi_o(t)) \quad (2.3)$$

$$= \frac{A_i A_o}{2} \{ \cos[(\omega_i - \omega_o)t + (\phi_i - \phi_o)] + \cos[(\omega_i + \omega_o)t + (\phi_i + \phi_o)] \} \quad (2.4)$$

The LF removes the sum-frequency term, leaving:

$$V_C(t) = B \cos[(\omega_i - \omega_o)t + (\phi_i - \phi_o)] \quad (2.5)$$

B is the amplitude of the control signal. At this point, it is assumed that the loop is locked or nearly locked, so that the frequency difference is zero, and the phase difference is small. The LF output is then:

$$V_C(t) = B \cos(\phi_i - \phi_o) = B \cos(\Delta\phi) \cong B(1 - \frac{\Delta\phi^2}{2}) \quad (2.6)$$

which can be assumed as a linear function when the phase difference is very small. As a result, the time averaged error signal produced by the PD becomes:

$$\overline{V_e} = K_{PD}(\phi_i - \phi_o) \quad (2.7)$$

K_{PD} is the gain of the PD and is dependent on the amplitude and duty cycle of the input signals, V_i and V_o . The LF uses the time averaged V_e to generate a control voltage, V_C , which is used to control the VCO frequency. The LF also attenuates the switching noise in the output of the PD which could otherwise modulate the VCO signal, V_o , because of circuit non-linearities. If the phase or frequency difference between V_i and V_o is too large, the LF will remove even the difference term in Equation (2.4) and the loop will fail to lock.

An ideal VCO generates a periodic signal whose output frequency is a linear function of its control voltage, V_c :

$$\omega_o = \omega_{FR} + K_{VCO} V_c \quad (2.8)$$

ω_{FR} is the free running frequency and K_{VCO} is the gain of the oscillator. As phase is the time integral of frequency, the transfer function of the VCO is:

$$H_{VCO}(s) = \frac{\phi_o(s)}{V_c(s)} = \frac{K_{VCO}}{s} \quad (2.9)$$

The VCO output signal, V_o , is fed back to the PD in a negative feedback loop. This negative feedback loop allows excellent noise immunity and stability of the output signal.

The polarity, inverting or non-inverting, of the filter design is important and can cause the loop to fail to lock if connected incorrectly. The proper connection depends on the slopes of the PD and VCO characteristics. Figure 2.2 shows the PD and VCO characteristics with positive slopes.

Figure 2.2: Characteristics of (a) PD and (b) VCO

Table 2.1 below shows the appropriate filter polarities that should be used with respect to the slopes of the PD and VCO characteristics.

Table 2.1: Polarities of Filter with Respect to the Slopes of the Characteristics of PD and VCO

Slope of PD	Polarity of Filter	Slope of VCO
+	Inverting	+
-	Non-inverting	+
+	Non-inverting	-
-	Inverting	-

If the input frequency, ω_i , is decreased, ϕ_i will be a positive quantity as will the phase error V_e . If an inverting filter is used, a positive V_e will lead to a negative V_c , and the VCO output frequency will be reduced - the output signal is tracking the input signal and the PLL will eventually lock. If a non-inverting filter is used, positive V_e will lead to a positive V_c , and the VCO output frequency will be increased. The loop is moving away from a locked condition.

A PLL with one integrator, VCO, in the forward path is called a Type-I PLL. A PLL with two integrators, Charge Pump (CP) and VCO, in the forward path is called a Type-II PLL. The number of poles in a PLL closed-loop transfer function defines the order of the PLL. Different types of PD and VCO will be discussed in detail in Chapter 3 and different PLL structures will be discussed in the rest of this chapter.

2.1.1 First-Order Type-I PLL

A first-order PLL uses a unity gain filter, $F(s) = 1$, which introduces zero degrees of phase shift into the forward path. Such a filter can be a simple attenuator created by a voltage divider where the bandwidth is controlled by the resistor values. This type of PLL contains only one pole - from the VCO. By referring to Equation (2.9), the $\frac{1}{s}$ term of the VCO creates a slope of -20 dB/decade (or -1) in the PLL magnitude and a -90° constant phase shift. Figure 2.3 shows the filter circuit and the corresponding Bode plots.

Figure 2.3: First-Order PLL Filter Circuit and Bode Plots [4]

Since the phase margin of an ideal first-order PLL is always 90° , the loop is unconditionally stable. The transfer function of the loop is easily found to be:

$$H_{PLL}(s) = \frac{K_{PD} K_{VCO}}{s + K_{PD} K_{VCO}} \quad (2.10)$$

Equation (2.7) suggests a definition for the loop phase error:

$$\epsilon = \frac{V_c}{K_{PD}} \quad (2.11)$$

Combining the -3 dB bandwidth obtained from Equation (2.10), $\omega_{-3dB} = K_{PD} K_{VCO}$, with Equation (2.8), one has:

$$\epsilon = \frac{\Delta\omega}{K_{PD} K_{VCO}} \quad (2.12)$$

The product $K_{PD} K_{VCO}$ determines both the loop gain, K , and loop bandwidth, ω_{-3dB} . This lack of flexibility results in a higher loop gain that contributes to a smaller phase error but a larger bandwidth. The added bandwidth could cause the loop to be susceptible to power supply and substrate noise. The solution to this problem is to replace the unity gain filter or attenuator with a RC loop filter.

2.1.2 Second-Order Type-I PLL

The second-order PLL uses a first order filter. Figure 2.4 shows the filter design and the corresponding Bode plots.

Figure 2.4: Second-Order PLL Filter Design and Bode Plots [5]

With $\omega_{LF} = 1/\tau$, the closed-loop transfer function becomes:

$$H(s) = \frac{K_{pd}K_{vco}}{\frac{s^2}{\omega_{LF}^2} + s + K_{pd}K_{vco}} \quad (2.13)$$

The -3 dB bandwidth is $\omega_{-3dB} = \sqrt{\omega_{LF} K_{pd} K_{vco}}$. The magnitude curve of the $\frac{1}{1+s\tau}$ term has a slope of 0 and a phase of 0° at low frequencies, and a slope of -1 and a phase of -90° at high frequencies. As a result, the PLL will have a close to 180° overall phase at the unity gain point. With a phase margin of close to 0° , the loop is prone to instability; therefore, **phase lead** correction is needed to prevent this problem.

2.1.3 Second-Order Type-I PLL With Phase Lead Correction

Lowpass filters and integrators may be used for phase lead correction. Figure 2.5 shows some possible filter designs and their associated Bode plots.

Figure 2.5: Second-Order PLL With Phase Lead Correction Filter Designs and Bode Plots [5]

The closed-loop transfer function of the PLL is:

$$H(s) = \frac{K_{pd}F(s)K_{vco}}{s + K_{pd}F(s)K_{vco}} \quad (2.14)$$

With the addition of a zero, the PLL phase returns back to -90° at high frequencies. The frequency of the zero can be adjusted to obtain a reasonable phase margin (larger than 60°), and loop stability can be guaranteed.

But the LF's attenuation of high-frequency signals is weakened because of the addition of the zero. This can be dealt with by adding a small capacitor from V_C to ground to suppress these high frequency signals. However, this would increase the time delay as well as the settling time. The added capacitor makes the system a third-order PLL.

For real PLL systems, parasitic capacitors within the loop would cause the loop to effectively be of a much higher order than the one designed. These parasitic poles could interfere with lower frequency poles, create stability problems and affect the loop's damping factor and its bandwidth. But usually, the poles created by these capacitors are at relatively very high frequencies and the loop performance can still be analyzed as a second-order one.

Higher-order LFs are often used in PLLs to meet specifications regarding loop bandwidth, gain and phase noise. Systems with more poles allow sharper cut-off characteristics, but are also more difficult to stabilize especially when process and temperature variations are taken into account. In monolithic designs, small resistor and capacitor values are desirable and various LF structures can be used to minimize the passive component area. For instance, the use of a dual-loop filter structure can significantly reduce the capacitor size in silicon [6]. These designs will not be discussed in detail here.

2.1.4 Type-II PLL

With the addition of a Charge Pump (CP), a PLL has two integrators, CP and VCO, in its forward path and is considered a Type-II PLL. The capture range of the PLL is now limited only by the VCO frequency range, and the static phase error of the PD is negligible. Figure 2.6 shows a Charge-Pump PLL (CPPLL).

Figure 2.6: Charge-Pump PLL [5]

Conceptually, a CP produces an average output current, $\overline{I_{CP}}$, which is proportional to the phase difference between the two input signals of the PD, V_i and V_o . A 3-state PD, which will be discussed in detail in Section 3.1.1.3, is used to generate the "up" or "down" currents for charging or discharging the capacitor C_2 . Capacitor C_1 , which is much smaller than C_2 , is used for ripple suppression. The resistor, R , provides a zero to guarantee loop stability.

The PLL can be approximated by a continuous-time system. It is found that [7]:

$$\omega_{-3dB} = \sqrt{\frac{I_{CP}}{2\pi C_2} K_{VCO}} \quad (2.15)$$

$$\zeta = \frac{R}{2} \sqrt{\frac{I_{CP} C_2}{2\pi} K_{VCO}} \quad (2.16)$$

The -3dB bandwidth, ω_{-3dB} , and the damping factor, ζ , can be increased by increasing the charge pump current, I_{CP} , and the gain of the VCO, K_{VCO} ; therefore, the loop bandwidth

and the loop stability can be improved. A disadvantage of the CPPLL is that the CP will introduce spurs to the system. This will be covered again in Section 2.3.

2.2 PLL Architectures

Different PLL architectures were developed to suit the applications of the PLL. Some of these PLL architectures will be discussed below.

2.2.1 Full-Rate PLL Architecture

A Full-Rate PLL (FRPLL) is a PLL without a divider in the feedback path, as shown in Figure 2.1. The FRPLL has the simplest PLL structure and is commonly used in Clock and Data Recovery (CDR) applications.

In a CDR application, the PLL input is a data signal and the PLL output is a clock signal. The PD responds only to the data transitions; therefore, the gain of the PD, K_{PD} , is dependent on the data transition density and does not have a constant value.

Despite the structural simplicity and operational robustness, a full-rate PD is required in the FRPLL. In high speed operations, full-rate PD designs stretch the speed capabilities of many technologies.

2.2.2 Integer-N Architecture

With the addition of a frequency divider in the feedback loop of a PLL, an Integer-N PLL is formed. Figure 2.7 shows the structure of an Integer-N PLL.

Figure 2.7: Integer-N PLL [7]

In this architecture, the output signal is divided by the programmed integer N . The phase of the divided signal is compared to the input phase. The PD can work at much lower speeds, and the PLL's input frequency is correspondingly lower. In high speed CDR applications, Half-Rate PLLs (HRPLLs) are often used. An HRPLL is an Integer-N PLL with a divide-by-two divider (i.e. $N = 2$). In frequency synthesizer applications, channels are selected by changing the value of N .

A disadvantage of using PLLs with frequency dividers is that the cut-off frequency of the Loop Filter (LF), shown in Figure 2.1, will be scaled down by the division ratio, N . Therefore, the settling time of the loop will be increased by a factor N . Various PLL architectures have been used to solve this problem. For instance, switched-capacitor arrays in oscillator designs [8] and V_c voltage enhancement [9] have been used to reduce the settling time. These structures will not be discussed in detail in this overview.

Another disadvantage is that the input frequency must be equal to the channel spacing in this structure, the fact that N is an integer places self-evident restrictions on the PLL input

frequency, loop bandwidth and channel spacing. Moreover, any phase noise introduced with the input signal is multiplied by N , and this can be a significant problem in large division ratio designs. Fractional- N and sigma-delta modulation PLL designs have been developed to solve these problems respectively. These two PLL architectures will be discussed in the next two sections.

2.2.3 Fractional- N PLL

By using a dual-modulus or multi-modulus divider, an effective fractional division ratio can be obtained by changing the modulus periodically. Figure 2.8 shows a dual-modulus divider structure.

Figure 2.8: Fractional- N PLL Using a Dual-Modulus Divider [7]

If the dual-modulus divider has a division ratio of N for X pulses and has a division ratio of $(N+1)$ for Y pulses, the average division ratio is $N + \frac{Y}{X+Y}$.

Since a Fractional- N PLL allows the output frequency to be a fraction of the input frequency, the input frequency can be much greater than the channel spacing. However, it has a "fractional spurs" problem caused by the quantization noise generated by the

switching action between different division ratios. When a fixed division ratio is used, a single quantization frequency component would appear as a noise tone in the frequency spectrum. When a random division ratio is used, a white quantization noise spectrum would be added to the output. A sigma-delta modulator can be used to solve this problem.

2.2.4 Sigma-Delta Modulation

Figure 2.9 shows that the Sigma-Delta Modulator is used to randomize the modulus control in order to suppress spurs.

Figure 2.9: Noise Shaping in PLL by a Sigma-Delta Modulator [7]

After randomization by the modulus control, the average division ratio will still be the desired fractional value. However, the noise spectrum is "noise shaped" – the noise increases in proportion to the frequency. The noise spectrum thus has most of its energy in the high frequency region, energy that can be easily removed by the LF block. Therefore, superior noise performance can be achieved.

2.2.5 Dual-Loop PLL

A fractional division ratio in a PLL can also be obtained when two or more PLLs are used. Figure 2.10 shows three of the commonly used Dual-Loop PLL structures.

Figure 2.10: Dual-Loop PLLs (a) Series Structure (b) Parallel Structure with SSB Mixer Outside the Loop (c) Parallel Structure with SSB Mixer Inside the Loop [7]

The loops can be placed in series with one other or else in parallel to each other with the Single-Sideband (SSB) Mixer outside or inside the loop. The basic idea is to separate the frequency variation into a high frequency loop, PLL_1 , which has a fixed frequency offset and a low frequency loop, PLL_2 , which has a fine tuning frequency variation. The division ratio variation only happens in the low frequency loop.

In (a), PLL_1 is used to generate a reference frequency for PLL_2 . In (b), the frequency output of PLL_1 is added to the frequency output of PLL_2 by a SSB Mixer. The disadvantages of this structure are that both an accurate quadrature SSB Mixer and low harmonic distortion loops are needed for the frequency addition process. In (c), the SSB Mixer is placed in the feedback loop. The advantage is unwanted sidebands generated by the mixer can be suppressed by the LF in the loop. However, this configuration has a longer settling time.

The main advantage of dual-loop over single loop PLLs is that the close-in phase noise of VCO_1 can be suppressed by the wide loop bandwidth in PLL_1 . The phase noise of VCO_2 is insignificant as it operates at a much lower speed. In addition, the division ratios of the dividers can be reduced.

A disadvantage of the dual-loop PLL is the high level of sidebands produced in SSB mixing. Moreover, because of the requirement for a wide tuning range VCO_2 , the channel bandwidth, loop gain and damping factor can be varied substantially. A complicated design with large power consumption is another concern.

2.3 Design Issues

One must consider many issues when designing PLLs. These include phase noise, spur and sideband suppression, settling time, acquisition range and jitter accumulation, all of which will be discussed below.

2.3.1 Phase Noise

Ideally, the output signal, V_o , from the PLL should be a pure monotone signal. But in practice, there will be noise entering with the input signal, V_i , and noise generated internal to the PLL itself, especially by the VCO block. As shown in Figure 2.11, the phase of V_o will fluctuate and skirts of noise around the carrier signal will appear in the frequency domain.

Figure 2.11: Phase Noise Power Spectrum

$S_v(f)$ is the power spectrum of the VCO output voltage (or current). The phase noise at a given frequency offset from the carrier is defined as the ratio between the noise level in a 1-Hz bandwidth at the corresponding frequency offset, f_{offset} , to the carrier power. The phase noise is specified in units of dBc/Hz. The phase noise generated by the PLL itself, specifically that coming from the VCO block, will be studied in detail in Section 3.2.

2.3.2 Spur and Sideband Suppression

The VCO output signal, V_o , can be modulated by some noise signals with fixed frequencies created by switching actions in PLL components, such as the charge pump. These actions will modulate the output signal and two or more tones of fixed frequency offsets, f_{offset} , from the carrier will appear as lower and upper sidebands of the carrier

signal. These tones are called spurs. Spurs cause problems, especially in frequency conversion systems where Signal to Noise Ratio (SNR) can be degraded significantly. As shown in Figure 2.12, spurs are quantified by the ratio of spur power to carrier power in dBc.

Figure 2.12: Carrier Signal With Sidebands in Frequency Spectrum

In order to minimize phase noise and to suppress spurs in the input signal, V_i , a narrow loop bandwidth should be used. However, this would increase the settling time and limit the capture range. On the other hand, wider loop bandwidth would attenuate noise close to the carrier in the VCO. Therefore, design trade-offs have to be made carefully to optimize the performance of the PLL.

2.3.3 Settling Time

A rule of thumb is that the loop bandwidth be limited to one tenth of the reference frequency in order to guarantee stability, to avoid sampling effects in the PD and to minimize the effect of reference feed-through. But larger loop bandwidths that give shorter settling times are desirable, especially in frequency hopping systems. If more channels are to be fit into the frequency spectrum, a smaller step size must be used, one which would lead to a higher level of noise interference.

2.3.4 Acquisition Range

Acquisition range or capture range is the maximum deviation of the input frequency to the free running frequency of the VCO, ω_{FR} , that the loop can lock onto. In monolithic designs, ω_{FR} can vary substantially with temperature and process; therefore, a wide acquisition range is desirable even if the input signal frequency is tightly controlled.

Since the loop gain of a PLL drops as the frequency deviation, $\Delta\omega$, increases, the acquisition range cannot be made arbitrarily wide. The acquisition range, $\Delta\omega_{acq}$, is directly proportional to the loop gain at $\Delta\omega$ which is determined by the LF bandwidth, ω_{LF} , and the loop gain, K [10]:

$$\Delta\omega_{acq} = K_{PD} K_{VCO} |F_{LF}(j\Delta\omega)| \quad (2.17)$$

With the addition of a frequency acquisition block, which will be covered again in Section 3.1, the acquisition range can be increased significantly. The capture range can become independent of K and ω_{LF} , and will be limited only by the VCO oscillation range.

The acquisition range differs from the tracking range in the sense that the tracking range is the range over which the loop can follow an input signal. The loop may not be able to enter the locked state in the tracking range, which is generally larger than the acquisition range. The tracking range is determined only by the linear ranges of the PD and VCO components, provided that the LF characteristic is linear. These linear ranges will be studied again in Chapter 3.

2.3.5 Jitter Accumulation

Jitter stands for waveform period variation and is related to phase noise. The PD, LF, VCO and the input signal all contribute jitter to the output signal, with the VCO and the input signal being the dominant contributors. Since the transfer function of a PLL with respect to its input signal has a low pass characteristic, a narrow loop-bandwidth would mean that the loop will track the input fluctuations less severely, and therefore would reduce the impact of jitter from the input signal. But because the total jitter is made up of the errors in the most recent cycles of oscillation, wider loop-bandwidth would allow faster correction from the PLL. Therefore, wide loop-bandwidth would mean VCO errors can be corrected more quickly. This agrees with the fact that the transfer function of a PLL with respect to its VCO has a high pass characteristic.

Jitter accumulation is mainly caused by the VCO. Due to the feedback loop of the VCO, jitter in one clock period will be passed to the starting point of the next cycle; therefore, jitter will be “accumulated”. Other than using a wider loop-bandwidth, as discussed above, the jitter accumulation problem can be eliminated by using a Delay Locked Loop (DLL). However, DLL suffers from other problems like high spur levels caused by switching actions in the Voltage Controlled Delay Line (VCDL), and is usable only in certain applications where the duty cycle of the output signal is not of great importance [11]. In CDR or cascaded PLL systems, there is an allowable jitter transfer from one loop to another loop. This will be studied again in Section 4.2.2.

2.4 Conclusion

Different types of PLL architectures have been reviewed. Their structures, functionalities, design issues, advantages and disadvantages are studied.

Because of its structural simplicity and operational robustness regardless of the data pattern, the Full-Rate PLL (FRPLL) is selected to be the architecture used in this thesis. PLLs with frequency dividers or half-rate structures require high speed power-consuming divider designs, and they suffer from poor phase noise, poor jitter performance and slow settling time. Therefore, the Half-Rate PLL (HRPLL) is not preferred unless quadrature outputs are required.

The disadvantage of a full-rate PLL lies in the difficulty of designing a full-rate PD. These PDs stretch CMOS capabilities, especially in 10-Gb/s NRZ data PD designs where phase comparison of a 10-GHz clock signal to a 10-Gb/s data signal is required. Nonetheless, a full-rate PD and a 10-GHz VCO will be designed and developed in this thesis.

Chapter 3. Clock Recovery Circuit Building Blocks Overview

Clock recovery is a useful technique that finds applications especially in data communications and disk drives. In many systems, data is transmitted without any timing information, and the clock signal must be recovered from the data signal in order for the data to be synchronized and retrieved at the receiver end. The PLL is commonly used in Clock Recovery Circuits (CRC).

In this chapter, the two blocks responsible for most PLL design challenges, namely the PD and the VCO, will be reviewed. The advantages and disadvantages of different circuit structures will be discussed.

3.1 Phase Detectors

The dynamic performance of a PLL is influenced considerably by the type of its PD. For instance, the phase offset, loop gain and jitter performance of a PLL depend on the PD's properties. Different PD structures will give different phase detection ranges, operating frequency ranges, linearity, dead-zone locations, power consumption and costs (ie. chip area); therefore, the PD type must be selected carefully in light of the applications and specifications of the PLL. In high speed CRC applications, the PD needs to have the capability of handling random Non-Return to Zero (NRZ) data in order to recover the clock signal from the data stream.

In this section, a brief overview of the PDs commonly used for clock and low speed Return to Zero (RZ) data signals will be discussed. Then, a detailed review of the current PD designs used for high speed NRZ data signals will be given.

3.1.1 PD For Clock And RZ Data Signals

Figure 3.1 shows the time and frequency domain characteristics of clock and RZ data signals.

Figure 3.1: Clock Recovery on Clock and RZ Data Signals

Both the clock and RZ data contain spectral components at the clock frequency. Clock recovery operation can be done by filtering the noise around the clock component and locking onto the spectral component with a PLL. The types of PDs used in this area can be separated into three main categories: XOR, Two-State and Three-State PDs.

3.1.1.1 XOR PD (Gilbert Cell Mixer)

Figure 3.2 shows the waveforms and characteristic of an XOR PD.

Figure 3.2: XOR PD (a) Symbol (b) Waveforms (c) Characteristic

When the phase difference between V_i and V_o increases, the phase error, V_e , increases. The phase error reaches its maximum value when the two input signals are 180° out of phase. The XOR gate can be implemented with a Gilbert Cell Mixer. Figure 3.3 shows the schematic of a Gilbert Cell Mixer.

Figure 3.3: Gilbert Cell Mixer

The shape of the PD characteristic is dependent on the input signal amplitudes. If large signal input signals are used (ie. signals with amplitudes much greater than kT/q), a sawtooth characteristic as shown in Figure 3.2(c) will be obtained. But if small signal

input signals are used, a sinusoidal characteristic as discussed in Equation (2.4) will be obtained.

3.1.1.2 Two-State PD (R-S Latch)

Figure 3.4 shows the state diagram, a possible implementation, the waveforms and output characteristic of the two-state PD.

Figure 3.4: Two-State PD (a) State Diagram (b) RS-Latch Implementation (c) Waveforms (d) Characteristic

The PD has two states: the rising edge of V_i pushes V_e to high and the rising edge of V_o pulls V_e to low. Consecutive rising edge transactions at the inputs do not alter the state of the PD. An edge-triggered RS-latch is one of the possible implementations of the two-state PD.

This type of PD has advantages over the XOR PD in the form of independence from input duty cycle variations (due to the edge-triggered nature of the circuit) and broader linear phase detection range. However, a PLL that uses a two state PD can lock onto the

harmonics of its input signal if the VCO frequency range is sufficiently wide or if the input signal spectrum has strong components at the harmonic frequencies [10].

3.1.1.3 Three-State PD (Phase Frequency Detector)

Figure 3.5 shows the state diagram, a possible implementation, the waveforms and characteristic of the three-state PD.

Figure 3.5: Three-State PD (a) State Diagram (b) A Possible Implementation (c) Waveforms (d) Characteristic

A PD having three or more logic states can detect both phase and frequency differences between two input signals, V_i and V_o . The use of this type of PD can lead to substantial improvements in PLL acquisition range and locking speed.

The operation of the PD can be explained as follows: assuming the PD is initially in State 1, a rising edge in V_i will move the circuit to State 2 and a rising edge in V_o will move the circuit to State 3. If the PD is in State 2 or State 3, a rising edge in V_o or V_i

respectively, will move the circuit back to State 1. If $\omega_i > \omega_o$, the PD will toggle between State 1 and 2. Positive pulses will appear at V_{UP} only with $V_{DN} = 0$ (ideally). If $\omega_i < \omega_o$, the PD will toggle between State 1 and 3, and positive pulses will appear at V_{DN} only with $V_{UP} = 0$. If the PD is initially in the wrong state, the higher frequency input will eventually have two transitions in one time interval, this will force the PD to move to the correct state. If $\omega_i = \omega_o$, pulses with widths equal to the phase difference between V_i and V_o will appear at either V_{UP} or V_{DN} , with V_{UP} and V_{DN} never being 'high' simultaneously. Thus, the average value of $V_{UP} - V_{DN}$ is an indication of the frequency and phase differences.

One of the possible implementations of the three-state PD, as shown in Figure 3.5(b), uses two edge-triggered D Flip Flops (DFFs) with an AND gate. A rising edge on V_i will push V_{UP} to high. Subsequent transitions on V_i will be ignored until a rising edge on V_o occurs, where V_{DN} will be pushed to high until the AND gate resets both DFFs. The outputs of the circuit, V_{UP} and V_{DN} , can be used to drive a differential amplifier or charge pump. The total delay through the AND gate and the reset path is important. It has to be large enough to ensure V_{UP} and V_{DN} will be able to reach full logic levels for the elimination of the **dead zone**. However, increasing the reset delay will reduce the phase detection range. Therefore, the delay time must be selected carefully.

The dead zone is a region in the PD characteristic where the gain of the PD decreases as the phase error approaches zero. This is due to speed limitations of the technology in use. The dead zone problem is an issue of all the PDs discussed so far. This issue will be studied again in the Hogge PD section.

3.1.2 PD For NRZ Data

To transmit an equal amount of data, the RZ format requires more transitions than the NRZ format does. Since channel and circuit bandwidth are costly, the NRZ data format is more commonly used in data transmission.

Figure 3.6 shows the time domain waveforms and frequency spectrum of NRZ data.

Figure 3.6: Clock Recovery on NRZ Data

Since the spectrum of the NRZ data does not contain any energy at the data rate, the PD will need to perform a nonlinear operation at the front end to generate some energy at the data rate frequency if the clock is to be recovered. Phase detection can be performed either by transforming the NRZ data to RZ data and then using the PDs discussed in Section 3.1.1, or by using PDs designed specifically for direct NRZ data detection. The latter method allows higher speed performance and is categorized into linear and non-linear PDs. Both methods will be discussed in detail below.

3.1.2.1 NRZ To RZ Data Conversion

Figure 3.7 shows the two most common methods of NRZ to RZ data conversion.

Figure 3.7: NRZ to RZ Data Conversion (a) Using Delay Cell and XOR (b) Using Differentiator and Squaring Circuit

A common means of accomplishing NRZ to RZ data conversion is to sense both the rising and falling edges of the NRZ data. In (a), the input signal, V_{in} , is delayed for half a bit period, T_B . Then, XORing V_{in} with the delayed signal yields an output signal, V_{out} , with a RZ data spectrum. The time domain data content of V_{out} is unimportant in a clock recovery operation since only a spectral component at the bit rate of the NRZ data is required.

In (b), a differentiator is used to produce pulses at the rising and falling edges of V_{in} . A squaring circuit or a full-wave rectifier is then used to convert the negative pulses to positive ones. This method allows higher input data rate than the one in (a).

Another method of NRZ data detection employs flip flops operating at both the rising and falling edges of the data stream. This method will be discussed in detail in the linear and non-linear PD sections.

3.1.2.2 Linear PD

In this section, two types of linear PDs will be discussed: Hogge and conventional Sample-and-Hold PDs.

3.1.2.2.1 Hogge PD

The most widely used linear PD is probably the Hogge PD [12]. Figure 3.8 shows a simple Hogge phase detector structure.

Figure 3.8: Hogge Phase Detector [12]

Here, the clock signal is directly recovered from the NRZ data without using non-linear operations on the data signal such as limiting, differentiation, rectification or filtering. In closed loop, the clock signal is forced to the center of the data eye and the device is inherently self correcting. Figure 3.9 shows the waveforms of the Hogge PD.

Figure 3.9: Hogge PD Waveforms [13]

Phase comparison is done only during clock and data transitions. If the rising edge of the recovered clock is centered in the data eye, the average values of V_a and V_b will be equal. Average values of the digital signals, $\bar{v}_a$ and $\bar{v}_b$, can be obtained by passing the voltages through Low Pass Filters (LPF). If the clock rising edge is lagging the center of the data

eye, $\overline{V_a}$ is higher than $\overline{V_b}$. If the clock rising edge is leading the center of the data eye, $\overline{V_a}$ is lower than $\overline{V_b}$. Since V_b has a constant pulse width under all conditions, the change in $\overline{V_a} - \overline{V_b}$ value is due solely to the variation of the V_a pulse width. The PD characteristic is plotted in Figure 3.10. Here, for a 50% data transition density, the peak voltage level of $\overline{V_a} - \overline{V_b}$ is $V_p = \frac{V_{\max} - V_{\min}}{4}$.

Figure 3.10: Conversion Characteristic of the Hogge PD

There are many advantages and disadvantages of using the Hogge PD in PLL designs. One advantage is the ability to retime and recover the data, which is very important in Clock and Data Recovery (CDR) applications. Another advantage is that the Hogge PD does not have the dead zone problem, as discussed in the Three-State PD section, because the PLL is considered locked when the rising edge of the clock is centered in the data eye. A linear PD characteristic can be obtained even when the phase error approaches zero. Because of the setup and hold time limitations of the DFFs, the PD performance is pushing the speed limit of the technology only when the rising edge of the clock is close to the data transition and away from the center of the data eye, where the phase error is close to -180 or 180 degrees. The non-linearity of PD gain in this region is unimportant in PLL designs.

However, a phase offset exists in the PD characteristic because the input signals of the two XOR gates in Figure 3.8 have different delays. And, like other PDs that require output voltage level averaging for VCO control, the Hogge PD produces a strong ripple component which deteriorates the jitter performance. Furthermore, the PD's performance is sensitive to the clock duty-cycle due to the double edge-triggered action of the circuit.

There are many modified Hogge PDs that overcome these problems. For instance, another DFF (or a multiplexer) can be added between the Data signal and XOR3 in Figure 3.8 to balance the signal delay in order to solve the phase offset problem. The D input of this DFF can be set to high and the Data signal can be connected to the Clock input of the DFF. In [14], the use of a half period delay block between the Data and XOR3 was claimed to have solved the phase offset and noise performance problems. The jitter performance can be improved by using a PD that does not require output voltage level averaging, for instance, a Sample and Hold (S&H) PD. The S&H PD can also be used to solve the clock duty-cycle sensitivity issue. This type of PD will be discussed in detail in the next section.

3.1.2.2.1.1 D Flip Flop

There are many different ways to construct a D Flip Flop (DFF). The most common structures are the master-slave (or level-triggered) and the edge-triggered flip flops [15]. In Hogge PD designs, the edge-triggered type DFF is used. This type of DFF can be constructed by static, dynamic, True Single-Phase Clocking (TSPC) dynamic or differential Current-Mode Logic (CML) topologies. Figure 3.11 shows the basic structures of the static and dynamic edge-triggered DFFs.

Figure 3.11: Edge-Triggered D Flip Flop (a) Static Logic Circuit [15] (b) Dynamic Logic Circuit [16]

In (a), a static DFF is built using 3 sets of cross-coupled gates. The two sets on the left drive the one on the right. Each of the outputs on the left is fed back as an input to the other set. The cross coupling of the gates leads to an unstable positive feedback loop that is responsible for the positive edge-triggered action. The negative edge-triggered DFF needed for DFF2 in Figure 3.8 can be constructed simply by replacing the NAND gates with NOR. However, this type of DFF has a large number of transistors; therefore, it is suitable only for low speed operations where poor noise performance is acceptable.

The basic dynamic logic circuit in (b) is used to overcome these problems. When clk is low, precharging occurs on the transistors on the left and evaluation occurs on the transistors on the right. When clk is high, predischarging occurs on the transistors on the right and evaluation occurs on the transistors on the left. Because of the precharging and predischarging actions and low transistor count, high speed operation with low power consumption can be achieved.

However, since dynamic circuits use parasitic capacitances to store information, charge sharing may result in glitches or even in malfunction. Moreover, the complicated clocking scheme that requires two clocking signals for each rail-to-rail branch results in a clock skew problem [16]. In addition, the output node is not precharged in this type of structure. For instance, after discharging the output of the DFF, the output node is not charged back to its original level. Last but not least, improvement on the drivability of the circuit is needed, and the output signal needs to be restored to full rail voltage level in order to be compatible with the standard static logic family.

High speed dynamic DFF design is a huge topic and extensive research has been done to overcome the problems stated above. For instance, Figure 3.12 shows a type of dynamic DFF using the True Single-Phase Clocking (TSPC) technique [17].

Figure 3.12: Improved TSPC Dynamic D Flip Fop [17]

The use of the TSPC technique allows simplified clock distribution and reduction of clock skew problems. It also solves the charge sharing, lack of precharging and drivability problems of the basic dynamic DFF at the expense of requiring only a slightly larger number of transistors. Therefore, the TSPC Dynamic DFF is commonly used in high speed DFF designs [17].

For operating speeds that are pushing the limits of the technologies, for instance, a gigahertz range design that operates at a speed close to half of the Transition Frequency (f_t), the differential Current-Mode Logic (CML) topology is used. Figure 3.13 shows a differential CML DFF.

Figure 3.13: Differential CML (a) DFF (b) Implementation of Each Latch [7]

A differential CML DFF consists of two latches which sample or hold the differential input signal, V_{in} , at the rising or falling edge of the differential clock signal, CK.

Differential circuits, which improve substrate, common mode and power supply noise rejection, are often used in high performance designs. The current-driven nature of CML circuits inherently has very high speed capability. The speed and power trade-offs can be done by proper sizing of the transistors. However, if a differential CML circuit has an active load, a Common-Mode Feedback (CMFB) circuit is needed to stabilize the common-mode voltage. High speed and large differential signal CMFBs can be challenging designs [18]. Furthermore, CML circuits require larger rail-to-rail supply voltage headroom and may suffer from slew-rate reduction due to poor conduction in

analog switches. But in spite of the design problems mentioned above, the noise immunity and speed capability advantages of differential circuits still makes them a very popular modern high performance design choice [19].

3.1.2.2.1.2 XOR

There are many different designs for the XOR gate that appears in the Hogge PD. Design trade-offs in speed, propagation delay, noise, power consumption and transistor count are done according to the specifications of the PLL. Figure 3.14 shows a 4-transistor XOR design having low power consumption but poor speed performance, large propagation delay and poor drivability.

Figure 3.14: 4-Transistor XOR Gate [20]

For high speed XOR designs, differential CML circuits should be used. For instance, the Gilbert Cell Mixer shown in the XOR PD section, Figure 3.3, has superior speed performance but high power consumption.

3.1.2.2.2 Conventional Sample-and-Hold PD

Another type of linear PD is the conventional Sample-and-Hold (S&H) PD. Figure 3.15 shows the circuit concept and associated waveforms for this type of PD.

Figure 3.15: Conventional Sample-and-Hold PD (a) Circuit Concept (b) Waveforms [21]

This PD operates as follows. The current source, I , continuously charges the ramp capacitor, C_R . At the reference frequency rate, the reference switch, $S1$, discharges C_R , resulting in a sawtooth waveform at the V_R node. When the sample switch, $S2$, is closed,

the ramp voltage, V_R , is transferred to the hold capacitor, C_H . When S2 is opened, C_R is prevented from charge sharing with C_H , and C_H maintains its voltage level until the next sample pulse. The output amplifier isolates C_H from the load. The S&H PD has the same conversion characteristic as does the Hogge PD in Figure 3.10 except that the average output voltage, $\overline{V_O}$, replaces $\overline{V_a} - \overline{V_b}$ on the y-axis.

The advantages of the conventional S&H PD include linear output voltage, very high-speed acquisition and superior jitter performance. However, as shown in [22], pulse generator designs, which are required to produce the reference and sample pulses, are difficult. A reference pulse cannot be too wide as it would reduce the linear range of the ramp voltage, and a sample pulse cannot be too narrow as sufficient time is needed for a current to go through the sample switch to charge up the hold capacitor. In high-speed designs, the pulse generator design often limits the speed capability of the technology. Furthermore, a high-frequency noise component at a multiple of the reference frequency rate may be translated to a lower frequency noise signal in the sampling process; therefore, a high-level noise floor can lead to significant noise appearing in the loop. This last problem can be solved by sampling the data with the generated clock outside of the clock recovery loop as shown in Figure 1.1.

3.1.2.3 Non-linear PD

The Bang-Bang PD [23] (similar to the Alexander PD [24]) is the most widely used non-linear type of PD. In this section, the operations of the conventional, modified and simplified Bang-Bang PDs will be studied.

clock signal is centered in the data eye, its respective pulling pulse will be turned on. For instance, if a clock signal having a phase between those of clk1 and clk2 (i.e. point A) is centered in the data eye, the PD output will be a constant V voltage until a clock signal in another region is centered in the data eye. The operation of the Bang-Bang PD is summarized in (c).

Comparing to the linear PDs, the Bang-Bang PD shown here has the disadvantage of having a non-constant gain. When the loop gets closer to the locked state, the PD gain increases significantly and is not proportional to the phase error. It is interesting to note that at high frequency, the linearity of the Bang-Bang PD improves significantly because of the parasitic capacitances in the circuit.

Another disadvantage of this PD is that it provides only two output states, V and $-V$. A significant amount of ripple on the VCO control line is created in the locked state and the jitter performance of the loop is degraded. A number of modifications have been made to the Bang-Bang structure in attempts to solve these problems. One of these will be discussed in the next section.

3.1.2.3.2 Modified Bang-Bang PD

Figure 3.17 shows one of the Modified Bang-Bang PDs [26].

Figure 3.17: Modified Bang-Bang PD (a) Schematic (b) PD Characteristics (c) Summary Table [26]

In (a), the clock signals, $clk1$, $clk2$, $clk3$, $clk4$ and $clk5$, are obtained by taking signals from successive nodes of a differential four-stage ring oscillator. The phase difference between adjacent clock signals is $\pi/4$. The ‘pulling pulses’, $Pu2$, $Pu1$, $Pd1$ and $Pd2$, are used to control the charge pump whose output ($V_{up} - V_{dn}$) is in turn used to control the VCO.

Part (b) shows that if a clock signal is centered in the data eye, its respective pulling pulse(s) will be turned on. For instance, if clk2 is centered in the data eye, either Pu1 or Pu2 will be high and the charge pump output will be either $V1$ or $V2$. When the loop is locked and clk3 is centered in the data eye, the charge pump output will be either $V1$ or $-V1$. This metastability occurs randomly and the resulting high frequency component will be removed by the loop filter. If a clock signal having a phase between those of clk1 and clk2 (i.e. point A) is centered in the data eye, the charge pump output will be a constant $V2$ voltage until a clock signal in another region is centered in the data eye. The operation of the Bang-Bang PD is summarized in (c). Compared to the traditional Bang-Bang PD, the modified Bang-Bang PD gives better jitter performance at the expense of speed reduction.

3.1.2.3.3 Simplified Bang-Bang PD

A Simplified Bang-Bang PD is capable of very high speed operation. Figure 3.18 illustrates its structure.

Figure 3.18: Simplified Bang-Bang Phase Detector [27]

The Simplified Bang-Bang PD is essentially a DFF type of circuit [27]. The DFF used here is a **level-triggered** FF [15]. For instance, a master and slave FF can be used. Depending on whether the clock is leading or lagging the data, the phase detector output will be in the high or low state respectively. The Simplified Bang-Bang PD has the same characteristic curve as does the Conventional one, Figure 3.16 (b).

Compared to the linear type PD, this non-linear type PD has a very simple structure that allows much higher operating speeds. A simple voltage-to-current converter instead of a complicated tri-state charge pump circuit can be used following the PD. Its simple structure is insensitive to mismatches and therefore can be easily implemented in silicon. But, since a level-triggered FF is used, the PD's performance will be sensitive to the duty cycle of the clock signal.

3.1.3 Conclusion

Different types of PDs for clock recovery and RZ and NRZ data detection were studied in this section. Their circuit structures, functionalities, advantages and disadvantages were investigated. For phase detection of high speed NRZ data in Clock and Data Recovery (CDR) applications, linear and non-linear PDs are the most suitable choices. The advantages and disadvantages of linear and non-linear PDs are summarized in Table 3.1.

	Hogge PD	Sample & Hold PD	Bang-Bang (or Alexander) PD
1. Sensitivity to Clock and Data Duty Cycle	Sensitive	Insensitive	Sensitive
2. Jitter Performance	Reasonable (averaging of pulses creates jitters).	Good (high level noise floor can be filtered).	Poor (large amount of switching create jitters).
3. Self-Centering of Clock to Data Signal	Might have phase offset.	Might have phase offset.	No phase offset problem.
4. Level of Difficulty in Implementation	More components. Challenging design for high speed applications.	Difficult to design and implement glitch generator block.	Fewer components. Easy to implement.

Table 3.1: Performance Summary of Hogge, S&H and Bang-Bang PDs.

For each type of PD circuit, there are many modified versions to deal with its disadvantages. In this thesis, a type of circuit, which combines the advantages and avoids the disadvantages of the linear and non-linear PDs, was selected for development. The detailed design structure will be discussed in Section 4.1.

3.2 Voltage-Controlled Oscillators

The performance of a VCO circuit is described in terms of its spectral purity (or phase noise), frequency tuning range, gain factor and cost. Some of these factors are mutually contradictory; therefore, different design tradeoffs are needed to optimize a circuit for a particular application. There are vast variations on the structure of VCO circuits. They can be categorized into two main categories: resonatorless and LC VCOs.

3.2.1 Resonatorless VCOs

This type of VCO does not contain an LC tank circuit for frequency selection, and therefore, is called 'resonatorless'. According to the oscillation conditions, the resonatorless VCOs can be separated into two main categories: the ring oscillator type, which requires sufficient open loop circuit gain at 180° phase shift in order for oscillation to occur; and the relaxation oscillator type which, by using hysteresis, can oscillate even if the small signal phase shift does not appear to be sufficient. These two types of resonatorless VCOs will be discussed in detail below.

3.2.1.1 Ring Oscillators

The basic structure of the ring oscillator is shown in Figure 3.19. A ring oscillator consists of at least two gain stages in a loop. The number of gain stages can be odd or even number. A differential structure is needed if an even number of gain stages is used so that an inverting configuration can be connected in the feedback loop.

Figure 3.19: (a) Ring Oscillator Feedback System (b) Ring Oscillator Circuit [7]

According to the Barkhausen's criteria [7], in order for oscillation to occur, a ring oscillator must have a unity loop gain and a total delay around the feedback loop which corresponds to a zero or 360° (or 180° if a negative feedback is used) phase shift. There are many different types of ring oscillators. Three different types of ring oscillators are selected and discussed below.

3.2.1.1.1 Three-Stage Ring Oscillator

The most commonly used ring oscillator is the Three-Stage Ring Oscillator. Figure 3.20 shows a linearized model of a three-stage ring oscillator and an implementation of one of its stages.

Figure 3.20: (a) Linearized model of a three-stage ring oscillator (b) A simple implementation of one stage [25]

The open loop transfer function for the three-stage ring oscillator of the figure is:

$$H(j\omega) = \left[\frac{-G_m R}{1 + RCj\omega} \right]^3 \quad (3.1)$$

In order for oscillation to occur, the Barkhausen's criteria require that the gain of each stage must be $G_m = \frac{2}{R}$ at oscillation frequency $\omega = \frac{\sqrt{3}}{RC}$. The circuit oscillates when the open loop phase shift is 180° . This means each stage must contribute a 60° phase shift. There are a few methods to tune the oscillation frequency of the ring oscillator. Figure 3.21 shows three of the commonly used methods.

Figure 3.21 (a) Varying the load impedance (b) Varying the bias current (c) Varying the delay [27]

These three different methods vary the oscillation frequency by altering the delay in the signal path. In (a), voltage-controlled variable resistors or capacitors implemented by FETs are used to control the load impedance. Increasing the load will increase the delay and therefore, reduce the oscillation frequency. In (b), voltage-controlled current source is used to control the tail current. Increasing this current will increase the transistor's transconductance and therefore, reduce the delay and increase the frequency. In (c), two different delay paths, one fast and one slow, are selected depending on the control voltage. More signals passing through the fast path will give a higher oscillation frequency.

As ring oscillator oscillates with a period of $2MT_d$, where M is the number of gain stages and T_d is the delay of each stage with a fanout of one, a smaller number of stages is desirable in high frequency applications. In addition, VCOs with quadrature output signals, such as those used for phase/frequency detection in CRC or quadrature mixing and single-sideband generation in radio communications circuits, are often preferred in current applications [7]. Since an even number of stages in the ring oscillator is needed to produce quadrature outputs, the two-stage ring oscillator has in recent times become a focus of research. However, using fewer stages in ring oscillators could cause difficulty in achieving oscillation due to the reduction in open loop gain at 180° phase shift. These will be discussed in detail in the next section.

3.2.1.1.2 Two-Stage Ring Oscillator

A Two-Stage Ring Oscillator is shown in Figure 3.22 below.

Figure 3.22: (a) Linearized model of a two-stage ring oscillator (b) A simple implementation [25]

The open loop transfer function for the two-stage ring oscillator can be found to be:

$$H(j\omega) = -\left[\frac{-G_m R}{1 + RCj\omega} \right]^2 \quad (3.2)$$

In order for oscillation to occur, the Barkhausen's criteria require that the gain of each stage must be $|G_m| = \omega C$ with $\omega \gg \frac{1}{RC}$. Since the phase shift produced by the transistor transconductance is very small here, an 180° open loop phase shift can only be attained at infinite frequency where the loop gain is zero. Therefore, the above system cannot oscillate unless G_m is a complex number. Figure 3.23 shows a two-stage ring oscillator with a synthetic inductive load that is used to produce a complex transconductance.

Figure 3.23: An implementation of a two-stage ring oscillator with an inductive load [27]

At sufficiently high frequencies, G_m becomes a complex number. With careful selection of the R , C and PMOS device parameters, a synthetic inductive load that can provide enough phase shifts for oscillation to occur can be formed.

The transfer function for one stage or one differential pair is:

$$\frac{V_{out}}{V_{in}} = \frac{-G_m \cdot (1 + RCs)}{G_{m_p} + (C + C_L + \frac{RC}{R_{O_p}})s + RCC_L s^2} \quad (3.3)$$

Where G_{m_p} is the PMOS's transconductance, C_L is the load capacitance (including the drain junction capacitance of the MOS devices, the input capacitances of the next stage and the isolation buffers), and R_{O_p} is the PMOS's output resistance.

The differential pair's transfer function has two poles (ω_{p1} and ω_{p2}) and one zero (ω_0), and whether oscillation occurs depends on their locations.

$$\omega_0 = \frac{-1}{RC} \quad (3.4)$$

$$\omega_{p1} + \omega_{p2} = \frac{C + C_L}{RCC_L} \quad (3.5)$$

In order to get 180° open loop phase shift at the unity gain frequency, the two poles must be located to the left of the zero. Hence, $C < C_L$ must be met. However, the synthetic inductive load creates an LC tank that would attenuate the oscillating signal; therefore, the tuning range and the oscillating frequency of the circuit would be reduced. A coupled two-stage ring oscillator is used to solve these problems.

3.2.1.1.3 Coupled Two-Stage Ring Oscillator

In a Coupled Two-Stage Ring Oscillator, two separate ring oscillators are coupled to one another as shown in Figure 3.24.

Figure 3.24: Linearized model of a coupled two-stage ring oscillator [25]

At the oscillating frequency, a 90° phase shift must occur in each stage. In order to maintain the same degree of phase difference between the coupling and ring inputs, the bottom ring oscillator is 45° phase offset from the top ring. This produces two sets of quadrature outputs. However, because of the addition of a large number of components, this type of ring oscillator can be very noisy. This problem will be covered again at the end of the resonatorless oscillator section.

3.2.1.2 Relaxation Oscillator

A relaxation oscillator is a circuit in which a capacitor is alternately charged and discharged as an internal voltage moves between thresholds. Figure 3.25 shows such a device.

Figure 3.25: (a) Circuit concept of the relaxation oscillator [28] (b) A simple implementation [7]

In (a), when power is applied, the op-amp's output is at the positive supply rail, V_+ . The capacitor starts charging up to $\frac{1}{2}V_+$ at time constant R_1C . When the voltage passes this threshold, the op-amp's output switches to the negative supply rail voltage, V_- . The capacitor starts discharging down to $\frac{1}{2}V_-$ with the same time constant. This cycle repeats indefinitely [28].

In (b), a simple implementation illustrates how hysteresis can produce differential oscillating signals. Values of I1 and I2 will affect both the operating frequency and duty cycle. With a process similar to (a), when power is applied, one of the transistors is turned on because of noise or threshold level inconsistency. When M1 is on, the potential at the source of M1 starts increasing as the capacitor charges through M1. The drain of M1 is pulled down, keeping M2 off. When the voltage passes a certain

threshold, M1 is turned off. Then, M2 is turned on and vice versa. Here, the positive feedback around M1 and M2 allows rapid switching between the capacitor charge and discharge phases [7].

Resonatorless oscillators are simple to implement and can have wide tuning ranges. However, since many noisy active and passive devices are in the signal path, this type of oscillator has poor phase noise performance. Their open loop quality factor,

$$Q \equiv \omega \cdot \frac{\text{energy stored}}{\text{energy lost}} \quad (3.6)$$

is close to unity. Therefore, LC oscillators are used when superior phase noise performance is needed.

3.2.2 LC Oscillators

An LC oscillator can be viewed as a feedback system, as shown in Figure 3.26, with an LC tank used as a frequency selective element.

Figure 3.26: Frequency Selective Feedback System [7]

The gain block, $H(s)$, can be as simple as one active device. Figure 3.27 shows one of the simplest circuit architectures.

Figure 3.27: LC Oscillator With One Active Device [7]

In order for oscillation to occur, a feedback path from the transistor's collector to its emitter is used to satisfy the Barkhausen's criteria (total phase shift around the loop must be zero with gain ≥ 1). Here, an impedance transformer is needed to increase the parallel resistance seen by the tank, R_{parallel} . Without the impedance transformer, the feedback loop would make $R_{\text{parallel}} = 1/g_m$. This small impedance would drastically reduce the Q of the tank, pull the loop gain below unity and prevent oscillation from occurring. Step-down transformers, passive dividers or buffers can be used for the impedance transformation. In monolithic approach, the latter two methods require less chip area, and therefore are preferred. They will be discussed in detail below.

3.2.2.1 Passive Dividers (Colpitts and Hartley Oscillators)

The two most commonly used passive dividers are shown in Figure 3.28

Figure 3.28: Common Base Approach: (a) Colpitts Oscillator (b) Hartley Oscillator [7]

Capacitive or inductive dividers are used for the impedance transformation in Colpitts and Hartley oscillators respectively. $R_{parallel}$ for both circuits are shown above and the two approaches have similar impacts on the Q value. However, the Colpitts oscillator requires only one inductor and is therefore used more frequently in monolithic designs. Both common base and common collector configurations are popular. Figure 3.29 shows the common collector approach.

Figure 3.29: Common Collector Approach: (a) Colpitts Oscillator (b) Hartley Oscillator [29]

Common emitter approach is not often used in monolithic designs because it requires large capacitors and RF chokes. This approach also suffers from the Miller effect since neither the base nor collector is grounded.

Since differential operation rejects undesirable common-mode noise from the substrate and power supply, differential Colpitts and Hartley oscillators are often desirable. Furthermore, differential VCO signals are commonly needed to drive the mixers in RF communication. Figure 3.30 shows the Colpitts and Hartley oscillators in differential common base and common collector forms.

Figure 3.30: Differential Approach: (a) Colpitts Oscillators (b) Hartley Oscillators [29]

The differential structure can be easily derived from the single-ended approach. The basic idea is to identify the nodes that are held at AC ground in the single-ended design, put two single-ended designs side by side, and connect those nodes together forming an axis of symmetry in the middle of the circuit.

One problem with the passive divider approach is that a large ratio of the capacitors or inductors is required in order to significantly improve the Q value of the resonator. Therefore, an active buffer that can be implemented by simply adding a second active device is often used [7].

3.2.2.2 Negative-Gm Oscillator

In order to increase the resistance seen by the tank, a buffer such as an emitter follower can be used in the feedback loop. This is also known as the **negative-Gm oscillator** because the Gm of the tank is cancelled by the negative Gm of the active circuit. Figure 3.31 shows oscillators using active buffers for the impedance transformation.

Figure 3.31: Negative-Gm Oscillator: (a) Single-Ended (b) Differential [7]

Different circuit arrangements can create single-ended or differential circuits. In (a), in order to ensure both transistors (Q_1 and Q_2) have the same DC operating points, the base of Q_1 is connected to V_{cc} . In (b), the differential structure can be formed by cross-coupling the nodes that are connected to the power supply. It is interesting to note that

the impedance looking into the collectors of Q1 and Q2 is $R_{in} = \frac{-2}{g_m}$. Therefore, if $R_{in} = -R_{parallel}$, where $R_{parallel}$ is the parallel resistance of the tank, the circuit oscillates. The negative impedance, R_{in} , must be slightly larger than the series resistance of the tank in order for the oscillation to be self-starting.

3.2.2.3 Phase Noise

In electronic devices, noise is a topic that is still not well understood. In fact, the identification of noise sources is so difficult that Arno Penzias and Robert Wilson of Bell Labs won the 1978 Nobel Prize in Physics by tracking down a noise source of a microwave receiver and successfully showing that the “noise” was actually remnant radiation from the Big Bang.

In this section, different noise sources and their influences on monolithic circuit design will be discussed. In addition, some phase noise equations developed by some well-known authors will be studied.

The various noise sources which have been discovered in monolithic designs are categorized as follows [30]:

(1) **Thermal Noise** manifests itself as a randomly varying current caused by thermally agitated charge carriers in a conductor. This random current can be converted to a random voltage using Ohm's law. The mean square noise voltage is:

$$\overline{e_n^2} = 4kTR \cdot \Delta f \quad (3.7)$$

Where k is the Boltzmann's constant, T is the temperature and R is the resistance value of the device. All resistors generate thermal noise. All FETs have thermal drain current noise that is generated by the resistive behaviour of the device and thermal gate current noise that is generated by the thermal agitation of channel charge. Both drain and gate noise currents are proportional to a device's operating bandwidth and current levels and are inversely proportional to its channel length. In order to reduce thermal noise in short channel length devices, minimum practical drain voltages, which create smaller electric fields and therefore less carrier heating, should be used. The operating temperature of the device should also be kept as low as possible.

(2) **Shot Noise** is a randomly varying current caused by 'hopping' of charge carriers over a potential barrier. The mean square noise current is:

$$\overline{i_n^2} = 2qI_{DC} \cdot \Delta f \quad (3.8)$$

Where q is the electron charge and I_{DC} is the DC current through the device. Shot noise is proportional to the current and operating bandwidth of the device. All nonlinear devices have shot noise. Shot noise exists in the base and collector currents of bipolar transistors and the drain and gate currents of FETs. Since gate current is very small, shot noise is negligible in FETs.

(3) **Flicker Noise** is a randomly varying current caused by phenomena that may or may not have obvious connection to the device itself and that have fluctuations with a $1/f$ characteristic (ie. signals with higher frequencies will have lower noise levels). These phenomena include trapped surface charge carriers, the earth's rotation rate and galactic radiation noise. The mean square noise (either voltage or current) has the following form:

$$\overline{N^2} = \frac{K}{f^n} \cdot \Delta f \quad (3.9)$$

K is device-specific and n is usually close to unity. Resistors exhibit $1/f$ noise when there are DC currents flowing through them. The noise level is inversely proportional to the frequency and directly proportional to the current level. Due to the defects and impurities at the surface or interface of transistors, charge carriers are randomly trapped and released resulting in $1/f$ noise in transistors. MOSFETs, which are surface devices, exhibit much greater $1/f$ noise than bipolar transistors, which are bulk devices. Larger MOSFETs have less $1/f$ noise as larger gate capacitances allow better smoothing effect on the fluctuations of channel charges. In most cases, PMOS devices, which use buried channels, exhibit less $1/f$ noise than NMOS devices do. Furthermore, forward-biased junctions also exhibit $1/f$ noise. As the base-emitter junction in a bipolar transistor is the only one which is forward-biased in all transistor operations, the base current is the only one that exhibits $1/f$ noise due to this cause. In summary, $1/f$ noise can be reduced by minimizing the DC drop across a resistor and by increasing the transistor size.

(4) **Popcorn Noise (or burst noise)** is a type of noise in semiconductors caused by metal ion contamination. Burst noise has a non-Gaussian amplitude distribution because the noise voltage (or current) switches between two or more discrete values at random times. It is difficult to describe this noise as an equation since its characteristics are so variable, to the extent that devices fabricated in exactly the same way can exhibit different amount of burst noise. Meticulous cleanliness during processing is the best way to reduce burst noise.

In oscillator design, the noise sources described above can perturb both the amplitude and phase of the output signal. Because all practical oscillators incorporate amplitude-

limiting mechanisms, amplitude noise is usually negligible in comparison to phase noise. The effect of injected noise on phase noise is illustrated in Figure 3.32.

Figure 3.32: Noise Impulse Injected at (a) Peak of Waveform (b) Zero Crossing Point of Waveform [30]

Phase noise can be explained as the fluctuation of the zero crossing locations of a signal. In (a), noise injected at the peak of the waveform does not result in any phase noise, but in (b), the same noise injected at a zero crossing point (or anywhere near one) of the waveform results in phase noise. As a result, phase noise is a time-varying phenomenon. That is, the resulting phase deviation is dependent on the location of the noise injection. The Impulse Sensitivity Function (ISF) defines the amount of phase deviation as a function of its location within a clock period with respect to noise impulses.

Because the output signal level of a real oscillator is limited by the power supply, the phase noise amplitude is insignificant compared to the carrier signal magnitude. Therefore, it is reasonable for the phase noise to be approximated as a linear function of frequency and to be modelled in a **linear time-varying** format.

Since random signals are involved, the noise corruption of the output spectrum is more easily visualized in the frequency domain than in the time domain. This representation may be obtained by taking the Fourier transform of the time-domain equation. For example, the phase noise equation of an ideal oscillator modelled as a simple **Linear Time-Invariant (LTI)** system is:

$$L(\Delta\omega) = 10 \cdot \log \left[\frac{2kT}{P_{sig}} \cdot \left(\frac{\omega_o}{2Q \cdot \Delta\omega} \right)^2 \right] \quad (3.10)$$

A limitation of this equation is that it accounts only for noise associated with tank loss - noise originating in the $\frac{1}{(\Delta\omega)^2}$ region and noise floor contributions at large frequency offsets are not included.

The **Leeson equation**, Equation (3.11), is a modification made to Equation (3.10) in order to overcome these problems:

$$L(\Delta\omega) = 10 \cdot \log \left\{ \frac{2FkT}{P_{sig}} \cdot \left[1 + \left(\frac{\omega_o}{2Q \cdot \Delta\omega} \right)^2 \right] \cdot \left(1 + \frac{\Delta\omega_{1/f^3}}{|\Delta\omega|} \right) \right\} \quad (3.11)$$

Where P_{sig} is the carrier power; F and $\Delta\omega_{1/f^3}$ are factors determined from measurements. The factor F is used to account for the noise level in the $\frac{1}{(\Delta\omega)^2}$ region. The addition of unity to the $\left(\frac{\omega_o}{2Q \cdot \Delta\omega} \right)^2$ term would account for the noise floor, and the inclusion of the $\left(1 + \frac{\Delta\omega_{1/f^3}}{|\Delta\omega|} \right)$ term would account for the $\frac{1}{(\Delta\omega)^3}$ region. Unfortunately, both the F and $\Delta\omega_{1/f^3}$ parameters must be determined from physical measurements which makes phase noise prediction a difficult task, and the noise floor starting point, $\frac{\omega_o}{2Q}$, is not always true.

The output spectrums of both equations are shown in Figure 3.33.

Figure 3.33: Phase Noise Spectrum of Linear Time-Invariant Equations [30]

Both equations show that the phase noise at a given frequency offset improves (i.e. L decreases) as both carrier power and Q increase.

The **Hajimiri approach** overcomes the limitations of both the simple LTI and Leeson equations by developing the phase noise equation as a **linear time-varying** model. Figure 3.34 illustrates the frequency conversion of noise.

Figure 3.34: Up and Down Frequency Conversion of Noise into the Carrier Region [30]

Here, $N(\omega)$ is the noise spectral density of an arbitrary noise source (voltage or current) injected into an oscillator. $S_\phi(\omega)$ is the power spectrum of the excess phase $\phi(t)$ and is a convolution of $N(\omega)$ and the ISF. $S_v(\omega)$ is the power spectrum of the oscillator output voltage, which is disposed around the carrier. Noise near DC (or $1/f$ device noise) is up-converted and weighted by the ISF coefficient C_0 to become $\frac{1}{f^3}$ noise near the carrier. Noise near the carrier does not get any frequency conversion and is weighted by the ISF coefficient C_1 . Finally, white noise near multiples of the carrier frequency undergoes down-conversion and is weighted by ISF coefficients (C_2, C_3 , etc) to become noise in the $\frac{1}{f^2}$ region.

In [31], Hajimiri presented the noise spectrum in the $\frac{1}{f^3}$ region as:

$$L(\Delta\omega) = 10 \cdot \log \left[\frac{\frac{\overline{i_n^2}}{\Delta f} \cdot c_o^2}{8q_{\max}^2 \cdot \Delta\omega^2} \cdot \frac{\omega_{1/f}}{\Delta\omega} \right] \quad (3.12)$$

and that in the $\frac{1}{f^2}$ region as:

$$L(\Delta\omega) = 10 \cdot \log \left[\frac{\overline{i_n^2} \cdot \Gamma_{rms}^2}{2q_{max}^2 \cdot \Delta\omega^2} \right] \quad (3.13)$$

Where Γ_{rms} is the RMS value of Γ , the Impulse Sensitivity Function (ISF), and q_{max} is the maximum charge displacement across the capacitor.

The Hajimiri model gives new insights into the spectral description of phase noise. The model allows a quantitative estimate of the effect of $1/f$ noise up-conversion on close-in phase noise. The model also allows the modelling of cyclostationary noise sources (ie. noise sources that are varying periodically). Moreover, the $\frac{1}{f^3}$ phase noise corner is found to be $\Delta\omega_{1/f^3} \approx \omega_{1/f} \cdot \left(\frac{C_0}{C_1}\right)^2$. Therefore, reducing C_0 , the DC gain, would reduce the $\frac{1}{f^3}$ phase noise corner.

3.2.3 Conclusion

Different types of LC and ring oscillators have been reviewed. Their circuit structures, functionalities, advantages and disadvantages are investigated. Their advantages and disadvantages are summarized in Table 3.2.

	Ring Oscillator	LC Oscillator
1. Phase Noise Performance	Poor	Superior (contains fewer active and passive components).
2. Oscillating Frequency Control	Coarse control. Dependent on the transistor delay. Large variation in center frequency with respect to power supply, device models and temperature.	Fine control. Controlled by the value of the LC tank. Signals at unwanted frequencies are attenuated.
3. Tuning Range	Large	Small
4. Level of Difficulty in Implementation	Relatively easy.	Extremely accurate inductor models, which are very hard to generate, are needed in high frequency designs.

Table 3.2: Performance Summary of Ring and LC Oscillators.

The structure of the LC VCO developed in this thesis will be discussed in detail in Section 4.2, as will the problems of small tuning range and the difficulty of implementing inductors on chips.

Chapter 4: Design Methodology and Implementation

In this chapter, the circuit structures selected for the PD, VCO and buffer driver will be discussed. The design selections were based on the circuit overview of Chapter 3. The design issues, implementation methods and simulation results of the Sample-and-Hold PD and complementary LC VCO will be discussed here. The complete circuit schematics and testbenches discussed in this chapter are included in Appendices B and C.

As CMOS technology advances to shorter channel lengths for higher speed applications, reduction in transistor breakdown voltages has led to smaller rail-to-rail supply voltages available which makes cascode configurations difficult to implement. Low voltage circuits suffer from poor conduction in analog switches, inaccuracy in low current transistor models, lower SNR [32] and lower operating frequencies [33]. A new “dual-substrate” technique, a method which has not been described before, will be explained in the following section.

4.1 Dual-Substrate Technique

Figure 4.1 shows a cross section view of a dual-substrate configuration that can be implemented with most CMOS technologies.

Figure 4.1: Cross-Section View of Silicon with Deep NWELL Feature.

Here, the P-well (PW) of the NMOS transistor is reverse biased to the surrounding N-well (NW) and Deep N-well (DNW). Likewise, the N-well of the PMOS transistor is reverse biased to the surrounding P-substrate (P-SUB). This raises the supply headroom from 1.6V to 3.2V. The Deep N-well and P-substrate junction is not forward biased unless the P-substrate is pulled up to 0.6V. Therefore, cautious layout, with multiple P+ contacts on the P-substrate, is required in order to avoid its voltage from building up.

For 1.8V devices, the voltages $|V_{gs}|$, $|V_{ds}|$ and $|V_{bs}|$ must always be kept below 1.8V in order to prevent the gate oxide from breaking down. The SpectreRF simulator fails to run when any of these voltages exceed 4.1V. If any of these voltages must exceed 1.8V, then 3.3V devices are used. Here, the voltages $|V_{gs}|$, $|V_{ds}|$ and $|V_{bs}|$ must be kept below 3.3V. One added advantage of the Deep N-well process is that each transistor can be individually isolated so that substrate current or noise is subsided. However, the layout area is slightly increased due to the use of DNW in this technique. This may affect the performance of the circuit if extremely accurate matching is required.

4.2 Sample-and-Hold Phase Detector

The design methodology, circuit implementation and layout issues of the PD chip will be discussed in this section.

4.2.1 Design Methodology

By combining the advantages and avoiding the disadvantages of different types of PD as summarized in Table 3.1, a new type of Sample-and-Hold PD [27] was selected to be developed. The linear characteristics of the Hogge and the conventional S&H PD were combined with the high speed performance of the non-linear Bang-Bang (or Alexander) PD in this new structure. This type of S&H PD differs from the conventional S&H PD in the sense that glitch generation is not required [22]. Figure 4.2 shows the overall functionality of the PD, and Figure 4.3 shows the detailed circuit structure.

Figure 4.2: Sample-and-Hold Phase Detector Circuit Structure

Figure 4.3: 10-Gb/s Sample-and-Hold Phase Detector Schematic [23]

In Figure 4.3, the activation of the master and slave stages is controlled by the input data signals. The differential clock signals are sampled when the master stage is turned on. When the slave stage is turned on, the master stage is turned off and its PMOS transistors work as resistors to prevent the holding capacitors from discharging. The slave branch samples the voltage levels stored in the holding capacitors at this time. When the slave branch is turned off, its PMOS transistors prevent the PD outputs from discharging. The master branch is turned on to sample the next set of clock signals. When the phase offset between the clock and data signals is constant, the PD outputs converge to a finite DC voltage level.

State switching that creates ripple does not occur with this circuit so superior jitter performance of the loop can be expected. The circuit has a very high phase difference resolution; therefore, its dead zone region is negligible and very high-speed phase detection is possible. In other words, this PD has neither the speed limitation problem of

the Hogge PD nor the ripple problem of the Bang-Bang (or Alexander) PD. However, this circuit might suffer from a PD characteristic with a smaller linear range and a phase offset. These issues will be discussed again in the Measurement Results section.

4.2.2 Implementation

The sample-and-hold phase detector was developed in a 0.18- μm CMOS technology. The implementation and post-layout simulation results will be discussed in this section.

The differential clock signal branch of the PD's master block involves the fastest switching operations in the circuit. Appendix A shows the characteristics of the transistors used. A minimum transistor length was selected to permit high frequency operation. The width of the transistor was selected based on the tradeoffs between the PD's gain and linear range. Wider transistors would give a larger gain but smaller linear range and would consume more power. Capacitor size selection is based on the tradeoffs between settling time and output voltage level of the circuit. Smaller capacitors would allow shorter settling times but smaller output voltage ranges.

Since transistors provide smaller common-mode impedances when they are operating in the triode region, the PMOS transistors attached to the capacitors are operating in the triode region to eliminate the need for a common-mode feedback circuit. The differential data signal branch draws twice the amount of current of the master and slave branches. This is because the current mirrors are located at the tail portions of the master and slave branches, but are the differential loads of the data signal branch. The current mirrors are designed accordingly.

Compared to the master branch described above, the differential data signal branch and the slave branch will be operating at much lower speeds, and therefore, the transistor sizes of these devices are less stringent. Transistor sizes were optimized to ensure all transistors were operating in the saturation region. The testbenches and schematics of the PD are shown in Appendix B.

Figure 4.4 shows the transient response of the PD circuit with a 10-GHz clock signal and a 10-Gb/s data signal with a 50% data transition rate (i.e. data altering in a 1010 sequence).

Figure 4.4: Phase Detector Post-Layout Transient Response

Here, $VT("/I31/25")$ and $VT("/I31/26")$ are the differential output voltages of the phase detector circuit. $VT("/buf_out_p")$ and $VT("/buf_out_n")$ are the differential output voltages of the driver block. The output voltage levels can be fine-tuned for testability since the buffer driver has separate VDD and VSS supply pads.

The transient response shows that the PD has a settling time, $PD_{\text{settling_time}}$, of about 80ns. This settling time is needed to obtain the steady state response due to the charging and discharging actions of the ramp and hold capacitors. A 90ns settling time was used to plot the PD characteristic. Thirty different points of phase error between the clock and data signals were simulated. Figure 4.5 shows the resulting waveform.

It is interesting to mention that in a practical SONET OC-192 system, the CDR loop bandwidth should be greater than 4-MHz to meet the jitter tolerance requirement. To avoid interference or sampling effects in the loop filter, the reference frequency ($1/PD_{\text{settling_time}}$) should be much greater than the CDR loop bandwidth. As mentioned in Section 2.3.3, the reference frequency should be at least ten times the loop bandwidth. As a result, $PD_{\text{settling_time}} < 25 \text{ ns}$ should be used.

However, the new Sample-and-Hold PD used here differs from the conventional one in that the former replaces the common PD and LPF blocks of the PLL [34]. The circuit gives a DC output voltage that is directly proportional to the input phase difference, so that filtering is unnecessary. The elimination of the filter simplifies the loop structure and reduces its response time. As a result, interference with the LF is not a concern and the guideline that the reference frequency should be at least ten times the loop bandwidth is unnecessary here. The $PD_{\text{settling_time}}$ for the current design, about 80 ns, is not a problem. The loop performance (especially loop stability, loop acquisition range,

modulation of VCO outputs and effectiveness of filtering input disturbances) should be monitored closely when using this type of PD.

Figure 4.5: Phase Detector Post-Layout Characteristic

Here, PD_pd_out and PD_pd_out_n are the differential output voltages of the phase detector block. PD_buf_out and PD_buf_out_n are the differential output voltages of the driver block. The gain of the PD at 50% data transition rate was found to be $K_{PD} \approx 1.4 \times 10^{11}$ V/s.

Despite the advantages of this type of PD discussed in Section 3.1, the simulation result shows that this type of PD has a linear range of only 30 to 50 percent. According to the SONET OC-192 specification [35], a 0.15 UIp-p (Unit Interval peak to peak) jitter tolerance is required for jitter frequencies up to 4-MHz. In order to accommodate data

misalignment and VCO random jitter, the 30 to 50 percent linear range provided by the PD does not give enough margins for errors. Although this range can be increased by reducing the gain of the master or slave branches or by reducing the clock signal swing level, it is still much smaller than the 60 to 70% linear range provided by a conventional Hogge PD. Besides, reducing the gain will likely pull down the operating frequency of the PD. Fortunately, the measurement results show a very promising linear range and this will be discussed in detail in Section 5.1.

Post-layout simulations involving different supply voltages (± 1.5 , 1.6 and 1.7 V), device models (Best, Typical and Worst) and temperatures (0° , 55° and 125°) were done prior to the design was submitted for fabrication.

4.2.3 Floorplan and Layout

Figure 4.6 shows the floorplan and layout of the PD.

Figure 4.6: Floorplan and Layout of PD

The PD was fabricated in a $0.18\mu\text{m}$ CMOS technology with a pad-limited die area of $1410 \times 1010 \mu\text{m}^2$. The positions of the PD and driver circuits are shown in the floorplan diagram. The layout was designed according to the Electro-Migration (EM) rules and slottings were used on metals wider than $35 \mu\text{m}$. Ground shielding was used to improve the noise immunity of the core circuit. All NMOS transistors were surrounded by N-wells and Deep N-wells as mentioned in Section 4.1. High frequency signal pads were laid out on the M4 to M6 layers, while DC supply pads were laid out on the M1 to M6 layers. The antenna rules were met and the metal fill was done to increase the yield of the chip. A pitch distance of $150 \mu\text{m}$ was used for all pads. The Diva DRC/LVS and Calibre DRC were passed before the submission to fabrication.

4.3 Complementary LC VCO

The design methodology, circuit implementation and layout issues of the VCO chip will be discussed in this section.

4.3.1 Design Methodology

In Section 3.2, the LC VCO was found to be the most suitable for high-speed applications because of its superior phase noise performance and operating frequency accuracy. The complementary LC VCO, which has a structure similar to that of the two-stage ring oscillator with inductive load in Figure 3.23, was selected for development. Figure 4.7 shows the overall VCO design concept and Figure 4.8 shows the detailed circuit structure.

Figure 4.7: Complementary LC VCO Circuit Concept

Figure 4.8: 10-GHz Complementary LC VCO [36]

The parallel resistance created by the inductor is the major source of loss in the LC tank circuit. The cross-coupled NMOS transistors provide a negative resistance of $-2/g_m$ that can cancel out the loss in the LC tank circuit. The cross-coupled PMOS transistors are twice the size of the NMOS ones. This half-circuit symmetry allows a partial correlation of noise that minimizes the up-conversion of $1/f$ noise and therefore leads to improved phase noise performance. The addition of the cross-coupled PMOS transistors changes the negative resistance value to $-1/g_m$; therefore, the transistors are designed such that $1/g_m$ is equal to the parallel resistances created by the inductors. The bridge-like quad transistor structure leads to much greater signal swing and a consequent improvement in output power.

The following two sections address the design considerations of the varactor and inductor components.

4.3.1.1 Varactor Design

Inversion mode PMOS varactors that allow large tuning ranges [37] are used. Figure 4.9 shows a substrate cross-section view of a varactor.

Figure 4.9: Substrate Cross-Section View of an Inversion Mode PMOS Varactor [37]

The varactor is called an inversion mode device because its pn-junctions are reverse biased by connecting the NWELL to the VDD. Since the NWELL and the PMOS drain-source nodes provide an AC ground, the total capacitance of the varactor is $C_{\text{total}} = C_{\text{gs}} + C_{\text{gd}} + C_{\text{depletion_region}}$. Minimizing the parasitic capacitances, C_{gs} and C_{gd} , would allow a larger tuning range; therefore, the physical layout of the varactor is important. Careful layout using parallel short channel width transistors with multiple *via* contacts would minimize the channel and gate parasitic resistances and the Q value of the varactor would be increased. In order to feed in the control voltage, V_{ctrl} , into the differential structure, the gates of the PMOS varactors are connected to the VCO outputs, and the drains and sources are connected to V_{ctrl} .

4.3.1.2 Inductor Design

The definition of the quality factor, Equation (3.6), indicates that Q is inversely proportional to energy lost; therefore, VCO designs with better phase noise performance and lower power consumption can be implemented. In this thesis, octagonal inductors that have large quality factors are used. ASITIC [38] was used to create the inductors, to find their Q values and their pi model parameters. The inductors were protected by guard rings for noise shielding and were created at the top metal layer, Metal 6, which has the lowest sheet resistance value. The radii, widths and spacings of the inductors were optimized for the largest Q value. If the width is too wide, energy (or AC signals) will be lost through the parasitic capacitances between the substrate and inductor metal. If the width is too narrow, the metal resistance, hence loss, is increased. The optimization technique will be discussed in detail in the Implementation Section below. Numerical values will be given.

Since CMC supports only the use of the M6 layer for inductor construction, optimization of the inductor thickness could not be done in this thesis. The M6 layer of thickness 0.99 μm was used to construct the inductors. It is worth mentioning that a thicker inductor would lead to reduced loss due to metal resistance, but increased loss due to parasitic capacitances between the substrate and inductor metal and between the turns of the inductor metal itself.

4.3.2 Implementation

The complementary LC VCO shown in Figure 4.8 was developed in a 0.18- μm CMOS technology. The implementation and post-layout simulation results will be discussed in this section. The testbenches and schematics of the VCO are shown in Appendix C.

PMOS transistors with the shortest length (0.18 μm) and a relatively small width were used to build a high Q value varactor. The S-parameter analysis was used to determine the capacitance range of the varactor. The S-parameter testbench is shown in Figure C.1 of Appendix C. Figure 4.10 below shows the S-parameter analysis of the PMOS varactor.

Figure 4.10: S-Parameter Analysis of an Inversion Mode PMOS Varactor

The capacitance value of the varactor vs. the control voltage is shown. "wavew23sli1" is the imaginary part of the impedance seen at the S-parameter port. As S-parameter port 2 is used here, $Z_{22_{img}} = \frac{1}{sC}$. The capacitance value of the varactor can be written:

$$C = \frac{-1}{\text{"wavew23sli1"} * 2\pi * f}.$$

By using $C = 360$ fF, $L = 0.3$ nH and $\omega = \frac{1}{\sqrt{LC}}$, the oscillation frequency of the VCO is: $f = 15.3$ -GHz. However, it will be shown in the next two diagrams that the actual oscillation frequency was significantly reduced due to the parasitic capacitances of the routing metals, the buffer load and the cross-coupled PMOS and NMOS transistors.

Minimum transistor length was used for the cross-coupled PMOS and NMOS transistors for high speed operation. The IV characteristics of various transistor widths were found and the level of current consumption of the circuit was determined. A higher current would allow operation at higher frequencies and larger output voltage swing due to higher gain but would also have higher power consumption. The Q-point (Quiescent Operating Point) was picked at roughly midway along the DC load line to avoid clipping or signal distortion. The current mirror was designed according to the current consumption of the PMOS and NMOS cross-coupled transistors. Minimum length transistors were not used for the current mirror to prevent antenna damage (or gate-oxide damage). The ratio of the current mirror is 1:1. A smaller ratio could have been used to improve power consumption. The inductor pi model generated by ASITIC was used for simulation. The inductor, parasitic capacitor and resistor values of the pi model are shown in Appendix C. The estimated Q value of the inductor at 10-GHz is around 14 to 15.

It is also important to mention that the accuracy of simulation results will very much depend on the accuracy of the device modelling, especially to the inductor pi model here.

Figure 4.11 shows the steady state response of the VCO at 10-GHz.

Figure 4.11: VCO Steady State Response

This graph shows the voltage level of the VCO and driver outputs after the start-up state. VT("/Vout_p") is the driver output and VT("/I11/vco_p") is the VCO output. The VCO output is much more symmetric compared to the driver output. This is due to the fact that the VCO driver design has a stronger pull-up than pull-down current. The addition of the driver did not significantly affect the noise performance of the VCO but it did significantly reduce the operating frequency due to the large parasitic capacitances of the driving transistors. Here, 3.3 V devices, which have larger parasitic capacitances compared to the 1.8 V ones, were used in the driver to avoid gate oxide breakdown. The

driver design will be discussed in detail in Section 4.4. Figure 4.12 shows the tuning range of the VCO.

Figure 4.12: VCO Post-Layout Tuning Range

This graph shows the frequency vs. control voltage of the VCO. LC VCOs are known to have small tuning ranges. However, by using a smaller inductor value ($L = 0.3 \text{ nH}$) and a larger varactor value ($C_{\text{average}} = 365 \text{ fF}$), a reasonable tuning range was obtained. A strong dependence of frequency tuning range on the tail current was found. With a larger tail current, the tuning range was significantly increased. In this case, a 3.6 mA tail current was used to obtain a frequency tuning range of 9 to 11 GHz in post-layout simulation when the control voltage was changed from 0.1 to 1.4 V. The control voltage cannot be too high in order to assure the pn-junctions of the PMOS varactors are reverse

biased or are operating in inversion mode. This condition is necessary for the formation of the depletion region capacitance.

The gain of the VCO, K_{VCO} , is approximately -1.87 GHz/V over the control voltage range of 0.2 to 1.2 V. The magnitudes of K_{VCO} are reduced over the control voltage ranges of 0 to 0.2 V and of 1.2 to 1.4 V, the K_{VCO} values are -1.02 GHz/V and -1.75 GHz/V respectively.

Parasitic capacitances were included in the post-layout simulations and the operating frequency was slightly reduced. However, parasitic resistances were not included in the simulations and the loss in the oscillator is expected to be higher. Figure 4.13 shows the phase noise result of the VCO at 1-MHz frequency offset when the control voltage was swept from 0 to 1.4 V. SpectreRF was used for the phase noise simulation with the maximum sideband set to five and the number of harmonics set to ten.

Figure 4.13: Phase Noise of VCO at 1-MHz Frequency Offset with Various Control Voltages

This graph shows the pss and pnoise simulation results from SpectreRF. The phase noise at a 1-MHz frequency offset varies from -100 to -114 dBc/Hz over the control voltage range of 0 to 1.4 V. Figure 4.14 shows the phase noise value as a function of the control voltage.

Figure 4.14: Phase Noise of VCO vs. Control Voltage

This graph shows that the phase noise values at 1-MHz offset lie between -100 and -105 dBc/Hz most of the time.

As shown in Figure 4.12, frequency decreases as the control voltage increases. In the higher control voltage region, greater carrier power is obtained because of the high frequency magnitude roll-off characteristic of the VCO; therefore, increased Signal to Noise Ratio (SNR) and improved phase noise are seen in the higher control voltage region in Figure 4.14 above. On the other hand, because of the reduction in the VCO gain, K_{VCO} , in the high and low control voltage regions, as shown in Figure 4.12, the output signal is less susceptible to device noise; therefore, better phase noise values are obtained in the control voltage regions in the vicinities of 0 and 1.4 V. These results agree with the Leeson equation as shown in (3.11).

As with the PD design, post-layout simulations against all corners (supply voltages, device models and temperatures) were done before the design was submitted for fabrication.

4.3.3 Floorplan and Layout

Figure 4.15 shows the floorplan and layout of the VCO.

Figure 4.15: Floorplan and Layout of VCO

The VCO was fabricated in a $0.18\mu\text{m}$ CMOS technology with a die area of $1047 \times 854 \mu\text{m}^2$. The positions of the VCO and driver circuits are shown in the floorplan diagram. All the layout rules described in Section 4.2.3 were met, as were some additional rules for the inductors. The inductor layout was designed and generated with ASITIC in metal layer M6. The layout was imported into the Cadence design environment as a CIF file, with a scale of 0.01. The inductor layout was treated as a macro cell with the pi model serving as the schematic.

4.4 Driver Circuits

Driver circuits are needed to avoid excessive loading of the PD and VCO circuits. Common source buffer circuits were used to drive the PD and VCO output signals to the $50\ \Omega$ termination resistance of the measurement equipment. Figure 4.16 shows the driver structure.

Figure 4.16: Buffer Driver Structure For PD and VCO.

A common source driver structure was used, as opposed to the source follower driver, for the VCO to ensure that there would be no ringing at the output nodes. This is because the driver circuit cannot form a positive feedback loop with the VCO output; therefore, isolation of the VCO from the outside world (probe pads and measurement equipment) is ensured. For simplicity, the PD uses the same driver structure. In order to prevent gate oxide breakdown, 3.3 V devices were used for both the PD and VCO drivers. The operating speed of the VCO will be affected significantly as 3.3 V devices have much larger parasitic capacitances than the 1.8 V devices have. The PD circuit is not affected by the parasitic capacitances of the driver as the output signals are not high speed signals.

Chapter 5: Measurement Results

In this chapter, the measurement methodologies and results of the PD and VCO chips will be discussed.

5.1 Phase Detector

Figure 5.1 shows the measurement setup for the PD chip.

Figure 5.1: Phase Detector Measurement Setup.

A Bit Error Rate Test (BERT) system was used to test the PD. A 10-GHz clock signal was generated and fed into an error performance analyzer. Differential 10-GHz clock and 10-Gb/s NRZ data signals were generated with the delay between the two sets of

signals controlled by the mainframe. The signals were fed into the die through two RF probes. DC blocking capacitors and Bias-T components were used for DC voltage level isolation and adjustment between the equipment and die. The output signals were fed into an oscilloscope through another RF probe. Attenuators were used to reduce the output signal levels to ones compatible with the measurement equipment and thereby to avoid damaging it. After the equipment was set up, the die was probed on a 40-GHz probe station. Figure 5.2 shows the probed die photograph.

Figure 5.2: Phase Detector Die Photograph.

Two dual RF probes (GSGGSG), one 6-pin DC probe (PGPPGP) and one 14-pin DC/RF probe (PGGSGGP-PGGSGGP) were used in the measurement. Figure 5.3 shows the clock and data signals as they appeared on the oscilloscope.

Figure 5.3: Input Clock and Data Signals Waveforms on Oscilloscope.

Figure 5.3 shows that the clock signal has a swing of 38 mV and the data signal has a swing of 88.5 mV approximately after 20-dB attenuation. Figure 5.4 shows the PD output signals.

Figure 5.4: Output Signals of the Phase Detector.

At 30 ps data delay, the difference between the output signals after 20-dB attenuation is 45.2 mV, as shown in Figure 5.4. By varying the delay between the clock and data signals through the BERT, the phase detector characteristic was measured and plotted. Figure 5.5 shows the DC output voltage of the PD vs. the phase error.

Figure 5.5: Phase Detector Characteristic with Simulated and Measured Results.

Figure 5.5 shows that the simulated and measured results have different linearity and output voltage levels. The measured result has smaller voltage levels but much better linearity. The reduction of the measured output voltage levels is due to the attenuation of the input and output signals by the measurement equipment (probes, SMA cables and connectors). This reduction of voltage levels would not affect the performance of the PD in a CDR application because a charge pump or buffer would be used for voltage level sensitivity adjustments.

On the other hand, the improvement in the linearity is due to the fact that the die has higher parasitic capacitances and resistances in the signal paths than the simulation models provide for. These parasitics would lower the corner frequency of the PD and would cause the PD gain to roll-off at a lower frequency. The reduction in input clock voltage levels explained above also contributes to the PD gain reduction. The PD gain roll-off compensates the higher than required gain of the master branch in Figure 4.3, and the PD's linearity is improved.

Both the measured and simulated results exhibit a non-zero phase offset which can be explained by the fact that the data signal propagates through a slightly longer signal path to the output node than the clock signal does. The output voltage value at zero phase offset will be heavily dependent on process, voltage and temperature factors. An external delay block can be used with the PLL to compensate this difference in CDR applications. This will be discussed again in Section 6.2.2.

It is shown that this type of PD combines the linear characteristic of the Hogge with the high-speed performance and the Bang-Bang (or Alexander) PD. A linear range with no dead zone for phase errors from $-\pi/2$ to $\pi/2$ is shown.

This design has extremely low power consumption. The fastest switching node, the master branch of the PD, requires a 1mA tail current, and the entire PD draws less than 4.64mA. This corresponds to a power consumption of less than 14.9mW from a +/- 1.6 V supply. The power consumption of the output drivers is not included in this calculation. The output driver draws a current of around 20 to 30 mA which varies according to the measurement setup.

Figure 5.7: VCO Die Photograph.

One dual RF probe (GSGGSG) and two 6-pin DC probes (PGPPGP) were used in the measurement. Unfortunately, no oscillation was observed in the initial trial. The following explanations might explain the failure.

5.2.1 Probe Damages

It was noticed that the dual RF probe was damaged. The signal and ground pins were “opened” when floating but were “shorted” when the probes were pressed onto the die. It is also possible that some of the probe fingers did not make proper contact with the probe pads.

5.2.2 Melting of Gate Oxide

There is a possibility that the gate oxides on top of the transistors were melted due to the dual substrate technique used. Figure 4.11 shows that the VCO output voltage swing might be too large. Although 3.3 V devices were used at locations where $|V_{gs}|$, $|V_{ds}|$ and $|V_{bs}| > 1.8V$ and no gate oxide meltdown was noticed in simulation results, in order to ensure oscillation, it may be better to start a measurement with small supply voltages and then increase the voltages gradually.

5.2.3 Inductor Pi Model Inaccuracy

Some bugs were observed with the inductor modelling tool, ASITIC [38]. The modelling tool failed to analyze more than one *via* layer; therefore, only one *via* layer was used to generate the pi model. ASITIC also did not take the **eddy and skin effects**, which play significant roles in high frequency operations, into account. These modelling failures generated a lower than expected pi model parasitic resistance, R_0 , and a higher than expected Q value (the Q value obtained, around 14 to 15, seems unrealistically high). The inductor pi model is shown in Figure C.5.

To demonstrate the importance of this parasitic resistance value, Open Loop Gain (OLG) AC simulations were done and the results are shown below. The schematic and testbench of the OLG AC simulations are shown in Appendix D. The OLG AC simulation results for $R_0 = 1.07 \Omega$ is shown in Figure 5.8 and for $R_0 = 1.3 \Omega$ is shown in Figure 5.9.

Figure 5.8: Open Loop Gain AC Simulation Result With $R_0 = 1.07 \Omega$

Figure 5.9: Open Loop Gain AC Simulation Result With $R_0 = 1.3 \Omega$

With a small increase in the inductor's parasitic resistance value, R_0 was increased from 1.07 to 1.3 Ω , the maximum AC gain dropped from 25.66 in Figure 5.8 to 13.52 in Figure

5.9. The higher than expected parasitic resistance created a larger loss in the inductor. This loss significantly reduced the small-signal gain of the VCO and oscillation cannot be self-starting.

Another possibility lies with an approximation made during simulations. In high frequency oscillators, inductor values are small and a small variation on the inductor value would result in large operating frequency variation. Here, the pi model inductor value, L_0 , was rounded up from 228 pH to 300 pH to compensate for the deficiencies of the modelling tool. The actual inductor value is lower than the simulated one and is operating at a much higher frequency range. As a result, the VCO, which has a high frequency gain roll-off characteristic, could damp or suppress the oscillation.

Although raising the current level of the VCO could increase its small-signal gain, this could result in gate oxide meltdown in certain devices and could damage the die.

5.2.4 Parasitic Resistances of Metal Lines

Other than the parasitic resistance of the pi model, R_0 , not being accurately represented, the extraction tool failed to generate the parasitic resistances of the metal lines. In post-layout simulations, the generated parasitic capacitances affected the operating frequencies but not the small-signal gain of the circuit. As stated in Section 5.2.3, a larger parasitic resistance caused larger losses in the VCO. As a result, the oscillator did not have enough gain to self-start oscillation.

Chapter 6: Conclusion

In this chapter, the work that has been done will be summarized and possible future work will be discussed.

6.1 Summary of Contributions

The following is a list of contributions from this thesis:

- Design techniques for PLL, PD and VCO for CDR applications were investigated.
- A full-rate PD suitable for SONET OC-192 systems was designed, implemented and tested. The die was fabricated in a 0.18 μm CMOS technology. Table 6.1 summarizes the performance of this PD and other published designs.

	Tang [41]	Savoj	Pottbacker [1]	Anand	Wu [42]	This Work
Data Signal Frequency (Gb/s)	2.5	5	8	2.5	10	10
Process	0.25 μm CMOS	0.18 μm CMOS	Si Bipolar	0.4 μm CMOS	AlGaAs /GaAs	0.18 μm CMOS
Phase Margin	$\pm \pi$	$\pm \pi$	$\pm \pi/2$	$\pm \pi/2$	$\pm \pi/2$	$\pm \pi/2$
Linear Range (%)	~ 30-40	~ 60-70	\	~30-40	~70	~60-70
Power Dissipation	40 mW (excluding drivers)	\	1.4 W	\	\	14.9 mW (excluding drivers)
Supply Voltage (V)	2.5	2.5	-5	3.3	-5.2	± 1.6
Architecture	Multi-phase CK signal	Linear	PD/QPD	S&H	Hogge	S&H
Chip Area (mm^2)	Schematic only	\	1.63x2.3	\	1.75x1.2	1.41x1.01

Table 6.1: Comparison of Performances With Other PD Designs For CDR Applications

Compared to the other designs, this design has the lowest power dissipation, the highest operating frequency and a relatively large linear range. A single Sample-and-Hold PD now replaces the PD, CP and LPF block in Figure 1.1. The PLL structure is significantly simplified and the response time is reduced.

- A 10-GHz Complementary LC VCO was designed, implemented and tested. Initial measurements showed that the design failed to oscillate. Extensive investigation has revealed that the failure is likely caused by the higher than expected parasitic resistance values of the VCO circuit and inductor, and a lower than expected inductor value.

Nonetheless, it is still interesting to compare the post-layout simulation results of the VCO with some other reported designs. This is shown in Table 6.2.

	Coban [43]	Mukherjee [44]	Rogers [45]	This Work
Oscillating Frequency (GHz)	12	10	10	10
Process	0.35 μm SiGe BiCMOS	0.13 μm CMOS	0.18 μm CMOS	0.18 μm CMOS
Tuning Range	4.38 GHz	3.7 GHz	125 MHz	2.2 GHz
Phase Noise	-113.5 $\rightarrow$ -112.3 dBc/Hz @ 10MHz offset	-99 dBc/Hz @ 1MHz offset	-103 dBc/Hz @ 1MHz offset	-100 $\rightarrow$ -105 dBc/Hz @ 1MHz offset
Power Consumption	0.1287 W	3.6 mW (excluding current mirrors and drivers)	70 mW (excluding drivers)	24.2 mW (excluding drivers)
Supply Voltage (V)	3.3	1.2	1.8	± 1.6
Architecture	Quadrature LC VCO	LC VCO	LC Delay Line VCO	Complementary LC VCO
Area (mm^2)	0.36 (active)	Schematic	1.9x1.5	1.047x0.854

Table 6.2: Comparison of Performance With Others VCO Designs

Compared to other designs, this VCO design has relatively low power consumption, good phase noise performance and a large tuning range. The die area is the smallest in the table.

- The objective of establishing a technology replacement for SiGe or GaAs by a standard digital CMOS process in very high speed mixed signal designs has been achieved.

6.2 Future Work

There are two major areas for future work. They are explained in the following sections.

6.2.1 VCO

In future VCO designs, extremely small inductor values should not be used as a little variation of the inductor value would result in a large operating frequency variation and VCO gain roll-off. When the small-signal gain is too small, oscillation cannot be self-starting.

Better modelling tools that take eddy and skin effects into account should be used to find the parasitic resistances or loss of the inductors. For instance, Fast Henry, ADS Momentum, SONET, GEMCAP2 or HFSS could be used. Loss from the parasitic resistances through the inductors and other metal lines must be modelled accurately to ensure the VCO has enough small-signal gain to self-start oscillation in simulations. If time permits, a network analyzer with de-embedding technique can be used to perform S-

parameter measurements on inductors employed with probe pads before VCO circuits are designed.

Patterned ground shields on inductors can be used to prevent eddy current from building up [40]. Depending on the conductivity of the substrate, reducing the eddy current could significantly increase the Q values of the inductors. Advanced inductor layout structures that would create less parasitic resistances and capacitances should be investigated. For instance, circular spiral inductors or inductors constructed with multiple metal layers. Different varactor structures can also be studied. The advantages and disadvantages of various PMOS and NMOS varactors can be investigated.

Last but not least, the VCO die can be tested again with fixed probes, where batteries can be used as power supplies for better noise performance and bypass capacitors can be added between the power supplies to stabilize the input voltage. Furthermore, measurement should be started with small supply voltage values to avoid device breakdown.

6.2.2 Clock Recovery Circuits

With adequate buffer designs between the PD and VCO blocks, a Full-Rate PLL can be developed. A delay block can be inserted before the DFF block in Figure 1.1 to overcome the phase offset issue mentioned in Section 5.1 and an OC-192 CDR circuit can be developed. It would be interesting to study and investigate different CRC structures. For instance, Half-Rate PLL or Delay-Locked Loop (DLL) structures can be designed, and their performances, advantages and disadvantages can be studied and compared.

Figure A.2: Transistor IV Characteristic

Appendix B. Phase Detector Schematics and Testbench

Figure B.1: Phase Detector Testbench

Figure B.2: Phase Detector Top Level Schematic

Figure B.3: Phase Detector Schematic

Appendix C. VCO Schematics and Testbenches

Figure C.1: Varactor Testbench

Vt_Tt_Pt

Figure C.2: VCO Testbench

Figure C.3: VCO Top Level Schematic

Figure C.4: VCO Schematic

Figure C.5: Inductor Model

Figure C.6: VCO Driver Schematic

Appendix D. VCO Open Loop Gain AC Simulation Schematic and Testbench

Figure D.1: VCO Top Level Schematic For OLC AC Simulation

Figure D.2: VCO Schematic For OLC AC Simulation

References

- [1] A. Pottbacker, U. Langmann, H. U. Schreiber, "A 8-Gb/s Si Bipolar Phase and Frequency Detector IC For Clock Extraction", ISSCC, pp. 162-163, February 1992.
- [2] J. Savoj and B. Razavi, "A 10-Gb/s CMOS Clock and Data Recovery Circuit with a Half-Rate Linear Phase Detector", ISSCC, vol. 36, no. 5, May 2001.
- [3] J. Cao, A. Momtaz, K. Vakilian, et al, "OC-192 Receiver in Standard 0.18um CMOS", ISSCC, February 2002.
- [4] D. H. Wolaver, Phase-Locked Loop Circuit Design, Prentice Hall, 1991.
- [5] C. Plett, Phase-Locked Loops and Clock Recovery Circuits Slides, June 1998.
- [6] D. Mijuskovic, M.J. Bayer, T.F. Chomicz, N.K. Garg, F. James, P.W. McEntarfer, J.A. Porter, "Cell Based Fully Integrated CMOS Frequency Synthesizers," IEEE J. Solid-State Circuits, vol. 29, pp. 271-279, March 1994.
- [7] B. Razavi, RF Microelectronics, Prentice Hall, 1998.
- [8] A. Kral, F. Behbahani, Asad Abidi, "RF-CMOS Oscillators with Switched Tuning", Proceedings of the IEEE 1998 Custom IC Conference, pp. 555-558, 1998.
- [9] G. Goldberg, Digital Techniques in Frequency Synthesis, McGraw-Hill, 1996.
- [10] B. Razavi, Monolithic Phase-Locked Loops and Clock Recovery Circuits Theory and Design, IEEE Press, 1996.
- [11] B. Kim, T.C. Weigandt, P.R. Gray, "PLL/DLL System Noise Analysis For Low Jitter Clock Synthesizer Design", Proceedings of the International Symposium on Circuits And Systems, June 1994.
- [12] C.R. Hogge, "A Self-Correcting Clock Recovery Circuit", IEEE Journal of Lightwave Technology, vol. LT-3, pp. 1312-1314, Dec 1985.

- [13] F. Wei and T. Kwasniewski, "Submicron CMOS Building Blocks for High Speed Frequency Synthesis and Clock REcovery Applications", master thesis, Carleton University, May 1997.
- [14] H. Zhong, A. Gilman, S.I. Long, "Monolithic Clock And Data Recovery Chip For 10-Gb/s Fiber Communications Systems", master thesis, University of California, Santa Barbara, 1999.
- [15] R.J. Higgins, Electronics with Digital and Analog Integrated Circuits, Prentice Hall, 1990.
- [16] N. F. Goncalves, H. De Man, "Nora: A Racefree Dynamic CMOS Technique For Pipelined Logic Structures", IEEE Journal of Solid-State Circuits, vol. 18, issue 3, pp. 261-266, June 1983.
- [17] J. Yuan, C. Svensson, "High-Speed CMOS Circuit Technique", ISSCC, vol.24, no. 1, February 1989.
- [18] D. A. Johns, K. Martin, Analog Integrated Circuit Design, Wiley, 1997.
- [19] A. Garg, Y. L. Le Coz, H. J. Greub, J. F. McDonald, et al, "Accurate High-Speed Performance Prediction For Full Differential Current-Mode Logic: The Effect of Dielectric Anisotropy", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 18, issue 2, pp. 212-219, February 1999.
- [20] H.T. Bui, A.K. Al-Sheraidah, Y. Wang, "New 4-transistor XOR and XNOR designs", Proceedings of the Second IEEE Asia Pacific Conference, pp. 25-28, 2000.
- [21] W.F. Egan, Frequency Synthesis by Phase Lock 2nd Edition, Wiley Inter-Science, 2000.
- [22] T.L. Laopoulos, C.A. Karybakas, "A Phase Locked Motor Speed Control System with Sample-and-Hold Phase Detector", IEEE Transactions on Industrial Electronics, vol.35, issue 2, pp. 245-252, May 1988.

- [23] T.H. Toifl, P. Moreira, A. Marchioro and P. Placidi, "Analysis of Parameter-Independent PLLs with bang-bang phase-detectors", IEEE Circuits and Systems, vol. 2, pp. 299-302, 1998.
- [24] J. Alexander, "Clock Recovery from Random Binary Signals", IEEE Electronic Letters, vol. 11, pp. 541-542, Oct 1975.
- [25] A. Rezayee and K. Martin, "A Coupled Two-Stage Ring Oscillator", IEEE Circuits and Systems, vol. 2, pp. 878-881, 2001.
- [26] M. Ramezani, C. A. T. Salama, "An Improved Bang-Bang Phase Detector For Clock And Data Recovery Applications", IEEE International Symposium on Circuits and Systems, vol. 1, pp. 715-718, May 2001.
- [27] S. B. Anand and B. Razavi, "A CMOS Clock Recovery Circuit for 2.5-Gb/s NRZ Data", ISSCC, vol. 36, no. 3, pp. 432-439, March 2001.
- [28] P. Horowitz and W. Hill, The Art of Electronics, Cambridge University Press, 1996.
- [29] J.W.M. Rogers, T.J. Smy, C. Plett, "A Completely Integrated 2-GHz VCO with Post-Processed Cu Inductors", IEEE Custom Integrated Circuits, pp. 575-578, 2001.
- [30] T.H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, Cambridge, 1998.
- [31] A. Hajimiri and T.H. Lee, "A General Theory of Phase Noise in Electrical Oscillators", ISSCC, vol. 33, no. 2, pp. 179-194, February 1998.
- [32] F. You, S.H.K. Embabi, J.F. Duque-Carrillo, E. Sanchez-Sinencio, "An Improved Tail Current Source for Low Voltage Applications", ISSCC, vol. 32, pp. 1173-1180, August 1997.
- [33] C.C. Enz and E.A. Vittoz, "CMOS Low-Power Analog Circuit Design", Designing Low Power Digital Systems, Emerging Technologies, Pg. 79-133, 1996.

- [34] T. L. Laopoulos, C. A. Karybakas, "A Phase Locked Motor Speed Control System With a Sample-and-Hold Phase Detector", IEEE Transactions on Industrial Electronics, vol. 35, no. 2, May 1988.
- [35] Applied Micro Circuits Corporation, "SONET/SDH/ATM OC-192 Receiver Specifications", S3092, February 2002.
- [36] T.H. Lee and A. Hajimiri, "Oscillator Phase Noise: A Tutorial", ISSCC, vol. 35, no. 3, March 2000.
- [37] R. Bunch and S. Raman, "A 0.35-um CMOS 2.5-GHz Complementary -Gm VCO Using PMOS Inversion Mode Varactors", IEEE RFIC Symposium, pp. 49-52, 2001.
- [38] A.M. Niknejad, <http://formosa.eecs.berkeley.edu/~niknejad/asitic.html>.
- [39] L. Dussopt, D. Guillois and G.M. Rebeiz, "A Low Phase Noise Silicon 9-GHz VCO and an 18-GHz Push-Push Oscillator", IEEE Microwave Symposium Digest, vol. 2, pp. 695-698, June 2002.
- [40] C.P. Yue and S.S. Wong, "On-chip Spiral Inductors with Patterned Ground Shields for Si-based RF IC's," IEEE J. Solid-State Circuits, vol.33, pp. 743-752, May 1998.
- [41] Y. Tang, G. L. Geiger, "Phase Detector For PLL-Based High-Speed Data Recovery", Electronics Letters, vol. 38, no. 23, pp. 1417-1419, November 2002.
- [42] D. Y. Wu, A. C. Yen, D. Meeker, "Two Phase Detectors For 2.5 to 10-Gb/s NRZ Data Operation: a Hogge and a Balanced Mixer", IEEE GaAs IC Symposium, pp. 266-269, November 1996.
- [43] A. L. Coban, K. Ahmed, C. Chang, "A Highly-Tunable 12-GHz Quadrature LC-VCO in SiGe BiCMOS Process", Symposium on VLSI Circuits, pp. 119-120, 2001.
- [44] D. Mukherjee, J. Bhattacharjee, J. Laskar, "A Differentially-Tuned CMOS LC VCO For Low-Voltage Full-Rate 10-Gb/s CDR Circuit", IEEE MTT-S Digest, pp. 707-710, 2002.

- [45] J. Rogers, J. R. Long, "A 10-Gb/s CDR/DEMUX With LC Delay Line VCO in 0.18- μm CMOS", ISSCC, vol. 37, no. 12, December 2002.