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CRYSTALLIZATION PROCESSES IN AMORPHOUS SILICON

by

David F. Waechter, M.A.Sc.

A thesis submitted to
the Faculty of Graduate Studies and Research
in partial fulfillment of
the requirements for the degree of

Doctor of Philosophy

Ottawa-Carleton Institute for Electrical Engineering
Department of Electronics
Faculty of Engineering
Carleton University

June, 1987

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Abstract

This thesis examines a variety of techniques for producing good quality silicon films for integrated circuit and solar cell applications. Emphasis is placed on low pressure chemically vapor deposited silicon which is annealed in a furnace or by a scanning cw laser.

Most of the films used in this work are in-situ doped with phosphorus during deposition. The films are deposited in both the amorphous and polycrystalline form, using oxidized silicon wafers as substrates. The effect of initial film structure on phosphorus incorporation and on post-annealing structure and resistivity is examined.

The furnace annealing experiments use temperatures considerably below those of experiments reported previously in the literature, while the laser annealing experiments use temperatures up to and beyond the melting threshold. In order to model the laser process, a numerical model is developed for solving the three dimensional heat flow equation in multilayer structures.

In the last section a variety of techniques are examined for using seeding trenches to establish a particular crystal orientation. A novel technique, solid phase lateral seeding induced by a scanning cw laser, is examined for the first time.

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LIST OF SYMBOLS AND ABBREVIATIONS

α	optical absorption coefficient
a-Si	amorphous silicon
β	eccentricity
c	heat capacity
c-Si	crystalline silicon
CVD	chemical vapor deposition
cw	continuous wave
D	thermal diffusivity
$d_{\max}$	maximum lateral epitaxial distance
E_a, E_g, E_n	activation energies
EELS	electron energy loss spectroscopy
EPR	electron paramagnetic resonance
G	Green's function for heat flow equation
H	heat enthalpy function
H_x, H_y	lateral heat parameters
H_f	latent heat of fusion
h	Planck constant
k	thermal conductivity, Boltzmann constant or wave number (depending on context)
λ	wavelength
L_x, L_y	lateral heat diffusion functions
LPCVD	low pressure chemical vapor deposition
MBE	molecular beam epitaxy
N, n_i	refractive index

LIST OF SYMBOLS AND ABBREVIATIONS (cont'd)

ω	angular frequency
P	laser power
P_0	polarizability
θ	linearized temperature
q	photon wave vector
ρ	mass density
R	reflectivity
RTA	rapid thermal annealing
S, S_{ins}, S_{ss}	source functions
SEM	scanning electron microscope
SIMS	secondary ion mass spectroscopy
T	temperature
T_B	substrate temperature
T_M	melting temperature
T_0	reference temperature
T_z	temperature along z axis measured with respect to T_0
TE, TM	transverse electric, transverse magnetic
TEM	transmission electron microscope
t_R	crystallization time
$\mathcal{U}$	unit step function,
v	laser scan velocity
v_g	epitaxial growth velocity
v_0	epitaxial growth velocity prefactor
W	1/e intensity radius of laser beam

Chapter 1

Introduction

1.1 General Introduction

In the electronics industry, thin silicon films are used in an increasing variety of applications. Research into this area has been fueled by numerous advances both in film deposition techniques and in methods of post-deposition annealing. By using low pressure chemical vapor deposition (LPCVD), uniform thin films can be rapidly deposited onto large wafer loads. A variety of annealing techniques can then be used to yield material which is suitable not only for passive resistors and interconnects, but also for active device regions.

This chapter presents a review of film deposition techniques and methods of post-deposition annealing. This is followed by an overview of the many applications of deposited silicon films and an outline of the thesis and its objectives.

1.2 Review of Silicon Deposition Techniques

Processes for depositing thin silicon films fall into three general categories: (1) physical methods of deposition, (2) chemical methods and (3) combined physical-chemical methods.

The simplest physical method of deposition is vacuum evaporation.

from a heated source [1]. This method is inexpensive, easy to control and has high throughput. However the step coverage is poor and there can be radiation damage from e-beam generated x-rays. Another technique which is similar in principle but different in operational details is molecular beam epitaxy or MBE [2]. This technique uses a much slower deposition rate, operates under much higher vacuum but gives films which are epitaxially aligned with the substrate wafer. This method is considerably more expensive than conventional evaporation and is normally restricted to specialized applications. MBE material will be used in some of the lateral seeding experiments reported in the present work.

Another physical deposition method is glow discharge sputter deposition [3]. In this method material is removed from a target source by bombardment with positive ions from a rare gas discharge. The sputtered ions are then directed toward the substrate surface where they deposit. In magnetron sputtering, magnetic fields are used to confine the plasma and this results in a higher deposition rate. The method has good step coverage and low radiation damage but is relatively expensive.

Chemical vapor deposition (CVD) uses the pyrolysis of silane (SiH_4) to form the silicon deposit [4]. This method is relatively inexpensive and can be operated at pressures ranging from low to atmospheric. Low pressure gives a longer mean free path of the reactant gases and therefore gives better step coverage. It also yields higher throughput since wafers can be more densely stacked.

Low pressure chemical vapor deposition has become a standard process in the industry and will be used for most of the present work.

A number of groups have recently studied plasma-enhanced CVD, a combined physical-chemical method [5]. This technique uses plasma bombardment to foster breakdown of silane and permit deposition at a reduced temperature.

1.3 Review of Annealing Processes

When annealing deposited silicon films, certain constraints are imposed by devices already fabricated in the underlying substrate. High temperature annealing can have a number of deleterious effects including degradation of minority carrier lifetime and redistribution of impurities. The latter is an especially difficult problem for small geometry devices. The appearance of these effects is a function both of the temperature of the anneal and of its duration. In general, the maximum temperature which can be permitted during thermal annealing decreases as the duration increases.

Thermal annealing processes are usually categorized according to their duration, the available annealing modes being the adiabatic, thermal flux and isothermal modes. With reference to typical thermal response times of silicon layers, the corresponding durations are short, of the same order and long respectively. Table 1.1 presents a summary of these annealing modes, the durations involved and the resulting temperature profiles.

Table 1.1 Annealing processes and their characteristics.

Mode	adiabatic	thermal flux	isothermal	isothermal
Method	pulsed laser	cw laser	RTA	furnace
Time Duration (sec)	$t < 10^{-6}$	$10^{-6} < t < 10^{-3}$	0.1 - 100	$t > 10 \text{ min}$
Temperature Profile

In the isothermal mode, heat is uniformly distributed and the temperature is determined by a balance between input power and black body radiation. Conventional furnace annealing falls into this category as does rapid thermal annealing (RTA). RTA utilizes strip heaters or incoherent light sources and has attracted considerable attention in part because of its high throughput capability [6]:

The thermal flux mode can be realized using scanning cw lasers or electron beams [6]. In this mode higher temperatures are possible both because the heating time is shorter and because the heat is localized to the surface region. It should be noted that while the duration of heating in a given region is small, thermal flux annealing by a cw laser is not considered a high throughput process. This is because a narrow beam must be raster scanned over a comparatively large area. On the other hand, a cw electron beam can be focussed into a long narrow ribbon, making much higher throughput possible [7].

The adiabatic mode can be realized using pulsed lasers or electron beams. These sources can yield high throughput since the beam sizes can approach wafer dimensions [7,8].

The experiments reported in this thesis use both conventional furnace annealing and scanning cw laser annealing. In some respects it may be possible to infer conclusions about RTA or pulsed beam annealing from the present work. This would require interpolating or extrapolating results to the time durations and temperatures

involved. However the finely focussed laser beam also provides some unique capabilities which cannot be approached using other methods. These capabilities are particularly evident in lateral seeding processes, where large temperature gradients are required.

1.4 Applications of Thin Silicon Films

Heavily doped polycrystalline silicon has traditionally been used as gates and interconnects in integrated circuits. Low resistivity is increasingly important in this application due to the continuing trend to finer line widths. This has led a number of investigators to examine cw and pulsed laser annealing as a method of lowering the polysilicon resistivity [9]. However in recent years, many manufacturers have turned to silicide interconnects formed by reacting polysilicon with refractory metals [10]. These materials have significantly lower resistivity than even high temperature annealed polysilicon but at the expense of additional processing steps.

Heavily doped polycrystalline silicon has been studied extensively for use as a diffusion source [11,12]. The motivation for this research is related to problems with conventional doping methods. In a conventional phosphorus predeposition, point defects are generated by the in-going phosphorus atoms. These defects are responsible for the nucleation of extrinsic stacking faults and dislocations. They are also responsible for the pronounced tail in the phosphorus diffusion profile and for the so-called emitter dip effect in bipolar junction transistors. In addition, phosphorus precipitates may appear

in the surface region if the concentration exceeds the solubility limit. However Armigliato et al. [12] reported that these effects could be largely eliminated if diffusion occurs from a phosphorus doped polysilicon film. They found that polysilicon provides a sink for point defects and that any precipitation of dopants occurs in the polysilicon and not in the underlying crystal.

Recent studies have shown that if heavily phosphorus doped polysilicon is used as the emitter of a bipolar junction transistor, a common emitter current gain in excess of 10,000 can be obtained [13].

It is thought that back injection of holes, quantum reflected at the polysilicon/silicon interface, is responsible for the good injection efficiency and high current gain. In solar cells, a polysilicon emitter can yield a large open circuit voltage with good overall efficiency [14]. In this application the thickness of the film must be chosen as a compromise between high series resistance for a thin layer and loss of blue response for a thick layer.

Polysilicon films with lighter doping have proven useful for making resistive loads in integrated circuits. When used in place of depletion load devices, these films can yield a 30% reduction in cell size [15]. However some problems have been encountered in controlling the resistivity of the deposited films due to its sensitivity to implant dose. To circumvent this problem Yaron et al. [16] studied cw laser annealed polysilicon and found that annealing could reduce the sensitivity by a factor of 5. They attribute this improvement to an increase in grain size and a reduction in grain boundary trap

density.

Moderately doped silicon films deposited on insulator are becoming increasingly important for active device applications. Such films have been used in high speed CMOS circuits [17,18], in flat panel displays [19] and in PIN photodetectors [20]. Another important application is the incorporation of MOS logic functions into a thin layer which overlies high power bipolar devices [21].

Field effect transistors made in polycrystalline silicon generally have lower carrier mobilities and higher threshold voltages than devices made in single crystal silicon [22]. However the device quality can be greatly improved if the material is annealed by a cw laser or other localized heat source. These annealing methods often utilize a seeding trench to establish a specific crystal orientation [23]. Unseeded films can also yield device quality material provided optimum annealing conditions are used [24]. In either case it is desirable that any remaining grain boundaries be located away from active device regions where they may shift threshold voltages or short sources and drains [25,26].

1.5 Objectives and Thesis Outline

The major objective of this thesis is to develop processing techniques for producing good quality thin silicon films with minimum thermal budget. This objective is directed toward two types of thin films. The first type is heavily phosphorus doped films, suitable for

interconnects, diffusion sources or emitter junctions. The second type is device quality silicon-on-insulator. The structural quality requirements are generally more stringent for the latter type and these films will normally be less heavily doped. Since cw laser annealing can play a role for either film type, a further objective of the thesis is to develop a simple numerical method for solving the transient heat flow equation for multilayer structures.

It should be noted that while material studies are the primary focus of the present work, other researchers at Carleton are concurrently studying ~~ing~~ device applications. These studies mainly deal with polysilicon emitter transistors [13] and solar cells [14].

The thesis begins with several review chapters dealing with the deposition, annealing and characterization of thin silicon films. Chapter 2 discusses the deposition of silicon films by LPCVD while chapter 3 examines the physics of crystallization and growth. Chapter 4 then reviews the fundamentals of laser annealing. In chapter 5 the principles of operation of a number of experimental probes which will be used in the experimental work are examined. The remaining chapters summarize theoretical and experimental results obtained by the author.

In chapter 6 a numerical method is developed for solving the transient heat flow equation for cw laser annealed multilayer structures. Comparisons are made to experimental data and an analysis of the small observed error is given.

Chapter 7 presents the results of deposition and furnace annealing experiments on in-situ phosphorus doped LPCVD silicon. Oxidized silicon wafers were used as substrates and the films were deposited in both the amorphous and polycrystalline form. The experiments examine the effect of initial film structure on phosphorus incorporation and on post-annealing structure and resistivity. The annealing temperatures used are considerably below those found in experiments reported previously in the literature.

Chapter 8 reports on cw laser annealing experiments on the same LPCVD films. The properties examined are the film resistivity, structural quality and uniformity. The latter is of special interest in cw laser annealed films due to the nonisotropic nature of the laser process. The experiments reveal those annealing conditions required to give good uniformity with minimum resistivity.

In chapter 9 several lateral seeding techniques are examined for producing device-quality silicon-on-insulator. Solid phase lateral seeding induced by a scanning cw laser is proposed for the first time and is examined theoretically and experimentally.

Finally, chapter 10 presents conclusions and suggestions for further work.

Chapter 2

Low Pressure Chemical Vapor Deposition of Silicon Films

2.1 Introduction

Low pressure chemical vapor deposition was rapidly introduced into semiconductor production lines beginning in 1976. The technique can be used to deposit a wide variety of materials including polysilicon, silicon dioxide and silicon nitride [4]. The rapid acceptance of LPCVD was a result of the near order of magnitude improvement in labor, power and cost per wafer over previously used atmospheric pressure techniques. The cost reduction is largely due to high packing densities achieved with closely-spaced stand-up wafer loading. The use of low pressure reduces the importance of mass transport limitations compared to limitations of the surface reaction. This results in depositions which are extremely uniform both in composition and thickness.

Chemical vapor deposition of polycrystalline silicon provides the important capability of in-situ doping, thereby eliminating the cost and complexity of post-deposition ion implantation or diffusion. In-situ doping is achieved by addition of the dopant-bearing species directly into the source gas. B_2H_6 can be used to obtain p-type doping while either AsH_3 or PH_3 can be used to obtain n-type doping.

In the present chapter the physical processes involved in low pressure chemical vapor deposition of silicon films from SiH_4 are reviewed. The current understanding of the homogeneous and heterogeneous reactions involved is discussed as is the influence of various processing variables. Particular attention is paid to in-situ phosphorus doping and its effect on growth rates and deposition uniformity. The physical properties of the deposited films are also examined.

2.2 LPCVD Reactor Systems

Figure 2.1 shows a schematic diagram of an LPCVD reactor and the wafer loading configuration. As gases flow through the reactor, gas phase reactions occur to produce various precursor species. These are transported to the wafer surfaces by convection or diffusion where they then adsorb. Diffusion of adsorbed species and further reactions may occur on the wafer surface with volatile reactant gases being removed into the exhaust gas. Diffusion along the surface serves to improve thickness uniformity and step coverage. The surface mobility is inversely proportional to the bonding strength of the adsorbate.

The pressure in the reactor may be varied either by changing the inlet gas flow with constant pumping speed or by changing the pumping speed with constant gas flow. Deposition reproducibility is generally improved in the latter case [27]. When the pumping speed is constant, there is a continuous increase in deposition rate with increasing reactor pressure. This dependence is reduced if the pressure is

Figure 2.1 Schematic diagram of a low pressure chemical vapor deposition system.

determined by an inert carrier gas rather than by the reactant species. Pressures in LPCVD systems typically range from 0.1 to 1.0 torr.

The temperature in an LPCVD reactor is usually controlled by three resistive heating elements distributed along the length of the tube. These elements may be adjusted independently to give a uniform temperature distribution or to produce a temperature gradient. With a uniform temperature distribution the deposition rate may be lower near the exhaust end due to depletion of reactant species. Since deposition rates increase with temperature, uniformity across the load may be improved by increasing the temperature at the exhaust end. Uniformity may also be improved by using an inlet gas manifold which injects the source gases at distributed points along the tube.

2.3 Deposition Reactions in the Silane System

The chemical reactions occurring during chemical vapor deposition of silicon are complex and not fully understood. Pyrolysis of silane may involve many intermediate species including SiH_2 , SiH_3 , Si_2H_6 and higher order silanes. However successful modeling of the overall deposition reaction has been found possible by considering only a few of the most important reactions [28,29]. In general, those reactions involving silane and silylene (SiH_2) appear to be dominant. A number of authors [30,31] have proposed that the reaction sequence in the deposition of silicon is

In addition to these heterogeneous reactions, it is also possible for silylene to form homogeneously in the gas phase:

Gaseous silylene is believed to insert directly into Si-H bonds on the silicon surface, resulting in film growth. Scott et. al. [32] showed that the heterogeneous chemistry is usually dominant unless it is quenched. They also showed that this quenching could be achieved by maintaining the substrate at a temperature significantly below that of the ambient. Film growth then proceeds at a slower rate due to the homogeneous process only.

2.4 In-situ Phosphorus Doping

The addition of controlled amounts of phosphine to silane during chemical vapor deposition results in the desired doping of the film. However the addition of even a small amount of phosphine is found to decrease the deposition rate and degrade the sample uniformity [33]. The activation energy associated with the deposition rate approaches 1.95 eV for doped material compared to 1.39 - 1.74 eV for undoped

material. The phosphorus-doped films are found to be thicker near the periphery and this nonuniformity becomes progressively worse with higher substrate temperatures and lower interwafer spacing [28].

The effect of phosphine on the chemistry of film growth has been studied in detail by Meyerson et al. [30,34]. They found that phosphine adsorbs more readily onto the silicon surface than does silane and that both phosphine and phosphorus prevent silane molecules from reacting with the surface. However they suggest that these species do not interfere with silylene insertion, and this leads to film growth dominated by the homogeneous chemistry. A number of authors [28,29] have successfully modeled radial growth rate profiles in phosphorus-doped LPCVD at 625° C by assuming the growth rate due to heterogeneous chemistry to be only 2% of its value in the absence of phosphine.

The reactor model of Yeckel and Middleman [29] assumes that silylene in the interwafer region originates from two sources, the first being decomposition of silane in the interwafer region itself. Since their model predicts silane to have a uniform distribution, this component leads to uniform film growth. The second component, which is radially dependent, results from transport of silylene generated in the annular region. Film uniformity in phosphorus-doped LPCVD can be improved if this component is reduced or eliminated. This removal can be accomplished by surrounding the wafer load with a cage which provides additional surface area for annular-generated silylene to be adsorbed. Figure 2.2 illustrates such a cage configur-

ation and the resulting improvement in film uniformity. It is clear from the figure that proper cage design is essential for obtaining uniform deposits.

It should be noted that an alternative model for phosphorus doped LPCVD has been proposed by Learn and Foster [35]. They argue that silylene can be generated from silane at sites of phosphorus adsorption and that this silylene affects the growth rate at nearby silicon sites. Their model has also been successful in fitting measured radial growth rate profiles, both with and without a wafer cage.

2.5 Physical Properties of Deposited Films

The structural properties of silicon films deposited by LPCVD are strongly dependent on the deposition parameters and the presence of dopants or other impurities. At low deposition temperatures, deposited silicon atoms have limited mobility and may not settle into the most favourable configuration. This leads to amorphous growth. The threshold temperature for crystalline growth is normally reduced for lower deposition pressure.

At high temperature and low pressure, undoped polysilicon films have a preferred $\langle 220 \rangle$ orientation [36]. The film structure is columnar with the column diameter usually being reported as the grain size. The size of the grains is typically ~ 150 nm in 500 nm thick films and increases approximately linearly with increasing film

a)

b)

Figure 2.2 a) wafer cage configuration made from fused silica rods.
 b) radial growth rate profiles in in-situ phosphorus doped LPCVD polysilicon (from ref. 28). The numbers in the figure give the ratio of cage to tube area.

thickness [37]. The grain size also increases with increasing temperature or decreasing pressure. Bisaro et al. [36] suggest that the preferred $\langle 220 \rangle$ orientation results from nucleation at the surface, in contact with the gas phase. Nearer the amorphous/polycrystalline transition, $\langle 311 \rangle$ orientation dominates and the samples are nonhomogeneous, polycrystalline near the substrate/film interface and amorphous near the free surface. This inhomogeneity suggests that the material is amorphous when deposited but crystallizes during the deposition time. However Bisaro et al. suggest that the $\langle 311 \rangle$ orientation results from nucleation in the gas phase with the initial nuclei being too small to detect by X-ray diffraction. Further crystallization then occurs in the solid phase by capture of dangling bonds on a strained interface. The final $\langle 311 \rangle$ grains are generally small, ranging from 24 to 36 nm.

The properties of in-situ phosphorus doped films are somewhat different from those outlined above [33]. The crystallization temperature is approximately 20° C lower and the predominant orientation in the high temperature regime is $\langle 311 \rangle$. Just above the amorphous/crystalline threshold both $\langle 311 \rangle$ and $\langle 111 \rangle$ are prevalent. The average grain size in doped material of 500 nm thickness ranges from 30 to 90 nm in the high temperature regime and from 70 to 500 nm just above the crystallization threshold.

Chapter 3

Physics of Crystallization and Growth

3.1 Introduction

In many semiconductor device applications it is desired that deposited silicon films be epitaxially aligned with the underlying silicon wafer. This alignment may occur by direct contact with the wafer in all regions or by contact in isolated windows. In other applications the material requirements may be satisfied with non-aligned polysilicon, provided the grains are large and of good structural quality. Unfortunately it is usually found that as-deposited LPCVD silicon is either amorphous or relatively poor quality polycrystalline. Subsequent heat treatment is therefore required.

The present chapter reviews the physics of crystallization and growth during heat treatment of amorphous and polycrystalline silicon films. Both solid and liquid phase epitaxy are examined as is bulk and surface-induced nucleation from the amorphous phase. The influence of impurity content, optical excitation and crystal orientation are also examined.

3.2 Epitaxial Growth from the Amorphous Phase

3.2.1 General Description

Epitaxial growth occurs when atoms in an amorphous phase join an adjacent crystalline region under the influence of heat treatment. The transfer of atoms is characterized by an energy barrier of the type shown in fig 3.1. Since atoms may jump in either direction, the growth rate is given by [43]

$$V_g = V_0 \exp(-E_g/kT) \{1 - \exp(-E_a/kT)\} \quad (1)$$

where V_0 is the product of jump length and vibrational frequency. The quantities V_0 and E_g can be determined from an Arrhenius plot of the growth rate in the temperature range where $1 \gg \exp(-E_a/kT)$.

The growth rate prefactor V_0 is proportional to the distance between crystallographic planes and is inversely proportional to the atomic density in these planes. This appears to explain the qualitative features of the variation of V_0 with crystal orientation. The $\langle 100 \rangle$ value is 3 times the $\langle 110 \rangle$ value and about 25 times the initial $\langle 111 \rangle$ value [38]. For a given temperature V_0 is constant in time for $\langle 100 \rangle$ and $\langle 110 \rangle$ but nonlinear for $\langle 111 \rangle$. The quality of regrown $\langle 111 \rangle$ material is generally poor, there being a large number of defects and a strong tendency of twinning. The activation energy E_g is independent of crystal orientation.

Figure 3.1 Energy barrier for solid phase epitaxial growth.

The growth rate prefactor is also found to depend on impurity content, the presence of illumination and the preparation method of the amorphous layer. Electrically active dopants increase V_0 [39] while impurities like O and N reduce V_0 [40]. In undoped samples, laser irradiation can cause V_0 to increase by two orders of magnitude [41]. This effect is substantially reduced in doped samples [42]. The activation energy E_g generally shows less variation and is typically - 2.4 - 2.9 eV. Figure 3.2 summarizes growth rate data obtained by Olson et al. [39] for undoped, doped and compensated Si films.

A variety of models have been proposed to explain the dependence of V_0 on impurity content and illumination. The most successful models appear to be those which associate the increase of V_0 with electronic effects related to the position of the Fermi level [43-45]. In some of these models it is proposed that vacancies and their charge state determine the growth rate [43]. However Bisaró et al. [44] argue that dangling bonds are more common defects in amorphous silicon and that these play the dominant role. To test this hypothesis they measured the density of neutral dangling bonds in doped samples using electronic paramagnetic resonance (EPR). A direct correlation was found between the neutral dangling bond density and the crystal growth rate. This shows that dangling bonds and not vacancies are dominant in controlling epitaxy.

In the model of Germain et al. [45] it is proposed that the only

a)

b)

Figure 3.2 Solid phase epitaxial growth velocity vs. reciprocal temperature for silicon: a) undoped, b) doped, (ref 39).

sites on the amorphous side which are available for crystallization are those which have captured dangling bonds. Moreover, because the crystalline surface has both positively and negatively charged dangling bonds, those dangling bonds on the amorphous side which are charged have a larger capture cross section. Electrically active p-type dopants increase the growth rate by accepting electrons from dangling bonds, making them positively charged. Electrically active n-type dopants increase the growth rate by donating electrons to dangling bonds, making them negatively charged. On the other hand, illumination generates electron-hole pairs, resulting in both positively and negatively charged dangling bonds. In undoped samples illumination would be expected to substantially increase the growth rate, while in doped samples the effect would be reduced because charged dangling bonds are already present. Finally, the reduced growth rate in oxygen doped samples can be explained by a reduction in the dangling bond density.

3.2.2 Influence of a Native Oxide

The epitaxial process just described can proceed provided the crystalline/amorphous interface is reasonably clean and free of its native oxide. There is little difficulty in achieving this condition when the amorphous layer has been formed by ion implantation. However special cleaning techniques are normally required for deposited layers. Such techniques include sputter cleaning in ultra high vacuum [46] or reducing the oxide in H_2 at $1100^\circ C$ just prior to

deposition [47]. In a more novel approach Sigmon and Tseng [48] report breaking up and diffusing the native oxide with a post deposition Si implant. It would be desirable however to avoid these elaborate techniques and obtain epitaxy using only wet chemical cleans. This can in fact be accomplished, but the epitaxy then proceeds in a somewhat different manner, as discussed below.

Solid phase epitaxy using only conventional cleaning techniques was reported by von Allmen et al. [49] in 1979. Single crystal $\langle 100 \rangle$ substrates were degreased in organic solvents and given a 20 minute clean in an RCA solution (5:1:1; H_2O : NH_4OH : H_2O_2). They were then etched in 10% HF, rinsed in high purity water and immediately loaded into an evaporation chamber. After evaporating 1000 - 3000 Å of amorphous silicon, the samples were annealed at 550° C for various durations. Backscattering measurements showed no change of structure over the first 140 - 150 minutes. Beyond 150 minutes an increasing volume fraction of crystalline to amorphous material was found. By 210 minutes a single crystal film of reasonably good quality was obtained. The quality continued to improve upon further annealing at the same temperature.

The initial delay period is thought to be the time required for the crystal to penetrate the interfacial boundary in isolated weak spots. In the second shorter period, vertical and lateral growth transforms the rest of the material. With the cleaning procedure used the native oxide thickness is thought to be on the order of one atomic layer. When the HF etch is omitted an oxide thickness of ~ 20Å

is expected and von Allmen et al. [49] found that epitaxy could not be obtained. If the RCA clean was omitted epitaxy occurred only occasionally.

In more recent experiments Quach and Reif [50] achieved solid phase epitaxy in LPCVD polysilicon which had been amorphized by an Si implant. Interfacial impurities may be a more serious problem in these films due to the use of low pressures in a hot walled reactor [51]. Epitaxy was still achieved by annealing at 550° C provided the predeposition cleaning included a rinse in concentrated HF.

3.3 Epitaxial Growth from the Polycrystalline Phase

Fine grained polycrystalline silicon can be epitaxially aligned with an underlying substrate if the annealing temperature is sufficiently high. Complete epitaxial alignment of undoped LPCVD polycrystalline silicon was reported by Tsaur and Hung in 1980 [52]. Silicon <100> wafers were organically cleaned, etched in 10% HF and rinsed in deionized water immediately before insertion in the reactor. After depositing the polysilicon at 650° C the samples were furnace annealed at temperatures of 1000 - 1150° C. The subsequent alignment was found to proceed by the formation of epitaxial columns which then grew laterally, consuming the remaining material. A short delay period was observed, again connected with the time required for columns to penetrate the original interface in isolated locations. Samples annealed at 1150° C for 120 minutes were found to have only a small amount of defects, mostly twins. Polycrystalline silicon is

believed to be structurally stable but transformations are possible by self diffusion of Si.

It was recently reported by Wong et al. [53] that epitaxial alignment occurs more quickly and at lower temperatures for polysilicon doped with arsenic. They prepared samples in a similar manner to that just described, but dopants were introduced either in situ with the deposition or by ion implantation. Furnace annealing at 950° C produced complete epitaxial alignment in times on the order of one hour. Sample to sample variations in the time required for alignment were observed, depending on the continuity of the interfacial region and on the arsenic dose.

3.4 Bulk and Surface Nucleation

Amorphous silicon exists in a state of higher free energy compared to the crystalline phase. Under the influence of heat treatment atoms in the amorphous bulk may coalesce into a crystalline pattern. When this occurs the total free energy initially increases due to the influence of a surface free energy term. A maximum increase is reached at a critical crystallite size, typically on the order of 100 atoms [54]. Beyond this point the crystallite is stable and the total free energy is reduced by further growth. The nucleation rate n is defined as the number of stable crystallites which appear per unit time in an untransformed volume containing N atoms. This quantity is proportional to the epitaxial growth velocity but has an additional

activation energy term associated with the Gibbs energy for forming a critical crystallite [54].

Since crystallite nucleation is controlled to a large extent by the surface free energy, it follows that nucleation at a substrate interface may occur at a different rate than in the bulk. It is indeed observed that upon post-deposition furnace annealing, amorphous silicon on a noncrystalline substrate usually crystallizes first at the substrate interface [44,54]. The initial crystallites then grow vertically and laterally leading to a columnar structure.

In experiments which measure the time required to obtain a given crystalline fraction, it is difficult to determine whether the dynamics are controlled by nucleation or by growth. However Zellama et al. [54] found that either bulk or surface-induced nucleation could occur in evaporated amorphous silicon, depending on the conditions of evaporation, and that nucleation and growth rates could be separated. They found that the steady state bulk nucleation rate has activation energy 4.9 eV in the temperature range where V_g has activation energy 2.4 eV. There is also a transient delay time before steady state nucleation occurs. This delay time is also thermally activated and has activation energy approximately 13 % larger than that of V_g [55].

In principle crystallite nucleation can occur at any temperature but the rate may be sufficiently slow for the amorphous material to be considered metastable. In the literature reference is often made to the crystallization temperature or the crystallization temperature

range. This normally refers to the temperature at which complete crystallization would be expected for typical furnace annealing durations, on the order of 1/2 hour. The crystallization temperature is strongly dependent on both the sample composition and the preparation method.

In general, the temperature at which deposited amorphous silicon crystallizes is very near the transition temperature for amorphous/polycrystalline depositions. For example atmospheric pressure CVD yields amorphous silicon for deposition temperatures below 650° C and polycrystalline silicon for deposition temperatures above 700°C [56]. On the other hand, amorphous-deposited CVD silicon crystallizes upon post-deposition annealing at about 665° C [57]. A similar result holds for LPCVD silicon only the crystallization temperature is lower [58]. This suggests that the critical temperature for crystalline deposition is largely determined by the properties of the bulk material rather than by the surface mobility of adsorbed atoms during growth.

When trying to achieve solid phase epitaxy from a crystalline substrate, nucleation of crystallites in the amorphous bulk should be avoided. The extra activation energy term in the nucleation rate normally makes this possible. However competition with bulk nucleation will eventually limit the maximum epitaxial thickness. A lower annealing temperature normally increases the maximum epitaxial thickness at the expense of a slower growth rate. On the other hand, Quach and Reif [50] found that when attempting solid phase epitaxy

in the presence of an interfacial native oxide, higher annealing temperatures are preferred. They argue that the delay time for crystal penetration of the native oxide decreases with temperature at a rate which offsets the faster bulk nucleation.

3.5 Internal Energy and Explosive Crystallization

The internal energy of amorphous silicon generally exceeds that of the crystalline phase by about 400 J/g [59]. The exact value depends on the preparation method of the material and is associated with bond angle fluctuations and dangling bonds. In the case of implanted silicon low temperature annealing of the initial phase may cause structural relaxation to another phase, still amorphous, but with a reduced dangling bond density [60]. Evidence of multiple amorphous configurations has also been found in samples deposited by rf sputtering [61].

When crystallization occurs in one region of an amorphous solid the liberated heat can diffuse into adjacent regions and contribute to crystallization there. Under certain circumstances a self-sustained avalanche process can result with the crystallization wave propagating throughout a large region. This "explosive crystallization" can be initiated by a cw. or pulsed laser. In the case of some materials like amorphous germanium it can also be initiated by mechanical shock [62].

For explosive crystallization to occur the temperature of the

substrate must exceed a critical value , below which the liberated heat is insufficient to crystallize adjacent regions [63]. For cw laser annealing Auvert et al. [64]. found that a critical scan velocity must also be exceeded, below which only conventional crystallization occurs. They found that the critical velocity is of the order of 50 cm/s and depends on the temperature and thermal conductivity of the substrate.

CW laser annealed samples with explosive crystallization are characterized by a periodic array of crescent shaped regions running parallel to the scan direction. This pattern arises because the crystallization front outruns the laser, stops when it lacks sufficient support from laser heating, then restarts when the laser catches up. The average runaway velocity of the crystallization front is typically ~ 1000 cm/s. The region inside the crescents is found to be smooth fine-grained poly. Rougher large-grained poly is found if the laser power exceeds the melting threshold [65].

3.6 The Thermodynamics of Melting

The transition between crystalline and molten silicon occurs near 1690 K and is accompanied by a major rearrangement of structure. Molten silicon is known to be metallic and has a coordination number of 6.5, compared to 4 for the crystalline phase. The energy required to support this structural rearrangement is known as the latent heat of fusion and has a value of ~ 1790 J/g [66]. As silicon is heated

through the melting point, the temperature rise must pause momentarily while this latent heat is being supplied. Before all of the latent heat is supplied, a slush zone may exist in which only some of the crystalline bonds have been broken.

The melting of amorphous silicon is a more interesting phenomenon and indeed, has been the subject of some controversy. Its larger free energy with respect to the crystalline phase has led to the suggestion that a-Si may be metastable with the metallic liquid at a temperature substantially below 1690 K [67,68]. Recent calculations by Donovan et al. estimate the melting temperature of amorphous silicon to be 1420 K [69].

In order for the amorphous to liquid transition to be observed the heating rate must be sufficiently rapid for solid phase crystallization to be bypassed. Guttman [70] has argued that even in rapid pulsed laser annealing a microcrystalline phase will form first, followed by melting at 1690 K. However experimental evidence suggests that this is not the case. By measuring the electrical conductivity of the metallic liquid during pulsed laser annealing, the depth of melting can be monitored as a function of time. For amorphous silicon on a single crystal Si substrate, a plateau is observed, due apparently to a larger melting temperature of the underlying c-Si [71].

For cw laser annealing the dwell time is several orders of magnitude larger than typical laser pulse durations. Present evidence indicates that in this case a depressed melting temperature cannot be observed. Olson et al. [72] used reflectivity measurements during

cw laser annealing and found no evidence of a-Si melting up to 1645 K. They point out that this does not rule out a reduced melting temperature, but merely reflects on the kinetics of melting relative to solid phase crystallization.

Recent experiments by Alestig and Holmen [73] found that the cw laser power required to melt amorphous silicon on sapphire was the same as that required to melt crystalline silicon on sapphire. It appears that a solid phase amorphous to polycrystalline transition occurs early enough in the laser scan that the material behaves as though it had the optical and thermal properties of crystalline silicon throughout.

3.7 Epitaxial Growth from the Liquid Phase

When a molten/single crystal interface is held at the melting temperature, atoms cross the interface in both directions at equal rates. As heat is conducted away from the interface the liquid becomes undercooled and epitaxial crystallization becomes energetically favoured. The velocity of the moving interface is determined by the amount of undercooling and hence by the rate at which heat is conducted away by the substrate.

When silicon is annealed by a pulsed laser large temperature gradients are possible leading to large undercoolings and rapid solidification. Figure 3.3 shows the solidification velocity vs undercooling as calculated by Galvin et al. [74]. It is noted on

Figure 3.3 Solidification velocity vs. undercooling for silicon (ref 74).

the figure that typical solidification velocities for annealing with a pulsed ruby laser are $\lesssim 5$ m/s. This corresponds to an undercooling of $\lesssim 70$ K. It is also noted that for velocities in excess of 15 m/s, atoms are unable to epitaxially align with the crystal and an amorphous layer is formed. Interestingly, the undercooling for this point corresponds well to the calculated depression of the melting temperature of amorphous silicon relative to the crystalline value [67,68].

During cw laser annealing of a silicon wafer temperature gradients are reduced and vertical resolidification velocities are typically on the order of 2 cm/s. Horizontal resolidification velocities are near the scan speed and are generally below 100 cm/s. These correspond to undercoolings of the interfacial melt of 0.3 K and less than 14 K respectively. In this case it is possible to track the position of the interface with reasonable accuracy by solving the heat transport equation and noting the position where $T^* = 1690$ K. A more elaborate approach is required for pulsed laser annealing, taking into account the relation between undercooling and epitaxial growth velocity.

Liquid phase epitaxy in deposited silicon films is fairly insensitive to interface impurities provided the melt front penetrates the film/substrate interface [75]. If the melt penetrates only part way, the molten zone will resolidify in the polycrystalline form. For more extreme contamination as exists with a native oxide, the melt may have to penetrate somewhat deeper than the interface in order to disperse the impurities [76].

3.8 Solute Trapping and Diffusion

In doped material, the dopant profile can be altered if the segregation coefficient at the receding melt/solid interface differs significantly from unity. The segregation coefficient is defined as the ratio of the solute concentrations on the solid and liquid sides of the interface, ie. C_S/C_L . Equilibrium values for this quantity for boron, phosphorus and arsenic are 0.8, 0.35 and 0.30 respectively [77]. However theoretical models predict that these values should increase continuously as the interface velocity increases from zero [78]. This is a nonequilibrium phenomenon known as "solute trapping". Measurements by White et al. [79] determined that the segregation coefficients of boron, phosphorus and arsenic are all near unity for interface velocities near 3 m/s.

Solute trapping can result in electrically active dopants being incorporated into the material at concentrations exceeding the solid solubility limit (the solubility limit of phosphorus in single crystal silicon is $\sim 4 \times 10^{20} \text{ cm}^{-3}$ [77]). However beyond this point the material may not be stable upon further heat treatment. Studies in polycrystalline silicon implantation-doped to concentrations greater than 10^{21} cm^{-3} have shown that the resistivity is reduced to a very low value by laser annealing, but upon reheating in a furnace, the resistivity increases due to precipitation of dopants at grain boundaries [80]. This effect is quite pronounced in pulsed laser

annealed samples but is small in cw laser annealed samples, due to the larger grain size of these films [81].

While silicon remains in the solid form, the diffusivity of most dopants is less than $\sim 10^{-10}$ cm²/s [82]. This is small enough that for short annealing times characteristic of cw laser annealing, dopant diffusion is insignificant. On the other hand, when silicon melts, the diffusivity increases by many orders of magnitude. In the case of phosphorus, it increases to $\sim 5 \times 10^{-4}$ cm²/s [82]. With this value substantial dopant diffusion can occur. The characteristic diffusion length, $\sqrt{Dt}$, for a 0.1 ms heating time is then about 2 μ m which is clearly substantial compared to typical device dimensions.

Chapter 4

Fundamentals of Laser Annealing

4.1 Introduction

The characterization of a laser annealing process must consider three distinct aspects: the transfer of light energy into the material, the thermalization and transport of this energy and the response of the material structure to transient heating. All three of these aspects are examined in the present chapter. In addition, a review is presented of the optical and thermal properties of three materials of present interest: silicon, silicon dioxide and sapphire.

4.2 Coupling of Laser Energy to Solids

During optical excitation of a solid material photons are absorbed largely within a distance α^{-1} of the surface, where α is the optical absorption coefficient. Photons with wavelengths ranging from ultra violet to infrared interact primarily with electrons since atoms are too heavy to respond. In semiconductors the initial absorption is band-to-band with free electron absorption making an increasing contribution as carrier densities increase [83].

Optically generated carriers quickly thermalize with each other through Auger and other processes [83]. However thermalization with

the lattice is a somewhat slower process requiring frequent atomic collisions. Before this thermalization can occur some carriers will re-radiate their energy, giving rise to the sample reflectivity.

During cw laser annealing there exists an energetic equilibrium between the carrier and lattice systems, leading to nearly equal carrier and lattice temperatures. The net rate of energy absorption by electrons is nearly equal to the rate of energy transfer to the lattice and the two are usually considered spatially coincident. This is distinctly different from pulsed laser annealing where hot carriers may diffuse a significant distance before thermalizing with the lattice [84].

In any heated body electromagnetic radiation is emitted in accordance with the Stefan-Boltzmann law [85]. The emitted intensity is proportional to the fourth power of the absolute temperature and is about $3 \times 10^5 \text{ W/m}^2$ at 1500 K. For annealing durations in excess of 0.01 sec it is a balance between this radiated energy and the input power which determines the temperature. However in both pulsed and cw laser annealing, the energy is deposited in a much shorter time period and the input power density exceeds the radiated power density by several orders of magnitude. In this case thermal conduction into the substrate is the dominant mechanism of energy removal.

4.3 Temperature Rise Calculations

In the absence of significant energy loss due to radiation, the

temperature profiles in a heated body are governed by the well-known heat flow equation, derived from conservation of energy:

$$c\rho \frac{\partial T}{\partial t} = \nabla(k \nabla T) + (1 - R) S, \quad (4.1)$$

where $c\rho$ is the product of specific heat and mass density and k is the thermal conductivity. S is the source function, equal to the input power density, and R is the sample reflectivity.

Analytic solutions of eq. (4.1) are usually based on the conventional Green's function formalism for linear partial differential equations. In the case of pulsed laser annealing, these solutions have included the effect of temperature dependent optical and thermal properties using perturbation theory [86] or the adiabatic approximation [87]. Numerical finite difference techniques have also been employed [88].

The solution for pulsed beams can often be carried out in one dimension due to the uniformity and large size of pulsed beams. On the other hand, cw laser annealing demands a three dimensional solution. Three dimensional analytic solutions for the case of a stationary cw beam were pioneered by Lax [89,90]. More comprehensive solutions followed which considered multilayer structures [91] and moving beam annealing of single [92] double [93] and triple layer structures [94].

Analytic solutions of the heat flow equation can account for a temperature dependent thermal conductivity by introducing the

linearized temperature θ . This quantity is defined through the Kirchhoff transform:

$$\theta = \theta(T_0) + \int_{T_0}^T \frac{\kappa(T')}{\kappa(T_0)} dT'. \quad (4.2)$$

Substituting eq. (4.2) into eq. (4.1) gives a new equation with $\kappa(T)$ removed from the spatial derivative:

$$\frac{1}{D(T)} \frac{\partial \theta}{\partial t} = \nabla^2 \theta + (1 - R) S, \quad (4.3)$$

where the thermal diffusivity $D = k/c\rho$ has been introduced.

This linearization procedure is only possible in a restricted way for multilayer structures since it is required that the ratio of the thermal conductivities of the various layers be temperature independent [91,93]. Furthermore the procedure does not remove nonlinearities associated with other material properties. Those associated with melting, including the absorption of latent heat of fusion, are especially difficult to handle. Kokorowski et. al. [95] have presented a solution which includes melting but it is restricted to the time-independent problem.

A full solution of the heat flow equation which includes the nonlinearities associated with melting and temperature dependent optical and thermal properties is possible only using numerical techniques. However such techniques are difficult in three dimensions due to restrictions on computing power. Recently, Schvan and Thomas [96,97]

showed that if attention is restricted to the temperature rise along the centre of a circular laser beam, the three dimensional heat flow equation can be split into two coupled one dimensional equations, one describing the vertical heat flow, and the other the radial heat flow. In chapter 6 this approach is examined in detail and is extended to elliptical laser beams and to multi-layer structures.

4.4 Response to CW Laser Heating

During cw laser annealing the temperature varies rapidly and the net effect of this heating process must be determined from an integration over time. For example, the thickness of an amorphous layer which is epitaxially aligned with an underlying substrate can be written as

$$z = R_0 \int \exp[-E_g/kT(t)] dt. \quad (4.4)$$

Recently Gold and Gibbons [98] reported a calculation in which the temperature profile for scanning cw laser annealing, determined from the solution of Lax [90], was substituted into eq. 4.4. They found that the regrown layer thickness could be written in terms of an effective annealing temperature T_{eff} and an effective annealing time t_{eff} such that

$$z = R_0 t_{eff} \exp[-E_g/kT_{eff}]. \quad (4.5)$$

Their calculation showed that for a point along the center of a single cw laser scan, T_{eff} is simply the maximum temperature that occurs during the scan. The effective time is given by

$$t_{eff} = 2Wf/v \quad (4.6)$$

where W is the 1/e intensity radius of the laser beam and v is the scan velocity. The unitless quantity f varies slowly with E_g and substrate temperature and is typically ~ 0.3 [98].

In practice, samples will normally be annealed with multiple overlapping scans. In this case T_{eff} is unchanged but t_{eff} is replaced by [98]

$$t_{eff} = t_s (2 W f)^2 / A, \quad (4.7)$$

where t_s is the time required to scan over area A .

Analytic solutions of the heat flow equation generally show that the maximum temperature rise induced by a cw laser scan is directly proportional to P/Wk where P is the laser power and k the thermal conductivity [89,92]. In this factor the expected power density term, P/W^2 , has been multiplied by W in order to account for greater lateral heat diffusion for a narrower beam.

4.5 Material Properties: Silicon, Silicon Dioxide and Sapphire

As the temperature of a laser annealed material rises the optical properties affecting the absorption of light and the thermal properties affecting the transport of heat change. A knowledge of these changes is necessary for accurate modeling of the annealing process. The materials that are of interest in the present work are silicon, silicon dioxide and sapphire. The relevant properties of these materials are now examined. Empirical expressions are given which will be used in the calculations presented in later chapters.

4.5.1 Crystalline Silicon

The optical absorption coefficient of crystalline silicon has been measured as a function of temperature for wavelengths appropriate to various laser types [99]. For a multi-line argon ion laser with wavelengths between 488 and 514 nm the following empirical relation can be used

$$\alpha = 7500 \exp(T/435) \text{ cm}^{-1}, \quad (4.8)$$

with T in degrees Kelvin. The absorption coefficient of the metallic liquid silicon increases to a value of 10^6 cm^{-1} [95].

In the solid phase the reflectivity of silicon increases with temperature in a near-linear fashion. At the wavelengths of the argon ion laser we use the relation [100]

$$R = 0.367 + 4.29 \times 10^{-5} T \quad (4.9)$$

Molten silicon, being metallic, has a significantly larger reflectivity with value 0.72. For thin layers of molten silicon on a crystalline silicon substrate, thin film interference effects cause a gradual increase of the reflectivity from the lower solid state value at zero melt depth to the maximum value for depths in excess of 0.03 μm . Fig. 4.1 shows the reflectivity as a function of melt depth as calculated by Kokorowski et. al. [95], using the classical plane wave formalism [101].

Published thermal conductivity data for crystalline silicon [102] is well fit by the analytical function

$$k = 299/(T - 99) \text{ W/cm-K} \quad (4.10)$$

Upon melting the thermal conductivity increases sharply to a value of 0.64 W/cm-K [103].

The specific heat of silicon increases slowly with temperature [104] while the mass density decreases slightly. The mass density increases by about 10% upon melting [103]. The small variation in the specific heat - mass density product can be approximated by the function [100]

$$c_p = 2.33 (T - 159)/(T - 99) \text{ J/cm}^3\text{K}. \quad (4.11)$$

Figure 4.1 Reflectivity of a thin film of liquid silicon on a crystalline silicon substrate (ref 95).

4.5.2 Polycrystalline Silicon

The thermal properties of polycrystalline silicon can usually be considered very near those of single crystal silicon. However the optical absorption coefficient is generally about twice as large [105]. The real part of the refractive index is only slightly larger and the material has a slightly larger reflectivity [106].

4.5.3 Amorphous Silicon

Both the optical and thermal properties of amorphous silicon are significantly different from those of its crystalline counterpart. These properties also have some variation depending on the mode of preparation. It was noted in the chapter 3 that these differences have little effect for cw laser annealing of amorphous silicon-on-insulator. An amorphous to polycrystalline phase transition occurs early enough in the laser scan that the material behaves as though it had the optical and thermal properties of crystalline silicon throughout. However this result is not valid for pulsed laser annealing and it may not be valid for cw laser annealed amorphous silicon on a higher thermal conductivity substrate. It is therefore worthwhile to briefly examine some of the relevant properties of this material.

Amorphous silicon is a direct gap semiconductor and consequently

has a much larger absorption coefficient than crystalline silicon [107]. At the wavelengths of the argon ion laser the reflectivity is only slightly larger [107]. The specific heat - mass density product is near that of crystalline silicon while the thermal conductivity is at least an order of magnitude smaller [108].

4.5.4 Silicon Dioxide

Silicon dioxide is optically transparent at the wavelengths of the argon ion laser. However when placed on the surface of a silicon wafer it can act as an anti-reflection coating. The reflected intensity is reduced by destructive interference between light reflected at the air/oxide interface and at the oxide/silicon interface, as illustrated in fig. 4.2. The reflectivity is a periodic function of the oxide thickness d_0 and is given by [101].

$$R = \left| \frac{r_{12} + \rho_{23} \exp[i(\theta_{23} + 2\beta_0)]}{1 + r_{12} \rho_{23} \exp[i(\theta_{23} + 2\beta_0)]} \right|^2, \quad (4.12)$$

where

$$r_{12} = \frac{n_1 \cos \theta_1 - n_2 \cos \theta_2}{n_1 \cos \theta_1 + n_2 \cos \theta_2}, \quad (4.13)$$

$$\rho_{23} \exp[i\theta_{23}] = \frac{n_2 \cos \theta_2 - n_3 \cos \theta_3}{n_2 \cos \theta_2 + n_3 \cos \theta_3}, \quad (4.14)$$

and

$$\beta_0 = \frac{2\pi}{\lambda} n_2 d_0 \cos \theta_2. \quad (4.15)$$

Figure 4.2 Reflection of light from air/SiO₂/Si system.

In these equations λ is the wavelength of the light, while n_1 , n_2 and n_3 are the indices of refraction of air, silicon dioxide and silicon respectively. The latter number is complex in order to account for the finite absorption coefficient. The angles θ_1 , θ_2 and θ_3 are shown in fig. 4.2 and are related by Snell's law. Figure 4.3 shows the reflectivity as a function of oxide thickness calculated from eq. (4.12) assuming $n_1 = 1$ for air, $n_2 = 1.46$ for SiO_2 , $n_3 = 4.69 - 0.093i$ for solid silicon and $n_3 = 2.2 - 4.5i$ for liquid silicon. At other than normal incidence the reflectivity depends on whether the electric field vector is perpendicular to the plane of incidence (TE wave) or parallel to the plane of incidence (TM wave). In general, any incident wave can be split into TE and TM components and the two treated separately.

The anti-reflective effect of silicon dioxide is useful for providing selective heating in isolated areas during laser annealing. The oxide coat also serves to contain fluid flow during liquid phase processing and to minimize contamination when the annealing is done in air.

To the author's knowledge the thermal conductivity of silicon dioxide obtained by thermal oxidation of silicon has not been measured. In the literature some authors have used values appropriate to quartz single crystal [109] while others have used values appropriate to fused silica [110]. In the present work the latter is used since SiO_2 obtained by thermal oxidation of silicon is known to

Figure 4.3 Reflectivity of 5145 Å light from an oxidized silicon wafer. The solid lines are for solid silicon just below the melting temperature and the dashed lines are for liquid silicon.

be vitreous [111]. The constant value 0.02 W/cm-K obtained by Wray and Connolly [112] over a broad temperature range is used. The specific heat - mass density product of fused silica varies little with temperature in the high temperature regime and the constant value 2.5 J/cm³-K [104] is used here.

4.5.4 Sapphire

The thermal conductivity data for sapphire [113] is well fit by the empirical function

$$k = 0.056 + (T - 1550)^2 / 17300 \text{ T W/cm-K.} \quad (4.16)$$

Published specific heat [113] and thermal expansion [114] data yield a specific heat - mass density product which is fit by

$$c_D = 5.5 (T - 170) / (T - 68) \text{ J/cm}^3\text{-K.} \quad (4.17)$$

Sapphire, like silicon dioxide, is transparent at the wavelengths of the argon ion laser. However this property has little significance for the present work since sapphire is normally used as a substrate material and most laser light is expected to be absorbed in the top film.

Chapter 5

Probes for Material Characterization

5.1 Introduction

A wide variety of experimental probes are presently available for studying the structural properties or elemental composition of semiconducting materials. Those to be used in the present work include Raman spectroscopy, ellipsometry, electron microscopy and secondary ion mass spectroscopy. This chapter reviews the physical principles underlying the operation of these probes.

5.2 Raman Scattering

When light of frequency ω_0 is incident on a molecule or solid material, most of the scattered radiation also has frequency ω_0 . However a small portion of the scattered photons may lose energy to a vibrational mode giving a so-called Stokes line at frequency $\omega' = \omega_0 - \omega_1$. Photons may also gain energy from a vibrational mode giving an anti-Stokes line at $\omega' = \omega_0 + \omega_1$. The frequency ω_1 is characteristic of the vibrational mode and thus of the material structure.

In classical terms one may regard the Raman effect as arising from the strain dependence of the electronic polarizability. Writing the

polarizability as a Taylor series in the phonon amplitude u gives

$$P_0 = \eta_0 + \eta_1 u + \eta_2 u^2 + \dots \quad (5.1)$$

If the incident electric field is $E = E_0 \cos \omega_0 t$ and the phonon amplitude is $u = u_0 \cos \omega_1 t$ then the electric dipole moment contains the first order component

$$\eta_1 E_0 u_0 \cos(\omega_0 t) \cdot \cos(\omega_1 t) = 1/2 \eta_1 E_0 u_0 [\cos(\omega_0 + \omega_1)t + \cos(\omega_0 - \omega_1)t]. \quad (5.2)$$

Classical electromagnetic theory indicates that this oscillating dipole should radiate, giving both the Stokes and anti-Stokes lines.

The intensity of the Stokes line involves the matrix element for phonon creation while the anti-Stokes line involves phonon annihilation. Since phonon energies are distributed according to the Bose-Einstein distribution, the intensity ratio is approximated by [115]

$$\frac{I(\omega_0 - \omega_1)}{I(\omega_0 + \omega_1)} = \exp \left[\frac{\hbar \omega_1}{kT} \right]. \quad (5.3)$$

By measuring the relative intensities of the Stokes and anti-Stokes lines, it is possible to determine the sample temperature. In most experimental work however it is common to measure only the more intense Stokes line.

5.2.1 Raman Scattering in Crystalline Silicon

In crystalline silicon, first order Raman scattering occurs from the optical phonon near the center of the Brillouin zone, ie. $k \approx 0$. Because photon wavevectors are small compared to the dimensions of the Brillouin zone, phonons away from the zone center do not contribute. The selection rules for a one phonon process follow from conservation of energy and crystal momentum and can be written as

$$\hbar\omega' = \hbar\omega_0 \pm \hbar\omega_1(\vec{k}) \quad (5.4)$$

and

$$\hbar nq' = \hbar nq \pm \hbar k \quad (5.5)$$

where k is the phonon wavevector and nq and nq' are the incident and scattered photon wavevectors respectively. n is the refractive index of the crystal. In the above equations the lower signs refer to phonon emission (the Stokes component) and the upper signs refer to phonon annihilation (the anti-Stokes component).

At 300 K the optical phonon energy for silicon is 0.063 eV and this gives a Raman peak at wavenumber 520 cm^{-1} . The wavenumber of this peak can be shifted slightly upward by the application of compressive stress or slightly downward by the application of tensile stress [116]. In heavily doped samples, a shift can also occur due to phonon deformation potential interactions with free carriers. This

shift is to lower wavenumbers and is more pronounced in p-type material [117,118].

5.2.2 Raman Scattering in Amorphous Silicon

In amorphous semiconductors, long range order is absent and vibrational modes may extend only over a few tens of angstroms. From the Heisenberg uncertainty principle $\Delta x \Delta k \sim 2\pi$, it follows that k is no longer a "good quantum number" and the selection rule, eq. 5.5, no longer applies. Indeed the damped exponential factor $\exp(-ikr-r/\Lambda)$ characteristic of localized modes contains a Fourier spectrum of k values, all of which contribute to Raman scattering.

The Raman spectrum in amorphous silicon is proportional to the phonon density of states but also contains the Bose-Einstein factor, the $1/\omega$ harmonic oscillator factor and the relevant transition probabilities [119]. The spectrum has a broad peak centered at 480 cm^{-1} . Calculations by Beeman et al. [120] show that the width of this peak increases roughly linearly with the rms value of bond angle distortions of the network.

5.2.3 Raman Scattering in Polycrystalline Silicon

Raman scattering has proved to be a powerful tool for characterizing the structural quality of polycrystalline silicon films. The information obtainable from the Raman spectrum derives from the following points:

- In films which are only partially crystallized the Raman spectrum contains a superposition of the sharp peak characteristic of single crystal silicon and the broad peak characteristic of the amorphous matrix. The ratio of the integrated intensities of these peaks provides a relative measure of the amount of amorphous content.
- The crystalline perfection can be measured from the intensity of the 520 cm^{-1} peak above the background.
- Lattice perturbations and internal strain cause the 520 cm^{-1} line to broaden, mainly on the low wavenumber side. A relative measure of these disturbances can be obtained by comparing the Raman linewidth of the polysilicon sample to that of a single crystal standard.

In polycrystalline silicon with grain size less than $\sim 15\text{ nm}$, some additional effects occur due to the finite size of the crystallites. With decreasing crystallite size, the frequency of the crystalline peak decreases while the linewidth increases [121]. This is due to the partial relaxation of the $k = 0$ selection rule [122]. In addition to these changes, an amorphous-like peak appears in the vicinity of 480 to 498 cm^{-1} . Iqbal and Veprek [122] associate this peak with crystallite surface modes and suggest that surface-like modes of Si clusters may also contribute to the 480 cm^{-1} peak in amorphous Si. In experimental work, it is not possible to observe a continuous change to the amorphous spectrum as the crystallite size decreases because below 3 nm , the crystallites are unstable and a discontinuous change to the amorphous phase occurs [122].

5.3 Ellipsometry

Ellipsometry is a simple and convenient technique for determining the optical properties of thin film materials. In this technique elliptically polarized light is obtained by passing monochromatic light through a polarizer followed by a quarter wave plate. The beam is then directed onto the sample surface at an angle of incidence typically about 70° . The polarization of the reflected light is dependent on the complex index of refraction of the top sample layer. If this layer is transparent or semitransparent, the reflected polarization is also affected by the top layer thickness and the properties of the underlying substrate. In general, there is a unique rotation of the incident polarizer that will result in the reflected light having a linear polarization. The reflected light is then passed through another polarizer (usually referred to as the analyzer) and onto a photodetector. In ellipsometry, the polarizer and analyzer rotations required to obtain a null on the photodetector are recorded. From these values, properties of the material structure can be calculated.

Ellipsometer measurements can be used to obtain any two parameters of a material system provided all other relevant parameters are known. For example, in a single layer structure, the real and imaginary parts of the complex index of refraction can be determined. For a transparent material on a substrate of known properties, both the real part of the refractive index and the thickness of the top

layer can be determined. Formulae for calculating these quantities from ellipsometer data are given in ref [123].

In the present work ellipsometry will be used to detect crystallization in annealed amorphous silicon. The refractive index of amorphous silicon is substantially different from that of crystalline silicon and this difference can be easily detected. The difference in refractive index appears largely in the imaginary part which is related to the absorption coefficient.

5.4 Electron Microscopy

In an optical microscope the maximum magnification is limited to about 1200X and the depth of field at this magnification is small. This has led to the increased popularity of electron microscopy. The de Broglie wavelength associated with high energy electrons is much smaller than the wavelength of optical photons, making possible a much higher resolution. In the transmission electron microscope (TEM) a resolution of $\sim 5 \text{ \AA}$ can be achieved. For the scanning electron microscope (SEM) the minimum resolution is $\sim 100 \text{ \AA}$.

5.4.1 Transmission Microscopy

In the transmission electron microscope an electron beam is generated by a tungsten filament and is focussed onto the sample using electrostatic or magnetic lenses. The sample itself must be less than $1000 \text{ \AA}$ thick and is held under vacuum conditions. The

electrons are then transmitted through the sample and are focussed onto a film or fluorescent screen. In the standard operating mode the complete sample image is displayed instantaneously. However in some instruments it is possible to scan a narrow beam and then process the signal electronically to improve image contrast. This is referred to as scanning transmission electron microscopy or STEM.

Most electrons passing through a sample either lose very little energy or an amount of energy less than 50 eV. The latter loss is due to interactions with valence or conduction band electrons. Other incident electrons lose a greater amount of energy through generation of K-shell x-ray photons. The amount of energy lost in the K-shell interactions is characteristic of the particular element and can be used for elemental analysis [124]. This is referred to as electron energy loss spectroscopy or EELS.

5.4.2 Electron Diffraction

Electrons passing through a periodic lattice are diffracted according to the Bragg law. By slightly changing the TEM optics, a diffraction pattern rather than a surface image can be obtained. The diffraction pattern for a single crystal sample contains an array of spots which are characteristic of the crystal orientation. In addition to spots there may also be so-called Kikuchi lines. These are also characteristic of the crystal orientation and are associated with diffraction of electrons that have been inelastically scattered

[122].

In polycrystalline samples of random orientation the diffraction spots fall on a set of concentric rings. Each ring corresponds to a different orientation and the radii are related to the spacing of atomic planes [125]. If the grains are very small compared to the size of the illuminated region, the individual spots may no longer be discernable and the rings will appear continuous. In amorphous samples continuous rings are also observed. In this case the radii are related to nearest neighbor distances and the rings are somewhat broader due to the distribution of bond angles in the amorphous structure.

5.4.3 Scanning Electron Microscopy

In scanning electron microscopy the signal is obtained from the top surface of the sample and the restrictions on sample thickness no longer apply. As the beam is scanned, signals emitted from the electron illuminated region are detected and are used to control the image on a cathode ray tube. A variety of signals can be used for this purpose [126]. These include primary or secondary backscattered electrons, Auger electrons and x-ray photons. The latter two are characteristic of the excited atom and can be used for elemental analysis. In addition to these, some materials may also emit light by cathodoluminescence. For semiconductor device applications, it is common to use electron beam induced currents to generate an image.

5.5 Secondary Ion Mass Spectroscopy

Secondary ion mass spectroscopy (SIMS) is often used to measure dopant concentration profiles in semiconducting materials. In SIMS analysis the sample is bombarded with an ion beam, usually argon, and material is locally sputtered. Emitted secondary ions are then identified and counted using a mass spectrometer. Careful calibration is required in order to ensure constant sputtering rates and to ensure a minimum contribution from the sides of the sputtered hole. In some applications the ion beam may be raster scanned to give an elemental map of the sample surface.

Chapter 6

Modeling of Heat Flow in Multilayer CW Laser-annealed Structures

6.1 Introduction

In this chapter a numerical method is developed for solving the three dimensional heat flow equation for scanning cw laser annealing. The method is a generalization of an earlier work by Schvan and Thomas [96,97] which considered the case of a single layer structure annealed by a circular laser beam. The present work considers multilayer structures annealed by an elliptical laser beam. The use of elliptical beams has been found advantageous in certain applications like lateral seeding where larger defect free regions can be obtained [127]. The elliptical geometry can be achieved by using a nonzero angle of incidence or by using a cylindrical lens.

The numerical method involves splitting the three dimensional heat flow equation into three coupled one dimensional equations, thus reducing the required number of grid points. Results of the method are compared to melt threshold measurements in silicon-on-sapphire. The difference between theory and experiment is examined in detail and the sources of the small observed error are identified. A three-layer structure is then considered, silicon with a thin buried oxide, and the dynamics of melting are examined.

6.2 Numerical Model

In order to write the heat flow equation in a form which is valid both above and below the melting temperature we introduce the heat enthalpy function H . This quantity gives the total heat absorbed in a laser annealed sample including the latent heat of fusion. It can be written as

$$H(T) = \int_{T_B}^T c(T') \rho(T') dT' + \vartheta(T) H_f, \quad (6.1)$$

where T_B is the bulk substrate temperature, H_f the latent heat of fusion and ϑ the unit step function changing from 0 to 1 at the melting temperature T_m . For purposes of numerical computation ϑ can be replaced by a continuous function which rises over a suitably small temperature range. The three dimensional heat flow equation, expressed in Cartesian coordinates, is then

$$\frac{\partial H}{\partial t} = \frac{\partial}{\partial x} \left[k(T) \frac{\partial T}{\partial x} \right] + \frac{\partial}{\partial y} \left[k(T) \frac{\partial T}{\partial y} \right] + \frac{\partial}{\partial z} \left[k(T) \frac{\partial T}{\partial z} \right] + (1-R)S(x,y,z,t), \quad (6.2)$$

To simulate the effect of an elliptical Gaussian beam scanning in the x direction we use the stationary source function:

$$S = \frac{P}{\pi \beta w^2} \exp \left(-\frac{x^2}{w^2} - \frac{y^2}{\beta^2 w^2} - \frac{y^2 t^2}{w^2} \right) \alpha(T) \exp \left[-\int_0^z \alpha(z') dz' \right], \quad (6.3)$$

where P is the incident laser power, $\alpha(T)$ the optical absorption coefficient, v the scan velocity and t the time. W and δW are the $1/e$ intensity lengths in the x and y directions respectively.

The stationary source function given above is an approximation of the true source function for a scanning Gaussian beam. The approximation is valid only near the z axis and is used in order to take advantage of the resulting spatial symmetry. Figure 6.1 shows the true source function for a scanning Gaussian beam and the stationary source approximation. It is clear that along the z axis the stationary source has the correct intensity at all times but neglects the gradient in the source function present for $t \neq 0$. This approximation is justified by noting that most of the heating along the z axis will occur near $t = 0$.

Because of the symmetry noted above we now assume that the temperature distribution can be approximated by the Gaussian function:

$$T(x,y,z,t) = T_z(z,t) \exp \left[\frac{x^2 L_x(z,t)}{4 T_z} + \frac{y^2 L_y(z,t)}{4 T_z} \right] + T_0, \quad (6.4)$$

where T_z is the temperature rise along the z axis measured with respect to either the bulk temperature in the solid phase or the melting temperature in the liquid phase. The functions L_x and L_y are negative quantities which characterize the temperature distributions in the x - and y directions respectively. It will become clear from the next equation that these quantities, defined in the above manner, are directly proportional to the lateral heat flow. By substituting eq.

a) b)

Figure 6.1. x dependence of the source function for a scanning Gaussian beam: a) true source function, b) stationary source approximation.

(6.4) into eq. (6.2), then taking $x=y=0$, it follows that

$$\frac{\partial H}{\partial t} = \frac{k(L_x + L_y)}{2} + \frac{\partial}{\partial z} \left[k \frac{\partial T_z}{\partial z} \right] + (1-R)S. \quad (6.5)$$

The above one dimensional equation can be solved for the temperature rise along the z axis provided accurate calculations can be made of the lateral heat flow terms L_x and L_y . A first estimate of these quantities can be derived by assuming the characteristic $1/e$ decay lengths associated with the temperature distribution to be the same as those associated with the source function, ie.

$$\sqrt{4T_z/L_x} = W, \text{ and } \sqrt{4T_z/L_y} = BW \quad (6.6)$$

However because of lateral heat diffusion, the characteristic lengths associated with the temperature distribution should be somewhat larger than these values. To derive a more accurate equation describing the time evolution of L_x , we take the second partial derivative of eq. (6.2) with respect to x , then take $x = y = 0$. A similar equation for L_y follows by taking the second partial derivative with respect to y . The results are:

$$\begin{aligned} \frac{\partial H_x}{\partial t} = & \frac{3kL_x^2}{2T_z} + \frac{kL_xL_y}{2T_z} + \frac{\partial}{\partial z} \left[k \frac{\partial L_x}{\partial z} \right] - \left[\frac{(1-R)}{W^2} + \frac{\partial R}{\partial T} L_x \right] S, \\ & + \frac{\partial k}{\partial T} \left\{ \frac{3L_x^2}{2} + \frac{L_xL_y}{2} + \frac{\partial}{\partial z} \left[L_x \frac{\partial T_z}{\partial z} \right] \right\} + \frac{\partial^2 k}{\partial T^2} \left(\frac{\partial T_z}{\partial z} \right)^2 L_x \end{aligned} \quad (6.7)$$

and

$$\frac{\partial H_y}{\partial t} = \frac{3kL_y^2}{2T_z} + \frac{kL_xL_y}{2T_z} + \frac{\partial}{\partial z} \left[k \frac{\partial L_y}{\partial z} \right] - \left[\frac{(1-R)}{\beta^2 W^2} + \frac{\partial R}{\partial T} L_y \right] S, \\ + \frac{\partial k}{\partial T} \left\{ \frac{3L_y^2}{2} + \frac{L_xL_y}{2} + \frac{\partial}{\partial z} \left[\frac{L_y \partial T_z}{\partial z} \right] \right\} + \frac{\partial^2 k}{\partial T^2} \left(\frac{\partial T_z}{\partial z} \right)^2 L_y \quad (6.8)$$

where $H_x = L_x [c\rho - \delta(T-T_m)H_f]$ and $H_y = L_y [c\rho + \delta(T-T_m)H_f]$. δ is the Dirac delta function. The simultaneous solution of these coupled equations will yield the temperature rise $T_z(z,t)$ along the z axis.

In the original derivation by Schvan and Thomas the terms in $\partial k / \partial T$ and $\partial^2 k / \partial T^2$ in the lateral diffusion equation were neglected (in the more general formulation presented here these terms are the second lines of eqs. 6.7 and 6.8). However it turns out that this neglect is quite prudent. It will be seen in sect. 6.4 that the small error resulting from this neglect partially cancels that resulting from the approximation in the source function. For this reason these terms will also be neglected in the present work. The full temperature dependence of the thermal conductivity is still retained in the primary equation, eq. 6.5.

At the interface between two thermally conducting regions we require continuity of $k \partial T / \partial z$. It can be shown from eq. (6.4) that this implies continuity of $k \partial T_z / \partial z$ as the boundary condition for eq. (6.5) and continuity of $k \partial L_x / \partial z$ and $k \partial L_y / \partial z$ as boundary conditions for eqs. (6.7) and (6.8) respectively. At the top surface

we require $\partial T_z / \partial z = 0$, $\partial L_x / \partial z = 0$ and $\partial L_y / \partial z = 0$, while at the bottom surface we have $T_z = L_x = L_y = 0$.

The backward Euler implicit method [128] has been found efficient for solving nonlinear partial differential equations and is used in the present work. The computational details follow those described by Schvab and Thomas [96,97] with only minor modifications. For multilayer structures the spatial grid must be adjusted so that the internal boundaries fall exactly on a grid point. The difference equations for these points are then derived from the boundary conditions rather than from the heat flow equation. The z axis is divided into 90 grid points distributed over 250 μm . The grid spacing is narrow near the top surface of the sample and is wide near the bottom. The time steps are adjusted after each iteration in order to ensure convergence with efficient calculation.

In many instances it is only necessary to solve two of the three coupled equations. In the case of a circular laser beam, $\beta = 1$, we have $L_x = L_y$ and eqs. (6.7) and (6.8) become identical. For large β the lateral diffusion in the x direction is dominant and we need only solve eqs. (6.5) and (6.7) while using the approximate relation $L_y = L_x / \beta^2$. Figure 6.2 illustrates the effect of this approximation. The laser power threshold required to melt the surface of a silicon wafer is shown plotted as a function of the eccentricity β . The calculation assumed a substrate temperature of 500 K, a laser wavelength of 5145 Å and $W = 5 \mu\text{m}$. The material properties were as described in chapter 4. It is clear that the two-equation solution is

Figure 6.2 Laser power required for surface melting of silicon as a function of the beam eccentricity. The minimum $1/e$ intensity length of the laser beam is $5 \mu\text{m}$ and the substrate temperature is 500 K . The results were calculated using both the three equation solution and the approximate two equation solution.

generally sufficient for high scan velocity while the three equation solution may be required for low scan velocity. The curves are near-linear since the dominant effect of increasing β is to cause a proportionate decrease in the laser intensity.

With the three equation solution for $\beta = 6$, the $1/e$ decay lengths associated with the temperature profile were about 25% larger than W in the x direction and about 7% larger than βW in the y direction. These characteristic lengths showed little variation with time or with depth into the sample.

6.3 Comparison with Experiment

Alestig and Holmen [73] have recently measured the laser power threshold required to melt the surface of a 0.6 μm silicon layer on sapphire. They used a cw Ar ion laser operating in the TEM_{00} mode on the 5145 Å line. The circular beam was focussed to a 19 μm radius by a 150 mm focal length lens. In order to check the validity of the computational method described above the melting thresholds were calculated for the same laser conditions. These values are presented in table 6.1 along with those measured by Alestig and Holmen. The agreement between theory and experiment is generally good with the maximum difference being approximately 10 per cent.

Table 6.1 also presents for comparison the melt threshold values calculated by Alestig and Holmen using the analytical solution of Burgener and Reedy [93]. This solution uses the Green's function

Table 6.1 Laser power required for surface melting in 0.6 μm silicon-on-sapphire.

Substrate Temperature (K)	Scan Velocity ($\mu\text{m/s}$)	Melting Threshold (W)		
		Measured (ref. 73)	Calculated (present work)	Calculated (ref. 73)
300	1	2.1	1.92	2.14
	10	2.3	2.25	2.35
	100	4.4	4.17	3.77
400	1	1.7	1.64	1.70
	10	1.95	1.95	1.92
	100	3.9	3.68	3.25
500	1	1.4	1.43	1.47
	10	1.7	1.70	1.70
	100	3.4	3.27	3.09
600	1	1.2	1.25	1.26
	10	1.45	1.50	1.50
	100	2.9	2.91	2.85
700	1	1.0	1.10	1.06
	10	1.2	1.33	1.29
	100	2.5	2.59	2.57

method and requires temperature-independent values for the thermal diffusivity. Since this approximation is not strictly valid for silicon-on-sapphire, it is found that significant errors occur for high scan velocity with low to moderate substrate temperature. For other annealing conditions generally good agreement with experiment is obtained.

The Green's function method may not be adequate for some processing applications since high throughput requires high scan velocity. Furthermore the method becomes increasingly complex as more layers are added to the structure [94]. The method is also restricted to temperatures up to but not beyond the melting threshold. The numerical method presented here can handle many-layer structures as well as the nonlinearities associated with melting.

6.4 Error Analysis

A number of approximations have been used in the numerical model just described. It is likely that the most significant of these are the use of a stationary source function in place of the moving source and the neglect of the temperature dependence of the thermal conductivity in the lateral diffusion equations. The effects of these approximations are now examined. It will be seen that these two approximations lead to errors of opposite sign which partially cancel.

6.4.1 The Stationary Source Approximation

The moving source function S_{ms} for an elliptical laser beam scanning in the x direction can be written as

$$S_{ms} = \frac{P}{\pi B W^2} \exp \left[-\frac{(x - vt)^2}{W^2} - \frac{y^2}{B^2 W^2} \right] F(z), \quad (6.9)$$

where the function $F(z)$ describes the depth distribution into the sample. In the stationary source approximation the moving source S_{ms} is replaced by a stationary source S_{ss} centered on the z axis, namely

$$S_{ss} = \frac{P}{\pi B W^2} \exp \left[-\frac{x^2}{W^2} - \frac{y^2}{B^2 W^2} - \frac{v^2 t^2}{W^2} \right] F(z). \quad (6.10)$$

A quantitative estimate of the error introduced by the stationary source approximation can be obtained from the Green's function solution of the heat flow equation for a single layer structure. Assuming a constant thermal diffusivity, the linearized temperature rise can be written as a product of the source and Green's functions, integrated over space and time:

$$\theta = \iiint_{-\infty}^{\infty} \int_{-\infty}^{\infty} S(x', y', z', t') G(x', y', z', t' | x, y, z, t) dx' dy' dz' dt', \quad (6.11)$$

The Green's function for the linearized heat flow problem can be written as [92]

$$G = \frac{\exp \left[- \frac{(x - x')^2 + (y - y')^2 + (z - z')^2}{4 D (t - t')} \right]}{c \rho [4 \pi D (t - t')]^{3/2}} \quad (6.12)$$

By using the above formulas the linearized temperature θ_{ms} resulting from the moving source S_{ms} and the linearized temperature θ_{ss} resulting from the stationary source S_{ss} can be calculated. An estimate of the error can then be obtained.

To simplify the calculation it will be assumed that all of the radiation is absorbed at the surface of the sample, ie. $F(z) = \delta(z)$. This allows all of the integrations over the spatial variables to be carried out analytically. Since we are usually interested in the maximum temperature which is reached at the top surface, x , y and z are set equal to zero and t is chosen to be the time t_m at which the maximum temperature is reached. This time occurs just after the laser intensity reaches its peak and is slightly different for the stationary and moving sources. The error expressed in per cent is then

$$\% \text{ Error} = 100 \times \left[\frac{\theta_{ms} - \theta_{ss}}{\theta_{ms}} \right] \quad (6.13)$$

By using eqs. 6.9 - 6.13 and carrying out the integrations over x' , y' and z' it follows that

$$\% \text{ Error} = 100 \times \left[1 - \frac{\int_0^\infty \frac{du}{\sqrt{(u^2+1)(u^2+\beta^2)}} \exp \left\{ - \left(\frac{vt_m}{W} - \frac{vu^2}{4v_o} \right)^2 \right\}}{\int_0^\infty \frac{du}{\sqrt{(u^2+1)(u^2+\beta^2)}} \exp \left\{ - \frac{\left(\frac{vt_m}{W} - \frac{vu^2}{4v_o} \right)^2}{1+u^2} \right\}} \right] \quad (6.14)$$

where we have used the change of variable

$$u = \sqrt{4D(t-t')/W^2}, \quad (6.15)$$

and

$$v_o = D/W. \quad (6.16)$$

Figure 6.3 shows the error calculated from eq. 6.14 using numerical integration. It is seen that the error is small for both low and high scan velocity and approaches a maximum near $v = v_o$. In silicon at high temperature the thermal diffusivity D is about $0.13 \text{ cm}^2/\text{s}$. Combined with a W of 20 microns, this gives $v_o \sim 65 \text{ cm/s}$. The maximum error near this point is less than 15 % for a circular laser beam but becomes progressively worse for larger beam eccentricity. This occurs because the stationary source approximation primarily affects heat flow in the x direction and this component becomes comparatively more important as the beam spreads in the y direction.

Figure 6.3 Error introduced by the stationary source approximation as a function of laser scan velocity.

Clearly the stationary source approximation should be used with some caution for beam eccentricities greater than about 3.

It is important to note that for a given laser power, the stationary source approximation consistently underestimates the maximum temperature occurring in the sample. Stated conversely, the laser power required to produce a given maximum temperature is overestimated by the approximation.

6.4.2 Neglect of $\partial k / \partial T$ and $\partial^2 k / \partial T^2$ terms

In most materials, the thermal conductivity increases with decreasing temperature. As one moves laterally away from a laser heated region, the thermal conductivity rises, allowing more heat to diffuse. If this rise in thermal conductivity is neglected in the lateral heat flow equations, less heat will be seen to escape and the temperature at the center of the beam will be overestimated. This is the opposite effect of the stationary source approximation.

If the substrate temperature during laser annealing is high, the temperature variation of the thermal conductivity has little effect. In this case the stationary source approximation should provide the primary source of error and the laser power for a given maximum temperature should be overestimated. This is indeed confirmed by the data of table 6.1. On the other hand, the temperature dependence of the thermal conductivity is more important for low substrate temperatures and an underestimate may then occur. This is also

confirmed by table 6.1. The table shows that in the middle temperature range, 400 - 600 K, the various sources of error nearly cancel giving a net error generally less than 5 per cent.

6.5 Dynamics of Melting

In this section the dynamics of melting are examined for a silicon sample having a thin oxide layer buried 0.4 μm below the surface, as shown in fig. 6.4. This kind of structure is typical of that used in a lateral seeding process where liquid phase epitaxy is initiated in windows in the oxide and is extended laterally by translation of the laser beam. In the present work the perturbation in the heat flow analysis introduced by the windows is neglected.

We consider a sample with a 0.2 μm buried oxide scanned with a 7.8 watt circular laser beam having velocity 100 cm/s. The $1/e$ intensity radius of the beam is 20 μm , the wavelength is 5145 Å and the substrate temperature is 500 K. Figure 6.5 shows the temperature profiles into the sample at various times during the laser scan. The surface of the silicon is found to melt shortly before the laser intensity reaches its peak. The temperature gradient in melted silicon is smaller due to its higher thermal conductivity. Once melting begins, the further temperature rise is small in the top silicon but still substantial below.

In fig. 6.6 the depth of melting is shown as a function of time for a variety of laser powers above the melting threshold. There is

Figure 6.4 Silicon-on-oxide structure for lateral seeding process.

Figure 6.5 Temperature profiles in a silicon wafer with a $0.2 \mu m$ oxide layer buried $0.4 \mu m$ below the surface. The heating is induced by a $7.8 W$ circular laser beam of $1/e$ intensity radius $20 \mu m$. The scan velocity is $100 cm/s$ and the substrate temperature is $500 K$. The maximum laser intensity occurs at time $t=0$.

2

MicroD

Figure 6.6 Melt depth as a function of time for a cw laser scanned silicon sample with a $0.2 \mu\text{m}$ oxide buried $0.4 \mu\text{m}$ below the surface. The $1/e$ intensity radius of the beam is $20 \mu\text{m}$, the scan velocity is 100 cm/s and the substrate temperature is 500 K .

a broad range of powers for which only a thin layer of silicon is melted. This is the result of negative feedback produced by thin film reflectance phenomenon in the melt pool. The reflectivity of silicon increases with melt depth, approaching a maximum for depths in excess of $0.03 \mu\text{m}$ [95]. Once melting has extended beyond this point the maximum melt depth increases rapidly with laser power until the oxide interface is reached. For the laser powers examined, the maximum melt penetration occurs just after the peak laser intensity and well before the trailing $1/e$ intensity point.

To explore the influence of the buried oxide layer we show in fig. 6.7 the maximum melt penetration as a function of laser power, for a variety of oxide thicknesses. Because of the lower thermal conductivity of silicon dioxide, the laser power required to melt to a given depth is reduced for increasing oxide thickness. In a lateral seeding process the laser power required to melt to the substrate in the window region may be very near that required to induce damage in the silicon over the oxide. For this reason patterned anti-reflection coatings which reduce the reflectivity in the window regions only have been employed [129]. We also note that the presence of a buried oxide layer substantially increases the sensitivity of the maximum melt depth to laser power. Accurate control over the depth of melting is possible only in wafers without a buried oxide, scanned at high velocity.

In fig. 6.7 it is seen that the tails resulting from thin film reflectance phenomenon are present both with and without the buried

Figure 6.7 Maximum melt penetration as a function of laser power for a variety of scan speeds and buried oxide thicknesses. The $1/e$ intensity radius of the beam is 20 μm and the substrate temperature is 500 K.

oxide but are reduced in width for decreasing scan velocity. That these widths should decrease seems reasonable on physical grounds since for low scan velocity temperature gradients are reduced and less additional energy is required to melt to a given depth. However the tails should not disappear entirely as is suggested by fig. 6.7 for $v = 25$ cm/s. Indeed, tails are expected even for zero scan velocity [95]. Thus it appears that the numerical method, while fairly accurate for calculating temperatures up to the melting threshold, has diminished accuracy for calculating melt depths at low scan velocity. There are a number of factors which may contribute to this result. First, the melt depth is a sensitive function of the temperature profile and accuracy in the latter will not in general yield accuracy in the former. Second, we are monitoring the time evolution of a process, which for low scan velocity, is approaching steady state. Since the numerical computation must extend over a long time period, less accuracy in numerical computation is expected.

It should be noted that a scan velocity may be considered slow if it is small compared to $V_0 = D/W$. Furthermore, a scan velocity which is not slow for solid phase processing may become slow for liquid phase processing due to the three-fold increase in thermal diffusivity which occurs upon melting.

Schvan and Thomas [97] have measured the laser power required to melt to a depth of $0.3 \mu\text{m}$ in a silicon wafer. Their results are shown in fig. 6.8 for a variety of scan speeds. The figure also shows the required values of laser power which they calculated using the

Figure 6.8 Measured and calculated values of laser power required to melt to a depth of 0.3 μm in single crystal silicon (ref 97)

method described here. At 25 cm/s the laser power required to melt to 0.3 μm is slightly greater than the calculated value. This result can be explained by assuming that the laser power required for surface melting is accurately calculated but that a tail should be added to the maximum melt depth vs. laser power characteristic. This would push the calculated power for 0.3 μm melt depth closer to the measured value. The agreement between theory and experiment appears fairly good between 50 and 100 cm/s but degrades again after 150 cm/s.

Chapter 7

Deposition and Furnace Annealing Experiments

7.1 Introduction

The structural quality of polycrystalline silicon is dependent on the conditions of crystallization since further structural changes upon annealing are constrained to some extent by the initial polycrystalline structure. Harbeck et al. [33] found that only material which is deposited amorphous and is crystallized later has high quality in terms of smoothness, internal strain and lithographic properties. Their studies considered crystallization temperatures from 900 to 1000° C, approaching the acceptable limit for small geometry devices.

The present chapter reports on the properties of in-situ phosphorus doped LPCVD silicon which is deposited amorphous at 560° C and is crystallized later at 650° C. Comparisons are made to similarly doped polysilicon deposited at 627° C. The effect of further annealing at 900° C is also examined. The films were characterized using resistivity measurements, secondary ion mass spectroscopy, transmission electron microscopy and Raman spectroscopy. In general, the amorphous deposited material was found to have higher phosphorus incorporation, better structural quality and lower resistivity. A variety of physical mechanisms are proposed to explain these results.

7.2 Experimental

Substrates were prepared by growing a 1000 Å thermal oxide on <100> silicon wafers. Amorphous silicon was then deposited in a hot wall LPCVD reactor at a temperature of 560° C. Polycrystalline films were deposited in the same reactor at a temperature of 627° C. In both cases the silane flow was approximately 45 cm³/min, resulting in a pressure of 0.3 torr. In-situ phosphorus doping was achieved by addition of PH₃ diluted in SiH₄ to the gas mixture. In order to ensure uniform deposits, all source gases were admitted through a gas manifold extending along the length of the tube and the wafer load was covered by a quartz half cylinder. The deposition rate decreased with increasing PH₃ flow and ranged from 5 to 19 Å/min for the amorphous-deposited material and from 28 to 82 Å/min for the polycrystalline-deposited material.

After the silicon depositions, a 1000 Å oxide was deposited by low pressure oxidation of silane at a temperature of 406° C. This layer serves to prevent escape of phosphorus during subsequent anneals. The amorphous films were then crystallized by annealing for one hour at 650° C. Half of these were given an additional anneal for one hour at 900° C. Of the polycrystalline-deposited films, half were given no anneal while the rest were annealed for one hour at 650° C followed by one hour at 900° C. For the resistivity measurements, Van der Pauw cross patterns were etched using standard photolithographic

techniques. Unpatterned sections were used for SIMS analysis and for Raman spectroscopy.

The films for resistivity measurements were deposited to thicknesses in the range from 1000 to 4500 Å as determined by a Dektak IIA surface profilometer. Films for Raman spectroscopy were deposited thicker (~ 7000 Å) in order to eliminate contributions to the Raman signal originating from the substrate.

The process outlined above was modified slightly for the films used for transmission electron microscopy. The substrate wafers had the oxide thickened by depositing ~ 1 micron SiO_2 by LPCVD. The silicon depositions were then performed with a SiH_4/PH_3 flow ratio of 100/1 and the deposition thicknesses was ~ 600 Å. After patterning, the wafers were immersed in 10% HF for 2 hours causing portions of the film to lift off. The floating films were then scooped onto copper screens and sent for TEM.

7.3 Results

7.3.1 Dopant Concentration and Resistivity

Tables 7.1 and 7.2 summarize the phosphorus concentration results obtained from SIMS analysis for samples deposited at 560°C and 627°C respectively. The corresponding resistivity results are also shown. These results indicate that for the same silane to phosphine flow ratio, films deposited at 560° C have approximately four times the

Table 7.1 Properties of phosphorus doped films deposited at 560°C.

The annealing duration was 60 min at each of the temperatures indicated. Film thickness ~ 2500 Å.

Flow ratio SiH ₄ /PH ₃	P concentration cm ⁻³	Anneal temp. (°C)	Resistivity ohm - cm
600:1	2.1 x 10 ²⁰	650	2.5 x 10 ⁻³
600:1	2.1 x 10 ²⁰	650 & 900	1.2 x 10 ⁻³
300:1	5.2 x 10 ²⁰	650	2.5 x 10 ⁻³
300:1	5.2 x 10 ²⁰	650 & 900	1.0 x 10 ⁻³
150:1	not measured	650	3.5 x 10 ⁻³
150:1	not measured	650 & 900	8.2 x 10 ⁻⁴

Table 7.2 Properties of phosphorus doped films deposited at 627°C.

The annealing duration was 60 min at each of the temperatures indicated. Film thickness ~ 2500 Å.

Flow ratio SiH ₄ /PH ₃	P concentration cm ⁻³	Anneal temp. (°C)	Resistivity ohm - cm
600:1	5 x 10 ¹⁹	no anneal	6.1 x 10 ⁻²
600:1	5 x 10 ¹⁹	650 & 900	3.9 x 10 ⁻²
300:1	1.4 x 10 ²⁰	no anneal	1.4 x 10 ⁻²
300:1	1.4 x 10 ²⁰	650 & 900	2.1 x 10 ⁻³
150:1	not measured	no anneal	1.8 x 10 ⁻²
150:1	not measured	650 & 900	1.3 x 10 ⁻³

phosphorus concentration as films deposited at 627° C. After high temperature annealing, the corresponding resistivity ratio was somewhat less than four-to-one due to saturation of the resistivity vs. dopant concentration characteristic. On the other hand, films deposited at 560° C and crystallized at low temperature had a substantially lower resistivity than as-deposited 627° C films, even when the dopant concentrations were similar.

In films deposited with the lowest phosphine flow, there was a noticeable decrease of resistivity with increasing film thickness. This effect was more pronounced in films deposited at 627° C. In more heavily doped films, much less variation with film thickness was observed. The dependence of resistivity on film thickness has also been observed by Learn and Foster [35] and is likely connected with the larger grain size expected for thicker films.

7.3.2 Transmission Electron Microscopy

Two samples were prepared for transmission electron microscopy, one deposited at 560°C and crystallized at 650°C and the other deposited at 627° C with no further anneal. The TEM inspection was carried out at the National Research Council. Figure 7.1 shows the TEM images and diffraction patterns for the two samples. The images suggest an average grain size of ~ 800 Å and 270 Å respectively. Some fine structure is also visible within the individual grains. That, the amorphous-deposited film has larger grain size is confirmed by the electron diffraction patterns. For the same imaging conditions,

100 nm

Figure 7.1 TEM images and electron diffraction patterns for Si films a) deposited polycrystalline at 627° C, and b) deposited amorphous at 560° C and crystallized at 650°C. The magnification in the TEM images is 75,000 x and the camera constant for the diffraction patterns is 27 mm-Å.

the diffraction rings are continuous for the polycrystalline-deposited material and spotty for the amorphous-deposited material.

7.3.3 Raman Scattering

Raman scattering measurements were carried out in the Department of Chemistry at Carleton University using the 5145 Å line of an argon ion laser. The beam was focussed through a microscope lens to a diameter of approximately 1.5 microns and the laser power was 2 mW. Under these conditions the laser beam is not expected to alter the sample structure. The scattered radiation was collected by a double monochromator whose frequency window was slowly scanned over the desired spectral range. The output was filtered with a 10 sec time constant and displayed on a chart recorder. The Raman measurement apparatus unfortunately did not have an internal calibration standard which is necessary for intensity comparisons from sample-to-sample. However a considerable amount of data is still available by comparing frequency shifts and relative features within individual spectra.

Figure 7.2 shows the Raman spectra for films deposited with a SiH_4/PH_3 flow ratio of 600/1. In the as-deposited 627° C film the tail on the low wavenumber side appears to be rising toward an amorphous peak. The same tail for the amorphous-deposited film crystallized at 650° C appears more flat. Both of these tails were lowered by high temperature annealing.

In order to more thoroughly investigate the amorphous peak, the

Figure 7.2

Raman spectra of in-situ phosphorus doped LPCVD silicon films. The deposition and annealing temperatures are respectively: a) 627°C, no anneal, b) 627°C, 650 & 900°C c) 560°C, 650°C, d) 560, 650 & 900°C. Panel d also shows the Raman spectrum for bulk single crystal silicon (dotted curve).

Raman measurement was later repeated with a wider frequency scan. Both unannealed polycrystalline-deposited films and amorphous-deposited films crystallized at 650°C were examined. A faster frequency scan was used with a 1 sec time constant and the laser power was increased to 15 mW. The resulting spectra contained a considerable amount of noise but nevertheless suggested a larger amorphous component in the polycrystalline-deposited film.

In order to conduct a comparison of the Raman line shapes, the background was subtracted from the crystalline peaks of fig. 7.2 and the peak heights were normalized. Figure 7.3 shows the result for polycrystalline silicon deposited at 627°C . The figure also shows for comparison the Raman spectrum for bulk single crystal silicon. The Raman linewidth at one fifth of the peak (indicated in the figure) is 18 per cent larger in the polycrystalline material. Such a film is significantly strained and may be unsuitable for certain device applications. After high temperature annealing, the linewidth was reduced to a value only 7 per cent larger than that of the single crystal. The film deposited amorphous at 560°C and crystallized later at 650°C had a linewidth 6 percent larger than that of the single crystal. Further annealing at 900°C produced little change.

Compared to bulk single crystal silicon, the Raman peaks for the polycrystalline-deposited material appear to be shifted to a slightly higher wavenumber. On the other hand, the peaks for the amorphous-deposited material appear to be shifted to a slightly lower wavenumber. This suggests that the residual stress is compres-

Figure 7.3 Normalized Raman spectrum of bulk single crystal silicon (dashed curve) and polycrystalline silicon deposited at 627°C (solid curve).

sive in the former and tensile in the latter. Tensile stress is indeed expected in amorphous-deposited material due to the small increase in density which occurs upon crystallization [130]. We note however that in the amorphous-deposited films, which are more heavily doped, free carrier interactions should also contribute to the downward shift. In neither film type should grain size effects be important since the TEM results show the grains to be too large.

7.4 Discussion

During chemical vapor deposition phosphorus incorporation into the growing film may depend on a number of factors including film structure, deposition temperature and deposition rate. Because these factors are not entirely independent, careful interpretation of the available data is required to determine which plays the more significant role. We begin this discussion by considering the film structure during deposition and its possible effect on phosphorus incorporation. This is followed by a discussion of the effect of deposition temperature and deposition rate. Finally we discuss the resistivity results and the effect of high temperature annealing.

There is a growing body of experimental evidence suggesting that at 627° C crystallization is near-coincident with surface adsorption. Bisaro et al. [36] suggest that the preponderance of <220> orientation in undoped polysilicon deposited at temperatures in this vicinity, is associated with nucleation at the surface in contact with the gas phase. The poorer structural quality of polycrystalline

deposited films observed in the present work and by Harbeke et al. [33] may well be connected with this surface crystallization.

In films which crystallize quickly upon deposition the bonding configurations in the surface region are clearly different from those of a disordered material and this may have an influence on phosphorus incorporation. It seems likely that phosphorus incorporation would be greater in disordered material due to the possibility of satisfying a larger proportion of the five bonds per phosphorus atom. Moreover there is some reason to believe that a disordered structure may also assist the initial breakdown of adsorbed phosphine. Tsu et al. [131] have found that molecular hydrogen breaks down on internal surfaces of microvoids in amorphous silicon but does not break down on cleaved c-Si surfaces. They attribute this behavior to high electric fields in amorphous silicon caused by bond angle deviations from the tetrahedral angle.

In as-deposited CVD polysilicon in-situ doped with arsenic, dopant segregation to grain boundaries has been observed using scanning transmission electron microscopy [132]. This observation tends to support the notion that local bonding configurations can affect dopant incorporation. An attempt was made to confirm the presence or absence of dopant segregation in the samples used in the present work using electron energy loss spectroscopy. However this task turned out to be beyond the resolution capability of the instrument.

Learn and Foster [35] recently conducted an extensive study of phosphorus incorporation in LPCVD polysilicon. They measured phosphorus incorporation for several temperatures from 560 to 675° C

and found a continuously increasing phosphorus concentration with decreasing deposition temperature. Within the accuracy limits of their data the characteristic appears to be linear and without any kink at the crystallization threshold. This would appear to argue against a significant effect of material structure.

The effect of temperature on phosphine adsorption has recently been studied by Yu et al. [34,133]. They found that on <100> silicon a peak in phosphorus coverage occurs at 550° C. Below this temperature adsorbed phosphine is not entirely decomposed and above this temperature phosphorus begins to desorb. However the data of Yu et al. indicates that the difference in phosphorus coverage at 627° C and 560° C is only about 30%. Thus it seems unlikely that the temperature effect alone would be sufficient to explain the four-to-one difference in phosphorus incorporation observed in the present work.

For a given SiH_4/PH_3 flow ratio the deposition rate at 560° C was about four to five times slower than at 627° C. It is possible that this reduced deposition rate increases the ability of phosphorus to compete for surface sites. This possibility has also been suggested by Learn and Foster [35]. Experiments by these authors showed that in radially nonuniform depositions there was a direct correlation between phosphorus incorporation and the local film thickness or deposition rate.

Considering all of the above factors it seems likely that the deposition rate plays the dominant role in controlling phosphorus incorporation, with material structure and deposition temperature

contributing to a lesser extent.

In polycrystalline silicon the grain size is an important factor in determining electrical resistivity [134]. The larger grain size of amorphous-deposited films may well explain why these films have substantially lower resistivity than polycrystalline-deposited films even when the dopant concentrations are similar.

An additional factor which may also contribute to the lower resistivity of amorphous-deposited films is reduced dopant segregation to grain boundaries. It has already been noted that films deposited in the polycrystalline form may exhibit dopant segregation. However films which are deposited amorphous should have relatively uniform phosphorus concentration. If these films are crystallized later at 650°C, or later during the deposition time, the distribution should remain uniform due to the low diffusivity of phosphorus at these temperatures.

In polycrystalline silicon heavily doped with phosphorus, significant grain growth is possible upon high temperature annealing [33]. This effect likely contributes to the decrease in resistivity of amorphous-deposited films further annealed at 900° C. The greater decrease in resistivity of polycrystalline-deposited films annealed at 900°C likely results from both grain growth and dopant desegregation. These effects are not unrelated since separation of phosphorus from a grain boundary may result either from phosphorus diffusion or from movement of the boundary itself. In both the 560 and the 627° C films, increased dopant activation within the grains should also contribute to the lower resistivity at higher annealing temperatures.

Chapter 8

Laser Annealing Experiments and Characterization

8.1 Introduction

The resistivity values for furnace annealed LPCVD silicon presented in the previous chapter are considerably larger than those of bulk single crystal silicon of similar doping. Much higher temperatures are clearly required for optimal annealing. Previous studies have shown that implantation-doped polycrystalline silicon annealed by a scanning cw laser can have resistivity equivalent to bulk single crystal silicon [9,80]. The present chapter explores for the first time the effect of cw laser annealing on in-situ phosphorus doped LPCVD amorphous and polycrystalline silicon. It is seen that in this case as well resistivities equivalent to the bulk single crystal can be obtained. The chapter also presents data on the uniformity of laser annealed material and on the presence of laser damage. These properties are correlated with the onset of laser induced melting. Raman spectra are also presented.

It should be emphasized that while heavily doped films suitable for gates or bipolar emitters are used in the present studies, it is possible that many of the conclusions regarding dopant activation, uniformity and structure are also valid for lighter doped films suitable for passive resistors or active device regions.

8.2 Experimental

8.2.1 Wafer Preparation

Wafers used in the laser annealing experiments were prepared in the same manner as those used in the furnace annealing experiments described in chapter 7. The substrates were <100> silicon wafers with a 1000 Å thermally grown oxide. Deposited silicon films had thicknesses of about 2400 Å. In the furnace annealing experiments a 1000 Å oxide was deposited on top of the amorphous or polycrystalline silicon in order to prevent escape of phosphorus during annealing. In the laser annealing experiments the top oxide was deposited to thickness 960 Å and serves as an anti-reflection coating. This layer also helps to contain fluid flow during liquid phase processing. Most of the samples were in-situ doped with phosphorus as described previously. However during the later stages of the experimental work, diborane gas lines were installed in the LPCVD system. This permitted the deposition of in-situ boron doped silicon and two such samples were also examined.

8.2.2 Laser Scanning Apparatus

The laser used in the present work is a coherent CR-18SC argon ion laser operating on wavelength lines from 488 to 514 nm. The maximum output power is 18 W. The beam is directed through a beam expander and then onto a mirror which deflects the beam horizontally by 90°.

The beam then hits a second mirror which deflects it downward through a focussing lens and onto the sample chuck. The second mirror is attached to a motor whose angular deflection causes the beam to scan. During laser annealing, the beam scans at a constant rate and then snaps back quickly to its starting position. After each scan a stepping motor causes the mirror platform to step perpendicular to the direction of scanning. In this way multiple overlapping scans can be obtained. All of these operations are controlled by a KIM-1 microcomputer. A schematic diagram of the laser scanning apparatus is shown in fig. 8.1.

The beam expander mentioned above serves primarily to increase the laser spot size on the deflecting mirrors, thus minimizing the possibility of mirror damage. A 160 mm lens was used to focus the beam and this gave a spot diameter on the sample surface of about 40 μ m. The spot size was estimated by measuring the widths of laser crystallized regions produced by single laser scans. The experiments used multiple scans spaced by 6 μ m. The scan velocity was 15 cm/s.

The sample chuck is resistively heated and was held at a temperature of 600 K. The height of the chuck is continuously variable and was adjusted so that the silicon wafer lies near the focal point of the beam, approximately 160 mm below the lens.

The laser is equipped with an internal photodetector which measures the intensity of a portion of light deflected off the main beam. In order to determine a calibration factor which yields the intensity at the sample surface, the following procedure was used.

Figure 8.1 Laser scanning apparatus and timing diagram.

The laser power required to melt the surface of the polycrystalline layer in the experimental samples was estimated. This was done by looking for a change of slope in the resistivity vs. laser power characteristic. This point appeared to approximately coincide with the onset of a noticeably larger grain size. The laser power required for surface melting was then calculated using the computer algorithm described in chapter 6. The computer calculations used the material parameters described in chapter 4 and assumed a laser spot size of 40 μm . The calibration factor was then determined as the ratio of measured and calculated values of the melting threshold. It should be noted that the laser spot size assumed in the calculations is in fact of little significance since results will be presented as a function of the ratio P/W .

8.3 Resistivity and Uniformity of Laser Annealed Silicon

As in the previous chapter the resistivity was measured using Van der Pauw cross patterns which were etched after annealing. While these patterns provide a convenient method of measuring sheet resistance, they also provide a means for checking sample uniformity. Figure 8.2a shows a Van der Pauw cross configuration in which current flows approximately parallel to the direction of the laser scan. A perpendicular configuration is shown in fig. 8.2b. In uniform samples these two configurations should yield identical results. For nonuniform samples, different results may be obtained.

Figure 8.2 Van der Pauw cross configurations for sheet resistance measurement. a) parallel configuration, b) perpendicular configuration. Sheet resistance = $4.532 \text{ V/I ohm/square}$.

8.3.1 Laser Annealing of Amorphous Silicon

Figure 8.3 shows the resistivity as a function of laser power per characteristic radius, P/W , for an amorphous silicon sample deposited with a SiH_4/PH_3 flow ratio of 150/1. The open circles are results measured in the parallel configuration while the shaded circles are results measured in the perpendicular configuration. The figure also shows the calculated maximum temperature which occurs in the deposited film during a laser scan. Below about $0.12 \text{ W}/\mu\text{m}$ the laser power was insufficient to crystallize the amorphous film and the resistivity was very high, indeed immeasurable in many cases. Just after crystallization began, the resistivity dropped to a fairly low value, but the films were highly nonuniform. The resistivities were generally lower in the parallel configuration. For higher laser power, the resistivity dropped further and the uniformity improved. The best uniformity was achieved after the threshold of surface melting, and before the threshold of complete melting to the oxide. In one case, the resistivities in the parallel and perpendicular configurations were identical. The resistivity near this point was just under 0.3 mohm-cm . After the onset of surface melting, the further temperature rise is expected to level off due to the higher reflectivity of the melt. Complete melting down to the buried oxide did not occur until P/W reached $0.21 \text{ W}/\mu\text{m}$. This threshold was characterized by the onset of asperities in the buried oxide caused by the wetting action of molten silicon (the detection of these asperities will be discussed in detail in sect. 8.6). The uniformity was found to degrade again

Figure 8.3 Resistivity vs. P/W for in-situ phosphorus doped LPCVD amorphous silicon. $\circ$: parallel configuration, $\bullet$: perpendicular configuration. For the three points with the lowest laser power, the resistivities in the perpendicular configuration are 1.8, 1.9 and 1.5 mohm-cm (low power to high). The calculated maximum temperature of the film during laser annealing is also shown.

after this point.

Figure 8.4 shows the resistivity as a function of P/W for boron doped amorphous silicon. This material was deposited at 450° C with a $\text{SiH}_4/\text{B}_2\text{H}_6$ flow ratio of 250/1. The results appear quite similar to those of the phosphorus doped film.

The temperature profiles shown in figs. 8.3 and 8.4 were calculated assuming for the deposited Si films, the optical and thermal properties appropriate to polycrystalline silicon. This is justified by the following considerations. First of all, it is likely that because of the substantial overlap of adjacent scans, the material at the center of a given laser scan will already have been crystallized by the previous scan. Furthermore for such a thin film, the much lower thermal conductivity of amorphous silicon has relatively little effect. When the temperature calculations were repeated with the thermal conductivity of the top layer reduced by the factor 10, the maximum temperature rise at the crystallization threshold was only about 18% larger. The slightly larger reflectivity of amorphous silicon would also be expected to partially offset this increase. The melting thresholds were observed to be nearly the same for amorphous and polycrystalline films. The latter observation is in accord with previous observations by Alestig and Holmen for silicon on sapphire [73].

The temperature at the crystallization threshold was calculated to be about 1050°C. This is somewhat larger than the 600°C crystallization temperature observed for furnace annealed samples. A larger value

Figure 8.4 Resistivity vs. P/W for in-situ boron doped LPCVD amorphous silicon. o : parallel configuration, • : perpendicular configuration. The calculated maximum temperature of the film during laser annealing is also shown.

is, indeed, expected due to the shorter duration of laser induced heating.

8.3.2 Laser Annealing of Polycrystalline Silicon

Resistivity data for a phosphorus doped film which was deposited in the polycrystalline form is shown in fig. 8.5. For zero laser power a relatively large but measureable resistivity was found and the material was uniform. Beyond about $0.065 \text{ W}/\mu\text{m}$ the resistivity began to drop and nonuniformity became apparent. The nonuniformity was quite excessive near $0.12 \text{ W}/\mu\text{m}$ but began to decrease again as the melting threshold was approached. Once again, the best uniformity was achieved after the onset of surface melting and before the onset of complete melting to the buried oxide.

In comparing the amorphous-deposited and polycrystalline-deposited films, it is clear that there is a significant difference in sensitivity to laser power. Below the threshold of surface melting the resistivity of the phosphorus doped amorphous film of fig 8.3 decreased by about $200 \text{ mohm-cm}^2/\text{W}$. The corresponding drop in the polycrystalline-deposited film was $7000 \text{ mohm-cm}^2/\text{W}$, about 35 times larger.

8.3.3 Comparison with Bulk Single Crystal Silicon

The minimum resistivities obtained with laser annealing are considerably below those reported in the previous chapter for furnace

Figure 8.5 Resistivity vs. P/W for in-situ phosphorus doped LPCVD polycrystalline silicon. ○ : parallel configuration, ● : perpendicular configuration. The calculated maximum temperature of the film during laser annealing is also shown.

annealed films. Figure 8.6 shows the minimum resistivity of laser annealed films as a function of phosphorus concentration determined from SIMS analysis. The figure also shows for comparison the resistivity of bulk single crystal silicon [135]. The two points with the lowest phosphorus concentration are for films deposited in the polycrystalline form and these lie quite close to the curve for single crystal silicon. The point with the highest phosphorus concentration is for an amorphous-deposited film and it lies somewhat above the single crystal curve. The deviation in this case may be connected with the high phosphorus concentration, which in this case, exceeds the solubility limit.

8.4 Raman Scattering

Raman spectra were measured for the same laser annealed samples whose resistivity values were presented in figs. 8.3 and 8.5. The measurement again used the 5145 Å line of an argon ion laser with spot size and laser power 1.5 mm and 15 mW respectively. A relatively fast frequency scan was used with 1 sec time constant. The resulting spectra are shown in fig. 8.7. The tails of these spectra originally contained a considerable amount of noise but this has been suppressed by drawing straight line segments through the average of the scatter.

Figures 8.7a and 8.7b show the Raman spectra for the sections of the polycrystalline-deposited film annealed with P/W values of 0.05 and 0.15 W/mm respectively. It is clear that the higher laser power

Figure 8.6 Minimum resistivity vs phosphorus concentration for laser annealed silicon films. The solid curve shows values for bulk single crystal silicon obtained from ref [135].

Figure 8.7 Raman spectra for laser annealed in-situ phosphorus doped LPCVD silicon: a) polycrystalline-deposited, $P/W = 0.05$ W/ μ m, b) polycrystalline deposited, $P/W = 0.15$ W/ μ m, c) amorphous-deposited, $P/W = 0.12$ W/ μ m (solid curve: light band, dotted curve: dark band), d) amorphous-deposited, $P/W = 0.15$ W/ μ m (dotted curve: bulk single crystal silicon).

has caused the tail on the low wavenumber side to be lowered with respect to the peak, thus indicating improved crystallinity. Both spectra appear to peak near 520 cm^{-1} , with the spectrum of fig. 8.7b possibly being shifted down slightly.

Figure 8.7c shows the Raman spectrum for the section of the amorphous-deposited film annealed with P/W value $0.12\text{ W}/\mu\text{m}$. This value was very near the crystallization threshold. Visual inspection showed this section to be composed of alternating light and dark bands and Raman spectra were taken from each. The results clearly show the light bands to be crystalline and the dark bands to be amorphous. The spectrum shown for a crystalline band peaks at 512 cm^{-1} , which is considerably below the usual crystalline location. A shift of this magnitude is unlikely to be caused by free electron interactions alone and clearly suggests a significantly different structure from the ideal crystal. This is probably caused by the extremely heavy doping which in this case exceeds the solubility limit. A similarly large Raman shift has also been observed previously by Tsu [136] for silicon heavily implanted with arsenic.

The Raman spectrum for the section of the amorphous-deposited film annealed with P/W value $0.13\text{ W}/\mu\text{m}$ is shown in fig. 8.7d. This section was much more uniform and showed only an occasional dark band. The spectrum appears quite similar to the crystalline band of the $0.12\text{ W}/\mu\text{m}$ section except that the peak is shifted up to about 515 cm^{-1} . The tail on the low wavenumber side appears not to be lowered by the higher laser power. A section annealed at $0.22\text{ W}/\mu\text{m}$

was also examined and the spectrum (not shown) was little different from the 0.15 W/ μ m section.

8.5 Film Texture

After completing the Raman scattering measurements the laser annealed samples were treated in Wright etch [137] and inspected using an optical microscope. In the sections of the polycrystalline-deposited sample annealed with P/W values less than about 0.12 W/ μ m, the grain structure could not be discerned. At 0.153 W/ μ m both fine grained regions and regions containing large grains, typically $6 \times 2.5 \mu$ m could be seen. The large grains were usually longer in the direction parallel to the laser scan. Just below 0.21 W/ μ m a larger proportion of the grains were of the larger size and many were oriented at 45° to the laser scan. Above 0.21 W/ μ m the grains appeared roughly the same size but were slightly less directional.

In the section of the amorphous-deposited sample annealed with P/W value 0.12 W/ μ m, only a very fine grain structure could be discerned. At 0.153 W/ μ m some ring-shaped regions resembling explosive crystallization could be seen. In other regions annealed with the same laser power long thin grains about $8 \times 1.4 \mu$ m could be seen running either parallel or at 45° to the direction of laser scanning. Just below 0.21 W/ μ m large grains could also be seen but these were either perpendicular or at 45° to the direction of scanning.

8.6 Surface Roughness and Laser Damage

After the laser annealed samples were patterned they were inspected for physical damage using a Dektak IIA surface profilometer. The profilometer consists of a stylus which is translated across the sample and causes variations in surface height to be recorded.

In general, silicon films which were laser annealed in the solid phase appeared only slightly rougher than films which were not laser annealed. Likewise, films which were laser annealed just above the threshold of complete melting appeared only slightly rougher than films which were laser annealed in the solid phase. However more interesting variations in surface roughness were observed in the silicon dioxide underlying the silicon. Figure 8.8a shows a Dektak profile for the region surrounding a silicon island. The profile runs perpendicular to the direction of laser scanning, and the P/W value was $0.23 \text{ W}/\mu\text{m}$, well above the threshold of complete melting. Interestingly, the underlying silicon dioxide appears much rougher than the silicon itself. The asperities on the silicon dioxide are likely due to the wetting action of molten silicon. The fact that the silicon appears smoother is likely because the molten silicon was able to flow back into place, whereas the silicon dioxide was probably only softened. Figure 8.8b shows a Dektak profile over the underlying silicon dioxide for a laser power which is smaller but still in the complete melting regime. The asperities in the oxide are now of smaller height. These asperities disappear entirely for

a)

b)

c)

Figure 8.8 Dektak surface profiles perpendicular to direction of scanning: a) across silicon island annealed with $P/W = 0.23 \text{ W}/\mu\text{m}$; b) across underlying SiO_2 annealed with $P/W = 0.22 \text{ W}/\mu\text{m}$; c) across silicon island annealed with $P/W = 0.24 \text{ W}/\mu\text{m}$.

P/W values below $0.21 \text{ W}/\mu\text{m}$, which we interpret as the threshold of complete melting of the top silicon layer.

For laser powers significantly greater than the melting threshold, it is possible to severely damage the silicon film. Figure 8.8c shows a Dektak profile for a region annealed with $P/W = 0.24 \text{ W}/\mu\text{m}$. It is apparent that the laser has actually etched grooves into the silicon, with molten silicon being thrown off to the sides. This occurred even though there was a $960 \text{ \AA}$ silicon dioxide antireflection coating on the silicon during annealing, this layer being etched off later. In some cases the grooves also penetrated into the underlying silicon dioxide.

8.7 Discussion

Severe nonuniformity in cw laser annealed silicon on insulator has been found previously by Gat et al. [9] using Van der Pauw cross resistivity measurements. However they considered only a limited range of laser powers and did not note an improvement in uniformity just below the threshold of complete melting.

In the amorphous-deposited films annealed near the crystallization threshold the presence of alternating crystalline and amorphous bands would appear to explain the severe nonuniformity in the resistivity measurements. In the parallel configuration most of the current is able to channel down the crystalline bands while in the perpendicular configuration current is forced to traverse the high resistivity

amorphous bands. At higher laser power the amorphous bands are gradually eliminated but some nonuniformity remains likely because of the asymmetry in grain dimensions. Asymmetry in grain dimensions would also appear to explain the nonuniformity of polycrystalline deposited films annealed in the solid phase.

The nonuniformity which reappears beyond the threshold of complete melting is likely connected with the asperities observed in the underlying oxide. These asperities appear to be hills running parallel to the direction of laser scanning and would be expected to impede current flowing in this direction to a lesser extent than current flowing in the perpendicular direction. It is clear that in integrated circuit applications it is preferable to set the laser power just below this threshold in order to minimize this effect while still maintaining a resistivity equivalent to the bulk single crystal.

Chapter 9

Lateral Seeding

9.1 Introduction

In a limited class of applications polycrystalline silicon on insulator may have sufficient quality for device fabrication. However it is generally preferred that silicon films be single crystal of a specific orientation. A variety of techniques have been explored for producing these films. The most notable is liquid phase lateral seeding induced by a scanning cw laser or strip heater [138,139,140]. Solid phase lateral seeding induced by furnace annealing has also attracted considerable attention [141,142]. However in both these techniques there appears to be a fundamental limit on the maximum lateral distance that epitaxy can be extended.

The present chapter presents experimental results obtained by the author using both of the techniques mentioned above. A novel technique is then investigated for overcoming the limitations on lateral seeding distance. The novel technique is solid phase lateral seeding induced by a scanning cw laser or electron beam. A simplified theoretical analysis is developed which suggests the viability of this process should be examined experimentally. Some experimental results are then presented. While the theoretical analysis supports the viability of the process, the experimental results highlight certain practical considerations which appear to be detrimental.

9.2 Liquid Phase Lateral Seeding

9.2.1 Theory

In the lateral seeding process a silicon wafer is prepared with a thin patterned oxide and a thin silicon film is deposited on top. This type of structure was illustrated previously in fig. 6.4. Liquid phase epitaxy is then initiated in the windows in the oxide and is extended laterally by translation of the heat source.

It has been found that in the lateral seeding process there is a maximum lateral distance that epitaxial growth can be extended beyond the seeding trench. This maximum distance increases with increasing thickness of the deposited film [138] or with decreasing sweep speed [139]. Recent two dimensional computer simulations by Ohkura et al. [140] have clarified the reason for this behavior. The computer simulations showed that near the seeding trench, the receding melt/solid interface is approximately perpendicular to the wafer surface. As the melt front moves away from the seeding trench, the angle between the melt front and the oxide layer decreases from 90° . When the melt front comes close to being parallel with the oxide, lateral seeding is inhibited and resolidification occurs in the polycrystalline form.

9.2.2 Experiment

To examine the liquid phase lateral seeding process, substrates

were prepared by growing a 1000 Å thermal oxide on Si <100> wafers. The oxide was then patterned using standard photolithographic techniques. In lateral seeding experiments reported previously in the literature, polycrystalline films were usually deposited by CVD or LPCVD. However it was decided in the present work to use a film deposition technique which gives a cleaner, native oxide free interface with the silicon wafer. The films were therefore evaporated in an MBE reactor at the National Research Council. In this technique the wafers were first raised to temperatures in excess of 1000° C to remove all traces of native oxide in the wafer windows. Without breaking vacuum, the temperature was lowered to about 600° C and the silicon films were deposited. During deposition the silicon atoms were directed at an angle of incidence of 30° and the wafers were rotated in order to improve uniformity and step coverage. The resulting films were epitaxially aligned with the wafer in the window regions and were polycrystalline on the oxide. After the silicon depositions, a 960 Å silicon dioxide anti-reflection coating was deposited.

The laser annealing was accomplished using the same apparatus described in the previous chapter. However instead of scanning the beam by rotation of a deflecting mirror, the sample chuck was moved at the constant rate of 2.3 mm/s. A 160 mm lens was again used for focussing the beam and the substrate temperature was 600 K. Single nonoverlapping scan lines were used at a variety of laser powers. After annealing, the oxide anti-reflection coating was etched in 10%

HF and the wafers were treated in Secco etch [143] in order to expose the grain structure. The samples were then inspected under an optical microscope.

Figure 9.1 shows a photograph of a single laser scan running perpendicular to a horizontal seeding trench. This particular sample had film thickness $0.63 \mu\text{m}$ and the laser power was 2.7 W . On the trailing edge of the laser scan there appears to be a seeded region extending about $80 \mu\text{m}$ from the seeding trench. Figure 9.2 summarizes the lateral seeding distances observed in a variety of samples, as a function of film thickness. An increasing lateral seeding distance with increasing film thickness is clearly evident. The figure also shows data reported previously in the literature for CVD deposited films. Since the data found in the present work appears quite comparable, we conclude that the native oxide free interface in the MBE material does not provide significant improvement in the liquid phase lateral seeding process.

In silicon-on-insulator devices, a variety of considerations make it desirable for the crystalline films to be fairly thin. In MOS transistors an inversion layer can be formed more quickly if one need only deplete the thickness of the film rather than the characteristic depth associated with the channel doping. Junction capacitances are also reduced. A possible technique for obtaining these films is to use liquid phase lateral seeding in thick films and then thin the films later by oxidation or etching. However it is clearly preferable to obtain the epitaxial films by a method that is not as strongly affected by the original film thickness.

100 μm

Figure 9.1 Laser scan running perpendicular to seeding trench.
Lateral seeding distance = 80 μm .

Figure 9.2. Lateral seeding distance vs film thickness obtained using cw laser induced liquid phase lateral seeding.

9.3 Solid Phase Lateral Seeding: Theory

9.3.1 Furnace-Induced Lateral Seeding

In lateral solid phase epitaxy the silicon film is deposited in the amorphous form or is amorphized later by ion implantation. Special precautions must be taken to ensure that the interface with the crystal in the window regions is as clean as possible. The wafer is then heated in a furnace and solid phase epitaxy proceeds upward in the windows and then laterally onto the oxide. Experimental results have shown that for a given temperature, there is a maximum lateral seeding distance the epitaxy can extend before being inhibited by random nucleation of crystallites in the amorphous material [141,142]. This maximum distance depends on the properties of the amorphous material and on the temperature of the anneal.

In the heated amorphous layer there is a characteristic time t_R required for the volume fraction of crystalline material to reach a level sufficient to inhibit epitaxy. If this time is multiplied by the epitaxial growth velocity V_g , we obtain the maximum lateral seeding distance:

$$d_{\max} = t_R V_g \quad (9.1)$$

The epitaxial growth velocity as a function of temperature is

$$V_g = V_0 \exp[-E_g/kT] \quad (9.2)$$

while the time t_R is given by

$$t_R = t_n \exp[E_n/kT] , \quad (9.3)$$

and thus

$$d_{\max} = t_n v_0 \exp[(E_n - E_g)/kT] . \quad (9.4)$$

The activation energy E_n is partially related to the kinetics of nucleation and partially related to the kinetics of growth. It is therefore larger than E_g which is related to growth only. The maximum lateral seeding distance increases with decreasing annealing temperature but at the expense of a slower growth rate.

Ishiwara et al. [142] recently studied lateral solid phase epitaxy along the $\langle 010 \rangle$ direction in 2500 Å silicon films deposited by electron beam evaporation. The films were later implanted with silicon, boron or phosphorus. After annealing at 600° C for several hours, the maximum lateral seeding distances were 4.5, 6.5 and 44 μm in undoped, B-doped and P-doped films respectively. These authors indicate that the larger distances in the P-doped films results largely from a delay in polycrystallization.

For evaporated amorphous samples, it is important that the step height over the patterned oxide be small, preferably less than 500 Å. The evaporated films are otherwise porous near the step and this can inhibit epitaxy from extending over the edge [144].

9.3.2 Laser-Induced Lateral Seeding

Random nucleation of crystallites in the amorphous material can be suppressed if heat is applied only to the region near the epitaxial interface. This localized heating can be achieved using a focussed cw laser or electron beam. To the authors' knowledge this approach has not been reported previously in the literature.

Figure 9.3 shows a schematic diagram illustrating the solid phase lateral seeding process. The temperature profile produced by the leading edge of the heat source is shown approximated by a piecewise linear function. A change in slope is shown at the crystalline/amorphous interface due to the lower thermal conductivity of amorphous silicon. $T_{\max}$, T_i and T_s are the maximum temperature, temperature at the crystalline/amorphous interface and substrate temperature respectively. Δx is the distance over which the temperature changes from T_i to T_s . We assume that the temperature profile moves at the same velocity v as the heat source which is also equal to the epitaxial growth velocity. Under the right circumstances the latter condition should be maintained by negative feedback. If the crystalline/amorphous interface were to lag behind the heat source, the interface temperature would rise, causing the growth velocity to increase. Likewise, if the crystallization front were to outrun the heat source, the interface temperature would drop causing the growth velocity to decrease.

Figure 9.3 Schematic diagram showing temperature profiles for laser induced lateral solid phase epitaxy.

We now consider the point P indicated in the figure. We define F_c as the volume fraction of material which is crystalline at this point. Initially, F_c is zero. By the time the crystalline/amorphous interface reaches P, we would like F_c to be less than the amount "A" required to inhibit epitaxy. If this condition is satisfied, lateral solid phase epitaxy can be extended indefinitely.

If t_R is the time required for the crystalline fraction to obtain the value A, then the average crystallization rate is A/t_R . The crystalline fraction F_c is then

$$F_c = \int A/t_R dt = \int A dt / t_n \exp[E_n/kT(t)] \quad (9.5)$$

This equation assumes a constant crystallization rate for a given temperature and neglects the delay time for steady state nucleation. The temperature T varies with time according to

$$T = T_s + (T_i - T_s) vt/\Delta x \quad (9.6)$$

Substituting these results into the requirement $F_c < A$ gives

$$\int_0^{\Delta x/v} \exp \left[\frac{-E_n/k}{T_s + (T_i - T_s) vt/\Delta x} \right] dt < t_n \quad (9.7)$$

The integral in the above equation cannot be evaluated analytically. However an excellent approximation can be obtained by replacing the integrand by the function Ct^N where C and N are chosen to match the

integrand and its first derivative at $t = \Delta x/v$. This procedure gives the result

$$\exp \left[\frac{-E_n}{kT_1} \right] \left(\frac{kT_1^2}{E_n v} \right) \left[\frac{\Delta x}{T_i - T_s} \right] < t_n \quad (9.8)$$

The first factor on the left hand side of the above equation is simply the inverse of the temperature gradient. The scan velocity v must be equal to the epitaxial growth velocity g_s given by eq. (9.2) with $T = T_1$. By using these results and the definition of $d_{\max}$ given by eq. (9.4), the above equation can be rewritten as

$$T_1 > \frac{kT_1^2}{E_n d_{\max}(T_1)} \quad (9.9)$$

Thus the lateral solid phase epitaxy process can proceed indefinitely provided the heat source can maintain a temperature gradient greater than the critical value given by eq. (9.9). This equation also indicates that whatever material properties will yield the maximum lateral seeding distance in the furnace annealing process, will also permit sustained laser-induced epitaxy with the minimum temperature gradient.

9.4 Solid Phase Lateral Seeding: Experiment

9.4.1 Initial Experiments

In the course of the present work a large number of unsuccessful attempts were made to initiate solid phase epitaxy, before success was finally achieved. The initial experiments used both undoped and in-situ phosphorus doped amorphous silicon deposited by LPCVD at 550 or 560° C. The films were deposited onto <100> silicon wafers which were half covered by a 1000 Å thermal oxide. The substrates were given an RCA clean and 10% HF dip immediately before insertion into the reactor. Deposited films typically had thickness from 2000 to 3000 Å. The films were then annealed at a variety of temperatures between 550 and 600° C and were frequently removed from the furnace to check for crystallization using ellipsometry. If epitaxy were to occur before random crystallization, one would expect to find crystallization first over the bare silicon and later over the oxide. However crystallization was found to occur either simultaneously in the two regions or first over the oxide.

The problems in initiating solid phase epitaxy were likely caused by the interfacial native oxide which inevitably forms before deposition. Although epitaxy has been reported previously in LPCVD films [50], it seems likely that there may be system-to-system variations in the amount of native oxide grown. To deal with this problem two separate approaches were tried with LPCVD films. In the first, undoped material was given a heavy silicon implant in order to

break up the native oxide. The implant was done at the University of British Columbia using the energy and dose prescribed by Sigmon and Tseng [48]. In the second approach in-situ phosphorus doped polysilicon was annealed for two and one half hours at 1225° C in order to produce epitaxial alignment. The films were then amorphized by silicon implantation, also at U.B.C.. Both of these attempts proved unsuccessful. A possible reason for this failure is that the ion implanter at U.B.C. lacks a temperature controlled end station and the films may not have been fully amorphized. In fact, it was found that the films on oxide showed random crystallization very quickly at 600° C. Implanted amorphous films should normally withstand this temperature for many hours without such crystallization.

Several attempts were also made to achieve lateral solid phase epitaxy using films deposited in the MBE reactor at NRC. The substrates were prepared as previously described except that the field oxide was usually etched to less than 500 Å in 10% HF in order to reduce step coverage problems. Two types of deposition were then used, a high temperature deposition ($T > 500^{\circ} \text{C}$) giving crystalline material, and a low temperature deposition ($T \sim 100^{\circ} \text{C}$) giving amorphous material. The high temperature material was epitaxially aligned with the substrate in regions where the substrate was exposed and was polycrystalline over the field oxide. These films were later amorphized by phosphorus implantation at U.B.C.. However they failed to show lateral solid phase epitaxy, likely for the same reason outlined above. The amorphous-deposited films were first annealed at

500° C without breaking vacuum in order to reduce the void density in the amorphous structure [145]. They were then subject to the usual furnace annealing experiments from 550 to 600° C but failed to show lateral growth before random crystallization. SEM inspection at QRL showed the material on the oxide to be polycrystalline right up to the edge of the seeding trenches. Imperfect continuity of the film density over the oxide steps may have been the problem although it is not entirely clear that this is so.

9.4.2 Furnace-induced Lateral Seeding and Random Crystallization

Solid phase lateral seeding was finally achieved using material supplied by Northern Telecom Electronics. The samples were prepared by oxygen implantation into p-⟨100⟩ silicon wafers, followed by high temperature annealing. This process gave a top layer of single crystal silicon with thickness 1700 Å and an underlying oxide of thickness 3000 Å. Although the top silicon films already had the desired crystallinity, they were later amorphized in selected regions to provide a test vehicle for studying lateral solid phase epitaxy.

The silicon-on-insulator films were selectively amorphized by phosphorus implantation through a photoresist mask. The photoresist was patterned into stripes running parallel and perpendicular to the ⟨110⟩ direction and having widths ranging from 10 to 100 microns. Phosphorus ions were then implanted at Northern Telecom with the following energies and doses: $1.1 \times 10^{15} \text{ cm}^{-2}$ @ 40 keV, $2.4 \times 10^{15} \text{ cm}^{-2}$ @ 90 keV and $5.4 \times 10^{15} \text{ cm}^{-2}$ @ 180 keV. This series of implants is

the same as that used by Ishiwara et al. [142] and gives an approximately uniform phosphorus concentration of $3 \times 10^{20} \text{ cm}^{-3}$. Those regions which were protected by photoresist during implantation remained crystalline and could be easily discerned by visual inspection. Thin film interference effects gave the crystalline regions a green colour, while the amorphous regions appeared greyish.

After ion implantation the wafers were cut into small rectangles and were cleaned for furnace annealing. The widths of the crystalline stripes were then measured under an optical microscope and the sections were annealed in Nitrogen ambient at a variety of temperatures from 580. to 650° C . The sections were frequently removed from the furnace and the stripe widths remeasured. The widths were found to increase linearly with time, indicating lateral epitaxial growth. An Arrhenius plot of the epitaxial growth velocity is shown in fig. 9.4. The activation energy is $2.75 \pm .15 \text{ eV}$, in reasonable agreement with values reported in the literature [38,39].

Some time after epitaxial growth began, random nucleation and growth of crystallites began to occur in the amorphous regions. This random crystallization occurred sooner for higher annealing temperatures and showed some variation from section to section. The random crystallization appears to be affected by stress in the films and was found to occur first at edges where the sections were cut or were handled with tweezers.

Figure 9.4 Arrhenius plot of lateral epitaxial growth velocity for 1700 Å silicon film on oxide.

Figure 9.5 shows a photograph of a sample annealed at 620°C for 6.8 hours. The picture shows both the crystalline stripes and extensive random crystallization. While the stripe widths continued to grow beyond this point, it is clear that they were beginning to engulf random crystallites and could no longer be considered single crystal.

In order to monitor random crystallization in a quantitative manner, a novel technique was employed using a standard ellipsometer. The ellipsometer used has a mercury lamp source filtered to give wavelength 5461 Å. The light was incident at an angle of 70° and illuminated a region of size $2.8 \times 1.0\text{ cm}$. Sections were cut from the periphery of the wafers where there were no crystalline stripes. These sections were only slightly larger than the ellipsometer illuminated region. They were then placed onto the ellipsometer platform and the polarizer and analyzer settings were adjusted to give zero current in the photomultiplier tube. These settings were maintained throughout the remainder of the experiment. After furnace annealing, the samples were again placed onto the ellipsometer platform and the photomultiplier current measured.

In samples which are fully crystallized by the anneal, a finite photomultiplier current is expected due to the different optical properties of crystalline and amorphous silicon. In samples which are partially crystallized, those regions which remained amorphous should contribute zero to the photomultiplier current, while the crystalline regions should contribute in direct proportion to the fraction of

100 μm

Figure 9.5 Amorphous silicon film with single-crystal stripes and extensive random crystallization. Film was annealed at 620° C for 6.8 hours.

total area which has crystallized. The photomultiplier current as a function of annealing time is shown in fig. 9.6 for samples annealed at 600 and 620°C. After the first annealing duration, the photomultiplier current was found to increase slightly even though there were no visible crystallites. This increase is likely due to structural relaxation of the amorphous material, which gives a slight change in refractive index [60]. After a certain delay time, the photomultiplier current began to rise rapidly until it saturated at about 32 μ A. This saturation value appears to be associated with the photomultiplier tube rather than with 100% crystallization. Microscopic inspection shows that the saturation current occurs at approximately 50% crystallization.

An Arrhenius plot of the random crystallization time is presented in fig. 9.7 for the temperature range 600 to 650°C. The figure shows both the nucleation time, derived from the intercepts of fig. 9.6, and the time for approximately 50% crystallization. At 600°C the times for nucleation and 50% crystallization were 15.5 and 22 hours respectively. If the latter time is multiplied by the epitaxial growth velocity for this temperature, one obtains a maximum lateral seeding distance of 28 microns. This is somewhat less than the 44 μ m value reported previously by Ishiwara et al. [142] for P doped films. This difference is primarily due to a lower growth velocity, the random crystallization time being approximately the same.

With furnace annealing experiments, it is only possible to measure random crystallization over a limited temperature range. Because of

Figure 9.6 Current measured in ellipsometer photomultiplier tube as a function of annealing time for initially amorphous Si films. The polarizer and analyzer settings were adjusted to yield a null for amorphous silicon.

Figure 9.7 Arrhenius plot of random crystallization time. o : nucleation time, + : time for approximately 50% crystallization.

this limitation, and because of the section-to-section variations in random crystallization noted previously, it is not possible to determine with accuracy the activation energy for random crystallization. However fig. 9.7 notes several values of activation energy obtained by fitting particular sets of points. These values range from 2.9 to 4.1 ev. By comparison, we note that Roth et al. [146] obtained values ranging from 3.16 to 4.44 ev in UHV deposited amorphous silicon. Their data were measured over a broad temperature range using laser heating and in-situ optical monitoring. Their lower value is for undoped material annealed in vacuum, while the larger value is for B-implanted material annealed in air.

9.4.3 Laser-induced Lateral Seeding

The results of the furnace annealing experiments can now be used to assess the viability of laser-induced solid phase lateral seeding. If we assume an activation energy of random crystallization of 3.75 ev., an activation energy of epitaxial growth of 2.75 ev. and a maximum lateral seeding distance of 28 μm at 600°C, then:

$$d_{\text{max}}(T_i) = 4.75 \times 10^{-5} \exp[1.0/kT_i] \quad \mu\text{m}. \quad (9.10)$$

We now assume that the laser beam can produce a temperature profile in the amorphous region whose characteristic 1/e decay length is 15 μm . Assuming the substrate is held at room temperature and the extrapolated maximum temperature is the melting point, we write

$$T(r) = 300 + 1390 \exp[-r^2/152] \text{ K.} \quad (9.11)$$

It can be shown from these equations that the maximum temperature gradient induced by the laser exceeds the value given by eq. (9.9) over a wide spatial region. The temperature gradient exactly equals the critical value at a distance of 9.1 μ m from the center of the temperature profile, where the temperature is 1262 K. Extrapolating the epitaxial growth velocity data of fig. 9.4 to this temperature gives a growth velocity of 28 μ m/s.

To demonstrate the sensitivity of the above calculation to the activation energy for random crystallization, these calculations were repeated using the value 4.0 eV. The critical temperature gradient then occurred at $r = 10.1 \mu$ m, where $T = 1181$ K. The corresponding epitaxial growth velocity was then 5 μ m/s.

If a laser annealing experiment were to use a scan velocity exceeding the critical values calculated above, sustained epitaxial growth would not be possible. The crystalline/amorphous interface would have to be located at a higher temperature point, where the temperature gradient would be too small. On the other hand, if a lower scan velocity were used, sustained lateral seeding should still be achieved but with the crystalline/amorphous interface located at a lower temperature point.

Numerous attempts were made to achieve laser-induced lateral solid phase epitaxy using the Northern Telecom samples. The experiments

were performed over a period of three to four weeks and a large variety of experimental conditions were used. Some of the samples were annealed as-received while others were first covered by a 960 Å deposited oxide. In both cases, some of the samples were first furnace annealed at 600° C for 80 min. before annealing with the laser. The preanneal was intended to serve two purposes. First, the resulting epitaxial growth causes the crystalline/amorphous interface to extend beyond the original mask edge where transverse effects during implantation could cause nonuniformities in amorphization or in phosphorus content. Second, the anneal may cause structural relaxation to an amorphous phase of lower free energy. This would reduce the likelihood of explosive crystallization.

The samples were laser annealed in air with the substrate at room temperature. The beam was scanned across the crystalline stripes in the perpendicular direction with velocity ranging from 1.5 to 2.5 $\mu\text{m/s}$. Numerous scans were used with powers ranging from below the crystallization threshold to above the melting threshold. The beam was focussed by a 50 mm lens. To provide a measure of the beam spot size, the widths of the laser-crystallized regions were measured after annealing. These were typically $\sim 10 \mu\text{m}$. In a later experiment the beam spot size was increased somewhat using a 160 mm lens and the substrate was heated to 500 K.

After laser annealing, the samples were treated in Wright etch and inspected under an optical microscope. However evidence of lateral epitaxy was unfortunately not seen in any of the scans. A polycrys-

talline grain structure was usually visible in the annealed regions. In some cases the grains appeared random while in others, a ring pattern resembling explosive crystallization could be discerned. Except where the laser power was sufficient to melt, a faint line was always visible across the original crystalline/amorphous interface.

9.5 Discussion

The results of the liquid phase lateral seeding experiments appear quite similar to those reported previously in the literature. The use of MBE material, with its clean interface, appears not to provide a significant advantage.

The solid phase furnace annealing experiments produced results which were similar to those of Ishiwawa et al. [142] except that the epitaxial growth velocity at 600°C was only half as fast. This difference can be explained by the $\langle 110 \rangle$ seeding direction used in the present work. Ishiwara et al. used a $\langle 010 \rangle$ seeding direction which is known to have a growth rate that is faster by a factor of 2.5 to 3 [38]. When this factor is taken into account it appears that the films used in the present work have a growth velocity that is quite comparable or perhaps slightly faster.

In very recent experiments, Warabisako et al. [147] studied lateral epitaxy in CVD polysilicon which was deposited at 1000°C and was amorphized by phosphorus implantation. They used a $\langle 110 \rangle$ seeding direction and found that the growth rate at 600°C was twice as large

as the value reported here. Clearly the high temperature CVD technique provides better film properties for the lateral seeding process.

Both Ishiwara et al. [142] and Warabisako et al. [147] reported results only for the single temperature and therefore did not provide activation energies for epitaxial growth or random crystallization.

The experiments on laser-induced solid phase epitaxy proved unsuccessful even though the theoretical analysis seemed to support the viability of the process. Either explosive crystallization or random crystallization was found to occur rather than epitaxy. It is possible that this result was caused by stress in the films produced by the large temperature gradient. It was already noted in the furnace annealing experiments that random crystallization occurred more quickly in regions of the film stressed by mechanical handling. Thus it may be that the large temperature gradient required by the theory is in fact fundamentally incompatible with the desired epitaxial growth.

Chapter 10

Conclusion and Further Work

This chapter summarizes the main results obtained in the present work. Special emphasis is placed on those results considered to be novel and of practical importance. Some suggestions are then given for further work.

10.1 Conclusion

This thesis has examined a variety of areas related to the deposition and annealing of amorphous and polycrystalline silicon. A number of new results have been obtained.

First, a recently developed technique for solving the transient heat flow equation for cw laser annealing has been extended to a more general case. The technique had previously been applied only to single layer structures annealed by a circular laser beam. The present work has extended the technique to multi-layer structures annealed by an elliptical laser beam. Results of the technique were compared to melt threshold measurements in silicon-on-sapphire and excellent agreement was obtained. The technique should prove to be a powerful tool for optimizing device structures and laser annealing parameters for future silicon-on-insulator technologies.

The deposition and furnace annealing of in-situ phosphorus doped

LPCVD amorphous and polycrystalline silicon was then examined. Phosphorus incorporation was found to be larger in the amorphous-deposited material and this was attributed mainly to the lower deposition rate. Depending on the phosphine flow, the phosphorus concentration was found to approach and even exceed the solid solubility limit. Such films clearly have potential as diffusion sources and are less likely to induce point defects than conventional sources.

The amorphous-deposited films were later crystallized by furnace annealing at 650°C. This temperature is considerably below those of previous experiments reported in the literature. The resulting material was found to have better structural quality and lower resistivity than material deposited in the polycrystalline form at 627°C. The lower resistivity was observed even when the dopant concentrations were similar. This was attributed to a larger grain size and reduced dopant segregation to grain boundaries. In applications where high temperature annealing must be avoided, deposition in the amorphous form is clearly preferred.

CW laser annealing of in-situ phosphorus doped amorphous and polycrystalline silicon deposited on insulator was then examined for the first time. It was found that resistivities equivalent to bulk single crystal silicon could be obtained and that the best uniformity occurred just below the threshold of complete melting. To the author's knowledge the correlation between uniformity and melting threshold has not been noted previously. It was also found that once

crystallized, the resistivity of amorphous-deposited films was much less sensitive to laser power than polycrystalline-deposited films. In integrated circuits where laser annealed polysilicon is used for resistive loads this reduced sensitivity is clearly an important consideration.

Finally, a number of techniques were examined for producing seeded epitaxial growth. Both cw laser-induced liquid phase epitaxy and furnace-induced solid phase epitaxy were considered. Both of these techniques were found to be limited by a maximum lateral seeding distance, as has been noted previously by others. A novel technique, cw laser-induced solid phase epitaxy, was then examined for the first time. While a theoretical analysis seemed to support the viability of the process, certain practical considerations, in particular, temperature gradient-induced stress, seemed to render the process unworkable. Thus the first two processes mentioned above appear to be the most viable. The problem of the maximum lateral seeding distance will likely have to be addressed by using numerous closely-spaced seeding trenches.

10.2 Further Work

The results of the research reported in this thesis can be used as a starting point for further work in a number of areas. Some of these are now described.

First, STEM techniques could be used to confirm the presence or

absence of dopant segregation to grain boundaries in as-deposited phosphorus-doped LPCVD polysilicon. Such studies would help to clarify the role of film structure in dopant incorporation.

It would also be worthwhile to study the effect of rapid thermal annealing on in-situ phosphorus doped LPCVD amorphous and polycrystalline silicon. Judging from the results of the present work it seems likely that resistivities approaching those of bulk single crystal silicon could be obtained. However the uniformity should be much better than with cw laser annealing since RTA is not spatially localized.

The use of in-situ phosphorus doped LPCVD polysilicon as a diffusion source would be worthy of future study. A particularly interesting application of this process would be in shallow diffused silicon solar cells. Low pressure chemical vapor deposition onto p-type silicon substrates followed by RTA-induced diffusion would provide relatively high throughput. Moreover, the polysilicon layer would be expected to yield low sheet resistance and to getter diffusion-induced point defects. It is also relatively easy to make low resistivity aluminum contacts to heavily doped polysilicon without anisotropic interdiffusion phenomenon at the metal-semiconductor interface [148].

A good deal of work also needs to be done on the use of in-situ phosphorus doped polysilicon in polysilicon emitter transistors. While some preliminary studies have been done with encouraging results [13], substantially more work needs to be done to fully

understand the relation between bulk and interface properties and device performance.

Finally, some further work can be done on solid phase lateral epitaxy and random crystallization. It would be particularly interesting to examine in a quantitative manner the relation between random crystallization time and mechanical stress. RTA techniques would clearly be useful in these studies in order to cover a broader range of temperatures than examined here.

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Appendix A

Listing of Fortran Program for Solving the Heat Flow Equation

```

C
C THIS PROGRAM SOLVES THE NONLINEAR HEAT FLOW EQUATION FOR A SINGLE
C OR DOUBLE LAYER STRUCTURE ANNEALED BY A SCANNING ELLIPTICAL LASER
C BEAM. THE PROGRAM USES THE BACKWARD EULER IMPLICIT METHOD WITH
C NEWTON ITERATION. ADDING MORE LAYERS REQUIRES REPETITION OF THE
C BOUNDARY EQUATIONS FOR EACH NEW LAYER. THE PROGRAM USES THE TWO
C EQUATION SOLUTION OF THE HEAT FLOW PROBLEM. THE THREE EQUATION
C SOLUTION REQUIRES THE FOLLOWING ALGORITHM CHANGE: CALCULATE Lx
C ASSUMING Ly=Lx/C, THEN CALCULATE Ly AND UPDATE C.
C
C
C TEMP. PROFILE STORED ON FILE UNIT # 103
C GRID STORED ON FILE UNIT # 137
C SURFACE TEMP VS TIME DISPLAYED ON TERMINAL
C *****
C
C LIST OF IMPORTANT VARIABLES
C
C
C NP: NUMBER OF GRID POINTS (90)
C NBO: INDEX OF BOUNDARY POINT (NBO=500 IF NO BOUNDARY)
C X,DX: GRID POINTS AND SPACINGS
C AR: 0 OR 1 TO INDICATE PRESENCE OR ABSENCE OF AR COAT
C T,TE: TEMPERATURE AND TEMPERATURE AT LATER TIME
C LTHD: X COMPONENT OF LATERAL HEAT DIFFUSION
C HENGT,HENGTE: HEAT ENERGY AND HEAT ENERGY AT LATER TIME
C RHS: RIGHT HAND SIDE OF SYSTEM OF DIFFERENCE EQUATIONS
C DFTE,DFTEM,DFTEP: MATRIX ELEMENTS
C TM,DM,HF: MELTING TEMP, MELT DEPTH, LATENT HEAT OF FUSION
C RT,RTE,RTEO: REFLECTIVITY
C ABSRT,ABSO: ENERGY ABSORPTION
C HCAP: HEAT CAPACITY
C HCON,DHCON: HEAT CONDUCTIVITY AND ITS DERIVATIVE
C HCC,DHCC: HEAT CONDUCTIVITY AND ITS DERIVATIVE FOR BOTTOM MATERIAL
C AT BOUNDARY (HCON(NBO) AND DHCON(NBO) STORE VALUES
C APPROPRIATE TO THE TOP MATERIAL)
C TIME,DTIME: TIME AND TIME STEP
C W,BETA: MINIMUM 1/e LENGTH AND ECCENTRICITY OF LASER BEAM
C Ro,VC: MINIMUM 1/e LENGTH ASSOCIATED WITH TEMPERATURE DISTRIBUTION
C VELOC: SCAN VELOCITY
C
C

```



```

WRITE(6,*)'(500 IMPLIES SINGLE LAYER SILICON WAFER)'
READ(5,'(I3)') NBO
IF(NBO.EQ.500)XBAC=0.0D0
IF(NBO.LT.500)XBAC=10000.0D0*X(NBO)
WRITE(6,'(I1,'BOUNDARY DEPTH (MICRONS): ',F7.3)')XBAC
XBAC=XBAC/10000.0D0
ISOS=3
IF(XBAC.EQ.0.0D0)GO TO 1205
WRITE(6,*)'SUBSTRATE, 1=SAPPHIRE, 2=SILICA'
READ(5,'(I1)')ISOS
1205 CONTINUE
WRITE(6,*) 'MAX TIME INTERVAL (NORMALLY USE 1 MICRO SEC BUT CAN'
WRITE(6,*) 'INCREASE FOR SLOW SCAN SPEEDS) ?'
READ(5,'(E20.10)') TGI
TGI=TGI/1000000.0D0
DO 33 N=2,NP-1
33   DDN(N)=2.0D0/(DN(N)+DN(N-1))
C
C ESTABLISH CONSTANTS AND STARTING VALUES
C
TM=1690.0D0
HF=3280.0D0
DMRL=2.5D-6
TJ=1.0D0
TD=8.0D0
DMP=0.0D0
DDM=0.0D0
TE(NP)=T(NP)
TBL=T(NP)
UD(2)=0.0D0
UD(3)=0.0D0
VD(2)=0.0D0
VD(3)=0.0D0
MLIM=0
MDISP=2
ITLIM=20
NUMIT=10
RM=-1.0D0
TIME=0.0D0
TIMD=5.D-13
DTIME=3.D-9
DTEMP=10.0D0
TIME0=0.0D0
DRT=1.D-50
DRPDT=0.0D0
DRPDTE=4.29D-5
NUMTL=15
DM=0.0D0
DO 1688 N=2,NP
1688 T(N)=T(NP)
TE(N)=T(NP)
CALL ENGCON

```

```

DO 34 N=2,NP
HENG(T(N)=HENGTE(N)
HLTHD(N)=0.DO
LTHD(N)=0.DO
HDIFT(N)=0.DO
ABSRT(N)=0.DO
RHSN(N)=0.DO
34 CONTINUE
T27=T(2)
RT=REFL()

C
C      COMPUTATION STARTS
C

M=0
40 M=M+1
IF(M.LE.MLIM) GOTO 41
MDISP=M
WRITE(6,*) 'MAX NUM OF TIME STEPS /MLIM/?'
WRITE(6,*) '1-6 WILL STORE PRESENT T PROFILE, 0 STOPS PROGRAM'
READ(5, '(I5)') MLIM
IF(MLIM.EQ.0) GOTO 107
41 CONTINUE
C
UD(1)=UD(2)
UD(2)=UD(3)
UD(3)=1.D6*TIME
VD(1)=VD(2)
VD(2)=VD(3)
C
C INSERT VD(3) = VARIABLE WHOSE MAXIMUM IS SOUGHT. PROGRAM WILL FIT
C QUADRATIC FUNCTION TO VARIABLE VS TIME & PRINT MAXIMUM
C
VD(3)=TE(2)
IF((VD(2).GT.VD(1)).AND.(VD(2).GT.VD(3)).AND.(UD(3).GT.IMP8))
$CALL FMAX
C
C DISPLAY RESULTS VS TIME DURING COMPUTATION
C
IF(M.NE.MDISP) GOTO 43
MDISP=M+10
VC=0
IF(M.GT.4) VC=20000.DO*DSQRT(-1.DO*DT(2)/LTHD(2))
WRITE(6, '(1X,I5,1X, TIME: ', F8.3, 1X, 'TE: ', F9.3, 1X, 'DM: ',
$F8.4, 1X, 'RTE: ', F6.3, 1X, 'POWER: ', F7.3, 1X, 'Ro: ', E10.3)')
$M-1, 1.E6*TIME, TE(2), 1.E4*DM, RTE, ABSO*AREA, VC
C
C ADJUST TIME STEP IN INVERSE PROPORTION TO RATE OF CHANGE OF T OR DM
C
43 TEINC=10.DO
IF(T(2).GT.TM-TD-2.DO*TJ) TEINC=2.D-1
IF(T(2).GT.TM) TEINC=5.D-3
IF(DM.GT.DMRL) TEINC=0.5DO

```

```

      FINC=DMINI(DMAX1(0.5DO,DBLE(ITLIM)/NUMIT),2.DO)
      FINC=DMINI(TEINC/DTEMP,FINC)
      FINC=DMINI(FINC,2.D-3/DMAX1(1.D-50,DABS(DRT)))
      FINC=DMINI(FINC,3.D-7/DMAX1(DDM,1.D-7))
      DTIME=DMINI(DTIME*FINC,TG1)
      DTIME=DMAX1(DTIME,TIMD)
C
C SOLVE HEAT FLOW EQUATION FOR Tz
C
      DO 50 N=2,NP-1
      DHENG(N)=(DDX(N)*HDIFT(N)+(1.DO-RT)*ABSO*ABSRT(N)+
$HCON(N)*LTHD(N)*DB2)/HCAP(N)
50    CONTINUE
44    DO 46 N=2,NP-1
46    TE(N)=DTIME*DHENG(N)+T(N)
C-----
C
C BOUNDARY EQUATION
C
      IF(ISOS.NE.3) TE(NBO)=(HCC*TE(NBO+1)/DX(NBO)+HCON(NBO)*TE(NBO-1)
$/DX(NBO-1))/(HCON(NBO)/DX(NBO-1)+HCC/DX(NBO))
C-----
      RTE=DRPDT*DTIME+RT
C
      IF((DABS(RTE-RT).GT.2.D-3).AND.(DTIME.GT.TIMD))DTIME=DTIME/1.2DO
      IF((DABS(RTE-RT).GT.2.D-3).AND.(DTIME.GT.TIMD))GO TO 44
      IF((DABS(RTE-RT).GT.2.D-3).AND.(DTIME.LE.TIMD))WRITE(6,*)
$*** NOT CONVERGING**
C
C ITERATION STARTS
C
      IF(DTIME.GT.1.D-12) GOTO 54
      DM=DMELT()
      T27=TE(2)
      RTE=REFL()
      GOTO 200
54    NUMIT=0
      T37=TIME+DTIME
      ABSO=POWER()/AREA
      DTEM=1.D4
      IFLAGR=0
55    NUMIT=NUMIT+1
      IFLAGM=0
      IF((NUMIT.GT.ITLIM+15).AND.(DTIME.GT.TIMD))DTIME=DTIME/2.DO
      IF((NUMIT.GT.ITLIM+15).AND.(DTIME.GT.TIMD))GO TO 44
      IF((NUMIT.GT.ITLIM+15).AND.(DTIME.LE.TIMD))WRITE(6,*)'NOT CNVG'
C
C SET UP ARRAY FOR SOLEQN
C
      IF((DTEM.LT.5.D-3).AND.(NUMIT.GT.2)) IFLAGM=1
56    CALL ENGCON
C

```

C CALL ABSR IF NECESSARY

C

IZABSR=2
IF((DTEM.GT.5.D-3).AND.(DM.LT.1.5D0*DMRL))IZABSR=1
IF(IZABSR.EQ.1) CALL ABSR

C

AVC2=0.5D0*(HCON(2)+HCON(3))
DT2=(TE(2)-TE(3))/DX(2)
DO 70 N=2,NP-1
AVC1=AVC2
AVC2=0.5D0*(HCON(N)+HCON(N+1))
DT1=DT2
DT2=(TE(N+1)-TE(N))/DX(N)
HDIFT(N)=AVC2*DT2-AVC1*DT1
RHS(N)=HENGTE(N)-HENGTE(N)+DTEM*(DDX(N)*HDIFT(N)+
\$(1.DO-RTE)*ABS0*ABSRT(N)+HCON(N)*LTHD(N)*DB2)
IF(IFLAGM.EQ.1) GOTO 70
DFTEM(N)=DDX(N)*DTEM*(AVC1/DX(N-1)-0.5D0*DHCON(N-1)*DT1)
DFTEP(N)=DDX(N)*DTEM*(AVC2/DX(N)+0.5D0*DHCON(N+1)*DT2)
DFTE(N)=HCAP(N)+DTEM*(DDX(N)*
\$(AVC1/DX(N-1)+AVC2/DX(N)+0.5D0*DHCON(N)*(DT1-DT2))
\$-DHCON(N)*LTHD(N)*DB2)
70 CONTINUE

C

C

C

C

C

BOUNDARY EQUATIONS

IF(ISOS.EQ.3) GO TO 444
AVC1=0.5D0*(HCON(NBO-1)+HCON(NBO))
AVC2=0.5D0*(HCON(NBO+1)+HCC)
DT1=(TE(NBO)-TE(NBO-1))/DX(NBO-1)
DT2=(TE(NBO+1)-TE(NBO))/DX(NBO)
DFTEP(NBO)=DDX(NBO)*DTEM*(AVC2/DX(NBO)+0.5D0*DHCON(NBO+1)*DT2)
DFTE(NBO)=DTEM*DDX(NBO)*(AVC1/DX(NBO-1)+AVC2/DX(NBO)+0.5D0*
\$DHCON(NBO)*(TE(NBO)-TE(NBO-1))/DX(NBO-1)-0.5D0*DHCC*(TE(NBO+1)-
\$TE(NBO))/DX(NBO))
RHS(NBO)=DTEM*DDX(NBO)*(AVC2*DT2-AVC1*DT1)
AVC2=0.5D0*(HCON(NBO+1)+HCON(NBO+2))
AVC1=0.5D0*(HCC+HCON(NBO+1))
DT2=(TE(NBO+2)-TE(NBO+1))/DX(NBO+1)
DT1=(TE(NBO+1)-TE(NBO))/DX(NBO)
HDIFT(NBO+1)=AVC2*DT2-AVC1*DT1
RHS(NBO+1)=HENGTE(NBO+1)-HENGTE(NBO+1)+DTEM*(DDX(NBO+1)*
\$HDIFT(NBO+1)+(1.DO-RTE)*ABS0*ABSRT(NBO+1)+HCON(NBO+1)*
\$LTHD(NBO+1))
DFTEM(NBO+1)=DDX(NBO+1)*DTEM*(AVC1/DX(NBO)-0.5D0*DHCC*DT1)
DFTE(NBO+1)=HCAP(NBO+1)+DTEM*(DDX(NBO+1)*(AVC1/DX(NBO)+AVC2/
\$DX(NBO+1)+0.5D0*DHCON(NBO+1)*(DT1-DT2))-DHCON(NBO+1)*LTHD(NBO+1))
444 CONTINUE

C

IF(IFLAGM.NE.1) DFTEP(2)=DFTEP(2)+DFTEM(2)

C


```

C      CHECKS ERROR
C
      DRHS=0.00
      DO 71 N=2, NP-1
      IF(DABS(RHS(N)).GT.DRHS) DRHS=DABS(RHS(N))
71    IF(DABS(RHS(N)).GT.DRHS) NCR=N
C
C      SOLVES THE EQUATION SYSTEM (RESULT IS IN RHS)
C
      CALL SOLEQN(IFLAGM)
C
      DTEM=0.00
      DO 90 N=2, NP-1
      IF(DABS(RHS(N)).GT.DTEM) DTEM=DABS(RHS(N))
      IF(DABS(RHS(N)).GT.DTEM) NCT=N
90    TE(N)=TE(N)+RHS(N)
C
      RTEP=RTE
      DM=DMELT()
      T27=TE(2)
      RTE=REFL()
      ERTE=DABS(RTE-RTEP)
      IF((DTEM.LT.5.D-8).AND.(ERTE.LT.DMAX1(1.D-3*DABS(RTE-RT),1.D-8)))
$      GOTO 100
      IF((TE(2).LT.TM-1.DO).OR.(DM.GT.1.5DO*DMRL)) GOTO 55
      IF(DMAX1(DABS(RTE-RTET),DTEM).LT.DMAX1(5.D-2*ERTE,1.D-5))
$      GOTO 95
      RTET=RTE
      RTE=RTEP
      GOTO 55
95    IF((IFLAGR.EQ.1).AND.(RTEP.NE.RTEP0)) RM=(RTE-RTE0)/(RTEP-RTEP0)
      IF((IFLAGR.EQ.1).AND.(RTEP.EQ.RTEP0)) RM=-0.5DO
      RTE0=RTE
      RTEP0=RTEP
      RTET=RTE
      RTE=(RTE-RM*RTEP)/(1.DO-RM)
      IFLAGR=1
      GOTO 55
C
C      ITERATION COMPLETED
C
C      SOLVE LATERAL DIFFUSION EQUATION FOR Lx
C
100    DO 119 N=NP,2,-1
119    IF(TE(N)-TBL.LT.1.DO) NL=N
      NP=NL
      IF(NP.LT.4) NP=4
      DRPDTE=(RTE-RT)/(TE(2)-T(2))
      DO 120 N=2, NP-1
      DT(N)=TE(N)-TBL
      IF(TE(N).GT.TM) DT(N)=DMAX1(TE(N)-TM,1.DO)
120    CONTINUE

```

```

DO 123 N=2,NP-1
123  LTHD(N)=(HLTHD(N)+DTIME*RHSN(N))/HCAP(N)
C-----
C
C  BOUNDARY EQUATION
C
      IF (ISOS.NE.3) LTHD(NBO)=(HCC*LTHD(NBO+1)/DX(NBO)+HCON(NBO)*LTHD
$ (NBO-1)/DX(NBO-1))/(HCON(NBO)/DX(NBO-1)+HCC/DX(NBO))
C-----
C
      NUMT=0
      IFLAGM=0
      DLTHD=1.0D10
130  NUMT=NUMT+1
131  IF(NUMT.GT.NUMTL) WRITE(6,*)NUMTL, ' ITERATIONS: NOT CONVERGING'
      IF(NUMT.GT.NUMTL) GO TO 107
C
      IF(DLTHD.LT.5.D-2*DABS(LTHD(2))) IFLAGM=1
      AVC2=0.5D0*(HCON(2)+HCON(3))/DX(2)
      DT2=(LTHD(2)-LTHD(3))
      DO 140 N=2,NP-1
      AVC1=AVC2
      AVC2=0.5D0*(HCON(N)+HCON(N+1))/DX(N)
      DT1=DT2
      DT2=(LTHD(N+1)-LTHD(N))
      LDIF=(AVC2*DT2-AVC1*DT1)*DDX(N)
      RHSN(N)=LDIF+HCON(N)/DT(N)*(1.5D0+0.5D0/BETA2)*LTHD(N)**2
$      -((1.D0-RTE)*FPW2+DRPDTE*LTHD(N))*ABS0*ABSRT(N)
      RHS(N)=HLTHD(N)-LTHD(N)*HCAP(N)+DTIME*RHSN(N)
C
      IF(IFLAGM.EQ.1) GOTO 140
      DFTEM(N)=DDX(N)*DTIME*AVC1 /
      DFTEP(N)=DDX(N)*DTIME*AVC2
      DFTE(N)=HCAP(N)+DFTEM(N)+DFTEP(N)+
$ DTIME*(-1.D0*HCON(N)/DT(N)*LTHD(N)*(3.D0+1.D0/BETA2)+
$ DRPDTE*ABS0*ABSRT(N))
140  CONTINUE
C-----
C
C  BOUNDARY EQUATIONS
C
      IF(ISOS.EQ.3) GO TO 333
      IF(NBO.GT.NP-2) GO TO 333
      AVC2=0.5D0*(HCON(NBO+1)+HCON(NBO+2))/DX(NBO+1)
      AVC1=0.5D0*(HCC+HCON(NBO+1))/DX(NBO)
      RCAR=(1.D0+DB2)*HCON(NBO+1)/DT(NBO+1)
      DT2=LTHD(NBO+2)-LTHD(NBO+1)
      DT1=LTHD(NBO+1)-LTHD(NBO)
      LDIF=(AVC2*DT2-AVC1*DT1)*DDX(NBO+1)
      RHSN(NBO+1)=LDIF+RCAR*LTHD(NBO+1)**2
      RHSN(NBO+1)=RHSN(NBO+1)-((1.D0-RTE)*FPW2+DRPDTE*LTHD(NBO+1))
$ *ABS0*ABSRT(NBO+1)

```

```

      RHS(NBO+1) = HLTHD(NBO+1) - LTHD(NBO+1) * HCAP(NBO+1) + DTIME *
$RHSN(NBO+1)
      DFTEP(NBO+1) = CDX(NBO+1) * DTIME * AVC2
      DFTEM(NBO+1) = DDX(NBO+1) * DTIME * AVC1
      DFTE(NBO+1) = HCAP(NBO+1) + DFTEM(NBO+1) + DFTEP(NBO+1) + DTIME *
$(-1.00 * HCON(NBO+1) / DT(NBO+1) * LTHD(NBO+1) * (3.00 + 1.00 / BETA2) +
$DRPDTE * ABSO * ABSRT(NBO+1))
      DFTEM(NBO) = DEPM
      AVC2 = 0.50 * (HCC + HCON(NBO+1)) / DX(NBO)
      DFTEP(NBO) = DDX(NBO) * DTIME * AVC2
      DFTE(NBO) = DFTEM(NBO) + DFTEP(NBO)
      RHS(NBO) = DFTEP(NBO) * (LTHD(NBO+1) - LTHD(NBO)) - DFTEM(NBO)
$*(LTHD(NBO) - LTHD(NBO-1))
333  CONTINUE
C-----
      IF(IFLAGM.NE.1) DFTEP(2) = DFTEP(2) + DFTEM(2)
C
C      SOLVES THE EQUATION SYSTEM FOR D(LTE) (RESULT IN RHS)
C
      CALL SOLEQN(IFLAGM)
C
      DLTHD = 0.00
      DO 160 N=2, NP-1
      LTHD(N) = LTHD(N) + RHS(N)
      IF(DABS(RHS(N)).GT.DLTHD) DLTHD = DABS(RHS(N))
160  IF(DABS(RHS(N)).EQ.DLTHD) NR = N
      IF(DLTHD.GT.1.D-8 * DABS(LTHD(2))) GOTO 130
      DO 170 N=2, NP-1
170  HLTHD(N) = LTHD(N) * HCAP(N)
      NP = 90
C
C  ITERATION COMPLETED FOR LTE
C
C  SOME BOOKKEEPING
C
200  TIME = TIME + DTIME
      DO 205 N=2, NP-1
205  HENGTE(N) = HENGTE(N)
      DDM = DABS(DM - DMP)
      DRT = RTE - RT
      DTEMP = DABS(TE(2) - T(2))
      DRPDT = DRT / DTIME
      DMP = DM
      RT = RTE
      DO 45 N=2, NP-1
45  T(N) = TE(N)
C
C  STORE RESULT
C
      IF(MLIM.GT.6) GOTO 524
      DO 599 N=2, NP
      TEMPP(N, MLIM) = TE(N)

```

```

599 CONTINUE
524 DDMO=DABS(DM-DMO)
    DTEO=DABS(TE(2)-TEO)
    DMS=3.D-7
    IF(DM.GT.1.2*DMRL) DMS=5.D-6
    IF((DDMO.LT.DMS).AND.(DTEO.LT.5.D1).AND.(TIME.LT.TIMEO)) GOTO 40
    TEO=TE(2)
    DMO=DM
    TIMEO=TIME+5.D-6
    T37=TIME
    PW=POWER()
    DIST=(VELOC1*TIME-W)*1.E4
527 FORMAT(1X,F7.3,F7.1,F7.4,2F6.2,F7.1)
    GOTO 40
107 CONTINUE
C
C     SAVES DATA
C
    DO 600 N=2,NP
600 WRITE(103,601) 1.E4*X(N),(TEMPP(N,L),L=1,6)
601 FORMAT(1X,7(1X,E14.7))
C
1210 CONTINUE
    CLOSE(UNIT=103)
    CLOSE(UNIT=137)
    END
C
C
C     SUBROUTINE ENGCON
C
C ENGCON CALLS THE APPROPRIATE SUBROUTINE (DEPENDING ON
C DEPTH INTO SAMPLE) TO EVALUATE MATERIAL PARAMETERS
C
%INCLUDE 'EECLARE.FTN'
C-----
C
C     SAVE BOUNDARY VALUES
C
    IF(ISOS.EQ.3)GO TO 5
    N=NBO
    IF(ISOS.EQ.1) CALL SAPCON
    IF(ISOS.EQ.2) CALL SIOCON
    HCC=HCON(NBO)
    DHCC=DHCON(NBO)
5    CONTINUE
C-----
    DO 10 N=2,NP
    IF(ISOS.EQ.3) CALL CNGCON
    IF(ISOS.EQ.3) GO TO 6
    IF((ISOS.EQ.1).AND.(N.GT.NBO)) CALL SAPCON
    IF((ISOS.EQ.2).AND.(N.GT.NBO)) CALL SIOCON
    IF(N.GT.NBO) GO TO 6

```

3 of/de 3

```

      CALL CNGCON
6      CONTINUE
10     CONTINUE
      HCON(1)=HCON(3)
      DHCON(1)=DHCON(3)
      RETURN
      END

```

C

C

```

      SUBROUTINE ABSR

```

C

C

```

      CALCULATE OPTICAL ABSORPTION

```

C

C

```

      %INCLUDE 'EECLARE.FTN'

```

C

C

1

```

      N=1

```

```

      N=N+1

```

```

      TS=TE(N)

```

```

      ALFA1=ALFA2

```

```

      ALFA2=7.5D3*DEXP(TS/435.D0)

```

```

      ALFX=ALFX+5.D-1*(ALFA1+ALFA2)*DX(N-1)

```

```

      IF(N.EQ.2) ALFX=0.D0

```

```

      IF(ALFX.GT.15.D0) GOTO 10

```

```

      ABSRT(N)=ALFA2*DEXP(-ALFX)

```

```

      GOTO 1

```

10

```

      DO 20 J=N,NP-1

```

20

```

      ABSRT(J)=0.D0

```

```

      RETURN

```

```

      END

```

C

C

```

      SUBROUTINE SOLEQN(LFLAGM)

```

C

C

```

      SOLVE MATRIX EQUATION.

```

C

C

```

      %INCLUDE 'EECLARE.FTN'

```

C

```

      P(2)=DFTE(2)

```

```

      S(2)=RHS(2)

```

C

```

      DO 20 N=3,NP-1

```

```

          IF(LFLAGM.EQ.1) GOTO 21

```

```

      R(N)=DFTEM(N)/P(N-1)

```

```

      P(N)=DFTE(N)-R(N)*DFTEP(N-1)

```

21

```

      S(N)=RHS(N)+R(N)*S(N-1)

```

20

```

      CONTINUE

```

C

```

      RHS(NP-1)=S(NP-1)/P(NP-1)

```

```

      DO 30 N=NP-2,2,-1

```

30

```

      RHS(N)=(S(N)+DFTEP(N)*RHS(N+1))/P(N)

```

C

```

      RETURN

```

END

C
C

DOUBLE PRECISION FUNCTION POWER()

C

C CALCULATE LASER POWER VS TIME

C

INCLUDE 'EECLARE.FTN'

C

IF(VELOC1.EQ.0.D0) GOTO 10

SV=(T37*VELOC1/W-2.5D0)**2

IF(SV.GT.5.D1) GOTO 30

POWER=POWER0/DEXP(SV)

RETURN

10

POWER=POWER0

RETURN

30

POWER=0.D0

RETURN

END

C

C

DOUBLE PRECISION FUNCTION REFL()

C

C CALCULATE REFLECTIVITY

C

INCLUDE 'EECLARE.FTN'

C

RMIN=0.367D0

RMAX=0.28D0

IF(AR.EQ.1) RMIN=0.147D0

IF(AR.EQ.1) RMAX=0.296D0

RETL=RMIN+4.29D-5*DMIN1(T27,TM)

ET=(DMRL/2.D0-DM)/DMRL*6.D0

C

IF(DABS(ET).GT.20.D0) GOTO 5

RETL=RETL+RMAX/(DEXP(ET)+1.D0)

5

IF(ET.LE.-20.D0) RETL=RETL+RMAX

REFL=RETL

RETURN

END

C

C

DOUBLE PRECISION FUNCTION DMELT()

C

C THIS FUNCTION CALCULATES THE POINT WHERE T=MELTING TEMP OF SILICON.

C THIS IS DONE BY FITTING A FOURTH ORDER POLYNOMIAL TO T NEAR THE

C MELTING TEMPERATURE. NOTE THAT THIS POINT LOOSES SIGNIFICANCE WHEN

C IT LIES WITHIN THE INSULATING SUBSTRATE.

C

INCLUDE 'EECLARE.FTN'

C

```

      L=1
48    L=L+1
      IF(TE(L).GT.TM) GO TO 48
      DMEL1=0.D0
      IF(L.EQ.2) GOTO 100
      IF((L.LE.NBO+1).AND.(L.GE.NBO-1)) DMEL1=XBAC
      IF((L.LE.NBO+1).AND.(L.GE.NBO-1)) GO TO 100
      DMEL1=X(L)+DX(L-1)*(TM-TE(L))/(TE(L)-TE(L-1))
      IF(L.EQ.3) GOTO 101
      IF((L.LT.NBO+3).AND.(L.GT.NBO-1)) GO TO 100
C
      DO 10 I=1,3
      TT(I)=TE(L-2+I)-TE(L-2)
10    D(I)=X(L-2+I)-X(L-2)
C
      DO 30 N=1,4
      DO 20 K=1,3
      DO 20 M=1,3
      IF(M.EQ.N) A(K,M)=TT(K)
20    IF(M.NE.N) A(K,M)=D(K)**M
C
30    DET(N)=A(1,1)*(A(2,2)*A(3,3)-A(3,2)*A(2,3))
      $-A(1,2)*(A(2,1)*A(3,3)-A(3,1)*A(2,3))
      $+A(1,3)*(A(2,1)*A(3,2)-A(3,1)*A(2,2))
C
      DO 40 I=1,3
40    V(I)=DET(I)/DET(4)
C
C      NEWTON ITERATION
C
      SQ4=DMEL1-X(L-2)
      DS=0.D0
50    SQ4=SQ4+DS
53    TP9=TE(L-2)+V(1)*SQ4+V(2)*SQ4**2+V(3)*SQ4**3
      IF(DABS(TP9-TM).LT.1.D-07) GO TO 60
      DTE=V(1)+2.D0*V(2)*SQ4+3.D0*V(3)*SQ4**2
      DS=(TM-TP9)/DTE
      GOTO 50
60    DMEL1=X(L-2)+SQ4
      GO TO 100
101   DMEL1=DSQRT((TE(2)-TM)/(TE(2)-TE(3)))*DX(2)
100   DMELT=DMEL1
      RETURN
      END
C
      SUBROUTINE CNGCON
C
C      CALCULATE MATERIAL PROPERTIES FOR SINGLE CRYSTAL SILICON
C
      INCLUDE 'EECLARE.FTN'
      HCAP(N)=2.33D0-139.8D0/(TE(N)-99.D0)
      HENGTE(N)=2.33D0*TE(N)-139.8D0*DLOG(TE(N)-99.D0)+201.92D0

```



```
HCON(N)=299.DO/(TE(N)-99.DO)
DHCON(N)=-1.DO*HCON(N)/(TE(N)-99.DO)
```

```
ET=(TM-TD-TE(N))/TJ
IF(DABS(ET).GT.25.DO) GOTO 5
EET=DEXP(ET)
HENGTE(N)=HENGTE(N)+HF/(EET+1.DO)
HCAP(N)=HCAP(N)+HF/TJ*EET/(EET+1.DO)**2
DHCON(N)=(DHCON(N)+(0.64DO-HCON(N))/TJ/(1.DO+EET))*EET/(1.DO+EET)
HCON(N)=HCON(N)+(0.64DO-HCON(N))/(1.DO+EET)
```

```
5 IF(ET.GT.-25.DO) GOTO 10
HCON(N)=0.64DO
DHCON(N)=0.0DO
HENGTE(N)=HENGTE(N)+HF
10 RETURN
END
```

```
C
SUBROUTINE FMAX
```

```
C
CALCULATES & PRINTS MAXIMUM
```

```
C
ZINCLUDE 'EECLARE.FTN'
```

```
DOUBLE PRECISION UTMX,VTMX,VM1,VM2,DVM1,DVM2
VM1=(VD(2)-VD(1))/(UD(2)-UD(1))
VM2=(VD(3)-VD(2))/(UD(3)-UD(2))
DVM1=DABS(VM1)
DVM2=DABS(VM2)
UTMX=0.5DO*(DVM2*(UD(1)+UD(2))+DVM1*(UD(2)+UD(3)))/(DVM1+DVM2)
VTMX=VD(2)+(VD(3)-VD(2))/(1.DO+((UD(3)-UTMX)/(UD(2)-UTMX))**2)
WRITE(6,*)'*****'
WRITE(6, '(1X, 'TIME:',F8.3,2X, 'MAX VALUE:',F11.4)')UTMX,VTMX
WRITE(6,*)'*****'
RETURN
END
```

```
C
SUBROUTINE SAPCON
```

```
C
CALCULATE MATERIAL PROPERTIES OF SAPPHIRE
```

```
C
ZINCLUDE 'EECLARE.FTN'
```

```
HCAP(N)=5.5DO-561.DO/(TE(N)-68.DO)
HENGTE(N)=5.5DO*TE(N)-561.DO*DLOG(TE(N)-68.DO)+1660.DO
HCON(N)=TE(N)/17300.DO+138.873DO/TE(N)-0.123191DO
DHCON(N)=5.78034D-5-138.873DO/TE(N)/TE(N)
RETURN
END
```

```
C
SUBROUTINE SIOCON
```

```
C
CALCULATE MATERIAL PROPERTIES OF SILICA
```

```

ZINCLUDE 'EECLARE.FTN'
  HENGTE(N)=2.5D0*TE(N)
  HCAP(N)=2.5D0
  HCON(N)=0.02D0
  DHCON(N)=0.0D0
  RETURN
  END

```

```

C
C PROGRAM EECLARE.FTN
C

```

```

C DECLARE AND DIMENSION VARIABLES AND COMMON BLOCKS
C

```

```

  DOUBLE PRECISION HCC,DHCC,TM,HF,HFAC,TD,TJ,XBAC,DM,DMRL,UD(3),
  $VD(3),DT2,
  INTEGER N,NBO,AR,NP,ISOS
  DOUBLE PRECISION HCON(90),DHCON(90),HCAP(90),HENGTE(90),TE(90),
  $ABSRT(90),X(90),DX(90),VELOC1,POWER0,W,BETA,BETA2,T(90),
  $HENGTE(90),RHS(90),DFTE(90),DFTEM(90),DFTEP(90),P(90),R(90),
  $DHENG(90),HDIFT(90),RT,RTE0,RTE,DRT,DRPDT,TEINC,DT(90),DT1,
  $AVC1,AVC2,RTEP,ERTE,RTET,RTEP0,RM,ABSO,DRPDTE,DLTHD,DDX(90),
  $JLTHD(90),HLTHD(90),RHSN(90),DTEMP,DTIME,TIME,TIME0,FPW2,AREA,
  $LDIF,MAXT,FINC,MAGN,QO,TBL,DTEM,DTE0,TEO,DMS,DMO,DMP,DDM,DDMO,
  SVC,A1,TIMD,T27,TE7
  DOUBLE PRECISION TS,ALFA1,ALFA2,ALFX,S(90),SV,RMIN,RMAX,RETL,
  SET,TT(3),D(3),A(3,3),V(3),DET(4),SQ4,DS,DMEL1,EET,RCAR,TGI
  INTEGER NUMIT,ITLIM,IFLAGR,IFLAGM

```

```

  REAL TEMPP(90,6)

```

```

COMMON HCC,DHCC,TM,HF,TD,TJ,XBAC,DM,DMRL,UD,VD,DT2
COMMON N,NBO,AR,NP,ISOS
COMMON/EQN/ DFTE,DFTEM,DFTEP,RHS,P,R
COMMON/ABSRP/ ABSRT
COMMON/HEATSP/ VELOC1,POWER0,W
COMMON/HPAR/ HENGTE,HCAP,HCON,DHCON
COMMON/MELT/ X,DX
COMMON/TEMPR/ TE
COMMON/TTWO/T27,T37
COMMON/VAR/ TS,ALFA1,ALFA2,ALFX,S,SV,RMIN,RMAX,
$RETL,ET,TT,D,A,V,DET,SQ4,DS,DMEL1,EET

```

END

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FIN