1

MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS
STANDARD REFERENCE MATERIAL 1010a
(ANSI and ISO TEST CHART No. 2)

National Library
of Canada

Bibliothèque nationale
du Canada

Canadian Theses Service

Services des thèses canadiennes

Ottawa, Canada
K1A 0N4

CANADIAN THESES

THÈSES CANADIENNES.

NOTICE

The quality of this microfiche is heavily dependent upon the quality of the original thesis submitted for microfilming. Every effort has been made to ensure the highest quality of reproduction possible.

If pages are missing, contact the university which granted the degree.

Some pages may have indistinct print especially if the original pages were typed with a poor typewriter ribbon or if the university sent us an inferior photocopy.

Previously copyrighted materials (journal articles, published tests, etc.) are not filmed.

Reproduction in full or in part of this film is governed by the Canadian Copyright Act, R.S.C. 1970, c. C-30.

THIS DISSERTATION
HAS BEEN MICROFILMED
EXACTLY AS RECEIVED

AVIS

La qualité de cette microfiche dépend grandement de la qualité de la thèse soumise au microfilmage. Nous avons tout fait pour assurer une qualité supérieure de reproduction.

S'il manque des pages, veuillez communiquer avec l'université qui a conféré le grade.

La qualité d'impression de certaines pages peut laisser à désirer, surtout si les pages originales ont été dactylographiées à l'aide d'un ruban usé ou si l'université nous a fait parvenir une photocopie de qualité inférieure.

Les documents qui font déjà l'objet d'un droit d'auteur (articles de revue, examens publiés, etc.) ne sont pas microfilmés.

La reproduction, même partielle, de ce microfilm est soumise à la Loi canadienne sur le droit d'auteur, SRC 1970, c. C-30.

LA THÈSE A ÉTÉ
MICROFILMÉE TELLE QU'ELLE
NOUS L'AVONS REÇUE

Canada

DESIGN CONSIDERATIONS FOR HIGH-FREQUENCY SWITCHED-CAPACITOR FILTERS

by

David B. Ribner M. A. Sc.

A thesis submitted to the Faculty of Graduate
Studies and Research in partial fulfillment
of the requirements for the degree of

Doctor of Philosophy

Department of Electronics
Faculty of Engineering
Carleton University
Ottawa, Canada
September 1985

Permission has been granted to the National Library of Canada to microfilm this thesis and to lend or sell copies of the film.

The author (copyright owner) has reserved other publication rights, and neither the thesis nor extensive extracts from it may be printed or otherwise reproduced without his/her written permission.

L'autorisation a été accordée à la Bibliothèque nationale du Canada de microfilmer cette thèse et de prêter ou de vendre des exemplaires du film.

L'auteur (titulaire du droit d'auteur) se réserve les autres droits de publication; ni la thèse ni de longs extraits de celle-ci ne doivent être imprimés ou autrement reproduits sans son autorisation écrite.

ISBN 0-315-29866-9

The undersigned recommend to the Faculty of Graduate Studies and
Research the acceptance of the thesis:

"Design Considerations for High-Frequency Switched-
Capacitor Filters"

submitted by David B. Ribner in partial fulfillment of the
requirements for the degree of Doctor of Philosophy.

M.A. Copeland

Prof. M.A. Copeland
Thesis Supervisor

A.R. Boothroyd

Prof. A.R. Boothroyd
Chairman
Department of Electronics

Adel S. Sedra

Dr. A.S. Sedra
University of Toronto
External Examiner

October 25, 1985

ABSTRACT

The objective of this thesis has been to extend the application of switched-capacitor (SC) filtering to frequencies several orders of magnitude above voiceband. Achievement of this goal has required work in several separate, but related fronts. First, a new computer-aided analysis tool for the analysis of nonideal switched-capacitor filters is presented. This computer program is highly efficient, and facilitates detailed simulation of nonideal, notably finite bandwidth, effects in arbitrary switched-capacitor networks. A novel transient analysis technique is used, in a preprocessing phase, to enable subsequent frequency domain analysis; switch resistance effects, and arbitrary degrees of op amp dynamics can be simulated.

On the next front, several op amps suitable for application to high-frequency SC filtering are presented. A frequency compensation approach for wideband op amps is described; followed by details of several wideband op amps that have been implemented in a 1.25 micron CMOS technology. Differential and single-ended versions of these op amps operate with bandwidths in excess of 90 MHz. In addition, internally compensated op amps and buffers suitable for driving resistive loads, and off-chip, are presented. These op amps have also been implemented and have improved AC power-supply rejection ratios.

In the third related area, work is detailed on biquad alternatives for high-frequency SC filters. Here, single-ended and differential SC biquads are compared extensively, using both analysis, and the new nonideal SC network simulator. A new differencing-input filter is shown to have a significant performance advantage

over other options. In addition, a time invariant loading compensation methodology is presented that can offer further benefits.

Finally, results of a high-frequency SC filter test chip implemented in a 1.25 micron CMOS technology are presented. The results validate the biquad comparisons and demonstrate the superior performance of the differencing-input SC circuit. Accurate filtering of 1 MHz signals is demonstrated.

ACKNOWLEDGEMENTS

I would like to express my gratitude to my thesis supervisor, Prof. M. A. Copeland, for his continuing support and encouragement, during the course of this Ph. D. program. I am indebted to him, for suggesting the research topic, and for creating the opportunities for me to conduct research using industrial liaison. I also owe thanks to many people at several institutions who have helped me along the way.

At General Electric Corporate Research and Development, I owe a great deal to Dr. R. D. Baertsch, Dr. G. Ludwig, and to Mr. R. T. Jerdonek, for instituting a workable research arrangement for me. Also at G. E. I owe a great debt of thanks to Dr. M. Milkovic for generously contributing and assisting me with circuits and testing. I also wish to thank Kathy Panton for her tremendous help in testing; thanks are also due to Jim Richotte, and Ken Rohling for their excellent layout efforts. I am also grateful for the opportunity to work with and learn from Dr. T. L. Vogelsong, Mr. M. J. Demler, Mr. S. Chu, and Mr. M. Wu.

At Mitel Corp. I am indebted to Mr. M. S. Foster and Mr. L. P. Sellars, for creating an opportunity for me to conduct research at that company. I also am deeply indebted to Mr. C. Kurowski, for implementing specific versions of circuits for me, and for providing me with test results of other circuits. While at Mitel, I benefited greatly from the opportunity to work with Mr. F. Dea, Mr. S. Skierskan, Mr. R. P. Colbeck, and Mr. K. Dwevedi.

I am deeply grateful to my management at Bell Laboratories, in particular, my supervisor, Dr. M. R. Dwarkanath, my Dept. head, Dr. M. Maul, and my previous Dept. head, Dr. J. Wuorinen, for their support and encouragement, during the final phases of this work. I would also like to thank Mrs. Elvre Hung for her excellent text processing work on this thesis.

Last but by no means least, I wish to thank my wife Lesley for her endless patience during the course of my work. I realize that this mere acknowledgement can come no where near to repaying her contribution, but, I hope it will at least be a start.

The financial support of the Natural Sciences and Engineering Research Council of Canada, the General Electric Co., and Mitel Corp. is gratefully acknowledged.

TABLE OF CONTENTS

ABSTRACT	i
ACKNOWLEDGEMENTS	iii
TABLE OF CONTENTS	v
LIST OF FIGURES	viii
LIST OF SYMBOLS AND ABBREVIATIONS	xiv
CHAPTER 1. INTRODUCTION.....	1
1.1 Thesis Motivation.....	1
1.2 Background	2
1.3 The Switched-Capacitor Principle	3
1.4 High-Frequency Challenges	6
1.5 Thesis Overview	9
CHAPTER 2. HIGH-FREQUENCY CONSIDERATIONS.....	12
2.1 Introduction	12
2.2 Geometry Scaling of SC Circuits	15
2.3 Noise Behavior of Sampled-Analog Circuits.....	17
2.3.1 Thermal Switch Noise	19
2.3.2 1/f Noise in MOS Operational Amplifiers.....	24
2.3.3 Operational Amplifier Broadband Noise	26
2.3.4 Power-Supply Rejection	28
2.4 Bandwidth and Power Dissipation Considerations	37
2.5 Conclusions	42
CHAPTER 3. COMPUTER AIDED ANALYSIS OF NONIDEAL SWITCHED- CAPACITOR NETWORKS FOR HIGH-FREQUENCY APPLICATIONS.....	44
3.1 Introduction	44
3.2 Formulation of Equations.....	47
3.3 Frequency Response of the Discrete Time System.....	53
3.4 Solution of the Discrete System	54
3.5 Determination of the B_k and g_k Coefficients.....	55
3.6 A Computer Program for Analyzing Nonideal SC Networks.....	56
3.7 Numerical Efficiency of the Analysis Technique	57
3.8 High-Frequency Application Example.....	61
3.9 Conclusions	63
CHAPTER 4. OP AMP DESIGN FOR-HIGH FREQUENCY CIRCUITS	68
4.1 Introduction	68
4.2 A Frequency Compensation Approach for Wide-Band Op Amps.....	69
4.3 Transconductance Amplifiers.....	74
4.4 Overview of the High Frequency Op Amp Design Approach.....	77
4.5 Differential Op amps and Common-Mode Feedback	81
4.6 Current Steering Op Amps	86
4.7 Current Mirror Op Amps	106
4.8 A Comparison of Current Steering and Current Mirror Op Amps.....	128

4.9	Conclusions	130
CHAPTER 5. INTERNALLY COMPENSATED OP AMPS AND BUFFERS 132		
5.1	Introduction	132
5.2	Design Techniques for Cascoded CMOS Op Amps with Improved PSRR and Common-Mode Input Range	133
5.2.1	Introduction.....	133
5.2.2	Internally Compensated Noncascoded Op Amps.....	136
5.2.3	Internally Compensated Cascoded Op Amps	139
5.2.4	Results	152
5.3	Low Impedance High Swing CMOS Buffers.....	155
5.3.1	Introduction.....	155
5.3.2	Wide voltage swing output stages	157
5.3.3	The buffer circuit	163
5.4	Conclusions	168
CHAPTER 6. BIQUAD ALTERNATIVES FOR HIGH-FREQUENCY SWITCHED-CAPACITOR FILTERS.....		
6.1	Introduction	169
6.2	Transient Response of SC Integrators.....	170
6.3	Performance Limitations of SC Filters Using Finite Bandwidth Op Amps	176
6.4	Biquad Alternatives for Single-Ended and Differential High Frequency SC Filters	182
6.5	Finite Op Amp Bandwidth Effects on the Differential SC Biquad Alternatives.....	192
6.6	Methodology for the Compensation of High-Frequency SC Filters.....	199
6.7	Conclusions	205
CHAPTER 7. HIGH FREQUENCY SWITCHED-CAPACITOR FILTER TEST RESULTS		
7.1	Introduction	207
7.2	Frequency Response Measurements	208
7.3	Power-Supply Rejection Ratio	218
7.4	Conclusions	222
CHAPTER 8. CONCLUSIONS		
8.1	Summary	224
8.2	Suggestions for Future Work	227
Appendix A. Transient Response of Finite Bandwidth SC Integrators.....		230
Appendix B. Equation Formulation for Finite Bandwidth SC Integrators		234
Appendix C. Analysis of Finite Bandwidth SC Integrators.....		236
Appendix D. Analysis of a Cascode Amplifier		241
Appendix E. Analysis of the Stacked Current Mirror		245

Appendix F. Clock-Feedthrough Cancellation in Single-Ended SC	
Circuits	252
REFERENCES	256

LIST OF FIGURES

Fig. 1.1	Switched capacitor/resistor equivalence. (a) RC lowpass (b) SC lowpass (c) Two phase nonoverlapping clock waveforms.	4
Fig. 1.2	The two basic stray-free switched-capacitor integrators (a) Noninverting (b) Inverting.	7
Fig. 1.3	Switched-capacitor biquad filter.	8
Fig. 2.1	Stray-free switched-capacitor integrator.	13
Fig. 2.2	Effect of constant geometry scaling on analog circuit gain and bandwidth.	18
Fig. 2.3	Thermal noise model for an SC integrator. (a) SC integrator (b) SC integrator with noisy switches (c) Simplified noise model.	21
Fig. 2.4	Voiceband internally-compensated CMOS op amp.	30
Fig. 2.5	Effect of the parasitic capacitances of an op amp input transistors on the power supply rejection of an integrator.	32
Fig. 2.6	Clock feedthrough in an SC integrator. (a) SC integrator (b) Feedthrough of the $\phi 1$ clock as M1 opens (c) Feedthrough of the $\phi 2$ clock as M2 opens.	34
Fig. 2.7	Clock feedthrough effect on a sample and hold capacitor.	35
Fig. 2.8	CMOS inverter as a gain stage.	40
Fig. 3.1	Circuit elements required for simulation of nonideal linear SC networks.	48
Fig. 3.2	Switched-capacitor network with dynamic behavior during each clock phase due to a resistor. (a) Complete network (b) Compact subnetwork during $\phi 1$ (c) Compact subnetwork during $\phi 2$.	49

Fig. 3.3	Companion model representation of a capacitor for the backwards Euler integration algorithm.	58
Fig. 3.4	Model of a first-order transconductance amplifier.	57
Fig. 3.5	Nonideal switched-capacitor bandpass filter.	62
Fig. 3.6	Effect of op amp bandwidth on the SC bandpass filter.	64
Fig. 3.7	Effect of switch resistance on the SC bandpass filter.	65
Fig. 3.8	Combined effect of op amp bandwidth and switch resistance on the SC bandpass filter.	66
Fig. 4.1	Two approaches to high gain CMOS amplifier design. (a) Cascade of two common-source stages (b) Cascode stage.	71
Fig. 4.2	First-order transconductance amplifier.	75
Fig. 4.3	Cascode op amp approaches. (a) Current steering approach (b) Current mirroring approach.	79
Fig. 4.4	Schematic symbol for a differential output op amp.	82
Fig. 4.5	Biasing problem associated with differential signal paths. (a) Single-ended circuit with a well defined bias (b) Differential circuit with an arbitrary bias.	84
Fig. 4.6	Biasing the output of a differential output op amp through the use of a common-mode feedback loop.	85
Fig. 4.7	Differential current-steering op amp.	87
Fig. 4.8	Small-signal model of a current steering op amp.	89
Fig. 4.9	Single-ended current steering op amp with zero-systematic offset.	93
Fig. 4.10	Bias circuit for current steering op amps.	94
Fig. 4.11	Large signal closed loop response of current steering op amp.	96

Fig. 4.12	Open loop response of current steering op amp.	96
Fig. 4.13	Small signal frequency response at 250 μ A for the current steering op amp.	97
Fig. 4.14	Small signal frequency response at 500 μ A for the current steering op amp.	97
Fig. 4.15	Closed loop transient response for a 50 ns pulse for the current steering op amp.	98
Fig. 4.16	Closed loop transient response for a 20 ns pulse for the current steering op amp.	98
Fig. 4.17	Open loop large signal response for the current steering op amp.	99
Fig. 4.18	Fully differential current steering op amp.	102
Fig. 4.19	Single-ended to differential conversion using the differential current steering op amp. (a) Measured output (b) Test circuit.	106
Fig. 4.20	AC coupled current-mirror (a) simplified circuit (b) actual circuit.	108
Fig. 4.21	Op amp test structure.	109
Fig. 4.22	(a) Single-ended op amp and bias circuit (b) differential op amp.	110
Fig. 4.23	Block diagram of the current mirror op amp.	112
Fig. 4.24	Schematic of the current mirror op amp.	114
Fig. 4.25	Current mirrors. (a) Simple mirror (b) Cascoded mirror (c) Stacked mirror.	120
Fig. 4.26	Block diagram of the common-mode bias circuit.	122
Fig. 4.27	Simplified block diagram of the common-mode bias circuit.	123
Fig. 4.28	Differential current-mirror op amp with the common-mode feedback circuit.	125

Fig. 4.29	Single-ended current-mirror op amp.	126
Fig. 5.1	Conventional internally compensated CMOS op amp.	134
Fig. 5.2	Internally compensated cascoded CMOS op amp with high AC PSRR.	134
Fig. 5.3	Internally compensated folded cascode CMOS op amp with high AC PSRR and wide common-mode input range.	136
Fig. 5.4	AC small-signal model for the op amp of Fig. 5.1.	136
Fig. 5.5	AC small-signal PSRR model for the op amp of Fig. 5.1.	138
Fig. 5.6	AC small-signal model for the cascode op amps of Figs. 5.2 and 5.3.	138
Fig. 5.7	Gain peaking of frequency response when Q of parasitic pole pair is too high.	140
Fig. 5.8	Small-signal PSRR model for the cascode op amps of Figs. 5.2 and 5.3.	140
Fig. 5.9	Frequency response of the approximate model (points), and of a complete SPICE circuit simulation (solid lines) for the cascode op amp of Fig. 5.2.	153
Fig. 5.10	Photomicrograph of the cascode op amp of Fig. 5.3.	154
Fig. 5.11	V_{DD} PSRR for the cascode op amp of Fig. 5.3.	156
Fig. 5.12	(a) A complimentary source follower output stage, (b) A complimentary common-source amplifier output stage.	158
Fig. 5.13	Block diagram for a low impedance wide swing output stage.	159
Fig. 5.14	Simple buffer circuit.	161
Fig. 5.15	Improved buffer circuit using folded cascode predrivers.	162
Fig. 6.1	Stray-free inverting switched-capacitor integrator.	172

Fig. 6.2	Signal-flow diagram of the SC integrator during phase 2.	173
Fig. 6.3	Two integrators interconnected on a phase.	184
Fig. 6.4	Differential SC integrators (a) Noninverting (b) Inverting (c) Differencing-input.	186
Fig. 6.5	Biquad A: A single-ended SC filter.	189
Fig. 6.6	Biquad C: A differential SC filter using inverting integrators.	190
Fig. 6.7	Biquad D: A differential SC filter using differencing-input integrators.	191
Fig. 6.8	NISCAP simulation of biquad errors for finite bandwidth, zero output impedance op amps. (a) Resonant frequency error (b) Gain error.	196
Fig. 6.9	NISCAP simulations of biquad errors for second-order transconductance op amps and nonzero switch resistance (a) Resonant frequency error (b) Gain error.	197
Fig. 6.10	A noninverting SC integrator biquad (Biquad B) modified for time invariant op amp bandwidths.	206
Fig. 7.1	Photomicrograph of the high-frequency SC filter test chip.	209
Fig. 7.2	Biquad A: single-ended filter. (a) 5 MHz clock rate (b) 10 MHz clock rate.	211
Fig. 7.3	Biquad C: differential filter using inverting SC integrators. (a) 15 MHz clock rate (b) 5 MHz clock rate.	213
Fig. 7.4	Biquad D: differential filter using differencing-input SC integrators. (a) 10 MHz clock rate (b) 15 MHz clock rate.	214
Fig. 7.5	Biquad D: differential filter using differencing-input SC integrators. Detailed passband at a 10 MHz clock rate.	215
Fig. 7.6	Measured resonant frequency error for the test filter.	216

Fig. 7.7	Measured gain error for the test filters.	217
Fig. 7.8	PSRR of biquad C with a 5 MHz clock rate. (a) V_{DD} PSRR (b) V_{SS} PSRR.	219
Fig. A.1	Stray free inverting switched-capacitor integrator.	231
Fig. D.1	Analysis of a cascode amplifier (a) Cascode circuit (b) Small-signal equivalent circuit for determining output impedance.	242
Fig. E.1	Stacked current mirror.	246
Fig. E.2	Small signal equivalent circuit of the stacked current mirror.	247
Fig. E.3	Normalized parasitic pole frequencies as a function of current gain.	250
Fig. F.1	Single-ended biquad filter with clock-feedthrough cancellation circuitry.	253.
Fig. F.2	Simplified circuit that explains clock-feedthrough cancellation.	254

LIST OF SYMBOLS AND ABBREVIATIONS

$A_o, A(s), A(\omega)$	Amplifier open-loop gain and frequency response
A_{CMd}, A_{CMcm}	Common-mode gain: differential, and common-mode
A_k^T	Transpose of incidence matrix of the capacitor graph on phase k
B_k	Matrix relating initial capacitor branch voltages to final node voltages
B_{eq}	Noise equivalent bandwidth
BQ	Biquad
C_{DS}	MOSFET drain-to-source capacitance
C_{GS}	MOSFET gate-to-source capacitance
C_{GDO}	MOSFET gate-to-drain overlap capacitance
C_G	MOSFET gate capacitance
C_H	Sample and hold capacitance
C_p	Parasitic capacitance
C_o	MOSFET gate capacitance per unit area
C_k	Matrix relating initial to final node voltages for phase k
CCD	Charge-coupled device
CDS	Correlated-double sampling
CMRR	Common-mode rejection ratio

CMOS	Complementary metal oxide semiconductor
CODEC	Coder-Decoder integrated circuit
dB	Decibel
$D_p(\omega)$	Parasitic pole polynomial
E	Preprocessed matrix for frequency response
$E(\omega), E_D(\omega), E_N(\omega)$	Error response of an SC integrator for delayed and nondelayed sampling
f	Frequency
f_T	MOS transistor unity-gain bandwidth
f_{clock}	Clock frequency
g_m, g_{mb}	MOSFET transconductance and substrate transconductance
$g_{m\text{sc}}$	Amplifier short-circuit transconductance
G_m	Amplifier transconductance
g_k	Vector relating initial input voltage to final node voltages for phase k
g_k^p	Preprocessed g_k vector
g_o	MOSFET drain-to-source conductance
G_o, G_{oP}, G_{oN}	Current source conductance
GBW	Gain-bandwidth product
$H(z)$	Z domain right-hand side vector for NISCAP
$H_a(\omega), H_i(\omega)$	SC integrator actual and ideal frequency responses

HFSC	High-frequency switched-capacitor
$i_i(s), i_o(s)$	Current mirror input and output current
I_{DD}	MOSFET power-supply current
I_{DS}	MOSFET drain-to-source current
I_{os}	Amplifier offset current
I_B	Bias current
IC	Integrated circuit
k	Boltzmann's constant
K	MOSFET scaling parameter
K'	MOSFET gain factor Amp/Volt ²
L	Inductance
LDI	Lossless digital integrator
$m(\omega), m_D(\omega), m_N(\omega)$	SC integrator magnitude error response for delayed and nondelayed sampling
MOS	Metal oxide semiconductor
MOSFET	Metal oxide semiconductor field-effect transistor
$M(z)$	Frequency response matrix for NISCAP
MNA	Modified nodal analysis
NISCAP	Nonideal switched-capacitor analysis program
OTA	Operational transconductance amplifier
P_D	Power dissipation

P_f, P_p, P_t	Number of multiplications for frequency preprocessing, and total processing with NISCAP
PSR, PSRR	Power-supply rejection, and rejection ratio
PSD	Power-spectral density
q	Electron charge
Q, Q_{CH}	Charge, and MOSFET channel charge
Q, Q_a	Quality factor, actual quality factor
Q_p	Parasitic pole quality factor
R_o	Output resistance
$S_n(\omega)$	Noise power spectral density
$S_{C_c}^{Q_p}$	Sensitivity of Q_p to C_c
T	Absolute temperature
T_o	Clock period
$T_a(\omega), T_i(\omega)$	Actual and ideal magnitude responses of SC biquads.
V_{DS}, V_{GS}	MOSFET drain-to-source and gate-to-source voltages
V_{DD}, V_{SS}	MOSFET positive and negative power-supply voltages
V_{DSSAT}	MOSFET drain-to-source saturation voltage
V_T	MOSFET threshold voltage
$v_k, v_{j,k}$	Node voltage vector, and j^{th} node voltage for phase k
$v_k^b, v_{j,k}^b$	Branch voltage vector, and j^{th} branch voltage for phase k

$V(z), V_k(z)$	Z transform, Z transform for phase k
$v_{cm}, V_{oCM}, V_{osCM}$	Common-mode voltage: general, output, and input-referred
v_d	Differential input voltage
v_o	output voltage
v', v'_{om}	Rate of change of voltage, slew-rate
W	MOSFET channel width
w_k, W_k	Input voltage value during phase k: time domain, and Z domain
Y_s, Y_p	Admittances at the source terminal of a cascode circuit, and including the conductance of the biasing current source
β	MOSFET current equation constant, with unit of Amp/Volt ²
δ_k	Duration of clock phase k
ϵ	SC integrator settling error
$\theta(\omega), \theta_D(\omega), \theta_N(\omega)$	phase error: in general, for delayed, and nondelayed sampling
τ	time constant
$\tau_p, \tau_{pl}, \tau_{ph}$	Time constant for a pole: in general, for low frequency and high frequency poles
τ_{pd}	Time constant for the dominant pole
μ	Carrier mobility
ω	Radian frequency
ω_o, ω_{op}	Natural radian frequency of a second-order system
ω_T	Amplifier or device unity-gain radian frequency

ω_p

Radian frequency of a parasitic pole

ω_{pl}, ω_{ph}

Radian frequency of a low frequency and high frequency pole

ω_{pd}

Radian frequency of dominant pole

ω_z

Radian frequency of a zero

CHAPTER 1 INTRODUCTION

1.1 Thesis Motivation

A periodically switched-capacitor (SC) serves as a charge transfer device with the rate proportional to voltage. As such it simulates a resistor. This concept was originated by Maxwell [72] but was forgotten. It has since re-emerged as a practical means to achieve monolithic active filtering by obviating the major shortcomings of resistors fabricated on integrated circuits.

The major SC advantage is twofold. First, large area resistors required for voiceband filters can be replaced by much smaller switched capacitors. Secondly, large error tolerances in the fabrication of resistors and capacitors on an IC result in large errors in filter time constants. These are effectively reduced by orders of magnitude by the replacement of resistors by switched-capacitors. Time constants then depend on capacitor ratios that can be established to high accuracy.

At the start of the present work SC application had been limited to voiceband frequencies. Thus it was considered very worthwhile to extend the upper frequency limit. The desirability of achieving this goal has provided the motivation for the present Ph.D. program. The following sections describe the importance of high-frequency SC networks towards achieving cost effective monolithic circuits for data communication and radio application. After this the basic SC concept is briefly explained and, finally, an overview of the thesis is presented.

1.2 Background

Switched capacitor circuits have come to be widely used during the last decade in voiceband filters [1]. SC circuits closely parallel their continuous time active RC counterparts, but are amenable to monolithic realization [2],[3]. The ability to define filter parameters by ratioed capacitors rather than RC products makes this possible.

In the late 1970's, the introduction of monolithic voiceband filtering using SC techniques made a major impact on the telecommunications industry. The ability to perform precision filtering without trimming on a MOS integrated circuit resulted in the "per-channel" coder-decoder (CODEC) with on-chip filters [4]. The advent of this chip made possible the design of digital central offices and private branch exchanges. The "per-channel" requirement for CODEC's indicates a massive demand for this single part placing it alongside the random-access memory (RAM), the read-only memory (ROM), and the microprocessor in importance.

The evolution of IC technology towards achieving further levels of circuit miniaturization is well known. Wideband op amps can be designed using the high-frequency transistors available in a short channel process and lower resistance transmission gates can be obtained. With these advances, the implementation of corresponding high-frequency switched capacitor filters and networks are possible. It was conjectured at the start of this investigation that the applicable frequency range of monolithic SC filters could be extended from voiceband to moderately high frequencies on the order of 500 KHz. However, in the course of this work precision

filtering has actually been demonstrated for 1 MHz signals. The impact of monolithic filtering in this signal band is expected to at least equal that of the voiceband SC filters used in CODEC's. Two important applications illustrate this point.

Signal processing for high speed data communications

In the telecommunications industry there is a tremendous desire to develop digital subscriber loop technology and many projects are underway [5],[65]. The goal is 160K baud full duplex data transmission over existing copper pair subscriber lines. The development of a single monolithic chip to achieve this function is highly desirable. High speed data communications requires analog subsystems to achieve line equalization, filtering, echo-cancellation, and line interface functions. These circuits must be capable of operation with signal passbands on the order of the baud rate.

Signal processing for radio frequency

In mobile and cellular radio systems, a significant cost reduction can be achieved with an increasing level of system integration. It is expected that IF filtering and subsequent demodulation can be achieved using switched-capacitor techniques.

1.3 The Switched-Capacitor Principle

The basic resistor/switched-capacitor equivalence is well-known and described for example in reference [2]. It is appropriate, however, to briefly review the basic principle in this introduction. In Fig. 1.1, an RC lowpass filter is shown in (a) along

Fig. 1.1 Switched capacitor/resistor equivalence. (a) RC lowpass (b) SC lowpass (c) Two phase nonoverlapping clock waveforms.

with the SC counterpart in (9). In one clock period the charge that is transferred is

$$Q = (v_1 - v_0)C_r \quad (1.1)$$

The average current is therefore

$$I_a = \frac{Q}{T} = (v_1 - v_0) \frac{C_r}{T} = \frac{(v_1 - v_0)}{R_{eq}} \quad (1.2)$$

where T is the period of the clock. The equivalent resistance is

$$R_{eq} = \frac{T}{C_r} \quad (1.3)$$

and the RC time constant of the filter is

$$\tau = R_{eq}C = \left(\frac{C}{C_r} \right) T \quad (1.4)$$

This simple example illustrates the key points. First, a resistor can be simulated by a periodically switched capacitor, with its resultant value proportional to the clock period. A large valued resistor can therefore be simulated by a small switched capacitor if a suitably long clock period is used. The switched-capacitor/resistor equivalence is upheld only for clock frequencies that are high with respect to signal frequencies. In most instances, this is not the case, and the SC network must be analyzed using discrete time techniques.

The other key point is that the filter time constant depends on a capacitor ratio. On a monolithic IC this corresponds to an area ratio that can be established with accuracies on the order of 0.1%. Thus with a precise clock, the switched-capacitor

technique allows precision RC time constants to be achieved economically on an integrated circuit.

1.4 High-Frequency Challenges

High-frequency SC filtering cannot be accomplished without overcoming several obstacles. To illustrate the basic problems that impede high-frequency SC filtering, an example is cited. The basic SC integrator is shown in Fig. 1.2, and its application in a typical filter, for example, is shown by the SC biquad in Fig. 1.3. As a result of their periodic switching, SC networks are sampled analog systems that undergo transients on every clock phase. To operate at high clock and signal frequencies, the transients must settle quickly. Their settling time, however, is limited by the finite bandwidth and slew-rate of op amps, and the nonzero-resistances of the MOS transmission gates used in the filters. Thus, the first and foremost challenge is the development of high-bandwidth op amps suitable for SC networks.

To achieve high speed op amps and low resistance switches, recent advances in short-channel process technology are exploited here for this analog application. Through the use of a VLSI 1.25μ CMOS technology, along with innovative circuit design, high performance elements are obtained.

The second challenge in achieving high-frequency filtering is the ability to simulate the impairments on the frequency response due to finite bandwidth elements. Existing SC networks simulation methods are formulated for ideal networks with no provision for including the effects of incomplete transients. In

Fig. 1.2 The two basic stray-free switched-capacitor integrators (a) Noninverting (b) Inverting.

Fig. 1.3 Switched-capacitor biquad filter.

fact, transients are assumed to settle in infinitesimally short time. As such, it was not possible to determine op amp bandwidth requirements and switch resistance requirements for specific applications. It was also not feasible to study SC networks, searching for the most promising high-frequency filter topologies.

Motivated by these restrictions in existing SC CAD tools, an SC network simulator for nonideal SC networks has been developed. This computer-aided design tool is very useful for studying the amenability of various SC structures for high-frequency operation.

The remaining challenge in achieving high-frequency SC filtering is to find the best circuits for this purpose. Not all circuits are equally sensitive to finite bandwidth effects, so it is important to find the least sensitive ones. To this end, an effort has been made to optimize the basic SC biquad. Since most high order filters employ biquads as building blocks, the results are extendible beyond the context of second-order filters. Through extensive analysis and simulations using the nonideal SC network simulator, a superior circuit has been found. Simulation and results from a test circuit confirm a differencing-input integrator based biquad filter to have a major performance advantage over other circuits.

1.5 Thesis Overview

Extending the application of SC filtering to higher frequency requires due consideration of many interrelated factors; these will be dealt with in detail in the following chapters. The present section provides a brief overview of the topics

encompassed. Chapter 2 elaborates the high frequency design considerations in general: the amenability of small geometry MOS circuitry to this end; the noise behavior and power-supply rejection of SC circuits, and the bandwidth and power dissipation considerations for these circuits. This chapter explains the challenges for high-frequency SC filtering and presents the relevant theory for understanding the remainder of the thesis.

Chapter 3 presents a new computer-aided analysis approach for nonideal linear SC networks. This computer-aided design (CAD) tool provides the frequency domain analysis of arbitrary SC networks comprised of finite bandwidth amplifiers and switch resistances. It represents a valuable tool for designing and optimizing high-frequency networks.

As previously stated, achieving high bandwidth op amps is a formidable challenge for high-frequency SC filters. Chapter 4 describes op amp design for high-frequency circuits. It focuses on transconductance op amps that can drive only capacitive loads, but have significant advantages for SC circuits. Theory and test results are presented for single-ended and differential versions of both current-steering and current-mirroring designs.

The op amps of Chapter 4 are suitable only for internal use in switched capacitor networks. They are unable to drive resistive loads or large capacitive loads, and are thus not suitable for driving signals off chip. Chapter 5 presents op amps for these other applications. Internally compensated op amps are developed that have a much improved AC power supply rejection. These op amps

are then applied to the realization of high current drive, low impedance wideband buffer amplifiers that are suitable for delivering HF filtered signals off chip.

Biquad alternatives for high-frequency SC filters are discussed in Chapter 6. Here various biquad options are extensively compared with regard to high-frequency operation using analysis and the nonideal SC network simulation tool of Chapter 3. These comparisons are made for both low impedance and infinite impedance (transconductance) op amps. The results of a CMOS test chip that compares the biquad alternatives are presented in Chapter 7. The measurements demonstrate high-frequency bandpass filtering of 1 MHz signals and validate the ranking of biquads presented earlier. A differencing-input biquad is shown to have significant advantages over other circuits.

Finally in Chapter 8 conclusions are drawn, and suggestions for future work in this area are made.

CHAPTER 2 HIGH-FREQUENCY CONSIDERATIONS

2.1 Introduction

High-frequency switched-capacitor filter design poses many problems that do not arise with voiceband applications. The objective of realizing high-frequency SC filters requires close attention to specific design considerations. The stray free SC integrator of Fig. 2.1 is used as a vehicle for discussion, since it is the building block for all practical SC filters [6]. We are specifically concerned with the ability of the integrator to operate properly at high clock rates while introducing low levels of noise and distortion. To answer such questions we must consider the op amp performance principally in terms of noise and speed. Additionally, we must look for noise mechanisms inherent in the SC circuitry surrounding the op amp. The present chapter explores the problems of noise, bandwidth and power dissipation in the high-frequency context. Along with this, methods of dealing with the design problems are proposed.

The merits of short-channel technology towards achieving high-frequency SC circuit operation are outlined in the Section 2.2. The details are presented later, but the main thrust can be briefly illustrated at this point. Thus, consider a short-channel process obtained by constant geometry scaling of all physical dimensions and voltages by a parameter K , less than one, and scaling the substrate doping by $1/K$ [7,8]. The transconductance of a scaled device is unchanged; the gate capacitance, however, is reduced by K . The implications are favorable for op amp design, since parasitic poles due to capacitive gate loads are consequently at higher

Fig. 2.1 Stray-free switched-capacitor integrator.

frequencies. In addition, the enhanced lithographic resolution of a short-channel process allows the scaling of SC circuit capacitors values by K , resulting in improvements in amplifier bandwidths. Further, power dissipation is reduced by a factor K^2 . The combined effect is a large increase in gain-bandwidth product for SC filter op amps, and a reduction in power dissipation, making high-frequency operation feasible.

Geometry scaling, although useful for the required speed of operation, results in degradation of performance in the areas of noise and working signal range, and hence in signal to noise ratio. The scaling of circuit capacitors increases noise, and the reduction in supply voltages decreases working signal range. These negative aspects related to scaling must be traded off against the high-frequency benefits.

The noise problems that arise, consisting of internal and power-supply transmitted noise, are described in Section 2.3. The internal noise is twofold: thermal noise and $1/f$ noise [9]. Thermal (Nyquist) noise power arising from MOS transmission gates varies inversely with capacitance. The $1/f$ (flicker) noise power of the op amps is inversely proportional to the gate area of the input differential pair. Together these imply an increase in the dominant noise mechanisms with scaling. Power-supply transmitted noise is attributed to finite op amp power-supply rejection and clock feedthrough; this is a serious concern in HF applications. A brief discussion of clock feedthrough is also presented in Section 2.3.

The bandwidth and power dissipation considerations pertaining to high-frequency operation are discussed in Section 2.4. Wide bandwidth is shown to require large current bias levels within op amps. Typically, bias levels that meet bandwidth specifications greatly exceed those necessary for slew-rate.

The objective of the present chapter is to present detailed theory concerning the high-frequency considerations. This material is important in the context of the entire proposal, since it establishes the rationale behind the design approaches that are subsequently presented.

2.2 Geometry Scaling of SC Circuits

In order to theorize about the performance of SC circuitry in a short-channel process it is useful to assume the technology has been derived by constant geometry scaling of an existing longer-channel process. This method is now widely accepted in industry and is therefore relevant. It is now possible to make qualitative comparisons about SC circuits realized in short-channel as opposed to those designed for longer-channel processes.

The effect of geometry scaling by a constant parameter K less than one has already been reported [7,8]. The procedure is to reduce all device dimensions, gate width and length (W and L), and oxide thickness (t_{ox}) by the factor K , and increase the substrate doping concentration by $1/K$. The supply voltage must also be reduced by K to avoid punchthrough. Table 2.1 summarizes the affect this scaling has on the key circuit parameters.

Dimensions: W, L, t_{ox}	K
Doping Concentration (N)	1/K
Supply Voltage (V)	K
Transconductance (g_m)	1
Device Bandwidth (f_T)	1/K
Current (I)	K
Delay (CV/I)	K
Power Dissipation (IV)	K^2
Power-Delay (CV squared)	K^3

Table 2.1 The Effect of Geometry Scaling on Circuit Performance

The principal requirements for high-frequency operation are wide-band op amps and short RC time constants for the MOS switches when driving the SC circuit capacitors. Together these allow output settling times less than the duration of the shortened clock phases required by HF filters. Consider now the effect of scaling on op amp bandwidth:

The saturation current equation for an MOS transistor is

$$I_{DS} = \mu \frac{C_o}{2} \frac{W}{L} (V_{GS} - V_T)^2 \quad (2.1)$$

where μ is the mobility, C_o is the gate capacitance per unit area, V_T is the threshold voltage, I_{DS} is the drain current and V_{GS} is the gate to source voltage. With constant geometry scaling this indicates a reduction in operating current by a factor

K. Transconductance however will be constant if $(V_{GS} - V_T)$ is also scaled by K. A simple cascade of two complementary common-source gain stages, as shown in Fig. 2.2, illustrates this point. The gain of the circuit remains the same $(g_{m1}g_{m3})/(g_{m2}g_{m4})$ whereas the gain-bandwidth product $(g_{m1}g_{m3})/(g_{m4}C_{g3})$ increases by a factor $1/K$, owing to the reduction in gate capacitance of M_3 .

Unfortunately, with short-channel transistors the common-source output impedance decreases due to an increase in channel length modulation effect [10], to drain-induced barrier lowering [11], and to velocity saturation [12]. This reduces voltage gain in current source biased common-source stages and presents a serious problem for op amp design. As will be seen in Chapter 4, this effect may be partially overcome by using cascoding to decrease output conductance. However, the use of cascode connections can reduce the voltage swing. Fortunately, this drawback may be minimized with the design techniques presented in that later chapter.

2.3 Noise Behavior of Sampled-Analog Circuits

From the preceding section it is clear that the design of operational amplifiers to achieve wide bandwidth is facilitated through the use of short-channel technology. The noise implications of this design approach are explored in the present section. In order to put this into perspective, it is first necessary to discuss the noise behavior of sampled analog circuitry. Specifically, this discussion centers on SC networks, with the remainder of the next few paragraphs serving as an introduction to the noise topic. The detailed presentation appears in the subsections that follow.

$$\frac{v_o}{v_i} = \frac{g_{m1}g_{m3}}{g_{m2}g_{m4}}$$

Internal pole @ $\omega_p = g_{m2}/C_{g3}$

$$\text{Gain Bandwidth Product GBW} = \frac{g_{m1}g_{m3}}{g_{m4}C_{g3}}$$

Fig. 2.2 Effect of constant geometry scaling on analog circuit gain and bandwidth.

Noise in SC circuits arise from two mechanisms: thermal (Nyquist) noise of the MOS switches, and the noise from the active devices within the op amps. The first mechanism, which is described in Section 2.3.1, is a consequence of the basic SC process: simulating the operation of resistors through the use of periodically switched capacitors. At low frequency this has the power spectral density of the equivalent resistors. The spectrum, however, departs from this considerably at frequencies beyond the Nyquist rate. The second mechanism, op amp. noise, consists of two components: $1/f$ noise resulting from the surface states of the input differential pair (described in Section 2.3.2) and broad-band noise from the output stage (described in Section 2.3.3).

In addition to these noise sources within an SC network, another factor has a bearing on overall noise performance. Finite power-supply rejection (discussed in Section 2.3.4) introduces additional noise and is of increasing concern for high-frequency circuits. It represents the extent to which power-supply noise will appear in the signal path. Power-supply transmission results from the finite power-supply rejection of the op amps themselves and also from clock feedthrough.

These distinct noise mechanisms are considered in the present section. The extent to which geometry scaling has a deleterious effect on the noise performance is also outlined.

2.3.1. Thermal Switch Noise

At low-frequency, the dominant noise source is the $1/f$ noise of the op amps,

while at high-frequencies the thermal switch noise dominates. In fact, if noise translation techniques such as chopper-stabilization [13] or correlated-double-sampling [14] are used to shift the $1/f$ noise up to higher frequencies, then again the thermal noise is the limiting factor. Basic thermodynamics dictates that white-noise with power spectral density $2kTR$ (where k is Boltzmann's constant and T is absolute temperature) is generated by any resistor in an electric circuit. With SC networks, the action of a resistor is imitated in a limited sense, by a capacitor and a set of periodically switched MOS transmission gates. However, detailed analysis together with experimental results [15,16] confirm that at signal to clock frequency ratios well below unity the basic noise relation of a simple resistor is upheld.

The analysis proceeds by replacing each MOS transmission gate by a suitable equivalent circuit; this consists of an idealized switch in series with a resistance R_{on} representing the nonzero switch "on" resistance plus a white-noise generator with power spectral density $2kTR_{on}$ representing the thermal noise of the switch. The arrangement is shown in Fig. 2.3(b). Two types of noise are passed to the output of the integrator: under-sampled broad-band noise and gated broad-band noise.

Under-sampled broad-band noise

This type of noise arises when a wide-band noise is sampled by a capacitor, for instance when switch S_1 of Fig. 2.3(a) opens. The rate at which the noise is periodically sampled is much lower than the noise equivalent bandwidth; this results in an aliasing of all the noise to frequencies below half the Nyquist rate.

$$S_n(\omega) = \frac{2kT}{C_i f_s} \left[(C_i f_s / \omega)^2 + \tau \omega_0 / (4B_{eq}) \right]$$

Fig. 2.3 Thermal noise model for an SC integrator. (a) SC integrator (b) SC integrator with noisy switches (c) Simplified noise model.

Gated broad-band noise

This refers to wide-band noise that passes through a periodically switched transmission gate. When the gate is open, the noise goes through directly; however, when the gate is closed, no noise passes. It turns out that in this situation the gated noise power is lower than that of the noise itself; the degree of attenuation is proportional to the duty cycle of the gate [16].

For the integrator of 2.3(b) a combination of the two noise types is seen. Direct noise from S_2 is gated to the output during phase Φ_2 ; this noise is filtered by the transfer function to the output formed by the op amp, resistor and capacitors. Wideband noise is aliased down by the action of sampling capacitors in two places: by the input capacitor when S_1 opens and by the integrating capacitor when S_2 opens. In both cases the noise power spectral density is filtered by the appropriate transfer function.

Since the analysis is lengthy, the reader is directed to the references already cited [15], [16] and only the main results will be covered here. The noise model for the SC integrator of Fig. 2.3(a) is presented; it may be useful because of the wide applicability of the circuit. The power spectral density (PSD) of the input-referred noise of the integrator is:

$$S_n(\omega) = 2kT(T_0/C_i) \left[\sin^2(\omega T_0/2) + \tau \omega_0 / B_{eq} \sin^2(\omega T_0/2) \right] \quad (2.2)$$

where: k = Boltzmann's constant, T = absolute temperature, C_i = input capacitance, ω_0 = sampling radian frequency, T_0 = sampling period, ω = radian

frequency, τ = duty cycle of sampling clock, and B_{eq} = noise-equivalent bandwidth of the thermal noise.

The first term represents the under-sampled wide-band noise and is predominant in the range of frequencies below the Nyquist rate. The other term is a consequence of the low-pass filtered direct noise with a cut-off frequency of a few megahertz. Here the low-pass filtering is due to the first order RC low-pass filter formed by the nonzero "on" resistance of the MOS switch and the capacitor, and the transfer function of the op amp.

At low frequencies the relation simplifies to:

$$S_n(\omega) = 2kT(T_0/C_1), \quad (2.3)$$

the noise spectrum of an equivalent resistance of $R_{ieq} = T_0/C_1$, verifying earlier remarks. This equation suggests a simplified circuit model shown in Fig. 2.3(c) consisting of a Miller integrator with a noiseless input resistor: this is driven by its equivalent noise source with a power spectral density as above followed by a noise source at the output with a power spectral density of;

$$S_n(\omega) = 2kT(T_0/C_1)[\pi\omega_0/(4B_{eq})] \quad (2.4)$$

The model results in a noise PSD at the output of:

$$S_n(\omega) = 2kT(T_0/C_1)[(C_1 f_s/\omega)^2 + \pi\omega_0/(4B_{eq})] \quad (2.5)$$

One important result from the above noted relationship is that the thermal noise power spectral density varies inversely with capacitor size. Unfortunately, this

means that thermal noise performance must be traded off against circuit speed when scaling SC networks.

2.3.2 1/f Noise in MOS Operational Amplifiers

The low-frequency noise behavior of SC circuits is usually dominated by the 1/f noise contributed by the MOS op amps. This noise is highly process dependent and is concentrated at low frequencies; the corner is typically between 10 kHz and 100 kHz. Many theories have been presented to explain this noise [17], and the consensus is the following.

The silicon/silicon dioxide interface gives rise to extra electron energy states at the boundary, referred to as surface states. This is the channel surface of the MOS transistor, and hence the characteristics of the device depend somewhat on these states. Charging and discharging these states affects the amount of carriers available to flow as a current. In addition electrostatic effects from any electrons occupying the states may alter the device threshold. The surface states are located in the band gap; consequently they can only be charged or discharged slowly, giving rise to the low frequency dominance of the effects. A generally accepted relation for the noise spectrum is [9]

$$S_{1/f}(\omega) = K / (C_0 W L) \times (1/\omega)^a \quad (2.6)$$

Here a is a constant close to unity, and K is a constant with units of $V^2 F/Hz$ and is on the order of 10^{24} . There is a significant concern here for high-frequency circuits.

The power spectral density of 1/f noise will increase linearly, as transistor

dimensions are reduced according to constant geometry scaling.

Since $1/f$ noise is concentrated at low frequencies, it may be treated as narrow-band noise. In the case of voice-band filters it is possible to translate this noise to frequencies beyond the passband, greatly enhancing the dynamic range of the circuit. Two methods of frequency translation have been reported in the literature to date.

K. C. Hsieh, along with the Berkeley group [13], has demonstrated the chopper-stabilized approach to $1/f$ noise reduction. The method uses differential choppers on both sides of the differential-pairs inside all op amps. This convolves the $1/f$ noise of the input pair with the line spectra of the chopping waveform (a square waveform with zero DC offset) to shift the noise up to odd harmonics of the chopping waveform; hence the DC component of the noise is now at $3f_c$, $5f_c$, etc., (f_c = chopping frequency). This is well beyond the passband of the filter, if f_c is made equal to the clocking rate of the filter.

An alternative approach is the correlated-double-sampling technique often used with CCD's [18]. With this method, any voltage offset due to $1/f$ noise in an op amp is sampled on an input capacitor on one cycle, and then switched in series with the input on the following cycle. This removes the effect of the offset, which is a manifestation of the $1/f$ noise. It is simple to incorporate this into a SC network and test results on an experimental circuit have been reported by Carleton University [14].

The ability to resolve the $1/f$ noise problem with voiceband SC networks means that noise performance within the limits of the thermal noise characteristics can be achieved. For high-frequency circuits, however, there is the possibility that the passband of the filter can be located above the $1/f$ corner. In this case any method of $1/f$ noise reduction is unnecessary and noise will be attributable mainly to thermal switch noise and to broadband noise from the output of the MOS op amps.

2.3.3 Operational Amplifier Broadband Noise

In addition to the low frequency $1/f$ noise the op amp also contributes broadband thermal noise. This noise must be analyzed in a similar manner to that used for the thermal noise of the MOS switches. Since the noise extends to frequencies much higher than the clock rate, the broadband noise is under-sampled and aliased into the frequency band below the Nyquist rate. The analysis of this noise is complicated by the fact that the op amp has different characteristics above and below its unity-gain frequency.

For frequencies below the unity-gain bandwidth, the input-referred thermal noise may be considered. Suppose it is assumed that the input-referred thermal noise is relatively flat in this frequency range and that the switches sample at a rate much lower than the unity-gain bandwidth. Then the effect of aliasing can be treated by using an input noise generator with noise power spectral density of the broadband input-referred noise multiplied by the ratio of the unity-gain bandwidth to the sampling rate.

Beyond the unity-gain bandwidth the op amp gain is less than one, and its output impedance, which is decreased by an amount equaling the loop-gain, is no longer reduced by feedback. Thus the design of the op amp output stage and the location of the compensation point have a substantial bearing on noise performance. The circuitry from the compensation point to the output contributes the thermal noise beyond the unity-gain bandwidth. The circuitry ahead of the compensation point has its noise rolled off by the compensation network and is not a factor. The bandwidth of the output stage past the point of compensation is important in determining the additional noise contribution. If, for example, the op amp has a low output impedance due to an output buffer, then a wider noise equivalent bandwidth will be aliased down by a following stage. If, alternatively, the output stage has high impedance, then the noise will be sampled over a low bandwidth and the effect will be less pronounced.

The op amp compensation scheme presented in Section 4.2 is expected to minimize the effect of broadband noise. With this approach, the dominant pole is formed by the output of the amplifier and the load capacitor; consequently the bandwidth of the output stage is very low. The conventional approach to compensation is to use a pole-splitting capacitor to slow down the first stage of the amplifier and speed up the output stage. The bandwidth of the output stage must be far above the unity-gain bandwidth, in this case, in order to ensure closed-loop stability. The new method has a much lower output bandwidth, since the output stage must have an associated dominant pole at a frequency several decades below

the unity-gain bandwidth.

It is conjectured that amplifiers that achieve closed-loop stability by having a low-frequency pole formed at the output, as described in Section 2.4, will offer superior performance in terms of broadband noise; this is due to their inherent band limiting property. The low bandwidth of the output stage will likely make the thermal noise contribution negligible beyond the unity-gain bandwidth.

2.3.4 Power-Supply Rejection

Power-supply rejection (PSR) is a measure of the extent by which noise on a power supply is attenuated by a circuit before appearing as an output signal. Inadequate power-supply rejection severely impacts noise and cross talk performance owing to nonzero power rail impedance; it may thus prove to be a serious concern with high-frequency circuits. Inadequate supply rejection is chiefly attributable to the finite PSR of the resident op amps, to the clock feedthrough from the analog transmission gates, and capacitive coupling through the junction of the gates adjacent to the op amp integrating node.

When the PSR is multiplied by the open-loop transfer function the input-referred power-supply rejection ratio (PSRR) is obtained: $PSRR(\omega) = PSR(\omega) A(\omega)$, where A is the open-loop gain and ω is the radian frequency. At high-frequencies the PSRR of typical op amps drops as a consequence of the falling open-loop gain required for frequency compensation. Additionally, at high-frequency larger MOS transmission gates must be used to meet the short settling time requirements.

Clock feedthrough increases with gate area, and the PSR is reduced accordingly. These mechanisms are described in the following sections.

Op Amp Power-Supply Rejection

The finite power supply rejection of the resident op amps contributes to the overall circuit PSR as expected. When op amps are connected as integrators an additional problem arises. Coupling of charge into the integrator summing junction through the gate-to-drain/source overlap capacitances of the inverting input transistor may be a factor: this occurs if the operating point of the input differential-pair varies with power-supply level. The result is an output level fluctuation induced by power-supply noise.

The power-supply rejection depends on both the op amp and biasing circuitry. Usually the bias generator is designed to maintain a constant gate-source drive on the current-source transistors: these are M_5 and M_7 in Fig. 2.4. If this can be achieved, then the DC PSRR will be on the order of the DC open-loop gain. The AC PSRR to V_{DD} , however, rolls off prematurely due to the effect of the compensation capacitor C_c ; at moderate frequencies the gate of transistor M_6 becomes effectively shorted to its drain for AC, and the output follows the V_{DD} noise. The op amps described in Section 2.4 of this chapter and later discussed in Chapter 4 are compensated by their load capacitors and have improved AC PSRR. In addition, in Chapter 5 internally compensated op amps with improved AC PSRR are described and analyzed in detail.

Fig. 2.4 Voiceband internally-compensated CMOS op amp.

The second op amp related influence on the overall PSR is a consequence of the Miller integrator circuit connection, as shown in Fig. 2.5. This, however, is the configuration required in the popular stray-free state-variable SC filters. The integrator has the property that the inverting input is a charge-summing node held at virtual-ground by the feedback action of the integrating capacitor C_1 [27]: any signal capacitively coupled to this node will displace the output according to:

$$\frac{dV_0}{dV_{SS}} = \frac{C_{GS}}{C_1} \left(\frac{dI}{dV_{SS}} \times \frac{1}{2g_{m1}} + \frac{dV_{T1}}{dV_{SS}} \right) \quad (2.7)$$

$$\frac{dV_0}{dV_{DD}} = - \frac{C_{GD}}{C_1} \left(1 - \frac{dI}{dV_{DD}} \times \frac{1}{2g_{m3}} \right) \quad (2.8)$$

where I is the current in M_5 , V_{T1} is the threshold voltage of M_1 and M_2 , C_{GS} and C_{GD} are the gate-source and gate-drain capacitance of M_1 respectively and C_1 is the integrating capacitor.

This suggests two methods of enhancing power-supply rejection. First would be the use of a supply-independent current source to bias the input source coupled pair. Second is finding some means for reducing the variation of threshold voltage with negative power supply (an NMOS input stage is assumed here). This can be done by placing the input devices in a separate well, permitting a direct source-to-well connection, thus eliminating the backgate effect. Alternatively, a lightly doped substrate might be considered: this reduces the backgate effect but does not eliminate it.

Fig. 2.5 Effect of the parasitic capacitances of an op amp input transistors on the power supply rejection of an integrator.

Clock Feedthrough

The use of MOS transmission gates as switching elements in SC networks has deleterious results: power-supply rejection is degraded and DC offsets are induced. The square-wave clock signals driving the gates of the MOS switches capacitively couple to the signal path through the overlap capacitances. In addition, channel charge flows in and out of the MOSFETS as they turn on and off, generating charge errors in the network capacitors. Figure 2.6 shows these nonideal influences acting on a simple SC integrator.

The overlap capacitances connect V_{DD} and V_{SS} (the clock high and low levels) as additional inputs to the integrator. Through this mechanism supply levels are sampled and they influence the output signal. The channel charge is also supply dependent, governed by the applied gate-source and bulk-source voltages. This charge flows from the surrounding network, resulting also in supply dependent errors.

Analysis of the clock feedthrough effect on a sample and hold capacitor [69] as in Fig. 2.7 shows the channel charge to be dominant over the influence of the overlap capacitances. Fast clock gate signals compound the problem by forcing the channel charge to feedthrough to the maximum extent. This sets an upper limit on clock feedthrough of

$$\Delta V_0 = \frac{Q_{CH}}{C_H} = \frac{C_G}{C_H} (V_{GS} - V_T) = \frac{C_G}{C_H} (V_{DD} - V_{IN} - V_T) \quad (2.9)$$

where Q_{CH} is the channel charge, C_G is the gate oxide capacitance, and C_H is the

Fig. 2.6 Clock feedthrough in an SC integrator. (a) SC integrator (b) Feedthrough of the ϕ_1 clock as M_1 opens (c) Feedthrough of the ϕ_2 clock as M_2 opens.

Fig. 2.7 Clock feedthrough effect on a sample and hold capacitor.

hold capacitor. Slow-edged clock signals, however, alleviate the effect considerably. With sufficiently slow clock signals the channel charge has time to flow to the low impedance voltage source instead of to the hold capacitor. Thus for slow signals the mechanism is the capacitive coupling of the overlap capacitance C_{GDO} to the hold capacitance C_H . The gate swings from a gate-source voltage equaling the device threshold voltage V_T , to the clock low level V_{LOW} , feeds through an offset voltage of

$$\Delta V_0 = \left[\frac{C_{GDO}}{C_{GDO} + C_H} \right] (V_{IN} + V_T - V_{LOW}) \quad (2.10)$$

One useful finding is that the feedthrough is proportional to the ratio of gate capacitance (of the transmission gate transistors) to the integrating capacitor; clearly any effort to reduce this is worthwhile. Unfortunately with high-frequency SC filters, this is confounded by the need to use larger transmission gates to achieve low switch "on" resistance.

In order to reduce the RC time constants associated with the charging and discharging of filter capacitors through transmission gates, low switch "on" resistance is required. This, however, can only be achieved by increasing the size of the gate transistors at the expense of corresponding increases in gate capacitance and clock feedthrough. Also, any reduction in the size of filter capacitors, aimed at enhancing op amp bandwidth in order to improve settling times, can only be achieved at the expense of proportionate increases in clock feedthrough.

A precise theory describing clock feedthrough in switched capacitor networks has yet to appear in the literature. The problem is complicated by many factors.

Consideration of the transmission gates as MOS devices rather than as idealized switches is necessary to look at charge movement at the microscopic level. The same gates must be idealized as switches to look at the macroscopic behavior, i.e., at the noise power spectral density. In addition, the problem is further complicated by factors such as clock rise and fall times and edge spacing.

The effects of geometry scaling relevant to clock feedthrough is of particular interest. If all dimensions and voltages are decreased by the factor K and concurrently the doping is increased by $1/K$, the ratio of switch capacitance to gate capacitance to integrator capacitance will be unchanged. The switch conductance is also constant with respect to scaling, whereas the load capacitors are decreased by the factor K . This means that the RC time constants associated with the switching of capacitive loads are decreased by K . This result suggests that gate width may be reduced beyond the scaling parameter to maintain a previous time constant. The feedthrough level can be reduced accordingly.

2.4 Bandwidth and Power Dissipation Considerations in High Frequency Switched Capacitor Circuits

Amplifier power dissipation associated with a high-frequency SC circuit can prove to be the ultimate design constraint. A basic trade-off exists between bandwidth, slew-rate and power consumption, which must be confronted. The problem, simply stated, is that high speed op amps tend to consume a lot of power. These important considerations are developed in the present section. Later in Chap. 4, an op amp compensation approach favoring low power dissipation is

presented.

Before facing this question it is necessary to relate op amp parameters such as gain, bandwidth and slew-rate to system performance specifications. A biquad filter, for example, requires constraints on deviations of the undamped natural frequency ω_0 , and the quality factor Q , related to nonideal op amp performance. Op amp specifications may be established from the computer-aided design approach of Chapter 3, or from analytic formulae based on simplifying assumptions limiting them to first order responses, as discussed in Chapter 6. This area could still benefit from further work; any analysis which included nonlinear behavior, such as slew-rate limitation, would be useful.

The role of the operational amplifier in active SC circuits is to provide a means for transferring all of the charge stored on one capacitor to another. This charge transfer is typically accomplished with a switched capacitor integrator as shown in Fig. 2.1. Operation of this circuit is described in various publications [19]. For examination of the role of the operational amplifier in this circuit it is necessary to evaluate its bandwidth requirements and corresponding power dissipation. The op amp endeavors to bring its inverting input to ground whenever the switches change state. In so doing, a charge from the input is transferred to the integrator capacitor, driving the output to a new level by the end of the ensuing transient.

The effective capacitive loading is C_L in parallel with the series combination of $C_I + C_{in}$. This can be simplified to $C_L + C_{in}$, if, $C_I \gg C_{in}$; this is usually the case with circuits operating at moderate signal-to-clock frequency ratios. The op amp

must slew this load in a finite time, depending on the application, suggesting a constraint on the minimum slew-rate. A sinusoidal output, $v(t) = a[\sin(\omega t)]$, for example, imposes a lower bound on slew-rate of $\left. \frac{dv}{dt} \right|_{\max} > 2a\omega$ assuming a two phase circuit. This leads to the establishment of a link between bandwidth requirements, in the form of slew-rates, and the corresponding power dissipation.

The slew-rate is governed by the fundamental relationship for a capacitor: $i = C(dv/dt)$. Assuming the quiescent bias current of the op amp is diverted to the capacitive load during transients, the power dissipation can be related to the slew-rate. The CMOS inverter of Fig. 2.8 is sufficient to make the point. The fixed bias P channel device acts as a constant current source load for the N channel common-source amplifier. The maximum slew-rate in the positive direction is attained when the lower device is completely off and the constant current source charges the load capacitor at a rate I/C ; here I is the current bias level of the P channel device and C is the load capacitance. This example is typical of most MOS op amps whose maximum output current available for slewing is limited to an internal fixed bias level.

The important fundamental relationship linking power dissipation P to slew-rate

$\left. \frac{dv}{dt} \right|_{\max}$ is:

$$P_D = (V_{DD} - V_{SS})I = (V_{DD} - V_{SS})C \left. \frac{dv}{dt} \right|_{\max} \quad (2.11)$$

Fig. 2.8 CMOS inverter as a gain stage.

Alternatively, slew-rate equals

$$\left. \frac{dv}{dt} \right|_{\max} = P_D / [(V_{DD} - V_{SS})C] \quad (2.12)$$

Clearly an important tradeoff exists here which is crucial in high frequency circuits where high slew-rates are mandatory. Any circuit that can develop a slewing current higher than some internal quiescent bias level will benefit from low power dissipation.

The relationship between bandwidth and power dissipation is discussed next. Wide band op amps are a necessity in high frequency applications and large bandwidths are achieved at the expense of power consumption. To establish this, consider once again the inverter of Fig. 2.8. This amplifier has a D.C. gain of g_m/G_0 , where $G_0 = g_{01} + g_{02}$, and it has a single pole at $\omega_P = G_0/C_L$. In unity-gain feedback the bandwidth equals the gain bandwidth product, $\omega_T = g_m/C_L$. With these loop dynamics the step response of the amplifier is exponential, with a time constant of $1/\omega_T$.

The power dissipation is related to the gain bandwidth product as follows:

$$g_{m1} = 2\sqrt{K'(W/L)I_{D1}} \quad \text{where } K' = \mu C_0/2$$

$$P_D = \frac{(V_{DD} - V_{SS})}{4K'W/L} C_L^2 \omega_T^2 \quad (2.13)$$

Hence for MOS circuits power dissipation varies as the square of the gain-bandwidth product. This relationship illustrates the difficulty in jointly achieving wide

bandwidth and low power consumption. Fortunately, geometry scaling reduces power consumption by a factor of K^2 , as mentioned in Section 2.2. Scaling also increases gain-bandwidth product by a factor $1/K$.

2.5 Conclusion

This chapter covered detailed theory related to high-frequency switched-capacitor (HFSC) filters. It provides the necessary background material that is relevant to understanding the remainder of the thesis.

The ongoing trend towards short-channel CMOS technology was identified as a key factor in the development of high-frequency filters. The higher transconductance and lower power dissipation of short-channel devices is amenable to HFSC filtering. However, the scaling of transistor and capacitor geometries and voltages, can impact noise performance. Thus, SC filter noise mechanisms were discussed in the context of reduced circuit dimensions.

Op amp bandwidth and power dissipation, are important interrelated factors in HFSC filters. The requirement for wideband amplifiers in such filters is emphasized. A fundamental relationship that exists between an op amp's slew-rate and bandwidth, and its power dissipation has also been derived in this chapter. This result shows that high speed can be achieved at the expense of a significant increase in power dissipation. This result underscores the importance of further advances in submicron technology, towards continued advances in the frequency of operation of SC filters. It also emphasizes the importance of the development of SC

filter topologies with reduced sensitivity to finite op amp bandwidths.

CHAPTER 3 COMPUTER AIDED ANALYSIS OF NONIDEAL SWITCHED-CAPACITOR NETWORKS FOR HIGH-FREQUENCY APPLICATIONS

3.1 Introduction

In this chapter a formulation of equations for the computer aided analysis of nonideal switched-capacitor (SC) networks is presented to assist in the design and analysis of high-frequency SC filters.

The topic of equation formulation oriented toward computer-aided design (CAD) of general switched-capacitor networks has been tackled by many researchers in recent years. The interest is primarily due to the pervasiveness of monolithic analog integrated circuits that employ switched-capacitor circuit techniques. Details on efficient CAD programs for ideal SC networks have been published by Brglez [31],[33], Liou and Kuo [32], Tsividis [34], Vandewalle, DeMan and Rabaey [35],[36], Vlach, Singhal, and Vlach [37], and by a host of others too numerous to mention. Owing to the abundance of material in this area, and for the sake of brevity, the author has restricted the list here, and later, to those works he is most familiar with and feels are most representative.

More recently, a desire to extend the use of switched capacitor filters to higher frequencies has emerged and some such filters have been reported [21],[55],[64]. Several researchers have pointed out the theoretical limitations imposed by op-amp finite gain and bandwidth and, subsequently, the influence of nonzero switch resistance. The dynamics associated with finite bandwidth op-amps and nonzero

switch resistance in SC networks give rise to incomplete settling of transients in the available time; this has a deleterious bearing on frequency response. Gain and bandwidth limitations were analyzed first by Temes [42], and followed by papers by Martin and Sedra [43], Geiger and Sanchez-Sinencio [44], and others. Finite switch-resistance problems were recently reported by Sedra, Datar and Chomik [45].

Motivated by the desire to generate analysis programs that are applicable to these recent problems, many researchers have directed their efforts to analysis of switched-capacitor networks with the inclusion of op-amp modelling and switch resistance. The earliest works come from Liou [29], followed later by Strom and Signell [30]; however, their techniques are intended for active RC filters, and in fact break down for short circuit and open circuit switches [48]. In other respects their formulations are general and can model SC networks with nonidealities; however, the formulations are not oriented for computer solution. Other formulations oriented towards SC networks have been published by Rabaey, Vandewalle, and DeMan [38], Cutland, Lau and Sewell [39], Rudd and Schaumann [40], Wehrhahn [41], and others. From these studies it is apparent that any approach for the complete spectral analysis of general nonideal SC networks requires the solution of complicated equations, and is very time consuming.

Here, rather than tackle the complete spectral analysis, the solution is restricted to the discrete time system associated with an arbitrary nonideal SC network. (This restriction applies also in [39] and [40].) The restriction of sampled and held inputs is also invoked. The solution is therefore applicable only at a set of sampling

instants that are defined as the ends of each distinct clock phase. This is usually sufficient, since in many cases high-frequency SC filters are used only internally within a monolithic signal processing system and they interact with the rest of the system only in terms of the sampled data or discrete time values. This is the case, for example, when an SC filter is followed by an analog-to-digital converter.

The analysis of the discrete system is a subset of the general case of complete spectral analysis that includes continuous signal inputs and all frequency domain effects, such as $\sin(x)/x$, and has been presented in [38]. The formulation presented here, and its implementation, differ from those of earlier work in several respects. First, all ideal switches are eliminated on each phase and, instead, compact subnetworks are analyzed; this typically halves the number of nodes of a network. An eighth order SC ladder filter published by Martin and Sedra [47], for example, has its number of nodes reduced from thirty-three to seventeen with this approach. Next, the equations are formulated so that their coefficients are determined by a sequence of time domain transient analyses, using capacitor branch voltages and input signal sources as initial conditions. Efficient time domain analysis approaches, that already exist, are used at this step; in this case, the backward Euler integration formula is used with the modified nodal analysis formulation applied to the compact subnetworks. The sequence of transient analyses is performed only once. Finally, this is followed by a frequency independent preprocessing of the resulting equations; this is likewise carried out but once.

The transient method of coefficient generation is very efficient in the context of the analysis of nonideal switched capacitor networks. Since only linear models are used, Newton-Raphson iteration is not required at each timestep; only a single solution is necessary. In addition, the time required to perform the transient analysis is significantly reduced by the network compaction algorithm.

These notions have been incorporated in a computer program called NISCAP, an acronym for Nonideal Switched-Capacitor Analysis Program [66]; it implements the formulation of equations and the associated transient response method of coefficient determination that are developed below. Some examples are included to illustrate its application to high frequency switched capacitor networks.

3.2 Formulation of Equations

The analysis is restricted to the discrete time system associated with the network; it applies only to the value of node voltages at sampling instants. This is, however, sufficient for applications where sampled and held inputs are used. Networks containing ideal switches, capacitors, resistors, ideal op-amps, and voltage controlled current and voltage sources, as shown in Fig. 3.1 can be analyzed. High-order op-amp models can be constructed from these available elements.

As an illustrative example, the SC network of Fig. 3.2 is considered first. The network includes a resistor that gives rise to exponential transient responses on each phase. The connections of the network on the two phases are shown in Figs. 3.2(b) and 3.2(c). At the end of a phase, the node voltages are an algebraic sum of the

Fig. 3.1 Circuit elements required for simulation of nonideal linear SC networks.

Fig. 3.2 Switched-capacitor network with dynamic behavior during each clock phase due to a resistor. (a) Complete network (b) Compact subnetwork during ϕ_1 (c) Compact subnetwork during ϕ_2 .

capacitor branch voltages at the end of the previous phase along with a sum of the input voltages applied during the phase. At the end of phase one:

$$\begin{bmatrix} v_{1,1} \\ v_{1,2} \\ v_{1,3} \end{bmatrix} = \begin{bmatrix} -(\alpha + \beta e^{-\delta_0/\tau_1}) & \beta(1 - e^{-\delta_0/\tau_1}) \\ -\alpha(1 - e^{-\delta_0/\tau_1}) & \beta + \alpha e^{-\delta_0/\tau_1} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_{2,1}^b \\ v_{2,2}^b \end{bmatrix} + \begin{bmatrix} \alpha + \beta e^{-\delta_0/\tau_1} \\ \alpha(1 - e^{-\delta_0/\tau_1}) \\ 1 \end{bmatrix} v_{2,3}$$

Similarly at the end of phase two:

$$\begin{bmatrix} v_{2,1} \\ v_{2,2} \\ v_{2,3} \end{bmatrix} = \begin{bmatrix} 0 & -1 \\ 0 & e^{-\delta_1/\tau_2} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_{1,1}^b \\ v_{1,2}^b \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \\ 1 \end{bmatrix} v_{1,3}$$

The coefficients and time constants are defined as: $\alpha = C_1/(C_1 + C_2)$, $\beta = C_2/(C_1 + C_2)$, $\tau_1 = RC_1C_2/(C_1 + C_2)$, $\tau_2 = RC_2$, and $\delta_0 = \delta_1 = T/2$, and T is the period of the clock. Non-overlapping, 50% duty cycle clocks are assumed.

With this notation, the first subscript represents the phase, and the second subscript represents the node number; the superscript b indicates a branch voltage variable. In the two node equations, node and branch variables are mixed. To obtain equations in terms of only node variables we note that, in this example, the capacitor node and branch voltages are related as follows:

$$\begin{bmatrix} v_{1,1}^b \\ v_{1,2}^b \end{bmatrix} = \begin{bmatrix} -1 & 0 & 1 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_{1,1} \\ v_{1,2} \\ v_{1,3} \end{bmatrix} \quad \text{during phase one}$$

and

$$\begin{bmatrix} v_{2,1}^b \\ v_{2,2}^b \end{bmatrix} = \begin{bmatrix} -1 & 0 & 1 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_{2,1} \\ v_{2,2} \\ v_{1,3} \end{bmatrix} \quad \text{during phase two}$$

We may therefore rewrite the first two equations now strictly in terms of node voltages; at the end of phase one

$$\begin{bmatrix} v_{1,1} \\ v_{1,2} \\ v_{1,3} \end{bmatrix} = \begin{bmatrix} -(\alpha + \beta e^{-\delta_0/\tau_1}) & \beta(1 - e^{-\delta_0/\tau_1}) \\ -\alpha(1 - e^{-\delta_0/\tau_1}) & \beta + \alpha e^{-\delta_0/\tau_1} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} -1 & 0 & 1 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_{2,1} \\ v_{2,2} \\ v_{2,3} \end{bmatrix} + \begin{bmatrix} \alpha + \beta e^{-\delta_0/\tau_1} \\ \alpha(1 - e^{-\delta_0/\tau_1}) \\ 1 \end{bmatrix} v_{2,3}$$

Similarly at the end of phase two:

$$\begin{bmatrix} v_{2,1} \\ v_{2,2} \\ v_{2,3} \end{bmatrix} = \begin{bmatrix} 0 & -1 \\ 0 & e^{-\delta_1/\tau_2} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} -1 & 0 & 1 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_{1,1} \\ v_{1,2} \\ v_{1,3} \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \\ 1 \end{bmatrix} v_{1,3}$$

At this point, the step towards the general formulation for a multi-phase network is taken:

$$v_1 = B_1 v^b + g_1 w_1 \quad \text{for phase 1} \quad (3.1)$$

$$v_2 = B_2 v^b + g_2 w_2 \quad \text{for phase 2}$$

$$v_k = B_k v_{k-1}^b + g_k w_k \quad \text{for phase } k; \quad 2 \leq k \leq N$$

where v_k , for example, represents the node voltage vector on phase k ; in the example, this was the leftmost vector in the first equations. The matrix just right of

the equal sign is the B_k matrix for the k^{th} phase. The g_k vector is the rightmost vector in the equation for the k^{th} phase. Vector w_k represents the value of the input on the k^{th} phase. To relate capacitor branch voltages to node voltages, as was done in the example, the following relation is applied:

$$v_k^b = A_k^T v_k; \quad 1 \leq k \leq N \quad (3.2)$$

where A_k^T is the transpose of the incidence matrix of the capacitor graph on the k^{th} phase; in the example, this is the matrix next to the B_k matrix. Applying this relation to equation 3.1 results in:

$$v_1 = B_1 A_N^T v_N + g_1 w_1 \quad \text{for phase 1} \quad (3.3)$$

$$v_2 = B_2 A_1^T v_1 + g_2 w_2 \quad \text{for phase 2}$$

$$v_k = B_k A_{k-1}^T v_{k-1} + g_k w_k \quad \text{for phase } k; \quad 2 \leq k \leq N$$

The notation is simplified slightly with the following definition:

$$C_1 = B_1 A_N^T \quad (3.4)$$

$$C_k = B_k A_{k-1}^T; \quad 2 \leq k \leq N$$

Rewriting equation 3.3 we obtain:

$$v_1 = C_1 v_N + g_1 w_1 \quad (3.5)$$

$$v_2 = C_2 v_1 + g_2 w_2$$

$$v_k = C_k v_{k-1} + g_k w_k; \quad 2 \leq k \leq N$$

3.3 Frequency Response of the Discrete Time System

The z-transform of the system of equations in 3.5 can now be taken to determine the frequency response of the discrete system of equations that describe the network. In this section we closely parallel the presentation of Vlach and Singhal, which was used for the solution of a discrete system of an ideal SC network [37]. First we define the z-transforms of all the vector variables.

$$\sum_{n=-\infty}^{\infty} v_k(nT + \sigma_k) z^{-n} = V_k(z) \quad 1 \leq k \leq N-1 \quad (3.6)$$

$$\sum_{n=-\infty}^{\infty} v_N(nT) z^{-n} = V_N(z) \quad (3.7)$$

and note that

$$\sum_{n=-\infty}^{\infty} v_N(nT + \sigma_N) z^{-n} = \sum_{n=-\infty}^{\infty} v_N(nT + T) z^{-n} = z V_N(z) \quad (3.8)$$

Similar definitions apply for the z-transforms of w_k . The z-transform for the system of equations in 3.5 is:

$$\begin{bmatrix} I & & & \\ -C_2 I & & & \\ & -C_3 I & & \\ & & \ddots & \\ & & & -C_N \quad zI \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ \vdots \\ V_N \end{bmatrix} = \begin{bmatrix} g_1 W_1 \\ g_2 W_2 \\ g_3 W_3 \\ \vdots \\ g_N z W_N \end{bmatrix} \quad (3.9)$$

or

$$M(z)V(z) = H(z) \quad (3.10)$$

To obtain the frequency response of the network at a frequency ω_0 , we set $z = e^{j\omega_0 T}$. For the case of the transfer function of the network with sampled and held inputs, the right hand vector is replaced by:

$$H_{SH}(e^{j\omega_0 T}) = [g_1 g_2 e^{j\omega_0 \sigma_1} \quad g_3 e^{j\omega_0 \sigma_2} \quad \dots \quad g_N e^{j\omega_0 \sigma_{N-1}}]^T \quad (3.11)$$

where σ_i is the time from the start of the period to the beginning of the i^{th} phase.

3.4 Solution of the Discrete System

Preprocessing can be carried out on the system of equations by performing block Gaussian elimination as was done in [37]. In the present case we obtain:

$$(zI - E)V_N(z) = \sum_{k=1}^N g_k^p W_k \quad (3.12)$$

where

$$E = C_N C_{N-1} \dots C_2 C_1 \quad (3.13)$$

$$g_k^p = C_N C_{N-1} \dots C_{k+1} g_k; \quad 1 \leq k \leq N-1 \quad (3.14)$$

and

$$g_k^p = g_N; \quad k = N \quad (3.15)$$

The superscript p stands for preprocessed. The matrix E and the vectors g_k^p are frequency independent and are computed only once, prior to point by point frequency analysis. Solving 3.12 by Gaussian elimination or some other technique determines $V_N(z)$. The solutions for $V_k(z)$ for $1 \leq k \leq N-1$ are obtained from equation 3.5, solving first for $V_1(z)$, then $V_2(z)$, and so on. Finally, the transfer function of the discrete system is obtained:

$$T_D = \frac{1}{N} \sum_{k=1}^N V_k \quad (3.16)$$

3.5 Determination of the B_k and g_k Coefficients

The formulation of the discrete system of equations and the frequency domain solution have been discussed without considering how to generate the coefficients of the B_k matrices, and g_k vectors. In the example these were determined analytically, since only first order differential equations were involved. In general, on a given phase, a system of high-order differential equations must be solved. In order to handle arbitrary networks, a transient analysis technique is used, to generate the coefficients automatically.

The system of equations in 3.1 relates the final value of node voltages at the end of an elapsed phase to the capacitor branch voltages at the start of the phase, and to the sampled and held input voltage. Thus the i^{th} column of B_k is the final set of node voltages for the k^{th} subnetwork on the k^{th} phase resulting from an initial condition of one volt applied to the i^{th} capacitor. The g_k vector is similarly the set of node voltages of the k^{th} subnetwork after application of a unit voltage by the input signal source.

In order to construct the B_k matrices and g_k vectors, a sequence of transient response calculations are performed on each of the N subnetworks. The B_k matrices contain the same number of columns as there are capacitors in the network. Each column is the ordered set of node voltages that result from a transient analysis of a duration equaling the length of the k^{th} phase. Each transient response is started with an initial condition of unity on one, and only one, of the capacitors. Therefore a system of N phases and K capacitors requires NK transient solutions to determine all the coefficients for the B_k matrices. A further N transients are required to generate the g_k vector coefficients.

3.6 A Computer Program for Analyzing Nonideal SC Networks

As remarked earlier, the formulation outlined above has been incorporated into a computer program called NISCAP, an acronym for Nonideal Switched-Capacitor Analysis Program. Currently this program handles the case of two-phase networks only, but can be extended to the case of multi-phases, since the formulation is in a generalized form. The switches are eliminated and the network assumes a different

topological form on each phase as shown in the example of Fig. 3.2: these are called the compact subnetworks. In order to generate the B_k matrices and the g_k vectors, the program carries out transient solutions on the compact subnetworks.

The modified nodal analysis (MNA) formulation is used in the process of running the transient analysis on the compact subnetworks. This was chosen for convenience; other formulations such as the sparse tableau, or the two graph method [18], will serve equally well. The backward Euler formula is used for the numerical integration in the transient response calculations, with a fixed step size. The *companion model* representation for a capacitor, that is used with the backward Euler formula, is shown in Fig. 3.3. This circuit is substituted for every capacitor in the MNA formulation to facilitate time domain transient analysis. Other stiffly stable integration formulas will also work such as the trapezoidal formula, or Gears backward differential formulae. The central point is the use of transient analysis to generate coefficients for matrices and vectors that are subsequently used to calculate the frequency response of a network. The choice of subnetwork formulation and integration method is one of convenience.

3.7 Numerical Efficiency of the Analysis Technique

In order to estimate the computational efficiency of this method only the number of real multiplications need be considered, since this is typically dominant in numerical analysis. A total of $N(K+1)$ transient analyses are performed during preprocessing, where N is the number of phases and K is the number of capacitors. These are analyses of the N different compact subnetworks for $(K+1)$ different sets

Fig. 3.3 Companion model representation of a capacitor for the backwards Euler integration algorithm.

Fig. 3.4 Model of a first-order transconductance amplifier.

of initial conditions. Thus only N triangular decompositions (LU decompositions) are needed, one for each of the subnetworks. The $K+1$ transient analyses are performed by updating the right-hand side vector and performing forward and backward substitution on the lower and upper triangular matrices that result from the decomposition process. For the Crout triangular decomposition algorithm [72], approximately $M^3/3$ multiplications are performed for a square matrix of dimension M . Forward and backward substitution require a further M^2 multiplications. In the present case M is the average dimension of the MNA matrices associated with the compact subnetworks. This dimension is larger than the number of compacted nodes by an amount equaling the number of connected dependent and independent ideal voltage sources. However, voltage controlled current sources are more typical for op amp macro-modeling so, for simplicity, the order M of the MNA matrices is assumed equal to the number of nodes.

The computation required for preprocessing therefore involves

$$P_p \cong N \left(\frac{M^3}{3} \right) + N(K+1)T M^2$$

multiplications where T is the number of timesteps used in each transient analysis. The first term applies to the triangular decomposition: it is usually small by comparison with the time consumed by the many forward and backward substitutions (second term).

The frequency domain processing requires the solution of Eq. (3.12) for $z = e^{j\omega T}$ for each desired frequency point. Since the $(zI - E)$ matrix varies with frequency,

Gaussian elimination or LU decomposition must be performed at each frequency of analysis. This computation is dominant over any additional forward and backward substitution. Thus frequency processing requires

$$P_f \cong 4F \left(\frac{M^3}{3} \right)$$

multiplications, where F is the number of frequency points being analyzed. Since these are complex matrices and vectors, complex multiplications are used. This results in the additional factor of 4 to convert to the equivalent number of real operations.

Example

In order to illustrate typical computational requirements, consider a nonideal SC network with:

$N = 2$	phases
$K = 16$	capacitors
$M = 20$	nodes (in the compact subnetwork)
$T = 100$	timesteps
$F = 100$	frequency points

Preprocessing	$P_p \cong 1.3$	million multiplications
Frequency processing	$P_f \cong 1.1$	million multiplications
Total processing	$P_t \cong 2.4$	million multiplications

This example shows the frequency processing to be roughly as time consuming as the preprocessing. The frequency processing represents the absolute minimum of computational steps required to solve a network of a given number of nodes. For example, an ideal SC network requires at least this amount of computation. Thus for the price of a doubling in computation time a nonideal analysis can be obtained.

3.8 High-Frequency Application Example

The analysis technique is applied here to the example of a second-order switched-capacitor bandpass filter for demonstration. Specifically, we use the computer program to show the effect of finite op-amp gain-bandwidth product and nonzero switch resistance on the filter of Fig. 3.5. This circuit is designed for a nominal passband gain of 8 dB, a quality factor (Q) of 18 and a center frequency of 864 KHz when clocked at 10 MHz. In this example the number of nodes is reduced from fifteen, to nine during phase one, and to eight during phase two, through the use of the switch-elimination technique.

For purposes of these analyses a first order transconductance amplifier was used to model the op-amps as shown in Fig. 3.4. This model approximates closely the behavior of op-amps typically used in high frequency filters [20]. A transconductance op-amp has a high output impedance, often several $M\Omega$ in value.

Fig. 3.5 Nonideal switched-capacitor bandpass filter.

It is compensated by a low frequency dominant pole formed by the charging of a load capacitor through the output impedance. The radian frequency of the dominant pole in the first order model is $\omega_{pd} = 1/(R_o C_L)$, the DC gain is $A_o = g_m R_o$, and the gain-bandwidth product (GBW) is $\omega_T = g_m / C_L$. In a switched capacitor network the capacitive loading on the op-amps, and hence their gain-bandwidth products and settling times, vary from phase to phase. This transient-based analysis technique automatically includes all of these factors.

The effect of variation of op amp gain-bandwidth product on filter frequency response is shown in Fig. 3.6. In this case, the op amp DC gain was held constant at 3000, and the GBW is varied from 10 to 30 MHz. Figure 3.7 shows the effect on the frequency response as the switch resistance is varied between 0 and 10 k Ω ; ideal op amps are used in this example. Finally, in Fig. 3.8, the combined effect of GBW and switch resistance on frequency response is shown. In this example a fixed 5 k Ω switch resistance is used, and the op-amp GBW is varied from 10 to 30 MHz, with a constant gain of 3000. From these simulations it is evident that the resonant frequency drops with either lowered GBW or increased switch resistance. Severe Q enhancement is also demonstrated with increased switch resistance.

3.9 Conclusion

A formulation of equations for the computer-aided analysis of nonideal SC networks has been presented that is of use for the design of high frequency SC filters. In order to greatly simplify the problem, only the discrete time system is dealt with; however, this suffices in most practical circuit applications. An efficient

Fig. 3.6 Effect of op-amp bandwidth on the SC bandpass filter

Fig. 3.7 Effect of switch resistance on the SC bandpass filter.

Fig. 3.8 Combined effect of op amp bandwidth and switch resistance on the SC bandpass filter.

algorithm for the frequency response of multi-phase networks is developed, and it is implemented in a computer program. In the algorithm matrices required for frequency response calculations can be generated through a sequence of time domain transient analyses; this allows the use of efficient time domain methods that are already available. A network compaction method is also used, to reduce the number of nodes that are analyzed. Additionally, extensive frequency independent preprocessing of many vectors and matrices is incorporated in the algorithm, to further increase efficiency. As an example of the technique, a high frequency SC bandpass filter is analyzed.

CHAPTER 4. OP AMP DESIGN FOR-HIGH FREQUENCY CIRCUITS

4.1 Introduction

The ability to design monolithic filters with specifications determined solely by capacitor ratios is crucial in the SC approach for voice-band applications. To achieve this, op amp integrators within an SC filter must completely transfer charge according to a capacitor ratio within a clock phase. The settling time in this configuration depends significantly on the bandwidth and slew rate of the amplifier. Shorter clock periods and increased signal frequencies necessitate the development of fast op amps for HF applications. Hence, op amp performance is central to high frequency switched capacitor circuit design.

Present amplifiers with gains of 1000-3000 and gain-bandwidth-products (GBW) of 1-3 MHz are adequate for voice band-filtering. On the other hand recent HF applications require passbands on the order of 500 KHz with clock frequencies of 4 MHz. To achieve this op amps must reach GBW of 50-80 MHz and slew rates of 50-100 volts/usec. The increase in these parameters is on the order of fifty: clearly, attaining HF performance demands a radically different design approach.

Determining amplifier specifications precisely is a nontrivial problem. Circuit speed is pushed to the limit with HF applications, prohibiting the convenience of overdesigning. Instead, the circuit analysis CAD techniques described in Chapter 3 or the analytic models in Chapter 6, [42-44] which include amplifier dynamics, should be used to establish minimum requirements.

Although wide bandwidth is critical for the application, power dissipation and noise performance are also important. In Chapter 2 it was shown that these goals are at-odds with each other. High speed operation is fundamentally achieved at the expense of power dissipation. To circumvent this, short-channel design must be employed, which degrades $1/f$ noise performance. These factors must be traded off to conform to overall system specifications.

In this chapter, the details of several high performance amplifiers are presented. These amplifiers all have high impedance cascoded output stages and are compensated by their output loading. This amplifier approach is mandatory for high-frequency circuits. A cascoded output amplifier has the benefits of the lowest power dissipation for a given bandwidth and the highest frequency for the nondominant pole; this is explained in Section 4.1.

The op amps described here are distinguished by whether they have single-ended or differential (balanced or complementary) outputs. The differential amplifiers are very important in high-frequency filters due to their inherently superior rejection of power-supply noise, and the requirement for them in fully differential filters.

4.2 A Frequency Compensation Approach for Wide-Band Op Amps

With high-frequency circuits, a frequency compensation approach that minimizes power dissipation is needed. In this section, a new approach towards achieving this objective is proposed. The new procedure is shown to be vastly superior to the voice-band pole-splitting concept in achieving both low dissipation and wide

bandwidth.

Specifically, a problem arises when the voice-band approach is applied to HF applications. The output pole must be at an extremely high frequency to meet stability constraints. In order to achieve this, large W/L ratios and current bias levels are required in the output stage, along with a pole-splitting capacitor as shown in Fig. 2.4. The excessive bandwidth requirement on the stage results in exorbitant current bias levels that are far in excess of those required for slew-rate considerations.

An alternate approach is now presented; it has also been arrived at independently by others [21]. The new method is to use a high impedance output stage to form, along with the load capacitor, a low frequency dominant pole. The internal pole is now required to be at high frequency; ~~no additional~~ compensation capacitor is necessary. The advantages are twofold. First, parasitic poles that previously depended on the loading of the output by the relatively large circuit capacitors now depend on much smaller parasitic capacitors that load low impedance nodes inside the op amp. Therefore the parasitic poles are at much higher frequency, and the gain-bandwidth product can be made higher without compromising closed-loop stability. Secondly, only the capacitors in the filter load the op amp; there is no additional internal compensation capacitor to charge and discharge. Thus lower power consumption is achieved.

Consider the two circuit alternatives as depicted in Fig. 4.1. The first circuit is representative of the conventional circuit: a cascade of two common-source gain

Fig. 4.1 Two approaches to high gain CMOS amplifier design. (a) Cascade of two common-source stages (b) Cascode stage.

stages. The second is a cascode stage of identical gain but with a high output impedance. In order to assess their respective suitabilities for HF performance, the ratio of the parasitic high-frequency pole to the gain bandwidth product is used as a figure of merit. When a second-order system with two real poles is compensated with a dominant low-frequency pole, a phase shift of ninety degrees is introduced by the lower pole well before the unity-gain frequency. Thus the phase margin is determined by the location of the higher frequency pole. If, for example, it is located at the unity gain frequency, then a further forty-five degrees phase shift is introduced, and the phase margin will also be forty-five degrees. To increase the phase margin beyond this amount, the second pole must be placed higher than the unity-gain frequency. A large value for the ratio of the high frequency pole to the unity gain frequency corresponds to high phase margin and therefore closed-loop stability. The circuit that excels in this regard is superior for high-frequency applications.

The following table compares the cascade with the cascode. The cascade is not stable in closed-loop due to the proximity of its two poles. To overcome this, a pole-splitting compensation approach is usually adopted by including a Miller capacitor from the drain to the gate of M_2 . This variation on the cascade is representative of typical voiceband op amps and is included in the table. Reference [9] outlines the derivation of table entries for the cascade and compensated cascade circuits. The analysis of the cascode circuit is summarized in Appendix D.

	CIRCUIT		
	CASCADE	COMPENSATED CASCADE	CASCODE
GAIN	A_0	A_0	A_0
ω_{pl}	$1/(r_{02}C_L)$	$1/(A_2r_{01}C_C)$	$1/(A_2r_{01}C_L)$
ω_{ph}	$1/(r_{01}C_G)$	g_{m2}/C_L	g_{m2}/C_P
ω_T	g_{m1}/C_L	g_{m1}/C_C	g_{m1}/C_L
ω_{ph}/ω_T	$(C_L/C_G)(1/A_1)$	$(C_C/C_L)(g_{m2}/g_{m1})$	$(C_L/C_P)(g_{m2}/g_{m1})$

Table 4.1 Bandwidth Comparison of Cascade and Cascode Circuits

$$A_0 = g_{m1}g_{m2}r_{01}r_{02} = A_1A_2; A_1 = g_{m1}r_{01}; A_2 = g_{m2}r_{02}.$$

ω_{pl} = low frequency pole; ω_{ph} = high-frequency pole; ω_T = gain-bandwidth product.

C_G = gate capacitance of M_2 ; C_P = the stray capacitance on the source of M_2 , consisting of the intrinsic capacitance of M_2 plus the overlap and junction capacitances.

All three circuits have identical DC gain but differ considerably in regard to pole placement. The uncompensated cascade has its two poles too close together to be stable in closed loop, whereas the other can be stable. For this reason consideration

will be restricted to the compensated cascade and the cascode. A comparison of the ω_{ph}/ω_T ratios favors the cascode by a margin of $C_L^2/(C_C C_P)$. Usually for the cascade, C_C and C_L are close in size so that the margin is roughly C_L/C_P . For typical amplifiers driving typical loads the ratio is on the order of five to twenty, greatly favoring the cascode circuit.

With this wide margin of relative pole locations the cascode can be made wide-band and stable by a suitably low choice of load capacitance. The present chapter applies these design considerations in the design of several high performance wide-band amplifiers.

4.3 Transconductance Amplifiers

The cascoded output op amps discussed in this chapter are adequately modelled in many cases by simple transconductance amplifiers. Transconductance amplifiers have high output impedances, as do cascoded output op amps, and display a first-order dominant pole when loaded by a shunt capacitance. In this section the analysis of a simple transconductance amplifier is presented to permit analogies with real amplifiers.

A simple first-order transconductance amplifier is shown in Fig. 4.2. Simple analysis shows its frequency response to be

$$A(s) = \frac{g_m R_o}{1 + R_o C_L s} = \frac{A_o \omega_{pd}}{s + \omega_{pd}} \quad (4.1)$$

where $A_o = g_m R_o$ is the DC open-loop gain and $\omega_{pd} = 1/R_o C_L$ is the open-loop 3 dB

2

MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS
STANDARD REFERENCE MATERIAL 1010a
(ANSI and ISO TEST CHART No. 2)

Fig. 4.2 First-order transconductance amplifier.

bandwidth (pole frequency). The amplifier's unity-gain bandwidth (ω_T) or gain-bandwidth product (GBW) is

$$\omega_T = \omega_{pd} \sqrt{A_o^2 - 1} \approx \omega_{pd} A_o = g_m / C_L; \quad A_o \gg 1 \quad (4.2)$$

The DC gain, open-loop bandwidth and gain-bandwidth products are important parameters for any op amp. A cascoded output op amp generally has a DC gain which equals the product of its short-circuit transconductance (g_{msc}) and its open-circuit output impedance. The short-circuit transconductance is the transconductance of an amplifier operating into a short-circuit load. This is typically the transconductance of the input stages increased or decreased by the current gain or loss in the circuitry coupling the input and output stages. The frequency response of a real cascoded output op amp differs from the simple model due to the presence of internal parasitic poles. These result from capacitive loading on nodes in the signal path of an amplifier. In general, each gain stage in an op amp contributes a pole. Single-stage cascode amplifiers also have parasitic poles as described in Section 4.1; however, these are usually at high frequencies.

In order to compensate an op amp, the pole formed by the output driving a capacitive load must be several orders of magnitude lower in frequency than any parasitic poles. Therefore the transconductance amplifier model accurately describes the location of the open-loop bandwidth of a cascoded output op amp at $\omega_{pd} = 1/R_o C_L$. The unity-gain bandwidth of an actual op amp is also often well approximated by the transconductance model of $\omega_T = g_{msc} / C_L$. However, the

accuracy of this approximation varies with the proximity of parasitic poles to the amplifier unity-gain bandwidth. The approximation is good if the poles are considerably above this frequency, and it becomes progressively poorer for lower frequency poles at or below the unity-gain bandwidth.

In the remainder of this chapter the approximate relationships described by the transconductance model will be used with the understanding that the unity-gain bandwidth and phase margin will differ somewhat from this.

4.4 Overview of the High Frequency Op Amp Design Approach

The conventional approach towards op amp design is to use a cascade of two moderate voltage gain stages to achieve a high overall gain; in this context the voltage levels within the amplifier represent the signal. A different design approach is employed here [20], [23], however, to maximize bandwidth. Instead of voltage, current is chosen to represent the signal and the design objective is to achieve a voltage controlled current amplification [28] (operational transconductance amplifier, OTA).

Using current rather than voltage to represent a signal minimizes the internal voltage swings of the amplifier. If, in fact, the voltage changes are held to zero and current coupling is exclusively achieved, then parasitic poles depend on L/R rather than RC time constants. The associated R/L poles are at extremely high frequencies, owing to low inductance in the coupling path.

Complete freedom from internal voltage swings is impossible, but the current

coupled approach does minimize them. High voltage gain is achieved almost entirely at the output, if the amplifier has high output impedance (which is the case with a current source output). The voltage gain is simply the product of the first stage transconductance, the current gain and the output impedance.

The preceding considerations are applied herein to the design of several high-frequency op amps. The voltage input is converted immediately into a current signal and thereafter is directed to the output; it provides a short-circuit output current that is proportional to input voltage. Two classes of op amps that implement this design approach are the current mirror amplifier and the current steering or folded cascode amplifier. High output impedance is required to achieve high voltage gain, and is obtained in both cases through the use of cascoded output stages.

The two classes of operational transconductance amplifiers are distinguished by their methods of current coupling between input and output stages. The current steering approach is shown in Fig. 4.3(a) and the current mirror op amp technique is shown in Fig. 4.3(b). The current steering amplifier is limited in short-circuit transconductance to half the transconductance of its input stage transistors. In order to achieve high bandwidth with this circuit, the input differential pair must be biased at very high current levels and must also be implemented with a large aspect ratio to give it a large transconductance.

In contrast, the current mirror approach has the advantage of allowing current gain in the current mirror which allows the short-circuit transconductance to be

Fig. 4.3 Cascode op amp approaches. (a) Current steering approach (b) Current mirroring approach.

made arbitrarily large for a given transconductance of the input source-coupled pair. This allows the unity-gain bandwidth of such an amplifier to be made arbitrarily high. Open-loop DC gain is not increased, however, since the linear increase in transconductance with current gain is balanced by a corresponding decrease in output impedance to maintain a constant $g_{msc}R_o$ product.

In comparison of the two the principal advantage of current steering op amps is that their parasitic poles are approximately at the $\omega_T = g_m/C_G$ frequency of the cascode device. The parasitic pole of a current mirror op amp, however, is determined by the bandwidth of the current mirror $\omega_p = g_m/(n+1)C_G$ and is usually lower and decreases with the current gain n . For the case of $n = 1$, the current mirror parasitic pole is at approximately one half the frequency of the current steering amplifier's parasitic pole. This comparison is summarized in Table 4.2.

Op amps employing both of these circuit approaches have been implemented and tested and are described in the following sections. Both approaches have been explored since they each have strengths and weaknesses that determine which is more appropriate for a specific application. Differential and single-ended versions of both types of amplifier were implemented to cover the high-frequency op amp design problem thoroughly.

	Current Steering	Current Mirror
Gain	$g_{m1}R_0$	$g_{m1}R_0$
GBW	$\frac{g_{m1}}{C_L}$	$n \frac{g_{m1}}{C_L}$
Slew Rate	$\frac{I_B}{C_L}$	$n \frac{I_B}{C_L}$
Parasitic Pole	$\frac{g_{m2}}{C_G}$	$\frac{g_{m3}}{(n+1)C_G}$

Table 4.2 Comparison of current mirror and current steering op amps

4.5 Differential Op Amps and Common-Mode Feedback

The merits of differential SC circuitry, particularly in overcoming op amp and clock-feedthrough induced power-supply transmission, are described in Chapter 6. The adoption of this approach necessitates the design of differential op amps for use as components in SC circuits. The schematic symbol used for a differential amplifier is shown in Fig. 4.4.

The difference between single-ended and differential amplifiers is the use of complementary rather than single-ended outputs. With the differential op amp the output is taken as the difference of the two outputs $V_o = (V_{o+}) - (V_{o-})$. This has the benefit of excluding any common-mode input level or power-supply induced signal.

Fig. 4.4 Schematic symbol for a differential output op amp.

With single-ended circuits biasing is simple: the noninverting input is connected to the desired bias level, typically analog ground. Employing a balanced amplifier in a fully differential circuit prohibits this convenience. The noninverting input is connected to circuit elements symmetric with those on the opposite side and the ability to connect to a reference voltage is lost. An example illustrating the biasing virtues of a single-ended circuit appears in Fig. 4.5(a). The unity-gain follower is biased with its output equal to the reference level.

The differential version of the follower, shown in Fig. 4.5(b), self-biases to some arbitrary level, since it lacks an input for a reference level. In order to achieve maximal signal range a biasing method is needed which ensures that the output equals a reference level in the absence of signal. We are specifically concerned with integrator based circuits that preclude the use of any reference input. The approach adopted here involves the use of a common-mode biasing loop. In order to implement this, additional circuitry is required: first an additional input that controls the output common-mode level is needed; second, a circuit is needed to average the two output voltages to produce the common-mode level.

With this circuitry, a differential op amp can be biased as shown in Fig. 4.6. In the figure a differential input signal drives the common-mode amplifier, which controls the output common-mode voltage with a gain of A_{CM} . By the connection of the noninverting input to V_{REF} and the output common-mode level (as determined by the averager) to the inverting input, the output common-mode voltage is held at V_{REF} by the loop gain of the circuit. This is analogous to the manner in which

(a)

(b)

$$V_O = (V_{O+}) - (V_{O-}) = 0$$

$$V_{OCM} = [(V_{O+}) + (V_{O-})] / 2 = ?$$

= some arbitrary self-bias level

Fig. 4.5

Biassing problem associated with differential signal paths. (a) Single-ended circuit with a well defined bias (b) Differential circuit with an arbitrary bias.

Fig. 4.6 Biasing the output of a differential output op amp through the use of a common-mode feedback loop.

the single-ended op amp of Fig. 4.3(a) is biased except that the feedback signal is the output common-mode voltage. This approach is capable of achieving an output common-mode level of:

$$V_{oCM} = V_{REF}(A_{CMd} + A_{CMcm}/2)/(1 + A_{CMd} - A_{CMcm}/2) + |V_{osCM}| \quad (4.3)$$

where A_{CMd} is the differential gain of the common-mode amplifier, A_{CMcm} is the common-mode gain of the common-mode amplifier, and V_{osCM} is the input-referred offset of the common-mode amplifier.

Both continuous and SC sampled data approaches have been reported in the literature [13,26]. The current design implements the continuous feedback approach with minimal additional circuitry.

4.6 Current Steering Op Amps

The basic current steering or folded cascode amplifier circuit that is shown in Fig. 4.7 was developed at the Univ. of California, Berkeley [20],[21]. The op amp as shown is completely symmetrical and hence has complementary outputs. However, the circuit needs additional common-mode feedback circuitry to be usable as a differential amplifier or, alternatively, a single-ended to differential converter for single-ended application. In this section, the design, implementation and testing of both single-ended and differential current steering amplifiers are presented [60]. These amplifiers have been realized in the 1.25 micron CMOS process developed at the General Electric Co.

Fig. 4.7 Differential current-steering op amp.

Analysis of current steering op amps

A simplified small-signal model for the differential current steering op amp is shown in Fig. 4.8. This circuit has been analyzed previously [51], however, the analysis is included here for generality and to clarify some details. The single-ended DC gain is

$$A_v = \left(\frac{1}{2} \right) \cdot \frac{g_{m1}(G_{m2} + g_{o2})}{g_{o2}G_{o1} + (G_{m2} + g_{o2} + G_{o1})G_{o2}} \quad (4.4)$$

where the subscripts for the g_m 's and g_o 's refer to the transistor numbering in Fig. 4.7,

$$G_{m2} = g_{m2} + g_{mb2}$$

g_{mb2} = the substrate transconductance of the P channel cascode transistor.

$$G_{o1} = g_{o1} + g_{o5}$$

and G_{o2} is the conductance of N channel cascoded current source formed by M_3 and M_4 . From Appendix D

$$G_{o2} = \frac{g_{o3} g_{o4}}{G_{m3} + g_{o3} + g_{o4}} \quad (4.5)$$

and $G_{m3} = g_{m3} + g_{mb3}$. To maximize linearity and reduce distortion, the circuit should be relatively symmetric with regard to matching transconductance and conductance of the N and P cascodes, and the conductance of current source transistors M_4 and M_5 . This symmetry matches the small-signal impedance seen looking up into the drain of M_2 with that seen looking down into the drain of M_3 .

Fig. 4.8 Small-signal model of a current steering op amp.

In this circumstance the DC gain is

$$A_o = \frac{1}{2} \frac{g_{m1}(G_{m2} + g_{o2})}{2g_{o2}G_{o1}} \quad (4.6)$$

where

$$G_{m2} = G_{m3}$$

$$g_{o2} = g_{o3}$$

$$g_{o1} + g_{o5} = g_{o4}$$

This is comparable to the gain obtainable from a cascade of two common-source amplifiers. The factor of one half results from the absence of a differential to single-ended converter.

The other parameters for the simple transconductance amplifier model are: output resistance

$$R_o = \frac{G_{m2} + g_{o2} + G_{o1}}{g_{o2}G_{o1} + (G_{m2} + g_{o2} + G_{o1})G_{o2}} \quad (4.7)$$

and short-circuit transconductance

$$g_{msc} = \frac{1}{2} g_{m1} \left(\frac{G_{m2} + g_{o2}}{G_{m2} + g_{o2} + G_{o1}} \right) \quad (4.8)$$

The amplifier is compensated by a low-frequency dominant pole formed by the charging of the load capacitance through the output resistance of the amplifier.

$$\omega_{pd} = \frac{1}{R_o C_L} \left[\frac{g_{o2}G_{o1} + (G_{m2} + g_{o2} + G_{o1})G_{o2}}{G_{m2} + g_{o2} + G_{o1}} \right] \frac{1}{C_L} \quad (4.9)$$

A parasitic pole is formed by the charging of stray capacitance at the source of the cascode transistor M_2 . The admittance at this node is $Y_p = Y_{s2} + G_{o1}$ where Y_{s2} is the admittance looking into the source of the cascode transistor. From Appendix D,

$$Y_{s2} = (G_{m1} + g_{o2}) \left(\frac{Y_{o2}}{Y_{o2} + g_{o2}} \right) \quad (4.10)$$

where $Y_{o2} = G_{o2} + sC_L$ is the admittance of the N channel cascoded current source shunted by the load capacitance C_L . Since the poles are assumed widely spaced, i.e. $\omega_{pd} \ll \omega_p$ at the frequency of the parasitic pole, the admittance of the source is

$$Y_{s2} \approx (G_{m2} + g_{o2}) \left(\frac{sC_L}{sC_L + g_{o2}} \right) \quad (4.11)$$

but $\omega C_L \gg g_{o2}$ at high-frequency and

$$Y_{s2} \approx G_{s2} \approx G_{m2} + g_{o2}$$

$$Y_p \approx G_p \approx G_{m2} + g_{o2} + G_{o1}$$

and the parasitic pole is at a frequency.

$$\omega_{pH} \approx \frac{G_{m2} + g_{o2} + G_{o1}}{C_p} \approx \frac{G_{m2}}{C_p} \quad (4.12)$$

The parasitic capacitance consists of the gate-source capacitance of cascode transistor M_2 , along with the junction capacitance of its source, and drains of current source M_3 and input device M_1 . Increasing the width of M_2 to increase its transconductance also increases C_p so the frequency of the parasitic pole depends on the f_T of the process. When the junction capacitances are included, the parasitic

pole frequency can be less than half the f_T of the cascode transistor.

Single-ended current steering op amp

An implementation of the single-ended current steering op amp is shown in Fig. 4.9. This uses a zero-systematic offset current mirror that was originally presented in ref. [59] to perform differential to single-ended conversion. This is implemented here by transistors $M_{12} - M_{15}$, which control the gate voltage of current sources M_{10} and M_{11} in a feedback loop. The feedback forces the inverting op amp output at the gate of M_{12} to equal analog ground at the gate M_{15} . Systematic offset is eliminated by this approach since, by symmetry, the actual output will be forced to zero, even with systematic variations in process parameters, etc.

An additional benefit to the circuit is that no connection is required to the common diffusion between the source of M_8 and the drain of M_{10} (similarly for M_9 and M_{11}). This allows minimum polysilicon gate spacing to be used here; this minimizes the area of the junction capacitance on this node and improves the bandwidth of the N channel differential to single-ended converter.

The bias circuit that generates the four reference levels required for the op amp. is shown in Fig. 4.10. This implements the high-swing cascode biasing described in ref. [20] where the op amp output can swing within two V_{DSSAT} of either rail; where $V_{DSSAT} = V_{GS} - V_T$ for the bias current of the output stage. This particular implementation of a high-swing cascode bias circuit is operable with relatively low

Fig. 4.9 Single-ended current steering op amp with zero-systematic offset.

supply voltages. This enables the op amp to work normally with only ± 1.5 volt supplies, making battery operation feasible.

Test results for the single-ended current steering op amp

Output voltage swing is shown in Fig. 4.11 for closed-loop voltage-follower operation at ± 3 volts. The negative clipping reflects the common-mode input range limitation and prevents closed-loop testing of the lower output range in unity-gain voltage-follower mode. The positive cycle clips at about 200 mv. from the positive rail in both closed-loop photographs. Open-loop operation is shown in Fig. 4.12 for $\pm 3V$ supplies. Here it is evident that the output during the negative half-cycle has an even wider swing capability than it does in the positive direction. This is consistent with a lower V_{ON} for N channel versus P channel transistors.

The following test data is for operation with ± 3 volt supplies and a bias current of $250 \mu A$. The small-signal frequency response is shown in Fig. 4.13 for a capacitive load of $0.75 pF$. The DC gain of the op amp is 68.5 dB, and the gain-bandwidth product is 62 MHz. At a $500 \mu A$ current level the bandwidth increases to 91 MHz as shown in Fig. 4.14. The small-signal step response for the op amp is shown in Fig. 4.15, and 4.16 for a $250 \mu A$ bias current and a $0.75 pF$ capacitive load. In Fig. 4.15 a 50 ns. pulse is applied to the closed loop op amp whereas in Fig. 4.16, a 20 ns. pulse is applied. The op amp is sufficiently stable and has a settling time on the order of 20 ns. Large signal open-loop response is shown in Fig. 4.17. The slew rate is symmetrical and approximately $80 v/\mu s$

$$I_{DD} = 250 \mu A \quad C_L = 0.75 \text{ pF}$$

Fig. 4.11 Large signal closed loop response of current steering op amp.

Fig. 4.12 Open loop response of current steering op amp.

$$I_{DD} = 250 \mu A \quad C_L = 0.75 \text{ pF}$$

Fig. 4.13 Small signal frequency response at 250 μA for the current steering op amp.

$$I_{DD} = 500 \mu A \quad C_L = 0.75 \text{ pF}$$

Fig. 4.14 Small signal frequency response at 500 μA for the current steering op amp.

$$I_{DD} = 250 \mu A \quad C_L = 0.75 \text{ pF}$$

Fig. 4.15 Closed loop transient response for a 50 ns pulse for the current steering op amp.

$$I_{DD} = 250 \mu A \quad C_L = 0.75 \text{ pF}$$

Fig. 4.16 Closed loop transient response for a 20 ns pulse for the current steering op amp.

$$I_{DD} = 250 \mu A \quad C_L = 0.25 \text{ pF}$$

Fig. 4.17 Open loop large signal response for the current steering op amp.

The input-referred offset voltage averaged over 60 samples is -0.55 mV with a standard deviation of 3.0 mV. This very low average offset and the higher standard deviation validate the zero systematic offset circuit design. The data indicates that random offset, which corresponds to the standard deviation, is almost six times greater than systematic offset, which corresponds to the average offset.

The test results for the single-ended current steering op amp are summarized in Table 4.3.

Parameter	Condition	Units	Value
Gain		dB	69
GBW	$C_L = 0.75$ pF	MHz	62
Slew Rate	$C_L = 0.75$ pF	v/ μ sec	80
Offset	mean	mv	-0.55
Offset	std. dev.	mv	3.0
Noise	1 KHz	nv/ $\sqrt{\text{Hz}}$	160

$$V_{DD} = +3\text{v} \quad V_{SS} = -3\text{v} \quad I_{DD} = 250 \mu\text{A}$$

Table 4.3(a) Measured single-ended current steering op amp performance

I_{DD}	C_L	GBW
$250 \mu\text{A}$	0.75 pF	62 MHz
$500 \mu\text{A}$	0.75 pF	91 MHz

Table 4.3(b) Measured single-ended current steering op-amp bandwidth versus bias current.

Input referred noise measured using an HP8568A spectrum analyzer is tabulated in Table 4.4.

Frequency (Hz)	Input Referred Noise (nV/ $\sqrt{\text{Hz}}$)
100	850
500	298
1K	157
10K	124
100K	139
1M	932

Table 4.4 Input referred noise of the single-ended current steering op amp.

The data at 100 KHz and higher includes a substantial noise contribution from a buffer amplifier used in the measurement. The capacitance of external wiring connecting the buffer to the open-loop op amp reduced the bandwidth to below 1 MHz. At low frequency where the op amp gain is high the additional noise is negligible when referred to the input; at frequencies where this gain is low, however, the additional contribution can greatly exceed the op amp noise.

Fully-differential current steering op amp

A fully-differential current steering op amp is described next [20]. The op amp is shown in Fig. 4.18 and consists of a current steering differential amplifier and a common-mode feedback circuit. The differential amplifier here is identical to the one used in the single-ended op amp. Many performance specifications such as gain, output voltage range and common-mode input range are the same.

Fig. 4.18 Fully differential current steering op amp.

The common-mode circuit is a composite of two differential pairs ($M_{14} - M_{17}$) that are current summed into a single-current mirror load (M_{12} and M_{13}); a double differential pair was also used in reference [58]. The inputs to the common-mode circuit are the differential op amp outputs and the analog ground reference. The output of the current mirror drives the gate of the P channel current source transistors to jointly control the common-mode level of the differential outputs.

Each differential pair converts the difference between its respective output voltage and ground to a differential current. The addition of these currents yields a differential current approximately proportional to the sum of the two output voltages and ground. This senses the error in the common-mode output with respect to ground. The unity-gain feedback holds the common-mode level equal to the ground reference.

The large-signal operation of the common-mode circuit is explained as follows. The differential input voltage v_d applied at the input to a differential-pair increases the drain current by i_d on one side and decreases it by the same amount on the other, according to [9].

$$i_d = \beta v_d \sqrt{\frac{2I_B}{\beta} - v_d^2}; \quad |v_d| \leq \sqrt{\frac{2I_B}{\beta}} \quad (4.13)$$

where $\beta = \frac{\mu C_{ox}}{2} \left(\frac{W}{L} \right)$ and I_B is the bias current.

In this circuit there are two differential-pairs with differential input voltages

$$v_{d1} \triangleq v_{o1} - v_{cm}$$

$$v_{d2} \triangleq v_{o2} - v_{cm}$$

The differential output currents of the two pairs are summed in the circuit to give

$$i_{d1} + i_{d2} = \beta(v_{o1} - v_{cm}) \sqrt{\frac{2I}{\beta} - (v_{o1} - v_{cm})^2} + \beta(v_{o2} - v_{cm}) \sqrt{\frac{2I}{\beta} - (v_{o2} - v_{cm})^2} \quad (4.14)$$

This current equals zero only when the output common-mode voltage v_{ocm} equals the reference voltage v_{cm} , i.e.,

$$v_{ocm} = \frac{v_{o1} + v_{o2}}{2} = v_{cm} \quad (4.15)$$

Normally the reference is made equal to analog ground to maximize dynamic range. Even though the large signal behavior of the differential-pair is nonlinear as shown in Eq. 4.13, this circuit accurately controls the common-mode voltage for large differential output signals.

The loop-gain is quite high, on the order of $(g_m/g_o)^3$, the gain of a cascade of three common-source amplifiers. The common-mode amplifier has the gain of a single common-source amplifier and it drives a cascode amplifier which has a gain equivalent to the cascade of two common-source amplifiers. The differential pairs in the common-mode circuit must be able to handle large voltage swings at their inputs in order to keep the feedback loop closed for large output signals. If the signals are large enough such that one transistor in a pair is completely off, and the other passes the entire bias current, further increases in voltage will have no further

influence on differential currents. This effectively opens the feedback loop for very large output signals.

To maximize the input range of the differential-pairs, they are made long and narrow in accordance with the following equation [9].

$$|V_d| \leq \sqrt{\frac{2I_B}{\beta}} \quad (4.16)$$

Test results for the differential current steering op amp.

To illustrate the performance of the common-mode feedback design the circuit of Fig. 4.19(b) is used. The circuit generates buffered differential signals from a single-ended input signal; the output is shown in Fig. 4.19(a). The noninverting output follows the input signal as a normal voltage-follower, owing to the difference-mode feedback. The inverting output follows the input inversely due entirely to the internal common-mode feedback. This circuit handles signals up to 2.1 v_{pp} for a 250 μa bias current and up to 2.6 v_{pp} for a 500 μa current. The larger current extends the input range of the differential amplifiers in the common-mode circuit according to Eq. 4.16.

The input-referred difference-mode offset voltage is 1.4 mv with a standard deviation of 0.5 mV. The common-mode offset is -8.9 mv with a standard deviation of 11.7 mv. This is extremely low for the difference-mode offset and suggests that this circuit approach would be good for low offset single-ended amplifiers. The common-mode offset is not normally as low, and the levels here are very small by

DIFFERENTIAL OP AMP

Fig. 4.19 Single-ended to differential conversion using the differential current steering op amp. (a) Measured output (b) Test circuit.

conventional standards.

Unfortunately the differential current steering op amp is unstable in other configurations, traceable to an instability in the common-mode feedback loop. This is due to the use of three gain stages. Simulations show the circuit can be stabilized by using Miller feedback through the addition of capacitors between the gate of the P channel current sources, (M_4 and M_5), and the two outputs. Unfortunately, this adds capacitive loading to the output and reduces the difference-mode bandwidth.

An alternative compensation approach is to degenerate the gain of the common-mode loop by splitting the M_{12} , M_{13} current mirror, and connecting the gate to the drain of M_{12} . This provides stability but degrades the DC offset due to the reduction in loop gain. A variant on this approach is to use the novel AC coupled mirror shown in Fig. 4.20(a). This acts as a current mirror at low-frequency, providing high loop gain, and becomes effectively a pair of diode-connected loads at high-frequency, for stability. The practical implementation shown in Fig. 4.20(b) substitutes a MOS transistor for the resistor. Circuit simulations indicate adequate stability for both of these approaches. A photomicrograph showing the test circuit appears in Fig. 4.21. It shows from left to right: the bias circuit, two single-ended op amps, and two differential op amps. Closeup photomicrographs of the single-ended and differential op amps are shown in Figs. 4.22(a) and (b) respectively.

4.7 Current Mirror Op Amps

In this section the design and operation of a single-ended and a differential

Fig. 4.20 AC coupled current-mirror (a) simplified circuit (b) actual circuit.

Fig. 4.21 Op amp test structure.

Fig. 4.22 (a) Single-ended op amp and bias circuit (b) differential op amp.

current mirror amplifier are described. The circuits are also implemented in the 1.25 micron CMOS process developed by the General Electric Corporate Research and Development Laboratories and are used in the high-frequency switched capacitor filters described in Chapter 7. The principles of operation of the single-ended circuit can be readily deduced from the description of the differential amplifier which follows.

Credit goes to M. Milkovic of G. E. for the design of the single-ended current mirror op amp [22],[23]. Milkovic subsequently designed a fully differential version of the op amp. Earlier work by Copeland and Gillingham on transconductance amplifiers [25], uncovered bias stability problems in differential op amp implementations. Motivated by this problem, the author developed the common-mode bias circuit that was incorporated into Milkovic's differential op amp to make it workable.

A block diagram of the op amp is shown in Fig. 4.23. A conventional source-coupled pair converts a differential voltage input to a differential current proportional to their transconductance of $i = g_m v_i / 2$. Each drain of the source-coupled pair is connected to the reference side of a separate current mirror. Both mirrors have double outputs: one goes directly to an output node and the other crosses over to connect to a reference current input of a lower current mirror. On each side the op amp output is formed by the common connection of the upper and lower current mirror outputs. A current gain of n applies to these outputs with respect to their references. The upper and lower mirrors both contribute half of the

Fig. 4.23 Block diagram of the current mirror op amp.

total output current $i_o = n g_m V_i$.

With the mirror design the maximum output current is limited to $i_o = n I_B$ and the slew rate ($dv_o/dt = v'_{om}$) is consequently limited to

$$v'_{om} = n I_B / C_L. \quad (4.17)$$

The power dissipation is related to bias current as well:

$$P_D = (n + 2) I_B (V_{DD} - V_{SS}). \quad (4.18)$$

Finally, the slew rate is related to the power dissipation:

$$P_D = \left[\frac{n + 2}{n} \right] C_L (V_{DD} - V_{SS}) v'_{om}. \quad (4.19)$$

By using high current gain in the output mirrors (large n), the lowest power consumption attainable for a given slew rate is:

$$P_D = C_L (V_{DD} - V_{SS}) v'_{om}. \quad (4.20)$$

Low frequency model

The schematic of the amplifier with stacked current mirrors is shown in Fig. 4.24. In the following discussion the subscripts for the g_m 's and g_o 's refer to the transistor numbering in this figure. Short circuit current gain is very close to n for the stacked mirrors; with typical devices $n \times 0.9996$ is attained and the approximation $i_o/i_n = n$ is valid. The overall amplifier short-circuit transconductance then is

$$g_{msc} = n g_{m1} \quad (4.21)$$

The output conductance G_o is the sum of the conductances G_{oP} looking up into the P channel current mirror (drain of M_3) and G_{oN} looking down into the N channel current mirror (drain of M_1).

$$G_o = G_{oP} + G_{oN} \quad (4.22)$$

The equation for the output conductance of a cascode circuit is derived in appendix D; applying the result here gives:

$$G_o = \left(\frac{g_{o2}g_{o3}}{G_{m3} + g_{o2} + g_{o3}} \right) + \left(\frac{g_{o4}g_{o5}}{G_{m4} + g_{o4} + g_{o5}} \right) \quad (4.23)$$

where $G_m = g_m + g_{mb}$ and g_{mb} is the substrate transconductance of the cascode transistor. The output resistance is

$$R_o = \frac{1}{G_o} \cong \frac{G_{m3}G_{m4}}{g_{o2}g_{o3}G_{m4} + g_{o4}g_{o5}G_{m3}} \quad (4.24)$$

If the G_{oP} and G_{oN} conductances are matched with $G_{m3} = G_{m4}$, $g_{o2} = g_{o5}$ and $g_{o3} = g_{o4}$, linearity is enhanced, and the expression for output resistance becomes

$$R_o \cong \frac{1}{2} \frac{G_{m3}}{g_{o2}g_{o3}} \quad (4.25)$$

The single-ended open-loop voltage gain is simply the product of the short-circuit transconductance and the output resistance:

$$A_o \cong n g_{m1} \left(\frac{G_{m3}G_{m4}}{g_{o2}g_{o3}G_{m4} + g_{o4}g_{o5}G_{m3}} \right) \quad (4.26)$$

For the case of matched output conductances, the simplified expression for R_o in Eq. 4.25 is used

$$A_o \cong \frac{n}{2} \frac{g_{m1} G_{m3}}{g_{o2} g_{o3}} \quad (4.27)$$

This is comparable to the gain of a cascade of two common-source amplifiers increased by the factor "n". The 3 dB open-loop bandwidth is

$$\omega_{pd} = \frac{1}{R_o C_L} \cong 2 \frac{g_{o2} g_{o3}}{G_{m3} C_L} \quad (4.28)$$

Taking the product of Eqs. 4.27 and 4.28 gives the single-ended gain-bandwidth product

$$\omega_T = n g_{m1} / C_L \quad (4.29)$$

The differential-mode gain and bandwidth are double the amounts listed here.

High frequency model

Up until now, only low-frequency performance has been considered. The gain-bandwidth product expression of Eq. 4.29 is based on the single-pole transconductance model. This section describes the parasitic poles that degrade the high-frequency performance. It is assumed that the frequency limitation is due to the finite bandwidth of the stacked current mirrors in the amplifier. The stacked current mirror is analyzed in appendix E and is approximated by the transfer function

$$\frac{i_o(s)}{i_i(s)} \cong \frac{n}{s\tau_p + 1} \quad (4.30)$$

where $\tau_p = 1/\omega_p = (1/\omega_T)\sqrt{2(n+1)(2n+1)}$ and ω_T is the bandwidth of the I.C. technology (g_m/C_{GS}). This expression was derived under the following simplifying assumptions: junction capacitance is ignored, only MOSFET gate-source capacitance is considered; minimum channel lengths are used; the widths of the mirror transistors are matched such that $W_2 = W_3$, $W_4 = W_5$, $W_6 = W_7$, $W_8 = W_9$ and $W_{10} = W_{11}$; the widths of the output transistors in the current mirror are "n" times larger than those of the input transistors, i.e. $W_2 = nW_6$, $W_3 = nW_7$, $W_4 = nW_8$, and $W_5 = nW_9$.

The small signed output current is the sum of components from the two output mirrors; i_{oP} from the P channel mirror and i_{oN} from the N channel mirror.

$$i_o = i_{oP} + i_{oN} \quad (4.31)$$

The P and N channel mirrors have different time constants due to the different technological bandwidths of the minimum length P and N channel transistors; the mirror time constants are designated τ_P and τ_N , respectively. The output current i_{oP} goes only through one current mirror and has only one pole; the other current, i_{oN} , goes through two mirrors and has two poles. The output current is

$$\begin{aligned} \frac{i_o(s)}{i_i(s)} &= \frac{ng_{m1}}{2} \frac{1}{(s\tau_p + 1)} + \frac{ng_{m1}}{2} \frac{1}{(s\tau_p + 1)(s\tau_N + 1)} \\ &= ng_{m1} \frac{(s\tau_N/2 + 1)}{(s\tau_p + 1)(s\tau_N + 1)} \end{aligned} \quad (4.32)$$

To obtain the voltage gain this is multiplied by the output impedance.

$$A_v(s) = \frac{V_o(s)}{V_i(s)} = \frac{i(s)Z_o(s)}{V_i(s)} = ng_{m1}R_o \frac{(s\tau_N/2 + 1)}{(s\tau_{pd} + 1)(s\tau_P + 1)(s\tau_N + 1)} \quad (4.33)$$

where R_o is defined in Eqs. 4.24 and 4.25, and $\tau_{pd} = 1/\omega_{pd}$ and ω_{pd} is defined in Eq. 4.28.

From the equation for voltage gain, there is a low-frequency dominant pole due to the charging of the load capacitance by the high output impedance; a parasitic pole due to the finite bandwidth of the P channel mirror; and a parasitic pole-zero pair due to the finite bandwidth of the N channel mirror. The pole-zero pair partially cancel one another, since they are spaced one octave apart. In addition, the bandwidth of the N channel mirror is higher than that of the P channel mirror i.e. $\omega_n > \omega_p$. It is therefore reasonable to simplify the transfer function to a two pole expression if necessary.

$$A_v(s) \approx \frac{ng_{m1}R_o}{(s\tau_{pd} + 1)(s\tau_p + 1)} \quad (4.34)$$

Stacked current mirrors

The op amp design makes frequent use of current mirroring for interstage coupling. Current variations represent signal in the amplifier and the current mirrors direct proportionate currents to the outputs. Furthermore, compound mirrors such as the Wilson, the improved Wilson, the cascoded mirror, and the stacked mirror have cascode output stages. As mentioned earlier, the cascode is

required to achieve the high-output impedance necessary for high voltage gain and frequency compensation at the output.

A simple mirror, a cascoded mirror, and a stacked mirror are shown in Figs. 4.25(a), (b) and (c) respectively. The simple mirror has an output current greater than the reference current by an amount $g_{o2}(v_o - v_R)$, where g_o represents the nonzero output conductance of the MOSFET when operated in saturation. Through the use of a common-gate transistor in the cascoded mirror, the output conductance is reduced by the gain of a single device as shown in Appendix D. Here the gain of transistor M_3 decreases the output conductance so that $G_o = g_{o2}g_{o3}/(g_{m3} + g_{mb3})$ where g_{mb} represents the substrate transconductance of the device.

The stacked mirror shown in Fig. 4.25(c) also has high output impedance and does not require the cascode bias voltage. The output voltage at the drain of M_4 , however, cannot swing as close to the supply rail as the fixed bias cascode mirror. The stacked mirror can swing to within $V_T + V_{DSSAT}$ of the power rail where V_T is the threshold voltage and V_{DSSAT} is the minimum drain source voltage required for saturation; typically this is $V_{GS} - V_T$ where V_{GS} is the gate-source voltage. The fixed bias cascode, with a suitable bias voltage, can swing to within $2 V_{DSSAT}$ of the supply rail. The output conductance of the stacked mirror is the same as the cascoded mirror. The frequency response is analyzed in Appendix E.

With any mirror there is the option of acquiring current gain or attenuation.

Fig. 4.25 Current mirrors. (a) Simple mirror (b) Cascoded mirror (c) Stacked mirror.

The output current will be scaled according to the ratio of widths of lower devices, assuming they have equal channel lengths. In the preceding discussion of the op amp, current mirrors with gains of "n" were specified. This means the width of the device on the output side is "n" times larger than the diode connected device on the reference side. Another attribute of current mirrors is that the number of outputs need not be limited to one. Simply connecting additional devices in parallel with common gates realizes multiple outputs.

Common-mode feedback output biasing circuit

With differential op amps a circuit is needed to ensure that the output common-mode level is biased at an appropriate reference voltage. A simple method of imbalancing the N channel current mirrors is adopted as shown in Fig. 4.26. The four additional transistors $M_1 - M_4$ are all operating in the triode region. Two transistors M_1 and M_4 have their drains and sources in common and each gate is connected to one of the two op amp outputs. When operating in the linear region, this is equivalent to one device of double width with its gate connected to the average (common-mode) output voltage.

The other two devices, M_2 and M_3 , are completely in parallel with their drains at the bottom of the reference side of the two mirrors and their gates connected to the bias reference voltage. To simplify explanation of the operation, the circuit of Fig. 4.27, consisting of a single imbalanced mirror, is presented. The gate of M_2 is now driven by the output common-mode level to establish an equivalent circuit. This circuit is comparable to an op amp itself, with the gates of M_1 and M_2 forming

Fig. 4.26 Block diagram of the common-mode bias circuit.

Fig. 4.27. Simplified block diagram of the common-mode bias circuit.

the differential input. With the output connected to the inverting input (M_2), a unity-gain follower is attained. The noninverting input (M_1) controls the common-mode output and consequently is connected to the desired bias level.

For this circuit the output voltage is determined according to Eq. 4.3. To achieve proper biasing, adequate differential gain is required in the common-mode loop. This depends principally on achieving reasonable transconductance from the triodes. Since their transconductance increases directly with drain-source voltage a problem arises in simultaneously attaining a sufficient transconductance from the triode devices and full output voltage range. The output voltage is decreased by the voltage drop across the series triode device. A compromise can only be reached by trading off transconductance against voltage swing.

A complete schematic of the differential current mirror op amp appears in Fig. 4.28.

Single-ended current mirror op amp

The single-ended version of the current mirror op amp is shown in Fig. 4.29. It is identical to the differential op amp minus one output stage and its associated opposite current mirror, and the common-mode feedback circuit. Operation is identical to the differential amplifier. The P channel current mirrors have only single outputs now, and the capacitive loading is lower. This raises the frequency of the parasitic poles of the amplifier and improves the phase margin.

Otherwise performance is identical to the differential circuit; however, power

Fig. 4.28 Differential current-mirror op amp with the common-mode feedback circuit.

Fig. 4.29 Single-ended current-mirror op amp.

consumption is lower:

$$P_D = \frac{(n+3)}{2} I_B (V_{DD} - V_{SS}) \quad (4.35)$$

which is a 37.5% reduction for $n = 2$.

Test results

Test results for the current mirror op amp have already been published [22],[23] and are described here briefly. Typical results are summarized in Table 4.4 for the singled-ended op amp. Notable here is the achievement of a 70 MHz bandwidth, a 100 v/uses. slew rate and 60 dB of gain with only a 135 μ A bias current; the differential amplifier uses a 215 μ A current to achieve this. The unity-gain bandwidth varies directly with transconductance according to Eq. 4.29. For a MOSFET the transconductance is itself proportional to the square root of the bias current, hence a variation in op amp unity-gain bandwidth with current is expected; this is demonstrated in Table 4.4(b) for the single-ended op amp.

$$V_{DD} = 3v, V_{SS} = -3v, I_{DD} = 135\mu A.$$

Parameter	Condition	Value	Units
Gain A_0		69	dB.
GBW	$C_L = 1pF.$	70	MHz.
Phase marg.	$C_L = 1 pF.$	40	deg.
Slew rate	$C_L = 1 pF.$	100	v/usec.
CMRR		62	dB.
Output Z_0		3	$M\Omega$
Offset voltage	st.dev = 10	10	mv.
Noise	input ref.	540	$nv/\sqrt{Hz}$
Power dis.		0.81	mW.

Table 4.4(a) Measured single-ended current mirror op amp performance.

$$V_{DD} = 3v, V_{SS} = -3v.$$

GBW	A_0	I_{DD}	P_D
100 MHz.	66 dB.	267 $\mu A.$	1.6 mW.
70 MHz.	69 dB.	135 $\mu A.$	0.8 mW.
50 MHz.	70 db.	67 $\mu A.$	0.4 mW.

Table 4.4(b) Measured single-ended op amp gain and gain-bandwidth product versus bias current.

4.8 A Comparison of Current Steering and Current Mirror Op Amps

At this point circuit details and test results have been presented for both current steering and current mirror op amps. Earlier in Sect. 4.3 a simple theoretical comparison was made about the amplifiers respective performance. It is now appropriate to re-examine the comparison based on the test results obtained for the two circuits. A tabulation of measured data for single-ended op amps is shown in Table 4.5.

As predicted, the DC gain is comparable for the two circuits. The dynamic behavior is also in rough agreement with expectations. For example, the gain-bandwidth product and slew-rate are higher for the current mirror op amp principally due to the use of current gain in the current mirrors. This also serves to reduce the power dissipation of the current mirror op amp for a given bandwidth. An adverse effect to using current gain, however, is a reduced frequency in the op amp's parasitic pole. This is demonstrated herein by a reduced phase margin in the current mirror op amp. This results in a longer settling time for the current mirror op amp for small voltage transients. However, for large transients, the current mirror op amp's advantage in slew-rate can make up for its deficiency in linear-system settling behavior.

On a final note it's worthwhile to compare the noise performance of the two circuits. Here, it is evident that the current steering op amp displays significantly reduced noise level pointing to a fundamental disadvantage of the mirror amplifier. In order to reduce its input-referred noise, all devices that contribute significantly

to the noise must be increased in area. This includes its input transistors, and all current mirror transistors with source terminal connected to a power-rail. Unfortunately, the oversizing of current mirror devices will reduce the parasitic pole frequency of the op amp and thus reduce the maximum stable gain-bandwidth product that is achievable with that circuit. Thus low-noise high-frequency applications may prove inappropriate for current mirror op amps.

Parameter	Condition	Units	Value	
			Current Steering	Current Mirror
Gain		dB	69	69
GBW	$C_L = 0.75 \text{ pF}^*$	MHz	62	70
Phase margin	$C_L = 0.75 \text{ pF}^*$	degrees	60	40
Slew Rate	$C_L = 0.75 \text{ pF}^*$	$\text{V}/\mu\text{sec}$	80	100
Power Dissipation		mW	1.5	0.8
Offset	mean	mV	-0.55	10
Offset	std. dev.	mV	3.0	10
Noise	1 KHz	$\text{nV}/\sqrt{\text{Hz}}$	160	540

* $C_L = 1 \text{ pF}$ for the current mirror op amp

$$V_{DD} = +3\text{V} \quad V_{SS} = -3\text{V}$$

Table 4.5 A comparison of single-ended, current steering and current mirror op amp performance.

4.9 Conclusions

A comprehensive account of op amp design for application to high-frequency SC filters has been presented in this chapter. The desirability of cascoded output transconductance op amps to this end was emphasized. Details on the two approaches to this: current steering and current mirroring op amps, are subsequently addressed.

A thorough analysis along with test results of single-ended and differential versions of current steering op amps, designed and implemented by the author, has likewise been presented. These circuits were implemented in a CMOS 1.25 micron short-channel technology and achieved bandwidths in excess of 90 MHz.

In addition, the detailed analysis of some high performance current mirror op amps have been included in this chapter. A common-mode feedback circuit that was designed by the author was crucial for a differential current mirror op amp; that circuit has also been presented in this chapter. The current mirror op amps discussed herein have been used in the high-frequency SC filters described in Chapter 7.

CHAPTER 5 INTERNALLY COMPENSATED OP AMPS AND BUFFERS

5.1 Introduction

The preceding chapter describes high bandwidth op amps for internal use in switched capacitor networks. These op amps, however, are unsuitable for many other applications for two reasons: they have high output impedances and their bandwidths decrease directly with capacitive loading. They are thus unable to drive resistive loads and are inappropriate for driving signals off chip. They are also not capable of attaining wide bandwidth and high slew-rates with large, capacitive loads. For these other applications different amplifier techniques are more appropriate.

This chapter focuses on op amps for two related applications. First, two internally compensated CMOS op amps with improved AC PSRR are described; one is for virtual ground operation such as in switched capacitor integrators [49],[50],[61]-[63], and the other is a new circuit for buffer applications requiring wide common-mode input range [61]-[63]. These internally compensated op amps have lower bandwidths than those of Chapter 4, but they can handle larger capacitive loads and moderate resistive loading. Small-signal analysis is developed for the open-loop and PSRR response of the two amplifiers. In addition, design guidelines are suggested, and test results presented.

The second topic is the application of the new op amp circuit to the implementation of high current drive, low output impedance, wideband buffer

amplifiers. These circuit capabilities are required, for example, to deliver high-frequency filtered signals off chip. The amplifier described here is used as a linear line driver in a baseband data communication transceiver [65]. The analysis and development of the first two op amps are necessary for the progression to the high drive buffer amplifier and are therefore presented first.

5.2 Design Techniques for Cascaded CMOS Op Amps with Improved PSRR and Common-Mode Input Range

5.2.1 Introduction

As the maturity of analog MOS amplifier technology progresses, the basic issues of designing workable amplifiers have been solved and many components employing first generation amplifiers have been marketed, principally in filter CODECs and touch-tone decoders. After these initial successes, considerable effort is now underway in enhancing amplifier performance in terms of noise, power-supply rejection, gain-bandwidth product and output drive. The popular two stage op amp shown in Fig. 5.1, for example, suffers from poor positive power-supply rejection; this is because the output drive transistor at moderate frequencies becomes "diode-connected": its drain is AC shorted to its gate by the compensating capacitor, thereby coupling the supply signal to the output.

This section focuses on power-supply rejection problems and examines a recently developed cascoding technique [49],[50], that greatly improves high-frequency rejection, as shown in Fig. 5.2. The addition of transistors M_3 and M_4 in the input

Fig. 5.1 Conventional internally compensated CMOS op amp.

Fig. 5.2 Internally compensated cascoded CMOS op amp with high AC PSRR.

stage permits the connection of the compensating capacitor to the source of a common-gate device (cascode transistor), which decouples the gate of the driver transistor from the compensation capacitor. This technique offers a much improved high-frequency power-supply rejection ratio (PSRR), but it complicates the compensation of the amplifier. One disadvantage of this circuit, however, is a reduction in common-mode input range due to the voltage drop across the cascodes. This tends to restrict the use of such circuits to applications which use a virtual ground. Unity-gain buffers, however, require wide common-mode input range and therefore a folded cascode technique is presented in Fig. 5.3, which has wide common-mode range and retains the benefits of the compensation approach.

As a consequence of the inclusion of the cascode transistors, the design of an op amp becomes considerably more difficult; a second-order small-signal model is no longer sufficient to describe its performance. A detailed small-signal model for the cascoded op amp is presented in this section which is equally applicable to either amplifier. Through the use of this model design of these op amps is greatly simplified. In addition, a small-signal PSRR model is presented that demonstrates the improvement in PSRR of the new op amps over the earlier one in Fig. 5.1. A test circuit including these amplifiers has been fabricated, and experimental results are included that demonstrate improved performance.

5.2.2 Internally Compensated Noncascoded Op Amps

The voice-band op amp of Fig. 5.1 has been widely used for several years, but it is primarily deficient in its AC PSRR to the positive rail. A version of this amplifier

Fig. 5.3 Internally compensated folded cascode CMOS op amp with high AC PSRR and wide common-mode input range.

Fig. 5.4 AC small-signal model for the op amp of Fig. 5.1.

using P channel input transistors would suffer similarly with respect to noise on its negative supply. In order to appreciate the benefits of the cascoded amplifier, a review of the performance of the conventional circuit is in order.

The AC small-signal equivalent circuit is shown in Fig. 5.4. This has been analyzed many times previously, [9],[27], and is well characterized by a dominant pole $\omega_{pd} \approx G_{o1}G_{o2}/g_{m2}C_C$ due to the Miller effect acting on C_C ; this enhances its loading of the first stage by a factor of one plus the gain of the second stage. Here, $G_{o1} = g_{o2} + g_{o4}$ represents the conductances of the first stage, $G_{o2} = g_{o6} + g_{o7}$ represents the conductances of the second stage, and g_{m2} is the transconductance of M_6 . In addition, there is a high-frequency parasitic pole at $\omega_{pH} \approx g_{m2}/C_L$ from the effect of the AC "diode-connected" output transistor M_6 driving the load capacitance; there is also a zero due to the feed-forward path through the compensation network at $\omega_z \approx (g_{m2} - 1/R_Z)C_C$, which reduces phase margin. The nulling resistor R_Z is inserted to cancel the zero, and so it is normally made approximately equal to $1/g_{m2}$.

A small-signal model suitable for analyzing the PSRR to the positive rail (in this case) appears in Fig. 5.5; a recent paper, [59] presents a similar model. Conductance G_{o1} just equals g_{o4} here; g_{o2} connects to the source of the input pair which is an open-circuit for common-mode signals such as power-supply noise and must be excluded. The other conductance, G_{o2} , models the resistive V_{DD} coupling occurring through the P channel device M_6 and therefore equals only g_{o6} . Analysis of the model reveals that the PSRR as a function of the Laplace frequency variable s is:

Fig. 5.5 AC small-signal PSRR model for the op amp of Fig. 5.1.

Fig. 5.6 AC small-signal model for the cascode op amps of Figs. 5.2 and 5.3.

$$\text{PSRR}(s) \approx \frac{(s + \omega_{pd})}{(s + \omega_T)} \quad (5.1)$$

where $\omega_T \approx g_{m1}/C_C$, the unity-gain bandwidth of the amplifier, and ω_{pd} is the dominant pole defined above.

Unfortunately, the zero at the low-frequency of the dominant pole prematurely degrades the PSRR. The explanation is that as frequency rises the impedance of the compensation capacitor C_C becomes low, and the gate and drain of M_6 begin to track one another. The transistor is current-source biased by M_7 and must maintain a relatively constant gate-source drive consistent with the bias current. This requirement forces the gate of M_6 to track V_{DD} fluctuations which are in turn transmitted by C_C to the drain, which is the output of the amplifier.

After this examination of the conventional op amp it becomes evident that one approach to enhance AC PSRR is to find a means to decouple the compensation capacitor from the gate of the output driver (M_6). The cascode op amp, presented next, permits this and results in an appreciable PSRR improvement.

5.2.3 Internally Compensated Cascaded Op Amps

The circuit schematics of the cascoded, internally compensated op amps for virtual ground operation and high common-mode input range operation are shown in Figs. 5.2 and 5.3 respectively. They have the same small-signal equivalent circuit, and both offer excellent high-frequency PSRR. The equivalence can be appreciated by recognizing the similarity in the circuits from their N channel cascodes (M_3 and

M_4) and the P channel current mirrors (M_5 and M_6), through to their output stages and compensation capacitor hook-ups. The only difference is in the polarity of their input stages, and the manner in which they connect to the cascode transistors.

The first circuit uses the direct connection of an N channel source-coupled pair to the source of the cascode transistors. The other circuit, with wide common-mode range, uses a current folding circuit technique similar to that used in a Berkeley transconductance amplifier [20], to permit the direct connection of the drains of a P channel source-coupled pair to the sources of the cascode devices. This requires two additional transistors, (M_{10} and M_{11}), operating as current sources, to bias the first stage. The current-source biased P channel input stage, and the N channel current source devices introduce the same small-signal current variations though to the cascodes and the current mirror as does the N channel input pair of the first circuit. Both circuits force a small-signal current equaling the product of the input transconductance and half the differential input signal. Recognizing the similarity allows the conclusion that the two circuits perform comparably with regard to small-signal performance. The first circuit, however, is restricted in common-mode input range, in the positive direction, to voltages that do not cause an input device to be forced out of saturation by the source of a cascode transistor. With the other circuit, the comparison must be made with respect to negative common-mode input range, owing to the opposite polarity of the input pair. The circuit avoids the problem through the current folding, and it has wide range of the source, and hence the gate biases of the cascode devices are low. This is easily achieved since the gate

voltage of M_3 and M_4 can be quite low; it is restricted only by the need to maintain the N channel current sources M_{10} and M_{11} in saturation. This can be done by borrowing the high-swing cascode biasing technique [20], originally employed in a high-frequency amplifier.

A recent paper [53] presented an N channel input circuit similar to the circuit of Fig. 5.3 and emphasized its wide common-mode input range. That circuit, however, does not use the improved compensation method presented here, and it also suffers from a peculiar adversity due to its biasing which can be discussed in the context of the P channel input circuit of Fig. 5.3. If the gates of transistors M_{10} and M_{11} are driven by a fixed voltage, as in [53], then for large positive common-mode inputs, as exists with a voltage follower for example, the output will abruptly spike up to the positive supply voltage. The sources of the input transistors reduce the drain-source voltage of M_7 , for large positive common-mode inputs, and the bias current is reduced substantially. The input pair current is thus too small to be significant with respect to the fixed bias current of M_{10} and M_{11} , and the gate voltage of the output driver M_8 is therefore abruptly pulled down, pulling the output high.

Normally, when a common-mode input limit is exceeded, in a buffer for example, soft clipping of the output is the result. In this case, however, for positive signals rather than clipping, the output spikes to the positive rail. This problem can easily be avoided by using the novel biasing technique for the N channel current sources (M_{12} - M_{13}) shown in Fig. 5.3. A current mirroring approach is used here whereby the bias current through M_{10} and M_{11} tracks the current through the input source-

coupled pair. For excessive positive common-mode inputs the use of M_{13} , with its gate driven by the positive input, will force the current of M_{12} to follow that of M_7 . This imposes the same reduced drain source voltage on M_{12} as is on M_7 , and this current is mirrored to the N channel transistors. Difference-mode input components are normally held very small by feedback, and thus do not modify this behavior significantly. Through the use of this method there is no penalty when the positive common-mode input limit is exceeded, other than soft clipping.

AC Small-Signal Model

In order to design these op amps it is very useful to work with an appropriate small-signal model that can be used to determine the open-loop frequency response. A model developed for this purpose which shows close agreement with both device level circuit simulations and actual measurements of a test circuit, is shown in Fig. 5.6. The model is considerably more complicated than the one of Fig. 5.4, however, it has proved to be the simplest model that adequately explains the operation of the circuit.

In this section a brief explanation for the model is presented, which can be followed in the context of either Fig. 5.2 or Fig. 5.3. The two current sources of value $V_{tgm1}/2$ result from the action of the input source-coupled pair; the right-hand source corresponds to M_2 and connects to the compensation capacitor C_C and the source of the cascode transistor M_4 ; the left-hand source represents the effect of the small-signal current developed by M_1 after being reflected by the current mirror

formed by M_5 and M_6 . The voltages V_1 and V_2 in the model are the voltages on either side of the cascode transistor M_4 , shown in Fig. 5.2 and Fig. 5.3. The conductance G_{o1} is the small-signal conductance of M_6 , whereas g_{o1} is the small-signal conductance of M_2 for Fig. 5.2; g_{o1} must also include the conductance of M_{11} for Fig. 5.3. The dependent current source $V_1 g_{m2}$ represents the transconductance of cascode device M_4 , and g_{o2} represents its associated small-signal conductance; its current is controlled by its source voltage V_1 , according to the effective transconductance. Note that for a cascode device with a fixed gate bias the effective transconductance G_m is the sum of the gate-source transconductance g_m and the substrate transconductance g_{mb} .

The driver of the second stage of the amplifier, M_8 , is represented by the current source of value $V_2 g_{m3}$ in shunt with a conductance G_{o2} equaling the sum of the small-signal conductances of transistors M_8 and M_9 . The voltage V_2 at the junction of the drains of M_6 and M_4 drives the gate of M_8 , thereby controlling the output current source. The small-signal capacitances are included to effectively model the frequency response. The load capacitor C_L is connected directly to the output, and the compensation capacitor C_C is connected from the output to the source of M_4 . The three remaining capacitors represent parasitics: C_1 includes the gate-source capacitance of M_8 and junction capacitance; C_2 is the gate to drain capacitance of M_8 , and is mainly the overlap capacitance since M_8 is normally saturated; C_3 represents the source-gate capacitance of M_4 and its junction capacitance.

Having formed the model, a few comments and simplifications are in order. First, out of the input stage, only the action of transistors M_2 , M_4 , and M_6 is incorporated directly. These are the most important devices, since they drive both the compensation capacitor and the gate of the second stage. The effect of the other side of the input stage is modeled by the left-most dependent current source. This implies that the current developed by transistor M_1 is mirrored with no bandwidth reduction by M_6 ; the current, in reality, experiences a frequency dependence due to the pole associated with the M_5 - M_6 current mirror. For a voice-band amplifier if this pole is sufficiently fast it can be neglected; if this is not the case, its effect can be incorporated in capacitor C_1 . A simplification of the model is possible by the omission of conductances g_{o1} and g_{o2} ; this reduces the complexity of the model to third-order. Due to the cascoding of the input pair, the conductance seen looking into the V_2 node of the figures is the sum of G_{o1} and the conductance looking into the drain of the cascode device; however, the latter is negligible due to the impedance multiplication properties of a cascode circuit; the impedance is that of the lower device multiplied by the gain of the cascode transistor. Based on this, the DC gain of the circuit will be approximated with very small error by dropping the two conductances. The only other concern is the effect the conductances have on the output impedance at the V_1 node. Fortunately, the impedance is determined primarily by the effective G_m of the cascode device, i.e., $Z_{o1} \approx 1/G_{m2}(1 + g_{o2}/G_{o1})$, and so the conductances can be dropped with no appreciable error. Finally, C_3 may be neglected, since it is very small with respect

to the Miller multiplied compensation capacitor.

The dominant pole of the amplifier is formed by the loading of C_C , increased by Miller effect, on the source of transistor M_4 . The compensation capacitor C_C is multiplied by a factor of $1 + V_O/V_1$, where $V_O/V_1 = G_{m2}g_{m3}/[(G_{o1} + g_{o2})G_{o2}]$, the gain from the source of M_4 to the output. The time constant of the dominant pole is therefore:

$$\tau_{pd} = Z_{o1} \left[1 + \frac{V_O}{V_1} \right] C_C \cong \frac{1}{G_{m2}} \left[1 + \frac{g_{o2}}{G_{o1}} \right] \frac{G_{m2}g_{m3}}{(G_{o1} + g_{o2})G_{o2}} C_C = \frac{g_{m3}C_C}{(G_{o1}G_{o2})} \quad (5.2)$$

and the frequency of the pole is $\omega_{pd} \approx G_{o1}G_{o2}/(g_{m3}C_C)$. This result shows that the dominant pole of the cascoded op amp is located at the same frequency as a comparable noncascoded op amp; the reduced voltage swing at the left-hand side of C_C at the source of M_4 is exactly balanced by an increase in the Miller effect gain acting on C_C from that same node to the output. Omission of the conductances g_{o1} and g_{o2} does not change this fundamental conclusion. The DC gain of the amplifier can be shown to be:

$$\left. \frac{V_O}{V_1} \right|_{DC} = \frac{g_{m1}g_{m3}}{\left[G_{o1} + \frac{g_{o1}(g_{o2} + G_{o1}/2)}{G_{m2}} \right] G_{o2}} \approx \frac{g_{m1}g_{m3}}{G_{o1}G_{o2}} \quad (5.3)$$

The cascoding of the input stage makes the effect of g_{o1} and g_{o2} negligible and, as a result, the gain of the first stage is larger than that of a noncascoded circuit.

Analysis of the AC small-signal model, after considerable algebra and the discarding of minor terms, results in the following polynomial transfer function:

$$\frac{V_o}{V_i} = \frac{-s^2 \frac{g_{m1}}{2} C_C (C_1 + 2C_2) + s \frac{g_{m1} g_{m3}}{2} C_C + g_{m1} G_{m2} g_{m3}}{s^3 C_L C_C (C_1 + C_2) + s^2 \left\{ G_{m2} \left[C_L (C_1 + C_2) + C_C C_1 \right] + g_{m3} C_L C_2 \right\} + s G_{m2} g_{m3} C_C + G_{m2} G_{o1} G_{o2}} \quad (5.4)$$

The sign sequence of the numerator terms can only result from the product of two real zeroes; one in the right half-plane and one in the left half-plane. A simplification of the equation can therefore be obtained, by factoring the numerator and, additionally, by factoring out the dominant pole from the denominator. The result of this is:

$$\frac{V_o}{V_i}(s) = \frac{\frac{g_{m1}(C_1 + 2C_2)}{2C_L(C_1 + C_2)} \left[s - \frac{g_{m3}}{(C_1 + 2C_2)} (1 + \delta_1) \right] \left[s + \frac{G_{m2}}{C_C} \frac{1}{(1 + \delta_1)} \right]}{\left[s + \frac{G_{o1} G_{o2}}{g_{m3} C_C} \right] \left\{ s^2 + s \left[\frac{G_{m2} \left[C_L (C_1 + C_2 + C_C C_1) + g_{m3} C_L C_2 \right]}{C_L C_C (C_1 + C_2)} \right] + \frac{G_{m2} g_{m3}}{C_L (C_1 + C_2)} \right\}} \quad (5.5)$$

where $\delta_1 = \frac{(1 + \delta_2)^{1/2} - 1}{2}$ and $\delta_2 = \frac{G_{m2} (C_1 + 2C_2)}{g_{m3} C_C}$

Design Techniques for Frequency Compensation

Despite the complexity of this expression, several useful design principles can now be extracted. The presence of the right half-plane zero

$\omega_{zr} = [g_{m3}/(C_1 + 2C_2)](1 + \delta_1)$ differs from an equivalent left half-plane zero with respect to phase shift, and degrades phase margin by 90 degrees rather than increasing it. Fortunately, the frequency of this zero is substantially higher than the zero of a noncascoded op amp, and sufficient loop stability can be obtained despite its presence. The quadratic polynomial in the denominator, $D_p(s)$, contributes a pair of high-frequency poles which are best characterized by their natural frequency ω_{op} and quality factor Q_p . The equation for the pair of parasitic poles is:

$$D_p(s) = s^2 + s \left[\frac{G_{m2} [C_L(C_1 + C_2) + C_C C_1] + g_{m3} C_L C_2}{C_L C_C (C_1 + C_2)} \right] + \frac{G_{m2} g_{m3}}{C_L (C_1 + C_2)} \quad (5.6)$$

The corresponding natural frequency and quality factor are:

$$\omega_{op} = \left[\frac{G_{m2} g_{m3}}{C_L (C_1 + C_2)} \right]^{1/2} \quad Q_p = \frac{[G_{m2} g_{m3} C_L (C_1 + C_2)]^{1/2} C_C}{G_{m2} [C_L (C_1 + C_2) + C_C C_1] + g_{m3} C_L C_2} \quad (5.7)$$

In normal operation, output driver M_8 is saturated, and the drain to gate capacitance C_2 is mainly overlap capacitance, in which case $C_2 \ll C_1$. With this assumption, the expressions for ω_{op} and Q_p can be simplified.

$$\omega_{op} \approx \left[\frac{G_{m2} g_{m3}}{C_L C_1} \right]^{1/2} \quad Q_p \approx \left[\frac{g_{m3} C_L}{G_{m2} C_1} \right]^{1/2} \frac{C_C}{C_L + C_C} \quad \text{for } C_2 \ll C_1 \quad (5.8)$$

In order to obtain a satisfactory degree of stability, peaking in the frequency response must be avoided. It is possible to obtain a design with seemingly adequate

phase margin which, however, suffers from insufficient gain margin due to a peaking of the magnitude response beyond the unity-gain bandwidth, caused in turn by a high Q in the poles of $D_p(s)$, as illustrated in Fig. 5.7. This can be avoided by keeping the parasitic pole Q low by making the transconductance of cascode transistors M_3 and M_4 large with respect to that of output driver M_2 . In addition, a moderate value of C_C is required, since depending on the value of C_L , the sensitivity of Q_p to C_C

$$S_{C_C}^{Q_p} = \left\{ \frac{G_{m2}C_L(C_1+C_2) + g_{m3}C_LC_2}{G_{m2}[C_L(C_1+C_2) + C_C C_1] + g_{m3}C_LC_2} \right\} \approx \frac{C_L}{C_L + C_C} ; \text{ for } C_2 \ll C_1 \quad (5.9)$$

can approach unity, and gain peaking can occur. In such cases, with the value of the compensation capacitor reduced to avoid the peaking, the transconductance of the input transistors must be correspondingly reduced to maintain the same unity-gain bandwidth. One other method remains for controlling the parasitic pole Q . This consists of using a relatively large value for C_1 , which is principally the gate capacitance of the output driver. In practice, this can be achieved using a large area for the device, by giving it a relatively long length. the corresponding transconductance g_{m3} will be smaller than normal, but this moderates the Q as well, and the net effect is therefore considerable.

Up until now, only methods of reducing the Q of the high-frequency parasitic pole pair have been considered. These methods will of course also adversely affect

Fig. 5.7 Gain peaking of frequency response when Q of parasitic pole pair is too high.

Fig. 5.8 Small-signal PSRR model for the cascode op amps of Figs. 5.2 and 5.3.

the parasitic zero locations. The overall transfer function, however, displays a greater sensitivity to the parasitic pole pair than it does to the real zeroes, providing Q_p is high [54]; the design of cascoded op amps must therefore involve due consideration of the Q factor. A workable design can be obtained if a cancellation of sorts can be achieved. If the parasitic pole pair has a Q close to one half, then there is actually a double real pole at a frequency of ω_{op} . In this case one of the poles is close enough to approximately cancel the left half-plane zero located at $\omega_{z1} = 2(G_{m2}/C_C)(1+\delta_1)$. With this type of pole-zero cancellation, the op amp transfer function is approximately second-order; it consists of a low-frequency dominant pole, a high-frequency parasitic pole and a right half-plane high-frequency zero. The approximate transfer function assuming this type of cancellation is:

$$\frac{V_o}{V_i}(s) \propto \frac{(s - \omega_{z1})}{(s + \omega_{pd})(s + \omega_{op})} \quad (5.10)$$

A similar transfer function occurs in a noncascoded op amp. However, the right half-plane zero is at a lower frequency, and it must be canceled through the use of a resistance in series with the compensation capacitor. In the present case, however, the zero is at high frequency and such measures are unnecessary.

A.C. Small-Signal Model for PSRR

The PSRR small-signal model derivation closely follows that of the model just discussed, and hence it is not necessary to go into as much detail. The model appears in Fig. 5.8, and is similar to the model for the noncascoded op amp shown

in Fig. 5.5, except it is in the context of the cascode model of Fig. 5.6. The conductance g_{o1} is omitted here, since it connects to the source of the input pair, which is open-circuit for common-mode signals such as power-supply noise. Conductance G_{o2} now equals g_{o8} since the resistive coupling at the output stage is only through M_8 . As with the earlier PSRR model, the input signal V_i represents noise on the V_{DD} rail, and it is therefore not an AC ground.

Analysis of this model reveals a significant increase in the frequency of the zero in the transfer function of the V_{DD} noise to the output. The transfer function can be reasonably approximated by:

$$\text{PSRR}(s) \approx \frac{C_2}{C_C(1+\delta_3)} \frac{\left[s + \frac{G_{o1}G_{o2}}{g_{m3}C_2} \right]}{\left[s + \omega_T \frac{1}{(1+\delta_3)} \right]} \quad (5.11)$$

where $\delta_3 = \frac{1}{2} \frac{g_{m1}}{G_{m2}}$ and $\omega_T = \frac{g_{m1}}{C_C}$ the unity gain bandwidth.

The expression for the zero is very similar to that for the noncascode op amp. They differ only in the value of the capacitance: this is C_C for the previous op amp, and it is C_2 for the cascode op amp. From this analysis it is evident that the mechanism causing a zero is the same for either circuit, namely the amount of capacitance coupling the gate of M_8 to the output. The improvement in the zero frequency for the cascode op amps is therefore the ratio of C_C to C_2 ; this is very

high since C_C is the compensation capacitor whereas C_2 is only the drain to gate capacitance of a saturated transistor (M_8). The pole frequency is on the order of the unity-gain bandwidth, $\omega_T = g_{m1}/C_C$, as in the previous case.

5.2.4 Results

Comparison of Models with Full Circuit Simulation

In order to demonstrate the validity of the modeling and analysis of the cascode op amps, and of the improved AC PSRR, a plot of frequency response is presented in Fig. 5.9. Here, a complete SPICE circuit simulation of the cascode circuit of Fig. 5.2 (solid lines), is compared with the AC small-signal models (points) for the open-loop frequency response, and PSRR frequency response. The accuracy of the small-signal models is quite good and breaks down only at frequency beyond the gain-bandwidth product of the amplifier. Also included in the figure is a PSRR frequency response curve for a noncascode version of the same op amp. A major improvement in high-frequency PSRR (>30 dB.) is evident for the cascoded op amps.

Test Results

Circuits for the cascoded op amps of Figs. 5.2 and 5.3 have been fabricated and tested. A photomicrograph of the wide common-mode input range op amp of Fig. 5.3 is shown in Fig. 5.10, for example. Its biasing network, consisting of transistors M_{12} – M_{14} , was not fabricated and so test results regarding its input common-mode range are unavailable; however, simulations validate its effectiveness.

Fig. 5.9 Frequency response of the approximate model (points), and of a complete SPICE circuit simulation (solid lines) for the cascode op amp of Fig. 5.2.

Fig. 5.10 Photomicrograph of the cascode op amp of Fig. 5.3.

in overcoming the output glitching problem. In all other respects similar test results were obtained for both amplifiers, as expected, and are outlined in Table 5.1 for the circuit of Fig. 5.2. A photograph of the experimental V_{DD} PSRR for the circuit of Fig. 5.2 showing the excellent high-frequency rejection (>55 dB at 100 KHz.), appears in Fig. 5.11. The upper curve is the 0 dB reference level, and the lower curve is the V_{DD} PSRR.

$$V_{DD} = 2.5\text{v. } V_{SS} = -2.5\text{v. } I_{DD} = 124\mu\text{A.}$$

Parameter	Condition	Units	Value
Gain		dB	83
PSRR (V_{DD})	100 KHz	dB.	55
PSRR (V_{SS})	100 KHz	dB.	67
CMRR	100 KHz	dB.	44
Slew Rate	positive	v/ $\mu\text{s}^{\circ}\text{c}$	10
Slew Rate	negative	v/ μsec	3.3
Offset		.mv	7.3
Noise	1 KHz	nv/ $\sqrt{\text{Hz}}$	95

Table 5.1 Measured performance for cascode op amp of Fig. 5.2.

5.3 Low Impedance High Swing CMOS Buffers

5.3.1 Introduction

In this section the internally compensated folded cascode CMOS op amp is applied to the design of a buffer with wide-swing, high-current, low-output impedance and wide bandwidth. The previous small-signal analysis is applicable to the frequency compensation of the buffer. This is supplemented with large-signal

Fig. 5.11 V_{DD} PSRR for the cascode op amp of Fig. 5.3.

analysis to demonstrate the circuits benefits in high-current applications. A test circuit for the buffer has been fabricated and experimental results are presented.

5.3.2 Wide voltage swing output stages

In shorter channel technologies it is important for the output to be able to swing close to the rail. For example, in the 3 micron CMOS process used for the test circuits of this chapter, the power supply is restricted to 5 volts. In this case source follower output stages as in Fig. 5.12(a) are ruled out since they can only come within a threshold voltage of either power rail. The threshold voltage can be as high as 1 volt in magnitude and the output is limited to only a 3 volt swing with a 5 volt supply.

The alternative is the complementary common-source amplifier shown in Fig. 5.12(b) which can swing over the full 5 volt range. The combination of voltage gain and signal inversion gives this stage rail to rail capability.

The output impedance of the source follower stage is $1/(g_{mN} + g_{mP})$ and is relatively low. The common-source stage, however, has an output impedance $1/(g_{oN} + g_{oP})$, which is substantially higher. This high-output impedance must be reduced by feedback. The approach used here is motivated by the suggestion of Gray and Meyer [67] to use dual predrivers as shown in Fig. 5.13. This configuration has an output impedance of

$$R_o \cong 1/(g_{m1}A_1 + g_{m2}A_2) \quad (5.12)$$

Fig. 5.12 (a) A complimentary source follower output stage, (b) A complimentary common-source amplifier output stage.

where A_1 and A_2 are the gain of the P channel and N channel predrivers respectively.

This can be implemented using dual differential source coupled pairs as in Fig. 5.14 [68]. However, this approach severely restricts the gate source voltage that can be applied to either output transistor when operated in closed loop. For example, a positive input signal will be followed by the source of M_3 (node 1 in the figure) with a difference of a little more than a threshold voltage. On the other hand the gate of M_1 must go low to pull the output high since the output stage inverts. The low-going gate can only swing to the voltage at node 1, which is at a large positive value. Large resistive loads require large currents and therefore either large gate-source voltages or very wide output transistors. In order for two different sized transistors to pass the same current they must have different gate-source voltages according to

$$\frac{(W/L)_A}{(W/L)_B} = \left(\frac{V_{GSB} - V_T}{V_{GSA} - V_T} \right)^2 \quad (5.13)$$

Hence a major width reduction is permitted if the predriver can deliver a large gate-source voltage.

The folded cascode op amps of the previous section can deliver a gate-source voltage to the output driver almost as large as the total supply voltage and are therefore advantageous for use in a high-current buffer.

Fig. 5.14 Simple buffer circuit.

Fig. 5.15 Improved buffer circuit using folded cascode predrivers.

5.3.3 The buffer circuit

A schematic of the chosen buffer circuit is shown in Fig. 5.15. It uses a folded cascode circuit with an N channel input pair ($M_3 - M_{11}$) to drive the P channel output transistor, and a P channel input pair folded cascode circuit ($M_{12} - M_{20}$) to drive the N channel output transistor. The common-mode input range is limited to under a threshold voltage from either supply rail. If unity-gain feedback is applied, the output also has this restriction. This can be avoided by using the buffer in a noninverting gain-of-two circuit by applying resistive feedback. This halves the common-mode input range requirement.

Frequency compensation is provided by the capacitive feedback from the output to the sources of the cascode transistors (C_1 and C_2) and also to the gates of the output drivers (C_3 and C_4). The small-signal analysis of this type of circuit has already been presented in section 5.1.3. The previous amplifiers were compensated with a single capacitor connected to the source of the cascode. Here a high bandwidth is required, as is a high-current drive. The high-current capability requires wide, minimum length output transistors with high transconductance. Equation 5.8 shows that the Q of the parasitic pole pair varies as the square root of the transconductance ratio of the driver (g_{m3} in the eqn.) to the cascode (G_{m2} in the eqn.). Therefore the high-current buffer has a high Q parasitic pole pair.

A small amount of Miller compensation can reduce the Q as shown in Equation 5.7, where C_2 represents the Miller capacitor. This is implemented in the buffer with capacitors C_3 and C_4 . A slight improvement in stability is provided by

the use of series resistors $R_1 - R_4$. When the amplifier is operated with resistive feedback as a gain-of-two amplifier, the loop gain is attenuated by 6 dB. This provides a large enough increase in phase margin for good stability without the extra Miller compensation. Unity-gain operation, however, does require this additional feedback network. A problem that arises with the dual differential input pair type of buffer is the control of the quiescent bias current in the output stage. Ideally the output stage current is set by a current mirroring from the predrivers, which are biased with a constant current source. For example, in Fig. 5.14 if there is no random offset the drain voltages of M_7 and M_8 will be equal, and the current set up by current source M_{11} will be mirrored to M_5 in accordance with geometry scaling. The same argument applies for the current of M_6 . The circuit is therefore optimally designed if the mirrored currents for M_5 and M_6 are equal.

In practice random input-referred offset voltages are unavoidable for the two predrivers; this is shown in Fig. 5.13. These are always unequal, and their difference is multiplied by the gain to result in an offset in the output stage quiescent current according to

$$I_{os} = A_1 g_{m1} V_{os1} - A_2 g_{m2} V_{os2} = A g_m (V_{os1} - V_{os2}) \quad (5.14)$$

if $A_1 = A_2 = A$ and $g_{m1} = g_{m2} = g_m$. This offset varies inversely with the closed-loop output impedance $1/(2Ag_m)$. Consequently the output impedance cannot be made arbitrarily low without impacting the quiescent bias current. A large positive offset bias current consumes excessive power whereas a large negative offset current

dramatically increases crossover distortion by forcing the output into class B operation.

This problem can restrict the minimum output impedance to a moderate value. In some cases a two stage composite amplifier consisting of a conventional op amp preceding a closed-loop output buffer can be used to further reduce the closed-loop output impedance. The buffer's output impedance is reduced by one plus the loop gain of the composite amplifier. This works well for voiceband applications but is impractical for high bandwidth cases. The buffer amplifier is limited in bandwidth itself, and it contributes phase shift at high frequency. The composite amplifier must therefore be compensated at a reduced bandwidth to be stable.

A High Bandwidth Buffer For Data Communications

As an example, for a data communication application a relatively high bandwidth line driver is required. The amplifier needs to pass low distortion sine-wave type signals having significant energy between 64 KHz and 256 KHz, centered at 160 KHz. It is therefore desirable to have enough loop gain at the center frequency to significantly reduce distortion. To meet this need a buffer with a greater than 20 MHz unity-gain bandwidth was designed. It operates with resistive feedback as a noninverting gain of two amplifier to halve the common-mode input range requirements, and it has a loop bandwidth greater than 10 MHz in this configuration. This provides 40 dB of loop gain at 100 KHz and 36 dB at 160 KHz, with harmonic distortion below 1%.

It is sometimes possible to use an additional op amp preceding a buffer to form a composite amplifier with extremely low distortion. In this application, however, a composite amplifier cannot achieve the required bandwidth, so a buffer is used by itself. The output impedance in this case is $1/(2A_{gm})$ (eqn. 5.12) and can only be minimized by increasing A_{gm} . This is at odds with the requirements to reduce the output offset current I_{os} as described in equation 5.14. Consequently output impedance must be traded off against offset current depending on the application.

In the resistive driver application output current capability is important, otherwise the signal swing is limited. The output transconductance is chosen to meet two requirements: the output impedance and the current capability. The current capability is also governed by the maximum gate-source voltage that can be delivered by the predriver. If this voltage is low, then a larger transconductance is necessary; this can also be larger than required for output impedance considerations.

The predrivers used here allow the maximum voltage swings and permit the transconductance of the output stage to be minimized. This reduces the offset current, and it also enables the output stage to operate at a low quiescent current, yet still deliver high current when required. In addition, reducing the transconductance of the output stage decreases the width of its P and N channel transistors; capacitive loading on the predriver is minimized by this, and higher bandwidth operation is enabled.

Test Results

Test results for the low-impedance buffer are shown in Table 5.2. A bandwidth of greater than 20 MHz is attained, along with a 4 volt output swing into a 800 Ω load. The nominal design current is 650 μA , with 250 μA in the output stage. The test circuit has an average output current of 335 μA ; this is 135 μA above the nominal value due to the amplification of the difference of the two offsets. Equation 5.14 predicts a 200 μA variation in current for a 5 mV difference in input offset voltages. A variation of this size is not unreasonable compared to the nominal 650 μA bias current of the entire buffer.

TABLE 5.2 Test Results for High Bandwidth Buffer (± 2.5 V Supplies)

Parameter	Condition	Value	Units
GAIN		58	dB
GBW	unity-gain	25	MHz
OUTPUT SWING	$R_L = 800 \Omega$ gain = 2	4	V p.p.
OFFSET	typical	5	mV.
DISTORTION	typical	<1	%
I_{DB}	average	735	μA

5.4 Conclusions

Two internally compensated CMOS op amps with improved high-frequency PSRR have been reported: the first is for use in circuits with virtual ground operation, such as switched capacitor integrators; the second is a new circuit with wide common-mode input range, which is therefore useful in buffer applications. Both op amps are operable with moderate resistive loads; as such they are suitable for use in active RC prefilters and as off-chip drivers.

The wide-range circuit also solves an output spike phenomena that arose in operation of a previously reported op amp.

It is shown that both circuits are equally well described by the same small-signal model which is derived herein. Based on resulting considerations, design techniques for frequency compensation are presented. Test circuits for both op amps have been fabricated, and these corroborate the results of the small-signal model.

In addition the wide range op amp circuit is utilized in the implementation of a high current drive, low output impedance, wideband buffer amplifier. Test circuits for this amplifier demonstrate a 20 MHz bandwidth and large signal operation into 800 Ω loading.

CHAPTER 6 BIQUAD ALTERNATIVES FOR HIGH-FREQUENCY SWITCHED-CAPACITOR FILTERS

6.1 Introduction

By their very nature, SC filters are sampled analog systems that undergo transients on every clock phase. In order to operate at high clock and signal frequencies, these transients must settle quickly. The settling time, however, is limited by the finite bandwidth and slew-rate of the op amps and the nonzero resistance of the MOS transmission gates used in the filters. Recent success has been achieved in dealing with these problems in extending the application of SC filtering to higher frequency [20],[55],[56]. This has been done predominantly by increasing the speed of the op amps.

However, performance can also be enhanced by developing SC filters with reduced sensitivity to finite bandwidth elements. Thus, a considerable effort has been made here to optimize the performance of the SC biquad [70]. In addition, recent advances in short-channel process technology are exploited for this filtering application. The high-speed, 1.25 micron CMOS op amps described in Chapter 4 along with fast switches, are used in optimized biquad filters. The resultant combination achieves SC filtering in the low Mega-Hertz frequency range.

To this end the following route is taken: First, in Section 6.2, the transient response of the SC integrator is considered for circuits using both zero output impedance and high output impedance (transconductance) op amps. The latter

case is of specific importance, since the high bandwidth op amps actually used herein are of this type. The differences are clearly demonstrated. From here, in Section 6.3, the existing theory of finite bandwidth performance limitations is generalized, and extended to the important practical case of transconductance op amps.

Next, biquad alternatives are presented, in Section 6.4, for both single-ended and differential SC filters. The biquad is of immense importance since it is the building block of most practical filters. The biquad options differ drastically in their suitability for high-frequency operation, and they are ranked accordingly. This is demonstrated in Section 6.5 in terms of the earlier analytical results, and also through the use of a nonideal SC analysis program.

Finally, in Section 6.5, a methodology for the frequency compensation of high-frequency SC filters using transconductance op amps is presented. This method ensures op amp stability, despite periodically varying loading conditions within an SC filter.

6.2 Transient Response of SC Integrators

SC networks change state on every clock phase and repeatedly undergo transients to generate a sampled-analog output. The nature of the transients and the extent to which they are settled, have a profound influence on the frequency response. In the present section the transient behavior of the SC integrator, the basic building block of SC filters, is examined for two special finite bandwidth op

amp cases: zero impedance, and infinite impedance (transconductance) outputs. The latter case is of considerable importance, since higher bandwidths are achievable with cascoded output, i.e., with transconductance op amps as discussed in Chapter 2.

Finite bandwidth zero-output impedance op amps

The analysis of the transient response of the inverting integrator of Fig. 6.1 is detailed in Appendix A.1. The op amp is modelled therein by the first-order differential equation

$$\frac{dv_o(t)}{dt} = \omega_T v_i(t) \quad (6.1)$$

where ω_T is the unity-gain bandwidth.

The transient response during phase 2 from Eqs. (A.4) and (A.5) is

$$v_1(t) = \beta e^{-\omega_T \beta t} v_1(o^-) + \alpha e^{-\omega_T \beta t} v_i(o^-) \quad (6.2)$$

$$v_2(t) = v_2(o^-) - (1 - e^{-\omega_T \beta t}) v_1(o^-) - \frac{C_1}{C_2} (1 - e^{-\omega_T \beta t}) v_i(o^-) \quad (6.3)$$

where $\alpha = C_1/(C_1 + C_2)$ and $\beta = C_2/(C_1 + C_2)$; $0 < \beta \leq 1$.

These exponential responses result from the first-order differential equation and have a settling time constant $\tau = 1/(\omega_T \beta)$. The parameter β is the feedback factor. If β is less than its maximum value of unity the settling time is lengthened.

The feedback nature of the circuit during phase 2 is shown in the signal flow diagram in Fig. 6.2. The loop gain is attenuated by the factor β owing to the

3 OF/DE 3

MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS
STANDARD REFERENCE MATERIAL 1010a
(ANSI and ISO TEST CHART No. 2)

Fig. 6.1 Stray-free inverting switched-capacitor integrator.

Fig. 6.2 Signal-flow diagram of the SC integrator during phase 2.

voltage divider action of capacitors C_1 and C_2 . For comparison the ideal response can be obtained by letting ω_T tend to infinity in Eqs. (2) and (3). Clearly the error in the voltages is an exponential function of the bandwidth, feedback factor, and duration of the phase.

Finite bandwidth transconductance op amps.

The present case is representative of high output impedance cascoded output op amps in performance. These op amps are suitable only for operation into a capacitive load that serves also as the compensation capacitor. The transconductance amplifier has a unity-gain bandwidth $\omega_T = g_m/C_L$, where g_m is the short-circuit transconductance and C_L is the capacitance load. The transient response of the integrator for this case is described in Appendix A.2 by Eqs. (A.10) and (A.11).

$$v_1(t) = e^{-\omega_{T2}\beta t} v_1(o^-) \quad (6.4)$$

$$v_2(t) = v_2(o^-) - v_1(o^-) - \frac{C_1}{C_2} \left(1 - \frac{1}{\alpha} e^{-\omega_{T2}\beta t} \right) v_1(o^-) \quad (6.5)$$

where $\omega_{T2} = g_m/C_{L2}$ and $C_{L2} = C_1 C_2 / (C_1 + C_2)$.

The bandwidth for a transconductance amplifier depends on the capacitive loading of the circuit; as such it varies from phase to phase. It is important to ensure that this type of op amp is always loaded; otherwise, it can become unstable from internal parasitic poles.

A major difference in the transient response of the two types of integrators is the

feedforward path through the two capacitances C_1 and C_2 to the output. The output is a voltage source in the previous case; here, however, the input signal is initially connected to the output without resistance from the open-circuit amplifier. A capacitance load at the output, if present, will attenuate the feedforward signal. This tends to match the behavior of a zero output impedance circuit but the bandwidth is reduced accordingly. If, for example, a fixed capacitor C_4 is connected between the op amp output and ground, Eq. (5) becomes

$$v_2(t) = v_2(o^-) - \left[1 - \frac{C_4}{C_{L2}} e^{-\omega_T \beta t} \right] v_1(o^-) - \frac{C_1}{C_2} \left[1 - \left(1 + \frac{\beta C_2}{C_{L2}} \right) e^{-\omega_T \beta t} \right] v_1(o^-) \quad (6.6)$$

where $C_{L2} = C_1 C_2 / (C_1 + C_2) + C_4$.

Since v_1 is much smaller than v_2 or v_i , the predominant error mechanism is the departure of the v_1 term from the ideal value $-C_1/C_2$. The effect of the feedforward path is an addition to the relative error in this coefficient by the amount $\beta \frac{C_2}{C_{L2}} e^{-\omega_T \beta t}$ over the error for zero impedance op amps. The two types of integrators have errors (ϵ) related according to

$$\epsilon \Big|_{R_o=\infty} = \left(1 + \frac{\beta C_2}{C_{L2}} \right) \epsilon \Big|_{R_o=0} \quad (6.7)$$

The ratio of the errors varies from $1/\alpha$ for $C_4 = 0$ to unity for $C_4 \gg \beta C_2$. However, C_4 also influences the bandwidth of the transconductance op amp.

6.3 Performance Limitations of SC Filters Using Finite Bandwidth Op Amps

In this section the influence of finite op amp bandwidth on the frequency response of state-variable biquad filters is considered. The degradation due to nonzero switch resistance has already been explored [45] and is not dealt with here. Switch resistance can be made arbitrarily low (at the expense of clock feedthrough) by increasing the width of the MOS transmission gates; it is therefore considered less of a problem than finite op amp bandwidth. The basic approach to the finite bandwidth analysis for zero output impedance op amps comes from Martin and Sedra [43]. Their results are generalized here for all integrator switching configurations. The important case of transconductance op amps is also considered herein.

A detailed analysis is included in appendices A through C. Appendix A analyzes the transient response of finite bandwidth SC integrators and Appendix B develops an equation formulation for the frequency response of nonideal SC integrators. Appendix C applies the results of the transient responses in A to the equations in B to yield the frequency response of finite bandwidth SC integrators.

The influence of nonideal SC Integrators on state-variable SC biquads

The departure of the SC integrator from its ideal Z domain transfer function, owing to the finite op amp bandwidth, results in magnitude and phase errors. These errors deteriorate the frequency response of the double integrator state-variable SC biquad. High-order filters, whether cascades of biquads, or operational

simulations of passive LC ladders, employ biquads as their basic building blocks. It is therefore worthwhile to examine the performance of biquads comprised of nonideal SC integrators. Consider the inverting (Fig. 6.1) and noninverting stray-free SC integrators. The ideal discrete time transfer function is

$$H_i(\omega) \triangleq \frac{V_o(\omega)}{V_i(\omega)} = \pm \frac{\alpha_r}{j\omega T} \left[\frac{\omega T}{2 \sin \frac{\omega T}{2}} \right] e^{-j \frac{\omega T}{2}} \quad (6.8)$$

where $\alpha_r = C_1/C_2$. For a large clock-to-signal-frequency ratio, i.e., $\omega T \gg 1$,

$$H_i \approx \pm \frac{\alpha_r}{j\omega T} \quad (6.9)$$

and the SC integrators closely simulate the performance of continuous time integrators with a time constant T/α_r .

If the magnitude and phase of the SC integrators depart from those of ideal responses, due to incomplete settling of transients, then

$$H_a(\omega) = H_i(\omega)E(\omega) \quad (6.10)$$

and

$$E(\omega) = \frac{1}{[1 - m(\omega)]e^{-j\theta(\omega)}} \quad (6.11)$$

Where $H_a(\omega)$ is the actual response and $E(\omega)$ is the error factor, $m(\omega)$ is the magnitude error and $\theta(\omega)$ is the phase error; both m and θ are real functions of frequency. For the case of small magnitude and phase error, i.e., $m(\omega), \theta(\omega) \ll 1$, the error factor becomes

$$E(\omega) \cong \frac{1}{[1 - m(\omega) - j\theta(\omega)]} \quad (6.12)$$

Well known formulae exist for evaluating the deviation in frequency response of state-variable biquads, and operational ladder simulations due to magnitude and phase errors.

Consider a two-integrator biquad comprised of two nonideal SC integrators with magnitude errors $m_1(\omega)$ and $m_2(\omega)$ and phase errors $\theta_1(\omega)$ and $\theta_2(\omega)$, respectively; then the following equations apply. The resonant frequency has a relative shift of

$$\frac{\Delta\omega_o}{\omega_o} \cong 1/2 [m_1(\omega_o) + m_2(\omega_o)] \quad (6.13)$$

The actual Q factor (Q_a) is

$$Q_a \cong [1/Q + \theta_1(\omega_o) + \theta_2(\omega_o)]^{-1} \quad (6.14)$$

for the case of $\theta_1(\omega_o), \theta_2(\omega_o) \ll 1$ and equal integrator time constants. Finally, the gain at resonance differs from the ideal gain according to

$$\frac{|T_a(\omega_{oa})|}{|T_i(\omega_o)|} \cong \frac{1}{1 + Q[\theta_1(\omega_o) + \theta_2(\omega_o)]} \quad (6.15)$$

where T_a is the value of the actual transfer function.

Analysis of zero output impedance op amp SC integrators

In this section the results of the analysis in Appendix C are applied to the preceding formulas. The analysis shows that only two error factors ($E(\omega)$) describe both inverting and noninverting integrators. The applicable error factor depends

only on whether there is a one phase delay in sampling the output of an integrator after it has sampled its input. For the case of no delay, the error factor is, from Eq. (C.9),

$$E_N(\omega) \cong 1 - e^{-k_2} + z^{-1} \beta e^{-k_2} \quad (6.16)$$

where

$$k_2 = \omega_T \beta T / 2$$

If output sampling is delayed by one phase the error factor is from Eq. (C.13)

$$E_D(\omega) \cong 1 - \alpha e^{-k_2} \quad (6.17)$$

The subscripts N and D refer to nondelayed and delayed respectively.

The errors in magnitude and phase can be found by applying Euler's formula to z^{-1} and equating terms in Eq. (6.12); this leads to the expressions:

$$m_N(\omega) \cong - [1 - \beta \cos(\omega T)] e^{-k_2} \quad (6.18)$$

$$\theta_N(\omega) \cong - \beta \sin(\omega T) e^{-k_2} \quad (6.19)$$

$$m_D(\omega) \cong - \alpha e^{-k_2} \quad (6.20)$$

$$\theta_D(\omega) \cong 0 \quad (6.21)$$

Errors of similar magnitude are obtained for delayed and nondelayed sampling. The phase error for delayed sampling, however, is eliminated due to an increased settling time. These results may be substituted into Eqs. (6.13)-(6.15) to evaluate the error in resonant frequency, Q and gain for nonideal state-variable biquads. The exponential nature of Eqs. (6.18)-(6.21) is to be compared with the linear nature of the errors that occur in continuous time active RC state variable biquad

filters [54],[71].

Analysis of transconductance op amp SC integrators

For the two sampling cases, the analysis for transconductance op amp SC integrators results in error factors that are similar to those for zero impedance op amps. The error factor for the nondelayed case is, from Eq. (C.16)

$$E_N(\omega) = 1 - 1/\alpha e^{-k_2} + z^{-1}(C_2/C_1)e^{-k_2} \quad (6.22)$$

where $k_2 = \omega_T \beta T/2$ with $\omega_T = g_m/C_{L2}$ and $C_{L2} = C_1 C_2 / (C_1 + C_2)$; and for the delayed case the error is, from Eq. (C.20),

$$E_D(\omega) = 1 - e^{-k_2} \quad (6.23)$$

The associated magnitude and phase errors are

$$m_N(\omega) \cong \frac{1}{\alpha} [1 - \beta \cos(\omega T)] e^{-k_2} \quad (6.24)$$

$$\theta_N(\omega) \cong \frac{C_2}{C_1} \sin(\omega T) e^{-k_2} \quad (6.25)$$

$$m_D(\omega) \cong e^{-k_2} \quad (6.26)$$

$$\theta_D(\omega) \cong 0 \quad (6.27)$$

These errors are related to those preceding by

$$[m_N(\omega), m_D(\omega), \theta_N(\omega), \theta_D(\omega)] \Big|_{R_0=\infty} = \frac{1}{\alpha} [m_N(\omega), m_D(\omega), \theta_N(\omega), \theta_D(\omega)] \Big|_{R_0=0} \quad (6.28)$$

The difference in errors is due to the feedforward signal path. If a fixed

capacitor C_4 , is connected between output of the op amp and ground it can be shown that the error relationship between the two types of SC integrators is given by

$$\left[m_N(\omega), m_D(\omega), \theta_N(\omega), \theta_D(\omega) \right] \Big|_{R_0=\infty} = \left(1 + \frac{\beta C_2}{C_{L2}} \right) \left[m_N(\omega), m_D(\omega), \theta_N(\omega), \theta_D(\omega) \right] \Big|_{R_0=0} \quad (6.29)$$

where $C_{L2} = C_1 C_2 / (C_1 + C_2) + C_4$

This agrees with the original observation regarding the feedforward effect in Eq. (6.7); for that reason it indicates larger errors for transconductance op amp integrators. The other difference is that ω_T for the transconductance op amp depends on the circuit loading whereas this is a constant for internally-compensated low impedance op amps.

A few design considerations can be drawn from these results. First, delayed sampling is preferable over nondelayed sampling since the phase error is minimized and the gain and Q accuracy benefit. Second, all error terms derived herein depend on the bandwidth during the phase an integrator samples its input. Thus a transconductance op amp integrator is relatively insensitive to additional capacitive loading connected during the delayed sampling phase.

These formulas apply for single integrators; however, with transconductance op amps the interaction between connected integrators is much more significant. Fig. 6.3 illustrates some of the problems. Here, for example, two integrators are shown interconnected on a phase. The left-hand op amp is loaded by the driving-point impedance of the following integrator; in this circumstance, its settling

depends somewhat on the settling of the other integrator.

A second complication is that the formulas are restricted for sampled and held zero impedance inputs. In this example, a high impedance exponential input is applied to the right-hand integrator. The formulas in this case tend to underestimate the errors. The actual derivation of formulas for connected integrators is very tedious (it has been done for zero impedance op amps [44]), and it results in expressions far too complicated to extract meaningful principles from. A practical alternative is the use of a nonideal switched-capacitor analysis program that can handle arbitrary finite bandwidth networks. A simulator intended for this purpose called NISCAP, (a acronym for nonideal switched-capacitor analysis program [66]) has been described in Chapter 3. It is used in the next section to compare biquad structures.

6.4 Biquad Alternatives for Single-Ended and Differential High-Frequency SC Filters

In this section, various options for building double integrator state-variable biquad sections are considered and compared on the basis of their amenability for high-frequency operations. Most high-order filters use biquads as building blocks, so it is important to examine and optimize their performance. To this end, single-ended and differential biquads are extensively compared with respect to accuracy of frequency response. The comparison is done using the results of Section 6.5 and the nonideal SC analysis program NISCAP.

Single-ended biquads

In high Q filters the input and damping capacitors are approximately Q times smaller than the integrator input-capacitors. This justifies their exclusion in order to simplify the following comparisons. Only the undamped two-integrator loop is considered.

Existing state-of-the art single-ended biquads use the lossless digital integrator, (LDI) approach [24]. Here two opposite polarity integrators form a two integrator loop. Clock phasing is such that signals experience a one sampling period delay around the loop. The result is that the integrators have only magnitude errors and accordingly, have infinite Q factors; the delay is equivalent to a 360° phase shift and can be ignored. The LDI integrator transfer function is described by Eq. 6.8. The bracketed term is the magnitude error, and it can be corrected by prewarping the filter specifications. All biquads that are considered here use LDI timing for this reason.

For loop stability negative loop gain is required; hence, a combination of a noninverting and an inverting integrator is mandatory. No other options are possible for single-ended filters. It has been shown [43], however, that different LDI switch phasing can result in circuits with identical transfer functions, yet differing sensitivities to limited op amp bandwidths. In such circuits, on one of the phases both op amps are interconnected. On that phase the circuit should conform to Fig. 6.3, so that the left-hand integrator has no input capacitor. The resultant unity-gain feedback for that op amp allows the coupled transient to settle more quickly.

Fig. 6.3 Two integrators interconnected on a phase.

Differential biquads

Differential circuit techniques are useful wherever high common-mode and power-supply rejection are mandatory. With a differential signal path, clock feedthrough and op amp power-supply coupled noise are common-mode; hence they are distinguishable from difference-mode signals. Recently reported fully differential SC filters with improved power-supply rejection [26] demonstrate the viability of this approach. Marginal power-supply rejection is anticipated for high-frequency circuits; this is owing in part to a requirement for down-scaled capacitor sizes. Therefore differential implementation is proposed. An equally important reason which is substantiated in this chapter, is that superior high-frequency performance is attainable.

Differential stray-free integrators are derived from single-ended inverting and noninverting integrators by the connection of duplicate circuitry to the opposite side of the op amps, as shown in Fig. 6.4(a) and (b). Through the substitution of the balanced integrators, existing single-ended networks become differential-mode equivalents with identical Z domain transfer functions. Networks derived in this direct fashion are viable. However, several other switching variations exist in the differential realm. Signal inversion can be achieved by reversing connections of the op amp outputs in the differential signal path; both polarities of integrators are thus realizable from both inverting and noninverting single-ended prototypes.

The ability to arbitrarily invert signal polarity offers additional flexibility in the design of LDI biquads. In addition to implementing differential versions of existing

Fig. 6.4 Differential SC integrators. (a) Noninverting (b) Inverting (c) Differencing-input.

single-ended biquads, it is possible to configure biquads using solely inverting or solely noninverting integrators. All variants on the LDI state-variable biquads thus derived have identical transfer functions. However, they differ in their suitability for high-frequency operation. This is demonstrated in Section 6.5.

In addition to the biquad options just detailed, there exists another family of SC biquads, as shown in Fig. 6.4(c), based on differencing-input integrators [25],[26]. These new circuits deliver a double-size voltage step to the left-hand side of the input capacitors that is the difference of the balanced outputs of the preceding op amps. The implications of the differencing-input SC integrators are substantial. Most important is the amplitude doubling of the input voltage steps; this necessitates the halving of the input capacitor values to maintain the same time constant as applies to previous integrators.

The halving of the input capacitors offers several advantages for high-frequency operations. First, the feedback factor (β) is closer to unity, shortening the settling time. Along with this, the total capacitive loading on the op amps is reduced. For transconductance op amps this raises bandwidth and slew-rate to further reduce the settling time. For internally compensated op amps, the second-order parasitic poles formed by output capacitive loading are at higher frequency; this likewise can shorten settling time by improving the phase margin. Another benefit is a significant reduction in the RC time constants associated with the MOS transmission gates. If the input capacitors are much smaller than the integrating capacitors the time constants are almost halved. A final advantage to differencing-

input integrators is a reduction in error from finite op amp DC gain. Integrator error due to finite gain varies inversely with β and is therefore reduced with the differencing-input circuit.

Other considerations are important. For example, the inherent blocking of common-mode signals by the differencing inputs can, in principle, improve both common-mode and power-supply rejection. Also, for the two switched-capacitors in the main loop of a biquad, moderate capacitor ratios are typical. The reduced sizes are thus beneficial, diminishing chip area and op amp loading. Wherever small ratios are needed, however, the halving of capacitor sizes doubles the capacitor spread. In high Q filters further reduction in certain capacitor sizes (input and damping capacitors) cannot be tolerated. In such cases, conventional switching can be used for the smallest switched capacitors with differencing-input switching employed everywhere else.

The final point pertaining to the differencing-input approach is that the true functional bilinear transformed circuits are possible [25],[26]. Unfortunately, these circuits require both op amps to be interconnected in a loop on one phase; this degrades settling time, making them less practical for high-frequency application. For the bilinear transform to apply, differencing-input switching must be applied to all switched capacitors. Such circuits are thus ruled out for high Q filters.

The alternatives among differential biquads are summarized in the following table and shown in Figs. 6.5-6.7. Biquad B is not shown but is identical to C with the substitution of noninverting integrators.

Fig. 6.5 Biquad A: A single-ended SC filter.

Fig. 6.6 Biquad C: A differential SC filter using inverting integrators

Fig. 6.7 Biquad D: A differential SC filter using differencing-input integrators.

Biquad A	1 Inverting & 1 Noninverting SC integrator
Biquad B	2 Noninverting SC integrators
Biquad C	2 Inverting SC integrators
Biquad D	2 Differencing-input SC integrators

Table 6.1 Biquad alternatives for differential SC filters.

6.5 Finite Op Amp Bandwidth Effects on the Differential SC Biquad Alternatives

In this section the amenability of the four biquad options for high-frequency filtering is examined. Two approaches are taken for this comparison: an analytical approach using the results of Section 6.2, and a computer analysis based on the nonideal SC network simulator, NISCAP. The analytical approach is useful for a rough ranking of the biquads; however, it is inexact in some respects, since several approximations are needed to simplify the analysis. The computer approach, on the other hand, can incorporate second-order op amp models and nonzero switch resistance and provides very accurate results.

Comparison of the biquad options for finite-bandwidth, zero output impedance op amps.

Section 6.2 demonstrates that comparable errors are obtained for transconductance op amp and zero output impedance op amp biquads. For simplicity the four biquad options are therefore ranked on the basis of an analysis for zero impedance op amps. In this case interaction between coupled integrators

can be ignored and inputs can be assumed to be step functions. The four options are considered in turn.

Biquad A: One noninverting and one inverting integrator: The right-hand integrator is output sampled with no delay. Thus $m_1(\omega)$ and $\theta_1(\omega)$ are described by Eqs. (6.18) and (6.19) respectively. The left-hand integrator output is sampled after a delay, so that Eq. (6.20) applies for $m_2(\omega)$, and $\theta_2(\omega) = 0$.

The next three biquads obtain a signal inversion by a connection reversal in the balanced signal path, and they use completely symmetrical switching for the two SC integrators; as a consequence the errors are the same for both integrators in each of these cases.

Biquad B: Two noninverting SC integrators: The integrator outputs are sampled with no delay; hence Eq. (6.18) yields $m(\omega)$ and Eq. (6.19) describes $\theta(\omega)$.

Biquad C: Two inverting SC integrators: Here there is a one phase delay before output sampling; therefore Eq. (6.20) applies for $m(\omega)$, and $\theta(\omega) = 0$.

Biquad D: Two differencing input SC integrators: Analysis of this option is slightly more complicated since the differencing input samples half its signal with no delay, and the other half of its signal with a delay. The op amp being sampled is in the holding mode during the latter sampling instant, providing more settling time. This special case results in errors that are given by the average of the formulas for $m_N(\omega)$ and $m_D(\omega)$ for $m(\omega)$ and the average of $\theta_N(\omega)$ and $\theta_D(\omega)$ for $\theta(\omega)$; the resulting

error expressions are

$$m(\omega) = -1/2[1 - \beta \cos(\omega T) + \alpha]e^{-k_2} \quad (6.30)$$

$$\theta(\omega) = -1/2 \beta \sin(\omega T)e^{-k_2} \quad (6.31)$$

Performance parameters of the four biquad alternatives for a bandpass filter are compared in Table 6.2. The values of $\delta\omega/\omega_0$ and $|T_a|/|T_{id}|$ calculated from analytical formulas are compared with values obtained from complete computer simulations using NISCAP. The numerical results are similar considering the approximations used in deriving the analytical formulas. The filter used in this study has a Q of 18, a ratio of clock rate to resonant frequency of 11, a ratio of op amp bandwidth to clock rate of 2, and a gain at resonance of 6 dB.

Biquad Type	$\frac{\delta\omega_0}{\omega_0} (\%)$		$\frac{ T_a }{ T_{id} } \text{ (dB)}$	
	Analytical	NISCAP	Analytical	NISCAP
(a) Inverting and noninverting integrators	-0.67	-0.79	0.94	-1.2
(b) Noninverting integrators	-0.75	-0.90	1.98	2.48
(c) Inverting integrators	-0.59	-0.73	0.00	0.01
(d) Differencing-input integrators	-0.23	-0.27	0.46	0.61

Table 6.2. Performance comparison of the four biquad options for finite bandwidth, zero output impedance op amps

This comparison clearly demonstrates superior performance by the inverting and differencing-input integrators. The differencing-input filter has the lowest resonant frequency shift and the second lowest gain error whereas the opposite holds true for the inverting integrator biquad. The noninverting integrator biquad is the poorest performer, followed by the slightly better inverting/noninverting biquad.

NISCAP simulation of finite op amp bandwidth effects

Here the same bandpass filters are compared in more detail by means of NISCAP computer simulations. In Figs. 6.8 and 6.9 the four biquad variations are compared with respect to resonant frequency error in (a) and gain error in (b). In both cases the errors are plotted against a variable equaling the ratio of the clock rate to the unity-gain bandwidth. The case for zero output impedance op amps is shown in Fig. 6.8 and these results support the same rank ordering found in Table 6.2.

The next case compares the four options for second-order transconductance op amps with a nominal 40° phase margin, i.e. a second pole is included in the op amp model. The effect of switch resistance is also included in this simulation. Here the resistor value multiplied by the integrating capacitor value forms an RC product defined as the switch time constant. The ratio of the op amp time constant ($1/\omega_T$) to the switch time constant is taken as 0.5 in these simulations. Figure 6.9 shows the result. The preceding rank ordering for resonant frequency error now applies for gain error as well. In both respects, the differencing-input integrator biquad

Fig. 6.8

NISCAP simulation of biquad errors for finite bandwidth, zero output impedance op amps. (a) Resonant frequency error (b) Gain error.

Fig. 6.9 NISCAP simulations of biquad errors for second-order transconductance op amps and nonzero switch resistance (a) Resonant frequency error (b) Gain error.

provides superior performance in this, the most realistic simulation.

Comments on Results

A brief discussion of the foregoing results is in order. In three of the biquads, (a), (c) and (d) both op amps are interconnected on at least one of the two phases. The noninverting integrator biquad, however, allows independent unconnected settling of the two op amps. Intuitively, one would expect a single op amp to settle faster than the joint settling of two connected op amps. However, the detailed computer simulations prove that the opposite is true.

The noninverting integrator biquad must settle only one op amp at a time. Its settling time, however, is lengthened by the input capacitor which reduces the feedback factor β . In addition, the capacitive load reduces the bandwidth of this connection for transconductance op amps, and it thus contributes to a longer settling time. Another factor is that the load capacitor samples the op amp on the same phase that it samples the signal on its input capacitor. As discussed earlier, the integrator phase error is reduced considerably if the sampling is delayed until the succeeding phase.

The other two biquads require both op amps to undergo a transient simultaneously. These circuits correspond to a driver and slave connection, with the left-hand op amp being the driver. In both cases the driver has no input capacitor connected; thus its feedback factor is unity, and the settling time is consequently shortened. Also, in the action of the inverting integrator biquad, the

slave samples the driver one cycle after the driver has previously received its input signal. This minimizes the integrator phase error. This is partially true for the differencing-input biquad: half of the signal is sampled with no delay and contributes a phase error whereas the other half is sampled with a delay and therefore contributes no phase error. Together these factors make the differencing-input biquad and the inverting integrator biquad outperform the noninverting integrator biquad.

The differencing-input integrator outperforms the inverting integrator for the reasons described in Section 6.3. The favourable attributes all arise from the halving of the input capacitors. This halving increases the feedback factor and reduces the capacitive load; therefore there is an increase in bandwidth if transconductance op amps are used, and in phase margin if low output impedance op amps are used. If transconductance op amps are used there is in addition an improvement in slew-rate. Also, in all these cases RC switch time constants are reduced. Finally, the sensitivity to finite op amp gain is halved, a further benefit.

6.6 Methodology for the Compensation of High-frequency SC Filters

In this section practical considerations about the design, frequency compensation and optimization of performance of high-frequency SC filters are presented. As discussed in Chapter 4, practical, high-frequency SC filters must employ transconductance op amps. These amplifiers are suitable only for operation into a capacitive load that serves also as a compensation capacitor. This loading, provided by the capacitors in the SC filter, however, varies from phase to phase. In addition,

the feedback factors for each op amp also vary. These two factors cause the stability and settling time of each op amp to change appreciably from phase to phase. In order to ensure adequate operation despite this variability, a design methodology is presented.

First the properties of transconductance amplifiers are reviewed. The unity-gain bandwidth is

$$\omega_T = \frac{g_m}{C_L} \quad (6.32)$$

where g_m is the short circuit transconductance and C_L is the total capacitive load to ground.

The effective bandwidth in a feedback circuit is

$$\omega'_T = \omega_T \beta = \frac{g_m}{C_L} \beta; \quad 0 < \beta \leq 1. \quad (6.33)$$

Thus the bandwidth varies directly with β , and inversely with C_L . It follows that a value close to unity is preferable for β . A small value for C_L is also desirable; however, if C_L equals zero, the op amp can become unstable due to internal parasitic poles.

One note of caution: the virtual ground of an op amp does not effect a grounding of its integrating capacitor. In fact if there is no input capacitor connected, the integrating capacitor represents an open-circuit load. With an input capacitor present, the load is the series equivalent of the integrating capacitor and

the input capacitor. The virtual ground concept does not apply, however, until an op amp has completed a transient, and it cannot be invoked otherwise.

For the case of an op amp driver connected to a slave, it is complicated to assess the capacitive loading. The driving-point impedance looking into the input capacitor of the slave must be considered; this is illustrated with the aid of Fig. 6.4. For a low frequency input, the capacitor C_r appears as a purely capacitive load due to the virtual ground of op amp 2; however, at high frequency the input impedance is an open circuit. Thus, in a transient op amp 1, the driver, has a loading that varies exponentially with time from an open circuit to a capacitive load of C_r . It can be shown that the settling time for op amp 1 in such a connection is exponential of the form

$$v_{01}(t) = 1 - \frac{1}{2} e^{-\omega_T t/2} \quad (6.34)$$

where $\omega_T = g_m / C_2$.

The settling time constant for op amp 1 is effectively doubled for this configuration. This suggests using $2C_2$ as the equivalent capacitive loading on op amp 1. However, this gives a false impression of stability; therefore for the purposes of the design methodology, the virtual ground of op amp 2 is assumed.

A capacitive loading summary for each of the op amps of the four biquad options is shown in Table 6.3.

Biquad Type	Op Amp 1		Op Amp 2	
	$\phi 1$	$\phi 2$	$\phi 1$	$\phi 2$
(a) Inverting and noninverting integrators	$C_r + C'$	0	C_r	C'
(b) Noninverting integrators	$C_r + C'$	0	0	$C_r + C'$
(c) Inverting integrators	C'	C_r	C_r	C'
(d) Differencing-input integrators	$C_r/2 + C''$	$C_r/2$	$C_r/2$	$C_r/2 + C''$

where $C_r = C_{r2} = C_{r4}$, $C = C_1 = C_2$ and $C' = C_r C / (C + C_r)$ and $C'' = C_r C / (2C + C_r)$.

Table 6.3. Capacitive loading of state-variable biquads

The feedback factors of the op amps for the four biquads are shown in Table 6.4.

Biquad Type	Op Amp 1		Op Amp 2	
	ϕ_1	ϕ_2	ϕ_1	ϕ_2
(a) Inverting and noninverting integrators	β_1	1	1	β_1
(b) Noninverting integrators	β_1	1	1	β_1
(c) Inverting integrators	β_1	1	1	β_1
(d) Differencing-input integrators	β_2	1	1	β_2

where $\beta_1 = C/(C + C_r)$ and $\beta_2 = 2C/(2C + C_r)$.

Table 6.4 Feedback factors of state-variable biquads

From these two tables the relative bandwidth of each op amp is obtained by calculating β/C_L from the corresponding entry. This results in Table 6.5 which shows the relative bandwidths normalized with respect to g_m/C_r . The ranking inferred from the table is consistent with the earlier biquad ranking, showing biquads C and D to have the highest (stable) relative bandwidths.

Biquad Type	Op Amp 1		Op Amp 2	
	$\phi 1$	$\phi 2$	$\phi 1$	$\phi 2$
(a) Inverting and noninverting integrators	$\frac{1}{2 + \alpha_r}$	∞	1	1
(b) Noninverting integrators	$\frac{1}{2 + \alpha_r}$	∞	∞	$\frac{1}{2 + \alpha_r}$
(c) Inverting integrators	1	1	1	1
(d) Differencing-input integrators	$\frac{1}{1 + \alpha/4}$	2	2	$\frac{1}{1 + \alpha_r/4}$

Table 6.5 Relative op amp bandwidths of state-variable biquads.

The ∞ entries refer to the unloaded op amps and indicate a serious stability problem. Additional capacitance must be added to these op amps to provide compensation on these phases. This will as well, slow the amplifiers on the opposite phases and degrade performance. In order to avoid this, a compensation capacitor may be connected to ground on the unstable phase, through an MOS transmission gate, and floated on the stable phase. This can result in time invariant relative bandwidths for the op amps in a filter.

The three tables should be augmented to include any compensation capacitors that are added. It is also desirable to adjust compensation such that the relative

bandwidth is constant over both phases of each op amp. This allows the op amps to be designed for high bandwidth and stability in a single circuit configuration.

For example, assume the noninverting SC integrator biquad (biquad B) is compensated with switched load capacitors of value $C_R(2 + \alpha_r)$ connected to op amp 1 on phase 2 and to op amp 2 on phase 1 as shown in Fig. 6.10. The relative bandwidth for each op amp is $1/(2 + \alpha_r)$ on both phases, i.e. it is time invariant. The transconductance of each op amp and the capacitor sizes may be scaled to provide optimum performance and adequate stability for this constant loading of $C_R(2 + \alpha_r)$. The op amps may be unstable for smaller loads such as C_R , but this does not impair their operation within the compensated biquad.

6.7 Conclusions

Motivated by the desire to extend SC filtering to higher frequency, an attempt has been made to analyze and optimize the biquad: the basic SC filter building block. Various biquad options have been compared with regard to high-frequency operation, using analysis and simulation techniques that include the effects of transconductance op amps. From the numerical computations, a differencing-input biquad is predicted to have significant advantages over other alternative circuits. In the following chapter, test results from a high performance 1.25 micron CMOS test chip are used to confirm the predicted biquad comparison.

Fig. 6.10 A noninverting SC integrator biquad (Biquad B) modified for time invariant op amp bandwidths.

CHAPTER 7 HIGH-FREQUENCY SWITCHED-CAPACITOR FILTER TEST RESULTS

7.1 Introduction

This chapter presents test results on high-frequency switched-capacitor filters implemented in a VLSI 1.25 micron channel process [64]. The goal of the designs was to demonstrate the ability to do bandpass filtering at IF frequencies, such as would be required to implement radio receivers monolithically in CMOS VLSI. The short-channel process makes possible the low power, wide-band amplifiers required for such high-frequency filtering.

The three most favorable biquad options of Chapter 6 were implemented to effect a comparison of their amenability to high-frequency filtering. The measurements herein validate the analysis techniques of the preceding chapter, and they show the differencing-input integrator approach to have a significant advantage over the other alternatives. Accurate filtering of 1 MHz signals is demonstrated.

The single-ended filter (Biquad A) is included on the test chip. This allows comparisons of power-supply rejection ratio (PSRR), to be made for single-ended versus differential filters. The single-ended filter also supports operation in a clock feedthrough canceling mode as described in Appendix F [57]. The effectiveness of this circuit is likewise demonstrated herein.

High-frequency bandpass filters

The CMOS test chip contains three independent biquadratic bandpass filters with identical specifications; these correspond to biquads A, C and D of Chapter 6. Biquad A is a conventional single-ended circuit as shown in Fig. 6.5, whereas biquads C and D are fully balanced filters based on inverting integrators and differencing-input integrators, respectively and are shown in Fig. 6.6 and 6.7. A photo-micrograph of the test chip is shown in Fig. 7.1 and the specifications are listed in the following table.

Gain	2.0 (6 dB)
Q	18
f_0/f_{clock}	0.091
f_0	455 KHz
f_{clock}	5.0 MHz

Table 7.1 Filter specifications

7.2 Frequency Response Measurements

A sequence of photographs shows the frequency responses of these filters as measured with an HP network analyzer. In the photographs the lower trace shows the filter frequency response with a 1 MHz clock frequency. The upper trace shows the same filter clocked at a higher rate: either 5, 10, or 15 MHz. In most cases the

Fig. 7.1 Photomicrograph of the high-frequency SC filter test chip.

✓ curves are intentionally separated so they can be distinguished. To facilitate comparison of the lower frequency trace, which serves as a reference, with the higher frequency trace, the sweep frequency range of the network analyzer is adjusted according to the ratio of the clock frequencies. This normalizes the curves for direct comparison of high-frequency effects. SC filters, being sampled-data networks, have frequency responses that scale proportionally with their clock rates. Therefore matching the ratio of sweep frequencies of the two curves to the ratio of their clock frequencies will ideally cause the curves to overlap.

Biquad A: Single-ended filter with inverting and noninverting integrators

The single-ended filter shows the poorest performance consistent with the ranking of Chapter 6. An additional factor here is that the differential op amp used in the other two biquads has double the bandwidth and slew-rate of the single-ended circuit, as discussed in Chapter 4. Thus the comparison cannot be made here with equivalent op amps. Of course the ability to achieve twice the bandwidth with the differential current-mirror op amps makes the differential filters that much more attractive.

Figure 7.2(b) shows that the performance of biquad A with a 10 MHz clock suffers from severe Q enhancement and a drop in resonant frequency. In Fig. 7.2(a) a more accurate response is demonstrated at the lower clock rate of 5 MHz. In both figures the lower trace show the ideal response that is obtained at a 1 MHz clock rate.

Biquad C: Differential filter with inverting integrators

An improvement in performance is achieved with biquad C. Figure 7.3(a) shows this filter to suffer from Q degradation and resonant frequency shift at a 15 MHz clock rate. The response is very accurate at 5 MHz, however, as shown in Fig. 7.3(b), where the gain is within 0.03 dB.

Biquad D: Differential filter with differencing-input integrators

The best performance demonstrated by any of the filters is achieved with Biquad D. Figures 7.4(a) and (b) show it to have a reasonably accurate response at 10 and 15 MHz clock rates respectively. The detailed passband is shown at a 10 MHz clock rate in Fig. 7.5. The gain at resonance is within 0.1 dB at a 10 MHz clock rate and 2 dB at 15 MHz. Thus accurate filtering of signals in the 1 MHz range is demonstrated here.

Typical results for the three biquads are summarized in the next two figures. Error in resonant frequency is shown in Fig. 7.6 and gain error at resonance is shown in Fig. 7.7. Both sets of curves display an exponential relationship between error and clock rate. This is in agreement with the analytical and simulated results of Chapter 6 in Figs. 6.8 and 6.9. In addition, these experimental results support the rank ordering of biquad performance given in Chapter 6. These results lend credence to methods of analysis of Chapter 6, and to the simulation methods of Chapter 3.

(a)

TOP TRACE: 15 MHz CLOCK FREQUENCY
 BOTTOM TRACE: 1 MHz CLOCK FREQUENCY

(b)

TOP TRACE: 5 MHz CLOCK FREQUENCY
 BOTTOM TRACE: 1 MHz CLOCK FREQUENCY

Fig. 7.3 Biquad C: differential filter using inverting SC integrators. (a) 15 MHz clock rate (b) 5 MHz clock rate.

(a)

TOP TRACE: 10 MHz CLOCK FREQUENCY
 BOTTOM TRACE: 1 MHz CLOCK FREQUENCY

(b)

TOP TRACE: 15 MHz CLOCK FREQUENCY
 BOTTOM TRACE: 1 MHz CLOCK FREQUENCY

Fig. 7.4

Biquad D: differential filter using differencing-input SC integrators.
 (a) 10 MHz clock rate (b) 15 MHz clock rate.

Fig. 7.5 Biquad D: differential filter using differencing-input SC integrators. Detailed passband at a 10 MHz clock rate.

Fig. 7.6 Measured resonant frequency error for the test filter.

Fig. 7.7 Measured gain error for the test filters.

7.3 Power-Supply Rejection Ratio

The problems pertaining to PSRR for high frequency filters have been already been elaborated in Chapters 2 and 6. In the present section PSRR measurements on the test filters are presented.

An off chip clock circuit allows multiple measurement options; this allows flexibility to distinguish the relative strengths of the various power supply noise coupling mechanisms. PSRR measurements were taken for three cases: with the power supplies modulated on the clock circuit alone, for the power rails modulated on the test chip alone, and with the power supplies of both the chip and the clock circuit modulated. Measurements for the first case, the noisy clock, show the clock feedthrough influence on PSRR. On the other hand, measurements made on just the test chip display the effect of switch junction capacitance coupling and finite op amp PSRR on the PSRR of the filters. The combined measurement shows the overall performance of the filters.

For example, the V_{DD} PSRR of biquad C appears in Fig. 7.8(a) and the V_{SS} PSRR appears in Fig. 7.8(b). The upper trace refers to a single-ended PSRR whereas the lower trace is a balanced PSRR measurement. The results for all three filters are summarized in Table 7.2. Here the PSRR at resonance is tabulated for the three cases: noise on the clock circuit alone; noise on the test chip alone; and noise applied to both the clock and the test chip. The following Table 7.3 details the minimum PSRR over a signal frequency range of $1/50$ to $1/5$ of the clock frequency ($1/f$ noise impacts the low frequency measurements so the lower limit is

(a)

TOP: SINGLE ENDED
BOTTOM: DIFFERENTIAL

(b)

TOP: SINGLE-ENDED
BOTTOM: DIFFERENTIAL

Fig. 7.8

PSRR of biquad C with a 5 MHz clock rate. (a) V_{DD} PSRR (b) V_{SS} PSRR.

V_{DD} PSRR AT RESONANCE

V_{DD} PSRR Noise on:	BQA PSRR without canceling	BQA PSRR with canceling	BQC Single ended PSRR	BQC Differential PSRR	BQD Single ended PSRR	BQD Differential PSRR
Clock & Filter	10.4 dB	25.1 dB	27.0 dB	63.6 dB	25.1 dB	37.2 dB
Clock	24.6 dB	34.9 dB	47.8 dB	63.6 dB	39.9 dB	55.8 dB
Filter	12.0 dB	27.7 dB	28.0 dB	63.5 dB	26.0 dB	44.4 dB

 V_{SS} PSRR AT RESONANCE

V_{SS} PSRR Noise on:	BQA PSRR without canceling	BQA PSRR with canceling	BQC Single ended PSRR	BQC Differential PSRR	BQD Single ended PSRR	BQD Differential PSRR
Clock & Filter	11.7 dB	24.6 dB	27.2 dB	41.6 dB	24.9 dB	43.8 dB
Clock	31.6 dB	39.6 dB	43.6 dB	48.1 dB	46.6 dB	40.6 dB
Filter	13.5 dB	23.9 dB	22.8 dB	48.8 dB	25.8 dB	43.0 dB

Table 7.2 V_{DD} and V_{SS} PSRR at Resonance

not zero). This summarizes the measured data for a wide frequency range in contradistinction to Table 7.2, which applies only in the filter passbands.

MINIMUM V_{DD} PSRR

V_{DD} PSRR Noise on:	BQA PSRR without canceling	BQA PSRR with canceling	BQC Single ended PSRR	BQC Differential PSRR	BQD Single ended PSRR	BQD Differential PSRR
Clock & Filter	6 dB	19 dB	-8 dB	26 dB	-10 dB	21 dB
Clock	19 dB	25 dB	11 dB	36 dB	7 dB	34 dB
Filter	8 dB	20 dB	-7 dB	27 dB	-9 dB	23 dB

MINIMUM V_{SS} PSRR

V_{DD} PSRR Noise on:	BQA PSRR without canceling	BQA PSRR with canceling	BQC Single ended PSRR	BQC Differential PSRR	BQD Single ended PSRR	BQD Differential PSRR
Clock & Filter	7 dB	17 dB	-8 dB	28 dB	-11 dB	29 dB
Clock	20 dB	26 dB	10 dB	37 dB	7 dB	33 dB
Filter	9 dB	21 dB	-13 dB	27 dB	-15 dB	25 dB

Table 7.3 Minimum V_{DD} and V_{SS} PSRR for
Signal Frequencies between $1/50$ to $1/5$ of the Clock Frequency

Discussion of PSRR measurements

From the data of the two tables it is readily apparent that the levels of PSRR due to the test chip itself are much poorer than those due to the clock circuit. This means that switch junction capacitive coupling and finite op amp PSRR are the most significant degraders of the PSRR of this circuit. The improvement of PSRR for differential operation is readily apparent as well. In all cases the PSRR of the differential circuits is superior to that of the single ended circuits.

Also of note is the effectiveness of the clock feedthrough canceling circuit. In the passband (noise on both the clock and the chip) V_{DD} PSRR is improved by 13.7 dB and V_{SS} PSRR is improved by 12.9 dB. In the range of $1/50$ to $1/5$ of the clock frequency, V_{DD} PSRR is enhanced by 13 dB and V_{SS} PSRR is improved by 10 dB.

One additional factor that affects the PSRR measurements is the use of N channel source followers to buffer the outputs of all the filters. These have little bearing on the positive PSRR; however, they do degrade the negative PSRR performance. The buffers are included only to facilitate characterization of the chip. Without them measurements must be taken with high impedance, low capacitance probes (eg. Pico probes) on a probe station. Therefore the actual V_{SS} PSRR performance is superior to that reported.

7.4 Conclusions

A major objective of the thesis has been to implement several high-frequency SC filters on a 1.25 micron CMOS test chip. Test results from this circuit demonstrate the viability of SC filters, implemented in short-channel technology, towards HF filtering; operation at 1 MHz frequencies has been demonstrated.

A second major goal was to develop improved circuit topologies for HF filtering. The results presented herein clearly demonstrate a major performance advantage for a new differencing-input biquad filter developed by the author. The preceding chapter used analysis and simulation techniques to predict the advantages of the

new biquad circuit. This chapter has experimentally validated this earlier work.

CHAPTER 8 CONCLUSIONS

8.1 Summary

A desire to greatly extend the upper frequency limit of monolithic switched-capacitor filters has provided the motivation for the present Ph. D. thesis. Specifically, the goal has been to achieve a frequency of operation several orders of magnitude above voiceband. To this end, detailed design considerations for high-frequency SC filters have been elaborated in the preceding chapters. At the onset of this research program several high-frequency challenges were identified and have subsequently been addressed in this thesis.

The first and foremost problem was to enable the periodic transients generated in SC networks to settle rapidly. The settling time is limited by finite op amp bandwidths and slew-rate, and by the nonzero resistance of the MOS switches. Thus considerable effort was directed toward developing high-bandwidth op amps suitable for SC networks. Recent advances in short channel technology were exploited along with innovative circuit design to realize high speed op amps and low resistance switches.

The next major high-frequency challenge was the ability to simulate the impairments of filter frequency response due to finite bandwidth elements. Existing SC simulation methods are formulated for ideal networks and were thus inadequate for this purpose. In order to determine op amp bandwidth specifications and switch resistance requirements and optimal SC circuit topologies such a simulation

capability was highly desirable. Motivated by these considerations, a new simulator called NISCAP was developed to facilitate the study of high-frequency SC networks. This simulator proved to be an invaluable tool in this work.

The final high-frequency SC challenge was to discover filter topologies with low sensitivity to finite bandwidth effects. To this end, an effort was made to optimize the SC biquad. These results are extendible beyond the context of second-order filters, since the biquad is the basic building block of most higher-order filters. Through extensive analysis and simulations using the new nonideal SC simulation tool, a superior circuit was developed. Simulation and results from a test circuit confirm that a differencing-input integrator based biquad filter will have a major performance advantage.

These challenges were dealt with in the preceding chapters. After an introduction to the thesis in Chapter 1, the general high-frequency considerations were elaborated in Chapter 2. This included discussion of the desirability of short-channel MOS circuitry; The noise behavior and power supply rejection of SC circuits; the bandwidth and power dissipation considerations; and the performance limitations due to finite bandwidth op amps. Chapter 3 presented a new computer-aided analysis technique for nonideal linear SC networks. This program, called NISCAP, provides frequency domain analysis that includes the effects of nonideal elements such as high-order finite bandwidth op amps and switch resistance. NISCAP used a novel and simple approach whereby a sequence of time domain transient analysis are performed on the SC network to generate coefficients

for frequency domain analysis. This automatically handles nonideal networks of arbitrary complexity. Chapter 4 describes op amp design for high-frequency SC applications. It focuses on current mirroring and current steering transconductance op amps. Test results are presented for both single-ended and balanced amplifiers with bandwidths up to 100 MHz.

For driving resistive loads and off-chip circuitry, other op amps are needed. In Chapter 5 internally compensated op amps with improved AC PSRR are presented along with analysis and test results. These form the basis of a low impedance wideband buffer amplifier that is also described.

Biquad alternatives for high-frequency SC filters are extensively compared in Chapter 6. Analysis, techniques and simulation with NISCAP are used to extensively assess the performance of various single-ended and differential biquad options. Comparison is made for both low impedance and infinite impedance (transconductance) op amps.

A major objective of the thesis has been to physically implement several high-frequency switched-capacitor filters on a CMOS 1.25 micron test chip. Part of the objective was to compare the performance of several biquad filter designs with a view to testing the theoretical considerations presented herein. Another part was to demonstrate experimentally, the successful achievement of filtering at frequencies several orders of magnitude above voiceband. The chip design and the measurements therewith are presented in Chapter 7. The measurements demonstrate high-frequency bandpass filtering of 1 MHz signals and validate the

227-2
results of Chapter 6. A differencing-input biquad is shown to have significant performance advantages over other circuits.

8.2 Suggestions for Future Work

Significant progress towards high-frequency SC filtering has been made in the present work. Due to the broadness of the topic, and the host of potential important applications, further research in this area is indicated. To this end, recommendations of beneficial related topics for future research are made in this final section.

Op Amps

Op amp circuits for high-frequency SC filters are now fairly mature. No significant performance advance is anticipated for circuits implemented in current CMOS technology. It is expected that maximum op amp gain-bandwidth products will remain limited to $1/10$ of the single device f_T of any given process. Thus, most further performance improvements will be due to advances in short-channel technology from the present 1.25 micron levels.

SC Network Simulation

It is felt that the simulation of nonideal SC networks is still a fruitful area for research. It is very important to be able to simulate nonideal performance in order to develop high-frequency filters. The NISCAP CAD tool could be enhanced to include the complete spectral analysis of arbitrary networks, i.e. to include the

effects of continuous inputs, etc. It is conjectured that doing this in a numerically efficient manner would represent a formidable challenge.

High-Frequency Filter Design

Considerable effort has been directed here at optimizing biquad sections. It would thus be worthwhile to design high-order HF filters using the improved biquad structures that have been developed. High-order filters using differencing-input integrator biquads should be pursued. In addition high-order filters using time invariant loading techniques are worth exploring.

Some unanswered questions are worth pursuing. In SC ladder filters that realize finite transmission zeroes, continuous (unswitched) coupling capacitors are used. These capacitors inevitably connect several op amps together and thereby lengthen settling times. It would thus be worthwhile to develop, if possible, filters that realize transmission zeroes without using continuous coupling. Choi and Kaneshiro [21] found a method to transform switched coupling paths to continuous ones, so the opposite transformation is potentially feasible. It is expected that additional op amps would be required but the result should be beneficial.

Other more unconventional approaches should also be explored. For example it might be possible to exploit parallelism or pipelining to achieve higher-speed filtering at the expense of additional hardware. Another possibility is to develop filters that are optimized to meet their frequency specifications without completely settling their transients. It is conceivable that a reference oscillator using

incomplete settling SC integrators could be phase or frequency locked to a crystal in order to automatically tune a filter using similar integrators.

Appendix A Transient Response of Finite Bandwidth SC Integrators

A.1 Zero output impedance finite bandwidth op amps.

The transient response of an SC integrator (Fig. A.1) with finite bandwidth zero output impedance op amps is derived herein. A first order differential equation is used to describe the op amp in the form

$$\frac{dv_2(t)}{dt} = -\omega_T v_1(t) \quad (A.1)$$

where ω_T is the op amp unity gain bandwidth.

This can be Laplace transformed to give

$$sV_2(s) - v_2(0^-) = -\omega_T V_1(s) \quad (A.2)$$

The application of Kirchhoff's current law (KCL) at node 1 of the circuit during phase 2 results in

$$sC_2V_2(s) = s(C_1 + C_2)V_1(s) + C_2v_2^b(0^-) - C_1v_1(0^-) \quad (A.3)$$

In this notation the superscript b denotes a branch voltage, and the time $t = 0^-$ corresponds in this case to the instant just prior to the start of phase 2. Thus $v_2^b(0^-)$ is the initial condition on capacitor C_2 . Solving Eqs. (A.2) and (A.3) simultaneously; taking the inverse Laplace transforms, and setting $v_2^b(0^-) = v_2(0^-) - (v_1(0^-))$, gives the following transient responses during phase 2:

Fig. A.1 Stray free inverting switched-capacitor integrator.

$$v_1(t) = \beta e^{-\omega_T \beta t} v_1(0^-) + \alpha e^{-\omega_T \beta t} v_1(0^-) \quad (A.4)$$

$$v_2(t) = v_2(0^-) - (1 - e^{-\omega_T \beta t}) v_1(0^-) - \frac{C_1}{C_2} (1 - e^{-\omega_T \beta t}) v_1(0^-) \quad (A.5)$$

where $\alpha = C_1/(C_1 + C_2)$ and $\beta = C_2/(C_1 + C_2)$.

During phase one the following node equation applies at node 1:

$$s V_1(s) + v_2^b(0^-) = s V_2(s) \quad (A.6)$$

In this case time $t = 0^-$ represents the instant just prior to the start of phase 1.

Solving Eqs. (A.2) and (A.6) simultaneously and taking the inverse transforms gives the transient responses

$$v_1(t) = e^{-\omega_T t} v_1(0^-) \quad (A.7)$$

$$v_2(t) = v_2(0^-) - (1 - e^{-\omega_T t}) v_1(0^-) \quad (A.8)$$

A.2 Finite bandwidth transconductance op amp.

In this section the transient response for the SC integrator of Fig. 1 employing finite bandwidth infinite output impedance transconductance op amps is analyzed.

Here an amplifier with transconductance g_m is assumed, with an SC load C_3 connected on phase 2. During phase 2 Eq. (A.3) still applies at node 1. Application of KCL at node 2 results in

$$(sC_2 - g_m)V_1(s) = sC_2V_2(s) - C_2v_2^b(0^-) \quad (A.9)$$

Solving (A.3) and (A.9) simultaneously and taking the inverse transforms results in

$$v_1(t) = e^{-\omega_{T2}\beta t} v_1(0^-) \quad (A.10)$$

$$v_2(t) = v_2(0^-) - v_1(0^-) - \frac{C_1}{C_2} \left(1 - \frac{1}{\alpha} e^{-\omega_{T2}\beta t}\right) v_1(0^-) \quad (A.11)$$

where

$$\omega_{T2} = g_m / C_{L2} \text{ and } C_{L2} = C_1 C_2 / (C_1 + C_2)$$

Therefore $\omega_{T2}\beta = g_m / C_1$. During phase one, application of KCL at node 2 gives

$$(sC_2 + g_m)V_1(s) + C_2 v_2^b(0^-) = s(C_2 + C_3)V_2(s) \quad (A.12)$$

The transient response can be determined from Eqs. (A.6) and (A.13). The result is

$$v_1(t) = e^{-\omega_{T1}t} [v_1(0^-) + v_2(0^-)] \quad (A.13)$$

$$v_2(t) = - (1 - e^{-\omega_{T1}t}) [v_1(0^-) - v_2(0^-)] \quad (A.14)$$

where $\omega_{T1} = g_m / C_3$.

Appendix B Equation Formulation for Finite Bandwidth SC Integrators

In this appendix a general formulation of equations is developed that can be applied to the analysis of SC integrators with finite bandwidth op amp; they may have either zero or infinite impedance outputs. The analysis has been simplified for the case of two phase networks. The solution is restricted to the discrete time system associated with an arbitrary nonideal SC network; there is a further restriction of sample and held inputs. A final important point is that all ideal switches are eliminated on each phase and, instead, compact subnetworks are analyzed.

B.1 Formulation of Equations

At the end of a phase, each node voltage is an algebraic sum of the node voltages at the end of the previous phase along with a sum of the input voltages applied during the phase:

$$\begin{aligned} v_1 &= C_1 v_2 + g_1 w_1 && \text{for phase 1} \\ v_2 &= C_2 v_1 + g_2 w_2 && \text{for phase 2} \end{aligned} \tag{B.1}$$

where v_k is the node voltage vector on phase k , the C_k matrix relates the initial node voltages to the final node voltages on phase k , vector g_k does the same for input signals, and vector w_k is the value of the input on the k^{th} phase.

B.2 Frequency response of the discrete time system

The z-transform of Eq. (B.1) is taken in order to determine the frequency response of the discrete system of equations that describe the network.

$$\begin{bmatrix} 1 & -C_1 \\ -C_2 & zI \end{bmatrix} \begin{bmatrix} V_1(z) \\ V_2(z) \end{bmatrix} = \begin{bmatrix} g_1 \\ g_2 z^{1/2} \end{bmatrix} \quad (B.2)$$

Herein w_k has been set to unity so that V_k corresponds to the transfer functions. Equation (B.2) can be solved for $V_2(z)$ by performing block Gaussian elimination; the result is

$$[zI - C_2 C_1] V_2(z) = g_2 z^{1/2} + C_2 g_1 \quad (B.3)$$

This equation can be solved to yield the desired transfer function, $T(z) = V_2(z)$. The solution for $V_2(z)$ suffices for the case of sample and held inputs with a holding duration of T .

In order to apply this result to the SC integrators, the elements of the C_k and g_k matrices vectors are taken from the results of the transient analyses given in Appendix A. The error factor is determined by factoring out the ideal transfer function from the solution of Eq. B.3.

Appendix C Analysis of Finite Bandwidth SC Integrators

C.1 SC integrators using zero output impedance finite bandwidth op amps

The preceding analysis technique is applied here to the SC integrator; the objective is to determine the transfer function resulting from the use of finite bandwidth zero output impedance op amps. Both noninverting and inverting integrator transfer functions are developed in a form consisting of the product of the ideal response and an error factor. It turns out that only two different error factors exist. The error factor obtained in a particular case depends only on whether or not there is a phase delay in sampling the integrator output.

The analysis of the transient responses of the inverting integrator in Appendix A provides the specific entries in the C_1 , C_2 matrices and the g_1 and g_2 vectors. From Eqs. (A.7) and (A.8),

$$C_1 = \begin{bmatrix} e^{-k_1} & 0 & 0 \\ -(1-e^{-k_1}) & 1 & 0 \end{bmatrix} \quad (C.1)$$

$$-g_1 = [0 \ 0]^T \quad (C.2)$$

where $k_1 = \omega_T T/2$ and from Eqs. (A.4) and (A.5),

$$C_2 = \begin{bmatrix} \beta e^{-k_2} & 0 \\ -(1-e^{-k_2}) & 1 \\ 0 & 0 \end{bmatrix} \quad (C.3)$$

$$g_2 = \begin{bmatrix} \alpha e^{-k_2} \\ -\frac{C_1}{C_2}(1-e^{-k_2}) \\ 1 \end{bmatrix} \quad (C.4)$$

where $k_2 = \omega_T \beta T / 2$

Next the product $C_2 C_1$ is formed

$$C_2 C_1 = \begin{bmatrix} \beta e^{-(k_1+k_2)} & 0 & 0 \\ -(1-e^{-(k_1+k_2)}) & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix} \quad (C.5)$$

Eq. B.3 can now be evaluated

$$\begin{bmatrix} z - \beta e^{-(k_1+k_2)} & 0 & 0 \\ (1-e^{-(k_1+k_2)}) & z-1 & 0 \\ 0 & 0 & z \end{bmatrix} \begin{bmatrix} V_{2,1}(z) \\ V_{2,2}(z) \\ V_{2,3}(z) \end{bmatrix} = \begin{bmatrix} \alpha e^{-k_2} \\ -\frac{C_1}{C_2}(1-e^{-k_2}) \\ 1 \end{bmatrix} z^{1/2} \quad (C.6)$$

where the first subscript of V is the phase and the second is the node number.

Solving for $V_{2,2}(z)$, which is the output the integrator at the end of phase 2, results in the transfer function

$$\frac{V_o(z)}{V_i(z)} = \frac{-(C_1/C_2)z^{1/2}}{z-1} \left[1-e^{-k_2} + \frac{\beta(1-e^{-(k_1+k_2)})e^{-k_2}}{z - \beta e^{-(k_1+k_2)}} \right] \quad (C.7)$$

where $V_o(z) = V_{2,2}(z)$.

Typically terms with the factor $e^{-(k_1+k_2)}$ are insignificant when compared with

terms with the e^{-k_2} factor. On ignoring the $e^{-(k_1+k_2)}$ terms this simplifies to

$$\frac{V_o(z)}{V_i(z)} \cong \frac{-(C_1/C_2)z^{1/2}}{z-1} \left[1 - e^{-k_2} + z^{-1} \beta e^{-k_2} \right] \quad (C.8)$$

The error factor for this case is

$$E_N \cong 1 - e^{-k_2} + z^{-1} \beta e^{-k_2} \quad (C.9)$$

The other error factor is obtained when sampling is delayed by one phase; therefore an inverting integrator that samples on phase 1 and is sampled on phase two is analyzed. Proceeding in a similar manner to the previous analysis for the present case results in

$$\begin{bmatrix} z - \beta e^{-(k_1+k_2)} & 0 \\ (1 - \alpha e^{-k_2} - \beta e^{-(k_1+k_2)}) & z-1 \end{bmatrix} \begin{bmatrix} V_{2,1}(z) \\ V_{2,2}(z) \end{bmatrix} = \begin{bmatrix} \alpha e^{-k_1+k_2} \\ -\frac{C_2}{C_1} (1 - \alpha e^{-k_2} - \beta e^{-(k_1+k_2)}) \end{bmatrix} \quad (C.10)$$

Solving for the output at the end of phase 2 yields.

$$\frac{V_o(z)}{V_i(z)} = \frac{-(C_2/C_1)}{z-1} \left[1 - \alpha e^{-k_2} - \beta e^{-(k_1+k_2)} \right] \left[1 + \frac{\beta e^{-(k_1+k_2)}}{z - \beta e^{-(k_1+k_2)}} \right] \quad (C.11)$$

Ignoring the $e^{-(k_1+k_2)}$ terms as before simplifies the transfer function to

$$\frac{V_o(z)}{V_i(z)} \cong \frac{C_2/C_1}{z-1} (1 - \alpha e^{-k_2}) \quad (C.12)$$

Here again we are unconcerned about the delay associated with the input sampled and held signal. Its only effect is the possible addition of a $z^{1/2}$ factor to the ideal response. The second type of error factor is obtained in this case:

$$E_D \cong 1 - \alpha e^{-k_2} \quad (C.13)$$

Identical pairs of error factors (C.9) and (C.13) are also obtained for noninverting integrators. Which of the two applies depends only on whether or not sampling of the output is delayed by one phase.

C.2 SC integrators using finite bandwidth transconductance op amps.

The analysis of transconductance op amp integrators proceeds in a similar manner. The C_1 matrix is formed from Eqs. (A.14) and (A.15) with $g_1 = [0 \ 0]^T$, and C_2 and g_2 are found from Eqs. (A.10) and (A.11). After computing $C_2 C_1$ an equation in the form of B.3 is obtained:

$$\begin{bmatrix} z & 0 & 0 \\ 1 & z-1 & 0 \\ 0 & 0 & z \end{bmatrix} \begin{bmatrix} V_{2,1}(z) \\ V_{2,2}(z) \\ V_{2,3}(z) \end{bmatrix} = \begin{bmatrix} e^{-k_2} \\ -C_1/C_2(1 - \frac{1}{\alpha} e^{-k_2}) \end{bmatrix} z^{1/2} \quad (C.14)$$

The solution for the output of the integrator at the end of phase two is

$$\frac{V_o(z)}{V_i(z)} = \frac{-(C_1/C_2)z^{1/2}}{z-1} \left[1 - \frac{1}{\alpha} e^{-k_2} + z^{-1} \frac{C_2}{C_1} e^{-k_2} \right] \quad (C.15)$$

Thus the first error factor for the transconductance op amp integrator is

$$E_N = 1 - \frac{1}{\alpha} e^{-k_2} + z^{-1} \frac{C_2}{C_1} e^{-k_2} \quad (C.16)$$

The other error is obtained with a delay in sampling the output. As before, the inverting integrator that samples on phase 1 and is sampled on phase 2 is considered. After computing $C_2 C_1$ and $C_2 g_1$, an equation in the form of B.3 is

obtained:

$$\begin{bmatrix} z & 0 \\ 1 & z-1 \end{bmatrix} \begin{bmatrix} V_{2,1}(z) \\ V_{2,2}(z) \end{bmatrix} = \begin{bmatrix} e^{-(k_1+k_2)} \\ \frac{-C_1}{C_2}(1 - e^{-k_2}) + e^{-(k_1+k_2)} \end{bmatrix} \quad (C.17)$$

The solution is

$$\frac{V_o(z)}{V_i(z)} = \frac{-C_1/C_2}{z-1} \left[1 - e^{-k_2} - (1 - z^{-1}) \frac{C_2}{C_1} e^{-(k_1+k_2)} \right] \quad (C.18)$$

This is simplified as before by dropping the $e^{-(k_1+k_2)}$ terms, resulting in

$$\frac{V_o(z)}{V_i(z)} \cong \frac{-C_1/C_2}{z-1} [1 - e^{-k_2}] \quad (C.19)$$

The error factor here is

$$E_D \cong 1 - e^{-k_2} \quad (C.20)$$

Appendix D. Analysis of a Cascode Amplifier

This appendix summarizes the details of the derivation of the output impedance, gain, pole locations, and gain-bandwidth product for the cascode amplifier of Fig. D.1(a).

Output Impedance

The MOSFET's of Fig. D.1 (a) are replaced by their respective equivalent circuits in (b) in order to facilitate the analysis. For purposes of determining the dynamic output impedance the contribution of the current source of M_1 is a constant, and, it is therefore excluded. The transconductance G_{m2} is used for M_2 , where $G_{m2} = g_{m2} + g_{mb2}$ and g_{mb2} is the substrate transconductance of M_2 ; i.e. g_{mb2} is the transconductance caused by body effect, dI_{DS}/dV_{BS} . In the following derivation output conductance $g_o = 1/r_o$ is used to simplify the analysis. Taking nodal equations at nodes one and two:

$$(1) \quad i_o = (v_o - v_x)g_{o2} - G_{m2}v_x$$

$$(2) \quad (v_o - v_x)g_{o2} - G_{m2}v_x - g_{o1}v_x = 0$$

Solving these two equations simultaneously results in

$$R_o = v_o/i_o = (G_{m2} + g_{o1} + g_{o2})/(g_{o1} + g_{o2})$$

In saturation, $G_{m2} \gg g_{o1} + g_{o2}$;

Fig. D.1 Analysis of a cascode amplifier. (a) Cascode circuit (b) Small-signal equivalent circuit for determining output impedance.

therefore, $R_o = (1/g_{o1})G_{m2}/g_{o2} = r_{o1}A_2$,

where $A_2 = G_{m2}/g_{o2}$, the gain of transistor M_2 .

Gain

The gain is the small-signal output current multiplied by the output impedance of the cascode:

$$v_o/v_i = g_{m1}(r_{o1}A_2) = A_1A_2 \quad \text{where } A_1 = g_{m1}r_{o1} \quad (D.1)$$

Lower Pole

The low-frequency pole is formed by the load capacitor C_L and the output impedance of the cascode; its radian frequency is:

$$\omega_L = 1/(A_2r_{o1}C_L) \quad (D.2)$$

Upper Pole

The high-frequency pole is formed by the output impedance of node two and the parasitic capacitance C_P . The impedance looking into the source of common gate device M_2 is the reciprocal of its transconductance.

Therefore the radian frequency is:

$$\omega_H = G_{m2}/C_P \quad (D.3)$$

Gain-Bandwidth Product

The gain-bandwidth product (GBW) is simply the product of the open-loop gain, and the dominant pole:

$$\text{GBW} = A_1 A_2 / (A_2 r_{o1} C_L) = g_{m1} / C_L \quad (10.4)$$

In the development of Table 4.1 in Chapter 4, the assumption that G_{m2} is approximately equal g_{m2} has been made.

Appendix E: Analysis of the Stacked Current Mirror

This appendix summarizes the details of the analysis of the stacked current mirror shown in Fig. E.1. This type of mirror is used extensively in the high-frequency current mirror amplifier described in chapter 4. The equivalent circuit of Fig. E.2 is formed by replacing the four transistors by their small-signal equivalent circuits. To extract meaningful results the circuit is simplified by eliminating components of minor significance. First it is assumed that intrinsic MOSFET capacitances, such as the gate-source capacitances, are dominant over extrinsic capacitances, such as drain and source junction capacitances. This eliminates C_4 and C_5 ; C_4 represents the capacitance of the drain junction of M_1 , and C_5 represents the capacitance of the source junction of M_2 and the drain junction of M_4 . The latter is often made a common diffusion to minimize the capacitance.

Next g_{o2} and g_{o4} , the drain source conductances of M_2 and M_4 , are discarded; they are much smaller than the transconductances g_{m2} and g_{m4} that they shunt. These conductances must be included to determine the output impedance, but they are not significant for the frequency response.

The current equations at nodes 1-4 are:

Fig. E.1 Stacked current mirror.

Fig. E.2 Small signal equivalent circuit of the stacked current mirror.

$$(1) I_B + (v_2 - v_1)(g_{m1} + sC_1) + (v_4 - v_1)sC_2 = 0$$

$$(2) (v_1 - v_2)(g_{m1} + sC_1) - v_2(g_{m3} + sC_3) = 0$$

$$(3) I_o = g_{m2}(v_1 - v_4)$$

$$(4) (v_1 - v_4)(g_{m2} + sC_2) - g_{m4}V_2 = 0$$

solving these equations simultaneously results in

$$\frac{I_o}{I_B} = \frac{g_{m2}g_{m4}}{s^2C_2C_3 + s[g_{m2}C_3 + (g_{m3} + g_{m4})C_2] + g_{m2}g_{m3}} \quad (E.1)$$

The denominator cannot be factored easily, so the parasitic poles are found by means of the quadratic root formula.

$$\omega_p = \frac{1}{2} \left(\frac{g_{m2}}{C_2} + \frac{g_{m3} + g_{m4}}{C_3} \right) \left(1 \pm \sqrt{1 - \frac{4g_{m2}g_{m3}C_2C_3}{[g_{m2}C_3 + (g_{m3} + g_{m4})C_2]^2}} \right) \quad (E.2)$$

If the stacked mirror uses identical size transistors in the upper and lower sections (M_1 matches M_3 and M_2 matches M_4), and the output is scaled to achieve an "n-fold" current gain. Then

$$g_m \triangleq g_{m1} = g_{m3}$$

$$ng_m \triangleq g_{m2} = g_{m4}$$

If only large intrinsic MOSFET capacitances are considered, then C_2 is the gate-source capacitance of M_2 , and C_3 is the gate-source of M_3 and M_4 .

Defining

$$C \triangleq C_{GS1} = C_{GS3}$$

Then

$$C_2 = nC$$

$$C_3 = (n+1)C$$

Assume further that minimum channel length transistors are used to enhance speed.

Then, defining the bandwidth of the technology as $\omega_T = g_m/C_G$ (rad/sec), the parasitic pole radian frequencies are found to be

$$\omega_{pl} = \omega_T(1 - \sqrt{1-1/(n+1)}) \quad (E.3)$$

$$\omega_{ph} = \omega_T(1 + \sqrt{1-1/(n+1)})$$

The transfer function for the mirror is

$$H(s) = \frac{I_o(s)}{I_B(s)} = \frac{n}{(s\tau_{pl}+1)(s\tau_{ph}+1)} \quad (E.4)$$

where $\tau_{pl} = 1/\omega_{pl}$ and $\tau_{ph} = 1/\omega_{ph}$. This is characterized by two poles, one below the fundamental bandwidth of the technology and the other above it. The parasitic pole frequencies, normalized with respect to ω_T , are plotted versus current gain "n" in Fig. E.3. For current gains of one or greater, the spread in pole frequencies is quite large, and the frequency response can be well approximated by a single-pole model. The magnitude-squared denominator polynomial of Eq. (E.4) is

$$|D(j\omega)|^2 = 1 + 2(n+1)(2n+1)u^2 + (n+1)^2u^4 \quad (E.5)$$

where $u = \omega/\omega_T$. For frequencies well below the technology bandwidth this is

$$|D(j\omega)|^2 \cong 1 + 2(n+1)(2n+1)u^2 : u \ll 1 \quad (E.6)$$

Fig. E.3 Normalized parasitic pole frequencies as a function of current gain.

so the transfer function is

$$H(s) \cong \frac{n}{(s\tau_p + 1)} \quad (E.7)$$

where $\tau_p = \sqrt{2(n+1)(2n+1)}$ and $\omega_p = 1/\tau_p$.

Appendix F Clock-Feedthrough Cancellation in Single-Ended SC Circuits

This appendix describes a general circuit approach that greatly improves the PSRR of any single-ended active SC network. The basic idea is to degenerate a differential circuit into an equivalent single-ended circuit by grounding one of its balanced signal paths, as shown in Fig. F.1. The resultant single-ended circuit has the insensitivity to feedthrough of a balanced circuit but with a single-ended signal path. The duplicate switches and capacitors connected to the input of the noninverting op amp inject comparable noise signals to the elements in the signal path. These, being common-mode signals, are rejected by the amplifier.

A more rigorous explanation of the cancellation method follows. First, it is assumed that power-supply noise is coupled only through the following: the parasitic gate capacitances of the MOS switches; the transistors drain and source junction capacitances; and the capacitance to the bottom plate of all intended circuit capacitors. It is further assumed that all passive SC circuitry including the aforementioned parasitics can be treated as a passive linear RC network. The implications of the assumption of linearity are discussed later.

An SC integrator can now be represented as an op amp plus a passive linear network as shown in Fig. F.2. Here the network N_1 represents all intended capacitors and switches and, in addition, all parasitic coupling to a power supply.

The input V_N represents the noisy power-supply signal that couples through the parasitics. Network N_2 is an unknown network whose composition is to be

Fig. F.1 Single-ended biquad filter with clock-feedthrough cancellation circuitry.

Fig. F.2 Simplified circuit that explains clock-feedthrough cancellation.

determined.

Normally, in a single-ended circuit, N_2 is a direct connection to ground for the noninverting op amp input.

The transfer function of the noise to the output is

$$\frac{V_0(s)}{V_N(s)} = \frac{T_{24}(s) - T_{14}(s)}{T_{13}(s) + 1/A(s)} \quad (F.1)$$

where

$$T_{13}(s) = \left. \frac{V_1(s)}{V_3(s)} \right|_{V_4(s)=0}, \quad T_{14}(s) = \left. \frac{V_1(s)}{V_4(s)} \right|_{V_3(s)=0}$$

for network N_1 and

$$T_{24}(s) = \frac{V_2(s)}{V_4(s)}$$

for network N_2 . Noise transmission is completely eliminated if $T_{24}(s) = T_{14}(s)$.

This is achieved by simply making network N_2 identical to N_1 , and grounding its unused node.

Complete cancellation is achievable in the linear case. However, the channel charge, intrinsic capacitance and junction capacitance of MOS transistors adjacent to signal inputs are nonlinear functions of input voltage. Thus the dummy network N_2 cannot exactly match N_1 since some elements vary nonlinearly with input signal. Insofar as this is true, cancellation is impaired.

REFERENCES

- [1] D. A. Hodges, P. R. Gray and R. W. Broderon, "The potential of MOS technologies for analog integrated circuits," IEEE J. Solid State Circuits, vol. SC-13, pp. 285-294, June 1978.
- [2] J. T. Caves, M. A. Copeland, C. F. Rahim, and S. D. Rosenbaum, "Sampled analog filtering using switched capacitors as resistor equivalents," IEEE J. Solid State Circuits, vol. SC-12, pp. 592-599, Dec. 1977.
- [3] B. J. Hosticka, R. W. Broderon, and P. R. Gray, "MOS sampled data recursive filters using switched integrators," IEEE J. Solid State Circuits, vol. SC-12, pp. 600-608, Dec. 1977.
- [4] B. K. Ahuja, D. G. Marsh and M. R. Dwarakanth, "A single-chip CMOS PCM CODEC with filters," in Proc. Int. Solid State Circuits Conf., pp. 242-243, New York, N.Y., Feb. 1981.
- [5] N. Holte and S. Stuefflotten, "A new digital echo canceller for two-wire subscriber lines," in Dig. Tech. Papers, 1982 National Telecommunications Conf., Houston, Texas, Dec. 1980.
- [6] K. Martin, "Improved circuits for the realization of switched-capacitor filters," IEEE Trans. Circuit Syst., vol. CAS-27, pp. 237-244, Apr. 1980.
- [7] R. H. Denard et al., "Design of ion implanted MOSFET's with very small

dimensions," IEEE J. Solid State Circuits, vol. SC-9, pp. 256-268, Oct. 1974.

- [8] S. Wong and C. A. T. Salama, "Scaling of MOS analog circuits for VLSI applications," in Dig. Tech. Papers, 1982 Symp. VLSI Technology, Tokyo, Japan, Sept. 1982.
- [9] P. R. Gray, "Basic MOS operational amplifier design-An overview," in Analog MOS integrated circuits, New York: IEEE Press, pp. 28-49, 1980.
- [10] D. Frohman-Bentchkowsky and A. S. Grove, "The output conductance of MOST's in saturation," IEEE Trans. Electron Devices, vol. ED-16, pp. 108-115, Jan. 1969.
- [11] R. R. Troutman, "VLSI limitations from drain-induced barrier lowering," IEEE J. Solid State Circuits, vol. SC-14, pp. 383-391, Apr. 1979.
- [12] J. Schreiffer, "Effective carrier mobility in surface space charge layers," Physics Review, vol. 97, pp. 641-646, 1955.
- [13] K. C. Hsieh, P. R. Gray, D. Sendowicz, D. G. Messerschmitt, "A low-noise chopper-stabilized differential switched-capacitor filtering technique," IEEE J. Solid State Circuits, vol. SC-16, pp. 708-715, Dec. 1981.
- [14] K. Lam, M. Eng. Thesis, Carleton University, Aug. 1983.
- [15] C. A. Gobet and A. Knob, "Noise analysis of switched capacitor networks," in Proc. Int. Symp. Circuits Syst., Chicago, IL, Apr. 1981.
- [16] J. H. Fisher, "Noise sources and calculation techniques for switched capacitor

- filters," *IEEE J. Solid State Circuits*, vol. SC-17, pp. 742-752, Aug. 1982.
- [17] J. C. Bertails, "Low frequency considerations for MOS amplifier design," *IEEE J. Solid State Circuits*, vol. SC-14, pp. 773-776, Aug. 1979.
- [18] M. H. White, D. R. Lampe, F. C. Blaha, and I. A. Mack, "Characterization of surface channel CCD image arrays at low light levels," *IEEE J. Solid State Circuits*, vol. SC-9, pp. 1-12, Feb. 1974.
- [19] R. W. Broderon, P. R. Gray, and D. A. Hodges, "MOS switched capacitor filters," *Proc. IEEE*, vol. 67, no. 1, pp. 61-74, Jan. 1979.
- [20] T. C. Choi, R. T. Kaneshiro, R. W. Broderon and P. R. Gray, "High frequency CMOS switched capacitor filters for communications," in *Proc. IEEE Int. Solid State Circuit Conference*, pp. 246-247, New York, N.Y., Feb. 1983.
- [21] T. C. Choi, R. T. Kaneshiro, R. W. Broderon, P. R. Gray, W. B. Jett, and M. Wilcox, "High-frequency CMOS switched-capacitor filters for Communications Application," *IEEE J. Solid-State Circuits*, vol. SC-18, No. 6, pp. 652-664, Dec. 1983.
- [22] M. Milkovic, "70 MHz CMOS Operational Amplifiers Using Stacked Current Mirrors," CRD TIS Report No. 84CRD123; May 1984; General Electric Research and Development, Schenectady, N.Y. 12301.
- [23] M. Milkovic, "VLSI High Frequency CMOS Operational Amplifiers for Communications Applications," presented at the IEEE 27th Midwest

Symposium on Circuits and Systems, Morgantown, W. Va., June 1984.

- [24] L. T. Bruton, "Low sensitivity digital ladder filters," IEEE Trans. on Circuits and Systems, vol. CAS-222, no. 3, pp. 168-176, Mar. 1975.
- [25] P. Gillingham, "Switched capacitor circuits for VLSI, a design study," M. Eng. Thesis, Carleton Univ., Dec. 1982.
- [26] D. Senderowicz, S. F. Dreyer, J. H. Huggins, C. F. Rahim and C. A. Laber, "A family of differential NMOS analog circuits for a PCM CODEC filter chip," IEEE J. Solid State Circuits, vol. SC-17, pp. 1014-1023, Dec. 1982.
- [27] W. C. Black, D. J. Allstot, R. A. Reed, "A high performance low power CMOS channel filter," IEEE J. Solid State Circuits, vol. SC-15, pp. 929-938, Dec. 1980.
- [28] F. Krummenacher, "High voltage gain CMOS OTA for micropower SC filters," Electronics Letters, no. 17, pp. 160-162, 1981.
- [29] M. L. Liou, "Exact analysis of linear circuits containing periodically operated switches with applications," IEEE Trans. Circuit Theory, vol. CT-19, no. 2, pp. 146-154, Mar. 1972.
- [30] T. Strom and S. Signell, "Analysis of periodically switched linear circuits," IEEE Trans. Circuits Syst., vol. CAS-24, no. 10, pp. 531-541, Oct. 1977.
- [31] F. Brglez, "Exact nodal analysis of switched-capacitor networks with arbitrary switching sequences and general inputs-Part I," in Conf. Rec. 12th

Annual Asilomar Conf. on Circuits, Systems and Computers, pp. 679-683, Nov. 1978.

- [32] M. L. Liou, and Y. L. Kuo, "Exact analysis of switched capacitor circuits with arbitrary inputs," IEEE Trans. Circuits Syst., vol. CAS-26, no. 4, pp. 213-223, Apr. 1979.
- [33] F. Brglez, "Exact nodal analysis of switched-capacitor networks with arbitrary switching sequences and general inputs-Part II," in Proc. IEEE Int. Symp. on Circuits and Syst., pp. 748-751, July 1979.
- [34] Y. P. Tsividis, "Analysis of switched-capacitive networks," IEEE Trans. Circuits Syst., vol. CAS-26, no. 11, pp. 935-947, Nov. 1979.
- [35] H. J. DeMan, J. Rabaey, G. Arnout, and J. Vandewalle, "Practical implementation of a general computer design technique for switched capacitor circuits," IEEE J. Solid-State Circuits, vol. SC-15, No. 2, pp. 190-200, Apr. 1980.
- [36] J. Vandewalle, H. DeMan, and J. Rabaey, "Time, frequency, and z-domain modified-nodal analysis of switched-capacitor networks," IEEE Trans. Circuits Syst., vol. CAS-28, no. 3, pp. 186-195, Mar 1981.
- [37] J. Vlach, K. Singhal, and M. Vlach, "Computer oriented formulation of equations and analysis of switched-capacitor networks," IEEE Trans. Circuits Syst., vol. CAS-31, pp. 753-765, Sept. 1984.

- [38] J. Rabaey, J. Vandewalle, and H. DeMan, "On the frequency domain analysis of switched capacitor networks including all parasitics," in Proc. IEEE Int. Symp. on Circuits and Systems, pp. 868-871, Apr. 1981.
- [39] N. J. Cutland, C. Lau, and J. I. Sewell, "General computer analysis of switched-capacitor networks including non-ideal amplifiers," in Proc. IEEE Int. Symp. on Circuits and Systems, pp. 17-20, May 1982.
- [40] E. P. Rudd, and R. Schaumann, "An analysis program for switched-capacitor filters including the effects of op-amp bandwidth and switch resistance," in Proc. IEEE Int. Symp. on Circuits and Systems, pp. 13-16, May 1982.
- [41] E. Wehrhahn, "Exact analysis of periodically switched linear networks," in Proc. IEEE Int. Symp. on Circuits and Systems, pp. 884-887, Apr. 1981.
- [42] G. C. Temes, "Finite amplifier gain and bandwidth effects in switched-capacitor filters," IEEE J. Solid-State Circuits, vol. SC-15, no. 3, pp. 358-361, June 1980.
- [43] K. Martin, and A. S. Sedra, "Effects of the op amp finite gain and bandwidth on the performance of switched-capacitor filters," IEEE Trans. Circuits Syst., vol. CAS-28, no. 8, pp. 822-829, Aug. 1981.
- [44] R. L. Geiger, and E. Sanchez-Sinencio, "Operational amplifier gain bandwidth product effects on the performance of switched capacitor networks," IEEE Trans. Circuits Syst., vol. CAS-29, no. 2, pp. 96-106, Feb. 1982.

- [45] A. S. Sedra, R. B. Datar, and M. W. Chomik, "High-frequency switched-capacitor filters: performance limitations and design considerations," in Proc. IEEE Int. Symp. on Circuits and Systems, pp. 646-650, May 1984.
- [46] K. Singhal and J. Vlach, "Two-graph tableau and mixed nodal tableau formulation of networks with ideal elements," 1978 European Conf. Circuit Theory and Design, (Lausanne, Switzerland), pp. 553-557.
- [47] K. Martin and A. S. Sedra, "Exact design of switched-capacitor bandpass filters using coupled-biquad structures," IEEE Trans. Circuits Syst., vol. CAS-27, pp. 469-475, June 1980.
- [48] M.-L. Liou, Y.-L. Kuo, and C. F. Lee, "A tutorial on computer-aided analysis of switched-capacitor circuits," Proc. IEEE, vol. 71, no. 8, pp. 987-1005, Aug. 1983.
- [49] R. D. Jolly and R. H. McCharles, "A low-noise amplifier for switched capacitor filters," IEEE J. Solid-State Circuits, vol. SC-17, pp. 1192-1194, Dec. 1982.
- [50] D. J. Allstot and W. C. Black Jr., "Technological design considerations for monolithic MOS switched-capacitor filtering systems," Proc. IEEE, vol. 71, pp. 967-986, Aug. 1983.
- [51] R. T. Kaneshiro, "Circuit and technology considerations for high frequency switched-capacitor filters," Ph. D. Dissertation, Univ. of California, Berkeley, June 1983.

- [52] B. K. Ahuja, "An improved frequency compensation technique for CMOS operational amplifiers," IEEE J. Solid-State Circuits, vol. SC-18, pp. 629-633, Dec. 1983.
- [53] D. C. Stone, J. E. Schroeder, R. H. Kaplan and A. R. Smith, "Analog CMOS building blocks for custom and semi-custom applications," IEEE J. Solid-State Circuits, vol. SC-19, pp. 55-61, Feb. 1984.
- [54] A. S. Sedra and P. O. Brackett, "Filter Theory and Design: Active and Passive," Champaign, Il., Matrix Publ., 1978.
- [55] K. Matsui, T. Matsuura, and K. Iwasaki, "2 Micron CMOS switched capacitor circuits for analog video LSI," Proc. IEEE Int. Symp. Circuits and Systems, pp. 241-244, May 1982.
- [56] S. Masuda, Y. Kitamura, S. Ohya, and M. Kikuchi, "CMOS sampled differential-push-pull cascode operational amplifier," Proc. IEEE Int. Symp. Circuits and Systems, pp. 1211-1214, May 1984.
- [57] K. Martin, "New clock feedthrough cancellation technique for analogue MOS switched-capacitor circuits," Electronics Letters, vol. 18, pp. 39-40, 1982.
- [58] P. W. Li, M. Chin, P. R. Gray, and R. Castello, "A Ratio-Independent Algorithmic A/D Conversion Technique," in Proceedings IEEE International Solid-State Circuit Conference, pp. 62-63, Feb. 1984.
- [59] B. K. Ahuja, W. M. Baxter, and P. R. Gray, "A Programmable CMOS Dual Channel Interface Processor," in Proceedings IEEE International Solid-State

Circuit Conference, pp. 232-3, Feb. 1984.

- [60] D. B. Ribner, M. A. Copeland and M. Milkovic, "80 MHz. Low Offset CMOS Fully Differential and Single-Ended Op Amps," in Proc. IEEE Custom Integrated-Circuit Conf., pp.174-177, Portland, Oregon, May 1985.
- [61] D. B. Ribner and M. A. Copeland, "Some Variations in CMOS Operational Amplifier Design," in Proc. IEEE Mid-West Symp. on Circuits & Systems, Morgantown, W. Va., June, 1984.
- [62] D. B. Ribner and M. A. Copeland, "Design Techniques For Cascoded CMOS Op-Amps With Improved PSRR And Common-Mode Input Range," IEEE J. Solid-State Circuits, vol. SC-19, no. 6, pp. 919-925, Dec. 1984.
- [63] D. B. Ribner and M. A. Copeland, "Small Signal Design Techniques For Cascoded CMOS Op-Amps With Improved PSRR," 1984 Canadian Conference On VLSI, pp. 2.58-61, Edmonton, Alta., October, 1984.
- [64] D. B. Ribner, M. A. Copeland, and M. Milkovic, "15 MHz CMOS Switched Capacitor Filters," in Proc. IEEE Int. Solid-State Circuits Conference, pp. 284-285, New York, N.Y., Feb. 1985.
- [65] K. Buttle, R. Colbeck, R. Gevais, P. Gillingham, H. Schafer, R. White, G. Aasen and D. B. Ribner, "A 160 KB/s Full Duplex Digital Echo Cancelling Transceiver," in Proc. IEEE Int. Solid-State Circuits Conference, pp. 152-153, New York, N.Y., Feb. 1985.

- [66] D. B. Ribner and M. A. Copeland, "Computer-Aided Analysis of Nonideal Linear Switched-Capacitor Networks For High-Frequency Applications," in Proc. IEEE 1985 Int. Symp. on Circuits & Systems, pp. 1169-1172, Kyoto, Japan, Jun. 1985.
- [67] P. R. Gray and R. G. Meyer, "MOS Operational Amplifier Design - A Tutorial Overview," IEEE J. Solid-State Circuits, vol. SC-17, pp. 969-983, Dec. 1982.
- [68] K. E. Brehmer and J. B. Weiser, "Large swing CMOS Power Amplifier," IEEE J. Solid-State Circuits, vol. SC-18, pp. 624-629, Dec. 1983.
- [69] B. J. Sheu and C. M. Hu, "Modelling the Switch-induced error voltage on a Switched-Capacitor," IEEE Trans. Circuits Syst., vol. CAS-30, no.12, pp. 911-913, Dec. 1983.
- [70] D. B. Ribner, and M. A. Copeland, "Biquad Alternatives for High-Frequency Switched-Capacitor Filters." accepted IEEE J. Solid- State Circuits, Dec. 1985.
- [71] G. W. Stewart, "Introduction to Matrix Computations," Academic Press, New York, N.Y., 1973.
- [72] J. C. Maxwell, "A Treatise of Electricity and Magnetism," Oxford: The Clarendon Press, pp. 420-421, 1881.

END

FIN

31 03 87