**DETERMINANTS OF SUCCESSFUL SEMICONDUCTOR DESIGN AND
MANUFACTURE FOR A CAPTIVE FACILITY**

By

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**A thesis submitted to the Faculty of Graduate Studies and Research in partial fulfilment
of the requirements for the degree of
Master of Management Studies**

School of Business

Carleton University

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The personal interest, ready accessibility, professional advice and financial support of Professor Tony Bailetti was invaluable and is gratefully acknowledged. Tony's (unwitting-?) real time demo of a model heavy weight product manager provided as much learning as this thesis itself !

Thanks to Professor Don Gerwin for arranging collaboration with the company studied, for his comments on successive thesis drafts and for making available financial support for this research from the Research Program in Managing Technological Change in Manufacturing.

The time and advise given by Dave Simmons from the semiconductor facility studied was critical and is much appreciated. Thanks to Professor Martin Snelgrove for consenting to be on the thesis committee.

The undersigned recommend to the faculty of Graduate Studies and Research
acceptance of the thesis

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ABSTRACT

The objective of this study was to examine perceptions of critical success factors for a captive semiconductor design and manufacturing facility of large multinational telecommunications company. This study used meeting chip development interval as the key measure of success. A total of 45 critical success factors were identified from the literature review and from interviews with senior managers in the company studied. Three hypotheses investigated perceptions of importance of critical success factors 1. independent of functional departments and chip project types 2. for each functional department and 3. for each chip project type.

Concept maps were obtained, using the Concept Systems software program, for all interviewees, for interviewees from each functional department and for interviewees from each chip project type. Two concepts were formulated that were independent of functional departments and chip project types-the communication and linkages concept and the chip business planning concept. Communication and linkages was perceived to be of high importance and chip business planning was perceived to be of low importance to meeting chip development interval. There was confusion about ownership of critical success factors that are perceived to contribute most to meeting chip development interval.

Differences exist in the formulation of concepts and the perceived importance of the concepts between the system design, silicon design and silicon manufacturing

departments. The system design department formulated three new concepts that were not formulated by other functional departments-technical competence, external support and silicon manufacturing operations.

Three chip project types were identified based on cluster analysis of three variables-chip forecast volume, chip gate count and wafer starts per year. There exist some differences in the formulation of concepts and the perceived importance of concepts among chip project types. Chip project type 2 formulated two new concepts that were not formulated by the other 2 chip project types-the chip costs and top management concept and the participant expertise concept.

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TABLE OF CONTENTS

Abstract	iii
Acknowledgements	v
List of Tables	viii
List of Figures	ix
List of Appendices	x
CHAPTER 1 INTRODUCTION	1
1.1 Research Problem	1
1.2 Motivation for the Study	5
1.3 Summary of Contribution	6
1.4 Organization of Thesis	7
CHAPTER 2 LITERATURE REVIEW	8
2.1 Comparison with Previous Research	9
2.2 Chip Development Characteristics	11
2.3 Issues Related to Product Development Success	12
CHAPTER 3 RESEARCH DESIGN	25
3.1 Research Questions	25
3.2 The Study's Variables and Their Measures	27
3.3 Data Collection	37
3.4 Data Analysis	42
CHAPTER 4 RESULTS	48
4.1 Concept Map Result for All Interviewees	48

	4.2 Functional Department Concept Maps	54
	4.3 Cluster Analysis Results	65
	4.4 Concept Maps for Chip Project Types	67
	4.5 Interviewees' Comments on Issues Related to Meeting Chip Development Interval	78
CHAPTER 5	DISCUSSION OF RESULTS	81
	5.1 Hypothesis 1	81
	5.2 Hypothesis 2	85
	5.3 Hypothesis 3	92
CHAPTER 6	CONCLUSIONS	99
	6.1 Conclusions	99
	6.2 Contribution	105
	6.3 Limitations	107
	6.4 Future Research	109

LIST OF TABLES

TABLE	DESCRIPTION	PAGE
1	MAIN RESPONSIBILITIES OF FUNCTIONAL DEPARTMENTS	3
2	COMPARISON OF THREE NEW PRODUCT DEVELOPMENT STREAMS AND THIS STUDY	9
3	LIST OF CRITICAL SUCCESS FACTORS USED IN THE QUESTIONNAIRE	36
4	CRITICAL SUCCESS FACTOR GROUPINGS BY ALL 23 INTERVIEWEES	50
5	CRITICAL SUCCESS FACTOR GROUPINGS BY 7 INTERVIEWEES FROM SYSTEM DESIGN DEPARTMENT	56
6	CRITICAL SUCCESS FACTOR GROUPINGS BY 8 INTERVIEWEES FROM SILICON DESIGN DEPARTMENT	59
7	CRITICAL SUCCESS FACTOR GROUPINGS BY 8 INTERVIEWEES FROM SILICON MANUFACTURING DEPARTMENT	62
8	COMPARISON OF CONCEPT MAPS FOR ALL RESPONDENTS WITH FUNCTIONAL DEPARTMENT CONCEPT MAPS	65
9	RESULTS OF CLUSTER ANALYSIS	66
10	CRITICAL SUCCESS FACTOR GROUPINGS FOR CHIP PROJECT TYPE 1	69
11	CRITICAL SUCCESS FACTOR GROUPINGS FOR CHIP PROJECT TYPE 2	72
12	CRITICAL SUCCESS FACTOR GROUPINGS FOR CHIP PROJECT TYPE 3	75
13	COMPARISON OF CONCEPT MAPS FOR CHIP PROJECT TYPES	77

LIST OF FIGURES

FIGURE		PAGE
1	CONCEPT MAP FOR ALL 23 INTERVIEWEES	49
2	CONCEPT MAP FOR 7 INTERVIEWEES FROM SYSTEM DESIGN DEPARTMENT	55
3	CONCEPT MAP FOR 8 INTERVIEWEES FROM SILICON DESIGN DEPARTMENT	58
4	CONCEPT MAP FOR 7 INTERVIEWEES FROM SILICON MANUFACTURING DEPARTMENT	61
5	CONCEPT MAP FOR CHIP PROJECT TYPE 1	68
6	CONCEPT MAP FOR CHIP PROJECT TYPE 2	71
7	CONCEPT MAP FOR CHIP PROJECT TYPE 3	74

LIST OF APPENDICES

Appendix A	FACTOR IDENTIFICATION INTERVIEW PROTOCOL
Appendix B	QUESTIONNAIRE

1 INTRODUCTION

1.1 Research Problem

The objective of this research is to examine perceptions of critical success factors that contribute to chips being delivered on schedule by the captive semiconductor design and manufacturing facility of a large multinational telecommunications company. The captive semiconductor facility studied provides a wide range of Application Specific Integrated Circuits (ASICs) to the company. The ASICs supplied by this facility are critical components of rapidly evolving products including telephone and data switches, transmission equipment, wireless terminals and base stations, telephone sets and multimedia terminals. The captive semiconductor facility provides custom ASIC development services including ASIC specification development, ASIC design, hardware prototypes and volume ASIC manufacture to business divisions of the company. In this study, ASIC and chip are used interchangeably.

This study answers the following questions:

- What are the critical success factors perceived to contribute to meeting chip development interval commitments in a captive semiconductor design and manufacturing facility ?

relevant functional groups helps to communicate changes in product requirements and to ensure early identification of technical inconsistencies in a product. Organizational practises like manufacturing signoffs and rotation of design engineers to manufacturing contribute to improved product development performance.

(Adler, 1995) provides a descriptive taxonomy of lateral coordination mechanisms including standards, schedules and plans, mutual adjustments and teams that are used for improved performance. Adler concludes that for improved performance, complex coordination mechanisms need to be implemented for rapid conflict resolution.

Also (Cooper and Kleinschmidt, 1994) note that dedicated project teams, where members are responsible for only one project, as opposed to "having a dozen projects on the go", contributed to product development success. Increased integration may result if a team member can devote more time to a project or if the team member has a limited range of projects tasks that he/she is responsible for at a given time.

4. Guiding visions across projects: Product development is successful when managers are able to identify and manage the link between specific design and development decisions and the evolution of strategic capabilities within the firm.

Functional departments refers to the three main engineering groups in the captive facility of the company studied. Table 1 describes the main responsibility of each of the three functional departments.

TABLE 1 MAIN RESPONSIBILITIES OF FUNCTIONAL DEPARTMENTS

Functional department name	Main responsibility
System Design	Design end products and generate requests for chips that go in as hardware components of the end products
Silicon Design	Produce chips designs from the requirements given to them by the system designers
Silicon Manufacture	Develop and utilize electro mechanical and chemical processes to fabricate the chips designed by the silicon designers

Chip project types are a classification of the chip projects in the facility into mutually exclusive groups. Three chip project types were identified through cluster analysis: chip project type 1, 2 and 3. Cluster analysis was performed using three variables- chip forecast volume, chip gate count and number of wafer starts per year. However only one variable, chip gate count, helped discriminate between the three chip project types.

Success Measure

Success in product development is a multidimensional concept (Griffin and Page

1993). In this study, meeting chip development interval commitments was selected as the relevant measure of product development success. Product development success measures associated with development time are increasingly being emphasized both in the academic literature and by the managers in the captive facility studied. In a study of the automobile industry, Clark and Fujimoto (1991) identify lead time as a key success metric. Cooper and Kleinschmidt (1994) in a study of the chemicals industry and Eisenhardt and Tabrizi (1995) in a study of the mini computer and mainframe industries, focus exclusively on development interval and factors leading to reduction in development interval. Hatch and Mowery (1994) found that the speed with which new products are developed and introduced is critical in the ASIC industry. The Competitive Semiconductor Manufacturing Survey (1994) states "It can be argued that an ASIC facility sells development time in addition to it's ASIC product offering".

The use of meeting development interval commitments as a key success metric has also been corroborated by the managers in the company and in the semiconductor facility. In most development projects, the chips developed by the semiconductor facility are on the critical path of the development process of the end product. Working prototypes of the chips are required as early as possible to enable system level testing and to develop software.

1.2 Motivation for the Study

This study is important for three reasons. The captive semiconductor facility being studied is presently changing operations from being a cost centre to a profit centre. The answer to the first question can be used to guide the facility's transition from being a cost centre to a profit centre. The results of this study will highlight those aspects of chip development that are perceived to be important for meeting development interval. This can enable managers to begin shortening chip development interval, an important influence to profit making. Answering the first question entails: 1. identification of an appropriate metric for chip development interval and 2. identification of critical success factors that contribute to chips being developed on time.

Second, this is the first empirical study of what perceptions determine success in meeting development interval commitments that are specific to a captive semiconductor facility. Previous studies have used cases and multifirm surveys that are generalizable across industries without distinguishing between project types and across functional departments' views. However, each functional department focuses on different aspects of the chip development process. Differences in departmental thought worlds and organizational routines may inhibit effective chip development (Dougherty, 1992). The research design of this study permits the identification of perceptions of critical success factors across chip project types and

functional departments.

Third, this study can be used to understand what skills and attitudes are critical in managers of captive semiconductor design and manufacturing facilities. Managers in the facility can develop and acquire the skills necessary for each perceived critical success factor explicated by this study.

1.3 Summary of Contribution

This study provides the following contributions. First, this study explicates the 'glue' that binds together elements contributing to successful captive chip development. The explication of this 'glue', across functional departments and chip project types, provides managers in the facility with a shared view of what contributes most to successful captive chip development. Second, this study highlights the need for improved management of prototype development for successful captive chip development. Third, this study provides managers in the facility with a template that can be used for better project planning and evaluation. Fourth, this study highlights key elements that need consideration for developing a tool to assess development personnell's skills and attitudes. As the facility changes operations to a profit centre mode, the tool can be used by managers to learn more about and monitor changes in development personnel's skills and attitudes.

1.4 Organization of Thesis

The next chapter provides a review of the literature. Chapter 3 describes the research design used in this study including the data collection and data analysis plan. The results obtained from the data analysis are reported in Chapter 4. The results are examined in Chapter 5. Chapter 6 provides the conclusions and limitations of this study as well as suggestions for further research.

2 LITERATURE REVIEW

Literature on product development reviewed included studies on product development success factors (Lilen and Yoon, 1989; Cooper and Kleinschmidt, 1991, 1994; Madique and Zirger, 1984; Zirger and Madique, 1990; Griffin and Page, 1993; Eisenhardt and Tabrizi, 1995), cross functional integration (Gupta and Wilemon, 1990; Hise, O'Neal, Parsuraman and McNeal, 1990) and project management (Pinto and Slevin, 1988a, 1988b). The semiconductor related literature (Hatch and Mowery, 1994; Mody and Wheeler, 1987; Gruber 92; Gerwin 94), was reviewed to identify industry specific issues that may not have been captured in the new product development literature.

In Section 2.1, this study is compared with the existing product development literature. Section 2.2 describes the special characteristics of the semiconductor industry given in the semiconductor related literature. Issues identified in the literature as significant contributors to improved product development performance are reviewed in Section 2.3. Each issue that was identified is described with corresponding citations to the authors of the studies from where the issues were identified.

2.1 Comparison with Previous Research

The new product development literature can be broadly classified into three research streams. Product development can be studied as: 1. a rational plan; 2. a communication web; and 3. as disciplined problem solving (Brown and Eisenhardt, 1994). Table 1 provides a comparison of the three research streams given above with this study.

TABLE 2 A COMPARISON OF THREE NEW PRODUCT DEVELOPMENT RESEARCH STREAMS AND THIS STUDY

Concepts	Rational Plan	Communication Web	Disciplined Problem Solving	This study
Key Idea	Success via superior product, attractive market, rational organization	Success via internal and external communication	Success via problem solving with discipline	Success defined via functional departments and product type
Theory	Mostly atheoretical	Information and resource dependence	Information including problem solving	Exploratory
Methods	Bivariate analysis; single informant; many independent variables	Deductive and inductive; multivariate; multiple informants	Progression from inductive to deductive; multiple informants; single industry, global studies	Multivariate analysis; single informant; single company
Performance (Dependent Variable)	Financial success (profits, sales, market share)	Perceptual success (team and management ratings)	Operational success (speed, productivity)	Operational success (meeting target development interval)
Independent Variables	Includes product, market, top management project team, communication, suppliers customers	Includes communication, project leader	Includes product integrity, top management, project team, organization of work, project leaders, suppliers	Includes chip related measures, communication, project leader, top management, internal integration, customers
Sample studies	Cooper and Kleinschmidt, 1987; Zirger and Madique, 1990; Gupta and Wilemon, 1990	Allen, 1977; Katz and Allen, 1985; Dougherty, 1992	Imai et. al, 1985, Hayes et. al. 1988; Clark and Fujimoto, 1991, Eisenhardt and Tabrizi, 1995	

This study is exploratory in nature and uses techniques most often found in the rational plan stream of studies. Like the rational plan stream, this study uses a diverse set of variables that capture chip related measures, communication, project leader, top management, internal integration and customer related concerns. Simultaneously this study also uses variables used in the communication web stream. The performance variable in this study, like in the problem solving perspective, is an operational success measure-product development interval.

This study uses key elements of each of the three perspectives described in Table 1 to examine chip design and manufacture in a single captive facility.

2.2 Chip Development Characteristics

Special characteristics of the semiconductor industry include the relatively young age of the chip fabrication process industry; the high degree of interdependence between chip design and chip fabrication process development; the simultaneous, rapid evolution of technologies for both chip design and chip fabrication; and the close coupling between chip design support tools and the physical design of chips, (Hatch and Mowery, 1994). Other, business related, characteristics of the semiconductor industry (including the telecom specific semiconductor segment) are importance of fast evolving technical public standards (Gerwin, 1994), heightened competition (Gruber, 1992), relatively short product life cycles and compressed

product development intervals (Hatch and Mowery, 1994).

According to (Schoonhoven and Jelinek, 1990), on the one hand, in the semiconductor industry, continuity, control and integration between departments are required for the orderly process of new technology development and reliable high quality manufacturing. On the other hand changing market environments and fast evolving chip design and manufacturing technologies require organizational adaptability, increased learning capabilities and development flexibility. It seems apparent from the literature that this dilemma or "dynamic tension" (Schoonhoven and Jelinek, 1990) is both organizational and technical. According to (Crawford, 1990) to gain speed it is necessary to avoid projects that require lots of learning. New 'breakthrough' products, on the other hand, offer increased future product differentiation scope and provide for sustained competitive advantage. Apparently contradictory technical and business requirements need focussed management for successful chip development.

2.3 Issues Related to Product Development Success

This section provides the issues that were identified as being important contributors to improved product development performance. The studies reviewed are not limited to those where performance was measured in terms of development time. A broader perspective was adopted in the writing of this section.

New Product Development Literature

1. Product definition and vision: This issue pertains to the formulation of a clear product concept and establishment of sharp product definition early in the development process.

Rationale: (Gupta and Wilemon, 1990) state that: "Poor definition of product requirements was the number one reason for product development delays". According to (Clark and Fujimoto, 1991) "A strong product concept evokes in the minds of the designers and engineers a palpable vision of the future product experience. A powerful concept ... captures a whole complex of customer needs and interests". This is the cornerstone of what (Clark and Fujimoto, 1991) described as product integrity. Product integrity, as defined and described by Clark and Fujimoto, has two dimensions-internal and external. Internal integrity refers to the consistency between the function and the structure of the product and external integrity is related to the quality of customer-producer linkages. Clear product vision and definition are embodied in product integrity and contribute to shortening product development interval.

2. Predevelopment Planning: Detailed predevelopment business and technical planning contributes to fewer delays downstream and reduces cost overruns.

Rationale: The importance of detailed predevelopment planning has been emphasized by (Gupta and Wilemon, 1990), (Clark and Fujimoto, 1991), (Hayes, Wheelwright and Clark, 1988). According to (Cooper and Kleinschmidt, 1994) "Projects where the team spent more time and effort on up-front homework (or the predevelopment tasks) actually saved time later !". Upfront explication of the project focus, on both technical and business goals, contribute to improved performance. This issue relates to estimation, planning and scheduling of a development project's activities, while the previous issue relates to capturing and translating product requirements into product specifications.

3. Integration within a development project: Integration of team members with varied functional skills and backgrounds within a project is important for product development success.

Rationale: (Dougherty, 1992) underscores the existence of "thought worlds" driven by different functional specializations of product development team members. Various studies have identified the critical role of good cross functional integration within projects including (Cooper and Kleinschmidt, 1994), (Gupta and Wilemon, 1990), (Zirger and Madique, 1990), (Clark and Fujimoto, 1988), (Hayes et al., 1987). According to (Gupta and Wilemon, 1990) "Getting these (multi functional) groups to cooperate and coordinate their efforts is key to successful product development". Early involvement of design, manufacturing, marketing and other

relevant functional groups helps to communicate changes in product requirements and to ensure early identification of technical inconsistencies in a product. Organizational practises like manufacturing signoffs and rotation of design engineers to manufacturing contribute to improved product development performance.

(Adler, 1995) provides a descriptive taxonomy of lateral coordination mechanisms including standards, schedules and plans, mutual adjustments and teams that are used for improved performance. Adler concludes that for improved performance, complex coordination mechanisms need to be implemented for rapid conflict resolution.

Also (Cooper and Kleinschmidt, 1994) note that dedicated project teams, where members are responsible for only one project, as opposed to "having a dozen projects on the go", contributed to product development success. Increased integration may result if a team member can devote more time to a project or if the team member has a limited range of projects tasks that he/she is responsible for at a given time.

4. Guiding visions across projects: Product development is successful when managers are able to identify and manage the link between specific design and development decisions and the evolution of strategic capabilities within the firm.

Rationale: According to (Bowen, Clark, Holloway and Wheelwright, 1994) "the interlocking visions for product development-the product concept, the project vision and the functional departments vision-provides the link between specific design decisions and the growth of strategic capabilities within a firm by identifying the project's learning goals, including what the product means to the customer". Creating and communicating each of the three guiding visions listed above, the line of business vision, the project vision and product vision, is related to clear task partitioning and decreased technical uncertainty. This is related to development interval.

5. Project leadership: The performance of a product development project has been linked to the effectiveness, empowerment, technical knowledge and political savvy of the project leader.

Rationale: One of the main themes of the findings of the Harvard auto studies that included (Clark and Fujimoto, 1991), (Hayes, Wheelwright and Clark, 1988) and others was the importance of the "heavyweight product manager". According to the (Clark and Fujimoto, 1991), "A heavyweight product manager possesses multiple skills, coordinates specialists, and champions product concepts ... (he/she) effectively functions as the general manager of the product ... A true heavyweight product manager can significantly influence the degree of internal integration a firm achieves ... (he/she is) also essential if a firm desires external integrity. Having a

true heavyweight manager appears to be an effective strategy for meeting diverse, uncertain and inarticulate customer needs". A heavyweight product manager with a clear understanding of the product concept, with good project coordination skills, significant decision making responsibility and good lobbying skills with senior management contributes to on time product development.

6. Quality of execution of activities: The technical competency of each of the participating units including system design, silicon design, silicon design tool support, product engineering, applications engineering, silicon manufacturing, test engineering, end product manufacturing influence chip development success.

Rationale: All of the units listed above participate in the development process of a chip. The chip development project is expected to be only as successful as the quality of the intermediate tasks done by each unit. This conclusion can be derived from the studies by (Zirger and Madique. 1990) and (Cooper and Kleinschmidt, 1987, 1994). According to (Clark and Fujimoto, 1991) "Highly productive engineering organizations are source of fresher, more attractive products and greater product line variety". For example technically competent chip designers should not only be able to understand and convert system requirements into chip implementations but also understand constraints of the chip fabrication process. This reduces the probability of technical inconsistencies resulting in reduced iterations and corrections leading to reduced development time.

7. Ownership and commitment of senior management: The level of senior management support is important to a development projects success.

Rationale: The importance of ownership and commitment of senior management is repeatedly stressed in the literature (Cooper and Kleinschmidt, 1987; Gupta and Wilemon, 1990; Katz and Allen, 1985; Zirger and Madique, 1990). According to (Brown and Eisenhardt, 1995) "senior management support is essential for fast and productive product development". In contrast to the above given studies, (Crawford, 1992) cautions that "much accelerated product development is focussed on projects whose product innovation charter calls for low risks where top management can stay off". This suggests that different development projects may require different levels of commitment by senior management. In either instance, senior management support does seem to be a relevant issue for product development interval.

8. Strong market orientation: The characteristics of the products' market, like market size, market growth rate and number and size of competitors, influence product development success.

Rationale: According to (Cooper and Kleinschmidt, 1994) "products aimed at attractive markets-large, growing, high need, good margins, good economic climate-and competitive markets-will feature better cycle time". The study also states that

"markets characterized by many competitors, intense aggressive competition... will see more rapid product developments". The existence of the conditions listed above may induce a company to act quickly to extract the potential profits to be gained by getting the product to the customer quickly, by high potential sales volumes or by meeting/exceeding the competitor's product delivery schedule.

9. Good internal and external communication: The frequency and content of communication between product development team members and other units within and outside the organization stimulates the performance of product development teams.

Rationale: Increased company internal communication and information exchange within development teams and between development teams and other functional departments within the company can lead to faster problem solving. However a caveat is in order here. Often the languages spoken by people from different functions differ-this inhibits building working relationships and makes communication difficult. But as (Brown and Eisenhardt, 1995) state "frequent and appropriate structured task communication leads to comprehensive and varied information flow to team members and thus, to higher performing development processes. Also frequent political communication (typically external) leads to a higher performing development process by increasing the resources such as budget, personnel and equipment that are available to the team". The term frequent

external communication above refers to communication by team members and the team leader with managers from other functional departments within the company. Even though there exist semantic differences between functions, several studies identify increased communication as a significant contributor to improved product development performance (Allen 1977, Ancona and Caldwell, 1990).

10. Prototyping: The practice of using more prototypes early in the project and more prototypes that capture system interactions contributes to product development success.

Rationale: According to (Bowen, Clark, Holloway and Wheelwright, 1994) "system level prototypes help in project coordination and integration". Improving prototype management is identified by (Clark and Fujimoto, 1991) as being critical to shortening product development intervals without adding people or diminishing the product's quality.

11. High customer involvement: Significant customer involvement in each phase of the product development process contributes to the project's success.

Rationale: Tight linkages with the customer ensure focussed, effective, 'on target' product development. As (Zirger and Madique, 1990) state "Value can be provided

to the customer by a lower cost design ... superior technical performance ... or a combination of these. In order to understand the real value of particular features of the product, development firms need to have close contacts between the development team and the end user". Additionally (Clark and Fujimoto, 1991) identify "customer access and orientation" as leading to improved development performance.

12. High supplier involvement: More supplier involvement is associated with product development performance.

Rationale: Suppliers in the context of this study are design tool companies and external silicon vendors. For example, as the chip design process is closely coupled with the chip design tools used in a project, instant access to technical advice or having personnel from the design tool provider helps in faster and more timely problem solving by the chip design team. Another example of the advantage of more supplier involvement is the design of chips into a fabrication process external to the company. In this situation having a representative from the chip fabrication company can lead to early identification of technical problems and inconsistencies leading to shortening of development interval. However, this study does not examine externally fabricated chips.

(Imai, Ikujiro and Takeuchi, 1985) highlight the importance of supplier networks.

Suppliers can acquire a very high level of technical understanding in a specialized area, which allows them to fulfil sudden requests quickly. According to (Eisenhardt and Tabrizi, 1995) "if suppliers are involved early in the many of the steps of the process, then they are more likely to catch future problems, such as contradictory specifications or unrealistic designs, sooner in the process, when they are easier to fix". (Mabert, Muth and Schmenner, 1992) also state in their conclusions that, projects can be accelerated with the early involvement of suppliers and vendors.

13. Good project management: Project management activities like monitoring the project's progress, the existence of control systems, matrix management structures and good information support tools contribute to development success.

Rationale: (Gupta and Wilemon, 1990) state that about 29% of the interviewees in their study attributed development delays to poor project management. (Pinto and Slevin, 1988a, 1988b) identify good project execution to be critical to a projects' success - " proper attention to schedules represents an important consideration for both project leaders and team members, not only in terms of actual time frame to completion, but also as a periodic check-list for feedback on project performance". Good project management tools are not only remedies to technological barriers, but also facilitate the introduction of organizational enablers.

Semiconductor related studies

14. Learning associated with a chip: "Learning" is defined as improvement in both the line yield¹ and the die yield² for a silicon wafer.

Rationale: For any semiconductor manufacturer the steepness of the learning curve is the critical determinant of unit product costs over the products' life cycle, (Mody and Wheeler, 1987). According to Florida and Kenney (1990), "The value of semiconductor fabrication (especially in ASIC fabs) is increasingly changing from the traditional process based on extraction of marginal units of physical labour to a process based on continuous knowledge extraction and innovation both in the lab (development fab) and on the shop floor".

The factors leading to improved chip manufacturing line yield include: 1. reduction in number of broken wafers and 2. reduction in number of processing errors. The line yield factors are associated with improved fabrication floor management. The factors leading to die yield improvement are: 1. reduction of defects on each wafer, 2. improving the compatibility of various devices on a chip, and 3. improving chip design. The three die yield factors listed above are associated with manufacturing

¹ Line yield expresses the average fraction of wafers started that emerge from the fab process flow as completed wafers.

² Die yield is the fraction of the total die on a wafer that pass the wafer probe test.

equipment precision requirements, design for manufacturability and design complexity respectively. Once substantial technical knowledge from each of the areas listed above is accumulated, this learning is transferrable across multiple chips using the same fabrication process.

According to (Hatch and Mowery, 1994) "in the case of ASIC producers, the constraints and opportunities resulting from the incremental, controlled introduction of new process technologies must be clearly incorporated into the design rules that determine the range of custom products that can be manufactured within a given foundry". ASIC fabs frequently introduce incrementally modified manufacturing processes to adapt to the different chip requirements. This needs careful projection of the evolutionary path of process technology. For a product type the factors specific to a particular fabrication process contributes to chip differentiation scope, associated price sensitivity and larger fixed costs per process.

3 RESEARCH DESIGN

Section 3.1 lists the research question and the hypotheses. Section 3.2 gives a list of the variables and measures used in this study. This section includes measures of meeting chip development interval, measures of the 14 issues related to product development success identified in the literature review (Chapter 2), description of the interviews with senior managers to ascertain their views on critical success factors contributing to meeting chip development interval and the final list of critical success factors used for data collection. The data collection procedure, presented in Section 3.3, includes the unit of analysis, the sample size of this study, a description of the identification of the chip project types, interviews for grouping critical success factors and the questionnaire used to rate the critical success factors. Section 3.4 describes the data analysis procedure used for answering the research question and the hypotheses.

3.1 Research Questions

Research Problem

To identify critical success factors perceived by stakeholders to contribute to meeting chip development interval commitments in a captive semiconductor design and manufacturing facility, and to investigate whether critical success factors

depend upon functional departments and chip project types.

The hypotheses investigated in this study are:

Hypothesis 1

There exist certain perceived critical success factors that are independent of participant functional departments and chip project types.

Hypothesis 2

Perceptions of critical success factors vary across participant functional departments.

Hypothesis 3

Perceptions of critical success factors vary across chip project types.

3.2 The Study's Variables and Their Measures

The measure used for estimation of meeting chip development interval is given below. This is followed by a description of the procedure used to obtain critical

success factors from the 14 issues, affecting product development success, identified in the literature review. This is followed by a description of interviews with senior managers to ascertain their views of critical success factors contributing to meeting chip development interval.

- Meeting chip development interval

Chip development interval is met when the actual delivery for a chip occurs on the week specified in the delivery plan decided upon on at the time that the chip's specifications were agreed upon.

- Issues identified from literature review

Each of the 14 issues that affect product development success, identified in the literature review (Chapter 2), have multiple components. The multiple components of each issue are listed item wise below. Critical success factors were derived from each issue by interpreting the issue in terms of the operations of the captive chip development process of the company studied. For example the first issue identified in the literature review, product definition and vision, relates to chip specification formulation and establishment in the chip development process of the company studied.

1. Product definition and vision:

Item 1: Clear technical specifications were provided at the chip definition gate- these specs remained largely unchanged during the development process.

2. Predevelopment Planning:

Item 2: Market and business analysis was conducted and documented for the chip and the product.

Item 3: Assessment of technical feasibility conducted and documented for the chip and the product.

3. Integration within a development project:

Item 4: Members from different groups within a functional department, like Process Technology Development, Product Engineering and Test Engineering in the silicon manufacturing department, participated early in the chip development process and provided credible, detailed and timely input.

Item 5: Members from other functional departments, like the Systems Design group and the Systems manufacturing group, participated early in the chip development and provided credible, detailed and timely input .

Item 6: Members on the development team for a chip had clearly prioritized individual project assignments.

Item 7: Early manufacturing assessment was done for the chip.

Item 8: A manager was designated with ownership of the entire chip development

program.

Item 9: All development team members were in close physical proximity (in the same location).

4. Guiding visions across projects:

Item 10: A business plan was made for the chip project with senior managers assessing the compatibility of the project with the strategic needs of the company and the functional departments.

5. Project leadership:

Item 11: The chip development project had a dedicated, technically knowledgeable project manager who was able to lobby with and negotiate resources from senior management.

Item 12: The project manager had a clear vision of the product concept.

Item 13: The project manager was able to secure cooperation from other units in the organization.

6. Quality of execution of activities:

Item 14: Managers from the system design group in the chip development project were professionally competent and did a good technical job.

Item 15: Managers from the silicon design group in the chip development project were professionally competent and did a good technical job.

Item 16: Managers from the silicon manufacturing group in the chip development project were professionally competent and did a good technical job.

Item 17: Managers from the product manufacturing group in the chip development project were professionally competent and did a good technical job.

7. Ownership and commitment of senior management:

Item 18: Senior management demonstrated its commitment by clear formal recognition that achieving project goals is necessary for continued corporate success.

Item 19: Senior management demonstrated its commitment by providing the necessary resources and autonomy to make decisions.

8. Strong market orientation:

Item 20: Chip's volume growth rate was estimated accurately.

Item 21: The positioning of the chip and the end product relative to the competitors' product offerings were reviewed.

Item 22: Competitor size and aggressiveness was appraised.

9. Good internal and external communication:

Item 23: There was frequent task oriented communication between team members and managers in other functional departments within the organization.

Item 24: There was frequent task oriented communication between team members

and managers from other functional departments about events external to the company.

10. Prototyping:

Item 25: Critical elements of the chip were prototyped as early as possible in the development process.

Item 26: System level hardware prototypes were produced as early as possible in the development process to facilitate software co development.

11. High customer involvement:

Item 27: The internal customer (buyer of the functional departments' product) participated extensively in the chip development process.

12. High supplier involvement:

Item 28: Suppliers, for example silicon design tool providers and silicon manufacturing testing equipment contractors, were involved in the development process.

13. Good project management:

Item 29: Good project management tools were used in the chip development project.

Item 30: Frequent and relevant short term milestones and reviews were held for the

chip development project.

14. Learning associated with a chip/ Process Maturity:

Item 31: Choice of fabrication process technology.

Item 32: Extensive process characterization was done in the development fab.

Item 33: A number of new process steps were used.

Item 34: There was substantial past cumulative volume experience in the process development fab.

Item 35: Existing cell libraries were used.

● Interviews with Senior Managers to Identify Critical Success Factors

Semi-structured interviews were conducted with four senior managers of the company to ascertain their views on the factors contributing to successful chip development. The four managers were asked: 1. what success of chip design and manufacture means to them and 2. to identify factors that contribute to this success. The protocol used for this set of interviews is provided as Appendix A. The senior managers, one from each of four functional departments in the company, were reputed, experienced technical managers. This increased the chance that all technical and managerial concerns would be comprehensively captured in the interviews.

Results of Interviews Four Senior Managers

The four senior managers interviewed initially stressed the importance of meeting chip development interval commitment as a key success measure for a captive ASIC facility.

All four senior managers repeatedly stressed the importance of inter and intra team communication for meeting chip development interval commitment.

The manager providing the semiconductor design perspective identified "inherent technical risks taken upfront" as the key factor contributing to meeting chip development interval commitment.

The manager providing the semiconductor manufacturing perspective identified the following factors contributing to meeting chip development interval commitment:

- "Clear upfront understanding of development requirements"

Clear definition of chip design, fab process, fab capability and of what is important for operations.

- "Complexity"

Including all of the following: number of process steps, complexity of testing and

number of gates.

- "Inherent inefficiencies in manufacturing"

Manufacturing 7 days a week causes intrinsic inefficiencies in operations.

The manager providing the system design perspective identified the following factors as contributing to meeting chip development interval commitment :

- "Quality of silicon designers"

Silicon designers should understand and convert system requirements into silicon implementations, understand limits of fab process and understand variation of fab process. Accurate analog simulation, knowledge of design tools and experience of a silicon designer are important.

- "Coupling between design and manufacturing units"

Smooth transfer for test and QA and seamless customer interface and ability to work with product development group are important.

The fourth manager interviewed was to provide the product line management perspective. This manager however, stated that he was not involved in the chip development process and that his only concern was the timely receipt of the chips.

The statements generated by the managers were assembled into a critical success factor list. This critical success factor list contains factors that contribute to chip design and manufacturing success. The critical success factors that were identified in the literature review, but were not mentioned by the managers, were added to the critical success factors list. Redundant factors were eliminated from the list. This list is given in Table 3 below.

Table 3 provides the combined list of critical success factors obtained from the literature review and the interviews with senior managers. This list of critical success factors was used in the questionnaire as shown in Appendix B. The critical success factors in bold type were obtained from the interviews with the senior managers. The rest of the critical success factors were obtained from the list of issues affecting chip development interval given earlier in this section. The importance of the contribution of each critical success factor for meeting chip development interval was measured using a seven point Likert scale running from a value of 1 to 7 as importance increased.

TABLE 3 LIST OF CRITICAL SUCCESS FACTORS USED IN THE QUESTIONNAIRE

Critical success factors which contribute to meeting chip development interval commitments	
1.	Clear chip specifications
2.	Unchanged chip specifications
3.	Accurate business plan formulation at project start
4.	Technical feasibility options assessment at project start
5.	Timely credible participation of other groups within the functional department
6.	Timely credible participation of other functional departments
7.	Prioritized individual project assignments
8.	Early chip manufacturing assessment
9.	Team member co-location in same city
10.	Long term business road map formulation for the chip
11.	Project leader's technical competency
12.	Project leader's chip concept vision
13.	Project leader's ability to secure cooperation from other departments
14.	System designer's technical competence
15.	Silicon designer's technical competence
16.	Silicon manufacturing technical competence
17.	Product manufacturing technical competence
18.	Operational autonomy given to development team
19.	Top management support visibility for project goals
20.	Resource provision by top management
21.	Accurate chip volume growth estimation
22.	Assessment of chip's positioning relative to competition
23.	Assessment of product's positioning relative to competition
24.	Assessment of chip competitor's market aggressiveness
25.	Frequent team member communication with other groups within functional department
26.	Frequent team member communication with groups from other functional departments
27.	Frequent intra team member communication
28.	Early prototype of critical elements of chip
29.	Early availability of system level prototypes
30.	Extensive customer participation
31.	Extensive supplier/contractor/partner involvement
32.	Use of good project management tools
33.	Frequent technical milestone reviews
34.	Choice of fab process used
35.	The number of new process steps used
36.	Past cumulative volume experience with the fab process
37.	Low initial fab line/die defect rates
38.	Formulation of process development evolution plan
39.	Fab NRE costs for chip
40.	Use of existing cell libraries
41.	Clear upfront understanding of development requirements
42.	Unchanged team member assignments for project duration
43.	Clear detailed documentation of hand off procedure between departments
44.	Unit chip costs
45.	Estimated chip price

3.3 Data Collection

Support for this research was solicited from managers of a captive chip design and manufacturing facility of a large telecommunications company. These managers agreed to provide office space and to support this study. A key contact manager was designated to help define key issues that pertained to the scope and focus of this research and to coordinate data collection.

Unit of Analysis

The unit of analysis for this study is a chip development project.

Sample Size

The sample for this study, for the purpose of chip project type identification, was eighty four chip development projects of the facility being studied. For the identification of concepts and perceptions of the importance of critical success factors a total of 23 individuals were interviewed from 19 chip projects.

Chip Project Types

Chips being developed by the facility consist of widely differing components and

have different technical attributes associated with the differing technical components. For example a chip for a high end switching application is considerably different from a chip for a telephone terminal in terms of gate count, die size, functionality, memory and many other technical attributes. Additionally the chips in the example above could also differ in terms of their business characteristics, like chip sales volumes, unit price and margins and other business attributes.

A total of 84 chips developed by the facility were included in this study for chip classification. The technical and business differences among chips entail differences among the chip development projects in terms of the project's importance to a functional department and the degree or kind of participation by a functional department. To make a meaningful assessment of perceptions of critical success factors contributing to meeting development interval commitments, the chips needed classification.

Data on 6 chip attributes for each chip included in this study were collected from the facility. The attributes to classify the chip projects were identified by the contact manager. The resultant chip project classification is later used to investigate Hypothesis 2, as described in Section 3.4.

Critical Success Factor Grouping Interviews

In chapter 2 the findings from the literature review were organized by the researcher into 14 different issues. For each issue, a series of items that defined critical success factors for meeting chip development interval were identified. Additional critical success factors were defined from the interviews with senior managers.

The large number of critical success factors identified and the possible shared association of the critical success factors necessitated the grouping of critical success factors into the underlying concepts. To identify groupings of the critical success factors into the underlying concepts the following procedure was used together with responses to the questionnaire described below.

A stratified random sample of engineers and managers was obtained in two stages to ensure comprehensive capture of the concepts prevalent in each of the three functional departments. First, all individuals involved with the design and manufacture of 77 of the 84 chips included in this study were separated into non overlapping groups defined according to their three functional departments. Data on individuals responsible for 7 chips were missing. Second, eight experienced individuals, with strong technical reputations, were selected from each functional department. The number of individuals interviewed for each chip project type was

roughly proportional to the number of chip projects in each chip project type. While there was no stratification of individuals according to chip project types, the large number of interviews with individuals responsible for each chip project type, increased chances of comprehensive capture of concepts for each chip project type.

Each individual selected using the above procedure was contacted and given a brief description of the objectives of this study. He/she was then requested to participate in this study by providing 45 minutes to 1 hour for an interview. In case the individual was unavailable, other persons from the same functional group were contacted for setting up interviews.

During the study 6 individuals from the product manufacturing department who were contacted by the researcher stated that they had no operational role to play in the chip development process. 4 individuals stated that, apart from some mechanical packaging considerations of multi chip packs, their only concern was the compliance of the completed chips and chip packs to the company's manufacturing standards and guidelines. 2 individuals from the product manufacturing department stated that they did not have any association at all with the chip development process. As a consequence of the above the product manufacturing department was excluded from further consideration in this study.

Interviews were set up with 24 individuals (eight from each functional department) but one interviewee was unavailable at the last moment. A total of 23 interviews were conducted with each of the 23 selected individuals. Each interviewee was provided with a set of 3x5 inch sorting cards. Each card had a statement from the critical success factor list printed on it. Each interviewee was asked to sort the cards into piles in a way that makes sense to him or her, placing similar statements in the same pile and grouping for similarity not priority (MacDonalds, Cousin, Bailetti and Rahman, 1995). In this context the term similarity refers to belonging to the same concept. After sorting the cards each of the 23 interviewees were requested to answer the questionnaire described below.

Questionnaire

Questionnaire responses obtained from the 23 individuals interviewed were used together with the card sorting procedure of each of the 23 individuals, described immediately above, to ascertain critical success factor groupings into concepts.

The questionnaire had 2 parts. In the first part, the respondent was asked to think about a chip, specified by the researcher, that he/she has helped develop and then provide information that describes the chip and the chip project. In the second part of the questionnaire, each respondent was asked to provide ratings for each of the critical success factors listed in the questionnaire on the factors' importance for

meeting chip development interval. Responses to the second part of the questionnaire are 7 point Likert scale rankings of the importance of the contribution of each critical success factor for meeting chip development interval.

3.4 Data Analysis

The data includes 23 sets of 3x5 inch card piles and 23 responses to the first and second part of the questionnaire.

Hypothesis 1: There exist certain perceived critical success factors that are independent of participant functional departments and chip project types.

The Concept Systems program (Trochim 1986,1989) was used to examine the information provided by the 23 individuals who were interviewed. This information includes: the 23 sets of 3x5 inch card piles and the ratings on each of the 45 critical success factors provided in the questionnaire, using meeting chip development interval as the definition for success. The above set of responses was entered into the Concept Systems program for analysis.

The output of the Concept Systems program was a concept map with clusters of critical success factors and importance ratings on each of these clusters. Each cluster represents a concept that leads to meeting chip development interval

commitments. The concept maps obtained as a result of data analysis are described in detail in the results given in chapter 4 (Section 4.1, concept map results for all interviewees).

Hypothesis 2: Perceptions of certain critical success factors vary across participant functional departments.

Card sort results and questionnaire responses provided by all 23 interviewees were separated into 3 sets corresponding to the 3 functional departments. Each set of responses were entered separately into the Concept Systems program for analysis. The output of the Concept Systems program was a concept map with clusters of critical success factors and importance ratings on each of these clusters for each set.

Hypothesis 3: Perceptions of certain critical success factors vary across chip project types.

Chip project classification

The eighty four chips included in this study were classified into three categories as described below.

The contact manager from the company initially identified 5 classification variables that were perceived to be relevant in comprehensively capturing the concerns of the different functions. The first variable was chip fabrication process. All chips that were included in the study were being fabricated using an advanced CMOS process. Silicon manufacturing is responsible for the development, characterization, adaption and validation of a fabrication process. The second variable identified was the device die size. This is the area of the chip before packaging - it is calculated as the product of the chip's X(length) and Y(width) dimensions. The die size of the chip affects important silicon manufacturing metrics like the die yield and line yield for a fabrication process. Thus, the above two variables are a proxy measure of silicon manufacturing's interest. The third variable identified was forecast sales volume in K units per year. This is a proxy measure of the business potential of a chip. The fourth variable identified was chip gate count. The chips included in this study had widely differing levels of integration varying from 300 to over 130,000 gates. This metric is a proxy measure of the complexity of the product for both chips design and manufacture. The fifth measure identified to classify the chips was percentage of analog components on a chip. The percentage analog component is a rough measure of the level of customization of chip. Generally speaking greater analog content, as opposed to digital content, in a chip entails greater design effort (no standard cell library, lack of analog synthesis tools etc). The chips in the sample had an analog content ranging from 0 (full digital) to 90% analog.

Data on the 5 variables was collected for the 84 chip sample. This data was analyzed as described in Cluster Analysis 1.

Cluster analysis 1:

Cluster analysis was performed, using SPSS, with 5 variables-chip fabrication process, device die size, forecast sales volume, gate count and percentage analog content. Some violations of the basic assumption underlying cluster analysis were detected. First while the chip fabrication variable was a categorical variable and chip gate count was a discrete variable, the other 3 variables identified were of the continuous type. This necessitated the exclusion of the fabrication process variable from the analysis. Additionally it was found that the variables gate count and die area were correlated ($.48, p=0.00$). This prompted the researcher to exclude the die area variable from the analysis. The exclusion of the die area variable was suggested by the contact manager.

The cluster analysis was done again to identify the ideal number of product groupings on 3 variables-gate count, percentage analog content and forecast sales volume. The agglomeration schedule of the hierarchical cluster analysis output revealed a large decrease in the distance co-efficient from the 4 cluster to the 5 cluster solution. This signified that, for the given sample of chips, there was a significant decrease in the overall "fit" of the clustering, from the 4 cluster to the 5

cluster solution. Consequently the cluster analysis was done using the above 3 variables with the target number of clusters being set to 4. The results were presented to the contact manager.

The contact manager indicated 2 modifications to the above. First he suggested removing an outlier chip that had a sales volume figure that was a magnitude order higher than the rest. Second he suggested using the number of wafer starts per year³ as an additional variable to capture the effort required by the manufacturing function in the facility. Data was collected for this variable for the 84 chip sample and the cluster analysis was redone. This is described in Cluster Analysis 2.

Cluster Analysis 2:

The wafer starts per year variable was found to be correlated to the percentage analog variable (0.25, $p=0.03$) prompting the exclusion of the latter variable from further analysis.

The final cluster analysis was redone using 3 variables (forecast sales volume, gate count, wafer starts per year). The resulting hierarchial agglomeration schedule

³ Blank wafers are used as the base for creating integrated circuits. A single wafer may have upto ten to some hundred identical circuits on it. The wafer starts per year is the total number of wafers processed through various steps to obtain the desired number of a particular chip.

again pointed to a sharp lowering of the distance coefficient from the 4 cluster to the 5 cluster solution. It was also noted that only one of the three variables, gate count, provided clear, mutually separate chip clusters. A probable explanation of this is that the facility, being captive, develops chips regardless of the expected sales or manufacturing volumes.

The 4 cluster solution resulting from this second analysis was shown to the contact manager and presented in a staff meeting. The managers suggested that there were actually just three groups. The managers pointed out that two of the four product groups (Clusters 3 and 4) were really quite similar on most dimensions and actually represented one group. This classification of 84 chips into three mutually exclusive groups is described in Chapter 4 (Results). The 3 chip clusters, representing 3 chip project types, were used for further analysis as described below.

Card sort results and questionnaire responses provided by all 23 interviewees were separated into 3 sets corresponding to the 3 chip project types. Each set of responses were entered separately into the Concept Systems program for analysis. The output of the Concept Systems program was a concept map with clusters of critical success factors and importance ratings on each of these clusters for each set.

4 RESULTS

Section 4.1 gives the concept map result obtained from analysis of the responses of all 23 interviewees using the Concept Systems program. The concept map result for each functional department is given in Section 4.2. Section 4.3 provides the results of the cluster analysis used to identify the chip project types. Section 4.4 gives the concept map result for each chip project type. Section 4.5 gives a summary of comments from the 23 interviewees on issues related to meeting chip development interval commitments that were not addressed in this study.

4.1 Concept Map Result for All Interviewees

Figure 1 and Table 4 provide the results of the concept map obtained from the analysis of the card sort data and the questionnaire responses of the 23 interviewees using the Concept Systems program. During the formulation of the research design it was estimated that, to investigate Hypothesis 1, the grouping of critical success factors into concepts needed not only investigation of information provided separately by interviewees from each functional department and from each chip project type, but also from the information provided by all interviewees together. As described in chapter 5 (discussion of results), 2 concepts were formulated not only by interviewees from each functional department and from each chip project type separately, but also by all interviewees together. In addition, the

TABLE 4 CRITICAL SUCCESS FACTOR GROUPINGS BY ALL 23 INTERVIEWEES

Identification Name	Critical success factors which constitute each concept	Bridging Index (Agreement Rating)	Mean Importance Rating
Concept 1.1	1. Clear chip specifications 2. Unchanged chip specifications 17. Product manufacturing technical competence 28. Early prototype of critical elements of chip 29. Early availability of system level prototypes 41. Clear upfront understanding of development requirements	0.69	5.53
Concept 1.2	11. Project leader's technical competency 12. Project leader's chip concept vision 14. System designer's technical competence 15. Silicon designer's technical competence 16. Silicon manufacturing technical competence	0.72	5.71
Concept 1.3	4. Technical feasibility options assessment at project start 8. Early chip manufacturing assessment 34. Choice of fab process used 35. The number of new process steps used 36. Past cumulative volume experience with the fab process 37. Low initial fab line/die defect rates 40. Use of existing cell libraries	0.57	5.02
Concept 1.4	3. Accurate business plan formulation at project start 10. Long term business road map formulation for the chip 21. Accurate chip volume growth estimation 22. Assessment of chip's positioning relative to competition 23. Assessment of product's positioning relative to competition 24. Assessment of chip competitor's market aggressiveness 44. Unit chip costs 45. Estimated chip price	0.10	3.66
Concept 1.5	38. Formulation of process development evolution plan 39. Fab NRE costs for chip	0.54	4.03

Concept 1.6	5. Timely credible participation of other groups within the functional department 6. Timely credible participation of other functional departments 7. Prioritized individual project assignments 9. Team member co-location in same city 13. Project leader's ability to secure cooperation from other departments 20. Operational autonomy given to development team 25. Frequent team member communication with other groups within functional department 26. Frequent team member communication with groups from other functional departments 27. Frequent intra team member communication 42. Unchanged team member assignments for project duration 43. Clear detailed documentation of hand off procedure between departments	0.16	5.39
Concept 1.7	18. Top management support visibility for project goals 19. Resource provision by top management 30. Extensive customer participation 31. Extensive supplier/contractor/partner involvement 32. Use of good project management tools 33. Frequent technical milestone reviews	0.71	4.77

The concept map shown in Figure 1 provides 1. a means to visualize the placement of the 45 critical success factors shown in Table 3 into concepts and 2. the positioning of the concepts with respect to each other (Trochim 1986, 1989).

In Figure 1, the dots represent critical success factors. Each small number beside each dot is the number of a critical success factor that corresponds to those listed in Table 3. For example, from Table 3 we know that the small number 29 represents the factor: early availability of system level prototypes. The lines surrounding the dots represent concept borders that delineate one concept from others. The big number in each concept is the number used to identify that concept. Each concept can be identified by the name given in the adjacent label. The concepts and the concept map are interpreted in the discussion of results (Chapter 5).

Table 4 provides the critical success factors belonging to each concept, the Bridging Index of the concept and the mean importance rating for each concept. The Bridging Index: is a measure of the agreement between interviewees on the grouping of the factors into the same concept. The Bridging Index can range from 0.00 to 1.00. The lower the numerical value of the Bridging Index for a concept, the higher the agreement between respondents on grouping the critical success factors together into that concept. For example the Bridging Index of 0.10 for Concept 1.4 identified in Table 4 indicates that most interviewees placed the factor cards constituting that concept into the same pile. The Bridging Index of 0.72 for Concept

1.2 indicates that the interviewees often placed the cards into different piles. This indicates that the critical success factors making up Concept 1.2 may be "bridges" between concepts. The mean importance rating for each concept is the numerical mean of the ratings of all critical success factors constituting that concept.

The Concept Systems software program provided a range of solutions with varying number of concepts. For each solution the ratio of the number of concepts with a Bridging Index of under 0.4 and the number of concepts with a Bridging Index of over 0.4 was calculated. The solution with the highest ratio was selected as the final solution. The Bridging Index limit for each meaningful concept was set to be 0.4 as this indicates that the number of interviewees who placed the constituent critical success factors into the same concept were more than the number of interviewees who did not place together the constituent critical success factors. There is no absolute ratio value that indicates a "good" solution. For example, this ratio in the 7 concept solution for all 23 interviewees (Table 4) is $2/5=0.4$, as 2 concepts have a Bridging Index under 0.4 (Concept 1.4 and Concept 1.6) and the remaining 5 concepts have a Bridging Index over 0.4. Another solution with a total of 8 concepts for all 23 interviewees had 2 concepts with a Bridging Index under 0.4 and 6 concepts with a Bridging Index over 0.4. This gives a ratio of $2/6=0.33$. The 7 concept solution was selected as it had a higher ratio than the 8 concept solution.

4.2 Functional Department Concept Maps

Figures 2-4 and Table 5-7 show the concept map results obtained from analysis of the card sort task and questionnaire responses from 7 interviewees from the system design department, 8 interviewees from the silicon design department and 8 interviewees from the silicon manufacturing department respectively. Table 8 provides a comparison of the concept map results for all respondents and for each functional department given in Table 4 through 7.

FIGURE 2 CONCEPT MAP FOR 7 INTERVIEWEES FROM SYSTEM DESIGN DEPARTMENT

**TABLE 5 CRITICAL SUCCESS FACTOR GROUPINGS BY 7 INTERVIEWEES
FROM SYSTEM DESIGN DEPARTMENT**

Identification Name	Critical success factors which constitute each concept	Bridging Index (Agreement Rating)	Mean Importance Rating
Concept 2.1	1. Clear chip specifications 2. Unchanged chip specifications 41. Clear upfront understanding of development requirements 43. Clear/detailed documentation of hand-off procedure between departments	0.56	5.75
Concept 2.2	11. Project leader's technical competency 12. Project leader's chip concept vision 14. System designer's technical competence 15. Silicon designer's technical competence 16. Silicon manufacturing technical competence 17. Product manufacturing technical competence 28. Early prototype of critical elements of chip 29. Early availability of system level prototypes	0.24	5.70
Concept 2.3	5. Timely credible participation of other groups within the functional department 6. Timely credible participation of other functional departments 7. Prioritized individual project assignments 9. Team member co-location in same city 13. Project leader's ability to secure cooperation from other departments 20. Operational autonomy given to development team 25. Frequent team member communication with other groups within functional department 26. Frequent team member communication with groups from other functional departments 27. Frequent intra team member communication 42. Unchanged team member assignments for project duration	0.07	5.63

Concept 2.4	18. Top management support visibility for project goals 19. Resource provision by top management 30. Extensive customer participation 31. Extensive supplier/contractor/partner involvement 32. Use of good project management tools 33. Frequent technical milestone reviews	0.37	4.7*
Concept 2.5	3. Accurate business plan formulation at project start 10. Long term business road map formulation for the chip 21. Accurate chip volume growth estimation 22. Assessment of chip's positioning relative to competition 23. Assessment of product's positioning relative to competition 24. Assessment of chip competitor's market aggressiveness 39. Fab NRE costs for chip 44. Unit chip costs 45. Estimated chip price	0.17	3.46
Concept 2.6	4. Technical feasibility options assessment at project start 8. Early chip manufacturing assessment 34. Choice of fab process used 35. The number of new process steps used 36. Past cumulative volume experience with the fab process 37. Low initial fab line/die defect rates 38. Formulation of process development evolution plan 40. Use of existing cell libraries	0.32	4.68

FIGURE 3 CONCEPT MAP FOR 8 INTERVIEWEES FROM SILICON DESIGN DEPARTMENT

TABLE 6 CRITICAL SUCCESS FACTOR GROUPINGS BY 8 INTERVIEWEES FROM SILICON DESIGN DEPARTMENT

Identification Name	Critical success factors which constitute each concept	Bridging Index (Agreement Rating)	Mean Importance Rating
Concept 3.1	1. Clear chip specifications 2. Unchanged chip specifications 41. Clear upfront understanding of development requirements	0.51	5.88
Concept 3.2	14. System designer's technical competence 15. Silicon designer's technical competence 28. Early prototype of critical elements of chip 29. Early availability of system level prototypes 43. Clear detailed documentation of hand off procedure between departments	0.81	5.31
Concept 3.3	4. Technical feasibility options assessment at project start 8. Early chip manufacturing assessment 16. Silicon manufacturing technical competence 17. Product manufacturing technical competence 34. Choice of fab process used 35. The number of new process steps used 36. Past cumulative volume experience with the fab process 37. Low initial fab line/die defect rates 40. Use of existing cell libraries	0.74	4.88
Concept 3.4	3. Accurate business plan formulation at project start 10. Long term business road map formulation for the chip 21. Accurate chip volume growth estimation 22. Assessment of chip's positioning relative to competition 23. Assessment of product's positioning relative to competition 24. Assessment of chip competitor's market aggressiveness 44. Unit chip costs 45. Estimated chip price	0.03	4.08
Concept 3.5	38. Formulation of process development evolution plan 39. Fab NRE costs for chip	0.68	3.67

Concept 3.6	<ul style="list-style-type: none"> 5. Timely credible participation of other groups within the functional department 6. Timely credible participation of other functional departments 7. Prioritized individual project assignments 9. Team member co-location in same city 11. Project leader's technical competency 13. Project leader's ability to secure cooperation from other departments 25. Frequent team member communication with other groups within functional department 26. Frequent team member communication with groups from other functional departments 27. Frequent intra team member communication 42. Unchanged team member assignments for project duration 	0.22	5.16
Concept 3.7	<ul style="list-style-type: none"> 12. Project leader's chip concept vision 18. Top management support visibility for project goals 19. Resource provision by top management 20. Operational autonomy given to development team 30. Extensive customer participation 31. Extensive supplier/contractor/partner involvement 32. Use of good project management tools 33. Frequent technical milestone reviews 	0.67	4.47

FIGURE 4 CONCEPT MAP FOR 8 INTERVIEWEES FROM SILICON MANUFACTURING DEPARTMENT

**TABLE 7 CRITICAL SUCCESS FACTOR GROUPINGS BY 8 INTERVIEWEES
FROM SILICON MANUFACTURING DEPARTMENT**

Identification Name	Critical success factors which constitute each concept	Bridging Index (Agreement Rating)	Mean Importance Rating
Concept 4.1	1. Clear chip specifications 2. Unchanged chip specifications 11. Project leader's technical competency 15. Silicon designer's technical competence 16. Silicon manufacturing technical competence 41. Clear upfront understanding of development requirements	0.60	5.88
Concept 4.2	14. System designer's technical competence 17. Product manufacturing technical competence 28. Early prototype of critical elements of chip 29. Early availability of system level prototypes 34. Choice of fab process used 35. The number of new process steps used 36. Past cumulative volume experience with the fab process 37. Low initial fab line/die defect rates 40. Use of existing cell libraries	0.49	5.45
Concept 4.3	3. Accurate business plan formulation at project start 10. Long term business road map formulation for the chip 18. Top management support visibility for project goals 19. Resource provision by top management 22. Assessment of chip's positioning relative to competition 23. Assessment of product's positioning relative to competition 24. Assessment of chip competitor's market aggressiveness	0.29	4.26

Concept 4.4	<ul style="list-style-type: none"> 4. Technical feasibility options assessment at project start 8. Early chip manufacturing assessment 21. Accurate chip volume growth estimation 32. Use of good project management tools 38. Formulation of process development evolution plan 39. Fab NRE costs for chip 44. Unit chip costs 45. Estimated chip price 	0.55	4.33
Concept 4.5	<ul style="list-style-type: none"> 5. Timely credible participation of other groups within the functional department 6. Timely credible participation of other functional departments 7. Prioritized individual project assignments 9. Team member co-location in same city 12. Project leader's chip concept vision 13. Project leader's ability to secure cooperation from other departments 20. Operational autonomy given to development team 25. Frequent team member communication with other groups within functional department 26. Frequent team member communication with groups from other functional departments 27. Frequent intra team member communication 30. Extensive customer participation 31. Extensive supplier/contractor/partner involvement 33. Frequent technical milestone reviews 42. Unchanged team member assignments for project duration 43. Clear detailed documentation of hand off procedure between departments 	0.35	5.37

Table 8 compares the concept map results for all 23 respondents and for each functional department given in Table 4 and Table 5-7 respectively. In Table 8 each concept with a Bridging Index less than 0.4 is in bold letters. Concepts that share more than half of the number of their critical success factors are considered comparable and are placed in the same row. Each comparable concept has a common subset of critical success factors representing more than half of the number of critical success factors in each comparable concept. In this sense concept 1.4 is comparable to concept 2.3, 3.4 and 4.3; concept 2.3 is comparable to the remaining 3 concepts in that row; concept 3.4 is comparable to the remaining 3 concepts in that row and concept 4.3 is comparable to the remaining 3 concepts in that row. In Table 8, concepts 1.4, 2.5, 3.4 and 4.3, made up of a total of 8, 9, 8 and 7 critical success factors respectively, have 5 common critical success factors. Concepts 1.6, 2.3, 3.6 and 4.5 made up of a total of 11, 10, 10 and 15 critical success factors respectively, have 9 common critical success factors.

**Table 8 COMPARISON OF CONCEPT MAPS FOR ALL RESPONDENTS
WITH FUNCTIONAL DEPARTMENT CONCEPT MAPS**

Concepts for All Interviewees	System Design Concepts	Silicon Design Concepts	Silicon Manufacturing Concepts
1.1			
1.2			
1.3	2.6	3.3	
1.4	2.5	3.4	4.3
1.5		3.5	
1.6	2.3	3.6	4.5
1.7	2.4	3.7	
	2.1		
	2.2	3.2	
		3.1	
			4.1
			4.2
			4.4

4.3 Cluster Analysis Results

Table 9 shows the results of the hierarchical cluster analysis using forecast sales volume, gate count and wafer starts per year. In the data set, chip forecast volume ranged from 0.6 to 1028.6 K units per year; chip gate count ranged from 1520 to 156,000 gates and wafer starts per year ranged from 4 to 3849 per year.

TABLE 9 RESULTS OF CLUSTER ANALYSIS

Cluster Identification	Number of chips in cluster	Number of chips in cluster as percent of chip sample	Final Cluster Centre for Chip Forecast Sales Volume (K units per year)	Final Cluster Centre for Chip Gate Count (Number of gates)	Final Cluster Centre for Wafer starts per year (Number per year)
Cluster 1	55	65.00%	106.72	11839.40	440.46
Cluster 2	21	25.00%	77.64	34966.62	605.40
Cluster 3	8	10.00%	8.20	104043.90	225.59

In Table 9 the numbers in the columns of the variables chip forecast sales volumes, chip gate count and wafer starts per year are the final cluster centres of each variable for the corresponding cluster. The final cluster centre is the mean value of the variable for a cluster. The three clusters can be compared by the relative increase or decrease of the final cluster centre for each variable.

Table 9 shows that Cluster 1 includes 65% of the 84 chips in the sample. The chips in cluster 1 are characterized by high forecast sales volumes and low gate counts (all chips were under 20,000 gates). The average number of wafer starts per year of the chips in Cluster 1 lies between the corresponding averages for Cluster 2 and Cluster 3.

Cluster 2 includes 25% of the chips in the sample. Cluster 2 is characterized by chips with higher gate counts than those in Cluster 1 and lower gate counts than

the chips in Cluster 3. The chips in cluster 2 have lower forecast sales volumes than the chips in cluster 1 but have almost ten times the forecast sales volumes of the chips in cluster 3. The chips in cluster 2 have the highest wafer starts per year.

Cluster 3 comprises about 10% of the total sample. Chips in Cluster 3 have very high gate counts (above 60,000 gates), low forecast sales volumes and low wafer starts per year.

Chip gate count helped discriminate between the 3 clusters. However, the classification described above is based on all 3 variables used in the cluster analysis.

4.4 Concept Maps for Chip Project Types

Figure 5 and Table 10 provide the concept map for the 12 interviewees that participated in type 1 projects. Figure 6 and Table 11 provide the concept map results for the 6 interviewees that participated in type 2 projects. Figure 7 and Table 12 provide the concept map for the 5 interviewees that participated in type 3 projects. Table 13 provides a comparison of concept maps for each chip project type given in Table 10 through 12.

FIGURE 5 CONCEPT MAP FOR CHIP PROJECT TYPE 1

TABLE 10 **CRITICAL SUCCESS FACTOR GROUPINGS FOR CHIP PROJECT TYPE 1**

Identification Name	Critical success factors which constitute each concept	Bridging Index (Agreement Rating)	Mean Importance Rating
Concept 5.1	1. Clear chip specifications 2. Unchanged chip specifications 14. System designer's technical competence 15. Silicon designer's technical competence 16. Silicon manufacturing technical competence 28. Early prototype of critical elements of chip 29. Early availability of system level prototypes 41. Clear upfront understanding of development requirements	0.66	5.89
Concept 5.2	4. Technical feasibility options assessment at project start 17. Product manufacturing technical competence 38. Formulation of process development evolution plan 39. Fab NRE costs for chip	0.85	4.38
Concept 5.3	8. Early chip manufacturing assessment 34. Choice of fab process used 35. The number of new process steps used 36. Past cumulative volume experience with the fab process 37. Low initial fab line/die defect rates 40. Use of existing cell libraries	0.59	4.95
Concept 5.4	3. Accurate business plan formulation at project start 10. Long term business road map formulation for the chip 21. Accurate chip volume growth estimation 22. Assessment of chip's positioning relative to competition 23. Assessment of product's positioning relative to competition 24. Assessment of chip competitor's market aggressiveness 44. Unit chip costs 45. Estimated chip price	0.17	4.03

Concept 5.5	5. Timely credible participation of other groups within the functional department 6. Timely credible participation of other functional departments 7. Prioritized individual project assignments 9. Team member co-location in same city 13. Project leader's ability to secure cooperation from other departments 20. Operational autonomy given to development team 25. Frequent team member communication with other groups within functional department 26. Frequent team member communication with groups from other functional departments 27. Frequent intra team member communication 42. Unchanged team member assignments for project duration	0.13	5.48
Concept 5.6	11. Project leader's technical competency 12. Project leader's clear concept vision 33. Frequent technical milestones reviews 42. Clear/detailed documentation of hand-off procedure between departments	0.61	5.33
Concept 5.7	18. Top management support visibility for project goals 19. Resource provision by top management 30. Extensive customer participation 31. Extensive supplier/contractor/partner involvement 32. Use of good project management tools	0.76	4.96

TABLE 11 CRITICAL SUCCESS FACTOR GROUPINGS FOR CHIP PROJECT TYPE 2

Identification Name	Critical success factors which constitute a concept	Bridging Index (Agreement Rating)	Mean Importance Rating
Concept 6.1	1. Clear chip specifications 2. Unchanged chip specifications 4. Technical feasibility options assessment at project start 8. Early chip manufacturing assessment 28. Early prototype of critical elements of chip 29. Early availability of system level prototypes 32. Use of good project management tools 34. Choice of fab process used 35. The number of new process steps used 36. Past cumulative volume experience with the fab process 37. Low initial fab line/die defect rates 40. Use of existing cell libraries 41. Clear upfront understanding of development requirements	0.74	4.60
Concept 6.2	3. Accurate business plan formulation at project start 10. Long term business road map formulation for the chip 22. Assessment of chip's positioning relative to competition 23. Assessment of product's positioning relative to competition 24. Assessment of chip competitor's market aggressiveness 39. Fab NRE costs for chip	0.11	2.81
Concept 6.3	18. Top management support visibility for project goals 19. Resource provision by top management 21. Accurate chip volume growth estimation 38. Formulation of process development evolution plan 44. Unit chip cost 45. Estimated chip price	0.15	3.59
Concept 6.4	20. Operational autonomy given to development team 30. Extensive customer participation 31. Extensive supplier/contractor/partner involvement 33. Frequent technical milestone reviews	0.71	3.58

Concept 6.5	5. Timely credible participation of other groups within the functional department 6. Timely credible participation of other functional departments 9. Team member co-location in same city 25. Frequent team member communication with other groups within functional department 26. Frequent team member communication with groups from other functional departments 27. Frequent intra team member communication 42. Unchanged team member assignments for project duration	0.31	5.19
Concept 6.6	7. Prioritized individual project assignments 12. Project leader's chip concept vision 13. Project leader's ability to secure cooperation from other departments 43. Clear/detailed documentation of hand-off procedure between departments	0.79	4.95
Concept 6.7	11. Project leader's technical competency 14. System designer's technical competence 15. Silicon designer's technical competence 16. Silicon manufacturing technical competence 17. Product manufacturing technical competence	0.20	5.45

FIGURE 7 CONCEPT MAP FOR CHIP PROJECT TYPE 3

TABLE 12 CRITICAL SUCCESS FACTOR GROUPINGS FOR CHIP PROJECT TYPE 3

Identification Name	Critical success factors which constitute a concept	Bridging Index (Agreement Rating)	Mean Importance Rating
Concept 7.1	1. Clear chip specifications 2. Unchanged chip specifications 11. Project leader's technical competency 12. Project leader's chip concept vision 13. Project leader's ability to secure cooperation from other departments 19. Resource provision by top management 41. Clear upfront understanding of development requirements	0.54	5.91
Concept 7.2	14. System designer's technical competence 15. Silicon designer's technical competence 16. Silicon manufacturing technical competence 17. Product manufacturing technical competence 28. Early prototype of critical elements of chip 29. Early availability of system level prototypes 40. Use of existing cell libraries	0.49	5.91
Concept 7.3	5. Timely credible participation of other groups within the functional department 6. Timely credible participation of other functional departments 9. Team member co-location in same city 20. Operational autonomy given to development team 25. Frequent team member communication with other groups within functional department 26. Frequent team member communication with groups from other functional departments 27. Frequent intra team member communication 31. Extensive supplier/contractor/partner involvement 33. Frequent technical milestone reviews 42. Unchanged team member assignments for project duration 43. Clear/detailed documentation of hand-off procedure between departments	0.20	5.55

Concept 7.4	7. Prioritized individual project assignments 8. Extensive customer participation 9. Use of good project management tools	0.87	5.00
Concept 7.5	3. Accurate business plan formulation at project start 4. Technical feasibility options assessment at project start 10. Long term business road map formulation for the chip 18. Top management support visibility for project goals 21. Accurate chip volume growth estimation 22. Assessment of chip's positioning relative to competition 23. Assessment of product's positioning relative to competition 24. Assessment of chip competitor's market aggressiveness 39. Fab NRE costs for chip 44. Unit chip costs 45. Estimated chip price	0.36	3.98
Concept 7.6	8. Early chip manufacturing assessment 34. Choice of fab process used 35. The number of new process steps used 36. Past cumulative volume experience with the fab process 37. Low initial fab line/die defect rates 38. Formulation of process development evolution plan	0.41	5.42

Table 13 compares the concept map results for each chip project type given in Table 10 through 12. In Table 13 each concept with a Bridging Index less than 0.4 is in bold letters. Concepts that share more than half of the number of their critical success factors are considered comparable and are placed in the same row.

TABLE 13 COMPARISON OF CONCEPT MAPS FOR CHIP PROJECT TYPES

Concepts for All Interviewees	Concepts for chip project type 1	Concepts for chip project type 2	Concepts for chip project type 3
1.1			
1.2			
1.3			
1.4	5.4	6.2	7.3
1.5			
1.6	5.5	6.5	7.5
1.7			
	5.1		
	5.2		
	5.3		7.6
	5.6		
	5.7		
		6.1	
		6.3	
		6.4	
		6.6	
		6.7	
			7.1
			7.2
			7.4

4.5 Interviewees' Comments on Issues Related to Meeting Chip Development Interval

The 23 interviewees identified a number of issues that were associated with meeting chip development interval commitments that were not adequately addressed in the data collection instrument. These issues are listed below.

- Some projects were affected by limited availability of computing resources to engineers like number of workstations, number and kind of design toolsets.
- Awareness of the functioning of chips in end products and aware .ess of subsequent 'real world' deployment of the end product increases ownership of the chip and motivates engineers to meet project performance targets. This was cited by an engineer from the silicon manufacturing department, which is most isolated from the deployment of the end product.
- Some chip projects required simultaneous learning about the technical parameters of the chip and the building in of testability. This was most often in the case of a new chip with a new fab process. The increased technical learning frequently increased project duration and caused schedule slippages.
- There were projects in which the manager's estimates of the development effort required were faulty. This led to setting of 'impossible' schedules. This

impossible schedule also resulted due to the squeezing of time for one department when the previous department overruns schedule.

- An interviewee from the silicon design department repeatedly stressed that the existence of a well defined chip development process itself does not necessarily lead to meeting project targets. He stressed the importance of technical expertise and contribution of individual silicon designers, in addition to the development process, for meeting project targets.
- The ability to assess, at project start, and agree upon, the amount of simulation required for chip design and for process characterization contributes to meeting chip development interval commitments.
- Interviewees from the silicon design and the silicon manufacturing department stated that lack of adequate knowledge about the other departments work and constraints were a source of increased negotiation, discussion and meetings. This often contributed to lengthening of the development interval and consequent slippage in meeting chip development interval commitments.
- Cost reduction chip projects were frequently accompanied with reduction in resources. This hindered development and was a factor in meeting development interval commitments.
- No documentation/check list captures all relevant features/aspects of a project. This incompleteness could be source of inability to meet development interval commitments.

- An engineer from the silicon design department suggested that together with the frequency of technical milestone reviews, the completeness of deliverables at the milestones was also a determinant of meeting chip development interval commitments.
- An engineer from the silicon design department stated that while accurate assessment of chip volume growth was important, incorrect assessment does not imply that his performance would be measured differently. This 'incorrect' evaluation affected his commitment to a project and his meeting development interval commitments.
- Informal technical knowledge gained from activities before SRTD could play a large role in meeting chip development interval commitments.

5 DISCUSSION OF RESULTS

Section 5.1 discusses the results of the research question. Section 5.2 discusses the results for hypothesis 1. Section 5.3 discusses the results for hypothesis 2.

5.1 Hypothesis 1

There exist certain perceived critical success factors that are independent of participant functional departments and chip project types.

Please refer to Table 8 and 13 which provide comparisons of the concept map results independent of participant functional departments and chip project types. As shown in the tables, two concepts (Concept 1.4 and Concept 1.6) were similar and comparable across all interviewees irrespective of their functional affiliations or the chip project types. Each of these concepts shared more than half of their constituent critical success factors.

Concept 1.4 in Table 8 consists of critical success factors related to the chip project's business plan, assessment of chip costs, market and competition. This concept will be labelled as chip business planning in this discussion. The Bridging Index of 0.10 of this concept (Table 4) indicates high agreement on placement together of factors constituting this concept. The low mean importance rating (3.66)

given to the chip business planning concept (Table 4) indicates that interviewees perceived this concept to be of low importance for meeting chip development interval. The lack of importance may be partially explained by the cost centre operations of the captive facility. As the facility changes operations to a profit centre and increasingly competes in the open market this perceived lack of importance for the chip business planning concept for meeting chip development interval may need to be addressed.

In Table 4 the chip business planning concept includes critical success factors related to assessment of chip volume growth and assessment of chips' and end products' competition. Simultaneously interviewees rated concept 1.1 in Table 4 to be of high importance. Concept 1.1 includes, among others, critical success factors related to chip specifications. In most chip projects competitive alternative silicon implementations of the required end product features are investigated concurrently with negotiations on proposed specifications of the chip offered by the captive facility. Assessment of the chips' competition frequently brings changes to chip specifications which may cause slippages in project schedule. Thus, the low perceived importance of chip business planning and the high perceived importance given to chip specification development may cause confusion and may significantly inhibit meeting chip development interval. This confusion needs to be addressed for the facility to operate as a profit centre.

Concept 1.6 in Table 4 consists of critical success factors related to communication between departments and coordination of development activities between the participants. This concept will be labelled as communication and linkages. There was high agreement among the interviewees on the placement together of the critical success factors constituting this concept (Bridging Index 0.16). The interviewees placed high importance (Mean Importance Rating 5.39, Table 4) on this concept. This indicates that the interviewees perceived easy mutual accessibility between development personnel to be of high importance for meeting chip development interval.

In addition, Table 8 shows that there was high agreement among interviewees on the placement together of critical success factors in 2 concepts and low agreement on the placement together of critical success factors in 11 concepts. However, many of the 11 concepts with low agreement on the placement together of the constituent critical success factors, were rated to have the highest importance. This shows that even though the interviewees rated the critical success factors as being most important to meeting chip development interval they did not agree about the association of these critical success factors with any particular concept or participant group. The absence of concepts may indicate confusion about the nature of and responsibility for the critical success factors constituting the concepts. This confusion indicates that there was little agreement in the facility about who 'owned' some of the most important critical success factors that were perceived to

contribute to meeting chip development interval.

The confusion of ownership of the critical success factors related to chip specification development and chip prototype development in concept 1.1 can be especially detrimental to meeting chip development interval. As most tradeoffs are made early in the chip development process, confusion of ownership of the critical success factors in this concept can have a large impact on the project meeting the estimated development interval.

In Table 4 critical success factors constituting concept 1.2 were perceived to be of high importance to meeting chip development interval. As there was little agreement on the placement together of critical success factors, this concept cannot be examined per se. However the high importance given to the critical success factors constituting this concept, across all functional departments and chip project types, necessitated further investigation. The critical success factors are related to the technical competence of functional departments and project leader's technical competency. Although this heavy reliance on technical competence of functional departments for meeting chip development interval is not surprising, the heavy reliance on the project leaders' technical competency and chip concept vision may corroborate the case of the importance of heavy weight product managers (Clark and Fujimoto, 1991) in development projects. Further investigation of the impact of heavy weight product managers on meeting development interval in captive chip

development may have significant implications for project planning, staffing and organization.

In concepts with Bridging Indices >0.4 , the 23 interviewees assigned the following critical success factors with a mean importance rating of over 6.00-critical success factor 1(6.00), 15(6.13) and 41(6.17). The perceived high mean importance of critical success factors 1 and 41 substantiates the identification of clear upfront understanding of development requirements as key by the senior manager from the silicon design department. The perceived high mean importance of critical success factor 15, silicon designer's technical competence, may indicate that the silicon design department was perceived to play a very important role in meeting chip development interval commitments. This result needs further investigation through a larger scale survey of development personnel.

5.2 Hypothesis 2

Perceptions of certain critical success factors vary across participant functional departments.

As in the case of all interviewees, interviewees from each functional department formulated two similar and comparable concepts (Table 8)-the chip business planning concept, given in the row beginning with concept 1.4, and the

2 OF/DE 2

PM-1 3½"x4" PHOTOGRAPHIC MICROCOPY TARGET
NBS 1010a ANSI/ISO #2 EQUIVALENT

communication and linkages concept, given in the row beginning with concept 1.6. Interviewees from each functional department rated chip business planning to be of low importance and communication and linkages to be of high importance to meeting chip development interval (Table 5-7). The following discussion interprets the concepts formulated by each functional department and compares the 2 concepts outlined above, chip business planning and communication and linkages, across functional departments.

SYSTEM DESIGN DEPARTMENT

Table 5 shows that, 5 of the 6 concepts formulated by interviewees from the system design department had a Bridging Index below 0.4. This indicates that there was high agreement among the interviewees from the system design department on concepts perceived to contribute to meeting chip development interval. In fact, interviewees from the system design department agreed on the formulation of concepts more than any other functional department. Given the diverse nature of the products that the department works on, this convergence of perceptions of concepts contributing to meeting chip development interval is noteworthy.

Interviewees from the system design department formulated 3 new concepts that were not formulated by interviewees from the silicon design and the silicon manufacturing departments-concept 2.2, 2.4 and 2.6 (Table 5).

In concept 2.2 (Table 5) interviewees placed together critical success factors related to the project leader's technical competence, functional department technical competence and prototypes. This concept can be labelled as technical competence. This concept was perceived to be of high importance (Mean Importance Rating 5.70) for meeting chip development interval. The formulation of this concept and its high perceived importance can be accounted for as follows. Usually in a chip development project the manager, from the system design department, who initiates a project relies on the technical competence of functional departments for a 'smooth' chip development process and for the project meeting its estimated development interval. The end result of the chip development process is the delivery of prototypes. The system design manager uses the early availability of prototypes to evaluate the effort of the participating functional departments.

Concept 2.4 in Table 5 has critical success factors that represent the external support given to a chip development project such as top management support visibility and resource provision, customer participation, supplier/partner involvement and milestone reviews. During a chip development project, top management usually conducts milestone reviews, provides resources and negotiates with customers and partners. This concept may represent the external support provided to a chip project by top management and the system design department. This concept can be labelled as external support.

Concept 2.6 in Table 3 can be labelled as silicon manufacturing operations as it consists mainly of critical success factors related to silicon manufacturing operations such as choice of fab process, cumulative experience with the fab process and line/die yield rates. The high agreement on the placement together of these critical success factors into one concept by interviewees from the system design department is not surprising. However, as described later in this discussion, the absence of this concept from the concepts formulated by the silicon design department is noteworthy.

The chip business planning concept in the system design department (Concept 2.5, Table 5) included Fab NRE costs. This result probably reflects the fact that the system design department usually pays the NRE costs out of its product development budget. The low perceived importance given to this concept may reflect the fact that development costs for the chip do not form a major part of the system development budgets.

In concepts with Bridging Indices >0.4 , interviewees from the system design department assigned the following critical success factors with a mean importance rating of over 6.00-critical success factor 1(6.29), 41(6.29). The perceived high mean importance rating of critical success factors 1 and 41 is common with the results for all interviewees.

SILICON DESIGN DEPARTMENT

Only 2 of the 7 concepts identified by interviewees from the silicon design department had a Bridging Index of below 0.4 (Concept 3.4 and 3.6, Table 6). Five of the 6 concepts identified by the system design department interviewees and 2 of the 5 concepts identified by the silicon manufacturing department interviewees had Bridging Indices of below 0.4 (Table 8). This indicates that, in general, there was least agreement among the silicon design department interviewees on the concepts perceived to contribute to meeting chip development interval.

The communication and linkages concept (Concept 3.6, Table 6) for this department included critical success factor 11, project leader's technical competency. This is probably due to the organization of the silicon design activities such that the designers need to consult regularly with the 'design prime' or project leaders on all problem issues.

Interviewees from the silicon design department did not agree on the placement together of the prototype development related critical success factors 28 and 29 constituting concept 3.2 (Table 6). In Figure 3, the two prototype development related critical factors (number 28 and 29) were formulated spatially close to the concept 3.3 which has critical success factors related to silicon manufacturing operations. The placement of the prototype development related critical success

factors spatially close to the silicon manufacturing operations related critical success factors by many silicon design department interviewees is significant. This indicates confusion about the association of prototype development as being 'more' related to the silicon manufacturing department. Given the high perceived importance of this concept (Concept 3.2, Table 6) and the established role of prototypes in problem solving and conflict resolution (Bowen, Clark, Holloway and Wheelwright, 1994), this confusion may be an important contributor to slippages in project schedule.

Unlike the system design department, there was little agreement among interviewees from the silicon design department on the placement together of critical success factors related to silicon manufacturing operations (Concept 3.2, Table 6). The absence of this concept in the silicon design department is surprising and unexplained, given the operational 'proximity' and the heavy reliance of the silicon design department on the silicon manufacturing department.

In concepts with Bridging Indices >0.4 , interviewees from the silicon design department assigned the following critical success factors with a mean importance rating of over 6.00-critical success factors: 15(6.00), 41(6.38). The perceived high mean importance rating of critical success factors 15 and 41 is common with the results for all interviewees.

SILICON MANUFACTURING DEPARTMENT

The chip business planning concept (Concept 4.3, Table 7) included critical success factor 18-top management support visibility for project goals and critical success factor 19-resource provision by top management . This is probably due to the flat hierarchy of the department which has all engineers reporting to just one senior manager.

The communication and linkages concept (Concept 4.5, Table 7) includes more critical success factors than those in this concept in other departments. This indicates that silicon manufacturing department interviewees rely on communication and linkages in many more ways as compared to the system and silicon design department. The researcher noted this in the operations of many chip development projects, where personnel from the silicon manufacturing department were constantly requesting technical information and 'clearances' from other functional departments. The high perceived importance of this concept is similar to the importance given to this concept by other functional departments.

In concepts with Bridging Indices >0.4 , interviewees from the silicon manufacturing department assigned the following critical success factors with a mean importance rating of over 6.00-critical success factor 1(6.13), 15(6.38), 16(6.25), 28(6.00). The perceived high mean importance rating of critical success factors 1 and 15 is

common with the results for all interviewees. In addition, the perceived high mean importance rating of critical success factor 16, silicon manufacturing technical competence, is not surprising. The perceived high mean importance rating of critical success factor 28, early prototype of critical elements of chip, is probably due to the responsibility of the silicon manufacturing department to ensure on time delivery of the test chip prototypes to 'prove' the silicon design and for use by the system designers.

5.3 Hypothesis 3

Perceptions of certain critical success factors vary across chip project types.

Managers in the facility agreed that the profile of three chip project types given in Table 9 was a good representation of the sample of chip projects included in this study.

Based on the results described in Table 9 this study proposes that the chip design and manufacturing facility deals with 3 broad chip project types. The first chip project type, corresponding to the cluster 1, are projects for "small" chips that are sold in high volumes to go into different end product applications. A major portion of the sample studied in this facility consists of these 'small' chips with 'routine' manufacturing volumes. The second chip project type, corresponding to the cluster

2, are those that have more (as compared to the type 1) features and are sold in lesser (as compared to the type 1) volumes. The smaller sales volume figures for the second type may reflect the 'must do' kind of chips that the facility needs to undertake as a captive chip developer. The third chip project type, corresponding to the cluster 3, are chips with advanced features which generally "push" the technology capabilities of the organization. These chips require extensive design and manufacturing effort, enhance the technical design and manufacturing capabilities and professional status of the facility.

Please refer to Table 13 which provides a comparison of the concept map results for each chip project type. As in the case of functional departments, the concepts chip business planning (Concept 5.4, 6.2 and 7.3, Table 13) and communication and linkages (Concept 5.5, 6.5 and 7.5, Table 13) were formulated by respondents from each chip project type.

CHIP PROJECT TYPE 1

Table 13 shows that only 2 of the 7 concepts formulated by chip project type 1 interviewees had Bridging Indices below 0.4-the chip business planning concept(Concept 5.4) and the communication and linkages concept (Concept 5.5). However 4 of the 7 concepts formulated by chip project type 2 interviewees and 2 of the 6 concepts formulated by chip project type 3 interviewees had Bridging

Indices below 0.4. This indicates that there was least agreement among chip project type 1 interviewees, as compared to chip project type 2 and type 3 interviewees, on the concepts perceived to contribute to meeting chip development interval.

The low variance in the mean importance ratings of all 7 concepts formulated by chip project type 1 interviewees, with mean importance ratings ranging from 4.03 to 5.89 (Table 10), indicates that interviewees perceived all concepts to contribute almost equally to meeting chip development interval. This inability to distinguish between the relative importance of concepts perceived to contribute to meeting chip development interval is unexplained and needs further investigation.

In concepts with Bridging Indices >0.4 , interviewees from type 1 chip projects assigned the following critical success factors with a mean importance rating of over 6.00-critical success factor 1(6.42), 15(6.33) and 41(6.42). This matches the corresponding result for all interviewees.

CHIP PROJECT TYPE 2

Table 13 shows that, 4 of the 7 concepts formulated by chip project type 2 interviewees had a Bridging Indices below 0.4. This indicates that there was most agreement among chip project type 2 interviewees, as compared to chip project type 1 and type 3 interviewees, on the concepts perceived to contribute to meeting

chip development interval.

The 4 concepts with Bridging Indices below 0.4 formulated by chip project type 2 interviewees are-concept 6.2, 6.3, 6.5 and 6.7. (Table 11). Two new concepts were formulated that were absent from the concepts formulated by type 1 and type 3 chip project interviewees-Concept 6.3 and Concept 6.7.

Concept 6.3 in Table 11 had critical success factors related to chips costs, chip volume growth estimation and top management support. This concept can be labelled as chip costs and top management. Chip project type 2 interviewees were in high agreement about the placement together of the factors constituting this concept (Bridging Index 0.15, Table 11). The formulation of this concept may be due to the 'must do' nature of the chips in chip project type 2. These chip projects may be 'unattractive' to work on for the development personnel as the chips do not significantly enhance the technical reputation of the facility. As a result, these chip projects may constantly require top management support. In addition the chips may be highly sensitive to unit chip costs due to the high number of wafer starts per year. Any change in either of the two critical success factors described above may have serious implications for chip project type 2. This may account for the placement together of critical success factors related to top management support together with unit chip costs into one concept. This concept was rated to be of low importance to meeting chip development interval. Given the vulnerability of these

projects described above, the low perceived importance is surprising and needs to be further investigated.

Critical success factors constituting concept 6.7 (Table 11) are related to the competence of functional departments and of the project leader. This concept may be labelled as participant expertise. The formulation of this concept may be due to the increased technical complexity, in terms of gate count, of the chips constituting chip project type 2. The increased technical complexity of chips may also account for the high perceived importance of participant expertise for meeting chip development interval.

In concepts with Bridging Indices >0.4 , interviewees from type 2 chip projects assigned the following critical success factors with a mean importance rating of over 6.00-critical success factor 13(6.00). The perceived high mean importance rating of critical success factor 13, project leader's ability to secure cooperation from other departments, may be linked to the increased technical complexity of the chips entailing a need for more skills, knowledge and resources from other departments. This result however needs further broad based investigation.

CHIP PROJECT TYPE 3

The Bridging Indices of the 2 of the 6 concepts formulated by chip project type 3

interviewees (Table 12) were below 0.4.

The chip business planning concept for chip project type 3 (concept 7.5, Table 12) includes the critical success factors related to unit chip costs and chip price. The significance of the inclusion of these critical success factors in this concept is unknown and merits further investigation.

Concept 7.6, with a Bridging Index of 0.41, has critical success factors related to silicon manufacturing operations. As the Bridging Index for this concept is just over the limit of 0.4, the researcher considers the critical success factors placed together to form a concept. Chips from project type 3 usually use new fabrication processes with which the facility has little previous experience. The formulation of the silicon manufacturing concept may be due to the increased dependence of development personnel working on type 3 chip projects on the silicon manufacturing department.

In concepts with Bridging Indices >0.4 , interviewees from type 3 chip projects assigned the following critical success factors with a mean importance rating of over 6.00-critical success factor 1(6.40), 11(6.20), 14(6.20), 15(6.40), 16(6.20), 28(6.00), 29(6.20) and 41(6.20). The perceived high mean importance rating of critical success factor 1, 15 and 41 matches the results for all interviewees. The perceived high mean importance rating of critical success factor 11, 14, 16, 28 and 29, related to technical competence of project leader, development personnel and to prototype

development may be due to the absence of previous experience with the technically complex type 3 chips and the use of new fabrication process variations.

6 CONCLUSIONS

6.1 Conclusions

This study used meeting planned chip development interval as the key success measure for a captive chip development facility.

This study concludes that communication and linkages between functional departments participating in the chip development process is perceived to be an important determinant of successful captive chip development. The formulation of this concept and its perceived importance was independent of participant functional department and chip project type. Development personnel from all participating functional departments and across all chip project types place high value on their mutual accessibility and rely on communication with each other to meet chip development interval commitments. This result corroborates with findings of other studies such as (Clark and Fujimoto, 1991) on the importance of internal integration for successful product development.

The chip business planning concept exists across all functional departments and chip project types. Development personnel in the in the system design, silicon design and the silicon manufacturing departments of the company view the chip business planning concept as being of low importance (mean importance rating

3.46, 4.08 and 4.26 respectively), as compared to the importance given by each functional department to the communication and linkages concept, for meeting chip development interval commitments. This conclusion contrasts with the importance given to external integration (Clark and Fujimoto, 1991) for successful product development. As the facility changes operations from a cost centre to a profit centre and as the facility increasingly competes openly this perceived low importance given to chip business planning for meeting chip development interval needs to be addressed.

The perceived low importance of chip business planning by the functional departments is inconsistent with the perceived high importance of clear chip specifications and may be a frequent source of changes in chip projects requirements. Addressing this inconsistency can bring improvements in chip project planning and can increase the likelihood of projects meeting the estimated development interval.

Development personnel from all functional departments are unclear about ownership of the critical success factors constituting the concepts that they believe contribute most to meeting chip development interval. Given the importance of ownership and commitment (Bowen, Clark, Holloway and Wheelwright, 1994) the absence of clarity on ownership of key critical success factors needs to be addressed. Better definition of the responsibility for the critical success factors

constituting these concepts, which are related to activities preceding actual development, can improve meeting chip development interval commitments.

Heavy weight product managers were perceived to be of high importance for meeting chip development interval. This result corroborates with the findings of previous research (Clark and Fujimoto, 1991) but needs to be further investigated in the particular instance of captive chip development.

In concepts with Bridging Indices >0.4 , all 23 interviewees assigned critical success factors 1, 15 and 41 with a mean importance rating of over 6.00. The perceived high mean importance of critical success factors 1 and 41 related to clear upfront understanding of development requirements is similar to the findings of Zirger and Madique, 1990. The perceived high mean importance of critical success factor 15, silicon designer's technical competence, may indicate that the silicon design department was perceived to play a very important role in meeting chip development interval commitments. This result needs further investigation through a larger scale survey of development personnel.

Two similar and comparable concepts contributing to meeting chip development interval were formulated by each functional department-chip business planning and communication and linkages. Interviewees from each functional department perceived chip business planning to be of low importance and communication and

linkages to be of high importance to meeting chip development interval.

Interviewees from the system design department agreed most on the concepts contributing to meeting chip development interval. Interviewees from the system design department formulated three new concepts contributing to meeting chip development interval that were not formulated by interviewees from the silicon design and the silicon manufacturing departments-technical competence, external support and silicon manufacturing operations. Technical competence was perceived to be of high importance. This result corroborates with the findings of other studies such as Zirger and Madique (1990) and Cooper and Kleinschmidt (1994). The external support concept and the silicon manufacturing operations concept were both perceived to be of lesser importance than technical competence for meeting chip development interval.

Clark and Fujimoto (1991) and Bowen, Clark, Holloway and Wheelwright (1994) found that prototyping was critical to shortening product development interval. The absence of agreement among interviewees from the silicon design department on the placement together of prototype development related critical success factors may inhibit meeting chip development interval. The absence of the formulation of the silicon manufacturing operations concept by interviewees from the silicon design department is unexplained.

Interviewees from the silicon manufacturing department gave a wider description of the communication and linkages concept than the system design and the silicon design departments. This may indicate that the silicon manufacturing department was more dependent on collaboration with other functional departments as compared to the system design and the silicon design departments.

3 types of chip development projects were identified using three variables: chip forecast sales volume, chip gate count and wafer starts per year. Chip gate count helped discriminate between the chip project types. Forecast sales volume and wafer starts per year vary irregularly in the facility's projects. The existence of a policy to undertake only specific type of projects may help focus the facility's development effort.

As in the case of functional departments, interviewees from each of the 3 chip project types formulated 2 similar and comparable concepts-chip business planning and communication and linkages.

Chip project type 1 interviewees did not discriminate between the relative importance of the 7 concepts perceived to contribute to meeting chip development interval. This result is unexplained and needs further investigation.

Chip project type 2 interviewees were in more agreement than chip project type 1

and type 3 interviewees on the formulation of concepts that were perceived to contribute to meeting chip development interval. Chip project type 2 interviewees formulated 2 new concepts that were absent among those formulated by chip project type 1 and type 3 interviewees-the chip costs and top management concept and the participant expertise concept. The low perceived importance of chip costs and top management, by chip project type 2 interviewees, for meeting chip development interval is surprising and unexplained. The high perceived importance of participant expertise for meeting chip development interval may be explained by the increased technical complexity of chips in type 2 chip projects.

Chip project type 3 interviewees formulated a concept with a Bridging Index of 0.41 with critical success factors related to silicon manufacturing operations. This concept may have been formulated due to the new fab process that are used in type 3 chip projects.

Interviewees' comments on the lack of adequate knowledge about other departments' work reinforce the perceived importance given to the communication and linkages concept. Comments regarding issues such as awareness of the functioning of chips in the end products, difficulty of simultaneous technical learning and building in of testability, estimation of amount of simulation required need to be addressed by managers in the facility. The comments by interviewees on issues related to meeting chip development interval may affect the conclusions described

above. The absence of the many of the issues, mentioned by the interviewees, in academic literature suggest the need for further investigation.

6.2 Contribution

Discussion of the contribution of this study has been organized in two parts: contribution to management practise and contribution to the academic literature.

Contribution to Management Practise

First, this study provides managers with a method for classifying chip development projects into mutually exclusive, non overlapping groups using both technical and business criteria. This method provides functionally focussed managers with better understanding of a semiconductor company's product portfolio.

Second, this study highlights the 'glue' that binds together elements of success full captive chip development. The explication of this 'glue' provides managers with a shared view of those aspects of captive chip development that are perceived to be of high importance to meeting chip development interval. The results of this study can be used by managers for improved integration of the chip development process by setting objectives for continuous improvement and training programs for development personnel. Better knowledge of critical success factors can help

improve coordination within and across projects. Comparison of critical success factors across functional departments can assist in the development of mechanisms to improve coordination across functional departments. Findings of this study can facilitate business planning with meaningful participation of functional departments.

Third, measures can be developed and applied for improved evaluation of chip development projects. The findings of this study can be used to develop a commitment management system for areas for which commitments from all functional departments are required to meet development interval. For example, one of the areas needing improved commitment management highlighted by this study is prototype development and delivery. Organization of a commitment management system for improved prototype development and delivery can provide substantial rewards to the facility.

Fourth, another motivation for this study was to understand what skills and attitudes are critical in development personnel of captive semiconductor design and manufacturing facilities. Managers can use the findings of this study to better understand the organizational changes required to move from operating as a cost centre to operating as a profit centre. The organizational changes include changes in development procedures and in managers' skills, attitudes and development approach.

Contribution to the Academic Literature

First, this study contributes to the literature on key success factors of product development interval. This research provides empirical evidence of the links between attaining development interval targets and development process characteristics.

One of the motivations of this study was to contribute to the new product development literature on perceptions of critical success factors for product development interval that are specific to project types and functional departments. This study examines the differences in perceived rankings of critical success factors across chip project types and functional departments. Previous academic literature has used higher aggregates, like industry types (Eisenhardt and Tabrizi, 1995) and product types (Lee and Na, 1994), as contingency or controlling factors. This is the first study, to the researcher's knowledge, that investigates the differences in perspectives on critical success factors between functional departments.

6.3 Limitations

The sample for this study consists of 84 chip development projects from a single captive semiconductor unit. This limits the generalizability of the findings of this study. Decisions such as what design capabilities to build, what volumes to

manufacture internally and what volumes to outsource are almost completely dependent on the parent company's size, position, product mix and corporate strategy. As these conditions are company specific the findings of this study may not hold true for other companies. The methods, tools and research design of this study, however, provide relevant templates that can be used by other semiconductor firms.

A second limitation of this study is that success factors are considered at the project level. Hence, any findings and conclusions reached need cautious interpretation because linkages between a product development project and other projects have not been explicitly researched.

A third limitation of this study is that all factors will be measured retrospectively, which may introduce some after-the-fact rationalization. However, this retrospective method is common in this type of empirical research.

Fourth, data has been collected on perceptions of how important certain critical success factors are in meeting planned chip development interval, but data has not been collected to test whether the critical success factors are in fact related to meeting planned chip development interval. For example, it is necessary to investigate whether there is a significant relationship between the extent to which specifications are clear (Critical success factor 1, Table 3) and meeting planned

chip development interval. One possible source of misconceptions might be the tendency to blame others when the actual minus the planned development interval is long.

Fifth the existence of other factors such as transfer of learning from previous projects, simultaneous testability requirements and existence of pre development simulation information have not been controlled for. There exist other methods of classification of products and product development projects such as incremental and radical products. While this study examined differences in perceptions of critical success factors according to functional departments and chip project types, it has not examined differences in perceptions according to incremental and radical chips.

6.4 Future Research

Investigation of the importance of heavy weight product managers in captive chip development projects is a fruitful avenue for further research.

As stated earlier, most important trade offs in captive chip development are made very early in the development project. Further research could be carried out to investigate the effect of lack of ownership of critical success factors at the pre-development and early stages of a captive chip development projects.

The benefits of improved interdepartmental coordination differ across participating functional departments, with one unit having more incentive to coordinate than the other. Future research could be done on what the incentives are, for different functional departments, to cooperate in the implementation of the success factors identified in this study.

This is a cross sectional study. A longitudinal study for identification of chip development success factors at progressive stages of a chip development project is another avenue for useful further research.

The concepts contributing to meeting chip development interval in a captive facility identified by this study can be compared with the concepts contributing to meeting chip development interval in other semiconductor firms which operate on a profit centre basis. Future research on this topic could provide valuable guidance for chip development facilities planning to change their operations.

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APPENDIX A

Protocol for Interviews with Senior Managers

DETERMINANTS OF SUCCESSFUL SEMICONDUCTOR DESIGN AND MANUFACTURE FOR A CAPTIVE FACILITY

INTERVIEW PROTOCOL

Part 1

Please answer the following questions:

Q. 1

Would you use chip development interval or meeting deliverables in all gates between SRTD and SRTV as the measure of success ?

Q. 2

What other measure of success would you use ?

Q. 3

What factors contribute to the success measure used in Question 1 ?

Q. 4

What phrases or words would you use to describe the factors identified in Question 3 ?

Q. 5

How would you classify the chips developed in this facility ? What dimensions would you use ?

Q. 6

What are the engineering groups involved in the design and manufacture of chips?

Q. 7

Do the groups identified in Question 6 agree on the definition of success ?

Q. 8

What factors would each group, identified in Question 6, believe contribute most to chip development success ?

Part 2

The research questions driving this research are:

Research Question 1

What are the critical success factors for meeting IC development interval in a captive semiconductor design and manufacturing unit ?

Research Question 2

How do critical success factors vary across participant functional departments ?

Research Question 3

How do critical success factors vary across chip development project types?

Please provide suggestions and comments as requested by the researcher.

APPENDIX B QUESTIONNAIRE

DETERMINANTS OF SUCCESSFUL SEMICONDUCTOR DESIGN AND MANUFACTURE FOR A CAPTIVE FACILITY

PART 1

This questionnaire pertains to the development project for chip _____
which was a component of _____

I was involved in ☐ System Design ☐ Silicon Design
 ☐ Silicon Manufacturing ☐ Product Manufacturing

At the time of this development project I was Band _____

I participated in this project in my capacity as (please check only one)
 ☐ Manager ☐ Engineer

This chip was part of a product
 ☐ Cost Reduction ☐ New Line

The chip represented technical innovation that can be classified as (please check only one)
 ☐ Incremental ☐ Radical

This chip was of type ☐ Gate Array ☐ Cell Based
 ☐ Full Custom Other _____

[NOTE: Following question for respondents from Silicon Design only]:

Please estimate the percentage of the design that was copied (e.g. repeated cells)
as: _____ % of total gates

From my perspective the priorities for this chip development project were:

Meeting Chip Development Budget	_____	%
Meeting Chip Functionality Requirements	_____	%
Meeting Chip Development Interval	_____	%
Other _____	_____	%
(Please specify)		

Total 100 %

PART 2

NOTE: While answering the questions listed below please keep in mind the development project for chip _____ which was a component of _____

Please use the following **DEFINITIONS** for further answers in this questionnaire:

- Chip development interval is met when the actual delivery for a chip (SRTV) occurs on the week specified in the delivery plan decided upon on at the time that the chip's specifications were agreed upon (SRTD).
- The word 'functional department' below refers one of the 4 departments that you may belong to: System Design, Silicon Design, Silicon Manufacture and Product Manufacture.

NOTE: Please try to use the entire scale in your answers below.

NOTE: Please mark NA if you do not know enough about a statement or if you think that a statement is irrelevant to the project.

Please rate each statement given below as it applies to meeting chip development interval, as defined above, for chip _____

	NOT IMPORTANT					IMPORTANT	
1 Clear chip specifications	1	2	3	4	5	6	7
2 Unchanged chip specifications	1	2	3	4	5	6	7
3 Accurate business plan formulation at project start	1	2	3	4	5	6	7
4 Technical feasibility options assessment at project start	1	2	3	4	5	6	7
5 Timely credible participation of other groups within the functional department	1	2	3	4	5	6	7
6 Timely credible participation of other functional departments	1	2	3	4	5	6	7
7 Prioritized individual project assignments	1	2	3	4	5	6	7
8 Early chip manufacturing assessment	1	2	3	4	5	6	7
9 Team members co-location in same city	1	2	3	4	5	6	7
10 Long term business road map formulation for the chip	1	2	3	4	5	6	7
11 Project leader's technical competency	1	2	3	4	5	6	7
12 Project leader's chip concept vision	1	2	3	4	5	6	7

	NOT IMPORTANT					IMPORTANT	
13 Project leader's ability to secure cooperation from other departments	1	2	3	4	5	6	7
14 System designer's technical competence	1	2	3	4	5	6	7
15 Silicon designer's technical competence	1	2	3	4	5	6	7
16 Silicon manufacturing technical competence	1	2	3	4	5	6	7
17 Product manufacturing technical competence	1	2	3	4	5	6	7
18 Top management support visibility for project goals	1	2	3	4	5	6	7
19 Resource provision by top management	1	2	3	4	5	6	7
20 Operational autonomy given to development team	1	2	3	4	5	6	7
21 Accurate chip volume growth estimation	1	2	3	4	5	6	7
22 Assessment of chip's positioning relative to competition	1	2	3	4	5	6	7
23 Assessment of product's positioning relative to competition	1	2	3	4	5	6	7
24 Assessment of chip competitor's market aggressiveness	1	2	3	4	5	6	7
25 Frequent team member communication with other groups within functional department	1	2	3	4	5	6	7
26 Frequent team members communication with groups from other functional department	1	2	3	4	5	6	7
27 Frequent intra team member communication	1	2	3	4	5	6	7
28 Early prototype of critical elements of the chip	1	2	3	4	5	6	7
29 Early availability of system level prototypes	1	2	3	4	5	6	7
30 Extensive customer participation	1	2	3	4	5	6	7
31 Extensive supplier/ contractor/ partner involvement	1	2	3	4	5	6	7
32 Use of good project management tools	1	2	3	4	5	6	7

	NOT IMPORTANT					IMPORTANT	
33 Frequent technical milestone reviews	1	2	3	4	5	6	7
34 Choice of fab process used	1	2	3	4	5	6	7
35 The number of new process steps used	1	2	3	4	5	6	7
36 Past cumulative volume experience with the fab. process	1	2	3	4	5	6	7
37 Low initial fab line/die defect rates	1	2	3	4	5	6	7
38 Formulation of process development evolution plan	1	2	3	4	5	6	7
39 Fab NRE costs for chip	1	2	3	4	5	6	7
40 Use of existing cell libraries	1	2	3	4	5	6	7
41 Clear upfront understanding of development requirements	1	2	3	4	5	6	7
42 Unchanged team member assignments for project duration	1	2	3	4	5	6	7
43 Clear/detailed documentation of hand off procedure between departments	1	2	3	4	5	6	7
44 Unit chip costs	1	2	3	4	5	6	7
45 Estimated chip price	1	2	3	4	5	6	7

What issues contributing to meeting chip development interval have not been captured in the statements above ?

What would you do differently if you had to do the project again ?

THANK YOU FOR YOUR COOPERATION.

END

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