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MOSFET Based Gamma Radiation Detector

by

Chris Peters

This thesis is submitted to the Faculty of Graduate
Studies and Research in partial fulfillment
of the requirements for the degree of

Master of Engineering

Ottawa-Carleton Institute for Electrical Engineering

**Department of Electronics
Faculty of Engineering
Carleton University
Ottawa, Canada**

January, 1992

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ISBN 0-315-76022-2

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and Research the acceptance of the thesis:

"MOSFET Based Gamma Radiation Detector"

Submitted by Chris Peters in partial fulfillment of the
requirements of the degree of Master of Engineering.

_____
Prof. N. G. Tarr
Thesis Supervisor

_____
Chairman,
Department of Electronics

ABSTRACT

A novel MOSFET based gamma radiation detector (RADFET) has been designed, fabricated and tested. The new RADFET is essentially a floating gate MOSFET. In addition large extensions over the field oxide have been attached to the floating gate and the control gate. The new structure reduces the subthreshold slope while maintaining the thick gate oxide required to obtain sensitivity to ionizing radiation. A second feature of the new RADFET is a decreased sensitivity to interface states and to radiation induced interface states.

The RADFETS were fabricated and tested with a Co^{60} gamma radiation source. The data indicate a large density of fast interface states were created during processing. The charging of these states prevented measurements at doses less than a few rads (Si). The sensitivities of the RADFETS tested were equal to or greater than any previous reported results.

ACKNOWLEDGEMENTS

I would like to thank my supervisor, Garry Tarr, for his useful advice and guidance in this work. The discussions with Ken Shortt on radiation physics and dosimetry and the use of the Co⁶⁰ source are very much appreciated. Thanks to Lyall Berndt, Carol Adams and Anne Ruhmland who did an excellent job in fabricating the RADFET's. But above all, it was all my fault.

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CHAPTER 1

INTRODUCTION

In 1962 several high altitude nuclear tests were conducted by both the United States and the Soviet Union. These tests caused significant radioactive contamination of the exosphere. The increased radiation resulted in the failure of the experimental satellite, Telstar 1. This vulnerability spurred research into the effects of ionizing radiation on electronic devices⁽¹⁾. The vast majority of this research was concentrated in the development of methods to minimize the deleterious effects of radiation on circuits designed for use in space or the military. Hence, the primary interest has been in large dose rates and large doses, $>1 \text{ rad/sec}$ up to Mrad/sec for a nuclear blast. More recently, attempts have been made to turn what was originally a problem into a useful tool as a dosimeter or a radiation detector^(2,10). This research, in many ways, is the reverse of the military work in that the interest is in the enhancement of some of the effects of the radiation and generally deals in very low dose rates, $< \text{mrad/sec}$. In either case, the scientific goal is in the understanding the effects of radiation on MOS devices.

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* One RAD is 100 ergs of energy deposited per gram of material. 1 Gray (Gy) = 100 RADS.

Considering an n-channel MOS (NMOS) transistor, ionizing radiation is absorbed in the gate oxide producing electron-hole (e-h) pairs^(3,11), figure 1.1(A). The electrons are swept out through the gate while the holes are transported to the Si-SiO₂ interface where they are trapped⁽¹²⁻¹⁴⁾. This positive interface charge causes a negative shift in the threshold voltage (V_t). The magnitude of the shift can be several volts for high radiation doses. Few circuits can function normally given such large threshold voltage changes. A second radiation effect is the build up of interface states^(1,15,16). Interface states can trap charge tunnelling into the oxide from the substrate, resulting in a shift in the threshold voltage. Interface states also degrade the transconductance of the transistor^(7,8). All designs for MOS radiation sensors or RADFET's, as they have come to be known, have made use of the first of these two effects, ie. the radiation induced V_t shift. The V_t shift is proportional to dose at low doses, <1Krad, hence, one need only measure the change in V_t with some simple circuitry to determine the dose.

The major issues in the design of a dosimeter are linearity, sensitivity, energy response and readout. At present, film badges and thermoluminescent devices (TLD's) are commonly used as dosimeters. At the photon energy of interest, ~1 MeV, the sensitivities of these dosimeters are 5 mrad and 10 mrad, respectively⁽⁶²⁾. RADFET's designed so far can detect doses of ~100 mrad⁽⁶³⁾. All these dosimeters exhibit

FIGURE 1.1: A) Basic RADFET (cross-section)
B) EPROM-like RADFET (cross-section)
C) EPROM-like RADFET (plan view)

linear behaviour at suitably low doses and have similar energy responses: increasing sensitivity with decreasing energy.

The principle advantages of RADFET's over the conventional dosimeters are size and simplicity of measurement. The RADFET and readout circuitry can be incorporated into a single VLSI chip allowing virtually instant readout. Film badges and TLD's can be small but the dose cannot be determined quickly and this measurement always results in the destruction of the information. The measurement of V_T has virtually no effect on the stored charge in a RADFET.

Most previous RADFET designs have consisted of single or matched pair of MOSFET's with a thick gate oxide, $>0.1\mu\text{m}^{(1,12)}$. Attempts have been made to increase the density of trapped holes through deliberate doping of the gate oxide⁽⁵⁾ and the use of novel gate dielectrics⁽⁶⁾ but the basic design has not been altered. Sensitivities as high as 4 mV/rad have been reported for these devices^(9,61). The intended purpose for these RADFET's has primarily been in the high dose regime, such as that encountered in radiotherapy, where small size is advantageous and sensitivity is a secondary issue.

In this work, we have attempted to improve the design of the RADFET for use in occupational environments such as nuclear power reactors and experimental and medical facilities where very low doses and dose rates are expected. The small size and immediate readout capability should improve the

utility of the dosimeter. Instead of a simple thick gate oxide MOSFET, we have studied an EPROM-like device, figure 1.1(B) onto which two large wing-like extensions have been attached. The wings, attached to the control and floating gates, are responsible for the charge collection. This design was intended to improve the stability of the RADFET by decreasing its sensitivity to radiation induced interface states and by increasing the transconductance compared to a standard floating gate MOSFET.

Further details of this new RADFET and the theory of its operation are presented in chapter 3. Chapter 2 provides a background in the relevant radiation physics and charge transport theory. A description of the fabrication of experimental RADFET's and their testing with a Co^{60} gamma source is given in chapter 4. The results and discussion can be found in chapter 5. The conclusions are in chapter 6.

CHAPTER 2

PHYSICS OF RADFET's

2.1 INTERACTION OF HIGH ENERGY PHOTONS WITH MATTER

Compton scattering is the basic mechanism by which electron-hole pairs are created by high energy photons in the oxide of a RADFET⁽¹⁾. The Compton effect is defined as the scattering of a photon by a free electron, although the process is not affected if the binding energy of the electron is much less than the photon energy^(17,18). At energies comparable to and somewhat greater than the binding energy (~100 keV for Si) the scattering is dominated by the photoelectric effect⁽¹⁷⁾. Figure 2.1(a) depicts a Compton scattering event. For the energies of interest here, ~1 MeV, the scattering is predominately in the forward direction with a mean energy transfer of 45%. The average electron scattering angle is ~17°. The Compton attenuation coefficient of photons at 1 MeV in Si and SiO₂ is very small, 0.06cm²/g, hence one need not consider multiple scattering in the thin structures of a RADFET. The photon directly creates only a single (e-h) pair. Unlike photons, charged particles have a large scattering cross section in condensed matter. It is the subsequent scattering of the secondary electrons, which have an average energy of 0.5 MeV^(17,18), that creates the vast majority of e-h pairs. The scattered electron creates other

FIGURE 2.1: A) a Compton scattering event
 B) photons incident on a slab showing the build up of charged particles

energetic free electrons which in turn are scattered. This process continues until all of the energy originally lost by the photon is spent in the creation of e-h pairs. The average energy required to produce one e-h pair is 17 eV^(1,3).

2.2 CHARGED PARTICLE EQUILIBRIUM

The discussion above assumed that no secondary electron escaped the solid prior to depositing all of its energy. Consider a thick slab, onto which there is an incident beam of gamma particles, figure 2.1(B). A small volume near the front of slab will have a higher number of electrons leaving it than entering it. The penetration depth of the secondary electrons is tens of microns. Until they have travelled at least this distance, they will still be capable of creating other energetic electrons. At a depth equal to the penetration depth of the most energetic secondary electron, the density of charged particles will reach a constant value, since as many will enter as leave any volume. This condition is known as *charged particle equilibrium*^(1,17,18). The largest energy dose is delivered to regions in equilibrium and therefore, this is where the active area of the RADFET should be placed. The *build-up layer*, figure 2.1(B), need not be the same material as the dosimeter as long as charged particle equilibrium is obtained. All RADFET's in this work were coated in paraffin wax (~4 mm) to obtain equilibrium. A Monte Carlo simulation of the build up curve for paraffin is shown in figure 2.2⁽¹⁹⁾.

FIGURE 2.2: A Monte Carlo simulation of charge build in paraffin wax; 14% hydrogen and the remainder carbon.

2.3 DOSE

The calculation of the absorbed energy for a system in charged particle equilibrium (CPE) is straightforward. As discussed in section 2.2, one need only calculate the energy lost by the photons. The dose or energy adsorbed per unit mass is given by :

$$D_{eq} = \phi \mu_{en}/\rho \quad (2.1)$$

where ϕ is the photon fluence (Mev/cm^2), μ_{en} is the energy absorption coefficient and ρ is the density. μ_{en}/ρ is known as the *mass energy attenuation coefficient*. The dose measured in one material, in CPE, can be related to the dose in another material through the relation⁽¹⁸⁾:

$$\frac{D_1}{D_2} = \frac{\mu_{en}/\rho)_1}{\mu_{en}/\rho)_2} \quad (2.2)$$

It was estimated that 90% of the secondary electrons in the SiO_2 originate in the paraffin. In the RADFET's tested the SiO_2 layer is not in CPE. The appropriate equation for the dose in the SiO_2 layer is:

$$D_{\text{SiO}_2} = \frac{S_{\text{SiO}_2}}{S_{\text{max}}} D_{\text{max}} \quad (2.3)$$

where 'S' is the *electron mass stopping power*.

Combining equation 2.2 and 2.3, the dose in the SiO_2 layer is given by:

$$D_{SiO_2} = \frac{S_{SiO_2} \mu_{en}/\rho}{S_{max} \mu_{en}/\rho} \Big|_{H_2O}^{max} D_{H_2O} \quad (2.4)$$

Paraffin was considered to be 86% carbon and 14% hydrogen. Silicon dioxide behaves very much like silicon so the values for Si were used in equation 2.4. All the values for S and μ_{en}/ρ were obtained from references 17 and 18.

The strength of the Co^{60} source used was 95 rad/min at one meter in water. This translates to 93 ± 5 rad/min at one meter in SiO_2 .

2.4 BASIC RADFET

The vast majority of RADFET's have been little more than thick gate oxide MOS transistors. Both n-channel and p-channel devices have been used. As shown in figure 2.3(A), for a n-channel device under positive gate bias, the e-h pairs generated by the radiation are separated in the oxide. The electrons drift to the gate where they are removed from the system. The holes migrate towards the Si-SiO₂ interface and are trapped within a few nanometers of the substrate⁽¹²⁻¹⁴⁾. Positive charge trapped at the interface causes a threshold voltage shift (ΔV_T) proportional to the gate oxide capacitance (C_{ox}): $\Delta V_T = -Q/C_{ox}$, where Q is the charge/area. The sign of the shift is opposite to that of the trapped charge so that for holes the shift in V_T is negative while the shift is positive for electrons. If the charge is trapped in the bulk of the oxide the shift is reduced to:

$$\Delta V_T = -1/C_{ox} \int x \rho(x)/t_{ox} dx \quad (2.5)$$

FIGURE 2.3: A) Basic RADFET
B) Band diagram of a RADFET under positive bias. Electrons and holes not trapped at the surface will simply fall into the substrate

where t_{ox} is the oxide thickness, $\rho(x)$ is the trapped charge density and the distance (x) is measured from the gate. The shift is greatest if the charge is trapped near the Si-SiO₂ interface and is zero for charge trapped at the gate.

Subsequent to the creation of an e-h pair, three events must occur to produce a maximum shift in the threshold voltage. First, the e-h pair must be separated by the electric field in the oxide before it simply recombines. Second, the electrons must drift to the gate and the holes to the Si-SiO₂ interface. Third, the holes must be trapped at or near the interface. The band structure is such that holes not trapped will enter the substrate, see figure 2.3B. The first of these conditions has been investigated both experimentally and theoretically. The experimental result on the ratio of e-h pairs separated to the number produced (the yield) vs. the oxide electric field is depicted in figure 2.4 for both Co⁶⁰ and 12 Mev electron radiation^(11,20). One can see that above ~0.5 MV/cm the yield is >0.7 but drops off very quickly at lower fields.

2.5 ELECTRON AND HOLE TRANSPORT IN SiO₂

Once the electron and hole have been separated, they must be transported through the oxide. The electron drifts under the electric field in the conduction band with a mobility of $\sim 20 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at 300 K and $\sim 40 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at 80 K and is therefore quickly swept out of the oxide⁽²¹⁾. The hole

FIGURE 2.4: Fractional yield verses applied electric field for a MOS capacitor. Fractional yield is the relative number of e-h pairs which escape recombination.

on the other hand, moves through the oxide via hopping conduction^(22,23) with an effective mobility of $\sim 10^{-4} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at 300 K and $\sim 10^{-11} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at 80 K. The hole takes 10^6 to 10^{13} times longer than the electron to move through the oxide. The hole mobility at low temperatures is so small that the hole is essentially trapped at the point it is created. There are two time scales for the hole transport, prompt and late. Prompt transport takes place within 10^{-5} seconds of generation with a mobility of $2 \times 10^{-5} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. It is speculated that during this time the hole hops between nearest neighbour nonbonding 2p oxygen orbitals⁽²³⁾, and travels on average only 10 nm before becoming self trapped as a small polaron. The hole then proceeds to move towards the interface by hopping between these localized states (small polaron) under the direction of the electric field. The localized sites are 2p nonbonding oxygen orbitals but due to disorder in the oxide they lie above the valence band mobility edge. The sites have a wide range of spatial distributions, and hence, a wide range of overlap integrals (hopping probabilities) causing the conduction to be strongly dispersive in time. The theory of continuous time random walks^(1,24,25) (CTRW) has been used to describe hopping conduction in SiO_2 . The basic feature of CTRW theory is that conduction occurs via phonon assisted hopping between localized sites which are randomly distributed in both space and energy. The term *dispersive conduction* refers to a time dependent mobility. Assume any distribution of holes in

the oxide. As time proceeds after the application of an electric field there will be a build-up of holes in the deep level traps and a concomitant decrease in the effective mobility. This behaviour is depicted in figure 2.5. The basic result for the current as function of time is:

$$I(t) \sim \begin{cases} t^{-(1-\alpha)} & t < t_r \\ t^{-(1+\alpha)} & t > t_r \end{cases} \quad (2.6)$$

$$t_r = [\rho/L(E)]^{1/\alpha} e^{\Delta/kT}$$

where ρ is the sample thickness, Δ is an activation energy for the transport and $L(\xi)$ is the average displacement per hop which is dependant on the electric field, E . In SiO_2 it has been found that the value of ' α ' is $1/4$.

The discussion, thus far, has assumed that given sufficient time all the holes will reach the interface. In all oxides there are deep level hole traps which essentially prevent all the charge from reaching the interface.

2.6 HOLE TRAPS

The density and distribution of hole traps depends on the oxide quality. "Good" oxides have a high density of traps within 5 nm of the interface with an exponential decay into the bulk⁽²⁷⁻²⁹⁾. The trap densities⁽³⁰⁾ near the interface range from 10^{18} to 10^{19} cm^{-3} .

The nature of the oxide hole traps offers an explanation

FIGURE 2.5: Integrated current in a MOS capacitor following a 3nsec irradiation. The slope of the curve is the hole current. reproduced from reference [1].

as to why they are abundant at the interface. It is believed that most hole traps are E' centers^(31,32), figure 2.6. The E' center is an oxygen vacancy, figure 2.6(B), in which there are two Si atoms each back bonded to three oxygen atoms. A hole is trapped in the Si-Si double bond, breaking the bond. The silicon atom without an unpaired electron is relaxed back into the plane of the oxygen atoms and the silicon atom with the unpaired electron is stretched further out of that plane, figure 2.6(C). This is a reversible situation in that an electron can re-establish the Si-Si double bond. The activation energy for the hole is ~3ev. The Si-SiO₂ interface is characterized by many oxygen vacancies (even in the best oxides) and strained Si-Si bonds or E' centers. This explains the high density of hole traps near the interface and why 'poor' oxides have a greater density of bulk hole traps. Any growth process that leaves oxygen vacancies will introduce hole traps. Oxide growth is discussed in section 2.8.

2.6 INTERFACE STATES

Electron spin resonance measurements of Si (100) surfaces have identified two defect centers associated with interface states⁽³³⁻³⁵⁾, P_{b0} and P_{b1}. The P_{b0} is a surface Si atom bonded to three Si atoms directed into the substrate and a dangling bond pointing into the SiO₂. The nature of the P_{b1} center has yet to be determined. The P_{b0} center can trap electrons at the interface resulting in a positive threshold

FIGURE 2.6: A) normal SiO_2 (a); oxygen vacancy in SiO_2 (b); a hole trapped at the oxygen vacancy (c).
 B) a hole captured in a oxygen vacancy.
 reproduced from reference (1)

voltage shift. There will always be some P_{b0} centers due to lattice mismatch. The best oxides have an interface state density of $<10^{10}$ which is sufficiently small not to cause any transconductance loss in MOSFET's with thin gate oxides, but the effect increases linearly with oxide thickness.

Interface states trap charge at the interface and are amphoteric in nature. As discussed earlier, charge trapped at the interface shifts the threshold voltage. Unlike oxide trapped charge, the density and even the polarity of the charge in interface states depends on their position relative to the fermi level. Hence, a shift in the applied gate voltage causes a change in the occupation of the interface states. Most interface states are known as fast in that they exchange charge with the substrate rapidly. Some states appear to change their occupancy very slowly (several seconds) but otherwise behave just as fast states⁽³⁶⁾. Interface states are important in RADFET's for three reasons: 1) they decrease or increase the sensitivity depending on their charge state. 2) traps which are filled slowly cause a long term drift in the threshold voltage increasing the uncertainty in the measurement. 3) fast interface states degrade the electron mobility of the MOSFET.

There are three models for radiation induced interface traps⁽¹⁾. The first is known as the hydrogen model. Hydrogen introduced to the oxide during processing attaches itself to a dangling Si bond at the interface. Direct radiation⁽³⁷⁾ or

holes^(38,39) can break this H-Si bond re-establishing the interface state. Other hydrogen models involve bulk H atoms or ions diffusing to the interface and reacting with the H-Si to produce an interface state^(15,41).

The second model proposes that holes at or near the interface recombine with electrons tunnelling from the substrate^(1,39,40). The resulting release of energy can break an interfacial Si-O bond creating a dangling Si bond.

The third model⁽⁴²⁾ suggests that e-h pairs created in the SiO₂ near the interface break a Si-O bond. The resulting oxygen defect moves under the influence of an interfacial strain gradient and upon reaching the interface creates a dangling Si bond.

The RADFET's in this work were processed to minimize the number of radiation induced interface states as discussed in section 2.8.

2.8 OXIDE QUALITY

The change in the threshold voltage resulting from irradiation should vary as the oxide thickness squared assuming the number of e-h pairs created depends linearly on the oxide volume and the distribution of this charge is independent of the thickness. However, experiments⁽⁴⁴⁻⁴⁸⁾ have shown a range of thickness dependencies from linear to cubic.

The second assumption above does not seem to hold for oxides grown by some processes. The exact details of the

growth process determines the density of bulk and interface region hole traps. The sensitivity of a RADFET is highest if the electrons and holes produced are trapped near the interfaces. Charge trapped in the bulk of the oxide can reduce the sensitivity through equation 2.5 and an increased probability of recombination. A low density of near interface traps can cause a loss of charge to the substrate. A third mechanism by which the thickness squared dependence can be altered is through the charging of radiation induced interface states. The density of interface states strongly depends on the oxide growth parameters.

Every parameter involved in the growth of an oxide affects the bulk and interface quality. The effect of each parameter is considered below.

1) The growth temperature is probably the most important. At low temperatures the diffusion of the oxygen and silicon in the oxide is low, allowing for the possibility of freezing in oxygen vacancies. The strain at the SiO_2 -Si interface is also increased in a low temperature growth which introduces interface states.

2) Thick oxides are more quickly grown in the presence of H_2O , but these oxides tend to be less dense and must be annealed to reduce the bulk trap density.

3) Most oxides are annealed in an inert ambient, typically Ar, N_2 or $\text{N}_2 + \text{H}_2$. A high temperature anneal in N_2 increases the sensitivity of MOSFET's to radiation. This is

probably due to an increase in the near interface traps^(44,45,49), although there is some evidence for an increase in the density of bulk oxide hole traps. A postoxidation anneal in Ar or H₂ + N₂ appears to have a reduced effect on the trap density^(1,30,45,49). The reasons for this are not clear at the present time.

The introduction of hydrogen in the growth process pacifies the interface states, but concomitantly increase the number of radiation induced interface states as outlined in section 2.6.

4) Impurities inadvertently or deliberately introduced into the oxide can act as either electron or hole traps. Depending on their distribution, this can be used to increase or decrease the RADFET sensitivity. A uniform distribution will increase the bulk trapping and recombination. However, if loss of charge to the substrate is important the bulk traps can increase the sensitivity.

Damage to the oxide caused by ion implantation has been shown to create both electron and hole traps^(3,23,50,51). An arsenic implant at 140 kev followed by a 450°C anneal leaves only the hole traps behind^(3,23).

5) Chemical vapour deposited oxides are more disordered, even after annealing, than thermal oxides. A large increase in the hole trap density has been observed in these oxides⁽¹²⁾. Over-glasses such as phosphosilicate glass (PSG) and boro-phosphosilicate glass (BPSG) have been shown to strongly

reduce radiation sensitivity due to an increase in bulk trapping and recombination⁽¹²⁾.

6) The thickness of the oxide also seems to play a role interface quality^(44,45,52,53). Thick oxides appear to have a higher density of interface traps. This was speculated to be due to an increasing strain at the interface. Very thin oxides have strongly reduced hole trapping efficiencies due to tunnelling to the substrate^(54,55).

In summary, the large number of parameters involved in oxide growth and the density of oxide traps has lead to some considerable confusion. When correlating oxide growth parameters to the density of electron and hole traps one must take all the parameters into account. Some authors do not always publish all the details of their process. Wet or dry oxides, carefully annealed exhibit similar charge trapping characteristics although there is variation in the results from different laboratories⁽¹⁾. Doped and deposited oxides have increased bulk trapping rates and recombination probabilities.

CHAPTER 3

DESIGN OF FLOATING GATE RADFET's

3.1 FLOATING GATE RADFET

Figure 3.1(A) depicts a cross sectional view of the novel RADFET studied in this work. Essentially it is a floating gate MOSFET with a large wing-like extension over the field oxide. Charge is collected on the floating gate through the electric fields set up by applying a voltage between the control gate and the substrate. The area of the wing is ~100 times that of the active region of the MOSFET. The number of e-h pairs produced is linearly dependent on the oxide thicknesses. The gate oxide (under the floating gate) is only 50nm thick and therefore produces very few e-h pairs compared to all other oxides. Since the vast majority of the e-h pairs are produced in the capacitive extensions and above the floating gate in the MOSFET region, the number of radiation induced interface traps should be greatly reduced from that of a conventional design (see section 2.6).

3.2 SUBTHRESHOLD SLOPE

The threshold voltage is often defined⁽⁴³⁾ as the gate-source voltage necessary to establish an inversion layer at the silicon surface. Alternatively, it is as the gate-source voltage required to obtain a surface potential of $2\phi_s$,

Figure 3.1: A) RADFET with wing extension
 B) top view: showing two RADFET's sharing the same source.

where $2\phi_s = kT/q \ln(N_A/n_i)$. Unfortunately, there is no easy method to directly measure the surface potential in a MOSFET. Often, V_T is determined by plotting the logarithm of the channel current versus the gate voltage at fixed source-drain voltage. At the threshold voltage the logarithm of the current begins to rise less steeply. The capacitance versus voltage curve can also be used to determine V_T . As there is no discontinuity at the threshold voltage one cannot measure V_T precisely. The shift in V_T can be measured more accurately than V_T . Hence, only the shift in V_T was measured in this work. Holes trapped in the oxide cause a voltage shift in the drain current versus gate voltage curve for a fixed drain source voltage. It was this change in voltage which was measured. Clearly, the voltage shift can be determined more accurately if the drain current is strongly dependent on the gate-source voltage. For this reason the currents were chosen to be in the subthreshold region where the drain current is exponentially dependent on the gate voltage but only weakly dependent on the drain source voltage. The drain current in the subthreshold region is given by⁽⁴³⁾:

$$I_D = \mu_n (W/L) a C_{ox} / 2 (n_i / \beta N_A)^2 \exp(\beta \phi_s) (\beta \phi_s)^{-1/2} [1 - \exp(-\beta V_D)] \quad (3.1)$$

where $a = \sqrt{2(\epsilon_s/L_D)/C_{ox}}$ and ϕ_s is the surface potential:

$$\phi_s = V_G - a^2/2(1/\beta) \{ [1 + 4/a^2(\beta V_G - 1)]^{-1/2} - 1 \} \quad (3.2)$$

A small current is chosen to minimize interface state charging, charge injection into the gate oxide and to reduce the power and voltages required to operate the RADFET. The subthreshold slope is defined as the gate voltage needed to produce one decade change in the drain current. In a conventional RADFET⁽⁴³⁾:

$$S = kT/q \ln(10) [1 - C_p(\phi_s)/C_{ox}] \left\{ 1 - (2/a^2) [C_p(\phi_s)/C_{ox}]^2 \right\}^{-1} \quad (3.3)$$

where $C_p(\phi_s)$ is the substrate capacitance. Smaller subthreshold slopes should allow for more accurate measurements of ΔV_T . The subthreshold slope increases with gate oxide thickness. A 50nm gate oxide has a slope of 87 mV/dec, but the slope increases to 310 mV/dec for a 500 nm gate oxide. The RADFET's described in the previous section reduce the subthreshold slope while maintaining the thick gate oxide necessary to give high sensitivity.

The largest capacitance in the floating gate RADFET is between the control and floating gate. This couples the floating and control gate potentials, thereby reducing the subthreshold slope. Without the capacitive wings the subthreshold slope would simply be that of a thick oxide MOSFET with the same gate oxide thickness.

3.2 CALCULATION OF ΔV_T vs. DOSE

A calculation of the change in threshold voltage

with respect to radiation dose is performed in this section. Referring to figure 3.1: $t_1 = t'_1$, by construction, Q_2 is the charge per unit area on the floating gate on the wing side, Q_1 is the charge per unit area on the MOSFET side, E is the electric field and V is the voltage applied to the control gate. Assuming the substrate is at zero potential and since the gates are equi-potential surfaces:

$$E_1 t_1 = E'_1 t'_1 \quad (3.4)$$

$$\Rightarrow E_1 = E'_1 \quad (3.5)$$

$$\text{and} \quad E_3 t_3 = E_2 t_2 \quad (3.6)$$

$$\Rightarrow E_3 = E_2 t_2 / t_3 \quad (3.7)$$

Summing the potential drops between the substrate and control gate leads to:

$$E_2 t_2 + E_1 t_1 = V - V_{fb} = V' \quad (3.8)$$

$$E_3 t_3 + E_1 t_1 = V - V_{fb} = V' \quad (3.9)$$

Applying Gauss' law :

$$Q_1 / \epsilon_{ox} = E_2 - E_1 = E_2 (1 + t_2 / t_1) - V' / t_1 \quad (3.10)$$

$$Q_2 / \epsilon_{ox} = E_3 - E_1 = E_2 (t_2 / t_3 + t_2 / t_1) - V' / t_1 \quad (3.11)$$

$$\frac{Q_1 / \epsilon_{ox} + V' / t_1}{Q_2 / \epsilon_{ox} + V' / t_1} = \frac{t_3 (t_1 + t_2)}{t_2 (t_1 + t_3)} = K \quad (3.12)$$

Note that K depends only on the relative oxide thicknesses.

$$Q_1 / \epsilon_{ox} = K Q_2 / \epsilon_{ox} + V' / t_1 (K-1) \quad (3.13)$$

$$Q = Q_1 A_1 + Q_2 A_2 \quad (3.14)$$

Q is the total charge on the floating gate. Substituting eq. 3.14 into eq. 3.13:

$$Q_1 = \frac{1}{1 + K A_1/A_2} [KQ/A_2 + V' \epsilon_{ox}/t_1 (K - 1)] \quad (3.15)$$

Substituting eq. 3.13 into eq. 3.8:

$$E_2 = t_1/(t_1+t_2) \left(\frac{1}{1+KA_1/A_2} [KQ/(\epsilon_{ox}A_2) + V'/t_1 (K-1)] + V'/t_1 \right) \quad (3.16)$$

The potential of the floating gate in terms of Q and the potential of the control gate is:

$$V_{FG} = E_2 t_2 \quad (3.17)$$

$$= \frac{t_1 t_3}{(t_1+t_3) (\epsilon_{ox} A_2 (1+KA_1/A_2))} Q + \frac{t_3 (1+A_1/A_2)}{(t_1+t_3) (1+KA_1/A_2)} V' \quad (3.18)$$

Equation 3.16 indicates how closely the floating gate will follow the control gate voltage. Assuming $A_2 \gg A_1$:

$$V_{FG} = t_3/(t_1+t_3) V' \quad (3.19)$$

The more closely the floating gate follows the control gate the smaller the subthreshold slope of the MOSFET. The values of $t_3/(t_1 + t_3)$ for the winged structures are 0.68 and 0.88 whereas for the wingless structures the equivalent values are 0.10 and 0.28 indicating a substantial improvement in the subthreshold slope.

The measured shift of the threshold voltage upon irradiation is the change in the control gate voltage required to maintain the floating gate at the same potential. From equation 15:

$$\Delta V_T = \frac{dV_T}{dQ} \frac{\Delta Q}{V_{FG}} = - \frac{t_1 \Delta Q}{\epsilon_{ox} (A_1 + A_2)} \quad (3.20)$$

For $A_2 \gg A_1$:

$$\Delta V_T = - \frac{t_1 \Delta Q}{\epsilon_{ox} A_2} \quad (3.21)$$

This result is identical to that for a conventional RADFET described in section 2.3, but the subthreshold slope is greatly improved in the present design.

3.4 SENSITIVITY

The sensitivity of RADFET's depends on geometry, relative oxide thickness and the number of free charges created by the radiation. The expected sensitivities of all the RADFET's studied are calculated in this section. Charged particle equilibrium is assumed throughout.

Simple RADFET

Referring to figure 3.2(A), the energy is deposited in the SiO_2 layer and the resulting e-h pairs are separated with an efficiency, $f(E)$, see figure 2.4. Assuming all the holes are swept to the interface, the number of free charges/area:

$$Q = D/W_0 \rho t_{ox} f(E) \quad (3.22)$$

where D is the deposited energy per unit mass, W_0 is the e-h creation energy, ρ is the density of SiO_2 , and t_{ox} is the gate oxide thickness. The change in the threshold voltage due to

FIGURE 3.2: A) simple RADFET
 B) EPROM-like RADFET
 C) EPROM-like RADFET with wing extension

the charge Q is:

$$\Delta V_T = - Q t_{ox} / \epsilon_{ox} \quad (3.23)$$

$$= - 3.98 \times 10^6 D t_{ox}^2 f(E) \quad (3.24)$$

W_0 has been found⁽⁵⁶⁾ to be 17 ± 1 ev. ΔV_T depends on the square of the oxide thickness, since the energy absorbed depends linearly on the thickness as does its effect on the threshold voltage. A 0.5 μm gate oxide RADFET has a maximum sensitivity of 10.0mV/rad.

eprom-like RADFET

The sensitivity of this structure, figure 3.2(B), is slightly higher than for the simple RADFET. Under positive bias, the holes in the interpoly oxide move to the floating gate and the electrons are removed at the control gate. In the thin gate oxide the holes are trapped near the substrate interface while the electrons move to the floating gate. Taking into account these various charges leads to a sensitivity of:

$$\Delta V_T = -3.98 \times 10^6 f(E) (t^2 - t_1 t + t_1 (t_1 + t)) \quad (3.25)$$

$$= -3.98 \times 10^6 f(E) D (t^2 + t_1^2) \quad (3.26)$$

eprom-like with capacitive wing

Assume that the area of the wing, figure 3.2(C), is very much greater than the area of the MOSFET active region. It is therefore a good approximation to ignore the charge collected in the MOSFET region. Under positive bias, the floating gate collects holes from the interpoly oxide and electrons from the field oxide. The holes swept to the Si-SiO₂ interface in the field oxide have very little effect on the threshold voltage. The sensitivity is given by:

$$\Delta V_T = 3.98 \times 10^6 D (f(E)_2 t_2 t - f(E)_1 t^2) \quad (3.27)$$

where different separation efficiencies have been assumed for the interpoly and field oxides. The sign of the threshold voltage shift depends on the relative efficiencies and oxide thicknesses. RADFET's with two different oxide thicknesses were tested in this work, $t=140$ nm and $t=505$ nm (see figure 3.2).

CHAPTER 4

EXPERIMENT

4.1 DEVICE FABRICATION

The RADFET's were fabricated utilizing a previously developed 5 μm nmos process at Carleton University. The details of the process are in appendix A. The most important element in the process was the choice of oxide growth parameters.

Three different oxides were used in the fabrication of the RADFET's studied here. The field oxide was wet grown and the gate oxide was dry grown. Both of these oxides were grown and annealed in N_2 at 1100°C . A combination of CVD and thermally grown oxide formed the interpoly oxide. First, 140 nm of thermal oxide was grown at 1000°C on the as-deposited phosphorous doped silicon floating gate. No information was found on the trapping characteristics of dry thermal oxide grown on polysilicon silicon, although it is known to have a high breakdown voltage⁽⁵⁷⁾. This thermal oxide was followed by 350 nm of CVD oxide in the thick interpoly oxide RADFET's. The choice of a deposited oxide was forced by the need to minimize the thermal budget on the floating gate and the source and drain diffusions. The 1.5 hour oxidation at 1100°C required to grow 350nm of oxide could cause considerable diffusion of the phosphorous in the source and drain regions. It could also

have caused some diffusion of phosphorous from the floating gate into the field and gate oxides, possibly introducing unwanted electron and hole traps.

Oxides grown on polysilicon are known to have lower breakdown voltages and higher leakage currents than oxides grown on single crystal silicon^(58,59). Improvements in the oxides have been found using what is known as a "lo-hi" procedure to grow the polysilicon. One initially deposits the silicon at a low temperature (550°C) such that the film is amorphous. Then, the deposition is continued at a higher temperature (625°C) to obtain a polysilicon film. The result is a smoother surface with larger grain size⁽⁵⁷⁾. The floating gates were deposited in this manner.

The wire bonding procedure caused many of the floating gates to charge. These samples were discarded. No attempt was made to discharge them. Samples whose preradiation threshold voltages were close to the theoretical values were then coated in up to 8 mm of paraffin wax. Four attempts were made to cover the RADFET's with an epoxy, but always resulted in the charging of the floating gates.

4.2 Co⁶⁰ GAMMA RADIATION SOURCE

The RADFET's were subjected to gamma radiation from a Co⁶⁰ source at the National Research Council of Canada (NRC). The source strength was 6435 Curies on March 1, 1990 producing

a photon flux at 1.00 meters of 1.75×10^9 photons/cm²/sec at the time of these experiments.

The gamma spectrum of Co⁶⁰ consists of two narrow lines at 1.17 Mev and 1.32 Mev, but Compton scattering from the source and the collimator walls produces the broad spectrum shown in figure 4.1⁽⁶⁰⁾. Approximately 30% of photon energy lies in the low energy tail. Low energy photons have a high cross section and hence are more efficient in producing e-h pairs. Detailed calculations of the dose from the photon spectrum are difficult, so, the dose in SiO₂ was calculated by scaling the equivalent dose measured in water, as described in section 2.3. The build up curve of paraffin, figure 2.1C, was simulated utilizing the full photon spectrum⁽⁶⁰⁾.

4.3 ΔV_T MEASUREMENT CIRCUIT

The shift in the threshold voltage after irradiation was determined with the circuit shown in figure 4.2. Only one half of the circuit is shown. Two MOSFET's were irradiated at the same time, one under a positive gate bias and the other with a negative gate bias voltage. The two sensors shared the same source, figure 3.1B. The difference in V_T between the two MOSFET's was measured with a digital voltmeter. The practice of using two sensors has several advantages. Since the gates were biased with opposite polarities, the threshold shifts were in opposite directions. Therefore one obtains a doubling of the sensitivity. Differential measurements eliminate the

FIGURE 4.1: Photon spectrum of Co^{60} source.
Reproduced from reference (60).

FIGURE 4.2: Circuit used to measure V_T shift for radfet. Actual circuit employed two sensors, biased oppositely and sharing the same source. There was one of the above circuits for each sensor.

threshold shifts due to parameters other than the irradiation, such as, temperature and charge injection from the substrate. Given an ability to measure V_t precisely, the differential method is insensitive to drifts in the drain current.

The essential features of the ΔV_t measurement circuit are shown in figure 4.3. Measurements were taken by placing $-0.1V$ on each source. The drain currents (0.01 or $0.02 \mu A/\mu m$) were fixed by the value of the resistor R_d and the current source output voltage, figure 4.2. The output of the op-amp, figure 4.3, will rise until the gate voltage is sufficient to allow this drain current. The difference between the gate voltages for the two sensors was measured with a Keithley 196 digital voltmeter. On switching from the measurement condition to the irradiation or bias condition (figure 4.2) the sources and drains are grounded and the output op-amp was setup as a voltage follower (output shorted to the negative input). This improved the stability of the op-amp on switching back to the measurement condition. The bias voltages during the irradiation period were taken directly from DC power supplies.

The circuit was implemented on a PC board with the sensor separated by $\sim 5cm$ from the remainder of the circuit.

A shutter with a preset timer controlled the exposure time. A typical total dose was $500-1000$ rad delivered in $50-100$ rad bursts.

FIGURE 4.3: Basic features of the circuit used to measure the threshold voltage shift. Only half of the circuit is shown.

CHAPTER 5

RESULTS AND DISCUSSION

5.1 RESULTS

Irradiations were performed on the four RADFET designs listed below and depicted in figure 5.1.

- 1)thn: eprom-like with a thin interpoly oxide, figure 5.1A
- 2)thk: eprom-like with a thick interpoly oxide, figure 5.1B
- 3)thn-w: eprom-like with a wing over the field oxide and a thin interpoly oxide, figure 5.1C.
- 4)thk-w: eprom-like with a wing over the field oxide and a thick interpoly oxide, figure 5.1D.

The results for all the samples successfully tested are in tables 5.1 thru 5.4 where the values of the sensitivities represent an average of up to ten data points. Note that the sensitivities are for a pair of RADFET's sharing the same source. The sign of the sensitivities refer to the direction of the threshold shifts. It appears that the RADFET's without wing extensions trapped a net negative charge at the control gate while those with extensions trapped a net positive charge. Table 5.5 shows a comparison of the experimental sensitivities to the predictions made in chapter 3. The theoretical values are the maximum sensitivities assuming 100% charge collection. Some samples were given a total dose of

FIGURE 5.1: A) RADFET with thin interpoly oxide
 B) RADFET with thick interpoly oxide
 C) RADFET with thin interpoly oxide and a wing extension
 D) RADFET with thick interpoly oxide and wing extension

FIGURE 5.2: Threshold voltage shift vs. dose for thick interpoly oxide with wing extension.

Table 5.1

Data for thick interpoly oxide with wing

<u>SAMPLE</u>	<u>BIAS VOLTAGE (volts)</u>	<u>SENSITIVITY mV/rad</u>
thk-w1	2.5	1.7
	5.0	2.2
thk-w2	2.5	2.0
	5.0	2.6
thk-w3	12.5	4.4
thk-w4	12.5	4.6
thk-w5	12.5	3.8
thk-w6	12.5	4.7
thk-w7	12.5	4.6
	20.0	6.0
	30.0	7.6
	40.0	discharged

TABLE 5.2

Data for thin interpoly oxide with wing

<u>SAMPLE</u>	<u>BIAS VOLTAGE (volts)</u>	<u>SENSITIVITY (mV/rad)</u>
thn-w1	2.5	0.7
	5.0	1.0
thn-w2	2.0	0.8
	4.0	1.4
	6.1	1.8
	8.1	2.0
	10.1	2.2
	12.2	2.4
	15.5	2.8
thn-w3	1.5	0.6
	2.5	0.9
	5.0	1.3
	7.5	1.8
	10.0	2.0
	12.5	2.2
	15.0	2.6
thn-w4	12.5	2.2

TABLE 5.3

Data for thick interpoly oxide

<u>SAMPLE</u>	<u>BIAS VOLTAGE (volts)</u>	<u>SENSITIVITY (mV/rad)</u>
thk-1	2.5	-1.8
	5.0	-3.0
thk-2	10.0	-4.4
thk-3	1.5	-1.8
	2.5	-2.2
	5.0	-3.4
	3.75	-2.8
	10.0	-4.9
	15.0	-5.7
thk-4	12.5	-5.5
thk-5	12.5	-5.0
thk-6	12.5	-5.0
thk-7	10.0	-4.4
	20.0	-6.6
	25.0	-7.1
	30.0	-7.5
	35.0	-6.3
	40.0	discharged

TABLE 5.4

Data for thin interpoly oxide

<u>SAMPLE</u>	<u>BIAS VOLTAGE (volts)</u>	<u>SENSITIVITY (mV/rad)</u>
thn-1	2.5	0
	5.0	0
thn-2	2.5	0
	5.0	0
thn-3	12.5	-0.3

TABLE 5.5

Maximum Sensitivies (mV/rad) (experiment vs. theory)

<u>sample</u>	<u>experiment</u>	<u>theory</u>
thk	7.5	20.0
thn	0.2	1.8
thk-w	11.5	22.3
thn-w	5.5	10.0

>3000 rad. The high doses were necessary to reduce the uncertainty in the value of V_T to a few percent. The threshold voltage was found to vary linearly with dose to within 10% for all samples. Figure 5.2 depicts this behaviour for typical sample, thk-w-3.

From the outset it was apparent that interface charging would not allow for low dose experiments. A voltage applied to the gates causes the interface states to move in energy relative to the fermi level and therefore change their charge state. Any change in the bias voltage results in a change in the charge stored in the interface states. On switching from a large positive bias voltage during the irradiations to a bias voltage of V_T , when the threshold voltage was measured, the apparent threshold voltage drifted by as much as 0.75 V in ~3 minutes. During these three minutes the interface states were discharging. The drift in V_T never completely stopped, it only slowed down to a few millivolt/minute at which time the data was accepted. An interface state density of 10^{10} cm^{-2} , uniformly distributed in energy across the forbidden gap is capable of creating a 0.23 V shift in V_T across a $0.5 \mu\text{m}$ gate oxide. A charge density of $3 \times 10^{10} q \text{ cm}^{-2}$, which is a plausible value for the NMOS process at Carleton University, could explain the measured shifts. No further attempt was made to characterize the interface states. *It should be noted that the direction of the drift was opposite to what would be expected for sodium ion contamination.*

In all cases, there was on average, no difference in the magnitude of the threshold shift for the positively and negatively biased MOSFET's, although the directions were opposite to reflect the sign of the charge stored on the floating gates. The measured value of the threshold voltage shift was actually twice the value for each individual MOSFET in the circuit of figure 3.2. The theoretical values for ΔV_T (in section 2.11) were multiplied by 2 to reflect this.

The sensitivity was a strong function of the applied electric field during irradiation as shown in figure 4.3 for the four designs. The largest voltages which could be applied to the wingless RADFET's were 35-40 V and 12-15 V for the thick and thin interpoly oxides respectively. This translates into ~ 0.7 MV/cm for the electric fields in the oxides. The floating gate voltage followed the control gate much more closely in the winged structures causing the largest electric fields to occur in the thin gate oxide. This gate oxide broke down at ~ 40 V and ~ 20 V bias, corresponding to ~ 3 MV/cm while the fields in the interpoly oxides were only ~ 0.2 MV/cm. Hence, breakdown occurred in the interpoly oxide at ~ 0.7 MV/cm and in the gate oxide at ~ 3 MV/cm. The breakdown of a sample was always irreversible in that the floating gate would no longer store charge upon further irradiation.

The curves in figure 5.3 agree only qualitatively with those from other groups, figure 2.4. The yield does not appear to rise as quickly at low applied fields and the maximum

FIGURE 5.3: Sensitivity vs. applied electric field for all RADFET's tested. Squares) thn-w; circles) thk; triangle) thk-w; diamond) thn.

values do not approach the theoretical predictions at the highest electric fields. This is especially true for the thn samples where the sensitivity was so low that it was difficult to obtain data.

The thk-w RADFET's were considerably more sensitive than the thk RADFET's whereas the theory predicted that they should be within 10% at the same electric fields. The dashed lines in figure 5.3 represent extrapolations assuming the shape of the curves are the same as the thk curve.

A third concern is that the ratio of the sensitivities of the thn-w and thk-w is as predicted, but the thn and thk sensitivities are far from scaling according to the prediction. The sensitivities of the thn RADFET's are far too low.

An interpoly oxide which was not effective in producing charge on the floating gate can explain most of the concerns above. The thin interpoly oxide consisted of 140nm of dry thermal oxide on heavily phosphorous doped silicon. No previous work on the electron and hole trapping in these oxides could be found in the literature. The thick interpoly oxides had 350nm of CVD deposited oxide on top of the 140nm thermal oxide. CVD oxide is known to have large densities of bulk electron and hole traps.

Consider the wingless RADFET's in figure 5.1(A) and 5.1(B). Electrons and holes trapped in the bulk interpoly oxide could not reach either the control or floating gate,

causing a reduction in their effect on the threshold voltage. Clearly, if both electrons and holes are trapped their effects will cancel. This condition would be indistinguishable from recombination. The most complete data were for the thk RADFET's. These were used to scale all the other data. The procedure was to assume the field effect coefficient was 0.7 at an electric field of 0.54MV/cm, from figure 2.4. The last data point in the thk curve of figure 5.3 was scaled accordingly. The remaining discrepancy between the experiment and the prediction was attributed to electron and hole trapping in the interpoly oxide. The result was that the interpoly oxide was only 53% efficient. This efficiency was then assumed for all interpoly oxides. All other oxides were taken to be ideal. New predictions were calculated based on the electric field effect and the interpoly oxide efficiency. These are presented in table 5.6 along with the old ideal predictions and the experimental data.

TABLE 5.6

sample	experiment	new prediction	ideal prediction
thk	7.5	7.5	20.0
thn	0.2	0.7	1.8
thk-w	11.5	22.2	22.3
thn-w	5.5	7.7	10.0

The new theoretical value indicate that given the assumption

of a poor interpoly oxide one can explain why the thk-w RADFET was significantly more sensitive than the thk RADFET. The experimental and predicted values of the sensitivity for the thn RADFET are brought closer. One could now make assumptions about the other oxides. This seems pointless as the main goal here is to compare the RADFET's with capacitive extensions to those with no extensions.

Although the thick oxide RADFET's with wing extensions are more sensitive than other thick gate RADFET's⁽⁶¹⁾, at the same electric fields, the requirement of ~100 V bias makes their practicality questionable. The principle advantage of the winged RADFET's lies in their decreased subthreshold slope. Measuring low doses (<100 mrad) will require the detection of V_T shifts on the order of 10 μ V. With the present scheme of detecting the V_T shifts, a gate voltage which is more sensitive to the bias current will facilitate this measurement. Table 5.7 shows a comparison of the subthreshold slopes for the RADFET's presented here. Note that the results for a conventional thick gate oxide RADFET should correspond to those for the wingless RADFET's at the same oxide thickness. The discrepancy between the measured and calculated values may lie in the effect of interface states. In the presence of interface states the subthreshold slope is⁽⁴³⁾:

$$S = S_0 \frac{1 + (C_d + C_{it})/C_{ox}}{1 + C_d/C_{ox}} \quad (5.1)$$

where $C_{it} = qD_{it}$ and D_{it} is the areal density of interface

SUBTHRESHOLD SLOPE

TABLE 5.7

<u>RADFET</u>	<u>SUBTHRESHOLD SLOPE (mV)/dec</u>	<u>MEASURED (mV)/dec</u>
thn-w	99	127
thk-w	127	200
thn	240	546
thk	310	1575

The charging of the interface states adds a capacitance in parallel to the substrate capacitance. The value of D_{it} required to bring the measured values of 'S' in agreement with eq. 5.1 is $5-9 \times 10^{10}$. This is a larger value of the interface state density than was suggested earlier and is quite high for the Carleton process, but is not inconceivable. Since C_{ox} between the control and floating gates is much larger in the winged structures than in the wingless RADFET's the effect of C_{it} is greatly reduced in the winged RADFET's.

These dosimeters were intended for use in low dose environments. Hence, their ability to retain charge while not in use (zero bias) is important. After approximately 3 months only one of the irradiated RADFET's lost in excess of 10% of its charge. One sensor completely discharged. In an ideal case, free charge induced by irradiation is trapped on the floating gate or at the floating gate-oxide interface. Charge loss can only occur via diffusion or drift across a SiO_2 layer to the substrate or the control gate.

CHAPTER 6

CONCLUSIONS

A novel design for a MOS based gamma radiation sensor has been analyzed, fabricated and tested. The new RADFET is essentially a floating gate MOSFET in which large wing-like extensions over the field oxide have been attached to both the floating and control gates. The large capacitance between the floating gate and the control gate reduced the subthreshold slope substantially from the value obtained in a simple thick gate oxide RADFET. A small subthreshold slope should allow for a more precise determination of the dose. The data suggested that a high density of fast interface states were created during the processing. Charging of the interface states on changes in the gate bias voltage caused drifts in the threshold voltage several times as large as the shift in V_t due to the irradiation. After a period of a few minutes (the time varied for each RADFET) the drift in V_t would substantially slow but never completely stop. This precluded measurements at low doses.

The majority of the radiation induced free charge (electrons or holes) is stored on the floating gate and not the SiO_2 -substrate interface. This reduces the sensitivity of the device to the creation of radiation induced interface states. This would also be true for a floating gate RADFET

without the wing extensions. The large capacitance between the floating and control gates also reduces the effect of any pre-irradiation interface states.

Electrons are not easily trapped at the SiO_2 -substrate interface, therefore conventional RADFET's are biased with a positive voltage during the irradiation. The floating gate sensor does not suffer from this limitation. Under negative bias electrons are trapped in the floating gate. The differential measurement using two floating gate RADFET's, one under positive bias and the other under negative bias, immediately offers an enhancement of the sensitivity by a factor of two. The sensitivity might be increased further by doping the interpoly oxide to reduce its ability to supply charge to the floating gate. Charge coming from the interpoly oxide is the opposite sign from that originating in the field oxide, therefore there would be less cancellation of the charge coming from the field oxide. In an ideal case, for the thk-w RADFET, this could further increase the sensitivity by a factor of two.

The major problem with the floating gate design with wing extensions is the large voltage it requires to operate. A 100 V bias needs to be applied to the control gate to obtain an electric field of 0.5 MV/cm in the field oxide. At this voltage the thin gate oxide will have an electric field of 13 MV/cm. A good oxide has a breakdown voltage of 13 MV/cm. The thin gate oxide produced for this work had a breakdown voltage

of only 3 MV/cm. The simplest solution to this problem is to increase the thickness of the thin gate oxide at the expense of increased sensitivity to radiation induced interface states. Another solution is to employ a different dielectric material for the thin gate oxide, but this complicates the process still further.

The final difficulty with the floating gate design is that it is considerably more complicated to fabricate than the simple RADFET.

Increasing the precision in the measurement of the threshold voltage shift will be important in low dose environments. The shift in V_T for a 10 mrad irradiation is only $\sim 20 \mu\text{V}$. The present sensor and circuitry are insufficiently stable to detect shift at the $10 \mu\text{V}$ level. For reasons not yet understood p-channel RADFET's are more stable than n-channel devices⁽⁶¹⁾. Efforts are presently underway to improve the circuitry for a p-channel device with the goal of reducing the uncertainty in the threshold voltage shift.

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APPENDIX A

FLOATING GATE RADFET PROCESS

A sketch of a cross section of the basic structure is in figure 1A. A brief outline of the process follows. The details can found in the process run sheet in this appendix.

The starting material was a clean 2" p-type ($2 \Omega\text{-cm}$) wafer. Silicon nitride was deposited and patterned to form the device wells and the $1\mu\text{m}$ field oxide grown by a wet thermal process. After stripping the nitride, a gate oxide was grown to a thickness of 54nm. A "lo-hi" process was used to deposit the floating gate. A phosphorous doped amorphous silicon film was deposited, on top of which a phosphorous doped polysilicon film was deposited. The resulting polysilicon layer has a smoother topography than a polysilicon film deposited directly. The floating gate was then patterned and n^+ diffusions performed for the source and drains regions of the MOSFET.

For all of the RADFETS a 140nm interpoly oxide was thermally grown in dry oxygen. The thick interpoly oxide RADFETS had an additional 350nm LPCVD oxide on top of the thermal oxide. The control gate was deposited directly as polysilicon at 625°C and was doped in-situ with phosphorous. The entire wafer was coated in BPSG.

FIGURE 1A: A cross section of the floating gate radfet.

NMOS PROCESS

STARTING MATERIAL: 1.8-2.6 Ω cm p (100)

1. PAD OXIDATION

a) RCA clean

b) Oxidation tube temperature 1100°C

5 min preheat	O ₂
2" every 6 sec push	O ₂
15 min oxidation	dry O ₂ + 2.5%HCL
5 min oxidation	dry O ₂
20 min anneal	N ₂
2" every 15 sec pull	N ₂
10 min cool	N ₂

target thickness: 80nm

2. NITRIDE DEPOSITION

LPCVD

tube temperature: 820°C

SiH₂Cl₂: 37.6% NH₃: 35.3% deposition time: 15 min

target thickness: 80nm

3. DEVICE WELL P.E.

a) apply, prebake, expose, develop, postbake POSITIVE PR

b) plasma etch nitride (Technics Planar Etch II)

power: 100W source gas: freon/5%O₂

pressure: 0.3Torr

estimated etch time: 1 min 50 sec

c) flood coat wafer fronts with POSITIVE PR; postbake

d) remove nitride from wafer backs (Technics Planar Etch II)

etch recipe as above

e) strip PR in Caro's acid

f) remove pad oxide

etch in buffered HF until pad oxide removed from
field regions
estimated etch time: 1 min 30 sec

4. FIELD OXIDATION

a) RCA clean

b) Oxidation   tube temperature 1100°C

5 min preheat	O ₂
2" every 6 sec push	O ₂
10 min oxidation dry	O ₂
180 min oxidation	O ₂ pyrogenic H ₂ O
30 min oxidation	O ₂ + 2% HCl
40 min anneal	N ₂
2" every 15 sec pull	N ₂
10 min cool	N ₂

target thickness: 1.0µm

5. NITRIDE AND PAD OXIDE REMOVAL

a) remove converted nitride

etch in 10% HF until oxide removed from top of
nitride
estimated etch time: 2 min

b) remove nitride (Technics Planar Etch II)

power: 100W   source gas: freon/5%O₂
pressure: 0.3Torr
estimated etch time: 1 min 50 sec

c) remove pad oxide

etch in buffered HF until oxide removed from device
wells
estimated etch time: 30 sec

6. GATE OXIDATION

a) RCA clean

b) Oxidation   tube temperature 1100°C

	5 min preheat	O ₂
2" every 6 sec	push	O ₂
	15 min oxidation	O ₂
	40 min anneal	N ₂
2" every 15 sec	pull	N ₂
	10 min cool	N ₂

target thickness: 50nm

7a. LO-HI POLYSILICON

a) in-situ doped amorphous

LPCVD

tube temperature: 550°C

SiH₄: 35.0%   SiH₄/PH₃: 26.9%

deposition time: 146 min

b) in-situ doped poly

LPCVD

tube temperature: 625°C

SiH₄: 35.0   PH₃: 26.9

deposition time: 192 min

target thickness: 0.5μm

8. GATE P.E.

a) apply, prebake, expose, develop, postbake POSITIVE PR

b) plasma etch poly (Technics Planar Etch II)

power: 100W   source gas: freon/5%O₂
pressure: 0.3Torr

estimated etch time: 4 min

c) strip PR in Caro's acid

9. SOURCE/DRAIN OXIDE ETCHBACK

etch in buffered HF @20°C until Si exposed in
source/drain windows

estimated etch time: 50 sec

10. SOURCE/DRAIN DIFFUSION

a) RCA clean

b) predeposition   source: POCl₃ @20°C
tube temperature: 1000°C

5 min preheat	N ₂ +O ₂
30 sec push	N ₂ +O ₂
5 min warm-up	N ₂ +O ₂
2 min dope	N ₂ +O ₂ +N ₂ /dopant
10 min hold	N ₂ +O ₂
15 sec pull	N ₂ +O ₂
5 min cool	N ₂ +O ₂

c) remove phosphosilicate glass: etch 10 sec in 10% HF

11. INTERPOLY OXIDATION

a) RCA clean

b) Oxidation   tube temperature 1100°C

5 min preheat	O ₂
2" every 6 sec push	O ₂
90 min oxidation	O ₂
20 min anneal	N ₂
2" every 15 sec pull	N ₂
10 min cool	N ₂

measured thickness: 140nm

REMOVE AND STORE 3 WAFERS

11B. OXIDE DEPOSITION

LOTOX UNDOPED   deposition time: 18.5 min.

measured thickness: 365nm

11C. OXIDATION + LOTOX DENSIFICATION

tube temperature 1100°C

	5 min preheat	O ₂
2" every 6 sec	push	O ₂
	90 min oxidation	O ₂
	20 min anneal	N ₂
2" every 15 sec	pull	N ₂
	10 min cool	N ₂

ALL WAFERS

12. POLYSILICON DEPOSITION

in-situ doped poly

LPCVD
 tube temperature: 625°C
 SiH₄:35.0 PH₃:26.9
 deposition time: 226 min

measured thickness: 0.5μm

13. GATE P.E.

a) apply, prebake, expose, develop, postbake POSITIVE PR

b) plasma etch poly (Technics Planar Etch II)

power: 100W source gas: freon/5%O₂
 pressure: 0.3Torr

estimated etch time: 4 min

c) strip PR in Caro's acid

14. BPSG DEPOSITION

LPCVD Recipe #3 temperature 406°C

SiH₄: 5.2% SiH₄/PH₃: 13.6% O₂: 27.5% TMB: 52.3%
 deposition time: 18.5 min

target thickness: 0.5μm

15. BPSG FLOW

a) flow tube temperature: 900°C (phosphorus

drive-in tube)

5 min preheat	N ₂
30 sec push to center	N ₂
20 min anneal	N ₂
30 sec pull	N ₂
10 min cool	N ₂

b) Caro's acid clean

16. CONTACT P.E.   mask CU-1   -03

a) apply, prebake, expose, develop, postbake NEGATIVE PR

b) etch in siloxide etch @ 20°C until bare Si exposed

(scribe channels will go hydrophobic)

c) strip PR in Caro's acid

17. CCNTACT CLEARING ETCH

etch in "BD" etchant until bare Si exposed
(scribe channels will become hydrophobic)

18. FRONT METALLIZATION

e-beam aluminum

target thickness: 1.0µm

19. METAL P.E.   mask CU-1   -04

a) apply, prebake, expose, develop, postbake POSITIVE PR

b) etch in phosphoric acid @60°C until Al removed

expected etch time: 5 min

c) rinse 30 min

20. BACK POLY/OXIDE REMOVAL

- a) rebake at 130°C for 30min
- b) flood coat fronts with POSITIVE PR; postbake
- c) etch in poly etch until polysilicon cleared from backs

estimate etch time: 45 sec

- d) place a drop of concentrated HF on wafers backs, and etch until field oxide removed

estimated etch time: 1 min

- e) strip PR in J-100

- i) ensure wafers are dry

- ii) J-100 @ 100°C for 10 min

- iii) rinse 30 min

21. METAL ANNEAL

tube temperature: 450°C

5 min preheat	N ₂
5 min tube purge	H ₂
20 sec push	H ₂
20 min anneal	H ₂
20 sec pull	H ₂
5 min cool	H ₂
10 min tube purge	N ₂

22. BACK METALLIZATION

e-beam evaporation

target thickness: 0.5μm

END

24.12.92

FIN