Passive Device Models for Monolithic Millimeter-Wave Integrated Circuits on Silicon

by

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in partial fulfillment of the requirements for the degree of

Master of Applied Science

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ABSTRACT

High frequency models for integrated monolithic passive devices on silicon substrates are developed and implemented in this thesis. Three common types of passive devices are investigated and modeled. The devices of interest are MIM capacitors, varactor diodes, and polysilicon resistors. All of which play important roles in the design of high frequency circuits.

The devices are modeled with equivalent circuit models since these are easily integrated into CAD environments for circuit design and simulation. The models are developed from physical principles and they use the geometrical attributes of the respective devices to compute the model parameter values.

The high frequency models were applied to devices fabricated in a high frequency silicon germanium bipolar process. The model predictions were generally inline with the measured results up to 40GHz, which was the frequency limit of the test equipment. Slight discrepancies were observed for certain devices and possible underlying causes are outlined for these respective cases.

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LIST OF SYMBOLS

Symbol	Description	Unit
ω	Angular frequency	rad/s
C	Capacitance	F
R	Resistance	Ω
L	Inductance	H
Y	Admittance	S
ε_0	permittivity in vacuum	F/cm
Tm	Thin oxide thickness in MIM capacitors	m
A	<i>Area</i>	m^2
P	Periphery	m
M	Mutual Inductance	H
Q	Mutual Inductane parameter	H
L_{self}	Self-Inductance	H
TP	MIM capacitor top plate	--
BP	MIM capacitor bottom plate	--
ρ	Conductor resistivity	$\Omega \cdot cm$
Q_{Y11}	Through path quality factor	--
$R_{L_{eff}}$	Effective input resistance	Ω
DAC	Anode to cathode Diode	--
DCS	Cathode to substrate Diode	--

V_{bi}	Build-in potential	V
m	Grading factor	--
ADS	Advanced Design System	--
GMD	Geometric mean distance	m
s	Finger separation distance (varactor diode)	m
C_{eff}	Effective capacitance	F
C_{j0}	Zero-bias anode to cathode junction capacitance	F
γ	Propagation constant	1/m
G	Conductance	S
β	Phase constant	1/m
α	Attenuation constant	1/m
Z_0	Characteristic Impedance	Ω
λ_g	Guided wavelength	m
σ	Conductivity	S/m
$ABDC$	Chain matrix	--
EM	Electromagnetic	--
C_{m21}	Top plate to bottom plate capacitance (MIM capacitor)	F
C_{ms}	Bottom plate to substrate capacitance (MIM capacitor)	F
C_s	Substrate capacitance	F
R_s	Substrate resistance	Ω
C_{mg}	Bottom plate to ground capacitance (MIM capacitor)	F

R_L	Load resistance	Ω
MOS	Metal-oxide-semiconductor	--
Csj0	Zero bias cathode to substrate capacitance (varactor diode)	--
L_s	Series inductance (varactor diode)	H
SiGe	Silicon Germanium	--
R_{well}	n-well resistance (varactor diode)	Ω
K	coefficient of mutual coupling	--

CHAPTER 1: Introduction

1.1 Introduction

Recently there has been a push to use silicon germanium (SiGe) bipolar transistors for physical layer circuits in OC-768 systems (40 Gb/s) and to some extent in high-speed wireless systems. This is mainly as a result of the cost effectiveness of silicon versus established high-speed processes such as GaAs or InP. The ability to combine SiGe bipolar with CMOS also proves advantageous since a much higher level of integration can be achieved in the sense that complete system solutions can be offered on a single die. Advances in SiGe bipolar transistors make the use of this technology for such high-speed applications plausible [1].

Optical systems running at 40Gb/s (return zero or non return zero) on silicon require that lumped passive devices such as integrated inductors, capacitors, varactor diodes, and resistors perform to very high frequencies. A voltage-controlled oscillator (VCO) is typically used in clock and data recovery circuits and is a good example of an integrated circuit that makes use of most passive devices. A VCO implementation often used in high frequency circuits is the differential Colpitts oscillator because of the comparatively high spectral purity of the sinusoid generated by the *LC* tank [2]. With advances in the performance of integrated inductors the tank circuit is now often integrated on-chip.

An *LC* differential Colpitts oscillator often makes use of the following integrated passive components: varactor diodes for frequency tuning, resistors for biasing and loads, MIM capacitors for impedance transformation and frequency selection, and finally inductors which are also part of the frequency selection network [3], [4].

The oscillation frequency of such a VCO is generally required to be between 20GHz and 40GHz for 40Gb/s systems (return to zero will most likely require 40GHz). The design of VCOs is very sensitive to the passive components and as such accurate CAD models for passives devices, in the frequency range of interest, must be available.

The motivation for this thesis work is two fold. First investigate the performance of passives at frequencies up to 40GHz through characterization of lumped capacitors, varactor diodes and resistors. Second develop equivalent circuit models, since they can easily be integrated into the existing CAD flow, for frequencies up to 40GHz. Verification of the high frequency models is accomplished by comparing a variety of measured results to the model predictions.

1.2 Thesis Format

The thesis begins with an overview of high frequency on-chip measurement principles. Specifically, error correction procedures pertaining to high frequency on-chip measurements are introduced/defined in chapter 2. This is followed by a discussion on three of the dominant modeling methodologies for integrated devices. Particular attention is paid to general application area, computation demand and accuracy.

In chapter 3, a high frequency equivalent circuit model for a MIM capacitor is developed from the physical geometry of the device. The physical principles behind the components in the model are outlined. The model is applied to fabricated devices and results are compared. Models of less complexity, derived from the high frequency model, are also presented. The resulting modeling accuracy when select high frequency components are removed is investigated by comparing the predictions of the low complexity models to measurements of devices.

In chapter 4, a high frequency equivalent circuit model for varactor diodes is developed from physical parameters. A detailed physical model invariant to the number of fingers in the device is first presented and the origin of the parasitic components is discussed. A reduction methodology is introduced (with particular emphasis on inductance) in order to devise a compact model. The compact model is eventually applied to actual devices and results are compared.

In chapter 5, a high frequency equivalent circuit model for polysilicon resistors is developed from physical parameters. Two distinct regions in the polysilicon resistor are

identified and modeled in consequence. The resistor is found to behave in a similar fashion to a lossy transmission line. General propagation theory is used to develop the model. The model is applied to fabricated devices and results are compared.

Finally, the thesis is summarized in chapter 6 and possibilities for future work are outlined.

CHAPTER 2: Characterization and Modeling of On-Chip Passives

In this chapter, general device characterization issues, such as system calibration and de-embedding, are introduced as they apply to on-wafer measurements. Various device-modeling methodologies are subsequently reviewed with emphasis on their respective application areas.

2.1 Characterization of Monolithic Integrated Passive Devices

Characterization can be summarized as the process of fully capturing a device's behavior through measurements. Characterization often serves the purpose of generating reference data for the development of models. Accurate characterization of devices is very important since the results are deemed representative of the actual physical devices.

On-wafer device characterization (active or passive) at very high frequencies is typically done with the use of scattering parameters (S -parameters). This is partially because direct Z , Y , H or $ABCD$ parameter characterization of an n -port network is a practical impossibility at microwave frequencies due to the lack of good quality short and open circuits needed for these methods. S -parameters are ratios of incident and reflected traveling waves and can be used to fully characterize a network up to very high frequencies. Current S -parameter characterization systems can perform measurements up to 120 GHz. All device measurements in this thesis were performed with the use of S -parameters.

In order to properly characterize a device it is essential that no errors be induced into the measurements by the measurement system itself or the on-wafer device interface i.e. test-fixture (for the purposes of this thesis the term "measurement system" encompasses all sub-systems involved in performing the measurement up to the microprobe tips). A diagram of a typical wafer probing setup is shown in figure 2.1 and a block diagram representation of the key components is shown in figure 2.2.

Figure 2.1: Typical high frequency measurement setup

Figure 2.2: Block diagram depiction of measurement system and on-wafer components.

In an ideal system, induced errors would not be a problem; the internal reference plane (the region in the measurement system where the incident and reflected traveling waves are sampled) could just as well be at the device interface (identified as the desired external reference plane in figure 2.2). However, under real measurement conditions the cables, probes and connectors (part of the external measurement system shown in figure 2.1) along with the on-wafer bond pads and interconnect (part of the on-wafer device interface) have a non-negligible effect on the traveling waves. Hence, the characteristics of the transport mediums are sensed at the internal reference plane. Under such

conditions the internal reference plane is not equivalent to the external reference plane. The measured reflected and transmitted waves will represent the behavior of the device in addition to all components within which the waves traveled. Without any correction mechanism the S -parameters will be representative of the part of the system that lies beyond the internal reference plane (i.e. cables, connectors, bias-tee, probes, bond pads, interconnect and device). Thus, it can be said that the external measurement system and on-wafer device interface introduce systematic error into the device measurement. Typically, systematic errors introduced by the external measurement system, and those introduced by the on-chip interface are dealt with separately [5]. Error correction procedures, whose purpose is the removal of such systematic errors, have been developed for both systems and will be discussed in turn.

2.1.1 Calibration

Calibration is an error correction procedure, which is most often used to eliminate errors caused by the external measurement system (i.e. errors introduced in the region between the internal reference plane and microprobe tips). Once corrections are applied, a reference plane is basically established at the microprobe tips, i.e. between the probe tips and bond pads, which is equivalent to the internal reference plane if the errors are totally eliminated.

In order to generate an error model, one that is representative of the impact that the external measurement system has on the measurement results, standards with known characteristics must be used to determine error coefficients. Error coefficients are parameters that relate the known reflection coefficient of a standard and the measured reflection coefficient of that particular standard. Calibration for a two-port measurement, in which the unlikely leakage error terms are ignored, will require the use of a minimum of three standards to determine the value of the 12 error coefficients that are part of the general error model. If the isolation and cross-talk errors are neglected, as is often done in practice, the number of error coefficients can be reduced down to 6 speeding up the calibration process [5]. The specific error terms neglected when isolation is omitted are

the forward and reverse terms, which account for leakage that occurs at the terminals of the network analyzer. Omitting the cross-talk error terms neglects leakage that bypasses the test fixture at the wafer or probe level.

For this thesis a $50\ \Omega$ LOAD, an OPEN and THRU are the standards that were used for calibration. These were packaged on a ceramic substrate (impedance standard substrate) that was provided with the coplanar microprobes. The error terms related to isolation were neglected in calibration since the isolation between ports is specified to be smaller than $-100\ \text{dB}$ [5].

Calibrating a measurement system beyond 20GHz can be a very difficult task requiring many attempts. Any perturbations to the measurement system, i.e. moving cables or changing connectors, require that the system be re-calibrated because the systematic errors (errors that calibration has been devised to deal with) will have been altered. Other types of errors, which calibration itself does not deal with, come into play to reduce the effectiveness of calibration over time. Such errors can be induced by random processes such as noise or caused by temperature drifts. Although difficult, achieving a good calibration is crucial in order to properly characterize an on-wafer device.

When a system is properly calibrated the properly formulated error model can safely be applied to subsequent measurements in order to eliminate the impact of the external measurement system. This will effectively move the reference plane from the internal measurement system to the probe/ bond pad interface.

2.1.2 De-Embedding

Once calibration is completed, non-idealities in the external measurement system have been taken into account. However, the on-wafer device interface parasitics are still part of the device measurement result. Thus, the measured S -parameters (corrected from calibration) are still representative of more than just the device. A typical on-wafer device interface (test-fixture for short) is shown in figure 4.3 surrounding the device, which is placed at the center.

Figure 2.3: On-wafer test fixture for measurement of integrated devices with two coplanar probes

In order to remove the parasitic effects of the test fixture and move the reference plane directly to the device boundary (i.e. at the point where the test-fixture interconnect meets the device) the parasitics associated with the test-fixture must be de-embedded from the measurement result. De-embedding is usually a post-processing error correction procedure since it is done when the measurements are complete.

The de-embedding methodology used in this thesis was originally proposed by [6] and is a commonly used approach [5], [7]. The method can correct for both series and shunt parasitics; these are shown in the equivalent circuit model for the test-fixture in figure 4.4. The shunt parasitic is the signal pad capacitance, C_{pad} and the series parasitics are the interconnect resistance, R_s , and inductance, L_s [5]-[7].

Figure 2.4: Equivalent circuit model for test fixture parasitics

In order for the parasitics shown in figure 4.4 to be de-embedded from the device measurement two additional test-fixtures, i.e. dummy test-fixtures are required to isolate all parameters involved. The two dummy test-fixtures that are needed include an open test structure and a test structure in which the interconnects leading to the device are shorted to ground at the center. Typical representations of both are shown in figure 4.5.

Figure 2.5: Short and open dummy test structures

The dummy open suffers only from a parallel parasitic while the short suffers from both parallel and series parasitics. The dummy open measurement can therefore be used to eliminate the pad capacitance from both the device fixture and short fixture measurements by subtracting the admittance of the open from the device and short

admittances. In order to rid the device measurement of the series parasitics the open corrected short impedance is subtracted from the open corrected device impedance. The result of the entire operation is simply the device impedance or admittance. The fully de-embedded device admittance is given by

$$Y_{dev} = \left(\left(Y_{dev_wp} - Y_{open} \right)^{-1} - \left(Y_{short} - Y_{open} \right)^{-1} \right)^{-1} \quad (2.1)$$

where Y_{dev_wp} is the admittance of the device with test structure parasitics, Y_{open} is the admittance of the open test structure and Y_{short} is the admittance of the short test structure.

Applying (2.1) to the measured data effectively brings the reference plane directly to the device (identified as desired reference plane in figure 2.2). Thus, after calibration has been performed and the data de-embedded the resulting measured data is a very good representation of the device behavior. This de-embedding method is widely accepted to provide an accurate enough measurement for modeling purposes.

De-embedding methodologies simpler than the one presented in this thesis exist. One principle method consists of de-embedding the shunt parasitics while neglecting any series parasitics. This de-embedding method only requires one test-fixture, but poor high frequency performance hinders its use [5].

2.2 Modeling Methodologies

Where characterization is the process of capturing the behavior of devices, modeling is the process of formulating functions which describe/predict the behavior of devices. Device models come in many forms (i.e. equivalent circuit models, empirical functions, s-parameter models and neural network representations) and various methodologies are employed to develop such models. Of significant importance is numerical EM modeling, neural network modeling and analytic or equivalent circuit based modeling. In

the following sections each methodology will be discussed in turn with particular emphasis on general application area, accuracy and computational demand of the model itself and process used in its creation.

2.2.1 Modeling with EM Solvers

Numerical electromagnetic based modeling generally involves the solution of Maxwell's equations in 2, 2.5 or 3 dimensions with the use of EM solvers. EM solvers, whether they use finite-element analysis or a planar presentation (method of moments approach), are computationally demanding and have a huge learning curve. They are, for the most part, impractical for integrated circuit simulation and optimization on a mass scale [8] and are thus mainly used to provide a reference for the development of a model using another methodology [9]-[11] and model critical paths/elements in a circuit.

Inaccuracies in EM solver results are also possible due to inherent assumptions made in the solution of Maxwell's equations or improper meshing of structures (i.e. with regards to the method of moments)[12].

Models generated with the use of EM solvers are generally represented by S -parameters although any two-port representation can generally be used. Any changes to a structure subsequent to the generation of the model in S -parameter form, for example, will require that the structure be fully analyzed once again and that a new S -parameter representation be developed.

2.2.2 Artificial Neural Network Models

Recently, the application of neural networks to modeling microwave active and passive devices has been investigated [8-11]. Various types of artificial neural networks (ANN) have been developed. Common to most ANNs, is the large amount of training data required in order to properly develop the neural network [9]. Usually, extensive EM simulations or measurements must be performed to build an adequate training

profile, thus requiring intensive effort. Once trained and verified neural networks have been shown to have very good predictive capability (on par with EM solver results) and are capable of dealing with variations in device layout without having to re-generate the model (as is the case with EM modeling). Variations on the basic form of the artificial neural network have been proposed such as the knowledge-based neural model [9] or space mapping based neural network model [10] with the goal of reducing the training time required. However, the initial development time remains demanding for one-time simulations of arbitrary structures where a single EM simulation will suffice. In circumstances where many variations on a common structure must be investigated, or any optimization is required, the adaptability of the neural network model becomes very attractive. The development time of the neural network model is far outweighed by the total simulation time of the EM solvers for the various configurations and thus a neural network approach would be advantageous.

In general, the neural network approach shares the same application areas as EM modeling. In [8], artificial neural networks were used to model lossy interconnects in VLSI circuits instead of using EM based models; the results show a massive reduction in optimization and simulation time. However, mass modeling on a circuit level of integrated passive components could be impractical due to the cost of training and subsequent validation of the models. In addition it is not clear that the neural network based approach would provide any computational advantage over standard equivalent circuit based models typically used in a CAD environment for integrated passive devices.

2.2.3 Equivalent Circuit Models

Equivalent circuit modeling is a widely used approach for modeling integrated devices including active and passive components. Equivalent circuit models are basically composed of an assortment of fundamental circuit building blocks such as capacitors, inductors, resistors and controlled sources that are interconnected in a specific fashion so as to represent the true behavior of the devices being modeled. The models are generally physics based because the values of the components included in the model, which are

representative of local electric or magnetic phenomenon, are calculated from closed-form analytic expressions derived to predict the respective physical behaviors involved.

Equivalent circuit models are also easily represented by a netlist and are thus ideal for integration in a CAD environment for circuit design and simulation. The models can also be used to perform time domain, i.e. transient, simulations and large signal simulations without modification unlike S -parameter models.

The accuracy achieved with equivalent circuit models is generally dependant on the number of phenomenons taken into account by the model and the assumptions made in the development of the analytic equations. In [13], for example, new concepts in the development of a compact equivalent circuit model for monolithic inductors are presented which lead to a more accurate representation and prediction of the behavior. Their results show very good agreement with measurements.

Although for high frequency applications equivalent circuit models can grow quite complex to account for various phenomena, simpler models can easily be implemented to model the device behavior at lower frequencies. Furthermore, such models can simply be derived from the more sophisticated versions by omitting parameters as they become irrelevant. This decreases the computational burden imposed by the model thus decreasing simulations times even further.

A trait that equivalent circuit models share with artificial neural network models is adaptability. Equivalent circuit models will usually have the physical dimensions of the device as input parameters therefore computing the values of all internal model elements based on the given inputs.

CHAPTER 3: Metal-Insulator-Metal Capacitors

In this chapter a high frequency compact equivalent circuit model for a metal-insulator-metal capacitor is presented. The model accounts for both magnetic and electrostatic phenomena. Low frequency models are then presented and tradeoffs between modeling accuracy and complexity are investigated.

3.1 Introduction to the Metal-Insulator-Metal capacitor

The metal-insulator-metal (MIM) capacitor is typically composed of two overlapping conducting layers, which are separated by a thin layer of dielectric material. The dielectric thickness is usually very thin to ensure a high capacitance is generated per unit area between the two overlapping conductors. There are various implementations of such MIM capacitors, some processes utilize existing metal layers to form the plates while others use dedicated metal layers, which require additional mask steps. A cross-section view of a MIM capacitor is shown in figure 3.1.

Figure 3.1: Cross-section view of a MIM capacitor

3.1.1 Models and Methodologies

An equivalent circuit model for MIM capacitors is presented in [14]. The proposed model consists of a simple pi-section that includes inductance, resistance and capacitance. The model was developed for MIM capacitors used on a GaAs substrate thus the effects of a conductive substrate on the behavior of MIM capacitors is not modeled or investigated. A similar equivalent circuit model is proposed in [15]. However, no specific information is given regarding the computation of the model parameters and the model was also only validated up to 18 GHz.

3.2 Level-2 Model: High Frequency Equivalent Circuit Model

The most advanced lumped equivalent-circuit model developed for the MIM capacitor in this research is termed the level-2 model. This model accounts for both electric and magnetic phenomena within the structure and therefore has the highest number of internal nodes and lumped elements. Its use would normally be restricted to higher frequency applications where models of lower complexity would not provide sufficient accuracy. The level-2 MIM capacitor model is shown in figure 3.2.

Figure 3.2: Level-2 equivalent circuit model for a MIM capacitor.

In order to create a model that is valid at high frequencies various parasitic phenomena, which are negligible at low frequencies must be considered. The proposed compact equivalent circuit model shown in figure 3.2 is composed of 8 lumped components and 5 internal nodes. The inductors, L_{m1} and L_{m2} , account for magnetic energy storage i.e. the magnetic fields created by the current flow in the MIM capacitor plates. The capacitors, C_{m21} and C_{ms} account for the electrical coupling between the metal plates and the coupling between the bottom plate and the substrate. The resistors, R_{m1} and R_{m2} model the losses in each electrode respectively. The resistor R_s represents the losses within the lossy silicon substrate and the capacitor C_s takes into account the dielectric nature of the substrate. It should be noted that the resistor R_s accounts for all loss within the substrate. For example, no distinction is made between the loss caused by electrical coupling or loss due to eddy current formation within the substrate. The following sub-sections will cover in detail every element included in the proposed high frequency equivalent circuit.

3.2.1 Electrical Coupling between Plates

The electrical coupling between the plates of a MIM capacitor is modeled by the capacitance, C_{m21} , in the high frequency model developed for this thesis. Since the inter-plate capacitance is a physical property of the two-conductor system the geometry of the two plates and the spacing between them will determine the amount of capacitance that is generated across the oxide. The capacitance C_{m21} will therefore have area and peripheral dependences, which are in turn governed by the dimensions of the smallest plate in the system. This is most often the top plate in MIM capacitors. The reason behind the distinct area and peripheral dependencies is due to electric field lines that originate from the surface of the plates (each plate in turn due to reversing polarity). Thus, field lines will emanate both from the periphery and plate surface area. An illustration of the electrical coupling between the plates is shown in figure 3.3.

Figure 3.3: Electric field lines coupling the top and bottom plate.

The per unit area component of the inter-plate capacitance accounts for the electric field lines that emanate from the plate surface area and thus it depends on the area of the plate. This capacitance is defined as a per unit area capacitance and is generally well described by

$$\hat{C}_{m21} = \frac{\epsilon \cdot \epsilon_r}{d} \quad (3.1)$$

which is the simple parallel plate capacitance equation where ϵ_r is the relative permittivity of the dielectric material and d is the separation distance between the top and bottom plate. The computation of the area component of capacitance using (3.1) assumes uniform charge distribution over the MIM capacitor plates.

The peripheral component of the capacitance accounts for the stray electric fields that emanate from the sidewalls of the plates. This capacitance is therefore a function of the periphery of the top plate unlike the direct coupling fields, which are a function of the top plate area. The characterization of the peripheral capacitance by means of an accurate and computationally efficient equation proves to be quite complex and has been the subject of much research. One method adopted by [16] and [17] applies function-fitting techniques to the results of two-dimensional field-solver simulations. The following equation developed by Meijs and Fokkema can be utilized to compute the peripheral component of capacitance [16].

$$C_{m21p} = (\epsilon \cdot \epsilon_r) \cdot \left[0.77 + 1.06 \left[\left(\frac{W}{d} \right)^{.25} + \left(\frac{Tm}{d} \right)^{.5} \right] \right] \quad (3.2)$$

where W is the width of the top plate, d is the separation distance between plates and Tm is the top plate thickness. The formula shown above must be multiplied by the length of the conductor because it was extracted from 2D field solver results. The accuracy it provides has been shown to be much better than similar methods, i.e [17], for geometries where large $\frac{W}{Tm}$ ratios exist making it the preferred choice for reasonably sized MIM capacitors[18].

The total capacitance between the two plates in a MIM capacitor represents the total electric energy storage within the system and is therefore the sum of area and periphery components. The total capacitance between plates can be defined as

$$C_{m21} = C_{m21}^A \cdot A + C_{m21}^P \cdot P \quad (3.3)$$

where A and P are the area and periphery of the smallest plate.

3.2.2 MIM Capacitor Magnetics

When a time varying currents flow through the conductive MIM capacitor plates, time varying magnetic fields are created. The time varying magnetic fields in turn induce electric fields in any conductors, or closed conductive loops, with which the magnetic fields are interacting. The induced electric fields will act upon the charges flowing through the plates to cause voltage drops. These induced electric potential drops are proportional to the magnetic capacity or inductance of the conductor loops. At high frequencies the induced electric potential drops become more significant and their effect must therefore be taken into account. Thus, inductors are included in the equivalent circuit in order to model the magnetic interactions within the structure.

The electric potential drops encountered in a conductor which are caused by a time varying magnetic field can be self-induced or be induced by other nearby conductive loops carrying time varying current. An electric potential drop that is induced into a conductor by a time-varying current flowing through the same conductor is proportional to the self-inductance of the conductor in question. Hence it is dependant on the

magnetic capacity of that specific conductor. An electric potential drop that is induced into a conductor by a time-varying current flowing through a separate conductive loop is proportional to the mutual inductance between the conductive loops. Thus, it is proportional to the magnetic capacity between the two conductors.

The self-inductance of a conductor or loop can be defined as the magnetic flux linkage per unit current in the conductor or loop itself. A closed-form expression for the exact self-inductance of a straight conductor has been developed by [19] and was subsequently expended upon by [20]. The self-inductance for a straight conductor of rectangular cross-section is given by

$$L_{self} = (0.002l) \cdot \left[\ln\left(\frac{2l}{a+b}\right) + .50049 + \left(\frac{a+b}{3l}\right) \right] \quad (3.3)$$

where L_{self} is the inductance in μH , l is the conductor length in centimeters and a and b are the dimensions of the cross-section in centimeters. The mutual inductance between two loops can generally be defined as the magnetic flux linkage with one loop per unit current in the other loop. In a two conductor system, the mutual inductance between the conductors is equal to the mutual inductance between two filaments, one in each conductor, that are separated by the geometric mean distance. Thus, the mutual inductance between two conductors of equal length is given by

$$M_{i,j} = 2lQ_{i,j} \quad (3.4)$$

where M is the mutual inductance in nanohenries, l is the conductor length in centimeters and Q is the mutual-inductance parameter which is a function of the geometric mean distance [20].

In the case of the MIM capacitor current flows in a continuous and unilateral fashion through each conductive plate, i.e. current flows into one plate and out the other plate as is shown in figure 3.4.

Figure 3.4: Inductive components in MIM capacitor. (Dotted line represents mutual inductance.)

The same current is therefore flowing through each MIM capacitor plate. The current flowing in the top plate will induce an electric field in the top plate at the same time it induces an electric field in the bottom plate. The same situation results with the current flowing in the bottom plate. An electric field will be self-induced into the bottom plate at the same time an electric field is induced into the top plate. Therefore each MIM capacitor plate will have self-inductance, i.e. self-induced electric fields, and mutual inductance. An equivalent circuit for the MIM capacitor plates, which takes into account the magnetic interactions, is shown in figure 3.5. The equivalent circuit only takes into account the plates; any losses within them are omitted.

Figure 3.5: Equivalent circuit for MIM capacitor plates

This is a correct physical model for the magnetic interactions. The equivalent circuit has inductors to model the self-inductances and a coupling term to account for the mutual inductance between the plates.

The plates in MIM capacitors are typically very close to each other in order to generate a high capacitance per unit area. The distance separating each plate can be on the order of a few hundred angstroms. Due to the proximity of the two plates their combined magnetic behavior can be simplified from that shown in figure 3.5. Essentially, the mutual term can be avoided if the effect is lumped with the inductors. In [14], Ladbroke alludes to such a procedure, but no specific account regarding the self and mutual inductances is given.

To illustrate this point, the magnetic field interactions within the plate structure must be revisited. A conductor can be thought of as being composed of finite conductive filaments which permeate the conductor and lie along the direction of current flow. This is demonstrated in figure 3.6 for MIM capacitor plates.

Figure 3.6: Mutual coupling interactions within MIM capacitor plate structure.

The self-inductance of a conductor, or in this case, the MIM capacitor plates, is the sum of the magnetic flux linkages between the filaments within the conductor. Thus, the sum of the mutual inductances between filaments is the self-inductance of the conductor. In MIM capacitors the dielectric layer separating each plate is very thin, i.e. typically on the order of a few hundred angstroms, therefore in terms of magnetic interaction the two plates act as one composite plate. Hence, this inductance analysis postulates that there is negligible error in evaluating the total inductance of the plates as the self-inductance of

the composite structure. The total effective inductance generated by the plates is therefore the self-inductance of the two plates if they were lumped together, i.e. the plates are so close together that the sum of the mutual interactions between the composing filaments is the same as the self-inductance of the composite plate. This analogy is demonstrated in figure 3.7.

Figure 3.7: Lumped plate equivalency in terms of magnetic interactions

The total inductance generated by the MIM capacitor as shown in figure 3.7 (a), i.e. the self-inductance of each plate along with the mutual coupling between the plates, is the same as the self-inductance of the lumped plate structure in figure 3.7 (b) if the separation distance between the MIM capacitor plates in case (a) is very small. The thickness of the lumped plate is that of both plates added together. Therefore the inductance generated by thin dielectric MIM capacitors can be computed using (3.3) where the dimensions are specified as being that of the composite plate. The lossless equivalent circuit for the MIM capacitor plates is therefore as shown in figure 3.8 where L_s is the inductance of the lumped equivalent plate. The equivalent circuit as devised here assumes lumped behavior.

Figure 3.8: Lossless MIM capacitor equivalent model for plate interaction

In the proposed high frequency equivalent circuit model of figure 3.2 the top and bottom plates are represented as two distinct circuit branches forming an axis of symmetry about C_{m21} . As a consequence and in order to represent the inductance of each plate in the high frequency model, the total block inductance, represented as L_s in figure 3.8, calculated from (3.3) is split between the top and bottom plate of the MIM capacitor. The contribution of each plate is assumed to be half of the composite plate inductance. Thus referring to figure 3.8 the inductances L_{m1} and L_{m2} of the high frequency equivalent circuit model are defined as

$$L_{m1} = L_{m2} = \frac{L_s}{2} \quad (3.5)$$

An erroneous assumption would be that only the self-inductance of each plate could be used to calculate the values for L_{m1} and L_{m2} . This ignores the magnetic linkage between both plates and would lead to an overestimation of the total inductance within the system.

3.2.3 Resistive Losses in MIM Capacitor Plates

The conductors forming the plates of typical MIM capacitors are lossy by nature. The losses encountered in the plates must be accounted for in an accurate model. For the purpose of this research the losses in the MIM capacitor plates are modeled in a frequency independent manner and the calculation is specifically done at DC where the computation is very simple. The resistance of the plates is given by

$$R_m = \frac{p \cdot L}{t \cdot W} \quad (3.6)$$

where p is the resistivity, L and W are the plate length and width. In most MIM capacitor implementations the capacitor plates will have a smaller L/W ratio than the conductors linking them to the rest of the circuit. Thus, the losses in the interconnect will easily overshadow the losses in the plate themselves. For this reason the skin effect or frequency dependant nature of the conductor resistance is ignored in the computation of the plate resistance. The modeling of the frequency dependant loss in thin film conductors, such as the capacitor plates, is an area of active research. Recent publications, [21] - [23], address this topic and present varying modeling methodologies.

3.2.4 Electrical Coupling to the Silicon Substrate

The bottom plate of the MIM capacitor will accumulate and transport charge if not used in a configuration where it acts as a ground. In such a situation, the charges flowing on the bottom plate of the MIM capacitor will cause charge of the reverse polarity to accumulate at the oxide/substrate interface in order to terminate the electric field. The charge cancellation will either be provided through accumulation of majority carriers or through the formation of a depletion region at the oxide interface. The process by which charge cancellation is provided will depend on the biasing of the bottom plate with respect to that of the bulk. The bottom plate and the substrate are therefore capacitively coupled.

In the high frequency equivalent circuit model shown in figure 3.2 the total electric capacity of the oxide region between the conductor and substrate is modeled via C_{ms} . The oxide capacitance, i.e. C_{ms} , will depend on the geometry of the bottom plate and the oxide thickness separating the plate and substrate. A cross-section view of such a system is shown in figure 3.9.

Figure 3.9: Cross-section view showing total oxide capacitance between bottom plate and substrate.

The metal to substrate capacitance will have an area and peripheral dependence. The portion of the capacitance that is a function of the bottom plate area is well described by the simple parallel plate capacitance equation, i.e. (3.1), where d is the thickness of the silicon dioxide or the distance between the bottom plate and oxide substrate interface. The capacitance that is a function of the periphery of the bottom plate can be computed using (3.2) as was done for the peripheral component of C_{m21} .

The total electric capacity of the oxide separating the bottom plate from the substrate is computed in the same manner as C_{m21} . The area and peripheral components are added to determine the total amount of capacitance. Thus, the following relation holds true

$$C_{ms} = \hat{C}_{ms} \cdot A + C_{msp} \cdot P \quad (3.7)$$

where the capacitive coupling is between the bottom plate and substrate, the capacitor C_{ms} is connected to the bottom plate terminal of the C_{m21} capacitor in the equivalent circuit model.

3.2.5 The Silicon Substrate

The electric capacity of the SiO_2 between the bottom plate and substrate has been explored and modeled via the capacitor C_{ms} , however, the oxide capacitance on its own is not a complete physical model for the relationship between the bottom plate of the capacitor and the substrate.

High resistivity substrates, such as those used in bipolar processes, act as a lossy medium for frequencies below approximately 8 GHz (for a typical substrate resistivity of $20 \, \Omega \cdot \text{cm}$) [24]. A resistor is therefore used to model the lossy nature of the silicon substrate. A total substrate resistance, R_s , which models all loss between the ground contact and the capacitor, is illustrated in figure 3.10.

Figure 3.10: Substrate represented as lossy medium

For low frequency applications modeling the substrate as a resistor suffices. However as demonstrated in [24], for frequencies higher than approximately 8 GHz the simple resistive model no longer accurately describes the substrate behavior. The principle reason behind the failure of the resistive model is that the dielectric nature of the silicon substrate is not taken into account. The capacitive nature of the substrate does not pose a problem at low frequencies; however, it can significantly affect device performance at microwave frequencies [24]-[27]. As such, the substrate capacitance must be included in the substrate model in order to correctly predict the behavior of passive devices in the double-digit GHz frequency range. The substrate capacitance and resistance are shown in figure 3.11 in a cross-section view of the substrate.

Figure 3.11: Dielectric nature of substrate modeled with capacitor

The substrate model presented in figure 3.11 and used in the MIM capacitor high frequency model was originally presented in [24]. Results presented in the same paper show that a lumped RC network can accurately model the substrate behavior up to very high frequencies.

For the purpose of this thesis the substrate parameters, C_s and R_s , are not calculated analytically due to the complexity of the problem [24]. Instead a curve fitting approach or empirical method is used to devise the parameter values. The following methodology can be used to determine the substrate parameters, C_s and R_s , for the high frequency model.

Firstly, a capacitance termed C_{mg} , i.e. metal to ground capacitance, is defined as follows

$$C_{mg} = \text{Im}(Z_{12})^{-1} \cdot \omega^{-1} \quad (3.8)$$

where Z_{12} is the impedance seen looking into the substrate shunting branch shown in a dashed box in figure 3.12.

Figure 3.12: Two-port representation of high frequency model

The metal to ground capacitance, C_{mg} , is the effective capacitance seen looking into the entire substrate network. The Z_{12} parameter for the level-2 model is given by

$$\text{Im}(Z_{12}) = - \frac{(1 + \omega^2 \cdot C_s^2 \cdot R_s^2 + \omega^2 \cdot C_{ms} \cdot C_s \cdot R_s^2)}{\omega \cdot C_{ms} + \omega^3 \cdot C_{ms} \cdot C_s^2 \cdot R_s^2} \quad (3.9)$$

Due to the relative values of C_{ms} , C_s and R_s , the low frequency C_{mg} is equal to C_{ms} and at very high frequencies C_{mg} converges towards the bulk capacitance. This can be explained as follows. At low frequency the substrate resistance effectively shunts the capacitance and the Z_{12} parameter is that of a series RC. The imaginary part of Z_{12} is therefore simplified from (3.9) to the following

$$\text{Im}(Z_{12}) = \frac{1}{\omega \cdot C_{ms}} \quad (3.10)$$

However, at very high frequencies, the substrate capacitance shunts the resistance and the substrate branch is effectively composed of two series capacitors. Since C_{ms} is often 10

to 15 times larger than the substrate capacitance the resulting series equivalent value is that of C_s . Therefore at very high frequencies C_{mg} is equal to the bulk capacitance.

The frequency behavior of C_{mg} is used as the basis for determining the substrate parameters. Since C_{ms} is well known the frequency dependent behavior of C_{mg} can be used to determine the substrate parameters. Thus, C_s and R_s can be optimized to achieve a curve fit between the model prediction of C_{mg} and the extracted C_{mg} from measured data. In this thesis, a Newton-Raphson optimization was performed to determine the substrate parameters.

A complete low frequency model would include scaling relationships to avoid per device extraction. Resistance is expected to be more difficult in this regard than capacitance due to its obvious dependence on the placement of substrate ground contacts.

3.3 Experimental Verification

Three MIM capacitor structures were fabricated using the STMicroelectronics SiGe2 process [28] in order to provide some experimental comparison for the MIM capacitor model. S -parameter measurements were performed on each device at three different sites on the wafer. Measurements were taken up to 40 GHz, which was the frequency limit of the test equipment.

3.3.1 The SiGe2 MIM capacitor

The MIM capacitors available in this technology, which has three levels of interconnect, are created using an overlay of second level metal and first level metal. A thin oxide layer of approximately 350 Angstroms is deposited via chemical vapor deposition on top of the first level metal where the MIM capacitor structure is to reside. This creates a capacitance in the thin oxide area of $1 \frac{fF}{\mu m^2}$ nominally between both metals

versus $0.02 \frac{fF}{\mu m^2}$ for typical interconnect capacitance in the same process. A cross-sectional view of the MIM capacitor is shown in figure 3.13.

Figure 3.13: Cross section view of MIM capacitor

The design rules require that both metal plates extend beyond the thin oxide region. This is specifically a yield issue since it is done to prevent defects from forming in the MIM capacitors. The minimum requirements are that the MIM capacitor bottom plate extend two microns in length and width beyond the thin oxide area while the top plate must extend one micron in both dimensions. This principle is illustrated in figure 3.14.

Figure 3.14: Top view of MIM Capacitor

3.3.2 Sample Devices

The design layer physical dimensions for the three MIM capacitor test structures implemented for this research are shown in table 3.1.

Devices (low frequency capacitance)	1 pF	2 pF	5 pF
Thin oxide window width (μm)	31.4	33	56
Thin oxide window length (μm)	31.4	60	90
Top plate width (μm)	33.4	35	58
Top plate length (μm)	33.4	62	92
Bottom plate width (μm)	35.4	37	60
Bottom plate length (μm)	35.4	64	94
Bottom plate thickness (μm)	1.02	1.02	1.02
Top plate thickness (μm)	1.02	1.02	1.02

Table 3.1: Physical specifications for the sample devices

3.3.3 Measurement Setup

The MIM capacitors were characterized with the use of s-parameters. The measurements were performed with a setup as shown in figure 3.15.

Figure 3.15: MIM capacitor measurement setup

The equipment used to generate and measure the voltage waveforms consists of an HP8510B vector network analyzer, HP83651B synthesized sweeper and an HP8517B s-parameter test set. The measurements were performed on-wafer though the use of a

semi-automatic probing station equipped with 40GHz GSG microprobes (40A-GSG-100-P) fabricated by Picroprobe.

3.3.4 High Frequency Model Parameters

The level-2 model parameters for the MIM capacitors are listed in table 3.2. The parameters, except for R_s and C_s , which model the substrate, have not been optimized to match the measured results. The substrate parameters were determined as explained in section 3.2.5. All other parameters were computed using the procedures and equations presented in the respective parts of section 3.2.

MIM capacitor	5 pF	2 pF	1 pF
L_{m2} (pH)	16.9	11.5	4.9
L_{m1} (pH)	16.9	11.5	4.9
R_{m2} (Ω)	0.044	0.05	0.028
R_{m1} (Ω)	0.15	0.17	0.096
C_{m21} (pF)	5.06	1.99	0.99
C_{ms} (fF)	130	58	31
C_s (fF)	10	4.2	2.2
R_s (Ω)	432	625	1130

Table 3.2: MIM capacitor Level-2 Model Parameters

3.3.5 Measurement Results and Level-2 Model Predictions

In this section the validity of the level-2 compact equivalent circuit model is verified through comparisons of the model predictions with respect to the devices' measured behavior. Specifically, the through path effective capacitance and the effective metal to substrate capacitance, or C_{mg} as introduced in section 3.2.5, will be compared from 100 MHz to 40 GHz.

The through path effective capacitance is extracted from the device and model with the following

$$C_{eff}(\omega) = \text{Im}(Y_{11}) \cdot \omega^{-1} \quad (3.11)$$

The effective capacitance generated by the models is compared to that exhibited by the devices in figure 3.16.

Figure 3.16: Effective capacitance comparison for all three devices.

The curves represent the effective capacitance of the devices and model as extracted with (3.11). There is relatively good agreement between model and device considering only the substrate parameters have been fit from the measurements. In the case of the 2pF and 5pF MIM capacitor the model correctly predicts the self-resonant frequency of each device. The small plate size of the 1pF MIM capacitor leads to a self-resonant frequency that lies beyond 40 GHz.

The largest difference between model and measurement, before resonance has occurred, is seen in the 1pF comparison. There is reasonably good agreement up to about 30 GHz (difference of approximately 4% between prediction and measurement at 30 GHz) after which the curves diverge at an increasing rate. The self-resonant frequency of

this device computed using the total inductance and C_{m21} is found to be approximately 50 GHz. Part of the discrepancy between model and measurement can probably be attributed to the fact that resonance is near. A reasonably small percentage difference between the prediction of the self-resonant frequency and the actual measurement usually translates to a much larger error in the near resonance region. In addition, the measurement becomes slightly noisy beyond approximately 33 GHz, which may be the result of some measurement related sensitivity.

The extraction of the effective capacitance proves to be relatively independent of the substrate network due to the ground that is inherently present on the bottom plate in the extraction therefore the through path components shown in figure 3.17 generally determine the shape of the effective capacitance curve. The inductances, L_{m1} and L_{m2} , combined with C_{m21} determine the self-resonant frequency of the MIM capacitors while the resistances, R_{m2} and R_{m1} , due to the effect of the inductance, control the slope and height of the resonant peaks.

Figure 3.17: High frequency model without substrate path

In order to demonstrate that the effective capacitance is invariant to the substrate path the effective capacitance of the of the 5pF MIM capacitor is extracted using (3.11) from the model shown in figure 3.17. The full analytic equation describing the effective capacitance for the network in figure 3.17 is shown in (3.12).

$$C_{eff}(\omega) = \frac{\omega \cdot C_{m21} \cdot (1 - \omega^2 \cdot C_{m21} \cdot [L_{m2} + L_{m1}])}{(1 - \omega^2 \cdot C_{m21} \cdot [L_{m2} + L_{m1}])^2 + \omega^2 \cdot C_{m21}^2 \cdot (R_{m1} + R_{m2})^2} \cdot \omega^{-1} \quad (3.12)$$

The computed result using (3.12) is compared to the extraction of the effective capacitance using (3.11) from the 5pF MIM capacitor measurement data. The results are shown in figure 3.18.

Figure 3.18: Effective capacitance of model without substrate network

The effective capacitance extracted from the 5pF device, hence from the measured data, and that generated using (3.12) are almost identical indicating that the behavior of the MIM capacitor with the bottom plate grounded is invariant to the substrate network. As a result the validity of the model is not assured with a comparison of the effective capacitance. A hypothetical model which did not account for the substrate path would fail in circumstances where a load connected to the bottom plate of the MIM capacitor is comparable in terms of impedance to the substrate path. In order to verify that the substrate path is modeled correctly it must be isolated to some extent and verified independently.

An extraction of the effective bottom plate to ground capacitance, C_{mg} , is used to show agreement between the high frequency model and device in terms of the substrate path. The effective metal-to-ground capacitance is extracted from the devices and high frequency model using (3.8). The results are shown in figure 3.19 for all three devices.

Figure 3.19: Effective metal to ground capacitance

There is good agreement between the substrate path model and the behavior exhibited by the devices. In all three cases the effective metal to ground capacitance starts off virtually equal to C_{ms} and then subsequently converges towards the substrate capacitance. As explained in section 3.2.5 this is caused by the relative size of the two capacitors and the resistor. Thus, the results agree with the theoretical expectations.

The high frequency model has been verified through comparisons with three distinct devices. The model predictions are very good considering that the parameters, other than R_s and C_s , have not been optimized in any fashion. The model was verified up to 40 GHz because that was the limit of the test equipment. However, the validity of the model may well extend beyond this measurement limit. The through path effective capacitance, and the metal to ground capacitance were used to compare the model to the

devices. These two figures of merit are enough to cover all the bases and show agreement between model and device.

Models of lower complexity will now be presented and the tradeoffs between predictive capability and computational efficiency investigated.

3.4 Level-1 MIM Capacitor Model

The high frequency equivalent circuit model, identified as the level-2 model, was developed in order to be able to predict MIM capacitor behavior out to very high frequencies. The model has been experimentally verified up to 40GHz, which was the limit of the measurement equipment. The level-2 model is relatively complex, possessing 5 internal nodes, which makes for a relatively high computational load. Simulating with such a complex model below GHz frequencies or even in the low single digit GHz frequencies, where the MIM capacitor is close to ideal, is a waste of compute time. A simpler model, termed level-1, suitable for accurate low frequency simulations is presented as an alternative to the high frequency model.

The level-1 model, shown in figure 3.20, sacrifices higher frequency accuracy for greater computational efficiency at lower frequencies. For this reason it possesses three internal nodes instead of five. The only difference between the level-2 and level-1 model is that the level-1 model ignores the magnetic fields created by current flow in the plates. Hence the inductors are removed from the level-2 model to create the level-1 model.

Figure 3.20: Equivalent Circuit Representation of Level-1 Model for MIM capacitor

The lack of inductors severely restricts the predictive capability of the level-1 model at high frequencies (the frequency at which the lack of inductance causes a noticeable error between model prediction and measurement is dependant on the geometry of the device in question); however, having removed 2 internal nodes from the more complex level-2 model improves its computational efficiency. The effective capacitances predicted by the level-1 model for all three devices are compared to the measurements in figure 3.21, 3.22 and 3.23.

Figure 3.21: Effective capacitance predicted by level-1 model for 5pF device

Figure 3.22: Effective capacitance predicted by the level-1 for the 2pF device

Figure 3.23: Effective capacitance predicted by the level-1 model for the 1pF device

The Y_{11} parameter for the level-1 model can be represented by the following expression.

$$Y_{11_L1} = \frac{\omega^2 \cdot C_{m21}^2 \cdot (R_{m1} + R_{m2})}{1 + \omega^2 \cdot C_{m21}^2 \cdot (R_{m1} + R_{m2})^2} + j \cdot \frac{\omega \cdot C_{m21}}{1 + \omega^2 \cdot C_{m21}^2 \cdot (R_{m1} + R_{m2})^2} \quad (3.13)$$

The effective capacitance, obtained via the Y_{11} parameter, is therefore given by

$$C_{eff} = \frac{\omega \cdot C_{m21}}{1 + \omega^2 \cdot C_{m21}^2 \cdot (R_{m1} + R_{m2})^2} \cdot \omega^{-1} \quad (3.14)$$

where it can be seen that the effective capacitance predicted by the level-1 model is slightly frequency dependant, however unlike the frequency dependence seen in the measurements, in this case it is not due to inductance, but to resistance. The level-1 model predicts that the through path effective capacitance will decrease as the frequency increases. This slope will be very small however, because the resistances are small. In the case of the 1pF MIM capacitor the level-1 model prediction is within 5% of the device data up to ~13GHz. As for the other two sample devices, the 2pF and 5pF devices, the level-1 model remains within 5% until roughly 5.5GHz and 3.2GHz respectively. The level-1 model is therefore severely restricted in terms of bandwidth when compared to the level-2 model for such large devices; however, it is accurate and valid for a certain bandwidth, which for these devices is the lower, single digit GHz frequencies.

The level-1 model can accurately predict the behavior of the MIM capacitor within its operational bandwidth because no other components were removed from the level-2 model. The Y_{11} quality factor predicted by the level-1 model closely matches that measured from the device, as is shown in figure 3.24 for the 5pF device, because the plate resistances were not omitted. The Q predicted by the model does not perfectly match the quality factor of the device because the Q is also a function of inductance, which the level-1 model does not take into account. This is clearly evident in figure 3.24

where the quality factor predicted by the model does not reach 0. However, the overall dependency of the Q on the inductance is small compared to the dependency on the resistance and capacitance.

Figure 3.24: Quality factor predicted by the level-1 model for the 5pF device

The substrate network is included in the level-1 model at the expense of one additional internal node because it can perturb the dynamics of the MIM capacitor even within the limited modeling range of the level-1 model. In applications where neither MIM capacitor port is grounded, such as inter-stage coupling capacitors, the substrate network can shunt the load and reduce power transfer efficiency. In other words, C_{ms} and the substrate network become part of an RC filter. The implementations shown in figure 3.25 were used to show that C_{ms} and the substrate network can have detrimental effects on the performance of the MIM capacitor irrespective of the frequency range and should therefore be included in the level-1 model. The plate resistances were ignored in the simulations because the load resistances were considerably larger.

Figure 3.25: Test bench for the characterization of substrate loss in the level-1 model

The level-1 model was connected to a 200Ω , 100Ω and 50Ω load in order to quantify the amount of signal loss occurring due to the metal-1 to substrate shunting path. The load resistance seen by the source is plotted for each load in figure 3.26 for the two cases shown in figure 3.25; the first case takes into account the substrate effect or the substrate capacitance and resistance while the second does not. In the second case the substrate is modeled as an ideal ground plane. The simulations were based on the 5pF MIM capacitor parameters.

Figure 3.26: Effective load resistance for level-1 model with and without substrate network

Both cases of the level-1 model predict that the 5pF MIM capacitors driving loads greater than 50Ω will see signal loss through the substrate due to the presence of the metal to substrate capacitance. However, even within the limited application band of the level-1 model, the signal loss predicted by the model with and without the substrate network diverge. The amount of signal loss is greater for the model with substrate network. Neglecting the substrate network in the level-1 model to reduce the node count further would therefore produce erroneous results. The level-1 model accounts for the substrate network in order to provide accurate results within its usable bandwidth. The tradeoff between modeling accuracy and model complexity is clear in this instance.

In summary, the level-1 model provides a complete representation of the MIM capacitor behavior in the low single digit GHz frequencies down to DC. The reduction in model complexity via the removal of inductance proves to be a natural regression in the model complexity because the main effect is a reduction in usable bandwidth not a reduction in modeling accuracy throughout the entire spectrum. Thus there is no need or

opportunity to redistribute errors over the remaining model terms. The omission of inductance from the model limits its ability to predict the behavior of the MIM capacitor at higher frequencies where the inductive reactance is of similar magnitude to the capacitive reactance. Thus, the model will not predict the self-resonant frequency or the increase in effective capacitance that occurs near resonance.

3.5 Level-0 MIM Capacitor Model

The level-1 model, although simplified from the level-2 implementation, is still relatively complex; possessing 3 internal nodes, which only enables it to model a restricted bandwidth with good accuracy. In this section, a further simplified model will be presented, one that has no internal nodes for optimum computational efficiency. This is achieved at the expense of the model's predictive capability. The difference between the level-1 and level-0 models is that the level-0 implementation models the substrate as an ideal ground plane and ignores resistive loss.

Due to their dominant behavior at the lower frequencies electrical coupling from top plate to the bottom plate and that from the bottom plate to the substrate are the only two electrical effects that are modeled in the level-0 implementation. The model is therefore composed of two capacitors. The first is C_{m21} , which models the top plate to bottom plate capacitance. The second, C_{ms} , models the bottom plate to substrate capacitance. An equivalent circuit representation of the level-0 model is shown in figure 3.27.

Figure 3.27: Level-0 equivalent circuit model

Particular to the level-0 model is the prediction of an infinite quality factor and perfect -90 -degree phase shift, since the model neglects all resistive losses in the structure. The simplifications cause the model predictions to be less accurate than the level-1 model and in some instances such as the quality factor prediction; the result will be totally erroneous.

The through path effective capacitance predicted by the level-0 model is given by the following

$$C_{eff} = \text{Im}(Y_{11}) \cdot \omega^{-1} = \omega \cdot C_{m21} \cdot \left(\frac{1}{\omega} \right) \quad (3.15)$$

Thus, the through path effective capacitance will be constant with frequency irrespective of the capacitor size. In terms of the effective capacitance the model will have the same accuracy as that of the level-1 implementation because the plate resistances (included in the level-1 model) are very small and only cause the effective capacitance to roll off significantly at frequencies beyond the level-1 and level-0 modeling range. The limitation of the level-0 model is that it cannot be used to gauge the quality factor or losses incurred in the MIM capacitor.

The metal to substrate capacitance is included in the model because it does not add any internal nodes and permits (to a certain extent) the model to take into account any signal loss in the substrate. Although not a perfect representation, as seen in figure 3.23, C_{ms} included on its own provides a limited degree of accuracy while keeping the internal node count to zero. The amount of signal loss to the substrate will not be very accurate because the substrate network is ignored.

The model presented in this section is adequate for lower frequency applications where the resistive losses of the MIM capacitor are not an issue. The model is tailored to be computationally efficient for the frequency range where the complexity of the more advanced models is not required. In many cases the resistance of the interconnect leading to the MIM capacitor will overshadow that of the device itself and in such circumstances the level-0 model coupled with interconnect resistance will yield accurate results in terms

of the MIM capacitor loaded-Q and phase shift in the bandwidth of interest. Also, in applications where the bottom plate of the MIM capacitor is grounded, the substrate branch in the level-1 model is effectively shunted and therefore has no impact on the behavior of the device. In such circumstances, the line between the level-0 model and level-1 model is blurred; the level-0 model can essentially be used to provide the same degree of accuracy as the level-1 model saving much compute time.

3.6 Summary

In this chapter a high frequency equivalent circuit model for a MIM capacitor was developed. The model accounts for various parasitics such inductance and substrate effects, which can significantly affect device performance at high frequencies. A procedure for determining the effective inductance based on a composite plate approximation was introduced with emphasize on the self and mutual inductance interactions. The high frequency model predictions were compared to measurements of actual devices. The results show very good agreement up to 40GHz. The parameters in the high frequency model can be determined as follows: R_s with (3.6), L_s with (3.3) and then L_{m1} and L_{m2} with (3.5), C_{m21} and C_{ms} with (3.1) and (3.2). Substrate resistance and capacitance are determined through curve fitting since they are very difficult to describe analytically.

Finally, lower complexity models were developed by selectively neglecting components on the high frequency model that are of specific importance at high frequencies. The results show a restriction in usable bandwidth, but very good agreement was seen at lower frequencies.

CHAPTER 4: Varactor Diode

In this chapter a varactor diode high frequency compact equivalent circuit model is presented. The model accounts for both magnetic and electrostatic phenomena. The compact equivalent circuit is derived from a higher order model, which was developed from the actual physical structure.

4.1 Introduction to the Varactor Diode

The varactor diode, a variable reactance device, finds use in circuits such as voltage-controlled oscillators where the variable capacitance, generated by the depletion region at the anode/cathode PN junction, is essential for frequency tuning. The capacitance is controlled through the application of a voltage that modulates the depletion region thickness. Varactors are not generally operated in strong forward bias since the resultant current is usually detrimental to circuit operation. Typically they can be operated from a pre turn-on bias voltage, in order to take advantage of the resulting narrow depletion region, which maximizes the capacitance, to near breakdown where the capacitance is at a minimum.

4.1.1 Device types

Varactor diodes can theoretically be formed from any PN junction, although some configurations will be better suited for the purpose. Often, the collector-base junction of a bipolar junction transistor is used. The emitter-base junction can also be used, however, this arrangement typically has poorer performance. Some processes specifically offer custom varactor diodes. The cathode of these custom devices is normally formed using the NPN bipolar collector sinker and buried layer, while the base is used as the anode. Typically the base or anode will have a custom implant. Custom varactor diodes often have a greater capacitance tuning range due to the optimized doping profile in the base implant. A cross-section view of a custom varactor diode is shown in figure 4.1.

profile in the base implant. A cross-section view of a custom varactor diode is shown in figure 4.1.

Figure 4.1: Cross-section view of varactor diode

Varactor implementations usually possess a buried layer and cathode implant because they serve as a low resistance return path for charges flowing to the cathode, hence reducing the loss in the structures. To this end, the cathode implant and buried layer are highly doped.

4.1.2 Depletion Capacitance Performance Metrics

Important figures of merit for varactor diodes are the tuning range and linearity of the capacitance versus voltage characteristic. The tuning range is characterized by the ratio of the depletion capacitance at two points along the $C(V)$ curve. The greater the ratio the more tuning is available to circuits such as a VCO. Linearity characterizes the slope of the capacitance vs voltage curve. Linear varactors are desired for more uniform phase noise performance over the tuning range in a VCO [29].

4.1.3 Varactor Diode Layout

A varactor diode can be laid out in various configurations. Two layouts of a varactor diode are shown in figure 4.2 and 4.3

Figure 4.2: Varactor diode with single anode and cathode contact

Figure 4.3: Varactor diode layout with multiple anode and cathode contacts

The layout of figure 4.2 describes a diode with only a single anode and cathode contact. The configuration has a longer average path from the anode to the cathode than the multi-anode and cathode configuration shown in figure 4.3. In terms of buried layer resistance the shorter average path of the multi-finger approach coupled with its parallel nature will result in a smaller buried layer resistance than the corresponding single anode-cathode varactor for the same active area. Hence, the layout in figure 4.2 will have more buried layer resistance than the corresponding multi-finger varactor. On the other hand, the

contact resistance on a per finger basis is higher in a multi-finger implementation because the contact areas are smaller. However, due to the parallel nature of the fingers in an interdigitated device, the total equivalent resistance of the diode will again be smaller than the equivalent resistance for a structure with a single anode and cathode contact. Therefore varactor diodes laid out as shown in figure 4.2 will exhibit poorer performance than an equivalent device laid out in the fashion depicted in figure 4.3.

The layout of a multi-finger structure must be carefully considered to derive optimal performance. There are several factors to consider such as the length and width of fingers, the number of fingers and specifically at high frequency the phase delay between the signals in each finger. The delay is non-zero if laid out as shown in figure 4.4(a). The current in the middle fingers will lead those in the outer fingers. This complicates the behavior of the varactor diode as will be discussed in section 4.2.2. A solution, shown in figure 4.4(b), which mitigates the phase delay problem is to gradually increase the interconnect width so that the currents in each finger are virtually synchronized. Essentially, the distance between each finger and the center of the interconnect is much closer with the implementation shown in (b).

Figure 4.4: Multi-finger varactor shown under two different connection schemes

4.1.4 Models and Methodologies

Recent work on varactor modeling, [30]-[33], has concentrated on metal-oxide-semiconductor (MOS) varactors. Although different from diode varactors, which are modeled in this thesis, similarities between the devices exist regarding high frequency behavior and modeling. Of specific interest are inductance and its impact on high frequency operation. Therefore the published works in this area are of some relevant interest.

The MOS varactor models developed in [31]-[33] have been verified up to approximately 10 GHz. This is considerably lower in frequency than the range of interest for this thesis. Nonetheless, measurement results show increases in effective capacitance with frequency even within this limited band. The majority of devices measured generated picofarads of capacitance, which explains the large increases (3x in one case) seen at these relatively low frequencies. The authors have made an attempt to account for this increase by adding an inductor in the model, the purpose of which is to model the gate inductance. However, the inductance value is simply extracted from the measurement result and used as a fitting parameter.

Although the authors have not modeled the inductance in a concise and analytic fashion, the results do speak to the importance of this parasitic and provide further justification for the work undertaken in this topical area.

4.2 Level 2 Model: High Frequency Compact Equivalent Circuit Model

The most advanced model developed for the varactor diode in this thesis is termed the level-2 model. This model accounts for both electric and magnetic phenomena within the structure. The level-2 model possesses many internal nodes and is therefore computationally demanding relative to lower frequency models. A compact equivalent circuit representation is shown in figure 4.5.

Figure 4.5: Level-2 Compact Equivalent Circuit Model for varactor diodes

The compact equivalent circuit is composed of seven lumped components and possesses four internal nodes. It includes the inductances identified as L_s to account for magnetic field interaction between the metallic fingers. The resistor, R_{eq} , accounts for the losses. A diode, DAC, essentially a variable capacitance identified as $C_j(V_d)$, models the behavior of the anode to cathode PN junction while the diode, DCS, identified as $C_{sj}(V_d)$, models the behavior of the buried layer to substrate PN junction. A capacitor, C_s , and resistor, R_s , are included to model the effects of the bulk.

The following sub-sections will review in detail the development of the compact model from the physical nature of the device. The origin of each model parameter and the computations used to find the equivalent values for the compact model are presented.

4.2.1 Anode to Cathode Active Depletion Capacitance

There are typically two depletion regions formed within a varactor diode structure. The first, modeled by DAC, is formed between the p^+ polysilicon contact or p^+ diffusion under the anode and the n-type anode implant. The second, represented by DCS, is formed between the buried layer (n^+) and the bulk substrate (p) (see figure 4.1). These two depletion regions are the source of the depletion capacitances.

The depletion region width, which varies in response to a modulating voltage, can respond to very high frequency signals because majority carriers are responsible for shortening or widening the depletion region [34]. The depletion capacitances are therefore invariant throughout the frequency spectrum of interest in this thesis and can therefore be calculated using the standard computation methods.

It should be noted that the capacitances have peripheral and area dependencies and that each may be implemented separately for accuracy. However, the extraction of required parameters and the methodology for computing the values from the geometry has already been developed [35]. The detailed computation of the capacitances is therefore not explored in this thesis for the afore mentioned reason and also because these are low frequency modeling issues.

The varactor diode is not usually operated in strong forward bias, where the depletion region width becomes very small and where a significant increase in mobile charge leads to diffusion capacitance [34]. A varactor diode model therefore does not need to include diffusion capacitance.

For the purpose of this work a depletion capacitance per finger area is defined for the anode/cathode junction, essentially abstracting the contribution of area and periphery to the finger capacitance. The total zero-bias junction capacitance is therefore given by

$$C_{j0} = \hat{C}_{ac} \cdot A_f \cdot N \quad (4.1)$$

where $\hat{C}_{ac}$ is the total capacitance generated per finger normalized to the finger area, A_f is the area of one anode finger and N is the total number of anode fingers. The capacitance, C_{ac} , is therefore defined as being the capacitance associated with one anode finger.

The voltage dependence of the anode to cathode depletion capacitance is well represented via (4.2), where V_d is the applied potential, C_{j0} is the zero-bias depletion capacitance, V_{bi} is the built in potential and m is the grading factor, but only until the depletion region extends to the edge of the buried layer.

$$C_j(V_d) = \frac{C_{j0}}{\left(1 - V_d/V_{bi}\right)^m} \quad (4.2)$$

The high doping density of the typical buried layer will limit the expansion of the space-charge region because charge neutrality is achieved with a much smaller incremental volume. Hence, dC/dV becomes much smaller to the point where the depletion capacitance virtually remains constant. Some diode models have the ability to predict this capacitance limiting effect. An accurate collector-base model for a BJT will have this ability [36].

4.2.2 Multi-Finger Inductance

In this section the inductances within multi-finger varactor diodes are considered and a methodology for developing a compact model, which takes into account inductance in multi-finger structures is presented. Due to the complexity of this problem, the scope of the analysis is initially restricted to magnetic and capacitive interactions because both are closely tied together. Thus, resistance is ignored initially, but is considered in the following section and the varactor model is altered in consequence.

The inductance included in the compact equivalent circuit, shown in figure 4.5, originates from the metal that forms the contact electrodes. Each of the electrodes or fingers in a varactor diode will carry time-varying current and by Ampere's law these currents will in turn create time varying magnetic fields. As explained in chapter 3, time varying magnetic fields which intersect conductors or loops will lead to the generation of electric fields within those conductors, i.e. fingers in this case, that cause potential drops. The resulting potential drops due to the induced electric fields are related to the time varying current, which instigated the induction process, by the magnetic capacity of the fingers or system of fingers. Thus, as was the case with the MIM capacitor plates, two distinct inductive effects will be present in each finger.

The first is self-inductance, as defined in chapter 3, and the second, also introduced in chapter 3, but reviewed here in the context of a multi-conductor system, is mutual inductance, which is caused by magnetic field interactions between conductors. The time varying magnetic field generated by current flow in one conductor or conductive loop intersects a second conductor or conductive loop and induces a time-

varying electric field that results in a voltage drop in the other finger. The mutual inductance between the conductors/fingers is the proportionality constant between the induced potential drop and the time-varying current that caused the formation of the time varying magnetic field. A representation of a multi-finger varactor showing the self-inductances and mutual coupling is shown in figure 4.6.

Figure 4.6: Self and mutual inductances for a 2-anode finger and 2-cathode finger device

The dotted arrows represent the mutual coupling between fingers. The current flow in such a structure, from anode to cathode and vice-versa, is unilateral in the sense that current flows in the same direction for all the fingers. The result is a magnetically induced voltage from the primary fingers into victim fingers that adds to the already existing voltage in those fingers. The electric field induced in the victim fingers will have the same orientation as the resident E-field due to the current being in phase. Hence, an additional voltage drop will be present in the victim loop. The mutual inductance linking each finger can therefore be stated as being positive mutual inductance. Each finger can be thought of as a primary finger (i.e. induces voltages in other fingers) and victim finger (i.e. its voltage drop becomes dependant on the current in other fingers) at the same time.

The computation of the finger self-inductance is done accurately with the extended Grover equation (3.3). The mutual inductance is a function of the conductor lengths and geometric mean distance. The equation presented by Grover for determining the mutual inductance between two parallel conductors/filaments is given in (3.4).

In this thesis, for the purpose of the mutual inductance computations, it was assumed that the lengths of the fingers were equal; hence the overlap of anode and cathode fingers was assumed complete. However, in an interdigitated structure the overlap of the anode fingers with respect to the cathode fingers is not complete. A segment of the overall finger length, denoted by $2\Delta L$ in figure 4.7, does not find itself with a parallel segment in the anode/cathode. This length is usually constant therefore its percentage of the overall length goes down as the finger length increases. Thus, $2\Delta L$ is assumed to be negligible. It should be noted that the anode to anode and cathode to cathode overlap are complete indicating that only a portion of the mutual terms will have some error caused by $2\Delta L$.

Figure 4.7: Overlap mismatch between anode and cathode fingers

The first step in computing the lumped inductances for the compact model, which are shown in figure 4.5, is to localize the mutual coupling to victim fingers. Localization is the process by which the mutual inductances, which represent the magnetic interactions between fingers, are instantiated as inductors and introduced into the victim loops of an equivalent circuit. Thus, a phenomenon which is typically not represented by an explicit instance in a circuit representation but by a mathematical relationship in the form of a coupling coefficient, is transformed into an inductor and integrated into an equivalent

circuit. This is similar to the approach used by Greenhouse in [20]; however, the important difference is that in this case the localization is done to parallel victim branches or loops. Thus, an instantiated mutual inductance is placed in series with the self-inductance of a *parallel* branch, not simply in series with the same loop or branch that induced a voltage into itself, i.e. in series with the self-inductance of a loop that had mutual coupling to itself, as done in [20].

The localization process places the self-inductance of the fingers in series with an inductance that is caused by the mutual coupling between parallel branches. This makes the voltage drop incurred by the victim finger, due to the mutual coupling, dependant on the current in the victim finger rather than the current in the primary finger. In a system consisting of two separate loops that are magnetically coupled, such as a transformer, the localization of the mutual terms to the primary and secondary loop is only valid if the loop currents are equal. The system shown in figure 4.8 represents such an example.

Figure 4.8: Transformer example

The voltage, V_1 , in the primary loop is given by

$$V_1 = L_1 \cdot \frac{dI_1}{dt} + M_{2,1} \cdot \frac{dI_2}{dt} \quad (4.3)$$

which clearly shows that V_1 is dependant on the current in the secondary loop. If the currents are the same, i.e. $I_1 = I_2$, the equation can be restated as follows

$$V_1 = L_1 \cdot \frac{dI_1}{dt} + M_{2,1} \cdot \frac{dI_1}{dt} \quad (4.4)$$

which is equivalent to saying that an inductance of value $M_{2,1}$, is in series with the self-inductance L_1 . Therefore the mutual inductance can be localized to the primary loop in such circumstance. However, if the loop currents are not equal, then such an operation will introduce an error in the voltage computation related to the difference between the two currents. Thus, to assess the impact of mutual inductance localization in the varactor fingers, the finger current values must be investigated.

In order to understand the current flow relationships and the localization issues a physical multi-finger model of the varactor diode must be introduced. To this end, a multi-finger physical equivalent circuit model of a 2-anode finger and 2-cathode finger varactor diode, which takes into account the mutual coupling, finger self-inductance and anode to cathode capacitive coupling is shown in figure 4.9. The losses in the structure are neglected at this point in time. The dotted lines represent the mutual coupling.

Figure 4.9: 3D multi-finger equivalent circuit for a 2-anode and 2-cathode finger device

The anode segments are composed of the self-inductance and depletion capacitance, which is distributed around the inductance. The cathode segments on the other hand are solely composed of inductance. The example shown in figure 4.9 is for a 2-anode 2-cathode finger device, however, larger devices can be represented by adding anode and

cathode segments. A planar representation of the equivalent circuit in figure 4.9 is shown in figure 4.10.

Figure 4.10: Planar multi-finger equivalent circuit for a 2-anode 2-cathode finger device

The equivalent circuit representation shown in figure 4.10 can be redrawn to emphasize the symmetry of devices, which have an equal amount of anode and cathode fingers, by collecting anode and cathode branches together. Figure 4.11 shows this form for a general N anode and M cathode structure. Mutual couplings are not illustrated in 4.11 for simplicity.

Figure 4.11: Multi-finger equivalent circuit for an $N+M$ finger device (mutual couplings not shown)

The capacitance that is in series with the cathode inductors in figure 4.11 is a parallel equivalent value. The number of parallel capacitances depends on the number of anodes; hence the capacitance associated with one anode is shown multiplied by N .

In a multi-finger varactor, as shown in figure 4.11, the current flows from the anode fingers to the cathode fingers through the capacitors, and vice-versa, therefore all fingers are part of a common loop. The current flow relationship between fingers, and hence inductors, in such a structure depends on the topology, i.e. odd or even number of fingers, and mutual coupling between the fingers. In order to understand the current flow relationships and hence the implications of mutual inductance localization, the network is first analyzed with the assumption that there is no mutual coupling. Hence a hypothetical situation is created where the fingers are magnetically isolated from one another. Under this assumption the current flowing through each anode finger would be equal, as would the current flowing through each cathode finger. This applies regardless of the chosen topology. However, under the same magnetic isolation assumption, the finger topology, i.e. $M=N$ or $N \neq M$, will determine whether the current flowing through

the cathode inductors and that flowing through the anode inductors are equal. The following analysis demonstrates the relationship between both currents if an even number of fingers, $M=N$, is assumed and if the coupling terms are ignored. Under such conditions, the current flowing through the anode inductors is given by

$$\overline{I_{LA}} = \frac{\overline{V}}{j\omega \cdot Ls + \frac{1}{j\omega \cdot \left(\frac{Cac(Vd)}{2}\right)}} \quad (4.5)$$

where $\overline{V}$ is the voltage applied to the anode. This relationship applies regardless of the number of anodes. The current flowing through the individual cathode inductors for the same topology is given by

$$\overline{I_{LC}} = \frac{\overline{V}}{j\omega \cdot \frac{Ls}{M} + \frac{1}{j\omega \cdot \left(\frac{Cac(Vd)}{2} \cdot N\right)}} \cdot \frac{1}{N} = \frac{\overline{V}}{j\omega \cdot Ls + \frac{1}{j\omega \cdot \left(\frac{Cac(Vd)}{2}\right)}} = \overline{I_{LA}} \quad (4.6)$$

Thus, the current flowing through all the inductors in such a situation will be equal. However, this only applies to varactors that have the same number of anodes as cathodes. For varactors where $N \neq M$ the current flowing through the anode inductors is given by (4.5) and that flowing through the cathode inductors is given by

$$\overline{I_{LC}} = \frac{\overline{V}}{j\omega \cdot \frac{Ls}{M} + \frac{1}{j\omega \cdot \left(\frac{Cac(Vd)}{2} \cdot N\right)}} \cdot \frac{1}{M} = \frac{\overline{V}}{j\omega \cdot Ls + \frac{1}{j\omega \cdot \left(\frac{Cac(Vd)}{2}\right) \cdot \left(\frac{M}{N}\right)}} \quad (4.7)$$

which clearly shows that for devices with an odd number of fingers the currents will differ. However, considering that a typical device with an odd number of fingers will

always have one more cathode than anode, i.e. $M=N+1$, the difference between the currents will decrease as the number of fingers is increased. The factor is therefore $\frac{N+1}{N}$ which has a maximum value of 1.5 at $N=2$ and is down to 1.2 at $N=5$. The expression, (4.7), also shows that if the number of anode fingers is the same as the number of cathode fingers all inductor currents will be equal as previously demonstrated with (4.6).

In addition to inequality of anode and cathode currents due to the inherent structure for $M \neq N$, mutual inductance also contributes to asymmetry of individual finger currents because the effect on a finger depends on its position in the structure (applies to $M=N$ and $M \neq N$). The only equality in either structure is between anode fingers placed symmetrically or cathode fingers placed symmetrically, not between finger pairs of asymmetrically placed fingers or between anode and cathode fingers, even for anode and cathode fingers symmetrically placed with respect to one another (for $N=M$), however this last condition is a result of the combined effect of mutual inductance and the different connection pattern for anode fingers and cathode fingers. The only exception to these conditions is the case of a single anode finger and single cathode finger, where the currents are equal because the structure has $N=M$ and there is only one mutual inductance and the connection pattern is the same. The two-finger case is a very simple even finger configuration that does not have asymmetric finger pairs, which complicate the current distribution.

Fingers which are asymmetrically spaced about the axis of symmetry have differing total mutual inductance therefore the current flowing through each finger in the asymmetric pair is different. This is readily seen through the following relationship for an example system consisting 4-parallel inductors with mutual coupling.

$$[\bar{V}] = [j\omega] \cdot \begin{bmatrix} Ls & M_{2,1} & M_{3,1} & M_{4,1} \\ M_{1,2} & Ls & M_{3,2} & M_{4,2} \\ M_{2,3} & M_{1,3} & Ls & M_{4,3} \\ M_{1,4} & M_{2,4} & M_{3,4} & Ls \end{bmatrix} \cdot \begin{bmatrix} \bar{I}_1 \\ \bar{I}_2 \\ \bar{I}_3 \\ \bar{I}_4 \end{bmatrix} \quad (4.8)$$

Given that the voltage, $\bar{V}$, must be equal for all parallel inductors and that the self-inductances are equal, the two middle inductors (row 2 and 3) will have the same amount of current flowing through them. This is also the case for the two outer inductors (row 1 and 4) since their impedances are also the same. However the impedance of the outer inductors will be different from the inner inductors, i.e. asymmetrical pairs, therefore their currents will differ. It is also clear from the expression that the total mutual inductance for fingers on one side of the axis of symmetry will be different.

To provide a quantitative example of the error involved in localizing mutual inductances the equivalent inductance of a system consisting of N parallel inductors with mutual coupling is compared to that of a system of N parallel inductors where the mutual coupling has been localized to victim fingers. The circuits in figure 4.12 represent two such systems. The self-inductances and mutual inductances are computed from the geometry of parallel conductors of rectangular cross-section using equations (3.3) and (3.4). The conductors were specified to be $1 \mu\text{m}$ thick, $1.4 \mu\text{m}$ wide and $24 \mu\text{m}$ long corresponding to reasonable values for an integrated varactor. The separation distance between the conductors was chosen to be $2 \mu\text{m}$.

Figure 4.12: System of parallel inductors

A circuit simulation using ADS of both networks was performed with the number of inductors varied from 2 to 14. The equivalent inductance of both circuits was computed for every combination. The percentage error between the equivalent inductances has been plotted versus the number of fingers in figure 4.13.

Figure 4.13: Percentage error between equivalent inductances vs the number of inductors

The error caused by the localization is 0% with two inductors and increases as the number of inductors increases. However, the error plateaus at approximately 2.3% for more than 10 to 12 inductors. If allowed to continue, the error would have started to decrease, converging towards 0%. Mutual coupling between conductors is effective, i.e. important, over a limited number of conductor spacings. Initially the error increases from 0 since all conductors see different combinations of conductors within their coupling range. As the number grows most inductors start to see the same amount of mutual coupling because their surroundings become very similar. Thus, the total mutual inductance affecting each inductor and hence the current carried by most inductors becomes very similar. The exception would be the edge inductors, but as the number of fingers gets very large the influence of the edges diminishes to the point where the impact on the overall system is not noticeable. Therefore, the error involved in the localization

of mutual inductances is small and is bounded. The error starts off at 0%, eventually plateaus and subsequently decreases to asymptotically approach 0%.

The localization error shown in figure 4.13 is that of a purely inductive system and is the result of differences in current flowing through each inductor. The differences in current are caused by the mutual coupling between inductors. Therefore in this instance the error was due to the mutual coupling affecting the current distribution in the inductors.

A qualitative representation for the mechanics of current flow in a multi-finger structure has been developed. It has been shown that there will be differences in current flowing through each finger regardless of the chosen topology. The localization procedure will therefore introduce an error in the equivalent network due to the current differences. However, for a general inductor case the error is well bounded. Mutual coupling and the finger arrangements are the cause of current inequality in both odd and even finger structures. In order to quantify the error for a varactor diode structure the localization procedure will be demonstrated and a localized equivalent circuit will be developed. Simulations of the localized equivalent circuit will then be compared to the coupled equivalent circuit in figure 4.11.

The localization of the mutual inductances to victim fingers can be done as follows. In a system of K parallel conductors, with a constant or uniform separation, there are $K-1$ unique mutual coupling terms. Assuming that the GMD can be approximated by the distance between the centers of two conductors [20] the unique geometric mean distances can be found by

$$GMD(unit) = (w + s) \cdot unit \quad (4.9)$$

where $w + s$ is the unit GMD and each mutual inductance is found from a multiple of the unit GMD. The mutual inductance terms are computed using (3.4). For example, a 2-anode finger and 2-cathode finger device will have three unique mutual inductances, one for each unit of separation. The following outlines the equivalency between the mutual inductance stated on a unit separation basis and the standard nomenclature in the context of this device example.

$$M_1 = M_{1,2} = M_{2,3} = M_{3,4} \quad (4.10)$$

$$M_2 = M_{1,3} = M_{2,4} \quad (4.11)$$

$$M_3 = M_{1,4} \quad (4.12)$$

The device in question would have coupling terms for two conductors side by side, two conductors with two separations between them and finally two conductors with three separation distances between them.

Once all the mutual inductances have been localized, each finger will have $K-1$ mutual terms placed in series with the inherent finger self-inductance. The total mutual inductance localized to finger j is given by

$$M(j) = \sum_{i=1, i \neq j}^K M_{|i-j|} \quad (4.13)$$

where M_k is the mutual inductance for $kGMD$ center spacing. As an example, the mutual inductance localized to the second finger of a four-finger device would consist of two M_1 terms, i.e. $M_{1,2}$ and $M_{3,2}$, along with one M_2 term, i.e. $M_{4,2}$.

The mutually coupled equivalent circuit shown in figure 4.11 becomes as shown in figure 4.14 when the mutual inductances are localized to victim fingers.

Figure 4.14: Multi-finger equivalent circuit with localized mutual inductances.

The validity of the localized equivalent circuit is an important step in the development of the compact model and is therefore verified by comparing it to the coupled multi-finger equivalent circuit; hence, the full physical model shown in figure 4.11. Three test cases are used to compare both models. The first is a device with 5-anode fingers and 5-cathode fingers; the second is a device with 2-anode fingers and 2-cathode fingers and the third is a device with 1-anode finger and 2-cathode fingers. A coupled and localized equivalent circuit was constructed for each test case. The relevant dimensions of the structures along with the model parameters are outlined in table 4.1, table 4.2 and table 4.3.

	Coupling coefficients	Localized total mutual inductance per finger
<u>Dimensions:</u>	K1=0.54	M(1)=51.72 pH
	K2=0.39	M(2)=61.02 pH
L = 30 μm	K3=0.30	M(3)=66.44 pH
W = 1.4 μm	K4=0.25	M(4)=69.60 pH
Separation = 1.8 μm	K5=0.21	M(5)=71.07 pH
Metal Thickness = 1 μm	K6=0.18	M(6)=71.07 pH
	K7=0.16	M(7)=69.60 pH
<u>Parameters:</u>	K8=0.14	M(8)=66.44 pH
	K9=0.13	M(9)=61.09 pH
Ls = 22.47 pH		M(10)=51.72 pH
Cac(0V) = 40 fF		

Table 4.1: 5-anode fingers and 5-cathode fingers with alternating structure

	Coupling coefficients	Localized total mutual inductance per finger
<u>Dimensions:</u>		
	K1=0.61	M(1)=76.69 pH
L = 60 μm	K2=0.46	M(2)=88.67 pH
W = 1.4 μm	K3=0.38	M(3)=88.67 pH
Separation = 1.8 μm		M(4)=76.69 pH
Metal Thickness = 1 μm		
<u>Parameters:</u>		
Ls = 53.00 pH		
Cac(0V) = 40 fF		

Table 4.2: 2-anode fingers and 2-cathode fingers with alternating structure

	Coupling coefficients	Localized total mutual inductance per finger
<u>Dimensions:</u>		
	K1=0.54	M(1)=20.85 pH
L = 30 μm	K2=0.39	M(2)=24.42 pH
W = 1.4 μm		M(3)=20.85 pH
Separation = 1.8 μm		
Metal Thickness = 1 μm		
<u>Parameters:</u>		
Ls = 22.43 pH		
Cac(0V) = 80 fF		

Table 4.3: 1-anode finger and 2-cathode fingers with alternating structure

The simulation results for both equivalent circuits can be seen in figure 4.15, 4.16 and figure 4.17. The generated Y-parameters from both equivalent circuits have been converted into an effective capacitance using (3.11). The two equivalent circuit predictions are in virtual agreement; the maximum percentage error between the coupled multi-finger model and localized multifinger version is approximately 0.4% for the ten-finger device, 0.2% for the four-finger device and 0.9% for the three-finger device. The maximum error for each test case occurs at 40 GHz.

Figure 4.15: Result for the ten-finger device. (Dotted line is localized model)

Figure 4.16: Result for the four-finger test case. (Dotted line is localized model)

Figure 4.17: Result for the three-finger test case. (Dotted line is localized model)

In all three test cases, the percentage error between the coupled equivalent circuit, figure 4.11, and the localized version, figure 4.14, is very small. The largest error occurs for the device with an odd number of fingers. The unequal current flowing through the anode finger and cathode fingers causes the error. As previously explained, the error incurred in structures with an odd number of fingers will diminish as the number of fingers increases. The errors for all the devices are reasonably small therefore the localized equivalent circuit has been shown to be equivalent to the explicitly coupled representation within a very reasonable error bound. It is also clear from the simulation results that the resulting perturbation in the localized equivalent circuit due to the localization of the mutual inductances is reduced significantly from the standpoint of a purely inductive system. Errors in equivalent inductance, i.e. figure 4.13, do not translate proportionately to errors in effective capacitance at frequencies reasonably far from resonance because the capacitive reactance damps out small changes in inductive reactance. However, this does not diminish the importance of inductance because a large error in equivalent inductance may lead to a significant error in the model prediction.

Further reduction of the localized equivalent circuit shown in figure 4.14 can be achieved by finding the parallel equivalent of the cathode inductors found inside the dashed box of figure 4.14. The corresponding capacitors can also be reduced via a parallel equivalent.

The cathode inductors are explicitly in parallel with one another therefore a parallel equivalent can be found without error. The same is true for the corresponding capacitors when losses are neglected. The total admittance of the cathode branches is therefore given by

$$Y_c = \frac{j\omega N \frac{C_{ac}(V_d)}{2}}{1 - \omega^2 N \frac{C_{ac}(V_d)}{2} \cdot \left(\sum_j \frac{1}{L_s + M(j)} \right)^{-1}} \quad (4.14)$$

where the resulting equivalent capacitance is simply the sum of N individual capacitances where N defines the number of anodes and the resulting cathode inductance is the parallel equivalent of the cathode inductances. The summation of the parallel inductances is defined by the range variable j , which serves to identify the cathode fingers. For example, in a system of K fingers where the even numbered fingers are the cathode j is defined by $j = 2, 4 \dots K$. The localized equivalent circuit with reduced cathode is shown in figure 4.18.

Figure 4.18: Localized equivalent circuit with reduced cathode

The resulting network is composed of LC branches, which are in parallel with each other. There is only one inductor representing the cathode inductances and one corresponding capacitor. However, there are still N anode branches. Therefore the localized equivalent circuit with reduced cathode can still be quite large depending on the number of anode fingers. Further simplification is required to obtain a compact model, which has a fixed number of lumped components and internal nodes regardless of the number of fingers in the structure. To this end the anode branches must be reduced. An equivalent representation for the anode branches will now be presented which permits a compact equivalent circuit to be derived.

The anode branches are each composed of a series capacitor and inductor where all the capacitors are of equal value, but the inductors can differ from one another. Parallel LC branches which have the same capacitance and inductance, as shown in figure 4.19 (a), can be reduced to a single LC branch, as shown in figure 4.19 (b), where the equivalent capacitance is the parallel equivalent of the capacitors and the equivalent inductance is the parallel equivalent of the inductances.

Figure 4.19: Parallel to series conversion example

The admittance of each parallel branch in figure 4.19(a) is given by

$$Y_{branch} = \left(\frac{1}{j\omega \cdot C} + j\omega L \right)^{-1} = \frac{j\omega C}{1 - \omega^2 \cdot L \cdot C} \quad (4.15)$$

The total admittance of the network in figure 4.19(a) is thus given by

$$Y_a = Y_{branch} \cdot n = \frac{j\omega(nC)}{1 - \omega^2 \cdot LC} = \frac{j\omega(nC)}{1 - \omega^2 \cdot \frac{L}{n}(nC)} \quad (4.16)$$

whereas the admittance of the equivalent network is given by

$$Y_{equivalent} = \frac{j\omega C_{eff}}{1 - \omega^2 \cdot L_{eff} \cdot C_{eff}} \quad (4.17)$$

The two networks are equivalent when $C_{eff} = nC$ and $L_{eff} = L/n$. Thus, a circuit consisting of parallel LC branches where all capacitors are of equal value and all inductors are of equal value can be reduced to a single series LC whereby the equivalent capacitance and inductance are the parallel equivalent of the individual components. However, if the values for the components in the parallel branches are not equal, the series LC circuit computed using this method would not be equivalent to the parallel representation.

This is the case for the anode fingers in the localized equivalent circuit because of the difference between the localized inductances. The magnitude of the error depends on the value of capacitance, the common inductance value between fingers and the difference between the inductor values, i.e. the ΔL between inductors. The error involved in defining a series equivalent LC network for the anode fingers, where the series inductance is the parallel equivalent of the anode inductors and the series equivalent capacitance is the parallel equivalent of the corresponding capacitors, is explored via a comparison of the localized equivalent circuit with reduced anode and cathode, shown in figure 4.20, to the localized equivalent circuit, i.e. figure 4.14.

Figure 4.20: Localized equivalent circuit with lumped cathode and lumped anode.

The admittance of the lumped anode, lumped cathode equivalent circuit is given by

$$Y_{lumped_localized} = Y_c + \frac{j\omega N \frac{C_{ac}(V_d)}{2}}{1 - \omega^2 N \frac{C_{ac}(V_d)}{2} \cdot \left(\sum_k \frac{1}{L_s + M(j)} \right)^{-1}} \quad (4.18)$$

where k identifies the positions of the anodes within the structure. For example, $k=1,3\dots K-1$, where K is the total number of fingers, will be the anode finger identifiers for a varactor diode in which the first finger is an anode and in which the number of anode fingers equal the number of cathode fingers. The summation of the capacitors in (4.18) depends on the total number of anodes, which is identified by the variable N . The

admittance of the localized equivalent circuit, figure 4.14, for the purpose of comparison, is given by

$$Y_{localized} = Y_c + \sum_k \frac{j \cdot \omega \cdot \left(\frac{C_{ac}(V_d)}{2} \right)}{1 - \omega^2 \cdot \left(\frac{C_{ac}(V_d)}{2} \right) \cdot (L_s + M(k))} \quad (4.19)$$

In order to show that the difference between both admittances is insignificant, hence that the lumped-anode lumped-cathode equivalent circuit model is equivalent to figure 4.14, the magnitude of (4.18) and (4.19) were compared for a wide range of practical varactor diode structures by computing the percentage error between the magnitude of (4.18) and (4.19) as a function of the number of fingers within the varactor diode and the finger length. The Y parameters were computed for every pair of finger length and number of fingers. The width and thickness of the fingers and the spacing between them were kept constant. These values were based on the minimum values allowed by STMicroelectronics in their SiGe2 process. The width and separation distance were set to reasonably small values because losses are minimized with them at a minimum. The width of the fingers was specified to be $1.4 \mu\text{m}$ while the separation distance between fingers was set to $1.8 \mu\text{m}$. The conductor thickness was set to $1 \mu\text{m}$. The other assumption made in this comparison was that the zero bias depletion width for the anode to cathode junction is $0.085 \mu\text{m}$. On a per finger basis, this translates to a zero bias capacitance per finger length of $1.721 \frac{\text{fF}}{\mu\text{m}}$. The percentage difference in the admittance magnitudes (at 40 GHz) between the lumped anode, lumped cathode equivalent circuit, i.e. figure 4.20 or (4.18) and the localized equivalent circuit, i.e. figure 4.14 or (4.19), in terms of finger length and number of fingers is shown in figure 4.21.

Figure 4.21: Percentage error in the admittance magnitude given by (4.18) and (4.19)

The error is larger for devices that have many fingers in conjunction with long finger lengths. This is simply because those devices are close to resonance at 40GHz and the very steep slope in the near resonance region makes for a larger error. Simulations of this same structure beyond 40GHz show a rapid increase in error followed by a very rapid decrease confirming the proximity of the self-resonant frequency. Also, a simple computation of the self-resonant frequency for a device with 80 fingers where each finger is 40um long results in 48 GHz. This is very close to the frequency used in generating figure 4.21 further demonstrating that resonance is a very plausible cause for the error observed in devices with relative large dimensions. If not for the effect of resonance the error would be smaller for larger devices because the localization error is attenuated with the presence of many fingers. In general, the lumped anode, lumped cathode equivalent circuit has a very good percentage error considering the increase shown in the figure is

due to the proximity of resonance. Thus, reducing the localized equivalent circuit, figure 4.14, down to only two parallel LC branches does not introduce any significant error.

The lumped anode, lumped cathode localized equivalent circuit, shown in figure 4.20, can be reduced even further, to a single series LC branch, by applying the same basic method. The parallel equivalent of all the inductors and the parallel equivalent of all the capacitors are placed in series to achieve the compact equivalent circuit. The admittance of the compact equivalent circuit is given by

$$Y_{compact} = \frac{j\omega N \frac{C_{ac}(V_d)}{2}}{1 - \omega^2 N \frac{C_{ac}(V_d)}{2} \cdot \left(\sum_{j=1}^K \frac{1}{L_s + M(j)} \right)^{-1}} \quad (4.20)$$

where N is the number of anode fingers and K is the total number of fingers. The percentage difference between the magnitude of the compact circuit admittance, i.e. (4.20), and the admittance of the localized equivalent circuit, shown in figure 4.15, is shown in figure 4.22 (a) and again in 4.22 (b) where the number of fingers has been restricted to a maximum of 10.

Figure 4.22: Percentage difference between admittance magnitudes given by (4.19) and (4.20)

The percentage difference between the compact model and the localized equivalent circuit, i.e. figure 4.14, is similar to that obtained between the quasi-compact model, figure 4.20, and the localized equivalent circuit except that there is a larger error for odd finger combinations at low finger counts in figure 4.22. From figure 4.22 (b) it is clear that odd finger combinations generate a much larger error than even finger combinations. The error decreases as the number of fingers increases to eventually converge to what had been obtained with the quasi-compact model. The large error at odd finger combinations is caused by the addition of inductance in the cathode for odd fingered structures. Every time a cathode finger is added there is one more inductor in the cathode than there is in the anode. Since the cathode inductors are in parallel the result of the cathode equivalent network can be significantly different from that of the anode. Thus, in computing the

compact model where a equivalent series LC branch is devised from the parallel equivalent of the equivalent anode and cathode inductances, an error is introduced due to the difference in the anode equivalent inductance and the cathode equivalent inductance. This error was not seen in the quasi-compact model comparison, shown in figure 4.21, since the anode and cathode branches were not lumped together. Although the error in the prediction made by the compact model is larger it remains within reasonable limits. The total equivalent lumped inductance is therefore given by

$$Leq = \frac{1}{\sum_{j=1}^K \frac{1}{Ls + M(j)}} \quad (4.21)$$

where K is the total number of fingers. The total equivalent inductance is divided into two as shown with (4.22) in order to split it between anode and cathode. The compact circuit is shown in figure 4.23.

$$Ls = \frac{Leq}{2} \quad (4.22)$$

Figure 4.23: Compact equivalent circuit model with only inductance and capacitance.

A compact equivalent circuit, which takes into account inductance and capacitance, has been developed for the varactor diode. The validity of the compact model is now verified via circuit simulation by comparing it to the full coupled multi-finger equivalent circuit of figure 4.11, where the mutual terms have not been localized to the fingers. Two test cases are simulated with both models. The first test case is a 4-

finger device while the second consists of a 10-finger device. Both have an alternating cathode/anode structure. The model parameters for each test case are shown in table 4.4 and table 4.5 while the results are shown in figure 4.24 and figure 4.25.

<u>Finger Dimensions:</u> L=10 μm W=1.4 μm Separation=1.8 μm Metal Thickness=1 μm	Coupling Coefficients	Inductance	Capacitance
Mutually Coupled Model	K1=0.42 K2=0.25 K3=0.18	Ls=5.39 pH	Cac(0V) =20 fF
Compact Model	N/A	Leq=2.64 pH	Cjeq(0V) =40 fF

Table 4.4: Model parameters for a four-finger device

<u>Finger Dimensions:</u> L=30 μm W=1.4 μm Separation=1.8 μm Metal Thickness=1 μm	Coupling Coefficients	Inductance	Capacitance
Mutually Coupled Model	K1=0.54 K2=0.39 K3=0.30 K4=0.25 K5=0.21 K6=0.18 K7=0.16 K8=0.14 K9=0.13	Ls=22.47 pH	Cac(0V) =600 fF
Compact Model	N/A	Leq=8.58 pH	Cjeq(0V) =3 pF

Table 4.5: Model parameters for a ten-finger device

Figure 4.24: Compact model (dotted) and coupled model (full) results for 4-finger device

Figure 4.25: Compact model (dotted) and coupled model (full) results for 10-finger device.

In both cases the compact equivalent circuit, figure 4.23, proves to be equivalent to the coupled multi-finger equivalent circuit, figure 4.11, within a reasonable error

bound. The percentage error between the resonant frequency of both models in the 10-finger case is 0.4%.

The main sources of error encountered in the development of the compact model are the inductance localization error and the error introduced in the final parallel branch reduction. The parallel branch reduction error, which depends on the existence of a localization error, was shown to be insignificant for reasonably sized devices. The error associated with localization was shown to depend on the number of fingers in the varactor. The error plateaus and then decreases after a certain number of fingers. For the varactor sizes investigated this error was found to be reasonable. Thus, a compact model, which takes into account capacitance and inductance, has been successfully developed.

The analysis has led to a methodology for calculating the required lumped inductance values based on an accurate representation of self and mutual inductances, and hence can be used to determine the model inductance parameters from physical dimensions. The methodology can be summarized as follows. The finger self-inductances and the mutual inductance between every finger pairs are computed from the physical geometry. This is followed by the localization of mutual inductances to victim fingers, which will result in each finger having $K-1$ localized mutual inductances where K defines the total number of fingers. Finally parallel equivalents are found for the total finger inductances and capacitance to create a compact model composed solely of one inductor and capacitor.

The losses found in the varactor diode will now be introduced and the compact model will be altered in consequence.

4.2.3 Resistive Losses in Varactor Diodes

There are many sources of loss in a varactor diode. Typically the main sources of resistance include the contact resistance, buried layer resistance, cathode sinker resistance and a voltage dependant resistance between the varactor implant and buried layer.

All resistances, other than the contact resistance, are computed from the resistivity and geometry of the respective regions. The precise computation of each parameter is a low frequency issue and will not be reviewed in detail. In general the buried layer resistance on a per finger basis can be computed by

$$R_{buried} = R_{sht} \cdot \left(\frac{sep + w}{l} \right) \quad (4.23)$$

where R_{sht} is the sheet resistance, l is the finger length, sep is the finger separation and w is the finger width. The sinker resistance can be computed from the area and depth by

$$R_{sinker} = \frac{\rho_{sinker} d}{wl} \quad (4.24)$$

where w , l and d are the width, length and depth of the sinker and ρ_{sinker} is the sinker resistivity. The well resistance can be computed in the same fashion as the sinker resistance; however, some of the geometrical parameters have a voltage dependency in this case. As the depletion region extends towards the buried layer this resistance will diminish because the length of the n-well segment between the varactor implant and buried layer will diminish. The following can be used to compute the well resistance

$$R_{well} = \frac{\rho_n d(Vd)}{wl} \quad (4.25)$$

where w and l are the width and length of the varactor implant, ρ_n is the resistivity of the n-well and $d(Vd)$ is the voltage dependant distance between the varactor implant and n+ epitaxial layer. The contact resistance, unlike the other losses, is a surface boundary resistance, which is not well defined analytically.

The contribution of each lossy source in the varactor diode is not equally weighted. The sinker and buried layer losses will be insignificant compared to the

variable well resistance in reasonably laid out structures because of the different doping concentrations. It is not unusual for the well to be two orders of magnitude lower in dopant concentration than the buried layer and sinker implant. The multi-finger equivalent circuit with localized mutual inductance and losses is shown in figure 4.26. The buried layer resistances and sinker resistances have been ignored for the reasons mentioned above. The inductance and resistance contained within the dashed box is associated with the cathode fingers. The capacitances and losses in series with the components in the dashed box are associated with the anode and therefore depend on the number of anode fingers not cathode fingers.

Figure 4.26: Equivalent circuit with localized mutual inductance and losses

The contact resistance can also be made negligible with proper layout of the contacts. The use of many parallel contacts or one big slot contact per finger can achieve this result. For this reason the contact resistances are deemed negligible for the purpose of this thesis. The multi-finger equivalent circuit with resistance is therefore reduced to that shown in figure 4.27.

Figure 4.27: Localized mutual inductance circuit without contact resistance

The reduction of the localized multi-finger equivalent circuit, i.e. figure 4.27, to the compact form when losses are considered is done as shown in the previous section. The parallel equivalent of the inductances and capacitances are used to create the compact model. The equivalent resistance is computed in the same manner. Since, the resistances are of equal value, their addition to the system does not introduce an error in the compact model as a result of there being differences in resistance values. At worst, the error (between compact model and localized model) will converge to that obtained for the compact LC (only) model when compared to the lossy multi-finger equivalent circuit with localized mutual inductance. This occurs when the resistance is much smaller than the inductive reactance. On the other hand, the percentage error between the predicted admittances will diminish when the resistance is larger or similar in magnitude to that of the reactance, because the resistances will tend to stabilize the impedance values and thus the percentage difference between branch impedances will diminish.

The percentage difference between the admittance magnitude predicted by the lossy multi-finger model with localized mutual inductance, figure 4.27, and the lossy compact model are shown in figure 4.28 and figure 4.29 for two cases. In the first case, the well resistivity is $9.3 \cdot 10^{-4} \Omega \cdot \text{cm}$ and the distance between varactor implant and buried layer at zero volts is $0.1 \mu\text{m}$ while in the second case the distance between regions

is increased to $0.9 \mu\text{m}$. The first case represents a low resistance condition while the second case represents a high resistance condition.

Figure 4.28: Percentage error in predicted admittance magnitude for low resistance

Figure 4.29: Percentage error in predicted admittance magnitude for high resistance

In the first case, the compact model is largely unaffected by the addition of resistance in terms of percentage error between the admittance generated by both models. Therefore the result is very similar to that obtained for the lossless compact circuit shown in figure 4.22(a). However, the overall error is considerably lower in the high resistance case. Even at the longest finger length the resistance, in this instance, is significant enough, compared to the inductive reactance at 40GHz, to reduce the effective error. Although the error can be significantly lower with the addition of resistance to the model, varactor diodes with high resistance values are not desired due to their poor performance. Hence, the error in the parallel reduction when resistance is considered will at worst converge to the error of the equivalent LC system for most practical varactor diodes. The equivalent resistance for the compact model is computed as follows

$$Req(Vd) = \frac{1}{\sum_{i=1}^K \frac{1}{2 \cdot Rwell(Vd)}} \quad (4.26)$$

where K is the total number of fingers in the varactor diode. The compact equivalent circuit with resistance is shown in figure 4.30.

Figure 4.30: Compact equivalent circuit with inductance, capacitance and resistive losses

4.2.4 Buried Layer Depletion capacitance

The buried layer depletion capacitance or substrate depletion capacitance is formed between the n^+ buried layer and the p-type substrate. In this work, this capacitance is described by

$$C_{sj0} = \hat{C}_{cs0} \cdot Ab \quad (4.27)$$

where Ab is the buried layer area and $\hat{C}_{cs0}$ is the buried layer capacitance on a per unit area basis. The capacitance is effectively normalized to the buried layer area. The voltage dependency of this depletion capacitance is well generally well described by (4.2) because of the monotonic nature of the substrate doping profile. The built-in potential and grading factor can be optimized specifically for the buried layer/substrate junction. The compact equivalent circuit model with buried layer capacitance is shown in figure 4.31.

Figure 4.31: Compact equivalent circuit with LCR and buried/substrate capacitance

4.2.5 Substrate Effects

The silicon substrate behaves as explained in chapter 3. Therefore the compact model developed for the varactor will model the substrate in the same fashion. Essentially a substrate capacitance is used to model the dielectric nature of the substrate and a resistance is used to model the losses within the bulk silicon. The two parameters are optimized from measured data using the same method that was used for the MIM capacitors. The method is described in section 3.2.5. The scaling issues affecting the substrate network for the MIM capacitor also affect the varactor diode. The complete compact model, with substrate network, is shown in figure 4.5.

4.3 Theoretical Verification

A coupled multi-finger model for describing varactor diode operation has been developed. From the coupled model, a compact version was proposed with the purpose of achieving better computational efficiency while at the same time providing a similar degree of modeling accuracy. The validity of the compact model in terms of its equivalency to the coupled version will now be verified via simulations of various hypothetical varactor structures. The compact model shown in figure 4.5 will be compared to the coupled multi-finger version shown in figure 4.32.

Figure 4.32: Full coupled multi-finger equivalent circuit (coupling not shown for simplicity)

The models are compared via an s-parameter simulation from 100MHz to 40GHz. All generated S -parameters from the models are compared. The setup and port arrangements are shown in figure 4.33.

Figure 4.33: Simulation setup for L2 models

The first hypothetical structure to be compared is a 2-finger varactor, i.e. one anode and one cathode finger. The length of each finger is $20\text{ }\mu\text{m}$ and their width is $2\text{ }\mu\text{m}$. The finger thickness is $1\text{ }\mu\text{m}$. The separation between nearest neighbors is $2\text{ }\mu\text{m}$. The parameters for both models are listed in table 4.6.

Multi-finger Model						
K	Ls	Cac0	Ccs0	Rwell	Rs	Cs
K1=0.48	12.54 pH	36.68 fF	35.64 fF	4.65 Ω	700 Ω	6 fF

Compact L2 Model						
Ls	Cj0	Csj0	Req	Rs	Cs	
4.63 pH	36.68 fF	35.64 fF	4.65 Ω	700 Ω	6 fF	

Table 4.6: Model parameters for a 2-finger device

The S -parameters generated from both models are plotted in figure 4.34. In this instance, there is virtually no difference between the S -parameters generated from either model. An extraction of the anode to cathode depletion capacitance via (3.11) indicates a percentage error of 0.01% at 40GHz between both model predictions.

Figure 4.34: S -parameters for the 2-finger test case. (Dashed lines represent imaginary numbers)

The second hypothetical structure to be compared is a 4-finger varactor, i.e. two anode and two cathode fingers. The length of each finger is $30\text{ }\mu\text{m}$ and their width is $1.4\text{ }\mu\text{m}$. The finger thickness is the same as in the previous case. The separation between nearest neighbors is $1.8\text{ }\mu\text{m}$. The fingers alternate between anode and cathode with one anode and cathode at the outer edges. The parameters for both models are listed in table 4.7 and the results can be found in figure 4.35.

Multi-finger Model						
K	Ls	Cac0	Ccs0	Rwell	Rs	Cs
K1=0.54 K2=0.39 K3=0.30						
	22.48pH	38.51 fF	55.49fF	4.43 Ω	600 Ω	9 fF

Compact L2 Model					
Ls	Cj0	Csj0	Req	Rs	Cs
6.58 pH	77.03 fF	55.49fF	2.22 Ω	600 Ω	9 fF

Table 4.7: L2 model parameters for a 4-finger device

Figure 4.35: S-parameters for the 4-finger device. (Dashed lines represent imaginary numbers)

As was the case with the 2-finger device, very good agreement is found between both models. The error in effective capacitance between the compact and coupled models at 40GHz is on the order of 0.05%.

The third hypothetical structure to be compared is a 6-finger varactor, i.e. three anode and three cathode fingers. The dimensions and arrangements are exactly the same as the 4-finger device. The parameters for both models are listed in table 4.8 and the results can be found in figure 4.36.

Multi-finger Model						
K	Ls	Cac0	Ccs0	Rwell	Rs	Cs
K1=0.54						
K2=0.39						
K3=0.30	22.48pH	38.51 fF	83.23 fF	4.43 Ω	550 Ω	13.5 fF
K4=0.25						
K5=0.21						

Compact L2 Model					
Ls	Cj0	Csj0	Req	Rs	Cs
5.50 pH	115.54 fF	83.23 fF	1.48 Ω	550 Ω	13.5 fF

Table 4.8: L2 Model parameters for 6-finger device

Figure 4.36: S-parameters for 6-finger device. (Dashed lines represent imaginary numbers)

In this case the percentage difference at 40GHz is approximately 0.1%.

The fourth hypothetical structure to be compared is an 8-finger varactor, i.e. four anode and four cathode fingers. The dimensions are as follows; the finger length is 40 μm , the width is 2 μm and the separation is 2.5 μm . The same anode/cathode alternating structure is used for this device. The parameters for both models are listed in table 4.9 and the results can be found in figure 4.37.

Complex L2 Model						
K	Ls	Cac0	Ccs0	Rwell	Rs	Cs
K1=0.52						
K2=0.37						
K3=0.29						
K4=0.24	30.42 pH	73.4 fF	153.1 fF	2.33 Ω	500 Ω	25 fF
K5=0.2						
K6=0.17						
K7=0.15						

Compact L2 Model					
Ls	Cj0	Csj0	Req	Rs	Cs
6.29 pH	293.44 fF	153.09 fF	0.58 Ω	500 Ω	25 fF

Table 4.9: L2 Model parameters for 8-finger device

Figure 4.37: S-parameters for 8-finger device. (Dashed lines represent imaginary numbers)

The eight-finger device simulation also shows good agreement between both models. The error between the effective capacitance at 40GHz is approximately 0.75%.

All test cases presented up to this point consist of devices with an even number of fingers. The final test case is a device with 5 fingers. There are 2-anode fingers and 3-cathode fingers. The two outer fingers are part of the cathode and the fingers alternate between anode and cathode. The finger width and length are $2.5 \mu\text{m}$ and $50\mu\text{m}$ respectively. The metal thickness is $2.5 \mu\text{m}$ and the separation distance between fingers is $1 \mu\text{m}$. The parameters for the two models are outlined in table 4.10.

Multi-finger Model						
K	Ls	Cac0	Csj0/2	Rwell	Rs	Cs
K1=0.67 K2=0.50 K3=0.40 K4=0.34	36.27pH	500 fF	50 fF	7 Ω	575 Ω	35 fF

Compact L2 Model					
Ls	Cj0	Csj0	Req	Rs	Cs
11.27 pH	1000 fF	100 fF	1.75 Ω	575 Ω	35 fF

Table 4.10: L2 Model parameter for 5-finger device

The capacitance for this test case was made large in order to verify the model behavior for structure with high capacitance. The s-parameter results for this test case are shown in figure 4.38.

Figure 4.38: S -parameters for 5-finger device. (Dashed lines represent imaginary numbers)

An extraction of the effective capacitance using (3.11) shows that this test case varactor resonates. The effective capacitance predicted by both models is shown in figure 4.39 and the predictions clearly show resonance.

Figure 4.39: C_{eff} for 5-finger test case. (Dotted line is compact model prediction)

The percentage difference between the predicted resonant frequencies is approximately 0.9% therefore demonstrating that the compact model is valid for odd finger combinations.

All theoretical test cases show very good agreement between the coupled multi-finger model prediction, i.e. figure 4.35, and the compact model prediction, i.e. figure 4.5. Thus, the equivalency of the compact model to that of the coupled multi-finger varactor representation has been verified. In the following section, the compact model will be applied to actual varactor diode measurements.

4.4 Experimental Verification

Three varactor diode structures have been fabricated using STMicroelectronics SiGe2 process in order to provide some experimental comparison for the compact varactor diode model. *S*-parameter measurements were performed on each device. Measurements were taken up to 40GHz, which was the frequency limit of the test equipment. The DC behavior of the devices was also characterized with a DC bias sweep ranging from 0.4V to -8V. The DC bias was applied to the cathode while the anode was grounded.

4.4.1 The SiGe2 varactor diode

The varactor diodes are formed using the standard NPN BJT mask steps. One main modification is made in the base implant. The modification is made in order to create a custom n-type doping profile appropriate for varactor diode operation. The diode looks roughly as shown in figure 4.1. The p^+ type material under the anode contact is formed through diffusion from the p^+ polysilicon deposited to contact the silicon. The anode/cathode depletion region is formed between the diffused p^+ silicon and the n-type varactor implant. Not shown in figure 4.1 are trenches, which are used to isolate the varactor diode from surrounding devices.

4.4.2 Sample devices

The sample devices consist of a 4-finger, 20-finger and 32-finger device. Each device has an equal amount of anode and cathode fingers. The outer edge fingers consist of one anode and one cathode finger. The fingers alternate from anode to cathode. The relevant physical specifications for each device are given in table 4.11.

	4-Finger	20-Finger	32-Finger
Number of anodes	2	10	16
Number of cathodes	2	10	16
Finger length in metal (μm)	12	22	22
Finger width in metal (μm)	1.4	1.4	1.4
Finger separation from closest metal edges (μm)	1.8	1.8	1.8
Varactor implant width (μm)	1.6	1.6	1.6
Varactor implant length (μm)	10	20	20
Buried layer width (μm)	13.7	64.9	103.3
Buried layer length (μm)	13.4	23.4	23.4
Finger (Metal) thickness (μm)	1.02	1.02	1.02

Table 4.11: Physical specifications for the sample devices.

4.4.3 Measurement Setup

The measurements were performed with a setup as shown in figure 4.40.

Figure 4.40: Varactor diode measurement setup

The varactor diode measurements were performed on-wafer therefore the equipment used to generate and measure the voltage waveforms is the same that was used to measure the

MIM capacitors. The reader is referred to chapter 3 for a complete listing. The DC bias condition was applied through the use of an HP4145B parameter analyzer.

4.4.4 Computation and Extraction of Model Parameters

The values for the parameters used in the compact model can be determined using various means. Some parameters can be computed using analytic equations presented in this thesis, but others require extraction from the measured devices. An overview of the methods used to determine the values of the compact model parameters will be presented in this section.

The anode to cathode depletion capacitance, C_j , is arguably the most important parameter in the compact model. An accurate value for C_{j0} is crucial in the models ability to predict the voltage dependant behavior of varactor diodes. In order to obtain an accurate value, C_{j0} is extracted from the devices using (3.11). Generally, the average of the values that lie below 2 to 3 GHz can be used as C_{j0} . The extraction can also be performed via (4.28), which basically assumes the network is composed of a series R and C. Results extracted with (4.28) are independent of resistance for series RLC networks. With (4.28) any frequency dependant behavior that is observed is caused by inductance.

$$C_{eff}(\omega, V_d) = \frac{|(Y_{22}(V_d))|^2}{\omega \cdot \text{Im}(Y_{22}(V_d))} \quad (4.28)$$

The low-frequency voltage-dependent behavior of $C_j(V_d)$ is predictable via (4.4). However, the built-in potential and grading factor are not easily computed analytically and a lack of information regarding doping concentration and profile for the devices in question requires that they both be determined through curve fitting. Thus, the C(V) curve of the anode to cathode depletion capacitance is fit to the measured C(V) curve of the devices. This is done at low frequency in order to isolate the depletion capacitance. The grading factor and built-in potential are tuned until a curve fit between the model and measurement is achieved.

The anode to cathode depletion capacitance in function of the applied voltage is shown at 1.7GHz in figure 4.41 for the 4-finger device. The maximum reverse bias voltage is -5.2V , which is ample enough to see the effect of the buried layer.

Figure 4.41: Buried layer limiting in 4-finger device. (Dotted line is compact model)

The measured result for the $C(V)$ curve of the 4-finger device clearly shows the effect of the buried layer. The measured capacitance characteristic is virtually flat beyond -3V . In figure 4.41 (a) the model prediction, i.e. the result obtained with (4.4), when m and V_{bi} are not specifically optimized for this voltage range does not match the measured data beyond -3V . The model predicts a larger slope than what is being shown by the device in the high voltage region. The grading factor and built-in potential were then optimized to achieve a better curve fit between the model prediction and the measurement. The optimized result for the full voltage range is shown in figure 4.41 (b). The match remains very poor. The error at high reverse bias voltages ends up being spread down in voltage in order to achieve a lower maximum error in the optimization attempt. Thus, the grading factor and built-in potential cannot be optimized to achieve a good match to this curve because of the complexity of the behavior. At high reverse bias

the depletion region is extended to the buried layer, which is a region of high doping density. As mentioned in section 4.2.1, the doping characteristic prohibits a good match with a low order polynomial expression. For the purposes of this thesis the voltage range of interest is therefore limited to -2.8V of reverse bias in order to avoid the effects of the buried layer. The anode/cathode depletion capacitance in function of the applied voltage (restricted to -2.8V) is shown in figure 4.42 for all three devices.

Figure 4.42: Anode to cathode depletion capacitance versus voltage

Very good agreement is seen between the compact model and the devices up to -2.8V . All three devices were found to have a grading factor of approximately 0.5. The built-in potentials were found to be approximately 0.9V for all three devices. The remaining model parameters will now be reviewed.

The values for the inductors, which are key at high frequency, are computed using the equations and methodology presented in section 4.3.2. The values have not been optimized in any fashion for the devices in question.

The buried layer depletion capacitance is extracted using (3.8). The voltage dependency of C_{sj} is well represented via (4.4) and the grading factor and built-in potential are curve fit to low frequency extractions of C_{sj} at various voltages. The built-in potential and grading factor were determined to be 0.7V and 0.5 respectively for all three devices. The substrate parameters were determined with the same method introduced in chapter 3 section 3.2.5, which was used for the MIM capacitor substrate

components. The resistance, R_{eq} , was extracted at 0V. The value was subsequently optimized in order to achieve a good curve fit between the quality factor predicted by the model and that measured from the devices. The analytical equation presented in section 4.2.3 is not used due to a lack of information regarding doping density and implant depths for the process in question.

4.4.5 Compact Model Parameters

The compact model parameters for all three devices are shown in table 4.12, 4.13 and 4.15 for the 4, 20 and 32 finger devices respectively.

Ls	Cj0 m=.48 vbi=.86V	Csj0 m=0.5 vbi=0.7V	Req0	Cs	Rs
1.74 pH	29.8 fF	30.2 fF	26 Ω	12 fF	2287 Ω

Table 4.12: Compact Model parameters for the 4-finger device

Ls	Cj0 m=.5 vbi=.89V	Csj0 m=0.5 vbi=0.7V	Req0	Cs	Rs
1.8 pH	291 fF	222 fF	3 Ω	33 fF	1128 Ω

Table 4.13: Compact Model parameters for the 20-finger device

Ls	Cj0 m=.5 vbi=.9V	Csj0 m=0.5 vbi=0.7V	Req0	Cs	Rs
1.3 pH	466 fF	302 fF	2.25 Ω	54 fF	689 Ω

Table 4.14: Compact Model parameters for the 32-finger device

The spice L3 diode model [37] is used to represent the depletion capacitances in the model simulations in order to allow the depletion capacitances to vary in function of the voltage. However, only the reverse bias parameters, i.e. m , V_{bi} and C_{j0} are utilized and the series resistance, R_s , is set to 0.

4.4.6 Measurement Results and Model Predictions

The validity of the model in terms of high frequency behavior is verified through comparisons of the effective anode to cathode depletion capacitance, quality factor with cathode grounded and the effective buried layer depletion capacitance. The effective buried layer depletion capacitance is compared to ensure the substrate path is modeled correctly by the compact model.

The effective capacitance for all three devices at 0V is shown in figure 4.43. Both the measurement result and model prediction are shown in the figure.

Figure 4.43: Effective capacitance comparison at 0V for all three devices

The bottom curves represent the extraction using (3.11), which assumes the network is composed of a parallel RC , and the top curves represent the extraction performed with (4.28), which assumes the network is composed of a series RC . The series extraction, (4.28), demonstrates more sensitivity to the inductance in the system (because inductance is in series with the rest of the network) and is therefore of particular interest. The measurements are slightly noisy but there is relatively good agreement between the model and measurement for the devices considering that the inductance values have not been optimized whatsoever. The wave like shape of the measurement result in 4.43(b)

does not correspond to oscillation, as this is a frequency domain measurement. At the time of this writing, no concise reason was found to explain why the model prediction for the 32-finger device was the furthest off. More measurement samples for this device may have shown the discrepancy to be measurement related. The model prediction is expected to be very good for devices with many fingers (because the errors involved in constructing the compact model decrease as the number of fingers increase) and good agreement was shown in the 20-finger device comparison.

The effective capacitance at various bias points is shown in figure 4.44 for the three devices.

Figure 4.44: Effective capacitance comparison at 0V, -0.4V, -0.8V and -1.2V.

The frequency dependant nature of the effective capacitance generated by the model is consistent with that of the measurement. However, the scaling with voltage is not perfect as is clearly seen in figure 4.44. This is the result of the combined effect of the buried layer and the varactor implant doping profile. The voltage and frequency dependencies are independent so errors related to voltage scaling have to be corrected with better voltage dependence.

The quality factors of the varactor diodes and the model predictions for the quality factor are shown in figure 4.45 at 0V for the case where the cathode is grounded.

Figure 4.45: Quality factor of devices and model with cathode at ground

All three cases show good agreement between measurement and model. The direct path from the anode to the cathode is therefore modeled correctly based on the results obtained with the effective capacitance and quality factor. However, the path shunting to the substrate has not been verified. In order to do so, the effective buried layer capacitance from the measurement is compared to that predicted by the model. The effective buried layer depletion capacitance is shown in figure 4.46 for all three devices.

Figure 4.46: Effective buried layer depletion capacitance comparison at 0V.

The model prediction for the behavior of the substrate path is reasonably good. In these devices, the buried layer depletion capacitance is much larger than the substrate depletion capacitance therefore the effective depletion capacitance quickly converges to the substrate capacitance. In addition, the substrate resistance for the test structures was quite large compared to the capacitance due to the placement of the substrate ground contacts therefore the substrate capacitance essentially shunts the signal from the resistance at low frequency making the convergence of the effective capacitance to the substrate capacitance occur very early in the frequency sweep.

4.5 Low Frequency Models

The form of the level-2 varactor diode compact model is very similar to that of the MIM capacitor. Therefore the development methodology/philosophy proposed for the MIM capacitor applies to the varactor diodes. The same forms of lower level models, i.e. level-1 and level-0, are therefore obtained with the varactor diode.

A model without inductance, i.e. magnetic behavior not taken into account, is therefore a natural regression of the high frequency equivalent circuit as was the case with the MIM capacitor. The effect of neglecting the inductance is to restrict the range of validity of the model to low frequencies.

The least complex model for the varactor will be an equivalent circuit that neglects inductive phenomenon while at the same time neglecting substrate effects. As with the MIM capacitors this representation will be very limited. Under loaded conditions the predictions will prove to be inaccurate. However, for low frequency use where the cathode is grounded this model can provide a very good prediction of varactor diode behavior. The reader is referred to chapter 3 for an in-depth investigation into the tradeoffs of model reduction.

4.6 Summary

In this chapter, a high frequency compact equivalent circuit was developed for a varactor diode. From the geometry of a typical varactor diode a physical model was first developed. The physical model accounted for magnetic interactions between fingers in interdigitated structures, self-inductances, capacitive coupling and losses, both in the substrate and well. To develop the compact model, a methodology for calculating the required lumped inductance values based on the accurate representation of self and mutual inductance in the physical model was first developed, and was used to determine the model inductance parameters from physical dimensions. Essentially the method consisted of calculating the physical self and mutual inductances based on the finger and inter-finger geometry, localizing the mutual inductances to victim fingers and computing a parallel equivalent. Simulation results showed excellent agreement between the lossless compact model and lossless physical model. A wide variety of geometries were simulated (varying finger length and number of fingers) in order to ensure the viability of this procedure for a broad base of devices.

The active region losses were subsequently introduced into the compact model by method of a parallel equivalent. Once again, very good agreement was seen between the lossy compact model prediction and the lossy version of the physical model for a wide range of structures with reasonable dimensions.

Finally, capacitive coupling to the substrate and a substrate representation were added to the compact model. Theoretical comparisons of the complete compact model and physical model were carried out for 5 hypothetical devices with dimensions corresponding to plausible real world device dimensions. Comparison of the generated S -parameters and predicted effective capacitance showed percentage differences below 1% for all test cases.

The model was then applied to devices fabricated with STMicroelectronics Sige2 process. The through path effective capacitance, quality factor and buried layer to substrate capacitance were used to compare model and measurement up to 40GHz. The

results showed reasonably good agreement between model prediction and measured behavior.

The high frequency model parameters can be determined with the following equations and procedures. Applying the methodology developed in section 4.2.2 the total equivalent inductance can be computed with (4.21) and then the two series inductances, L_s , can be computed with (4.22). The individual well resistances can be determined with (4.25) and the total equivalent value for the compact model can be computed with (4.26). The anode to cathode and buried layer to substrate capacitances can be computed with (3.1) and (3.2) with the voltage scaling relationship given by (4.2). For the purpose of this thesis however the area and peripheral components were normalized to the finger and buried layer area. The total capacitances were therefore given by (4.1) for anode to cathode junction and (4.27) for the buried layer to substrate junction. The substrate parameters, C_s and R_s , were determined through curve fitting as was done in the MIM capacitor case due to the lack of a closed form expression for each parameter.

CHAPTER 5: Polysilicon Resistors

In this chapter a high frequency distributed, n -section, equivalent circuit model developed for polysilicon resistors is presented. The model consists of a cascade of T-equivalent networks. A procedure for determining the required number of segments, based on physical parameters, is presented.

5.1 Introduction to Integrated Polysilicon Resistors

In silicon-based processes thin film resistors are often formed from polysilicon since, like single crystal silicon, its resistivity can be adjusted via added impurities. Sheet resistances ranging from $100 \Omega/\square$ to $1 \text{ k}\Omega/\square$ are common. A cross-sectional view of a generic polysilicon resistor is shown in figure 5.1.

Figure 5.1: Cross-section of a generic polysilicon resistor

The dopant concentration in the polysilicon strip edges is increased in order to provide a low resistance ohmic contact. The low resistivity polysilicon at the edges prevents the formation of a schottky diode, however, as a consequence of the low resistance poly, the effective length of the resistor is reduced from the drawn length. The separation distance between the two highly doped polysilicon regions determines the effective resistor length.

5.1.1 Models and Methodologies

Compact equivalent circuit models for resistors have been developed for silicon and III-V based processes. A high frequency lumped model for a NiCr resistor in a GaAs process is presented in [14]. The model consists of a pi-equivalent section, which includes resistance, capacitance and inductance, however no consideration is given to the delay line or distributed nature of very low conductivity resistors. A high frequency model for polysilicon resistors has also been developed by [38] with consideration to the distributed nature; however, the model is limited to two cascaded segments and no concise procedure is presented for determining the required number of segments based on physical parameters and frequency band of interest. In addition, very high frequency operation of the model has not been verified. In [39] a lumped element equivalent circuit model is developed for a meander-line resistor fabricated out of a high conductivity metal. Operation of the model has been demonstrated for resistances as high as $4\text{k}\Omega$; however, the frequency dependant behavior was only verified up to 16 GHz.

5.1.2 Extrinsic Parameters

A complete equivalent circuit model for a polysilicon resistor is shown in figure 5.2 where the core of the resistor, identified as the effective resistance region in figure 5.1, is abstracted with a block representation.

Figure 5.2: High level model for polysilicon resistor

The regions of highly doped polysilicon, at each edge of the resistor, effectively short the salicide or metal contacts to the high resistivity polysilicon. Hence carriers flowing through these regions do not experience a meaningful potential drop. In addition, the contact resistance, which can be a large portion of the total resistance for small devices [14], can also be made negligible through proper use of contacts. As a consequence both resistances can be neglected in the development of a high frequency equivalent circuit model. The capacitance, shown between each port of the resistor, in figure 5.2, models the coupling that occurs between the two metal contact regions. This capacitance can be neglected on the basis that the minimum spacing between contacts in most processes is too large to generate a significant amount of capacitance. Also, simply sizing the device appropriately can ensure that this parasitic capacitance remain very small. Thus, only the contents of the dashed box in figure 5.2 are considered in the development of a high frequency equivalent circuit model.

5.1.3 Distributed Models

When the wavelength of a signal propagating through a device approaches the physical dimensions of the device a distributed parameter model must be used to accurately represent the variation in magnitude and phase, which occurs along the length of the conductive medium.

At microwave frequencies the free-space wavelength can range from 1 mm to 1 m [40]. For signals propagating in a silicon-SiO₂ environment in quasi-TEM mode the velocity of propagation is reduced from the free-space value due to the effective permittivity of the medium. Thus, the wavelength, or guided wavelength, in a lossless conductive medium is shorter than that in free-space. Microstrip lines are a common element in integrated circuits that can have long physical lengths. Most structures on integrated circuits that have a long physical length, such as aluminum and copper microstrip lines, are very good conductors and can be analyzed as such. From transmission line theory it can be shown that the guided wavelength on a very good

conductor such as copper is approximately 4 mm at 40 GHz, when losses are neglected. In such a medium the guided wavelength is much larger than the dimensions of typical passive device structures thus a distributed parameter network is not explicitly required. However, this applies to lossless or very low loss conductive mediums. As shown in [41], for long and narrow microstrip lines, in which $R \gg \omega L$, a distributed n -section RC network is typically required to properly predict the propagation delay or phase shift.

Thin film resistors are essentially low conductivity microstrip lines. The characteristics of such a conductor, and the effects on wave propagation, are unlike that encountered for ideal or low-loss transmission media. In such conductors the guided wavelength becomes a function of the conductivity, or resistance, and as a result the wavelength can be shortened to a significant degree [41]. This is analogous to the behavior of long and narrow microstrip lines for which $R \gg \omega L$ and in which a distributed parameter model is required. It is generally assumed (simple rule of thumb) that in circumstances where the electrical length of a resistor is larger than approximately 5% of the guided wavelength a distributed model may be required to adequately predict the device behavior. No published result has dealt with the problem of estimating the number of sections required and the tradeoff of performance with the number of sections.

5.2 High Frequency Equivalent Circuit Model

The high frequency equivalent circuit model is concerned with the characteristics of the region inside the dashed box in figure 5.2. The capacitive coupling between the low resistivity polysilicon and the substrate, represented as C_p in figure 5.2, must be modeled, as does the high resistivity region of the polysilicon film, identified, as the effective resistance region in figure 5.2.

5.2.1 Capacitive Coupling at Low Resistivity Edges

The edges of the polysilicon film are distinct from the high resistance core due to their very low resistance. The contribution of these highly doped regions to the overall loss in the resistor may be negligible, however, capacitive coupling between the edge regions and the substrate is not. As shown in figure 5.2, two capacitors are used to model the coupling for each respective edge. The total capacitance at each edge is approximately given by

$$C_{p^+} \cong \hat{C}_{edge} A_{edge} + C_{peri} (L_t - L_{eff}) \quad (5.1)$$

where $\hat{C}_{edge}$ is the area component of the edge capacitance and can be computed using (3.1), A_{edge} is the area of each edge region, C_{peri} is the peripheral component of capacitance and can be computed using (3.2), L_t is the total length of the resistor and L_{eff} is the length of the high resistance region. The solution partitions the peripheral component equally along the length and is an approximate solution since it doesn't account for extra fringing at the edges.

5.2.2 Modeling the High Resistance Region

The high frequency model developed for the effective resistance region of a resistor is based on a special case of the theory of wave propagation through a lossy medium. Essentially it is based on the fact that $R \gg \omega L$ for most integrated monolithic resistors up to extremely high frequencies and that a distributed parameter network, or transmission line type model, may be required.

In order to illustrate that polysilicon resistors may fall into the category of a very lossy transmission line and thus may require an n -section distributed parameter network the system is initially simplified in the sense that the substrate is modeled as an ideal ground plane (i.e. any substrate effects are neglected).

From transmission line theory it can be shown that the general complex propagation constant, i.e. for any arbitrary medium that can support TEM mode, is given by

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} \quad (5.2)$$

where R , L , C and G are the per unit length resistance, inductance, capacitance and conductance of a general transmission line. For good conductors such as aluminum or copper interconnect, in which $R \ll \omega L$, it can easily be shown that the phase constant is approximately given by $\beta \cong \omega \sqrt{LC}$ and that the guided wavelength is basically equivalent to that found in a lossless medium of the same effective permittivity. However, for very lossy lines (either long and narrow metallic lines or high resistivity polysilicon lines) the assumption that $R \ll \omega L$, which leads to the lowloss approximation, is not valid. In a highly resistive medium the resistance will most likely dominate the inductive reactance. For example, a polysilicon resistor, which has a sheet resistance of $200 \Omega/\square$, and which is $9 \mu\text{m}$ long, $3 \mu\text{m}$ wide and $0.2 \mu\text{m}$ thick, will generate 600Ω of resistance. In contrast, the inductance generated by this polysilicon film calculated from (3.3) is 4.2 pH , which results in a reactance of 0.03Ω at 1 GHz and 1.06Ω at 40 GHz . This clearly demonstrates that the resistance is dominant over the inductive reactance for the frequency range of interest in this thesis. In addition, the conductance can also be neglected, but simply on the basis that silicon dioxide is a good dielectric. Therefore the following assumptions, $R \gg \omega L$ and $G \cong 0$, can be made and the complex propagation constant is therefore reduced to the following form.

$$\gamma \cong \sqrt{j\omega CR} \quad (5.3)$$

which can be further simplified to

$$\gamma \cong (1 + j) \sqrt{\frac{(\omega CR)}{2}} \quad (5.4)$$

In [41], expression (5.2) was used to show that the characteristic impedance of such a lossy line ($R \gg \omega L$) is approximately given by

$$Z_0 \cong (1-j)\sqrt{\frac{R}{\omega C}} \quad (5.5)$$

which clearly shows that the characteristic impedance is a function of the per unit length resistance and capacitance. From (5.3) it is also easily shown that the attenuation and phase constants are sole functions of R and C under such conditions and that both are given by

$$\alpha \cong \beta \cong \sqrt{\frac{(\omega CR)}{2}} \quad (5.6)$$

Thus, the guided wavelength, which is a function of the phase constant, has an inverse square root relation with resistance for very lossy lines. The guided wavelength is therefore given by

$$\lambda_g = 2\pi\sqrt{\frac{2}{\omega CR}} \quad (5.7)$$

where R and C are per unit length quantities. From (5.7), it is clear that the guided wavelength will be shorter in high resistance conductive mediums. To illustrate this further, the guided wavelength flowing through a $1\text{k}\Omega$ resistor is computed using (5.7).

The per unit length resistance and capacitance are chosen to be $0.2 \frac{\Omega}{\mu\text{m}}$ and

$0.55 \frac{\text{fF}}{\mu\text{m}}$ which equates to a high resistance region that is $5 \mu\text{m}$ long, $5 \mu\text{m}$ wide, with a

polysilicon and oxide thickness of $0.2 \mu\text{m}$ and $0.4 \mu\text{m}$. The sheet resistance for this example was chosen to be $1 \text{ k}\Omega/\square$. The guided wavelength in the resistor is found to be $53 \mu\text{m}$ at 40GHz , which indicates that the longitudinal dimension of the resistor

represents approximately 10% of the total wavelength. Thus, it is possible for the length of a physical device to be at least 5% or more of the guided wavelength in low conductivity mediums. As a consequence, a distributed parameter model, where the number of segments can be determined based on the properties of the resistor, is required.

5.2.2.1 Ideal RC Propagation Model

The T-section shown in figure 5.3 is a standard transmission line segment, one which represents a finite slice of a conductor, with the exception that the conductance, which models loss in the dielectric layer, has been ignored on the presumption of a low loss dielectric, and as discussed in the previous section, inductance is also neglected since

$R \gg \omega L$. Thus, the standard $RLCG$ transmission line segment is reduced to a simpler RC form.

Figure 5.3: Single segment of a distributed equivalent circuit model for a polysilicon resistor

The resistance, R , is half the per unit length resistance, since the incremental resistance is split in a T-section representation, thus it is given by

$$R = \frac{1}{2\sigma tw} \quad (5.8)$$

where σ is the polysilicon conductivity, and t and w are the polysilicon thickness and width. The parameter N represents the finite number of sections in the distributed

model. The capacitance, C , is the per unit length capacitance of the high resistance region and is given by

$$C = \hat{C}_{eff} w + C_{peri} \quad (5.9)$$

where $\hat{C}_{eff}$ is the per unit area capacitance of the high resistance region and can be calculated using (3.1) and w is the width of the resistor (or polysilicon strip).

Assuming that the guided wavelength is much larger than the physical dimension of the device only one T-section (segment) would be required to model the resistor. Thus, when $N=1$, each resistor in figure 5.3 will represent half of the total resistance and the capacitor will be equal to the total capacitance generated in the high resistance region. When conditions require a distributed network, such as the one shown in figure 5.4, the per unit length quantities (or half the per unit length quantity in the case of the resistors) can be multiplied by the length represented by each section to determine the per section values.

Figure 5.4: Equivalent circuit model for polysilicon resistors

The high resistance region is shown enclosed in the dashed box of figure 5.4. The total resistance in each respective section is given by $\frac{2RL_{eff}}{N}$ where N is the total number of sections in the distributed network, and where, $\frac{L_{eff}}{N}$ represents the length of each

respective section. The distributed network is simply a cascade of the section shown in figure 5.3. The network essentially takes the form of an RC delay line.

The total number of segments required to model the resistor can be determined from the physical length of the device and guided wavelength, which is a function of the frequency, and per unit length resistance and capacitance. From an arbitrary rule of thumb it is generally assumed one needs more than one segment when the device length is greater than 5% of the total guided wavelength. Assuming this condition is satisfied, the number of required segments, also assuming one segment is needed per 5%, is given by

$$N = \frac{20L_{eff}}{\lambda_g} \quad (5.10)$$

In order to illustrate the validity of this assumption an RC delay line of the form shown inside the dashed box of figure 5.4 is constructed for an arbitrary number of sections, i.e. N sections, using chain matrix principles. The $ABCD$ matrix describing one T-section of the distributed network of figure 5.4 is given by

$$M_{section} = \begin{bmatrix} 1 + \frac{j\omega C_{eff} R_{eff}}{2N^2} & \frac{R_{eff}}{N} + \frac{j\omega C_{eff} R_{eff}^2}{4N^3} \\ \frac{j\omega C_{eff}}{N} & 1 + \frac{j\omega C_{eff} R_{eff}}{2N^2} \end{bmatrix} \quad (5.12)$$

where R_{eff} is the total DC resistance and is given by $2RL_{eff}$, C_{eff} is the total capacitance of the high resistance region and is given by CL_{eff} and N defines the total number of sections. The $ABCD$ matrix of an entire distributed resistor model or RC delay line, as shown in figure 5.4, can be computed using (5.12). For N sections the final resistor chain matrix is given by

$$M_{res} = (M_{section})^N \quad (5.13)$$

From (5.13) general two-port parameters can be determined for the distributed network regardless of the number of sections it includes.

In order to validate (5.10), and the procedure to determine the number of sections based on the 5% per segment rule, three test case resistors are used to compare the results obtained with a model containing the number of segments predicted by (5.10) and a reference model. The reference is a distributed RC delay model that contains 800 segments. The reason for using 800 segments is that a distributed model with many segments provides a closer approximation to structures that exhibit transmission line type behavior. In this thesis it is assumed that 800 segments are enough to accurately represent the distributed nature of a network. The real part of the input impedance, i.e. the effective resistance, when one side of the delay line model is grounded is used for comparison of the reference model and the model containing a limited number of segments. The effective resistance obtained from the ABCD matrix, M_{res} , is given by

$$R_{eff}(\omega) = \text{Re}\left(A(\omega) \cdot C(\omega)^{-1}\right) \quad (5.14)$$

where A and C are parameters of the ABCD matrix. The parameters used to determine the number of sections required using (5.10) and construct the model and reference model, are listed in table 5.1 for all three resistors. A single tone signal was assumed and the frequency was chosen to be 40 GHz.

$R_{eff}(0)$ (Ω)	L_{eff} (μm)	w (μm)	Sheet resistance (Ω/SQ)	t_{poly} (μm)	t_{ox} (μm)	C_{eff} (fF)
10000	40	4	1000	0.15	0.4	18
4000	8	2	1000	0.15	0.4	2
300	9	3	100	0.15	0.4	3

Table 5.1: Parameters for three polysilicon resistors

The purpose of the comparison is not to validate the entire distributed approach of modeling the resistor, but to show that expression (5.10) is a good predictor for the number of segments required in an RC delay line given the maximum frequency, and total resistance and capacitance of a high resistivity conductive medium. The guided

wavelengths for the $10\text{k}\Omega$, $4\text{k}\Omega$ and 300Ω resistors were found to be approximately equal to $52\text{ }\mu\text{m}$, $47\text{ }\mu\text{m}$ and $160\text{ }\mu\text{m}$ respectively. The number of sections required according to (5.10) is 15 sections for the $10\text{k}\Omega$ device, 3 sections for the $4\text{k}\Omega$ device and 1 section for the 300Ω device. The simulation results are shown in figure 5.5, 5.6 and 5.7.

Figure 5.5: Effective resistance for $10\text{k}\Omega$ resistor

Figure 5.6: Effective resistance for 4kΩ resistor

Figure 5.7: Effective resistance for 300 Ω resistor

The simulated results obtained with (5.14) show excellent agreement between the reference RC delay line, i.e. model with 800 segments, and the model in which the number of segments was determined using (5.10). The percentage difference in effective resistance at 40 GHz is 2.5% for the 10k Ω resistor, 1% for the 4k Ω resistor and 0.1% for the 300 Ω resistor. Simulation results for the two high resistance cases, when only one section is used in the model, show a very large difference in effective resistance when compared to the reference model confirming the need for a distributed model in these instances.

In all three simulations the maximum signal frequency was assumed to be 40GHz, however, the method applies to higher frequencies since the guided wavelength is a function of frequency. For lower frequencies the section requirements would simply be less. Beyond a certain low frequency limit the physical length of a device will be less

than 5% of the guided wavelength and a single segment or lumped model is all that is required, such was the case for the 300Ω resistor even at 40 GHz.

The results obtained from comparisons of RC delay lines with one end connected to ground, i.e. inherently assumed in (5.14), showed that the 5% assumption was adequate in predicting the number of segments required. However, the ground applied at one end of the distributed network reduces the sensitivity of the method to the shunting pathways. A more robust approach would be to compare the input resistance of the same lines with one end open forcing all the current through the shunting pathways. This would accentuate the sensitivity of the effective resistance to the shunting pathways. It has been shown in [42] that the open circuit equivalent resistance of a network is $1/3$ the DC resistance for a certain bandwidth. This only applies for a limited bandwidth since the limit of the capacitive reactances as the frequency goes to infinity is 0. However, it does demonstrate the sensitivity of the open circuit equivalent resistance to the shunting pathways. In open circuit conditions a 1 section lumped model would never be enough since the effective resistance predicted by such a model would only be half the DC resistance in the limited frequency band. Therefore even the 300Ω resistor, which was deemed to require only one segment by the 5% rule and verified with the short method, could require more than 1 segment. In such an instance the 5% rule proves insufficient. Although certain models, in which the number of segments was obtained by the 5% rule, would prove inadequate in the open configuration, models, those that already contain many segments, will perform to satisfaction. Also, keeping in mind the general application areas of resistors, one can quickly determine that such a condition will most likely not occur. Rather than devising a new percentage that shows agreement with the effective open resistance, which will overestimate the number of sections needed in short conditions (a more likely outcome), the number of segments can simply be kept to that predicted by the 5% rule with the understanding that the model accuracy will decrease when connected to a relatively (i.e. relative to itself) high impedance.

5.2.2.2 Substrate Effects

In the preceding discussions the substrate was modeled as an ideal ground plane in order to simplify the system. However, as was shown in the MIM capacitor and varactor diode chapters, the substrate does not typically act as an ideal ground reference due to its finite conductivity and dielectric nature. As a matter of fact, the substrate was shown, in chapter 3 and 4, to affect the performance of the respective devices at high frequencies. Like in the previous two chapters, the substrate can be represented as a parallel resistance and capacitance; however, in this application it may be distributed depending on whether the core of the resistor needs a distributed representation.

Although important for MIM capacitors and varactors, the substrate network does not impact polysilicon resistors to the same degree. This is primarily due to the small size of most resistors. Generally, foundries offer polysilicon resistors with different sheet resistances. In most cases at least two offerings are made. For example, a low sheet resistance device ($\sim 100\text{s } \Omega/\square$) and a device with a considerably higher sheet resistance ($\sim 1000\text{s } \Omega/\square$). This provides the designer a means of achieving any desired resistance while keeping the device dimensions to a minimum. This degree of freedom is not generally found for MIM capacitors and varactors, hence the need for a complete substrate representation in those devices.

The implications, in terms of modeling the substrate, are two fold. The first is that the substrate capacitance will be very small ($C_s < 1\text{fF}$) in most cases since it is approximately 13 times smaller than the oxide capacitance (see MIM capacitors results), which in turn is small due to the size of the device. Hence, it can be assumed that the substrate resistance will shunt the capacitance for the frequency range of interest in this thesis. The second is that, in a design where the substrate is well grounded, the relative impedance of the oxide capacitance (due to the small size of the structure) will be much larger than the substrate resistance for most resistor values. Hence the sensitivity of the resistor to the substrate resistance is generally less than that of MIM capacitors or varactors. A substrate model consisting of a simple resistor could be implemented, but difficulty in predicting the value based on physical parameters and the distributed nature

of certain resistors will result in values that are erroneous and require subsequent optimization. Furthermore, the lack of a coherent scaling approach for the substrate resistance implies that optimization has to be performed for each individual device. Nonetheless, modeling the substrate as a resistor is a possibility despite the many difficulties surrounding extraction and scaling and is discussed further in comparison of resistance measurements.

5.3 Experiment Results

Three polysilicon resistors have been fabricated using STMicroelectronics SiGe2 process in order to provide some experimental comparisons for the high frequency resistor model. S-parameter measurements were performed on each device at two different sites on wafer. The measurements were performed up to 40 GHz, which was the frequency limit of the test equipment.

5.3.1 SiGe2 Resistors

The thin film resistors in the SiGe2 process are fabricated out of polysilicon. A cross-section of the resistors looks basically as shown in figure 5.1. There are two polysilicon resistor offerings, a low resistivity version, $115 \Omega/\square$, and a high resistivity version, $1000 \Omega/\square$.

5.3.2 Sample Devices

The specifications for the three sample resistors are listed in table 5.2.

DC Resistance	233 Ω	2k Ω	5k Ω
Total length (μm)	10.3	8.2	14.2
Effective length (μm)	6.1	4	10
Width (μm)	3	2	2
Sheet Resistance (Ω/SQ)	115	1000	1000
Oxide thickness (μm)	.4	.4	.4
Polysilicon thickness (μm)	.15	.15	.15

Table 5.2: Physical specifications for sample devices

5.3.3 Measurement Setup

The measurement setup and instruments are the same that were used for the MIM capacitor measurements, described in section 3.3.3.

5.3.4 Computation and Extraction of Model Parameters

There are three distinct parameters in the resistor model. The first is C_{p^+} , which models the capacitive coupling between the low resistivity edges of the resistor and the substrate. The second is the total DC resistance identified as $R_{eff} = 2RL_{eff}$ and the third is $C_{eff} = CL_{eff}$, which is the total capacitance of the effective resistance region.

Both capacitances, C_{p^+} and C_{eff} , are computed using equation (3.1) and (3.2) based on their respective geometrical parameters. The total DC resistance is extracted (since this parameter can easily be extracted) from measurement data in order to obtain an accurate value because it is known to have a 10% process variation [28]. The extraction is performed with (5.15) and the average of the first four low frequency points is generally used as the final value.

$$R_{eff} = Z_{11} + Z_{22} - Z_{12} - Z_{21} \quad (5.15)$$

The extraction assumes that the device can be modeled by a single T-section therefore it must be performed at lower frequencies in order to ensure that the results are valid.

Another model component that must be determined is the number of sections required in the model for each sample device. The number of sections for all three devices was determined from (5.10) and the per unit length resistance, $2R$, and per unit length capacitance, C . The per unit length quantities were computed by dividing the total values (i.e. $R_{eff}(0)$ and C_{eff}) by L_{eff} .

5.3.5 Model Parameters

The model parameters for all three devices are shown in table 5.3.

	$R_{eff}(0) (\Omega)$		$C_{eff} (fF)$	$C_{p^*} (fF)$	N
	Site 1	Site 2			
233 (Ω)	240.5	246	2.1	1.1	1
2 ($k\Omega$)	1877	1811	1.1	0.7	2
5 ($k\Omega$)	4700	4726	2.8	0.6	4

Table 5.3: Resistor Model Parameters for Sample Devices

The extracted values show that the resistances are on the low and high side of the nominal values. However, they are within process tolerances. Having analytically calculated the resistor values the model predictions would have been offset from the measurement.

5.3.6 Measurement Results and Model Predictions

The validity of the resistor model, i.e. figure 5.4, is verified through comparisons of the frequency dependant behavior of the effective resistance, i.e. $R_{eff}(\omega)$. Not to be confused with R_{eff} which is simply the DC resistance. The relation between both is given by $R_{eff}(\omega = 0) = R_{eff} = R_{dc}$.

The comparison of the model predictions and measured results will first be given for the 233 Ω resistor, followed by those for the 2k Ω and 5k Ω devices.

The effective resistance in function of the frequency is plotted in figure 5.8 for the 233Ω device.

Figure 5.8: Effective resistance of 233Ω device in function of frequency

The measurement results are slightly noisy. This is accentuated in figure 5.8 because the resistance scale is not very wide. The apparent increase in effective resistance seen between 35 GHz and 40 GHz in both measured results are most likely induced by the measurement system or de-embedding. From the measurement system point of view, the errors could easily be the result of a degraded calibration error model due to drift errors. Possible sources are probe degradation, vibrations, temperature drift or changes in the exact cable configuration from when calibration was done. De-embedding of the short test fixture could also have induced an error in the data leading to the increases seen around 35GHz [12]. Inductance can quickly be eliminated as a possible source of increase by computing the series inductance using (3.3). Results show that the

inductance is approximately 4.9 pH , and hence the inductive reactance is only $j1.2\Omega$ at 40GHz . This does not account for the increase shown in the measured result. The model predictions are inline with the measured results if the peaking seen at higher frequency is a result of measurement error. The model predictions shown in figure 5.8 are for a resistor model with 1 section, i.e. a lumped representation, as was determined necessary with (5.10). For comparison a simulation result for a model with 100 sections is superimposed on the result obtained with 1 section in figure 5.9 in order to show that further increases are fruitless.

Figure 5.9: Effective resistance of 233Ω device predicted with 1 and 100 sections in the model

Simulations with a model containing 100 sections show barely any difference in predicted value (approximately 0.1% at 40 GHz) agreeing with the result of (5.10) that only one section is required.

Having shown reasonably good agreement with the 233Ω device, the model will now be compared to measurements of the $2\text{k}\Omega$ device. The effective resistance in function of the frequency is plotted in figure 5.10 for the $2\text{k}\Omega$ device. The

model used for generating the predictions contains two sections. The parameters were computed given the specific geometry of the device in question and the number of sections used.

Figure 5.10: Effective resistance of 2k Ω device in function of frequency

The measured results are reasonably well behaved up to about 25 GHz to 30 GHz after which both results diverge from one another spiking in opposite directions. In both cases, once again, these are most probably the result of measurement error or an error associated with de-embedding. Since the devices each exhibit a different tendency this is an easier assumption to make than in a case where both exhibited the same behavior. In both cases, the model shows good agreement with the raw measured data up to about 25 to 30GHz (in the region where the measured data is well behaved). In order to show agreement up to 40 GHz, the measurement curves were fitted through polynomial regression up to approximately 27 GHz. A 2nd order polynomial was generated to represent the measurement up to that frequency. The polynomial was then used to extrapolate the measurement out to 40 GHz. The fitted and extrapolated measured results

are also shown in figure 5.10 (identified with regression in the legend). The model prediction and extrapolated measurement show very good agreement up to 27 GHz and even out to 40 GHz. There is slight disagreement between the model prediction and the measurement of the 1st device between 30 GHz and 40 GHz; however, this could be related to the frequency limit that was chosen when fitting the curve since there is a rapid decrease around 27 GHz for that device measurement. A higher order polynomial was not used since the behavior of the curve out to 27 GHz was fairly monotonic and easily represented by a 2nd order polynomial. Also, polynomials of higher order have more chance of oscillating outside the fitted region.

The number of sections required in the model, obtained from (5.10), was found to be 1.6, which was rounded up to 2 since an integer number of segments is required. This indicates that 1 section should also give a reasonable result. Simulation results for the model with 1 and 2 sections are shown in figure 5.11 along with one of the measurement results.

Figure 5.11: One and two section model predictions for 2k Ω resistor

The prediction of the model composed of two sections is slightly better than the 1 section version. Thus, rounding up to number from 1.6 to 2 gave slightly better accuracy.

The next comparison is with regards to the $5k\Omega$ device. The effective resistance in function of the frequency for the $5k\Omega$ device is plotted in figure 5.12. The model used for generating the prediction contains four sections and the per-section parameters were computed in consequence.

Figure 5.12: Effective resistance of $5k\Omega$ device in function of frequency

In this instance the measured data is reasonably well behaved for the entire frequency band. However, the model prediction is off by a considerable amount for most of the bandwidth. The number of sections was subsequently increased to verify whether adding or removing segments would result in an improvement. The predictions of a model with 1, 4 and 100 sections are shown in figure 5.13.

Figure 5.13: Predictions of model with 1, 4 and 100 sections for 5k Ω device.

Adding segments does not improve the predictive capability of the model. The prediction of the model when it contains 100 sections is basically the same as when it contains four sections. This demonstrates that 4 sections are enough for an accurate representation of the distributed nature. The predictive capability of the model when only one section is used is much worse than when it contains four sections also indicating that a distributed representation is required.

There are two problems with the model prediction. This first is that the decreasing slope of the curve at high frequencies is not modeled adequately and the second is that the curve is shifted upward in the low to mid-frequencies. Both issues will be addressed in turn.

Substrate resistance causes the decreasing slope of the effective resistance at high frequencies. The oxide capacitances, C_{p^+} and C_{eff} , also plays a part since their reactance is an inverse function of frequency. However, flattening to the degree seen in figure 5.13 between 30 GHz and 40 GHz is not solely caused by the asymptotic behavior of the substrate capacitance at high frequencies, given the values of capacitance for this device. Essentially, the incremental change in the magnitude of the shunt path impedance diminishes as the frequency increases. This occurs whether substrate resistance is present or not although the region in which the slope decreases is different depending on the relative size of the oxide capacitance and resistance. As the frequencies increase and the capacitive reactance of C_{p^+} and C_{eff} decrease, the substrate resistance becomes a larger part of the path impedance. Further increases in frequency beyond a certain threshold will not result in a significant change in path impedance, due primarily to the presence of the substrate resistance in this instance, and as a result the decrease in effective resistance will become less significant. This is thought to be more significant in high resistance devices (when compared to a low resistance device of the same area) because of the possibility that a larger proportion of the input signal leaks through the shunting capacitors. To account for this effect the model was modified to account for the substrate resistance of this device. A simple resistor was added between the shunting capacitors and ground. Its value was extracted from the device and slightly optimized. The predictions of the 1 section, 4 section and 100 section model are shown in figure 5.14 for a substrate resistance of 900Ω .

Figure 5.14: Result for model with substrate resistance ($R_s=900\Omega$)

When substrate resistance is included in the model, there is much better agreement at high frequencies. The general shape of the entire curve is well matched to the measured data. Therefore it is clear that substrate resistance plays a part in such large devices. However, the concerns outlined in section 5.2.2.2 still apply and as a result a formal model with substrate resistance is not developed. This only has implications for larger devices since the 233Ω and $2k\Omega$ devices were relatively well modeled without substrate resistance. Further work in this area would require the development of a scaling methodology for the substrate resistance.

The second discrepancy between the model prediction and measured data, i.e. the offset in resistance in the low to mid-frequencies, is most likely a simple issue of process variation, although this is not a certainty at this time. Assuming that the total oxide

capacitance calculated by the analytical equation is off by 15% the resulting predictions with slightly increased capacitance look as shown in figure 5.15.

Figure 5.15: Capacitive coupling for the $5k\Omega$ model is increased by 0.5 fF .

The model that has 4 sections is in very good agreement with the measured data. The 100 sections model is in very close agreement with the 4 sections model showing again that only 4 sections are required. The 1 section model is considerably off as expected. The offset has largely been removed from the measured data with a 15% increase in capacitance. The lack of substrate capacitance in the model was initially ruled out as a possible cause behind the discrepancy because its value is smaller than the oxide capacitance and would cause an effective decrease in capacitance, which is not the observed behavior. The $5k\Omega$ resistor was the longest and most narrow amongst the samples therefore it is most likely that some particularity with its structure caused a slight under-estimation of capacitance when computed using (3.1) and (3.3).

5.4 Summary

In this chapter a high frequency equivalent circuit model for polysilicon resistors was developed. From the physical nature of the device two distinct regions were identified and modeled according to their characteristics. The model accounts for the series resistance and parasitic capacitive coupling to the substrate. The model neglects inductance and the dielectric conductance on the basis that they are negligible. From propagation theory it was shown that a distributed representation might be required for certain resistors. As a consequence, a distributed model was developed along with a procedure for determining the required number of segments based on physical parameters. The number of sections required was shown to be specifically dependant on the per unit length resistance, capacitance and frequency bandwidth.

Finally, the model was compared to measurement results of three devices. Good agreement between the predictions and measurements was seen. Slight discrepancies exist for the largest and longest resistor (a $5k\Omega$ device); however, these were related to substrate resistance and process variations. It was shown that a substrate model consisting solely of a resistor may be required, however, a coherent scaling procedure must first be developed.

The parameters in the high frequency model can be computed with the following equations. The capacitive coupling between the low resistance region and substrate can be computed with (5.1), half the per unit length resistance can be computed with (5.8), the per unit length capacitance can be computed with (5.9) and the number of sections can determined from using (5.10).

CHAPTER 6: Conclusion

6.1 Summary

The design of 40Gb/s physical layer circuits in SiGe bipolar technologies requires that passive components on silicon substrates perform to very high frequencies. As a consequence, passive device models used for circuit design in CAD environments must have the ability to predict the behavior of such devices up to 40GHz. The work undertaken in this thesis was as an investigation into the behavior of passive devices on silicon up to 40GHz coupled with the development of high frequency equivalent circuit models. The passive devices were modeled with equivalent circuits since they are easily represented by a netlist and are thus ideal for integration in a CAD environment for circuit design and simulation.

The specific devices of interest for this thesis were MIM capacitors, varactor diodes and polysilicon resistors. These devices are crucial to the operation of many circuit building blocks for physical layer circuits such as voltage-controlled oscillators. Three versions of each device were fabricated in STMicroelectronics' SiGe2 process. All devices were characterized with *S*-parameters up to 40GHz. The high frequency behavior of most of the devices measured for this thesis was found to be far from ideal. The high frequency equivalent circuit models developed in this thesis, for every device type, were compared to measurements showing that the models were capable of predicting the devices behavior up to 40GHz.

Two parasitic effects were found to be the primary cause for the non-ideal behavior of MIM capacitors and varactor diodes at high frequency while an all-together different phenomenon was identified for polysilicon resistors. For MIM capacitors and varactor diodes, inductance and substrate effects were found to be non-negligible in terms of their impact on the behavior of the devices at high frequencies. Analytic equations were introduced for computing inductance and methodologies were presented for the

development of equivalent circuit models that account for inductance. A substrate representation was also introduced for both device models, however, the substrate impedance was difficult to model analytically at high frequencies and as such an extraction procedure was introduced for the computation of the substrate parameters. A distributed effect was found to be the cause behind the peculiar high frequency behavior of the resistors. The contents of the thesis will now be summarized and discussed in more detail on a per chapter basis.

In chapter 2, the overall measurement system was introduced along with an outline of possible sources of error. The measurement system was divided into two parts the first consisting of off-wafer components and the second, termed test-fixture, consisting of on-wafer components. The possible sources of error in each part of the measurement system were identified. These consisted of cables, connectors and probes for the off-wafer measurement system and bond pads and interconnect for the test-fixture. The need for error correction procedures for each part of the measurement system was subsequently outlined followed by the introduction of two of the main error correction methodologies used in on-wafer device characterization. The error correction procedure known as calibration was defined to remove all systematic errors associated with the off-wafer measurement system when no error coefficients are neglected in the general error model, while the error correction procedure termed de-embedding was shown to remove all systematic errors associated with the test-fixture. Measurements in which both corrections had been applied were deemed representative of the measured device.

The introduction to device characterization was followed by an introduction to three of the main modeling methodologies for integrated devices. These consisted of EM modeling, artificial neural network modeling and modeling with equivalent circuits. Each was shown to have respective application areas with equivalent circuit modeling being the most prominent in CAD environments for circuit design and simulation.

In chapter 3, a high frequency equivalent circuit model for a MIM capacitor was developed. The structure of a generic MIM capacitor was first defined as being two

overlapping conductors separated by a thin dielectric layer. The high frequency equivalent circuit model was subsequently presented as being an agglomeration of various components each representative of a phenomenon that must be accounted for up to very high frequencies. The equivalent circuit model was shown to be composed of two inductors, three capacitors and three resistances. The inductive effect was demonstrated to be particularly non-negligible at high frequencies and was therefore carefully modeled. The self-inductance of each plate and mutual inductance between plates were shown to be of significant importance in the overall inductive effect. However, due to the very close proximity of the conductors in MIM capacitors (hundreds of angstroms in separation distance) it was demonstrated that the mutual inductance could be lumped in with the self-inductances. Essentially, a composite plate approximation was presented where the self-inductance of the composite plate was the total inductance of the MIM capacitors. Simulation results with the total inductance calculated in this fashion were shown to be in very good agreement with measurement.

The parasitic capacitive effects were also shown to be of some significance, especially under loaded conditions. One parasitic capacitance was shown to be the result of the dielectric layer separating the bottom plate of the capacitor from the substrate while the other was a result of the dielectric nature of the substrate. In addition to its dielectric nature, the silicon substrate was also found to be lossy in the low GHz frequencies and was therefore modeled with the aid of a resistor in addition to a capacitor. Signal loss to the substrate under loaded conditions was demonstrated through simulations with various loads and the need for a substrate network in an accurate high frequency model was demonstrated. The substrate model components were not calculated analytically due to the complex nature of the problem. An extraction procedure was devised instead in order to extract the values from measured devices.

The model was finally applied to three actual devices, which had been measured up to 40GHz. The through path effective capacitance and metal to ground capacitance predicted by the model were shown to be in good agreement with measurement.

Models of less complexity were then developed by removing key high frequency components from the models. The first low complexity model, termed level-1, was

constructed by simply neglecting inductance. A large decrease (in comparison to the high frequency model) in the models predictive capability was immediately observed. The models predictive capability was found to be limited in frequency, but was still accurate at low frequencies. A second low complexity model, termed level-0, was then developed by neglecting inductance, losses and the substrate effects. This model was shown to have a very limited range of accuracy. The level-1 model could not predict the MIM capacitor quality factor and did not account for losses in the substrate in an accurate fashion.

In chapter 4, a high frequency model developed for varactor diodes was developed and presented. A typical varactor diode cross-section showing the active region was first introduced along with the common multi-finger configuration which is used to minimize resistive losses. A compact high frequency equivalent circuit model was then presented. The model was shown to account for inductances, capacitances and resistive losses.

In order to develop the compact model a full physical model dependant on the number of fingers was first developed. Initially, due to the complexity of the problem, the analysis of the full physical model was restricted to anode/cathode capacitive coupling and inductance interactions. Accurate modeling of the device at high frequency required an accurate representation for the inductive interactions. In this case it was shown that there was self-inductance in each finger and mutual inductance between every finger in a given pair. Analytic equations for calculating the self and mutual inductances were introduced along with a procedure for localizing the mutual inductances to victim fingers. An analysis of the finger currents was undertaken to quantify the error involved in localization. The error was found to be quite reasonable. The physical model (accounting only for anode/cathode capacitive coupling and inductances) was then reduced to a localized model where explicit mutual coupling between fingers had been instantiated into inductors and localized to victim branches. Simulations comparing the LC localized model and physical model (LC only) showed excellent agreement. However, the localized LC model was still dependant on the number of fingers in the

varactor diode. The final step in the reduction procedure involved finding the parallel equivalent value for the capacitors and inductors in the localized model. Thus, once a parallel equivalent for all the inductors and capacitors in the localized model had been determined, a single inductor and capacitor could be used to represent varactor diodes (LC only). This representation was the compact model since it no longer depended on the number of fingers. Simulation results of the compact model (LC only) showed excellent agreement with the localized (LC only) model. A wide variety of geometries were simulated (varying finger length and number of fingers) in order to ensure the viability of this procedure for a broad base of devices. In summary, the LC reduction methodology consisted of calculating the physical self and mutual inductances based on the finger and inter-finger geometry, localizing the mutual inductances to victim fingers and computing a parallel equivalent. The compact model (LC only) simulation results also showed excellent agreement with the physical model (LC only) results.

The losses in a typical varactor diode were then introduced into the physical model. Various sources of resistive losses were identified with the well resistance being the most prominent. All other sources of loss were neglected on the basis that the well resistance was dominant and that carefully laying out the structure would lead to a minimization of most other sources of loss. The well resistance was then added to the compact model by method of a parallel equivalent. Once again, very good agreement was seen between the lossy compact model prediction and the localized and physical models (RLC) for a wide range of structures with reasonable dimensions.

Capacitive coupling to the substrate and a substrate representation were then added to the compact model. Theoretical comparisons of the complete compact model and full physical model were carried out for 5 hypothetical devices with dimensions corresponding to plausible real world device dimensions. Comparison of the generated *S*-parameters and predicted effective capacitance showed percentage differences below 1% for all test cases.

Finally, the model was applied to devices fabricated with STMicroelectronics Sig2 process. The through path effective capacitance, quality factor and buried layer to substrate capacitance were used to compare model and measurement up to 40GHz. The

results showed reasonably good agreement between model prediction and measured behavior.

In chapter 5, a high frequency equivalent circuit model for polysilicon resistors was developed. A generic thin film polysilicon resistor was first presented. From the physical nature of the device two distinct regions were identified and modeled according to their characteristics. The first region was identified as a low resistivity region and the second was labeled as a high resistivity region. The losses in the low resistivity region were deemed negligible since they were insignificant compared to losses in the high resistance region.

The model representation for the low resistance region was first developed. The capacitive coupling to the substrate in this region was found to be non-negligible. Therefore capacitors were used to model the low resistance regions. A model representation for the high resistance region was subsequently developed. From general propagation theory it was shown that for a highly resistive medium such as polysilicon the phase constant and characteristic impedance were dependant mainly on the per unit length resistance and capacitance. As a consequence it was determined that the guided wavelength had an inverse square root relationship with the resistance and capacitance and that it was possible for the resistor dimension parallel to the wave propagation to be at least 5% or more of the guided wavelength. From this result a distributed resistor model was developed along with a procedure for determining the required number of sections. A simple relation for determining the required number of segments based on the resistance, capacitance, and frequency was developed. The computation also assumed multiple sections would only be required if the length of the device was at least equivalent to 5% of the guided wavelength. In addition, the number of segments required (assuming the previous condition was met) was based on attributing one segment per 5% of the total guided wavelength when the wavelength and device length are equal. The number of required segments is therefore normalized to the ratio of the device length and guided wavelength. Simulations of the model for various resistor values were carried out. Comparisons of the simulation results with the number of sections defined by the

equation to results obtained with a reference model containing 800 sections were in excellent agreement. The distributed networks were generated through an algorithm developed for automatically generating RC delay lines with n -segments. However, comparisons of the input resistances were carried out with one side of the RC chain grounded. A more robust method was also introduced, one which might have required changing the allocation requirements however, conditions under which this more robust method could have proven valid were deemed vary rare.

Finally, the model was compared to measurement results of three devices. Good agreement between the predictions and measurements was seen. Slight discrepancies were observed for the largest and longest resistor (a $5\text{k}\Omega$ device); however, these were related to substrate resistance and process variations. It was shown that a substrate model consisting solely of a resistor may be required, however, a coherent scaling procedure must first be developed.

6.2 Future Work

There are various directions in which this work may be continued. An obvious continuation would involve an investigation of the high frequency behavior of monolithic inductors with emphasis on sub-nanohenry inductors. The development of a physical high frequency equivalent circuit model for such inductors could also be undertaken. In conjunction with the work on inductors, a study on the performance of various 3D electromagnetic simulators in terms of their predictive ability, using inductors as a medium, would also be useful to ascertain if any deficiencies exist.

The high frequency performance of symmetric differential inductors also needs investigation. This type of configuration is growing in popularity for high frequency circuit design since it has been shown to yield a better quality factor and occupy less area on-chip. The work would involve the development of a high frequency equivalent circuit model for differential inductors and performance comparisons could be carried out at the circuit level. Perhaps using voltage-controlled oscillators as a testing medium.

In terms of the devices already investigated and modeled in the thesis further work is needed in order to apply the varactor model and resistor model to a greater variety of devices. Larger varactor diodes ($5\text{pF} > C_{j0} > 500\text{ fF}$) could be used to validate the model over a broader range. A larger set of sample resistors would also prove useful in this regard.

The development of a scaling methodology for the substrate impedance is also an important aspect that requires further investigation. For the most part, the models developed in the thesis make use of a substrate model, however, the lack of a scaling procedure for the substrate network requires that the substrate parameters be extracted for every device. Of particular interest is the impact of local substrate ground contacts on the value of the substrate resistance.

Another related area of interest is in the application of the high frequency models developed in this thesis to the design of high frequency circuits. To this end, comparisons of the high frequency models to existing lower frequency models could be carried out through simulation and design of a VCO. Simulation results of a VCO with lower frequency passive device models and with high frequency passive device models could be compared to measured results of the same VCO to ascertain the impact of the high frequency models at the system level.

Finally, further work is required to investigate the impact of system level parasitics and implications, if any, on the high frequency passive models. The work undertaken in this thesis was dedicated to the development of accurate high frequency equivalent circuits models. Passive devices were characterized in a somewhat isolated environment and were modeled in great detail without consideration to external components and effects. The necessity of certain components in detailed high frequency models must be ascertained when placed in a context where system level parasitics exist.

REFERENCES

- [1] Voinigescu, S.P., et al., "Circuits and Technologies for Highly Integrated Optical Networking IC's at 10 Gb/s to 40 Gb/s," in *CICC Digest*, 2001.
- [2] Razavi, B., *RF Microelectronics*. Englewood Cliffs, NJ: Prentice-Hall, 1998.
- [3] Voinigescu, S.P., Marchesan, D., and Copeland, M.A., "A Family of Monolithic Inductor-Varactor SiGe-HBT VCOs for 20GHz to 30GHz LMDS and Fiber-Optic Receiver Applications," in *RFIC Symposium Digest of Papers*, pp.173-177, 2000.
- [4] Li, H., Rein, H.-M., Kreienkamp, P., and Klein, W., "47GHz VCO With Low Phase Noise Fabricated in a SiGe Bipolar Production Technology," *IEEE Microwave and Wireless Components Letters*, vol. 12, no. 3, pp. 79-81, 2002.
- [5] Wijnen, P.J., *On the Characterization and Optimization of High-Speed Silicon Bipolar Transistors*. Cascade Micro Tech, Inc., 1995.
- [6] Cho, Hanjin and Burk, D. E., "A Three-Step Method for the De-Embedding of High Frequency S-Parameter Measurements," *IEEE Transactions on Electron Devices*, vol.38, no. 6, pp. 1371-1375, 1991.
- [7] Kolding, T.E., "A Four-Step Method for De-Embedding Gigahertz On-Wafer CMOS Measurements," *IEEE Transactions on Electronic Devices*, vol. 47, no. 4, pp. 1371-1375, 2000.
- [8] Veluswami, A., Nakhla, M.S., and Zhang, Q.J., "The application of Neural Networks to EM-Based Simulation and Optimization of Interconnects in High-Speed VLSI Circuits," *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, no. 5, pp. 712-723, 1997.
- [9] Wang, F., and Zhang, Q.J., "Knowledge-Based Neural Models for Microwave Design," *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, no. 12, pp. 2333-2343, 1997.

- [10] Bandler, J., et al., "Neuromodeling of Microwave Circuits Exploiting Space-Mapping Technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, no. 12, pp. 2417-2427, 1999.
- [11] Devabhaktuni, V.K., et al., "A Robust Algorithm for Automatic Development of Neural-Network Models for Microwave Applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 12, pp. 2282-2291, 2001.
- [12] Danesh, M., and Long, J.R., "Differentially Driven Symmetric Microstrip Inductors," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 1, pp. 332-341, 2002.
- [13] Sieiro, J., et al., "A Physical Frequency-Dependent Compact Model for RF Integrated Inductors," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 1, pp. 384-392, 2002.
- [14] Ladbrooke, P.H., *MMIC Design: GaAs FETs and HEMTs*. Norwood, MA: Artech House, 1989.
- [15] Pettenpaul, E., "CAD Models of Lumped Elements on GaAs up to 18 GHz", *IEEE Transactions on Microwave Theory and Techniques*, vol. 36, no. 2, pp. 294-304, 1988.
- [16] Meijs, N., and Fokkema, J.T., "VLSI Circuit Reconstruction from Mask Topology," *Integration*, vol.2, no.2, pp. 85-119, 1984.
- [17] Sakurai, S., and Tamaru, K., "Simple Formulas for Two-and-Three-Dimensional Capacitances," *IEEE Transactions on Electron Devices*, vol. ED-30, no. 2, pp. 183-185, 1983.
- [18] Lee, T., *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge, UK: Cambridge University Press, 1998.
- [19] Grover, F.W., *Inductance Calculations*, 2nd ed., New-York: D. Van Nostrand, 1947.

- [20] Greenhouse, H.M., "Design of Planar Rectangular Microelectronics Inductors," *IEEE Transactions on Parts, Hybrids and Packaging*, vol. PHP-10, no. 2, pp. 101-108, 1974.
- [21] Coperich, K.M., et al., "Systematic Development of Transmission-Line Models for Interconnects With Frequency-Dependent Losses," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 10, pp. 1677-1685, 2001.
- [22] Coperich, K.M., et al., "Enhanced Skin Effect for Partial-Element Equivalent-Circuit (PEEC) Models," *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, no. 9, pp. 1435-1442, 2000.
- [23] Faraji-Dana, R., and Chow, Y.L., "The Current Distribution and AC Resistance of a Microstrip Structure," *IEEE Transactions on Microwave Theory and Techniques*, vol. 38, no. 9, pp. 1268-1277, 1990.
- [24] Pfof, M., Rein, H.M., and Holzwarth, T., "Modeling Substrate Effects in the Design of High-Speed Si-Bipolar IC's," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 10, pp. 1493-1501, 1996.
- [25] Yue, C.P., and Wong, S.S., "A Study on Substrate Effects of Silicon-Based RF Passive Components," in *Microwave Symposium Digest*, vol. 4, pp. 1625-1628, 1999.
- [26] Fost, P., and Rein, H.M., "Modeling and Measurement of Substrate Coupling in Si-Bipolar IC's up to 40GHz," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 4, pp. 582-591, 1998.
- [27] Gharpurey, R., and Meyer, R.G., "Modeling and Analysis of Substrate Coupling in Integrated Circuits," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 3, pp. 344-353, 1996.
- [28] SiGe2 Electrical Specifications and Layout Design Rules, STMicroelectronics, 300 Fitzgerald Road, Ottawa, ON.

- [29] Rogers, J.W.M, Macedo, J.A., and Plett, C., "The Effect of Varactor Nonlinearity on the Phase Noise of Completely Integrated VCOs," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 9, pp. 1360-1367, 2000.
 - [30] Molnar, K., et al., "MOS Varactor Modeling With a Subcircuit Utilizing the BSIM3v3 Model," *IEEE Transactions on Electron Devices*, vol. 49, no. 7, pp. 1206-1210, 2002.
 - [31] Soorapanth, T., et al., "Analysis and Optimization of Accumulation-Mode Varactor for RF ICs," in *1998 Symposium on VLSI Circuits Digest of Technical Papers*, pp. 11-13, 1998.
 - [32] Su, C.Y., et al., "Scalable RF MIS varactor model," *Electronic Letters*, vol. 37, no. 12, pp. 760-761, 2001.
 - [33] Su, C.Y., et al., "BSIM3v3-based varactor model," *Electronic Letters*, vol. 37, no. 8, pp. 525-527, 2001.
 - [34] Sze, S.M., *Physics of Semiconductor Devices*, 2nd ed., New York: Wiley, 1981.
 - [35] Schroeter, M., and Walkey, D.J., "Physical Modeling of Lateral Scaling in Bipolar Transistors," *IEEE Journal of Solid State Circuits*, vol. 31, no. 10, pp. 1484-1492, 1996.
 - [36] Schroeter, M., et al., "Physics and Process-Based Bipolar Transistor Modeling for Integrated Circuit Design," vol. 34, no. 8, pp. 1136-1149, 1999.
 - [37] HSPICE, *HSPICE User's Manual: Elements and Device Models*, vol. 2., Campbell, CA: Meta-Software, 1996.
 - [38] Hai, T., "Modeling of Passives," Internal Report, Nortel Networks, 2000.
 - [39] Murji, R., and Deen, M.J., "A Scalable Meander-Line Resistor Model for Silicon RFICs," *IEEE Transactions on Electron Devices*, vol. 49, no. 1, pp. 187-190, 2002.
-

- [40] Pozar, D.M., *Microwave Engineering*, 2nd ed., New-York: John Wiley & Sons, Inc., 1998.
 - [41] Deutsch, A., "When are Transmission-Line Effects Important for On-Chip Interconnections," *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, no. 10, pp. 1836-1846, 1997.
 - [42] Wolf, P., "Microwave Properties of Schottky-barrier Field-effect Transistors," *IBM Journal of Research & Dev.*, vol.14, pp. 125-141, 1970.
-