Wireless System-on-Chip Sensor Design for Radiotherapy Applications

By

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Abstract

This research is focused on the development of a novel miniaturized wireless dosimeter for cancer patient radiotherapy. During radiotherapy treatment, cancerous region of the body are exposed to high energy radiation. The knowledge of the exact amount of radiation penetrating the body is essential for a successful treatment. Too little radiation will be ineffective and too much can seriously harm the patient. The device used to measure the radiation dose is called a dosimeter. Present dosimeters have numerous limitations. Most are either limited in sensitivity or are susceptible to temperature and environmental variations, thus leading to inaccurate measurements. The existing dosimeters are wired, large in size, non-wearable and require high operating voltages. The wires deflect and scatter the radiation away from the targeted region during the irradiation process. To alleviate the abovementioned problems, a miniaturized wireless dosimeter System on Chip (SoC) solution is proposed.

The foremost requirement of a wireless dosimeter is a miniaturized, highly sensitive and reliable low power radiation sensor. In this dissertation new radiation sensors have been designed in standard low cost CMOS process (DALSA 0.8 μm CMOS). Several innovative radiation sensors have been realized to i) improve sensitivity, ii) reduce operating voltage, iii) reject environmental and process changes, and iv) enable wireless operation. A fully integrated SoC dosimeter having radiation sensors with signal processing and readout circuits fabricated on the same chip has been demonstrated for the first time. The sensitivity of the sensor has been improved by more than 10 % by reducing the capacitance to the floating gate (FG) and using elevated metal shielding. Both the enhanced sensitivity of the sensors and the presence of an identical FG reference permit low voltage operation. The radiation sensors have been characterized for sensitivity, and stability using measurements, simulations and mathematical analysis. The use of an identical FG reference also eliminates the effects of environmental and process changes. The dosimeter has been designed for integration with a transmitter (TX) chip to transmit the sensor data in a wireless fashion. The integrated SPE on the sensor chip conditions the signal and converts it to the desired control signal that modulates the TX waveform. The entire wireless dosimeter is 0.5 cm^2 in size and consumes 5.3 mW of power.

To complete the wireless sensor system, a novel miniaturized receiver (RX) SoC has been designed. This is the smallest reported 5 GHz receiver (1.3 mm^2) with an on-chip antenna in a standard IBM 0.13 μm CMOS process. It incorporates a low noise amplifier (LNA) with unique on-chip antenna impedance matching and a fully differential Delay Lock Loop (DLL) circuit. The miniaturization is achieved by placing the circuits inside a meandered antenna. The co-design methodology for on-chip antenna and LNA is described. Such a methodology resulted in very wideband impedance matching without the need for matching elements. The LNA is completely differential, consumes only 8 mW of power with a noise figure of 2.9 dB and provides a gain of 21 dB. The total gain of the antenna and receiver chip is -15 dB and it consume 14 mW of power. Design tradeoffs and measurement challenges of the SoC RX are described in detail.

The results of this research demonstrate the feasibility of low power wireless radiation sensors, and provide a basis for the development of other wireless biomedical devices.

Dedication

This dissertation is dedicated to...

my mother,

for her prayers, unconditional love, support,
and being there whenever I needed her,

the loving memory of my father,

who believed in me right from the beginning,

and my wife,

for her love and invaluable support.

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I like to express gratitude for my friend and fellow Atif Shamim. He shares with me, more than anyone else, all the delightful, as well as, depressing moments throughout this work. His role was instrumental in this research. His help, suggestions, and encouragement were a constant source of inspiration for me both for this project and in specific matters of life. I couldn't have achieved so much without having him onboard. Thank you Atif!

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On a personal note, I wish to thank my mother, siblings, close family, and friends who have been very encouraging and keep praying for my success throughout this time. I would also like to thank my wife, Nausheen, for being supportive, loving and understanding during the long hours that I have spent working on my dissertation.

Table of Contents

Chapter 1

Chapter 2

List of Tables

List of Figures and Illustrations

List of Abbreviations and Symbols

α'	scattering coefficient
A	area
AFP	automatic floating gate programming
Al	aluminum
ASIC	application specific integrated circuit
AUT	antenna under test
BiCMOS	bipolar complementary metal oxide semiconductor
BMC	Best Medical Canada
BPSG /bpsg	boro-phospho-silicates-glass
C	columb or capacitance
C_1	
C_{fb}	capacitances from the floating-gate to the bulk
C_{fd}	capacitances from the floating-gate to the drain
C_{fs}	capacitances from the floating-gate to the source
CMC	Canadian Microelectronics Corporation
CMOS	complementary metal–oxide–semiconductor
^{60}Co	Cobalt-60
C_{ox}	capacitance of oxide
CP	charge pump
C_{sum}	sum of capacitance
D	radiation dose or down
dB	decibel
dBm	measured power referenced to one milliwatt
DCDL	digitally controlled delay line
DE	delay element
ΔV_T	change in threshold voltage
DFF	data flip flop
DIP	dual in line package
DLL	delay lock loop
E	electric field
E_{dep}	deposition of energy
E_0	
e-h	electron-hole
ε_{ox}	permittivity of oxide
E_{ox}	electric field across gate oxide
ESA	European Space Agency
EVARM	extra vehicle activity radiation monitoring

f	fraction of radiation generated charge trapped at interface
1/f	flicker noise
FG	floating gate
FGMOS	floating gate metal oxide semiconductor
FGMOSFET	floating gate metal–oxide–semiconductor field effect transistor
FGRADFET	floating gate radiation-sensitive field effect transistor
FG sensor	floating gate sensor
FN	Fowler–Nordheim
FOX / fox	field oxide
FPGA	field-programmable gate array
Frq	frequency
FSM	finite state machine
G	gain
γ	attenuation coefficient / high energy radiation rays
GaAs	Gallium Arsenide
G_c	on-chip antenna gain
GHz	giga hertz
GPS	Global Positioning System
gm_{FG}	trans-conductance of the transistor from the floating-gate
Gy	gray
HCI	hot carrier injection
HFSS	high frequency structure simulator
HiperLAN	high performance radio local area network
IC	integrated circuit
I_D	drain current
I_{DFG}	drain current of floating gate transistor
IFG	interdigitated floating gate
I_{fn}	FN tunnelling current
I_{inj}	Injector current
IIP3	input third-order intercept point
ISM	industrial, scientific and medical
I_{tun0}	pre-exponential current
IV	current voltage
J	joule
Jitter-pp	peak-peak jitter
k	Boltzmann's constant (1.38×10^{-23} m^2kg/ s^2K).
κ	sub-threshold slope
KHz	kilo hertz

Krad	kilo rad
L	gate length of a transistor
LET	*linear energy transfer*
LF	loop filter
LNA	low noise amplifier
LNA_G	gain of LNA
LOCOS	local oxide
LPF	low-pass filter
Ls	source inductor
LTCC	low temperature co-fired ceramic
μ	charge mobility or micro ($1x10^{-6}$)
M2	metal 2
M3	metal 3
MCML	MOS current mode logic
MEMS	micro-electro-mechanical- systems
MFG	multiple floating gate
MHz	mega hertz
MOSFET	metal–oxide–semiconductor field effect transistor
N	number of sensors connected in parallel
NF	noise figure
NBG	negative bias generator
NRC	National Research Council of Canada
NRC-INMS	NRC Institute for National Measurement Standards
$N_T(E_{fn})$	number of charge traps at the quasi-Fermi level
OCRI	Ottawa centre for research and innovation
Ω	ohm
OPAMP	operational amplifier
ox	gate oxide or oxide
PD	phase detector
PFD	phase and frequency detector
PIN	p- intrinsic-n
PLL	phase lock loop
PMOS	p-type metal oxide semiconductor
ρ_{ox}	oxide density
P_{rc}	received power
PS	phase selector
ρ_{SiO_2}	SiO_2 material density
P_t	transmit power

q	charge on an electron
Q	quality factor
Q_{col}	total charge collected
Q_{fg}	charge trapped on the floating gate
Q_{0t}	oxide trapped charge
R	roentgen or resistance
RADFET	radiation-sensitive field effect transistor
R(E)	recombination rate of the e-h pairs
rem	unit of absorbed radiation dose (1 rem = 0.01 Sv)
REM	Radiation Experiments and Monitors (a company)
R_f	feedback resistance
RF	radio frequency
RFID	radio frequency identification
RX	receiver
S11	input reflection coefficient
SFG	standard floating gate
Si	Silicon
SI	system international (of units)
SiGe	Silicon Germanium
SiO_2	Silicon di-oxide
SMFG	standard multiple floating gate
SoC	system- on- chip
S-Parameters	scattering parameters
SPE	signal processing electronics
Sv	sievert
t_{ox}	thickness of (gate) oxide
TX	transmitter
UV	ultra violet
U-NII	unlicensed national information infrastructure
UV-C	UV-conductance
U_T	thermal voltage
U	up
VCDL	voltage-controlled-delay-line
V_{CLK}	clock voltage
V_{ctrl}	control voltage
VCO	voltage controlled oscillator
V_D	voltages at the drain
V_{DD}	supply voltage
V_{DS}	drain to source voltage

V_f	constant that varies with oxide thickness
V_{FGo}	initial floating gate potential
V_{inj}	tunnelling injector voltage
V_o	output voltage
V_{out}	output voltage
V_{ox}	voltage across the oxide
V_S	voltages at the source
V_T	threshold voltage (of transistor)
W	channel width
$W_{e\text{-}h}$	electron-hole pair creation energy
W/L	width/length (of the gate of a transistor)
X, Y	predefined integers
Z_r	antenna impedance

Chapter 1

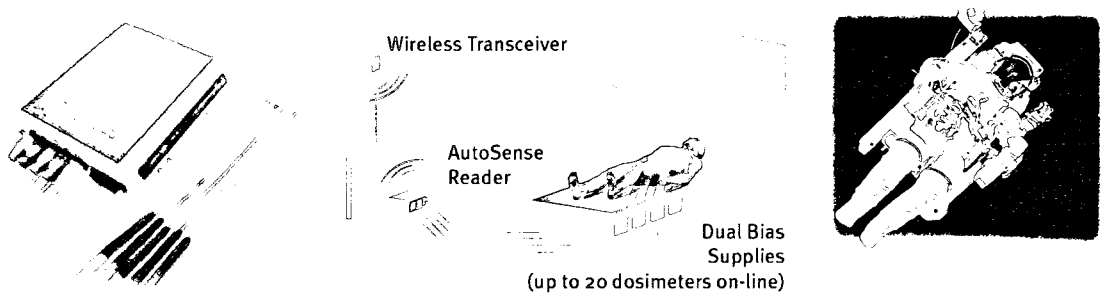
Introduction

The innovation in electronic device fabrication processes has enabled efficient and cost effective biomedical systems. The most active area of research in modern day health care is wireless sensors. The wireless aspect is not only revolutionary for health care delivery but also brings in added convenience for the patients. Wireless biomedical sensors of today are benefitting from the advancements in micro-fabrication processes, micro-electro-mechanical-systems (MEMS) and nano-structures. Systems such as chemical detection sensors, DNA sequencers, blood analysis sensors, environmental sensors, and systems for medical, military and outer space research are the prime focus of the ongoing research. One area needing much attention is radiation sensors used in radiotherapy applications.

1.1 Motivation

For radiotherapy applications, specifically for treating cancer affected tissues with high energy radiations, the knowledge of the exact amount of radiation penetrating the body is essential for a successful treatment. Too little radiation will be ineffective and too much can seriously harm the patient. The device used to measure the radiation dose is called a dosimeter. A state of the art dosimeter is shown in Figure 1.1 (a). These MOSFET based sensors, known as RADFETs, utilize the change in the threshold voltage before and after the radiation exposure to measure the dose. Present dosimeters have numerous limitations. Most are either limited in sensitivity or are susceptible to temperature and environmental variations, thus leading to inaccurate measurements. The existing dosimeters are wired, large in size, non-wearable and require high

operating voltages to enhance sensitivity. The wires deflect and scatter the radiation away from the targeted region during the irradiation process and cause damage to the healthy tissues along with the targeted cancerous region.



(a) (b) (c)

Figure 1.1 (a) Existing dosimeter by Best Medical Canada, (b) Clutter of wires over cancer patient for radiation dose measurements (c) Astronaut space walk

Moreover these radiation sensors employ discrete off-chip components to process and condition the signal from the sensor. In order to realize miniaturized, wearable and wireless dosimeter, these radiation sensors must operate at low voltages, have on-chip signal processing electronics and be ultra sensitive. They should be invariant to temperature and process variations for enhanced accuracy. If these challenges are overcome, then the realization of dosimeters suitable for wireless integration is feasible. This concept is beneficial for cancer patients undergoing radiotherapy (shown in Figure 1.1 (b) and is also suitable for applications like Extra Vehicle Activity Radiation Monitoring (EVARM) where continuous monitoring of the radiation experienced by the astronauts could be life saving (shown in Figure 1.1 (c).

Furthermore, incidents like [1] in France in which several casualties have been caused by the inaccurate exposure to the high energy radiations and similar incident [2] recently in Ottawa Hospital provoke the need of a low cost, accurate, and easy to use dose monitoring system.

A low power radiation sensor with on-chip signal processing circuitry capable of integration with a short range wireless transmitter would improve the overall effectiveness and efficiency of the radiation treatment and monitoring systems.

1.2 Challenges and Proposed System Concept

Key design considerations of a wireless dosimeter are to keep the size, power and cost of the module to a minimum without compromising the sensitivity, accuracy and real time wireless transmission capability. The major challenges associated with the development of such a system are designing accurate non-invasive sensors with on-chip interface signal processing circuitry, realizing low power transmitter (TX) and receiver (RX) circuits with on-chip antennas, incorporating a miniaturized battery that is transparent to high energy radiation and integrating all of the components on a small, and low cost platform. A block diagram of the wireless dosimeter system is shown in Figure 1.2. It consists of a system-on-chip (SoC) transmitter with monolithic dosimeter and a SoC receiver.

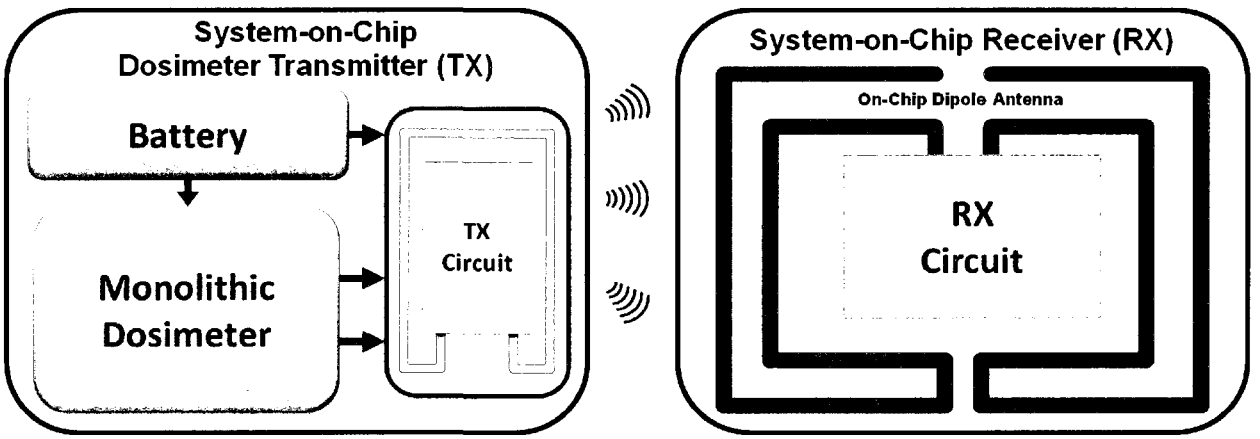


Figure 1.2 Proposed wireless dosimeter system

The realization of the overall system was a collaborative effort with fellow Ph.D. student Atif Shamim. This dissertation is focused on the design and challenges involved in monolithic dosimeter and wireless SoC receiver. An overview of all components is given in chapter 2 but the design details and challenges specific to this work only are presented in this thesis.

Radiation Sensor

The major challenge in the desired solution is to develop low power monolithic radiation sensor compatible with a wireless transceiver system. Specifically, the desired features in realizing such a radiation sensor are 1) low voltage operation while keeping the sensitivity within the range suitable for radiotherapy applications, 2) choice of a suitable low cost commercial

foundry process which is compatible with the remainder of the system, and 3) a fully integrated monolithic chip which eliminates interconnect losses and reduces noise levels to optimize the sensor performance.

Most of the MOSFET type sensors [3, 4] are either built in a specialized process, not suitable for the signal processing circuits, or require very high voltage [5, 6] to keep the sensitivity in the desired range, and hence not feasible for monolithic integration of the readout circuit. Designing the radiation sensor for low voltage operation in a standard CMOS process, while keeping the sensitivity high, and integrating the signal processing electronics (SPE), is a key challenge of this dissertation. Innovative design techniques are required to gain high sensitivity at low bias voltages.

Wireless Receiver

Designing a miniaturized, low power, and low cost, receiver suitable for the proposed wireless dosimeter transceiver system has its unique challenges. Innovative designs are needed to reduce the power consumption of RF buffers and amplifiers. Miniaturization requires elimination of off-chip components, such as the antenna and its matching circuitry. System stability and noise immunity are other desired features for system reliability.

1.3 Research Objectives

This research is focused on the design of an innovative radiation sensor with integrated read-out circuitry and a novel fully integrated RX chip. The following are the specific objectives for this dissertation.

Sensor:

1. Achieve higher sensitivity radiation sensor using a commercial CMOS process (having thin gate oxide) for low cost solutions
2. Achieve Low power operation without affecting radiation sensitivity
3. Realize novel dosimeter design to eliminate the environmental and process variations.
4. Conduct charge stability and temperature variation analysis of the new FG sensors

5. Design a monolithic Floating Gate Radiation Field Effect Transistor (FGRADFET) based dosimeter with integrated signal processing electronics (SPE)

Receiver:

6. Develop a fully Integrated CMOS receiver front end with a miniaturized on-chip antenna.
7. Achieve low power RX operation by eliminating off chip and matching components.
8. Design of a DLL based demodulator for inherent stability and noise performance.
9. Investigate feasibility of the complete RX and its extension to multisensory system.

1.4 Research Contributions

The major contributions of this work are listed below:

Contribution #1 High Sensitivity Radiation Sensor

An enhanced sensitivity radiation sensor design, which operates at zero bias and is invariant to environmental and process variations, fabricated in a standard (commercial) CMOS process.

Contribution #2 Novel Wireless Dosimeter for Radiotherapy

First reported monolithic Floating Gate Radiation Field Effect Transistor (FGRADFET) based dosimeter with integrated Signal Processing Electronics (SPE). Further, first of its kind, wireless dosimeter for radiotherapy applications has been demonstrated.

Contribution #3 Miniaturized System on Chip (SoC) Receiver with On-chip Antenna

A miniaturized fully integrated SoC receiver with an on-chip antenna that is conjugately matched to the Low Noise Amplifier (LNA) has been demonstrated. The backend circuitry includes a fast locking fully differential DLL.

Publications and Patent

One journal paper [7] and four conference papers [8-11] have been published that are directly related to this work. One journal paper has recently been accepted [12] and two more [13, 14] have been submitted. A US patent is pending [15] as a result of this research.

Statement of original Contributions in Joint Publications

Some parts of this thesis were done in collaboration with fellow student Atif Shamim. The details of the collaborative work and the resultant publications are listed below.

The wireless transmitter SoC was done in collaboration with Atif Shamim. The author was responsible for designing circuitry to control the TX frequency in the desired range and the SoC layout and verification. He was also extensively involved in the overall system integration and measurement aspects. One journal [7] and four conference papers [8-11] have been published and one journal paper [14] has been submitted as a result of this collaboration.

For the receiver work, the author has designed the LNA, and DLL based demodulator. The on-chip antenna has been designed by Atif Shamim. Again the author was responsible for the layout and verification of the complete receiver SoC, the post processing steps, and the measurements. One journal paper [12] has been accepted for publication from this work.

A journal paper [13] describing the design and challenges of the novel dosimeters has been submitted. The work is an original contribution by the author.

1.5 Significance of Work

This work is the first demonstration of a wearable wireless dosimeter which can measure the radiation dose in real time. The prototype developed in this work demonstrates the feasibility of highly miniaturized, ultra-low power, wireless biomedical sensor systems in standard low cost CMOS process. Though the design is specific to radiotherapy application, the concept can be applied to other applications like legal badges in nuclear labs, radiation monitoring for astronauts during space walks, radon gas detection and UV index monitoring. The demonstration of a wireless dosimeter module won the national technology innovation competition during the Canadian Microelectronics Corporation (CMC) Texpo [16]. The author also received the Ottawa Carleton Research and Innovation's (OCRI) "2008 Researcher of the year award" for this work.

1.6 Thesis Organization

This document is organized in a way that follows the design flow for the wireless radiation sensors.

In Chapter 1, an introduction of the subject and the description of the research objectives and contributions is provided.

The concept of a wireless radiation sensor and the DLL based miniaturized receiver is presented in Chapter 2 along with a detailed literature review of all system components.

Chapter 3 discusses the design of the radiation sensors. Various design iterations have been presented and advantages have been described.

Design of a fully integrated dosimeter is presented in Chapter 4 with details of signal processing electronics and system level integration with wireless transmitter.

In Chapter 5, the design of a low-power DLL based SoC receiver along with LNA and on-chip antenna is presented.

Finally, Chapter 6 concludes the thesis with a summary of the work and some recommendations for future research.

Chapter 2

Overview of Proposed Wireless Dosimeter and Related Research

This chapter presents an overview of the proposed wireless dosimeter along with a literature review of the relevant state of the art technology options. After describing overall system architecture each subsystem will be illustrated.

2.1 Wireless Dosimeter

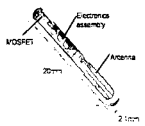
Wireless readout of the measured high energy ionizing radiation is extremely valuable for dose verification and control in radiotherapy. Scientists continue to pursue the development of a wireless dosimeter solution that is accurate, easy to use, small enough to pin-point the target area, facilitating continuous dose monitoring, and transparent to the incident radiation. Available wireless dosimeters do not fulfill most of the above mentioned requirements. They are either very large in size, obstructive to the incident radiation path, or are not sensitive enough to be used in radiotherapy applications.

2.1.1 Comparison of Existing Wireless Dosimeters

A comparison of the available wireless dosimeters that are either commercially available or in the research phase is presented in Table 2.1. In the available literature the only existing floating-gate (FG) MOSFET dosimeter [17] is quite large and is not intended for radiotherapy applications. Moreover, it uses a separate large transmitter module for wireless transmission of data. In the non-FG MOS based dosimeter class, [18] demonstrates a design for a permanent

implant. However, it is not capable of monitoring real time radiation dose and has a very low sensitivity and communication range. An electret-based wireless dosimeter is demonstrated in [19]. It has a communication range of 3–5 cm and an extremely low sensitivity of 11.45 Hz/rad. To compare, the wireless dosimeter presented in this thesis with FGRADFET sensitivity of 5 mV/rad has equivalent sensitivity of 0.5 MHz/rad (200 MHz change in frequency with 2 V change on floating gate). Hence the design is not suitable for practical radiotherapy applications. Another MOSFET based commercially available wireless dosimeter is [20]. The MOSFET sensor that it uses is quite small but the sensor is connected to the power supply and wireless communication module through long wire. The wires are not transparent to the radiation and cause the radiation to scatter in untargeted regions. Moreover the wireless transmitter and power supply unit is very large.

Table 2.1 Comparison of Existing Wireless Radiation Sensors

Parameter				
				
	[17]	[18]	[19]	[20]
Technology	FG-MOSFET	MOSFET	ELECTRET	MOSFET
Module Size	84 x 48 x 17.5 mm	20x2.1mm	1.5 cm diameter 3 mm thick	17.8 x 15.9 x 4.2 cm
Career Frequency	125KHz	-	7 MHz	2.4 GHz
Communication Range	1.2-2.4 m	12 cm	3-5 cm	10 m
Model	DMC 2000S	DVS	-	TN-RD-70-W
Sensitivity	-	0.45 mV/rad	(11.45Hz/rad)*	2.7 mV/rad
Sensor Size	-	0.3x5 μm	-	0.2x0.2 mm
Comments	Not for Radiotherapy	In-vivo	*Extremely Insensitive	Requires high voltage bias

2.1.2 Units of Radiation Dose

A wide variety of units exists in the field of dosimetry and is commonly used in the literature. Making direct conversion between them is confusing. This section describes the relationship between various measurement systems. The older quantity and unit of radiation exposure (ionization in dry air) is the roentgen (R), where 1 R is equal to 2.58×10^{-4} C/Kg. The older quantity and unit of absorbed dose is the rad (radiation absorbed dose), where 1 rad = 0.01 J/kg. The material absorbing the radiation can be tissue or any other medium for example, air, water, lead shielding, etc. To convert absorbed dose to dose equivalent or rem, where the biological effects in man are considered, one modifies with a quality factor. For practical scenarios, with low linear energy transfer (LET) radiation such as γ or x rays, 1 R = 1 rad = 1 rem.

In System International (SI) of quantities and units radiation exposure is now referenced to "air kerma," absorbed dose to gray (Gy), and dose equivalent to the sievert (Sv). 1 Gy = 100 rad, and 1 Sv = 100 rem [21].

Since for human tissue one roentgen equals one rad and the quality factor for x- and gamma rays is one, radiographers can consider the Roentgen, rad, and rem to be equal in value. The table below presents the Q factors for several types of radiation [21]. In this work rad and mV/rad will be used for radiation dose and radiation sensitivity respectively.

Table 2.2 Comparison of Radiation Measurement Units

Type of Radiation	rad	Q Factor	rem	Gy	Sv
X-Ray	1	1	1	0.01	0.01
Gamma Ray	1	1	1	0.01	0.01
Beta Particles	1	1	1	0.01	0.01
Thermal Neutrons	1	5	5	0.01	0.05
Fast Neutrons	1	10	10	0.01	0.1
Alpha Particles	1	20	20	0.01	0.2

2.2 Proposed Wireless Dosimeter System

To overcome the limitations of the available dosimeters a novel wireless System on Chip (SoC) dosimeter for radiotherapy applications is presented here. The hierarchical diagram of the designed wireless dosimeter transceiver system is shown in Figure 2.1.

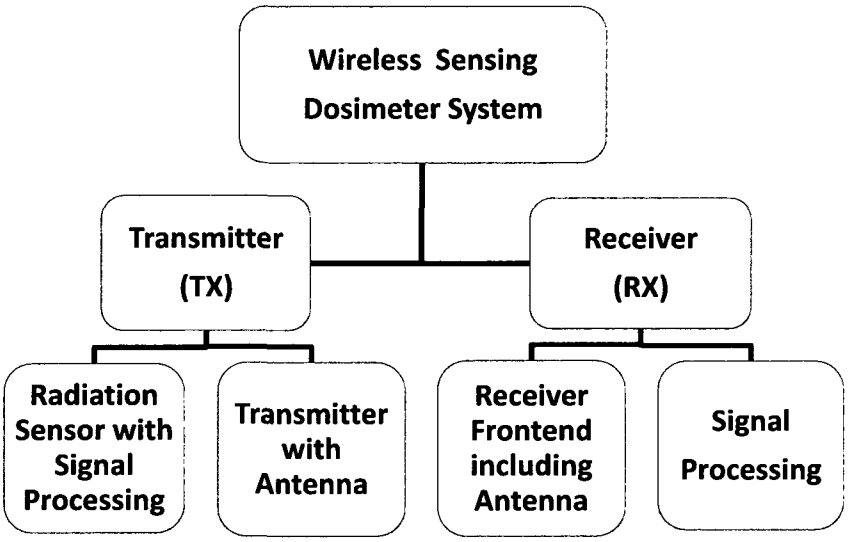


Figure 2.1 Hierarchical diagram of the proposed system

The system architecture has two major components, a wireless dosimeter transmitter (TX) and a Receiver (RX). A brief description of each block is as follows.

2.2.1 Wireless Dosimeter Transmitter

Individual components of the wireless dosimeter transmitter system, as indicated in Figure 2.2, along with related thesis objectives are as follows,

a. **Radiation sensor (FGRADFET)**

   It is the heart of the wireless dosimeter system. In accordance with first four thesis objectives the FGRADFET based sensors have been designed for small size and possibility of monolithic integration with the rest of the system components to achieve a complete SoC solution. Experiment based FGRADFET charge stability and thermal analysis has been done and presented in Chapter 3 for a better understanding of the device behaviours. Functional description and structural evolution of floating gate type dosimeters will be presented later in this chapter.

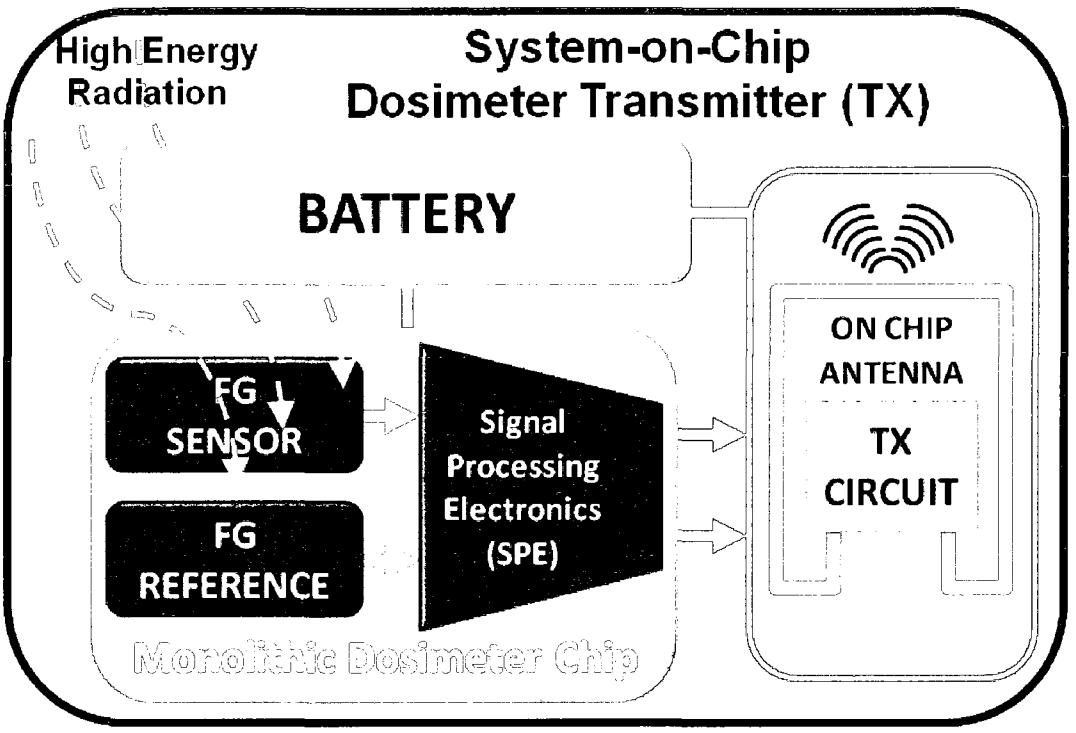


Figure 2.2 Wireless sensor SoC block diagram

b. Sensor Signal Processing Electronics (SPE)

Signal processing electronics is used to translate the change in the property of the sensors caused by incident radiation to an equivalent electrical signal in the desired voltage range. This is related to the objective # 5 of the thesis to design a monolithic dosimeter.

c. TX circuit with on-chip antenna

The signal from the SPE circuit is encoded and transmitted in the desired wireless band. An on-chip TX antenna facilitates the SoC dosimeter solution.

d. Power Source

The choice of a suitable power source for a wireless dosimeter SoC module is very critical. The source should be transparent to the incident radiation to avoid its scattering and causing damage to the healthy tissues. A lithium polymer battery, or ultra charged capacitors with voltage regulatory circuit, are two possibilities that could be considered to fulfill the power supply requirements of the wireless SoC sensor module.

2.2.2 SoC Receiver (RX)

As illustrated in Figure 2.3, similar to the wireless transmitter SoC, the RX front end and demodulating signal processing circuits consist of following parts,

a. **Receiving on-chip antenna**

   On chip antennas is an essential part of the system to achieve a compact SoC RX.

b. **Low Noise Amplifier (LNA)**

   The LNA is the most important component of the RX front end. Its gain and noise performance directly affect the performance of the entire RX. The LNA is co-designed with the antenna for a conjugate impedance match to eliminate the matching components, chip area, and reduce the power consumption of the design. This corresponds to thesis objective 6 and 7.

c. **DLL based demodulator**

   A delay locked loop (DLL) based architecture has been adapted to design the RX. DLL based RX is inherently more stable and doesn't accumulate the jitter as in PLL based demodulators. This work is related to the objective number 8 and 9 of this thesis. DLL based RX architecture will be introduced later in this chapter.

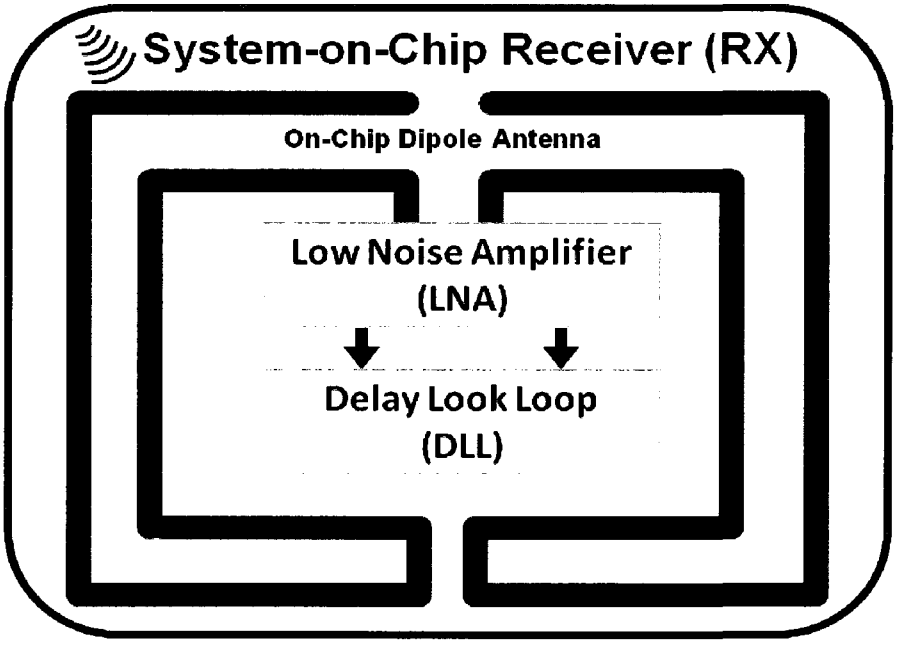


Figure 2.3 Receiver block diagram

2.2.3 Wireless Transceiver Frequency of Operation

For wireless communication of the sensor data, license free frequency bands 802.11a (Unlicensed National Information Infrastructure (U-NII) /5.x GHz frequency), 5.8GHz ISM, and 802.11b/g (ISM/ 2.4 GHz frequency) have been considered. Compared to 5 GHz range, 2.4 GHz band has become very congested. Wireless networks, Bluetooth devices, microwave ovens, baby monitors and cordless phones are all working in this range and are commonly present in any working environment. In contrast, 802.11a devices have 19 non-overlapping channels as compared to three for 802.11b/g devices. Furthermore, the lower part of the 802.11a is internationally used for indoor applications [22]. The 5.15-5.25 GHz range is sometimes referred to as U-NII Indoor. Regulations of this band require use of an integrated (no external) antenna [23]. In addition to the above, for the intended wireless SoC solution, it is much easier to implement on-chip efficient antennae at 5 GHz than 2.4 GHz. Therefore the 5.2 GHz U-NII band has been chosen to implement the proposed wireless SoC design.

RF 5.0 GHz U-NII band

The Unlicensed National Information Infrastructure (U-NII) band covers the higher 5.15-5.35 GHz and 5.725-5.825 GHz range, as displayed in Figure 2.4. It is designed to allow for higher data rates (up to 54 Mbps) via the 802.11a standard. The 802.11a standard defines 12 fixed, non-overlapping channels for use in the 5.0 GHz U-NII band. The European HiperLAN standard also operates in the U-NII band [24].

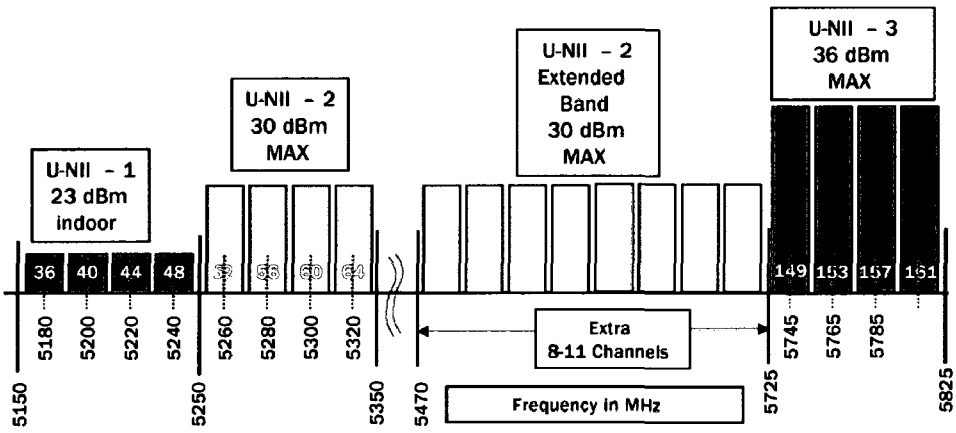


Figure 2.4 IEEE802.11a usage of 5.0 GHZ U-NII bands [24].

2.2.4 Target Specifications of the Proposed Wireless Dosimeter

The required radiation dose for radiotherapy treatment is dependent upon the type and stage of cancer being treated. As given in Table 2.3, for curative cases, the typical dose for a solid epithelial tumor ranges from 6000 to 8000 rad while lymphoma tumors are treated with 2000 to 4000 rad. In case of palliative treatment a single dose of 600 to 1000 rad may be given to painful superficial tumours, to relieve pain. Radiation dose is given in daily fraction called the fraction schedule. Typical fractionation schedule for adults is 180 to 200 rad per day, five days a week, whereas for children, a typical fraction size is 150 to 180 rad per day.

Table 2.3 Typical Radiation Dose for Radiotherapy

Cancer Treatment by Radiotherapy	Condition	Dose rad (cGy)	Fraction schedule
Curative Treatment	Solid epithelial tumor	6000 – 8000*	Typically adults receive 180-200 rad per fraction. The typical treatment schedule is 5 days per week
	Lymphomas	2000 - 4000*	
Palliative Treatment	Painful superficial tumours to relieve pain.	600 - 1000**	
* http://en.wikipedia.org/wiki/Radiotherapy ** http://www.medindia.net/patients/patientinfo/Radiotherapy_Dosage.htm			

Hence the dosimeter for radiotherapy should have the resolution and sensitive to differentiate and measure these radiation doses. Higher sensitivity of the dosimeter permits more precise control over the treatment. For wireless SoC dosimeter the size and power consumption are other major concerns which are affected by the sensor sensitivity, power consumption of the circuits, and the capacity and size of the battery. Table 2.4 summarizes the target specifications of the proposed wireless SoC dosimeter design to satisfy these requirements.

Table 2.4 Target Specifications for the Wireless SoC Dosimeter

Parameter	Target Specification	Limiting factor
Sensitivity	> 1 m V/rad	FGRADFET sensitivity
Power	< 10 mW	Battery capacity
Size	0.5 cm x 0.5 cm	Size of the battery
Wireless Communication Range	> 1 m	On-chip antenna efficiency

2.3 Technology Overview of the State-of-the-Art Wireless Dosimeter Components

The wireless dosimeter system, as described in previous section, has two main components. First is the SoC TX that consists of the radiation sensor and transmission circuitry to be placed on the patient's body, and the second is the SoC RX. The complete wireless dosimeter project has been done in collaboration with another fellow researcher. This thesis is focused on the radiation sensor and the receiver parts of the system. A detailed review of these components is as follows.

2.4 Radiation Sensors

Different types of radiation sensing techniques are known such as ionization chambers, proportional counters, Geiger-Muller counters, scintillation detectors, calorimeters, photographic films, thermo-luminescence, electret and semiconductor (PIN diode, MOSFET, and specialty semiconductors) based sensors [25]. The RADFET based dosimeter was first conceived by Poch and Holmes- Siedle in 1969. Radiation Experiments and Monitors (REM) Oxford Ltd, UK published full details of it over 30 years ago [26]. Shortly after, the European Space Agency (ESA) started using the idea for dosimetry in unmanned satellites [27]. Later, terrestrial applications offered a commercial future to these sensors. Original system ideas arose for the use of the RADFET in clinical, space and emergency applications [28], [29], [30] and later in high-energy physics [31], [32]. With all these applications, the RADFET has gained significance in dosimetry, especially where ultra-small, low-voltage sensors are required. Other advantages of RADFETS are the possibility to integrate with read-out circuitry, real-time read-out without destroying the data, and comparatively low cost. Conversely MOSFET based sensors have low radiation sensitivity if fabricated in commercial CMOS processes with thin gate oxide. To obtain all the advantages listed above, especially the ability to integrate with other circuit components, RADFET sensors are selected to be developed and implemented for the wireless dosimeter. In the following sections the structure, operation, and technology evolution of the RADFETs are presented in detail.

2.4.1 Radiation Field Effect Transistor (RADFET)

The basic structure of a RADFET, as shown in Figure 2.5, is identical to a common metal oxide semiconductor (MOS) transistor. Higher radiation sensitivity is usually achieved by increasing the thickness of the gate oxide or by applying a high bias voltage to a specially fabricated control gate.

Principal of Operation:

When the RADFET is exposed to ionizing radiation such as radon, gamma rays, or x-rays, it generates electron-hole (e-h) pairs in the gate oxide. Electrons are absorbed by the large positive voltage bias applied on the gate of the RADFET and the holes are trapped at Si / SiO_2 (device channel / gate oxide) interface accumulating a charge Q_{0t}. Trapped holes shift the threshold voltage V_T negatively i.e. making it harder to induce a channel. This change in the threshold voltage is used to measure the quantity of the incident radiation.

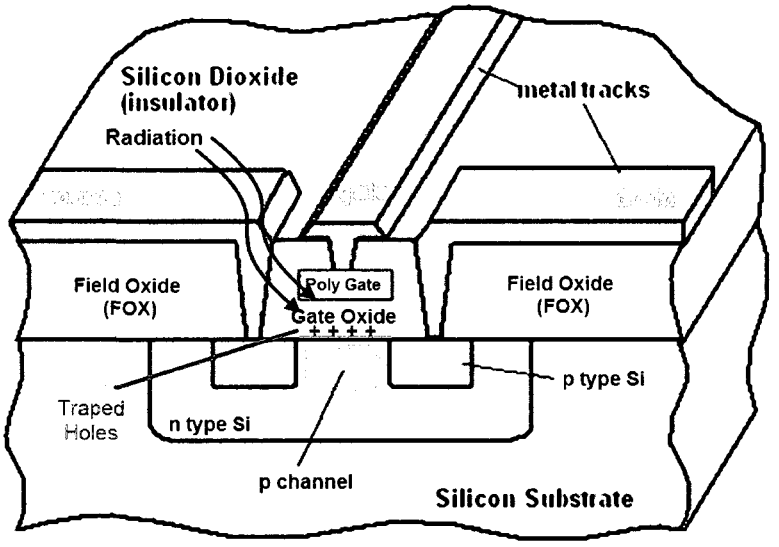


Figure 2.5 Radiation field effect transistor (RADFET)

Radiation Sensitivity

As described in [33], a one-dimensional capacitor model of the MOSFET can be used to derive the relationship between the radiation dose and the shift in threshold voltage (ΔV_T). The oxide trapped charge, Q_{ot}, causes the change in threshold voltage as,

$$\Delta V_T = -\frac{Q_{ot}}{C_{ox}} \tag{2.1}$$

where $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the capacitance per unit area of oxide, with ε_{ox} permittivity, and t_{ox} thickness.

From [33], the dependence of Q_{ot} on absorbed dose D is,

$$Q_{ot} = \frac{q\rho_{ox}\, t_{ox}\, Df}{W_{e-h}} \tag{2.2}$$

where,

W_{e-h} = *electron-hole pair creation energy (18eV)*

ρ_{ox} = *oxide density*

t_{ox} = *gate oxide thickness, and*

f = *fraction of radiation generated charge trapped at interface*

According to [34], f is initially rapidly varying function of the electric field in the oxide as shown in Figure 2.6.

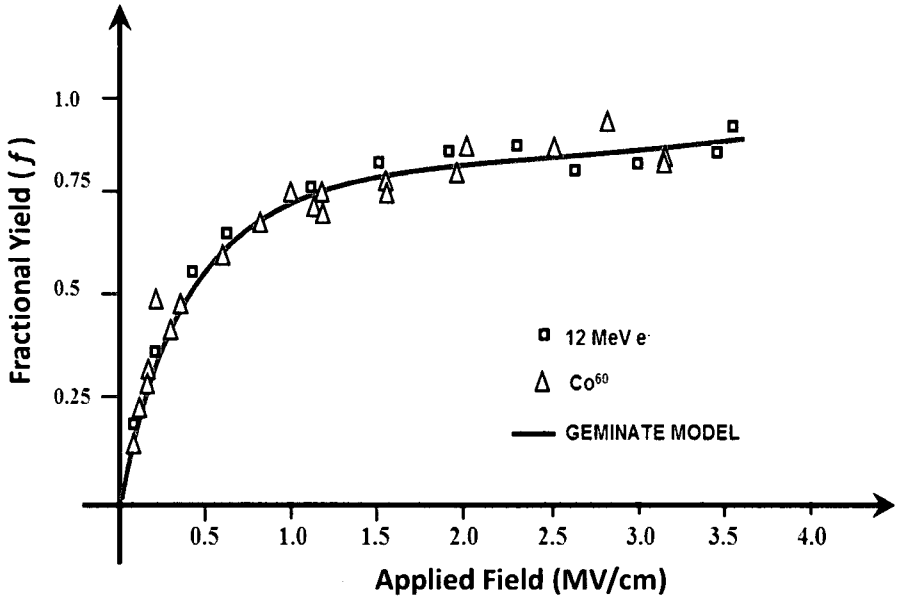


Figure 2.6 Fractional yield vs. electric field in the gate oxide [34]

Combining (2.1) and (2.2) yields,

$$\Delta V_T = \frac{q\rho_{ox} t_{ox}{}^2 Df}{\varepsilon_{ox} W_{e-h}}$$

Which reveals that $\Delta V_T \propto t_{ox}{}^2$ (2.3)

Hence a thick oxide is required for high sensitivity. In conventional CMOS processes with oxide thickness less than 10 nm the sensitivity will be less than 4 μV/rad. This is extremely low for radiotherapy applications. Hence either a micro volt resolution amplifier or a higher sensitivity device is needed. To obtain reasonable sensitivity, conventional RADFETs must use custom processing to grow a thick gate oxide which is expensive.

2.4.2 Floating Gate RADFET

Conventional RADFETs require continuous bias to achieve high sensitivity. A Floating Gate (FG) RADFET, as illustrated in Figure 2.7, eliminates the need for continuous high bias at the gate terminal.

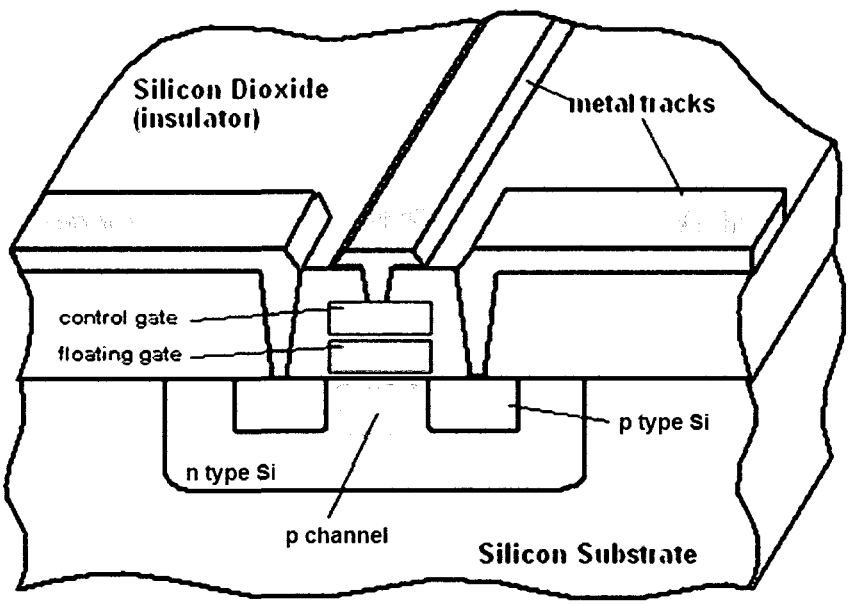


Figure 2.7 Floating gate RADFET

This design has replaced the oxide hole traps with an electrically floating polysilicon gate. The floating gate is made insulated on all sides by thermal oxide. The floating gate is pre-charged to a high voltage prior to irradiation. Pre-charging can be done by UV light or by electron tunnelling phenomena by introducing a pre-charging gate, called injector gate, as shown in Figure 2.8.

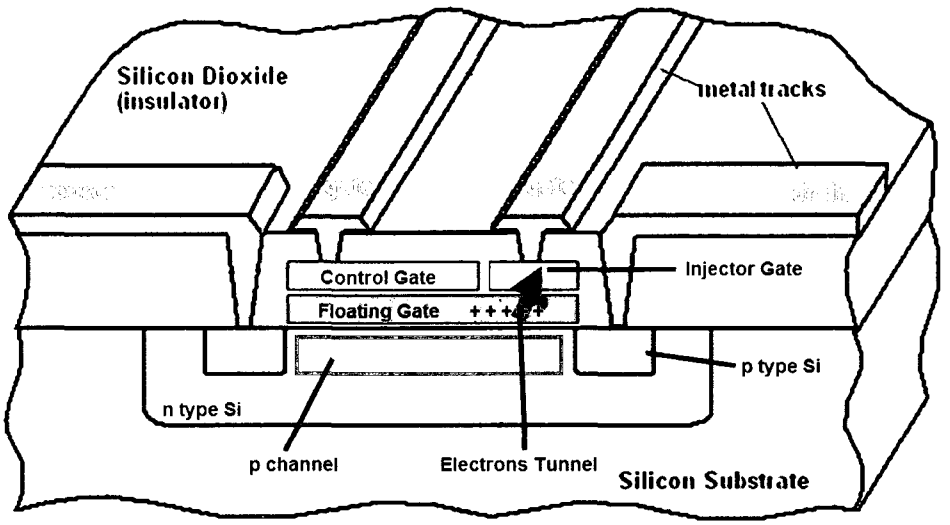


Figure 2.8 Electron tunneling to pre-charge floating gate through Injector gate

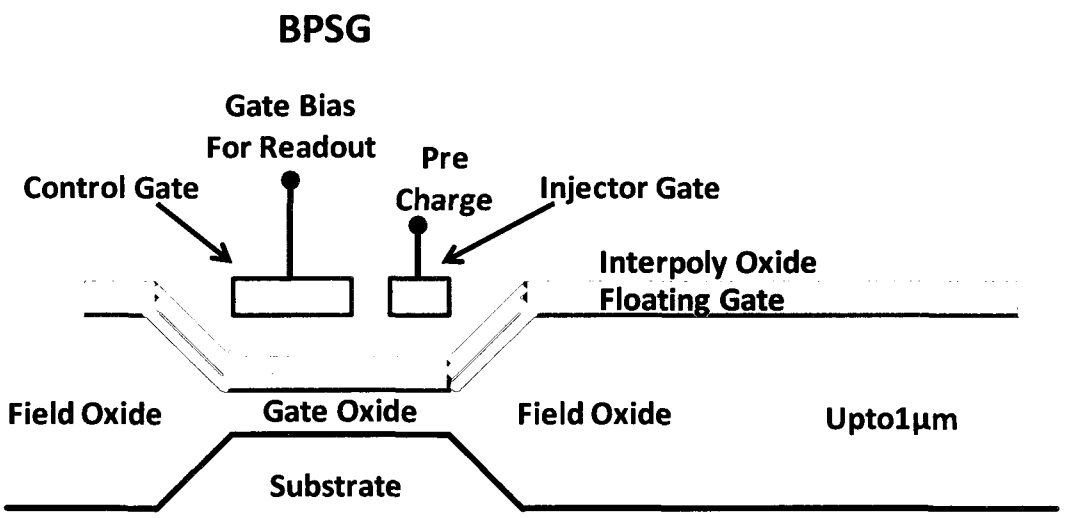


Figure 2.9 Cross section of the floating gate RADFET

Radiation generates e-h pairs in the oxide which discharge the floating gate, hence the threshold voltage is lowered, making the device channel easier to form. The change in threshold voltage is the measure of the amount of incident radiation. The advantage is we need no extra bias during the irradiation process.

The floating gate RADFET requires two polysilicon gate layers, which is a common structure in analog CMOS; hence, normal cost-effective foundry fabrication is possible. But still a thicker gate oxide is needed for measurable sensitivity, which is not available through commercial CMOS fabrication processes.

2.4.3 Modified floating gate structure

To enhance the sensitivity of the RADFET within the limitations of a standard CMOS fabrication process, several modifications and alterations have been made to the basic FGRADFET by Dr. Garry Tarr et. al. over last several years [35, 36]. After all those modifications, the recent form of the FGRADFET is illustrated in Figure 2.10.

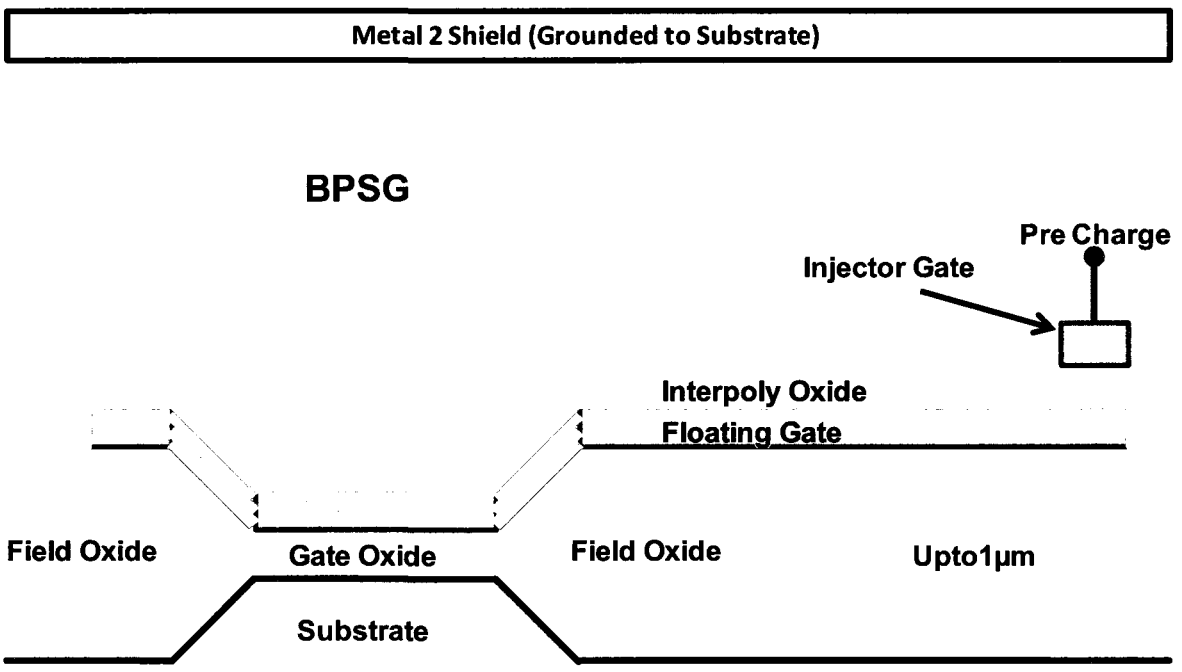


Figure 2.10 Modified floating gate RADFET [36]

Key structural and functional differences between the basic FGRADFET (as in Figure 2.9) and the most recent one as in Figure 2.10 are,

a. Extended floating gate over field oxide (FOX) to accumulate charges and increase sensitivity. Even in most advanced CMOS processes FOX is thick enough to provide measurable sensitivity.
b. Removal of control gate to reduce capacitance to the floating gate for increased radiation sensitivity. The floating gate must be charged so as to create a conducting channel (negative charge for a PMOS device). In this situation we do not have any direct way to measure V_T. Hence radiation is sensed as a change in channel current I_D. However, I_D is a strong function of temperature, hence temperature compensation is needed. First order temperature compensation is achieved using a same size MOSFET reference transistor.
c. Electrostatic shielding of the floating gate to insulate the poly-silicon from overlaying metal with boro-phospho-silicate-glass (BPSG).

2.4.4 Important RADFET parameters

Radiation Sensitivity:

Radiation sensitivity is the amount of change in the RADFET output (voltage or current) with respect to the incident radiation dose. This is the most important parameter of a RADFET. Traditionally sensitivity is measured in mV/rad which refers to the change in the threshold voltage (V_T) of the RADFET due to the incident radiation dose in rads.

Long Term Fading and Endurance:

Another important parameter in obtaining a RADFET suitable for radiation dosimetry is long term-fading. The long term fading is defined as the loss of information about dose when the RADFET is removed from the ionising radiation. This needs to be minimised for some applications, such as personnel dosimetry. However, in other applications it is not as significant. At room temperature the fading with time is very small.

Read-time Stability:

Read-time stability is another important parameter. When the dosimeter is powered-up in the measurement circuit, trapped charges near the Si/SiO_2 interface may either accumulate or dissipate and this causes the output voltage, Vo, to either increase or decrease. This in turn will give a variation in the estimation of the absorbed dose measurement, depending on the rate of change of trapped charge.

2.4.5 Flicker (1/f) noise and RADFET resolution

Almost all the effort to increase the sensitivity of the RADFET devices is focused on increasing the gate oxide thicknesses (t_{ox}). Values of t_{ox} as high as 2.3 mm have been reported [37], providing sensitivities up to 3.8 VGy^{-1} (38 mV/rad) with appropriately large gate bias. However, increasing t_{ox}, reduces oxide capacitance (C_{ox}) that in turn raises the output noise power, so the gains in resolution obtainable with thicker oxides are not as large as might be expected [38]. Obtaining high resolution in a dosimeter requires that attention be given not only to sensitivity, but also to the factors limiting the minimum change in V_T, that can be detected. The role of flicker noise in RADFET devices limiting the minimum resolvable dose has been described in [38]. It is mentioned that dosimeter resolution can be improved by reducing I/f noise in the sensors. The flicker noise current at the drain of a MOSFET in units of A^2/Hz can be expressed as [39],

$$I_{nfo}^2 = \frac{kT{I_D}^2}{\gamma fWL}\left(\frac{1}{N} + \alpha'\mu\right)^2 N_T(E_{fn}) \qquad (2.4)$$

where γ is the attenuation coefficient of the electron wave function into the oxide, α' is their scattering coefficient, $N_T(E_{fn})$ is the number of traps at the quasi-Fermi level, W and L are channel width and length, f is frequency, μ is the charge mobility, I_D is the drain current, and k is Boltzmann's constant.

Considering the relationship (2.4), it is suggested in [38] that flicker noise can be reduced through the use of larger device channel areas (maximum WxL), the use of a MOS fabrication process optimized for low noise, or, the use of a buried channel sensor structure.

2.4.6 Floating Gate RADFET Programming

The act of charging the floating gate to a desired voltage level is called FG programming. In this section three techniques frequently used for programming FG devices are presented.

UV-conductance

The charge stored on the floating gate is protected by an energy barrier provided by the insulating silicon dioxide. The classical mechanism for making silicon dioxide conductive is by using short-wave ultra-violet light, known as UV-C. The nominal wavelength of the light source should be 254 nm emitting high-energy light. Exposing silicon dioxide to UV-C generates free electron–hole pairs with sufficient kinetic energy to surmount the silicon dioxide energy barrier fencing in the floating-gate charge. The efficiency of UV-light conductance is not high since the UV-activated current through silicon dioxide is very small.

Fowler–Nordheim (FN) Tunneling

Another well established technique for charge transport through silicon dioxide is called Fowler–Nordheim (FN) tunnelling, after the first researchers who pointed out (in 1928) that electrons may tunnel through an energy barrier provided a sufficient electric field. The silicon dioxide shields the floating-gate charge with a 3.2 eV energy barrier. The strength of this barrier is proportional to the thickness of the silicon dioxide and determines the strength of the electric field required for tunneling of particles to occur. The FN tunneling is applicable to most structures insulated by a thin layer. Thicker insulating layers can also be used, but the voltage across the oxide must be raised accordingly. An inherent problem of FN tunneling is the texture of most insulators grown on silicon leaving a variable thickness. FN tunneling is an exponential function of both field and insulator thickness, leaving most of the current flow to the thinnest spots of the insulating silicon dioxide. These local high current spots are called "hot spots", since the current may locally be so high that the silicon diamond lattice is broken, leaving open traps for free carriers. The long-term effect is called "wear-out" of the silicon dioxide, making it leaky. Wearing out the silicon dioxide is the fundamental reason for a limited number of reprogramming cycles of floating gate devices. FN tunneling may be fast, provided sufficient electric fields across the silicon dioxide. Programming is usually carried out in a fraction of

second. Top and side view of a typical structure using FN tunnelling to program PMOS FG devices is illustrated in Figure 2.11. The trade-off between speed and wear-out is evident; faster programming implies higher fields, but increased damage to the silicon dioxide. A simple relationship to calculate the FN tunnelling current I_{fn} as given in [40] follows.

$$I_{fn} = C_1 WL(E_{ox})^2 e^{-E_o/E_{ox}} \tag{2.5}$$

Where C_1 and E_o are constants, W and L are width and length of the FG device, and E_{ox} is the electric field across the gate oxide.

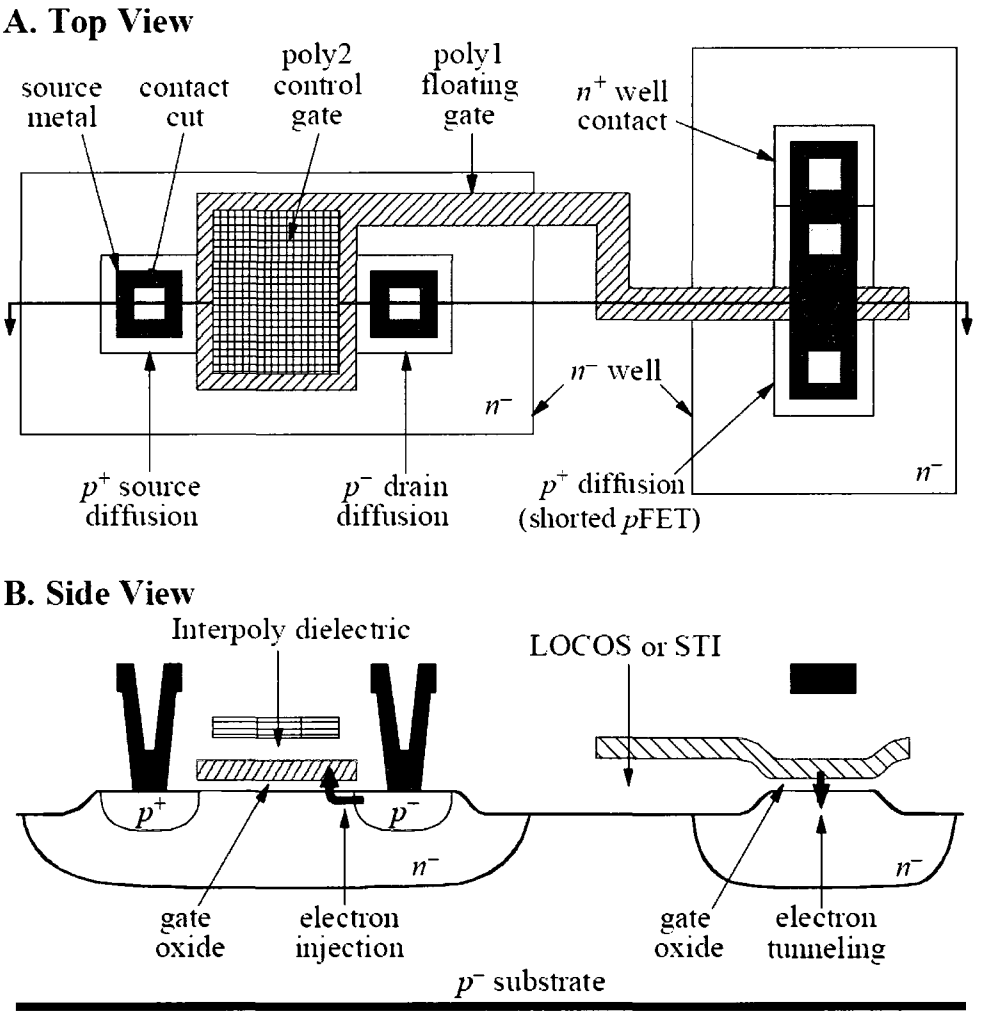


Figure 2.11 (A) front and (B) side view of PMOS HCI and tunneling structures with a PMOS structure at the left explaining HCI and tunneling structure to the right [41].

Hot Carrier Injection (HCI)

The most complicated method for charge transfer is the hot carrier injection (HCI). The idea is to produce free carrier, with sufficiently high energy in the channel underneath the gate. Carriers with sufficient energy (>3.2 eV) to tunnel through the thin gate oxide are called "hot carriers". Due to collisions in the channel, the free carriers will scatter in random directions and a fraction of them will accidentally tunnel through the gate oxide. In Figure 2.11, the current from the channel near the drain terminal towards the FG of the PMOS device is showing HCI. Normally HCI is not observed in standard (non-FG) MOS-transistor because the electric field in the gate oxide makes the carriers bounce back to the channel. To help this process an electric field towards the gate is provided. Looking closer at the transistor channel, we find the hot carriers located close to the drain side. The HCI technique may be used to implement fast transfer of gate charge, but usually required fairly high channel currents. Consequently the desired electric field in the gate oxide is not always easy to establish without special processing steps.

In this work, the metal shields over the floating gates of the FGRADFETs to collect additional charge from BPSG is opaque to the UV light, hence, do not permit the programming of FG devices using UV light. Furthermore, to avoid the high current levels needed for HCI, programming of the dosimeter FGRADFETs in this work has been achieved through FN tunnelling using similar programming structures as illustrated in Figure 2.11.

2.4.7 Charge Stability:

FGRADFET devices tend to lose charge immediately after programming. This is a known issue [42, 43]. Depending on charging conditions and FG device physical characteristics, a variable amount of time is needed before the charged devices settle down to a stable value or before the fading effect is sufficiently low that it can be calibrated. In other cases it may be insignificant for high dose measurements like in radiotherapy applications. Different solutions have been suggested in the literature to avoid this instability issue or to get the device stable quickly, but no detailed theoretical analysis or experimental study are available to address this issue. [36] has suggested to store the FG devices for a long time after programming to achieve

stability. In [42], it is shown that the FG devices can be stabilized faster by annealing. In this work, detailed experimental analysis of FGRADFET stability and stabilization techniques is performed and presented in chapter 3.

2.4.1 Comparison of RADFET Sensors

In Table 2.5 a comparison is presented of existing radiation sensors that either employ a similar technology or have comparable sensitivities to the sensors developed in this work. Most of them [3, 4, 5, 43] are either fabricated in a specialized process to attain thicker gate oxide or use high bias voltages to enhance the sensitivity [21, 33, 43]. Most of the devices are compared against their sensitivity at zero bias for a fair comparison. In the cases where zero bias sensitivity is not mentioned, the applied bias voltage is included [21, 33, 43]. Our work will focus on the improvement of radiation sensitivity of the FG type dosimeters using standard CMOS process.

Table 2.5 Comparision of Radiation Sensors

	[3]	[3]	[4]	[21]	[33]	[35]	[36]	[43]
Technology	Custom Process	Custom Process	Custom Process (TOT-500)	Unknown Process	1.2 µm BICMOS	1.5 µm, CMOS	1.5 µm CMOS	Unknown Process
Irradiation Bias	-	-	0	5-20	12	0	0	5
Sensor Size (µm)	-	-	-	2x2 mm Active 200x200	2.4x1.2	20x20 Active, 50x200 Fox	20x20 Active, 100x400 Fox	-
Device Type	RADFET	RADFET	RADFET	RADFET	FG MOSFET	FG MOSFET	FG MOSFET	RADFET
Sensitivity (mV/rad)	0.5	1.5	0.18	1.0 - 2.7	- 4 nA/rad	0.7	3	6
t_{ox} (nm)	400	1000	250	-	-	27	27	1000
Fox (nm)	-	-	-	-	-	600	1000	-
Min Dose (rad)	40	13	10		-	-	0.5	-

2.4.2 Dosimeter Read-out Circuit

In Figure 2.12, a conventional dosimeter system is presented [38]. It consists of two sensor MOSFETs and associated read-out circuitry. One sensor is acting as a reference for first order temperature compensation. The irradiation and read cycles are controlled by means of a microcontroller and solid state switches. Discrete components not being matched in this setup introduce error in the output and the circuit is subject to temperature and environmental variations.

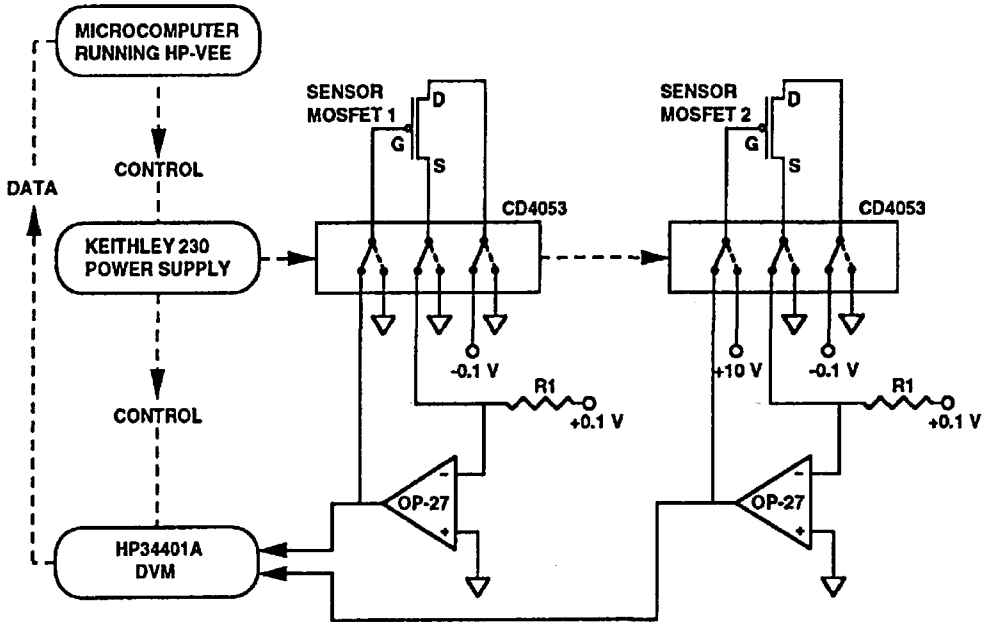


Figure 2.12 Conventional dosimeter sensor system with readout circuit [38]

Another dosimeter circuit based on the FGRADFET with no control gate is presented in [36], as shown in Figure 2.13. Without a control gate, the only means available to infer the charge on the floating gate is to measure the drain current I_D. However, I_D has significant variations with temperature change. To compensate for the variation in I_D with temperature, the sensor MOSFET is combined with a reference MOSFET having identical channel length and width as shown in the figure. The operational amplifier modulates the gate bias of the reference MOSFET until V_{DS} for the reference and sensor are equal. Due to the use of off chip components such as bias resistors (R1 and R2) and operational amplifier, this circuit will translate any mismatch in the component values to the output voltage.

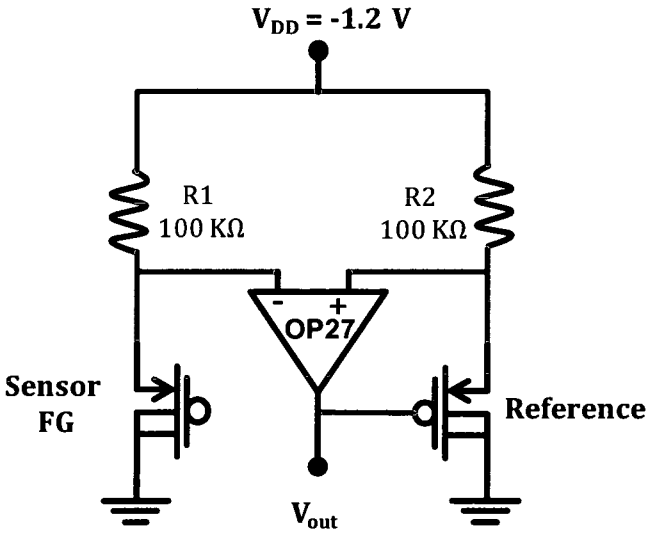


Figure 2.13 FGRADFET dosimeter circuit [36]

This work will integrate all the components on a monolithic dosimeter chip to obtain precise and accurate measurements of radiation dose by essentially eliminating the mismatch in values of read-out circuit components.

2.5 SoC Receiver

Wireless communications have been developed for more than a century, evolving from all discrete-component implementations to highly integrated systems. In a wireless communication system, the receiver is responsible for processing the signal collected from the receiving antenna to regenerate the transmitted signal. There are several classical receiver architectures such as super-heterodyne, direct-conversion and super-regeneration. Usually different receiver architectures match different applications depending on the system complexity, power consumption, external component count and system cost. Several choices of receiver architectures are available with advantages and limitations associated with each style. Phase Lock Loop (PLL) based receiver front ends remains a common choice for most RF designers. Recently, the Delay Locked Loop (DLL) based receivers are gaining popularity due to their simplicity and inherent performance advantages [44-45]. A simple block diagram of the proposed DLL based SoC receiver is shown in Figure 2.14 and the review of its key components follows.

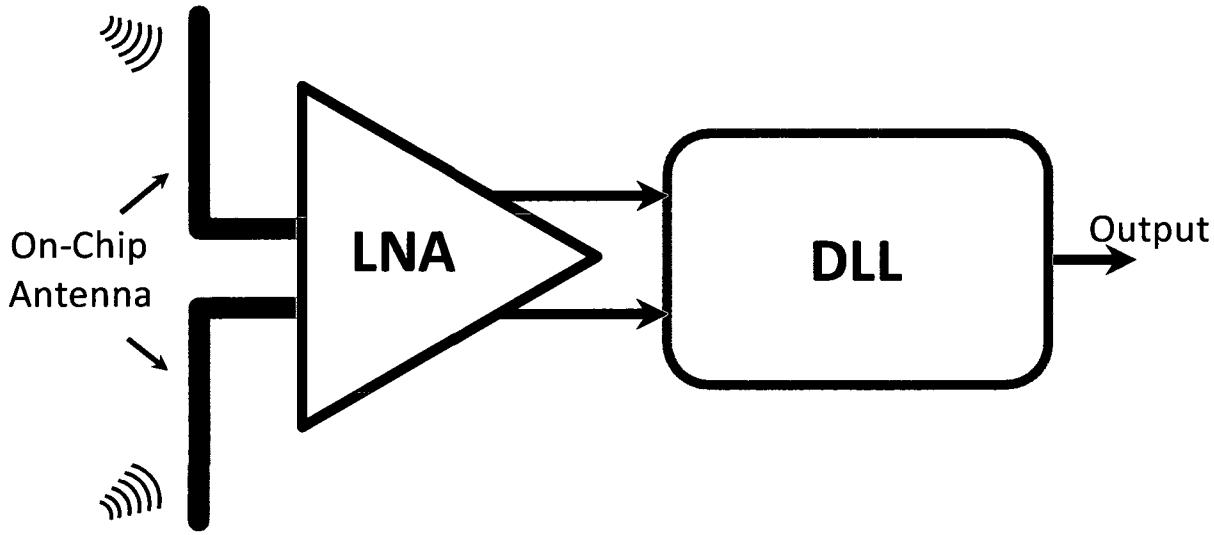


Figure 2.14 Simplified SoC RX block diagram

2.5.1 LNA with On-chip Antenna

The first two front end components of the SoC receiver are the antenna and the LNA. Receiving efficiency of the antenna, along with low noise and high gain of the LNA, are essential for any RX system and have a direct impact on the performance of the overall receiver. Monolithic integration of transceiver circuits on a single chip has been a long-awaited dream of RF designers. Recently, the performance improvement in advanced CMOS technology has paved the way for RF components integration with analog and digital on a single chip [46-48]. These scaled-down CMOS devices exhibit high cut-off frequencies, high performance integrated passives and operate at lower voltages. This progress of RF CMOS technology has motivated System-on-Chip (SoC) designs for highly compact handheld and portable devices. The attractiveness of these systems is that they can offer low cost, small physical size and low power consumption This concept has been widely accepted in applications like Wireless LAN and Bluetooth and is making inroads to cellular transceivers and GPS receivers [49]. It has also found its utility in many modern wireless sensor networks [50]. Though substrate noise coupling and low Q passives in standard low resistivity bulk silicon are still a challenge for efficient SoC implementation, highly integrated components and transceiver systems have none the less been successfully demonstrated [51-52]. Table 2.6 summarizes the characteristics of LNA with on-chip antenna, which is the focus of this receiver work.

Table 2.6 Comparison of LNAs with On-chip Antenna

	Freq (GHz)	Antenna Radiation Pattern	Size of Antenna (mm^2)	Size of Chip (mm^2)	Technology (μm)	LNA Gain (dB)	NF (dB)	Power (mW)
[53]	**77**	**Yes**	-	**6.8x3.8**	**.13 BiCMOS**	**23.8**	**5.7**	-
[54]	**24**	**Yes**	**2.1x0.75**	**2.3x2.3**	**0.8 SiGE**	-	**6.6**	**340**
[55]	**9.3**	**No**	**0.55x0.55**	-	**0.13**	**-10**	-	**15**
[56]	**5.0**	**No**	**0.6x0.67**	**2.75x1.45**	**0.13**	-	-	**6.6**
[57]	**60**	**Yes**	**0.9x-**	**1.6x2**	**0.13**	**18**	**5.8**	**17.8**
[58]	**20**	**No**	**3x0.12**	**.88x.83+Ant**	**0.13**	-	**7.2**	**7.3**
[59]	**140**	**Yes**	**0.18x0.095**	**.58x.7**	**0.065**	-	**>20**	**100**
[60]	**170**	**Yes**	**0.125x0.12**	**1.52x0.84**	**.13 BiCMOS**	**15**	**21**	**135**
[61]	**220**	**No**	**0.15x0.15**	**3.0x1.0**	**0.1 GaAs**	**11**	**8.4**	-

At present, on-chip antenna integration seems to be the bottleneck in single chip transceiver realization due to its large size at RF frequencies and inefficiency resulting from the lossy Si substrate. The completely integrated Bluetooth CMOS based transceiver SoC in [62] still has off chip components like the reference crystal and antenna. Lately, a 77 GHz phased array transceiver with an on-chip antenna has been demonstrated [53], however, in order to improve antenna efficiency many additional design and fabrication steps are performed. In another example of RF SoC, a 24 GHz receiver with an on-chip antenna is demonstrated but on a high

resistivity SiGe platform [54]. Recently, a 9 GHz [55] and 5GHz [56] slot antenna design has been presented with shielded ground plane to improve the on-chip antenna efficiency. This design, however, occupies large chip space (4 mm^2) and the on-chip antenna has not been optimized to conjugately match the LNA complex input impedance. Moreover the antenna is not characterized for its radiation pattern, which is one of the most important and challenging parts in on-chip antenna design. Low-power and miniaturization are not fully achieved in these designs. The design and challenges of a low power fully integrated DLL based SoC receiver with on-chip antenna suitable for a low power miniaturized wireless sensor node will be addressed in chapter 5.

2.5.2 Delay Locked Loop (DLL)

The signal flow block diagram of a conventional DLL is depicted in Figure 2.15. Instead of a Voltage Controlled Oscillator (VCO) employed in the phase-locked-loop (PLL), DLL uses a voltage-controlled-delay-line (VCDL). In the PLL, the VCO output is proportional to the integral of the input control voltage. However a delay line has an output delay proportional to the control voltage of an integrator. Thus a DLL has a transfer function inherently one order lower than that of the PLL [63].

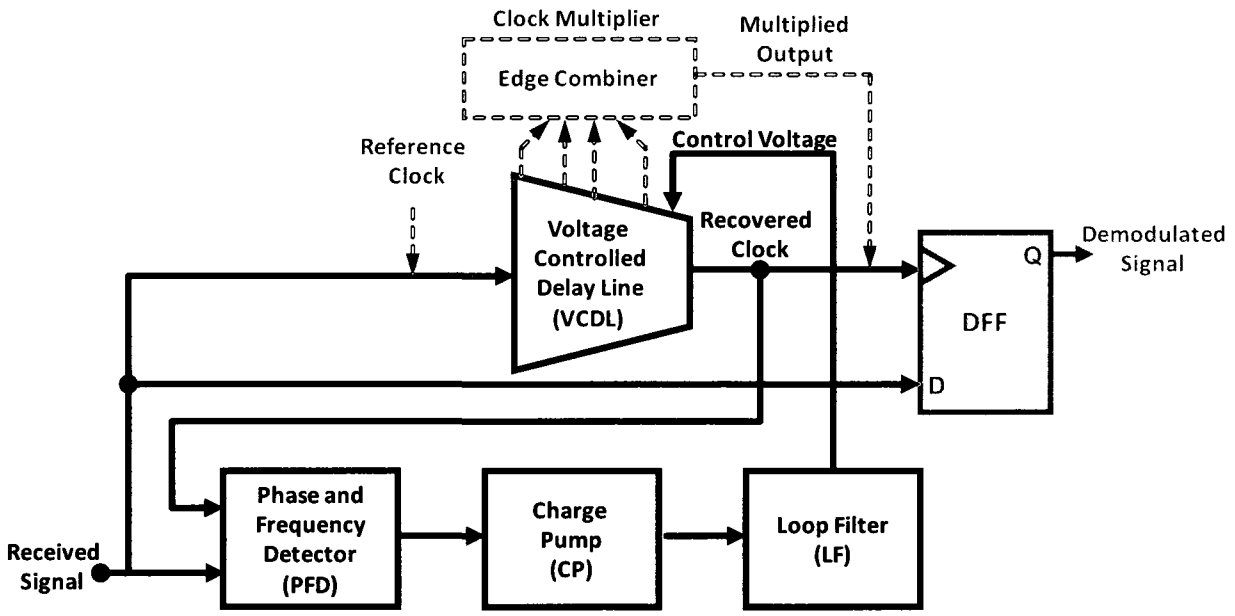


Figure 2.15 Simplified block diagram of a DLL based demodulator

An edge combiner (dotted circuit, in Figure 2.15) is equivalent to a clock multiplier divider in the feedback loop of a PLL. It is needed only when input career frequency is higher than the local clock reference. The output flip flop extracts the digital data from the incoming signal by removing the carrier frequency component using recovered or local clock reference.

Advantages of DLL based RX

DLL is a relatively recent innovation, first found in Dr. Combes' work [64] in the early 1990s, then popularized by Xilinx in their Virtex family of FPGA products [65]. Compared to PLLs, DLLs do not accumulate jitter. For this reason, the DLLs are inherently less noisy than the PLLs. The DLL is a stable first order system. The locking time of a DLL is faster and the loop filter is easier to design and integrate than in a PLL [63]. DLLs are generally easier to design. However, a DLL is more dependent on the reference signal than is a PLL, and its locking range is limited.

Classification of DLL

According to the principle of phase shift generation, DLL architectures can be divided into three classes: analog, digital, and hybrid (which is usually referred to as dual loop) [66]. Figure 2.16 illustrates all three types of DLL loops.

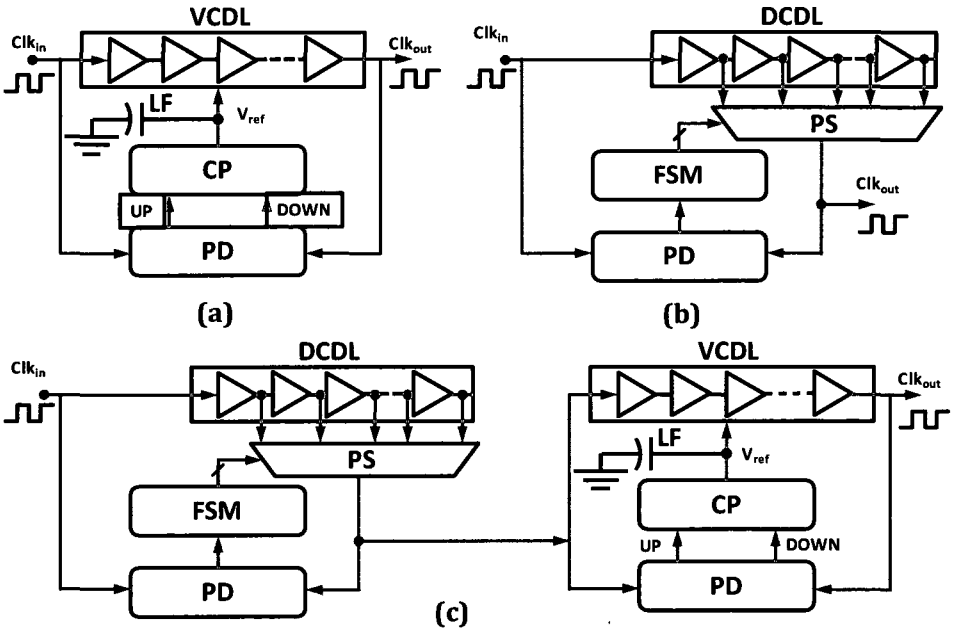


Figure 2.16 Classification of DLL (a) analog, (b) digital, and (c) hybrid [66]

The analog DLL as illustrated in Figure 2.16(a) consists of a voltage controlled delay line (VCDL), phase detector (PD), charge pump (CP), and first order low-pass filter (LPF). The VCDL is composed of several variable delay elements connected in cascade. The reference clock drives the input of VCDL. In order to determine the phase alignment error, the PD compares the rising edges of input and output signals. The CP and LPF act as an integrator, and generate a control voltage. When correctly locked, the total delay of the VCDL should be equal to one period of the reference clock. Analog DLLs are suitable for fine-grain delay variation. They are efficient in applications where small, accurate, and precise amount of delay is necessary to be achieved.

The digital DLL shown in Figure 2.16(b) consists of a digitally controlled delay line (DCDL), phase selector (PS), phase detector (PD) and finite state machine (FSM). The DCDL is implemented as a delay element chain of variable length. The number of elements in a chain determines the amount of the delay. The PS is realized as a multiplexer. At its output pulse of defined phase-shift (delay) is selected [67]. The FSM's output defines the amount of a delay. Delay elements, in DCDL, provide fixed and quantized time delays, and they are used for coarse-grain delay variation in a wide range of regulation. This means that the digital DLL quantizes the clock signal into several coarse-grain discrete delay steps.

The dual-loop DLL, sketched in Figure 2.16(c) is composed of a digital and an analog DLL connected in series [68]. In general, the dual-loop DLL provides a wide operating phase-shift range. Jitter performance is not good enough, because the clock propagation path includes two loops with a large number of delay elements. Hardware complexity and power consumption of the dual-loop DLL are high [69].

Because of the simplicity required in this work, we will use analog DLL to design the receiver.

2.5.3 Performance comparison of DLL based receivers

The performance of some recent DLL based designs has been compared in Table 2.7. Important parameters of a DLL besides the frequency of operation are jitter and power. Most of these receivers consume significant power [70, 71, 72] (i.e. more than 10mW) that is not suitable for portable wireless applications. Furthermore none of these designs qualifies as a SoC solution in

the absence of an on-chip antenna. To address all these weaknesses in the available state of the art RX designs, a low power full differential analog DLL based SoC receiver with an on-chip antenna suitable for our wireless sensor application will be presented in chapter 5.

Table 2.7 Performance Comparision of DLL based Designs [70]

	[70]	[71]	[72]	[73]
Process (μm)	0.13	0.09	0.18	0.18
Supply (V)	1.2	1	1.8	1.8
Frequency (GHz)	0.5-5	2-5	0.9-2.9	0.25-2
RMS Jitter (ps)	1.06 @5GHz	0.87 @5GHz	1.62 @2.16GHz	2.81 @2GHz
Jitter-pp (ps)	8 @5GHz	7.56 @5GHz	12.9 @2.16GHz	20 @2GHz
Power (mW)	36	45	19.8	6.4
Area (mm^2)	0.107	0.121	0.27	0.046

2.6 Summary

In this chapter an overview of the proposed wireless dosimeter has been given. The design and performance of existing wireless dosimeters components (radiation sensors, DLL, RX) has been presented and compared. A literature review has been conducted that justifies the fundamental design decisions in this work.

Chapter 3

Novel RADFET based Dosimeters

In accordance with the first four research objectives, a novel low power dosimeter architecture is presented in this chapter. In addition, the design of an enhanced sensitivity floating gate sensor is described. Three novel dosimeter designs for improved accuracy and radiation sensitivity are presented. Finally a performance comparison of the new dosimeters with previously reported designs is performed.

3.1 Dosimeter Architecture for Low Power Wireless Applications

The FGRADFET dosimeter architecture presented in [36] and discussed in section 2.4.2, has a trade off between supply voltage and sensitivity. If the FGRADFET is programmed at a high voltage for better sensitivity, this architecture requires a high voltage supply to be able to produce equivalent FG voltage at its output. Or if the FGRADFET is programmed at a lower voltage to facilitate the use of low supply voltage, the dosimeter will compromise on its sensitivity. Low voltage operation of the dosimeter without compromising sensitivity can be achieved if the reference MOSFET is replaced by an identical floating gate transistor (FGRADFET) reference without extension over the field oxide (FOX). Without gate extension over FOX the reference FGRADFET will lose most of its sensitivity to the incident radiation. Both the FG sensor and reference transistors are pre-charged to the same value. While irradiated, the FG sensor discharges proportionally to the amount of incident radiation dose, whereas charge on the FG reference ideally remains the same. Bias voltage, as little as 0.1 V, can be

applied to the drain terminal of the two FG transistors to observe the channel currents. This novel dosimeter idea is illustrated in Figure 3.1.

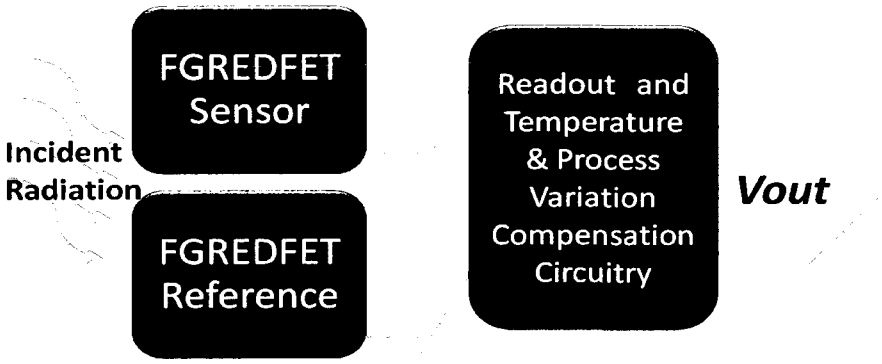


Figure 3.1 Proposed dosimeter block diagram

Current from both the devices can be compared by a readout circuitry to determine the amount of radiation dose received. A fully differential dosimeter structure having both reference and sensor devices as electrically identical FGRADFETs, helps to compensate the first order variations in the current with respect to the change in temperature. The architecture also rejects other on-chip gradient effects.

3.2 Modified FGRADFET Structure

The RADFET structure discussed in section 2.4.3 has been optimized to achieve better sensitivity. The modified structure is shown in Figure 3.2. The differences are (1) the removal of the double-poly injector gate replaced by a single-poly FG charging mechanism similar to the electron tunnelling structure discussed in section 2.4.6, and (2) the use of metal 3 (M3) shielding as opposed to metal 2 (M2) previously reported in [36]. From the results presented in [33] it is known that any capacitance to the floating gate decreases the dosimeter sensitivity. The injector gate has been removed from the floating gate. This reduces the overall capacitance on the floating gate and increases the sensor sensitivity. The floating gate is pre-charged by drain tunnelling from a charging structure placed on the side, as shown in Figure 3.2(b). The use of a single poly structure is also consistent with modern CMOS processes, most of which offer only one poly-silicon layer. The tunnelling structure does add some capacitance to the FG but it is negligible compared to the poly injector gate. The use of elevated metal 3 increases the

effective BPSG volume for the radiation to produce e-h pairs. The effect of both the changes will be analysed in detail later in this chapter. The dosimeter has been fabricated in a standard thick-oxide 0.8 μm (DALSA) CMOS process. The FG sensor has a large-area extension (100 μm by 80 μm) over the field oxide, as shown in Figure 3.2. The purpose of the extension is to capture radiation-generated charge from the thick field oxide. P-channel transistors are utilized in this work due to their superior 1/f noise performance as compared to the equivalent n-channel transistors. These transistors have channel lengths and widths of 4 μm and 20 μm respectively. The sensors have been fully shielded using poly, metal 1 and metal 3. This avoids the unwanted variation in the floating gate potential caused by the bias applied to other devices on the chip [36]. The microphotograph of the modified dosimeter chip is shown in Figure 3.3. Its overall dimensions are 300 μm x 400 μm.

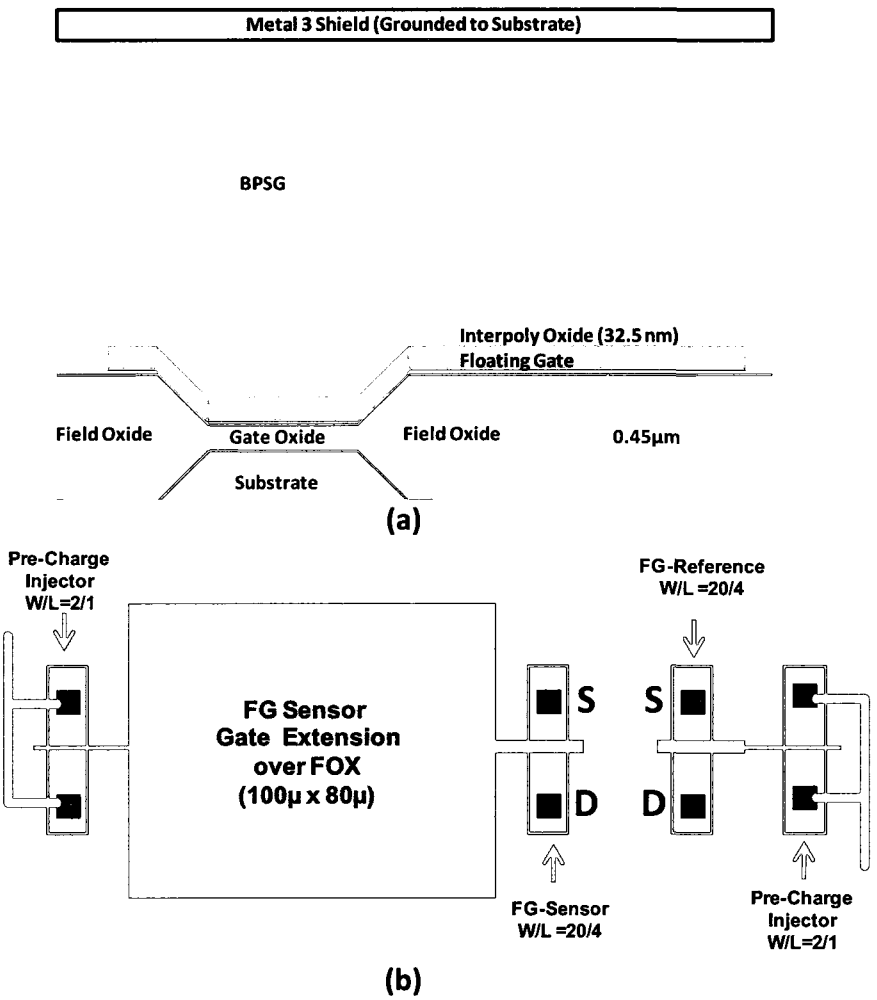


Figure 3.2 Modified FGRADFET structure (a) cross section and (b) top view with FG reference

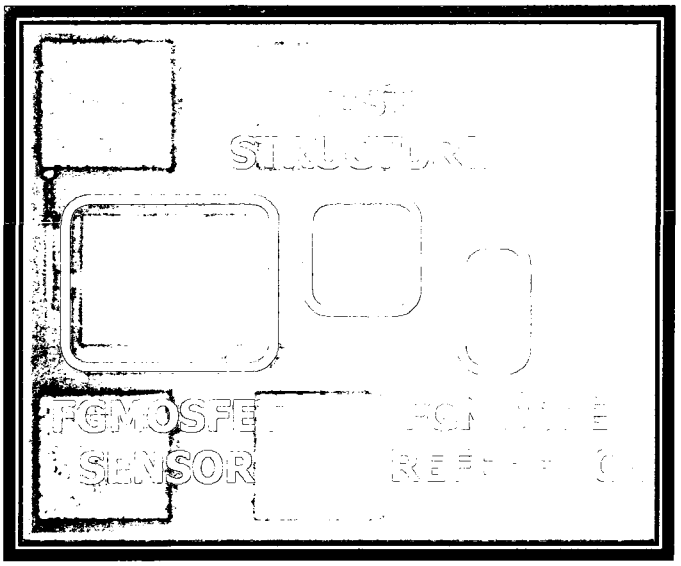


Figure 3.3 Microphotograph of the new dosimeter chip (300 μm x 400 μm).

This design enhances the compensation for the variation in I_D due to temperature and environmental variations by combining the sensor FGRADFET with a reference FGMOSFET for the first time. The floating gate reference is identical to the sensor in terms of channel length and width. However, the sensor has the floating gate extended over the field oxide thus making it more sensitive to the radiation than the reference. Since the two are identical and behave exactly the same way in response to all the variations other than the radiation absorption, the overall system cancels out the first- order temperature and environmental effects more accurately as compared to the earlier designs [36].

This is a new device; accordingly, a detailed analysis of its design and performance has been carried out to fully characterize and understand its behaviour. A mathematical analysis quantifying its sensitivity is presented in the following section, followed by a brief discussion of the design considerations made to minimize the flicker noise. Charging characteristics of the new devices are discussed in detail. Thermal behaviour, stability, and sensitivity have been measured and analysis of the results is presented accordingly.

3.2.1 Sensitivity Analysis of the Modified FGRADFET

The capacitor model and mathematical analysis of the FGMOS sensitivity presented in [33] has been adopted and modified to reflect the modifications in the new FG structure. The sensitivity

of the floating-gate dosimeter depends on the sensitivity of the read-out circuit and the sensor FGRADFET. Circuit sensitivity can be controlled through appropriate circuit design. The FGRADFET sensitivity is a function of its geometry, material properties, and the conditions under which the device is exposed to radiation. Since the material composition and layer thickness are fixed in a fabrication process, then, for a given fabrication process, the sensitivity parameters that can be customized are primarily affected by circuit design.

Circuit Sensitivity

The FGRADFET is a modified MOSFET structure. If the floating-gate voltage is known, the FGRADFET drain current can be determined using a standard MOSFET model. To determine the behaviour of the FGRADFET, the floating-gate potential can be found as a function of other terminal voltages, coupling capacitances, and trapped charges. Since the floating-gate can only be controlled by capacitive coupling, a capacitor model can be used to relate the floating-gate voltage to the other terminal voltages. In Figure 3.4 the capacitor model of the modified FGRADFET is presented with oxide capacitances C_{ox}, C_{fbpsg} and C_{fox}, depletion capacitance C_{dep}, and capacitances between floating gate and rest of the device terminals C_{fs}, C_{fb}, and C_{fd}. The capacitances C_{fc}, and C_{inj} in the dotted circle correspond to the eliminated control and injector gates.

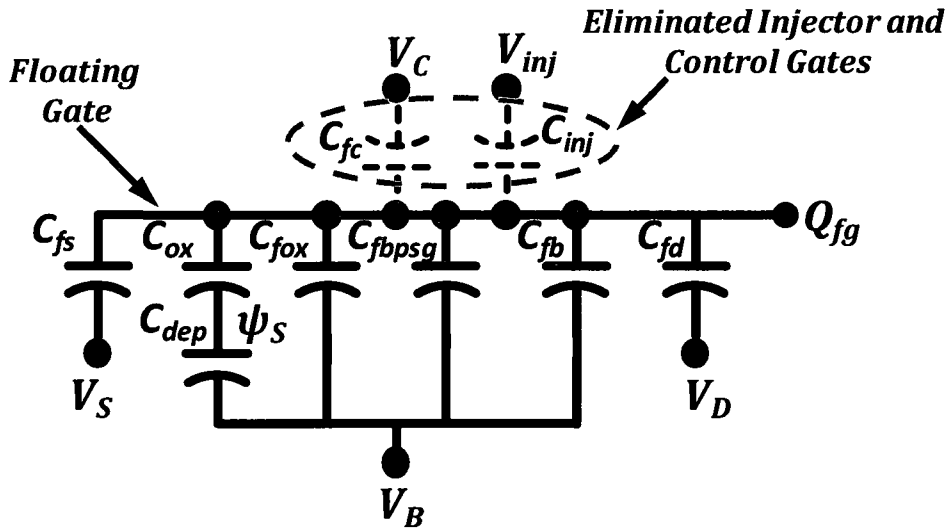


Figure 3.4 Capacitor model for modified FGMOSFET without control and Injector gate and floating gate extended over field oxide

Referencing all voltages to the bulk node V_B, the floating-gate voltage is expressed as,

$$V_{FG} = \frac{V_S C_{fs} + V_D C_{fd} + \psi_S C_{ox'} + Q_{fg}}{C_{sum}} \tag{3.1}$$

where V_S, and V_D are the voltages at the source and drain respectively; C_{fs}, C_{fd}, and C_{fb} are the capacitances from the floating-gate to the source, drain, and bulk, respectively; ψ_S is the surface potential; $C_{ox'}$ is the oxide capacitance; Q_{fg} is the charge trapped on the floating gate; and,

$$C_{sum} = C_{fs} + C_{fd} + C_{fb} + C_{ox'} \quad \text{where } C_{ox'} = C_{ox} + C_{fox} + C_{fbpsg} \tag{3.2}$$

The change in V_{FG} with respect to the change in Q_{fg} is

$$\frac{\partial V_{FG}}{\partial Q_{fg}} = \frac{1}{C_{sum}} + \frac{C_{ox'}}{C_{sum}} \frac{\partial \psi_S}{\partial Q_{fg}} \tag{3.3}$$

For small changes in the floating-gate charge, $\partial \psi_S / \partial Q_{fg}$ will be negligible and (3.3) simplifies to

$$\frac{\partial V_{FG}}{\partial Q_{fg}} = \frac{1}{C_{sum}} \tag{3.4}$$

Using the chain rule, the current sensitivity is,

$$\frac{\partial I_D}{\partial Q_{fg}} = \left(\frac{\partial I_D}{\partial V_{FG}}\right)\left(\frac{\partial V_{FG}}{\partial Q_{fg}}\right) = \frac{1}{C_{sum}}\left(\frac{\partial I_D}{\partial V_{FG}}\right) \tag{3.5}$$

Defining $gm_{FG} = \partial I_D / \partial V_{FG}$ as the trans-conductance of the transistor from the floating-gate, the change in drain current with respect to charge on the floating gate is,

$$\frac{\partial I_D}{\partial Q_{fg}} = \frac{gm_{FG}}{C_{sum}} \tag{3.6}$$

Supposing the FGRADFET is operating in the sub-threshold region, the drain current varies as the exponential of the floating-gate voltage, which leads to the trans-conductance

$$gm_{FG} = I_D \frac{\kappa}{U_T} \tag{3.7}$$

where κ is the sub-threshold slope and U_T is the thermal voltage. The resulting sensitivity is

$$\frac{\partial I_D}{\partial Q_{fg}} = \frac{\kappa I_D}{U_T C_{sum}} \tag{3.8}$$

For above-threshold operation, the drain current varies as the square of $V_{FG} - V_T$ with a proportionality constant of K. Therefore, the trans-conductance is equivalent to,

$$gm_{FG} = 2\sqrt{KI_D} \tag{3.9}$$

Hence the sensitivity in the above-threshold region of the FGRADFET is,

$$\frac{\partial I_D}{\partial Q_{fg}} = \frac{2\sqrt{KI_D}}{C_{sum}} \tag{3.10}$$

FGRADFET Charge-Collection Efficiency

As mentioned earlier, charge collection in the FGRADFET is a function of the device geometry, material densities, and recombination rate of the electron–hole pairs generated by incident radiation. Particles composing the ionizing radiation generate charge by the deposition of energy E_{dep}. The amount of charge created is

$$Q_{gen} = q\frac{E_{dep}}{W_{e-h}} \tag{3.11}$$

where $W_{e\text{-}h}$ (≈18eV) is the electron–hole pair creation energy. If R(E) represents the recombination rate of the e-h pairs, where E is the electric field across the medium, the total charge collected Q_{col} can be expressed as

$$Q_{col} = (1 - R(E))Q_{gen} = f\frac{qE_{dep}}{W_{e-h}} \tag{3.12}$$

where $f = (1 - R(E))$. Assuming the charge trapping oxide region as a parallel plate capacitor of area A and thickness t with a material density of ρ_{SiO_2}, then, the total dose D, which is the energy deposited per unit mass m, will be

$$D = \frac{E_{dep}}{\rho_{SiO_2}At} \tag{3.13}$$

where $\rho_{SiO_2}At = m$. Therefore,

$$E_{dep} = D\rho_{SiO_2}At \tag{3.14}$$

Combining (3.12) and (3.14) gives the total charge collected as a function of dose

$$Q_{col} = \frac{qD(1-R(E))}{W_{e-h}}\rho_{SiO_2}At \tag{3.15}$$

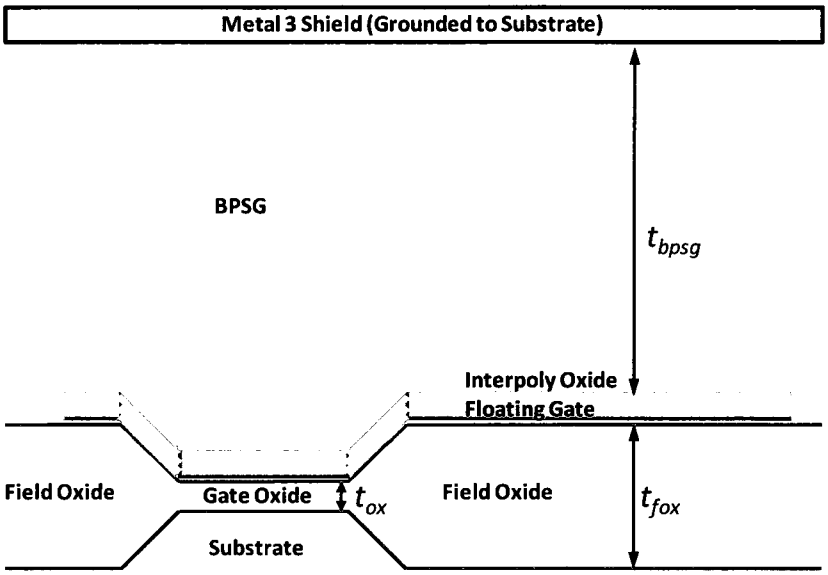


Figure 3.5 Inconsistent charge collection regions, gate oxide, field oxide, and BPSG

As illustrated in Figure 3.5, FGRADFET is an inconsistent collection volume. There are variations in area, thickness, density, and electric field across different portions of the transistor structure. To account for these differences, (3.15) can be generalized as

$$Q_{col} = \frac{qD}{W_{e-h}} \sum_i f_i \ \rho_i A_i t_i \tag{3.16}$$

$$= \frac{qD}{W_{e-h}} (f_{ox} \rho_{ox} A_{ox} t_{ox} + f_{fox} \rho_{fox} A_{fox} t_{fox} + f_{bpsg} \rho_{bpsg} A_{bpsg} t_{bpsg})$$

Where subscripts ox, fox, and bpsg represent gate oxide, field oxide, and boro-phospho-silicate glass regions, respectively.

Combined Sensitivity

From (3.6), the incremental change in drain current can be approximated as

$$\Delta I_D = \frac{gm_{FG}}{C_{sum}} \Delta Q_{fg} \tag{3.17}$$

The change in the floating-gate charge ΔQ_{fg} is simply the collected charge Q_{col} from (3.15). Therefore, the change in drain current as a function of dose is

$$\Delta I_D = q \frac{gm_{FG}}{C_{sum}} \frac{D}{W_{e-h}} \sum_i f_i \ \rho_i A_i t_i \tag{3.18}$$

Examination of (3.18) clearly establishes a design space in which one can work to optimize the sensitivity of the floating-gate dosimeter. Circuit designers generally do not have control of

layer thicknesses or composition. Therefore, t_i and ρ_i are fixed quantities. Recombination rate R is a monotonically decreasing function of electric field E. Therefore, it is advantageous to increase gm_{FG} and A_i while decreasing C_{sum} to maximize the sensitivity of the detector.

Incorporating the value of C_{sum} from (3.2) in (3.18) gives

$$\Delta I_D = q \frac{gm_{FG}}{C_{fs}+C_{fd}+C_{fb}+C_{ox}+C_{fox}+C_{fbpsg}} \frac{D}{W_{e-h}} \sum_i f_i \ \rho_i A_i t_i \tag{3.19}$$

Ignoring the smaller capacitances $C_{fs} + C_{fd} + C_{fb}$,

$$\Delta I_D = q \frac{gm_{FG}}{C_{ox}+C_{fox}+C_{fbpsg}} \frac{D}{W_{e-h}} (f_{ox}\rho_{ox}A_{ox}t_{ox} + f_{fox}\rho_{fox}A_{fox}t_{fox} + f_{bpsg}\rho_{bpsg}A_{bpsg}t_{bpsg}) \tag{3.20}$$

The M3 is shielding approximately twice as far from the floating gate as M2 shield. Hence the expected increase in sensitivity will be

$$\Delta I_D = q \frac{gm_{FG}}{C_{ox}+C_{fox}+C_{fbpsg}} \frac{D}{W_{e-h}} (f_{ox}\rho_{ox}A_{ox}t_{ox} + f_{fox}\rho_{fox}A_{fox}t_{fox} + 2f_{bpsg}\rho_{bpsg}A_{bpsg}t_{bpsg}) \tag{3.21}$$

where the factor of 2 in the bpsg term reflects the increased thickness of BPSG (t_{bpsg}) due to the M3 shielding. This is a key result that arises from the new structure developed in this thesis.

3.2.2 Flicker Noise Considerations

The dosimeter design presented in this dissertation is intended for radiotherapy applications which uses high radiation dose to treat a cancer tumor. The required radiation sensitivity for radiotherapy applications is far from the fundamental sensitivity limit discussed in [38], however, considerations have been given during the design to keep the flicker noise to a minimum within the limitations of the CMOS fabrication process. A p-type FGRADFET has been used as it produces less flicker noise compared to the n-type devices. Also the transistor size has been chosen to maximize the device area (WxL) with the maximum possible FG extension over FOX without violating the "antenna" rules of the process. The maximum allowed ratio of poly gate area (WxL) to the poly connected to the gate is 1:100 in DALSA 0.8 µm CMOS process.

For the FGRADFET sensor in our design, the sensor gate size (WxL) is 20 μm x 4 μm = 80 μm^2 whereas the FG extension over FOX is 100 μm x 80 μm = 8000 μm^2, as shown in Figure 3.2. Consequently the ratio is 1:100. Hence the proposed FGRADFET sensor is designed to obtain minimum flicker noise while still observing the process limitations.

3.2.3 FGRADFET Programming (pre-Charging) Mechanism

As described previously, the modified FGRADFET poly injector gate has been replaced with an electron tunnelling structure similar to a MOSFET with source and drain terminals connected together. The top view of the FGRADFET with FG programming structure is illustrated in Figure 3.6.

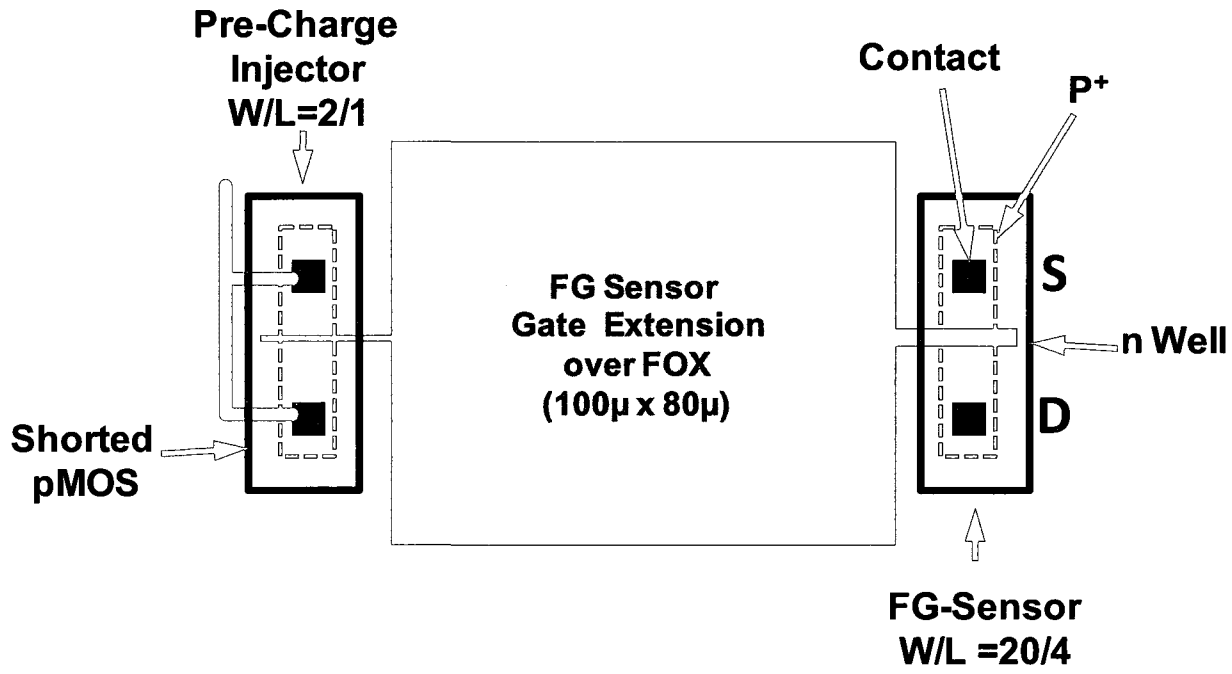


Figure 3.6 Top view of the FGRADFET and PMOS tunneling structures for programming

A Fowler-Nordheim tunneling phenomenon is used to increase the charge on the floating gate. A voltage difference between the tunneling junction, the shorted PMOS in Figure 3.6, and the floating gate causes the electrons to tunnel through the PMOS's gate oxide to the floating gate. The magnitude of this tunneling current depends on the oxide voltage. As mentioned in [41], this current can be approximated as,

$$I_{tun} = -I_{tun\,0} WLe^{-\frac{V_f}{V_{ox}}} \quad (3.22)$$

where I_{tun0} is the pre-exponential current, V_{ox} is the voltage across the oxide, V_f is a constant that varies with oxide thickness, and W and L are the width and length of the tunnelling PMOS, respectively.

3.2.4 Measured Results and Performance Analysis

The new RADFET based dosimeter has been fully characterized to observe,

a) FG programming;
b) FG charge stability;
c) Comparative performance of FG reference vs. standard MOS reference; and
d) Radiation sensitivity.

A detailed discussion of each point is as follows.

a) FG Programming and its Challenges

The starting point of using a FGRADFET based dosimeter is programming the FG to a desired level. Compared to the existing floating gate dosimeter architectures, this design has an additional challenge to charge both the sensor and reference floating gates to the exact same potential or as close as possible. This brings a new dimension of programming difficulties that will be described in detail. To verify the proper functionality of the dosimeters, initially unpackaged dies have been tested using a temperature controlled micro probing station and an HP Semiconductor Parameter Analyzer 4155A. The programming and analysis setup is shown in Figure 3.7. The packaged dosimeters have been tested using an HP 16058A Test Fixture, also depicted in Figure 3.7.

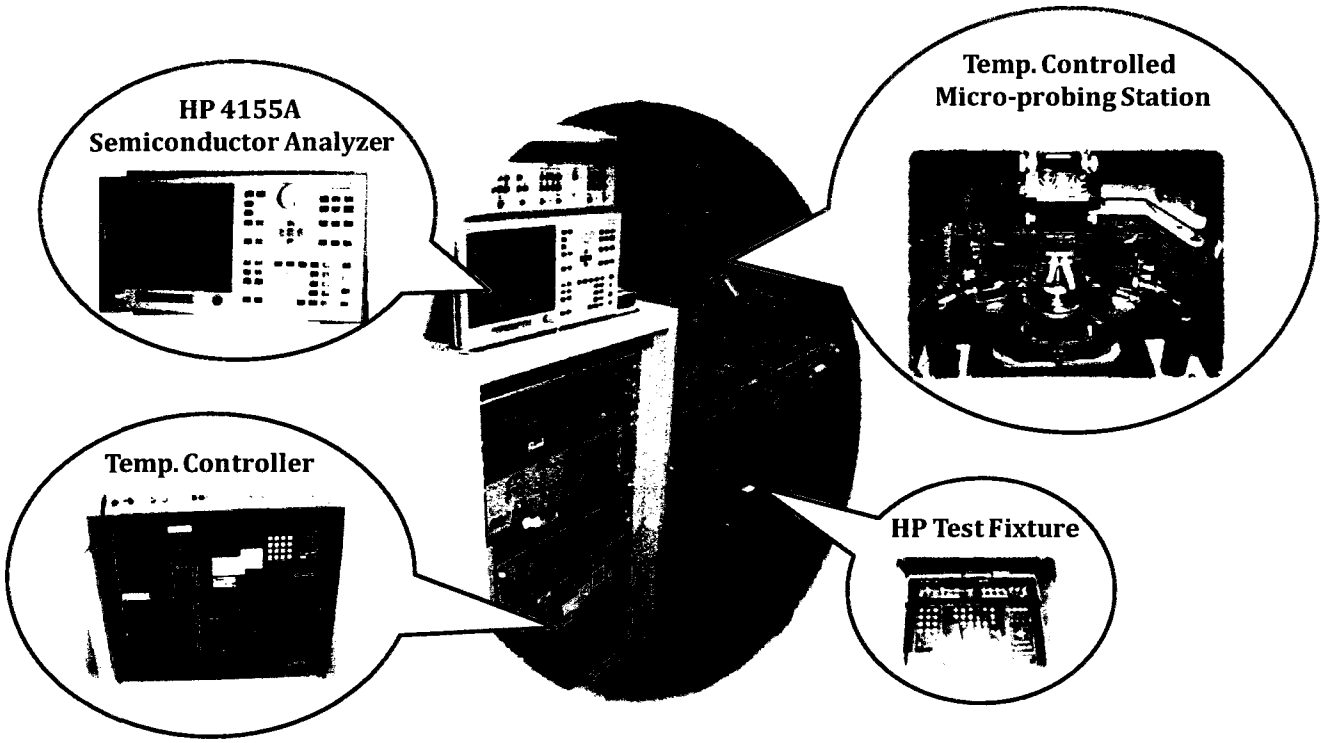


Figure 3.7 Dosimeter programming & analysis setup in a temperature controlled environment.

To charge the floating gate of both the sensor and reference FGRADFET, the source and body (n well) have been connected to ground (0 V), the drain terminal to -0.1 V, and tunnelling injector voltage V_{inj} has been swept from 0 V to -20 V in -10 mV steps. The programming schematic including bias points are illustrated in Figure 3.8.

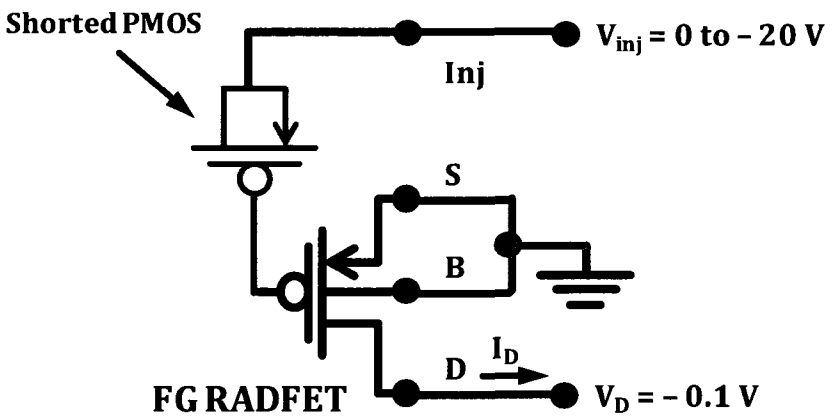


Figure 3.8 FGRADFET biasing during FG programming.

As soon as the drain current I_d reached a desired level, V_{inj} was turned off. Due to the manual on/off control it was very difficult to program the FG potential precisely to the desired level. However, we will discover later that the initial programming through this manual procedure has no practical effect on our ability to analyse the performance parameters or on the end result.

The programming behaviour of both the FG sensor and reference RADFETs is depicted in Figure 3.9(a). Currents are on a logarithmic scale. It can be observed that the FG reference has a higher initial channel current than the sensor. This can be explained by the residual charge left stored on the floating gate during fabrication. The second notable point is that the FG reference started charging earlier (V_{inj} = -14 V) than the FG sensor (V_{inj} = -15 V). This can be attributed to the small size of the reference FG.

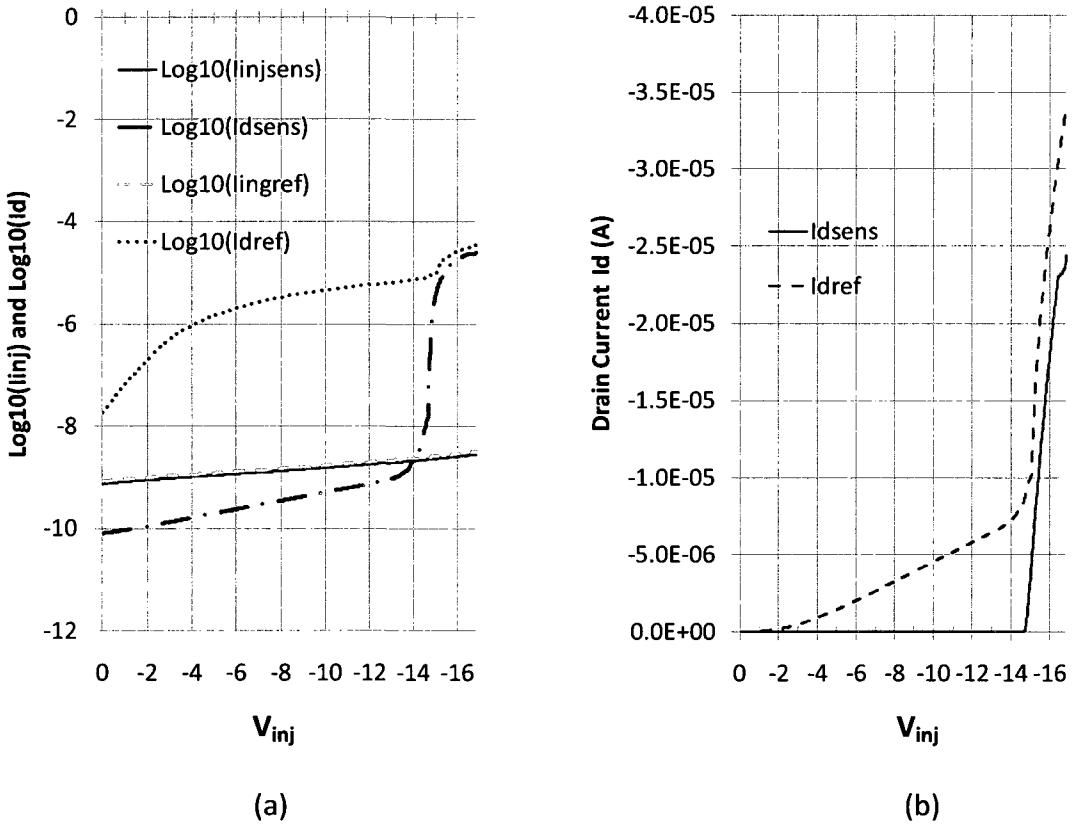


Figure 3.9 Programming of FG sensor and reference with V_{inj} on x-axis and (a) drain and injector currents on logarithmic scale and (b) drain currents on linear scale on y-axis.

Another interesting behaviour exhibited by the FG reference is more obvious on the linear current scale in Figure 3.9 (b). The channel current of the FG sensor device is negligible until the tunnelling phenomenon is initiated and the FG starts charging. But the FG reference shows a significant amount of current flowing through its channel from the very start of the IV curve. This behaviour can be explained by capacitive coupling due to relative size of the floating gate reference, as illustrated Figure 3.10.

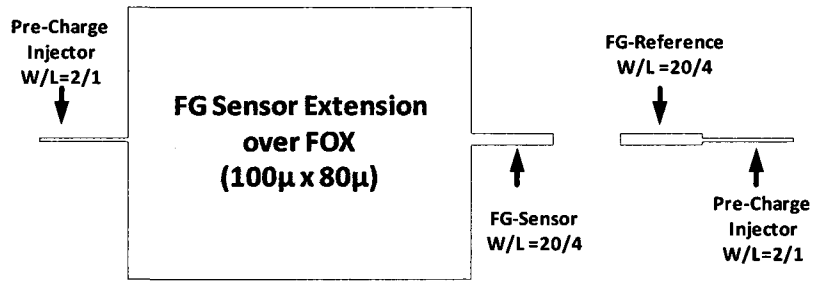


Figure 3.10 Size Comparison of sensor and reference FGRADFETs

The tiny size of the FG reference has a very small gate capacitance to be charged. When large negative voltage is applied to the tunnelling injector, the insulator oxide (SiO_2) does not allow the current to flow towards the gate until electrons start tunnelling through it under the influence of high electric field. But before electron tunnelling starts, under the influence of the applied potential on the injector terminal, a conducting channel in the PMOS device is established and current starts to flow through it. This behaviour is primarily attributed to the small size of the reference FG which exhibits charge localization on account of capacitive coupling and high voltage on the other terminal. Since the tunnelling has yet to start, the floating gate is not charged. This was verified by removing the programming potential from the injector and measuring the drain current. The plots in Figure 3.11, as observed during the programming of the FG reference, are evidence of this issue. Drain current I_D is plotted while varying V_{inj} from 0 – 20 V. The bottom line is Injector current I_{inj}. Initially the drain current I_D of the FG reference started flowing at V_{inj} = -8 V. In the first FG charging attempt programming was stopped when I_D reached 4 µA. But when checked at V_{inj}=0 V, the gate was not charged at all. The second time I_D started flowing at V_{inj}= -3V. Charging was stopped this time when I_D reached 8 µA. When measured the FG was only charged enough to produce 2 µA in channel.

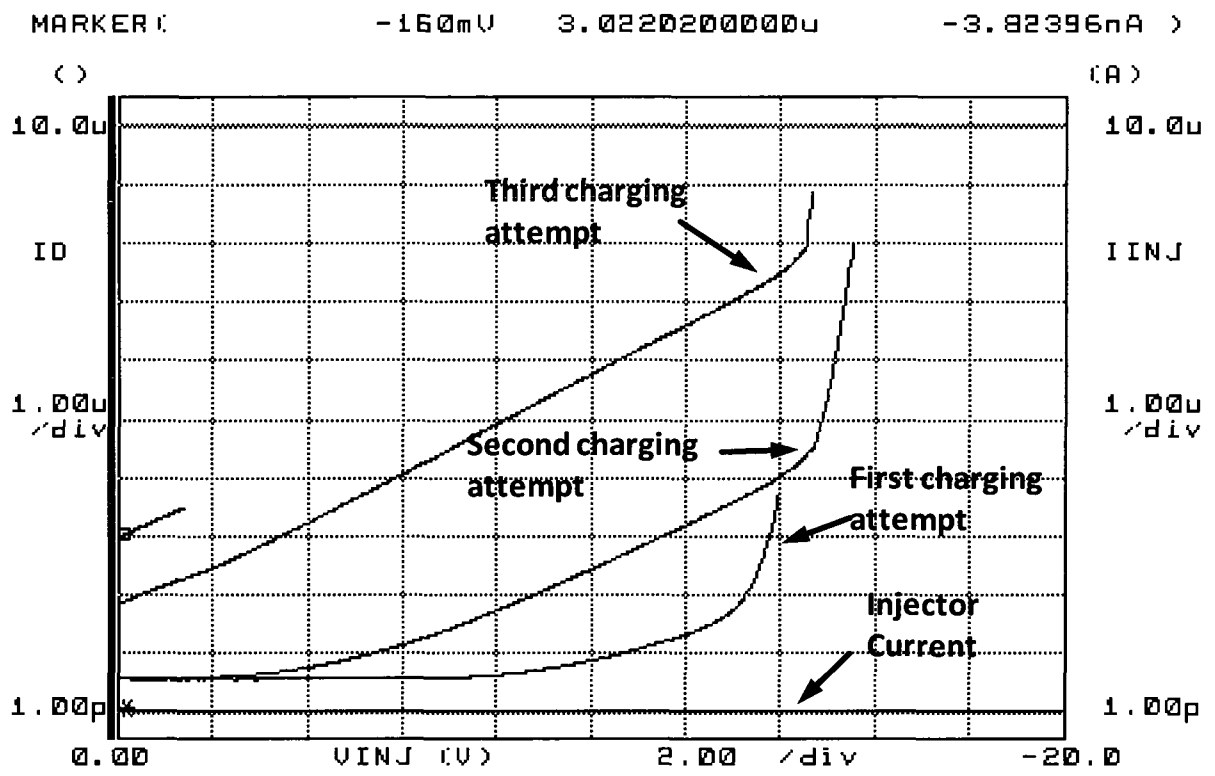


Figure 3.11 FG Reference FG programming

The third time I_D started flowing from the beginning (V_{inj}=0), since the FG was already charged to produce 2 μA current. The programming was stopped this time when ID reaches 9 μA. But the gate was only charged to cause I_D = 3 μA. The measurements show that the FG reference only charges for $|V_{inj}|$> 14 V. A possible explanation of this behaviour is the device channel formation due to the accumulation of minority careers beneath the gate under the influence of high negative bias applied to the injector terminal. This behaviour of FG reference poses unique FG programming challenges. It is very difficult to program the FG reference exactly to a desired level. As can be seen in Figure 3.9 (b) about 8 μA current, which corresponds to a gate voltage of -1.35 V, already flows through the device without any charge transfer to the FG. It is especially difficult to program the device to a lower potential.

Though the FG reference is affected the most by this problem, especially before charge starts tunnelling to the FG, this issue is not limited to the FG reference or lower programming voltages prior to the start of electron tunnelling effect. Both FG sensor and reference are affected to an

extent. In FG sensors, at higher $|V_{inj}|$ (>17 V) this effect is noticeable while at smaller values of $|V_{inj}|$ it is relatively unaffected due to the large floating gate area and associated capacitance. When the FG sensor on the same chip is charged to the same level (8 μA), a prescribed value was successfully achieved in the first attempt, as shown in Figure 3.12. In practice, while programming the FG manually to a higher absolute gate potential ($|V_{FG}| > 5$ V or $|I_D| > 40$ μA), the FG Sensor and reference were over charged roughly by 1 μA, and 3 μA respectively to achieve a close match to the desired charging level.

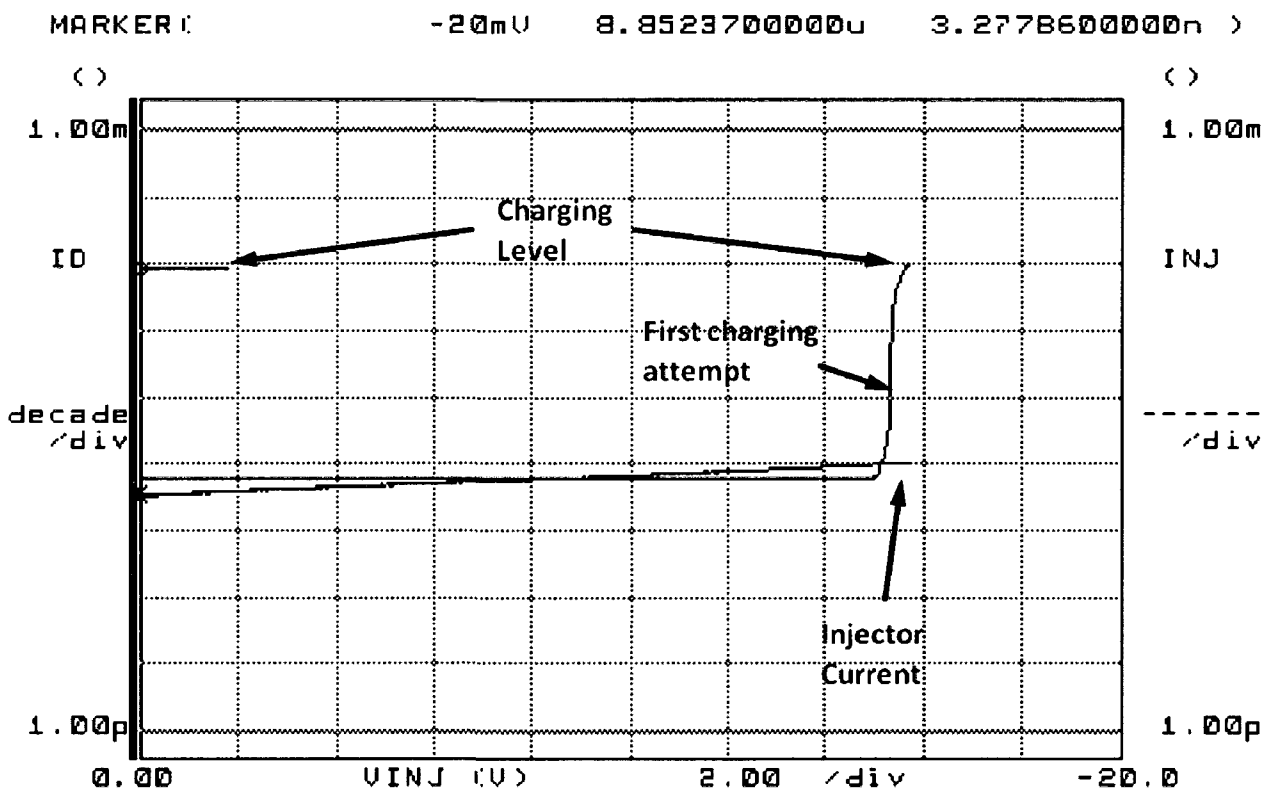


Figure 3.12 FG sensor programming behaviour

Improved Charging Injector:

In earlier versions of the dosimeters in this work, the charging injector as illustrated in Figure 3.13(a), a shorted PMOS was used. However in the latest designs, the n-well beneath the shorted PMOS structure was replaced with a p-well, as illustrated in Figure 3.13(b). An improvement in the charging behaviour has been observed. For the normal n-well FGRADFET,

the tunneling initiated at $|V_{inj}|$= 13.5 V whereas for the modified p-well type charging injectors, this value increased to $|V_{inj}|$ = 15.5 V. The only other difference between the n-well and p-well type charging injector devices is that in the former, the FGRADFET devices were shielded using M2, whereas the new FGRADFETs with p-well injector are shielded with M3. This metal shielding should not have any effect on the tunneling voltage.

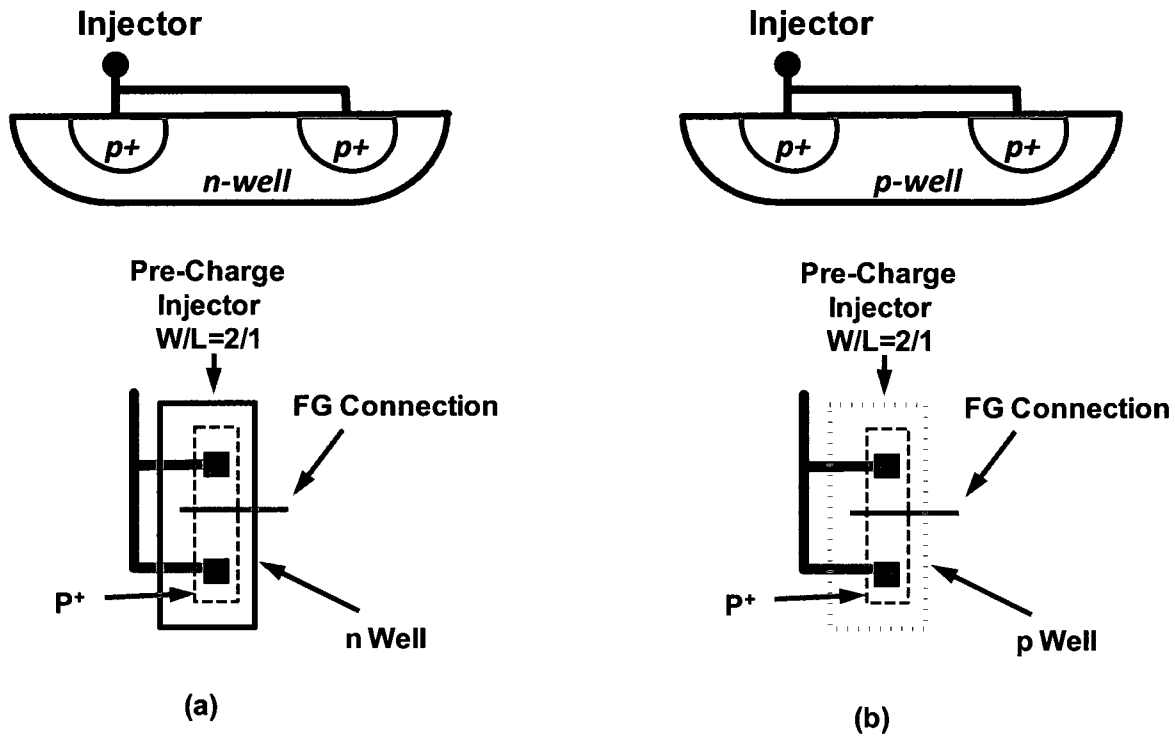


Figure 3.13 (a) Old and (b) new (improved) FG charging injectors

Removing Charge from the Floating Gate:

In previously reported dual poly injector gates, bidirectional charge transfer was possible. Hence precise programming level was easier to achieve by adding and removing charge on the FG. The new single poly shorted PMOS programming structure with a p-well beneath the shorted PMOS, while useful for efficient charging of the FG devices using single poly MOS like structure, has limitation of one way charging only. It is not possible to remove the charge from FG using this new charging mechanism through reverse tunneling. The means of removing

charge from FG in this situation are excessive heating, UV light, or exposure to ionizing radiation. Excessive heating may damage the FGRADFET and other on-chip components. Due to metal shielding over entire FG, discharging FG through UV light is not an option. Therefore floating gate devices with new single poly programming injector can only be discharged through exposure to high energy radiation.

b) Standard Reference IV Curves

On each of the new dosimeter chips standard PMOS reference transistor is included that is identical in size to the FGRADFET sensor and reference. This facilitate the accurate translation of the measured FG channel current at an equivalent floating gate potential. Representative IV characteristics of one of those standard reference PMOS measured at 25°C is plotted in Figure 3.14 and Figure 3.15.

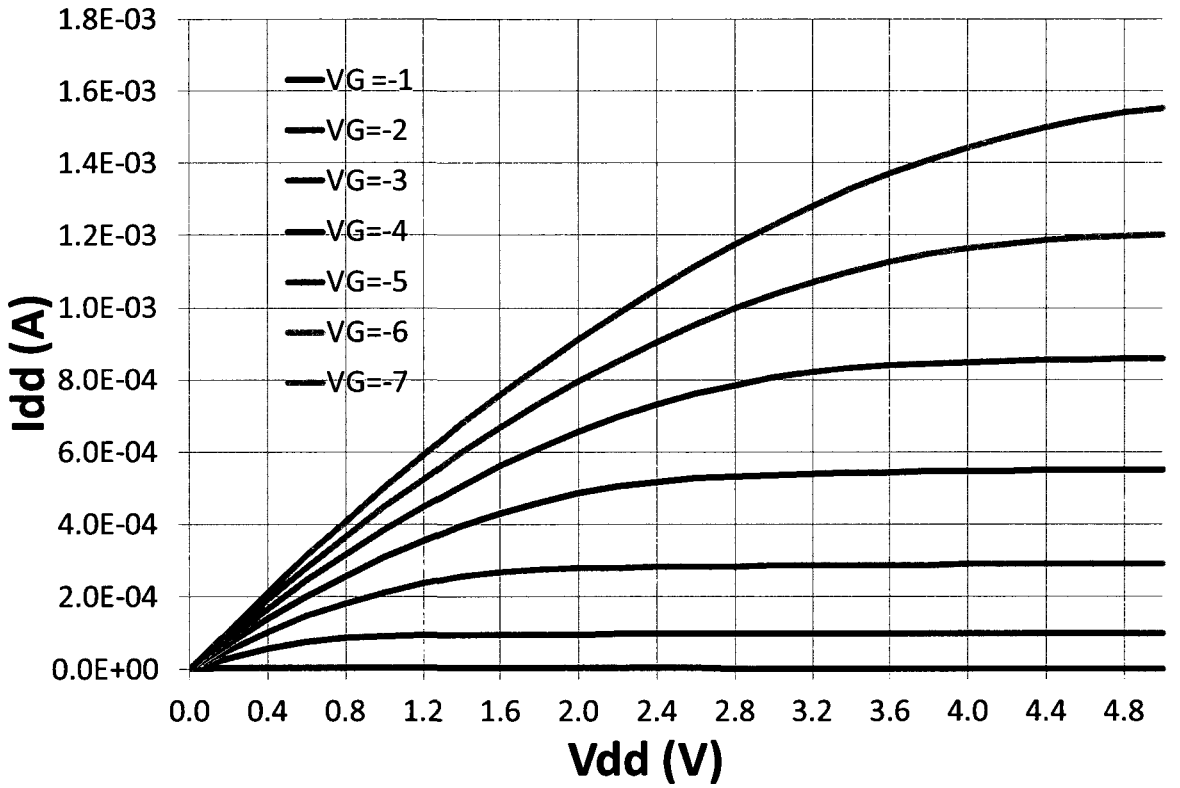


Figure 3.14 Standard PMOS reference measured IV characteristic (I_{DD} vs V_{DD})

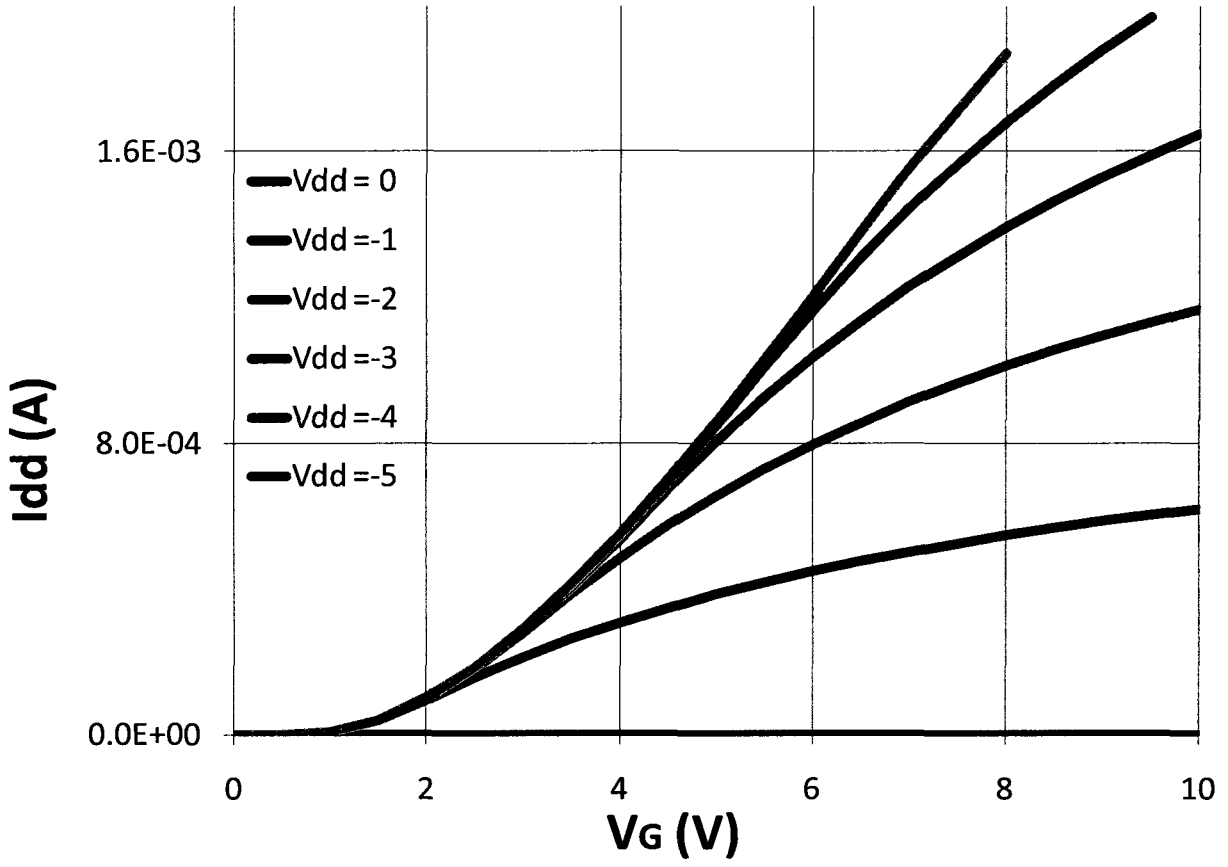


Figure 3.15 Standard PMOS reference measured IV characteristic (V_G *vs* I_{DD})

FG Charge Stability

Stability of the charge stored on the floating gate is a critical issue in RADFETs. After charging, floating gate devices tend to lose charge with a large time constant. To understand the effect of this phenomenon in the new floating gate devices used for the dosimeter design in this thesis, an experiment based analysis has been performed. For this analysis, several floating gate devices were charged to different voltages and left at room temperature. Unpackaged dosimeters were used for a tighter control of temperature during measurements and to avoid other uncertainties. The FG voltage of each unit was determined through measured channel current and compared with the characteristic (IV) curve of a standard reference MOS of identical size on the same chip. An example set of characteristic curves is shown in Figure 3.16 plotted for different temperatures.

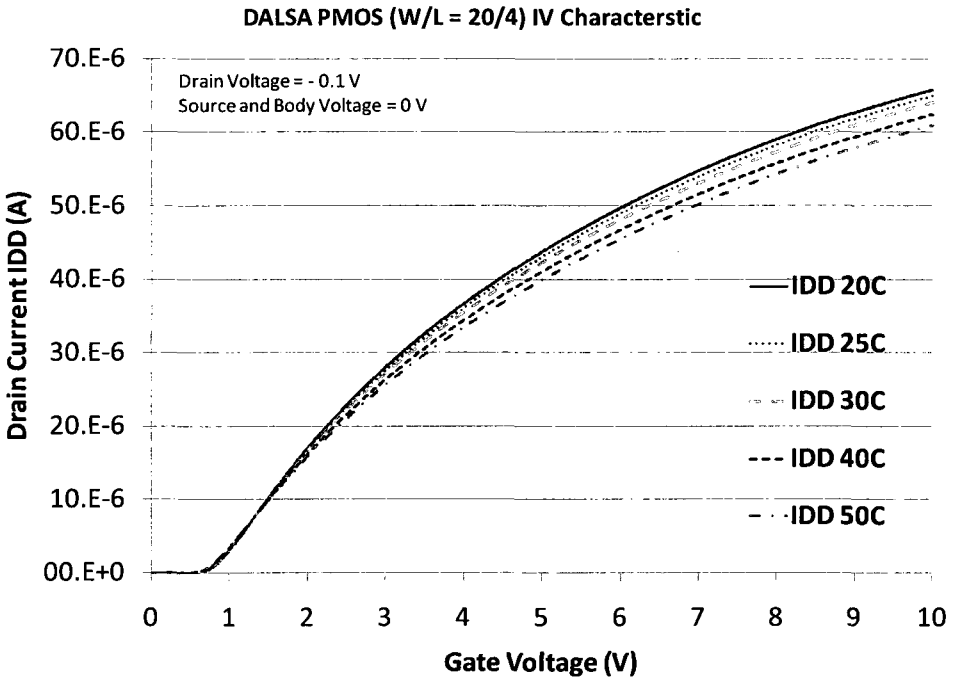


Figure 3.16 Gate voltage vs. drain current of DALSA PMOS at different temperatures

Current was measured once a day at controlled temperatures. The charge stability pattern of a representative FG device observed over a 2-week period is shown in Figure 3.17.

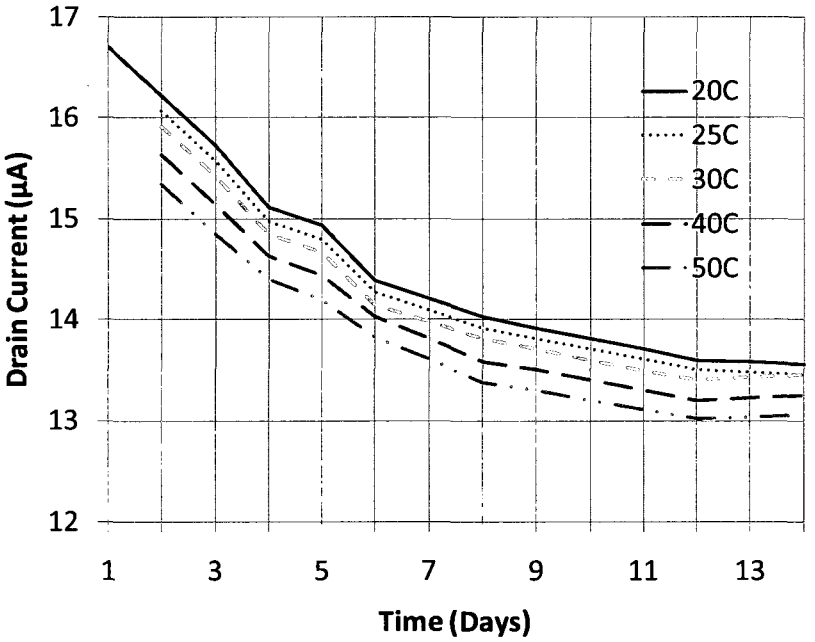


Figure 3.17 FGRADFET sensor stabilization

The FG device continuously loses charge and attains a somewhat stable level at around day 12. This is a well known phenomenon which was discussed in chapter 2. The primary reason for this behaviour is the very large time constant of the BPSG layer that these devices are buried in and use to trap additional charge particles for increased FG sensitivity [36]. The discharge rate depends upon several parameters including the device geometry, material properties, programming parameters, and temperature variations among the others. Given this behaviour of FG devices, it is not useful to charge them to a very precise value until they obtain stability. The discharging and stabilization behaviour of FGRADFETs varies from device to device. Figure 3.18 shows the stabilization of three devices observed over a period of 2 weeks.

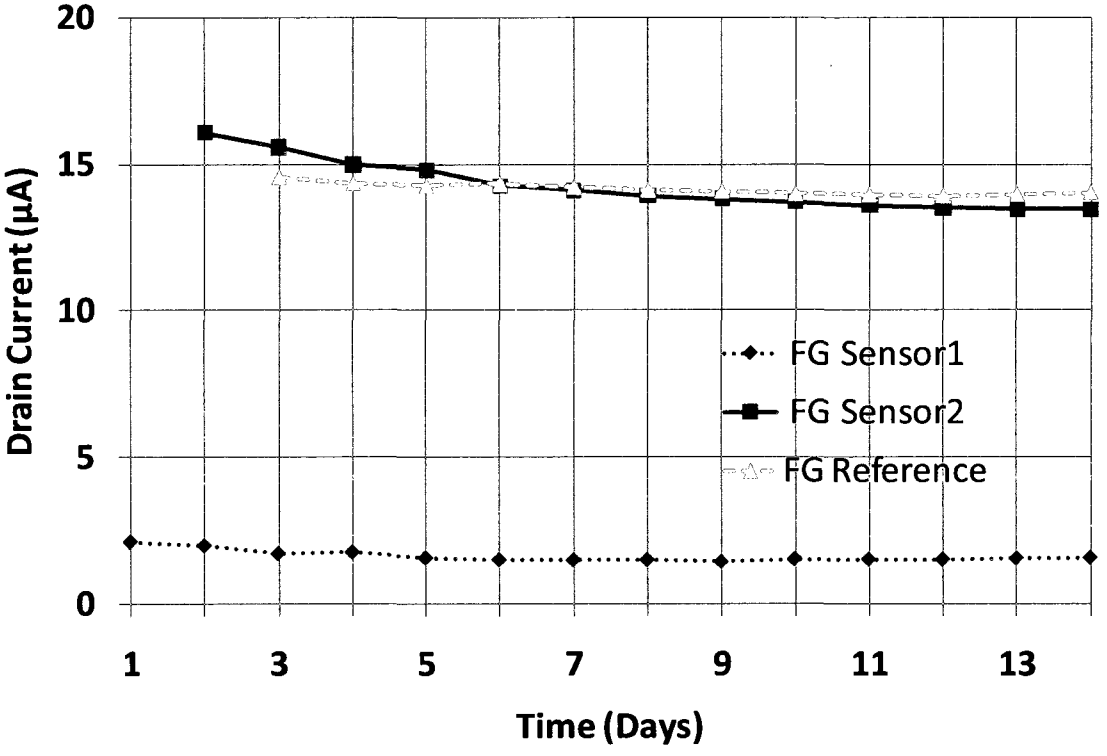


Figure 3.18 Stabilization of different FGRADFET devices (measured at 25°C)

It is obvious that the FG Reference device and FG Sensor1 with small initial charge have been stabilized earlier than FG Sensor2. In this work, less than 1% change in channel current per day was considered as stable. Given different discharging behaviour of FGRADFETs, initial manual programming does not adversely affect the reliability of the analysis.

FG Charge Stability and New Dosimeter Architecture

The architecture presented in this thesis requires the FG reference and sensor to be charged exactly to the same level to accurately single out the radiation dose from other variations in the environment. Figure 3.19 compares the charging stability of the floating gate sensor and reference. Both the RADFETs were charged to the same initial level and the discharging was observed daily for two weeks. All the measurements were done at a controlled 25 °C environment. It is observed that the two devices discharge at a different rate. The FG reference does not lose charge as fast as the FG sensor. Also the FG reference achieves the stabilized state (less than 1 % change) earlier than the sensor. This behaviour is somewhat predictable as the stability of the FG sensor is more dependent upon the large volume of BPSG above the FG extension over FOX, and the settling of the trapped charges and the charge distribution of the BPSG takes longer to settle down.

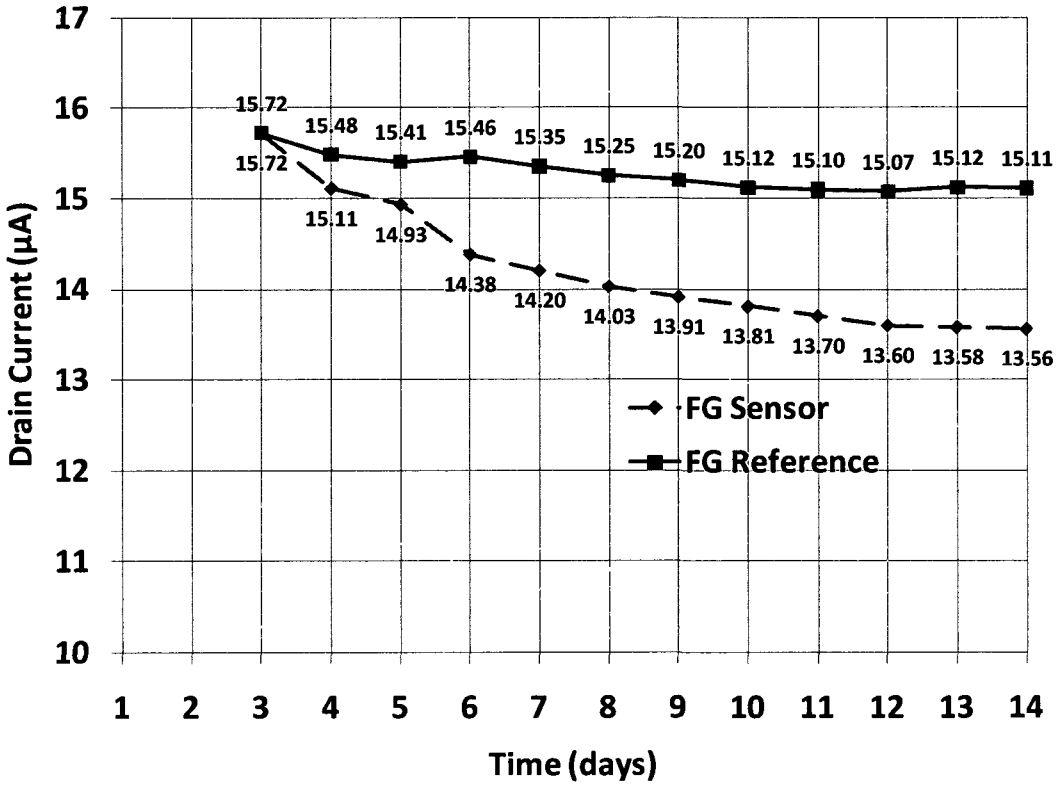


Figure 3.19 Stability Comparison of FG reference and sensor

Stabilization of RADFET:

The uncertainties and variations in the behaviour of FG devices due to the instability of charge on the floating gate limits its usability in an environment where precision is important, such as our target application of cancer dosimetry. It is crucial to eliminate or minimize these variations to obtain an accurate and precise dose from FGRADFET based dosimeters. The techniques to stabilize the charge on the FG are briefly touched upon the literature [36]. The problem is well recognized in other FG devices such as non-volatile memories [42], and analog trimming circuits [74], and is briefly discussed in FG dosimeter literature [28], However, insufficient information is available to establish a logical procedure yielding reliable and rapid stabilization of the charge on the FG devices. In this section, the results and analysis of the experiments performed to achieve the stability are presented.

1- *Long term storage after charging*

The first procedure as suggested in [36], is to store the FG devices after charging them long enough to allow the BPSG to release the stress caused by the programming of FG using high voltage tunnelling. We already analysed the stabilization of devices used in this thesis based on a 2 week observation, as shown in Figure 3.17. There is still a charge lose of around 0.5% per day. To understand the charge stability over an extended period of time, Figure 3.20 is provided to show the charge on a FGRADFET sensor fabricated in DALSA 0.8 μm CMOS process with metal 2 shielding over the FG area, tested after one and a half years of programming.

The rate of change in this device is less than 0.03% based on readings at 6th and 18th months. It is evident that storing the charged device for long time does bring stability to the FG devices; however, it is not practical to wait such a long time in most of the situations.

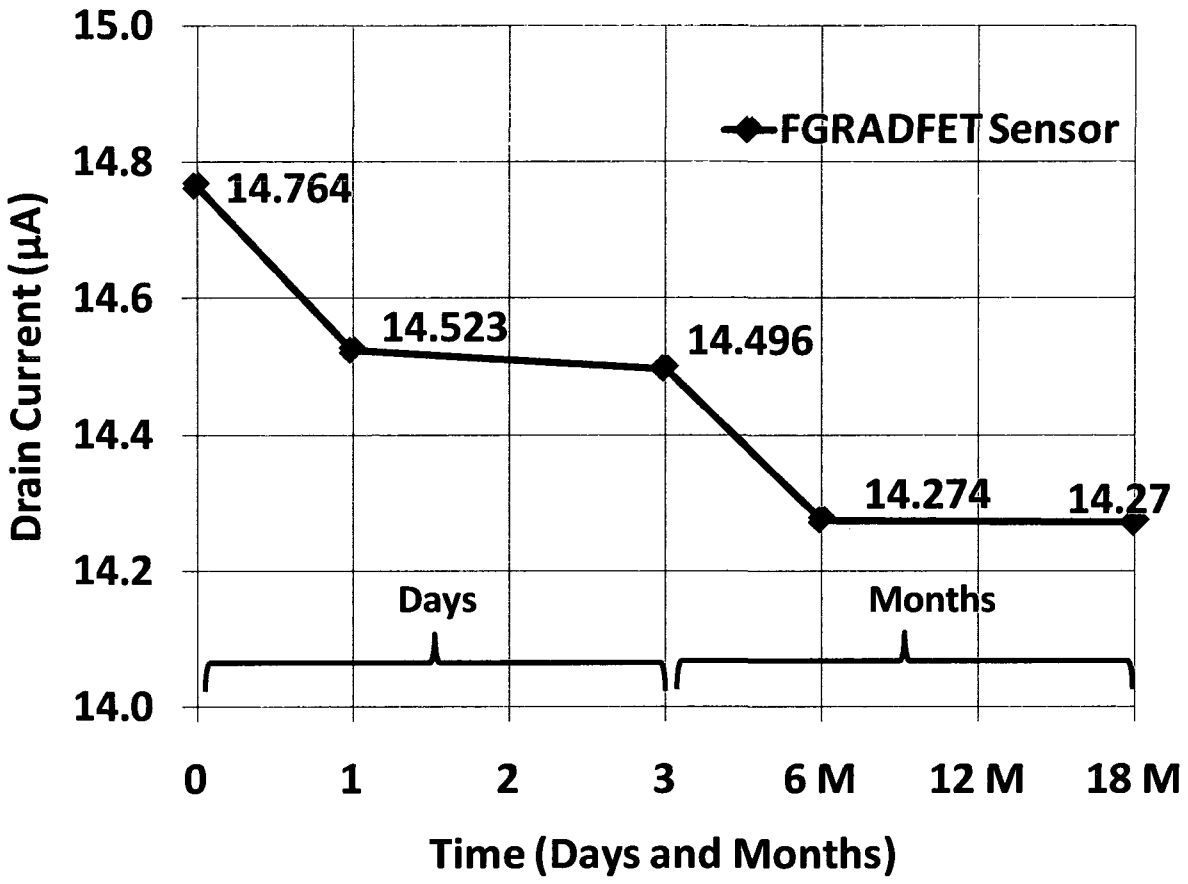


Figure 3.20 Long term fading and FG stability

2- Effect of Charging Time on FG Stability

It is suggested in [42] that slow charging of the FG results in fewer instability issues, hence a more stable charged floating gate device. To verify this, two FG sensors on the same die have been charged to approximately the same level, but with different charging times. FG Sensor1 was charged by varying the tunnelling injector voltage from 0 V to -17 V in 10 mV steps using the "Long" control feature of the HP4155 semiconductor analyzer. FG Sensor2 was charged under the same conditions except the input V_{inj} step size was 100 mV using the "short" setting of the HP4155. Charge levels on both the devices were observed over 12 days at 25°C. The results are shown in Figure 3.21.

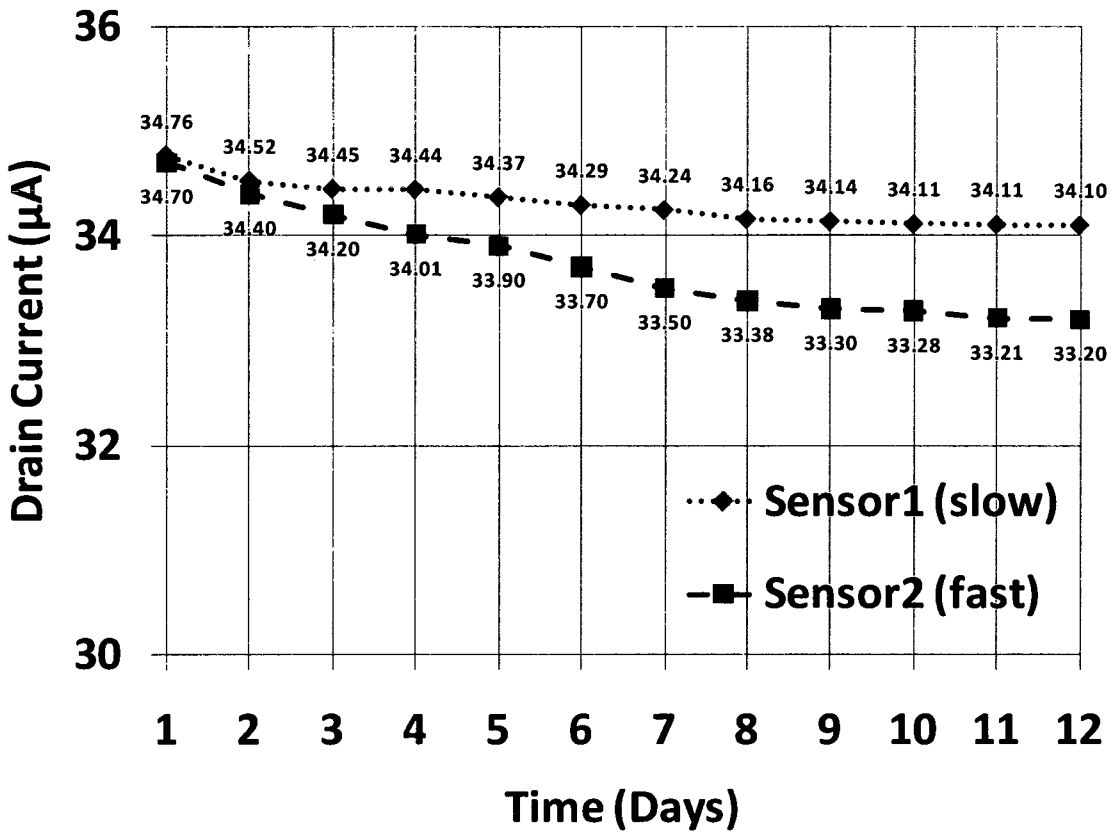


Figure 3.21 Effect of programming speed on FG stability

The device that was charged slowly not only stabilizes earlier it also experiences a lower amount of charge fading. Hence, it is observed that the slow charging of FG devices in small input voltage steps results in a more stable charged FG device. However, to fully understand the effect in order to model this behaviour, extensive analysis is still required.

3- FG Stability and Heat Treatment (Annealing)

A way to quickly obtain stability in FG devices is through heat treatment or annealing. As mentioned before, the main cause of instability of FG devices is the stress in the BPSG and trapped charge at the Si/SiO_2 interface. Annealing is a well known technique to remove the trapped charges from BPSG in semiconductor devices [5]. After annealing the semiconductor device usually has fewer defects and trapped charges in its BPSG layer and it should be more stable. To take advantage of annealing for rapid stabilization of the dosimeter FG devices, two

freshly programmed unpackaged dosimeters that include two FGRADFET sensors, and two FGRADFET reference transistors were heated in a temperature controlled oven at 150 °C. The charges on the FG devices were measured hourly after cooling them down to 25 °C on a temperature controlled micro probing station.

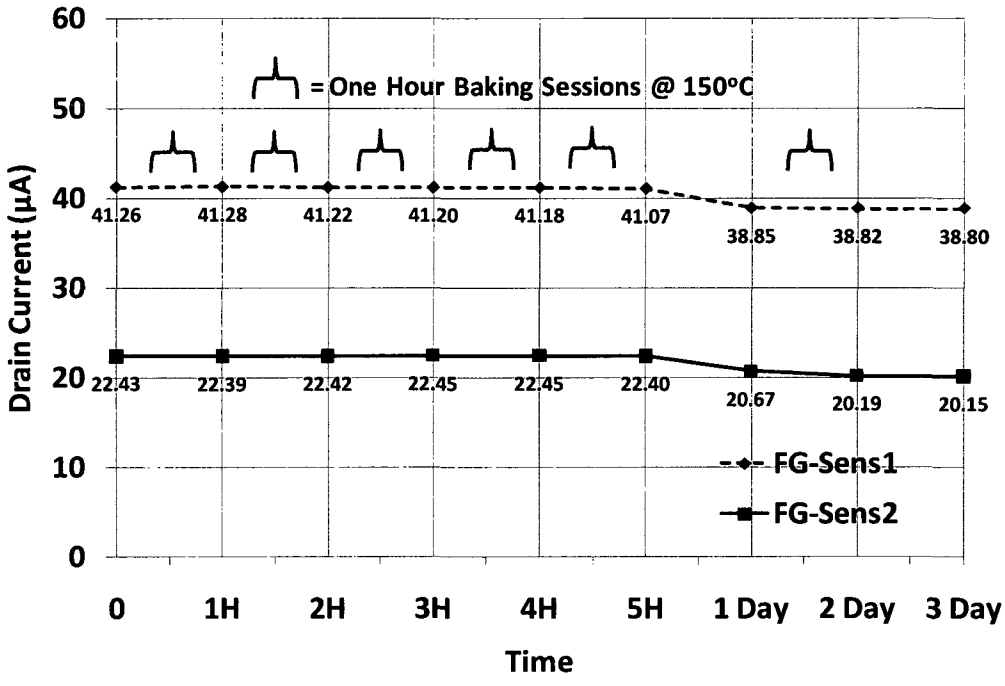


Figure 3.22 Annealing of FG sensors immediately after programming

It can be observed in Figure 3.22 that the devices annealed immediately after programming do not show fading as a result of annealing and devices appears to be stabilized. But when measured in two consecutive days after annealing, they lose the charge like an un-annealed device. However, after another one more annealing session on day 2 the FG devices reached a stable state. Corresponding to what an un-annealed device would reach after 10 -12 days. To help establish a fast stabilization technique, another FG sensor was programmed and left for one day. On day 1, after measuring the charge on the gate the device was annealed in one hour session at 150^{O}C until stabilization was achieved. As depicted in Figure 3.23, after 3 one-hour annealing sessions the charge on the FG was stabilized. The stabilized state was confirmed by observing the device for two more days after annealing.

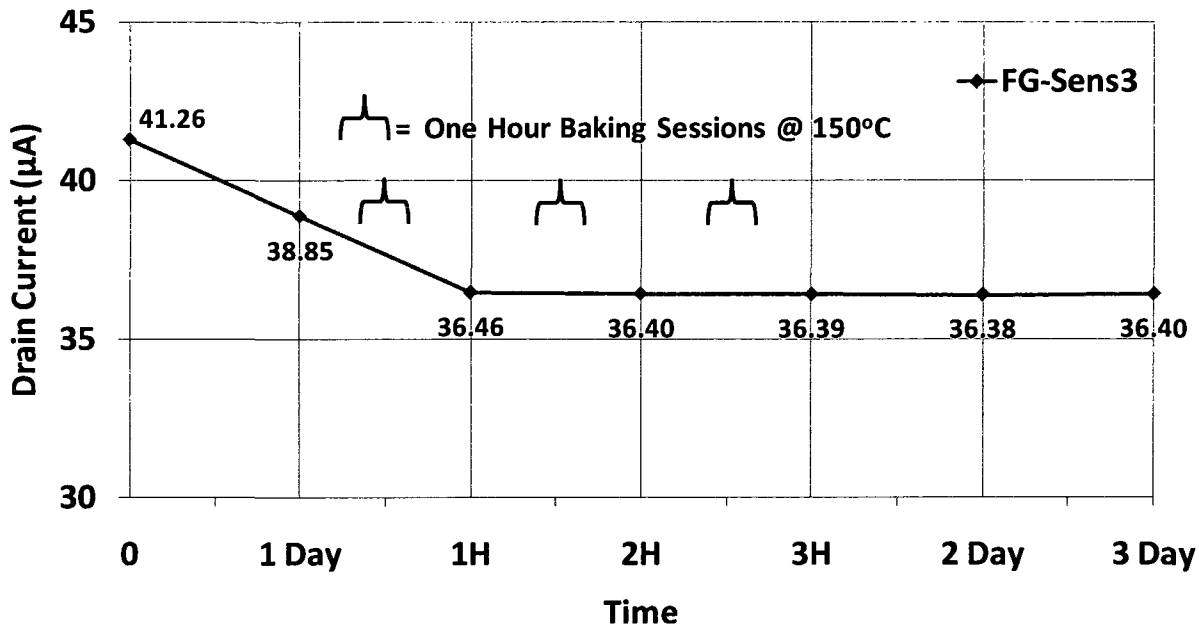


Figure 3.23 Annealing of FG sensor one day after programming

An interesting but unusual effect of annealing has been observed for FG reference devices. When the FG reference was programmed and annealed for an hour, the measured charge on the FG after annealing was slightly more than the level to which they were originally programmed. Figure 3.24 is showing this behaviour exhibited by the FG reference. To the author's knowledge, this effect has not been reported before. The exact explanation of this phenomenon is unknown but it appears that a stress produced in the device structure during programming is relieved by annealing, resulting in the additional charge on the floating gate. The FG sensors did not exhibit this effect. This behaviour can be explained by a delayed charging phenomenon that is happening in parallel to the fading effect in the FG devices. In normal conditions the fading effect is dominant, hence this behaviour, which is smaller in magnitude, was suppressed and not observed. When the FG devices were annealed immediately after programming, as in Figure 3.22, fading is not observed. Hence, this unknown phenomenon may become a dominant factor in the overall behaviour of the freshly charged FG devices undergoing annealing. This effect was not observed in the FG sensor devices. Large FG extension over FOX and its associated large capacitance may be the reason. Detailed theoretical and experimental analysis is needed to fully understand this behaviour.

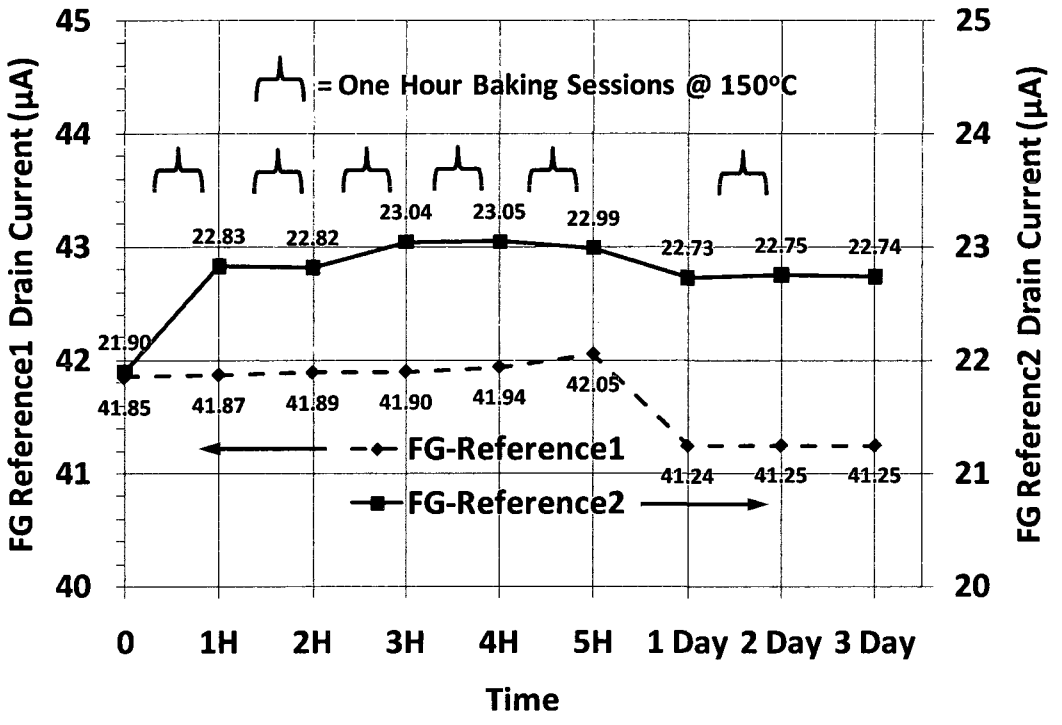


Figure 3.24 Charge top-up as a result of annealing immediately after programming of FG reference

c) Comparative Performance of FG Reference vs. Standard PMOS Reference Under Varying Temperature

To monitor the relative behaviour of the FG sensor and reference FGRADFET along with the standard reference PMOS for varying temperature and channel current, of all three devices have been observed under controlled variation in temperature using the test setup described in Figure 3.7. This test is performed to determine the effect of FG reference on the performance of the dosimeter, especially its ability to single out the change caused by the radiation dose from all other variations in the environment. Both the FG sensor and reference were initially programmed to produce identical channel currents under the same bias conditions (drain voltage = -0.1 V, source and body voltage = 0 V). The gate terminal of the standard reference PMOS has been set to produce the same current as the programmed FG devices at 20°C and then was kept at that value to observe the change in the channel current as a function of rising temperature. The test has been performed from 20°C to 50°C in steps of 5°C. The results are plotted in Figure 3.25.

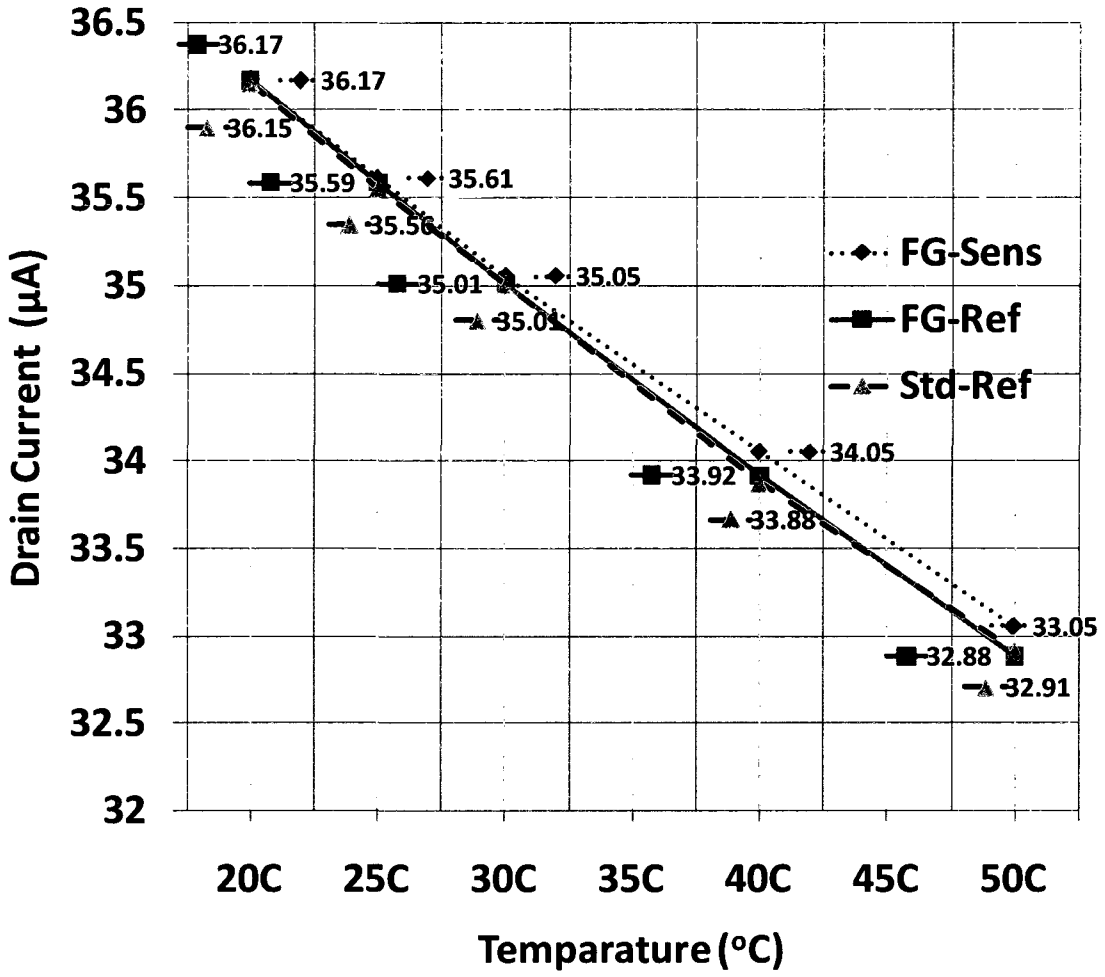


Figure 3.25 Thermal behaviour of standard and FG reference vs. FG sensor

This comparison suggests that all three devices behave in a similar manner under varying temperature, however compared to the FG sensor, both the FG reference and standard PMOS reference are in much tighter agreement.

These results confirmed the effectiveness of the differential structure of the dosimeter to filter the effect of variation in temperature, as was suggested in earlier designs [36]. The FG reference based differential dosimeter is as effective in filtering the changes in temperature as the standard reference based dosimeters. Thus the real advantage of using the FG reference is to achieve low power operation of the dosimeter, which is critical for self powered wireless dosimeter applications.

3.2.5 Automatic Programming of FGRADFET Dosimeter:

To ease the programming challenges of the floating gate devices, an automatic FG programming (AFP) architecture has been developed. The proposed architecture accounts for the device behaviour and specific challenges and limitations that have been experienced during programming.

One-way programming

In cases similar to the one presented in this thesis, where charging of FG devices is possible through electron tunnelling but discharging of the FG requires very large voltage that can potentially damage the devices, a one-way programming option is suggested. In one-way programming we can only add charge to the FG. This concept is illustrated in Figure 3.26.

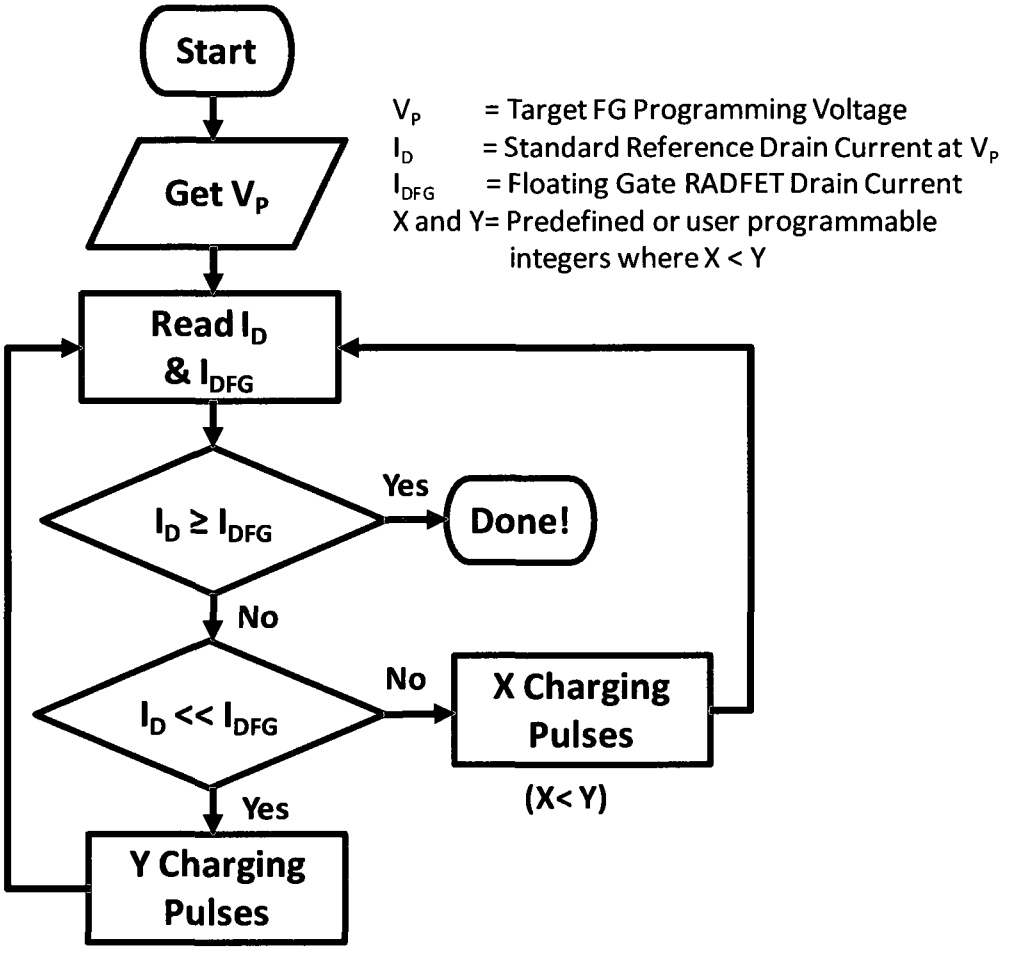


Figure 3.26 Flowchart of the proposed one-way programming scheme

The programming scheme is devised assuming that along with the sensor and reference FGRADFETs there is an identical size standard reference MOS present on the same chip. The presence of a standard reference is not only easier for traditional users to think in terms of floating gate voltage instead of channel current, it also provides a reliable reference point and avoids any mismatch of the device parameters from chip to chip while eliminating the effects of environmental variations. However, it is not necessary to have the standard MOS reference for the proposed AFP to work. In the absence of a standard MOS reference, instead of V_P, the user input will be in the form of channel current I_D and the system will charge the devices to that current level. The proposed programming scheme is as follows,

1) User provides the desired voltage, V_P, to be programmed on the FG
2) AFP system reads the equivalent current I_D by applying V_P at the gate terminal of the standard reference MOS. It also reads the initial current flow I_{DFG} through the FG device to be programmed.
3) Two currents are compared, if I_D is smaller or equal to I_{DFG}, AFP stops at this point. FG is already programmed at or more than the desired value. If it is overcharged, ultraviolet light or an ionizing radiation source can be used to bring it back to the desired level.
4) If I_D is larger than I_{DFG}, AFP determines the difference between the two. If the two values are far from each other it sends a stream of "Y" charging pulses to the electron tunnelling injector, where, Y is a pre- or user defined integer. On the other hand if the two currents are close to each other, AFP sends a stream of "X" charging pulses to the electron tunnelling injector. X is also a pre- or user defined integer where X<Y. This helps to fine control the charging of FG precisely to the desired value.
5) AFP reads the two currents again, and works in a cycle until it comes to a logical end.

Two-way programming

If the programming structure and physics of the FG devices allows the removal of charge from the floating gate, a two-way charging scheme similar to the one described above can be adopted. The flowchart representation of such a scheme is illustrated in Figure 3.27. The only difference is that now the level of charge on the FG can be fine tuned in both directions using either positive or negative voltage pulses.

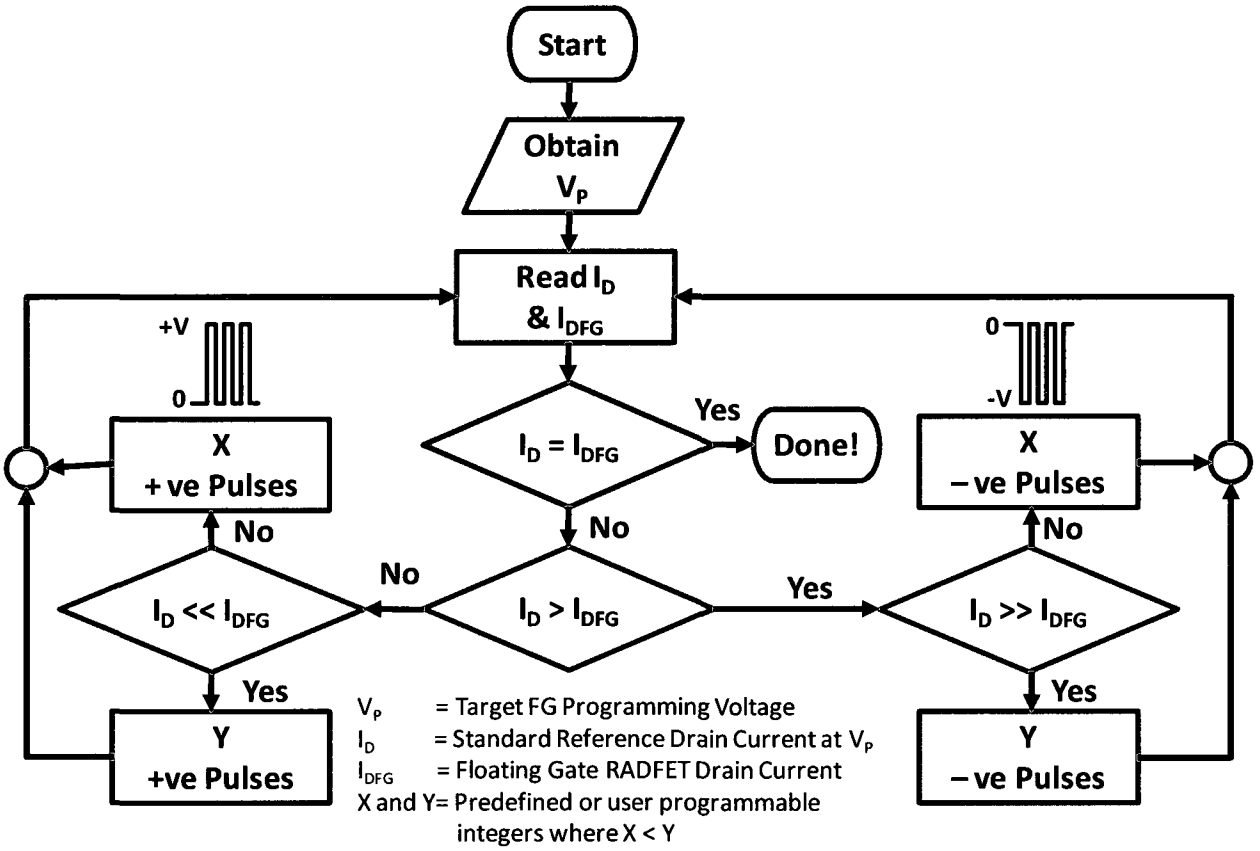


Figure 3.27 Flowchart of the proposed two-way programming

Implementation of AFP System

The physical implementation of the proposed AFP system is shown in Figure 3.28. There are 4 basic components of this system,

1) A dosimeter chip with sensor and reference FGRADFETs and a standard MOS reference.

2) A PC or a micro-controller to provide the user interface and hold the AFP algorithm.
3) Interface circuitry between the chip and the controller including dual polarity power supply. The internal circuit of this block mainly consists of solid state protection fuses and solid state switches operated by the signals from PC or micro-controller to make or break the connection between the high voltage power supply and the Injector terminals. Depending upon the maximum current flow, low voltage terminals can directly be driven by signals from the controller through a protection fuse to prevent any damage.
4) The final block is user interface elements such as keyboard to enter the values of desired parameters and a display. When using PC as a controller, these components are already available.

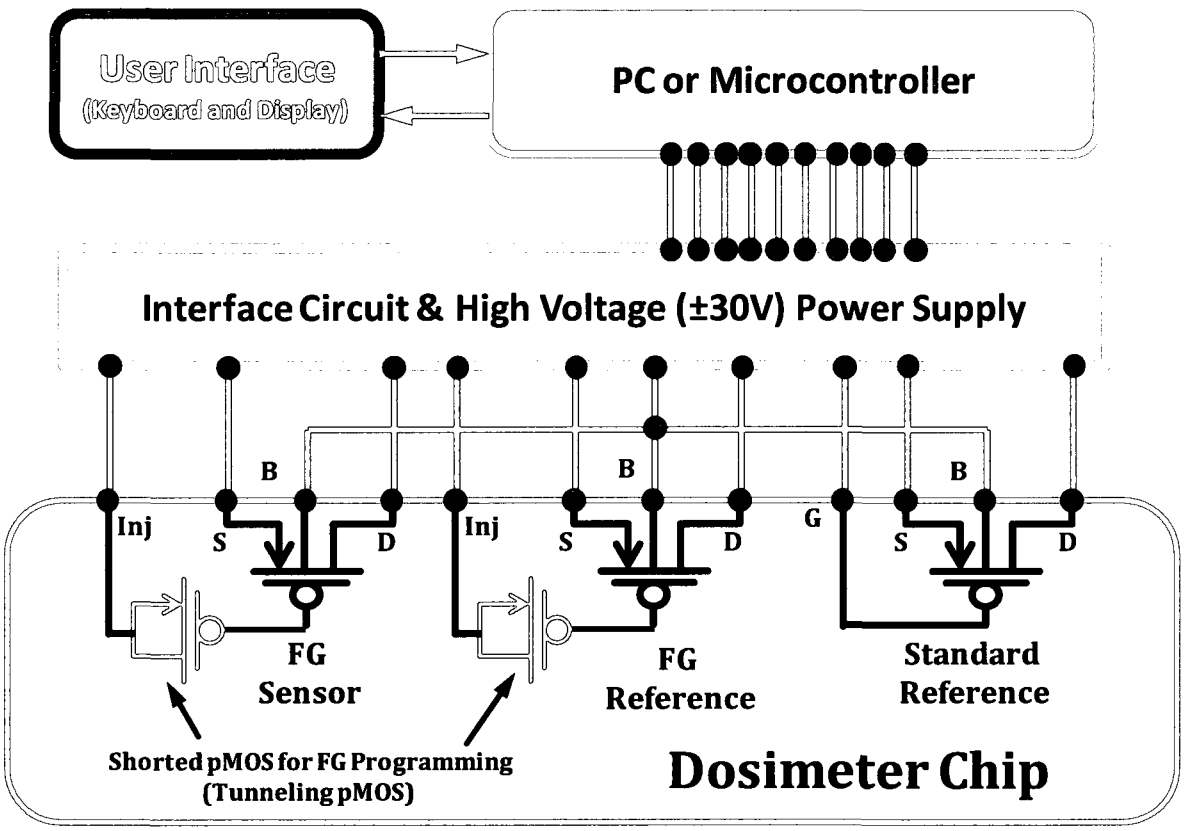


Figure 3.28 Proposed implementation of the AFP architecture

3.2.6 Measured Radiation Sensitivity of New Dosimeters

The dosimeter presented in this thesis has been tested for γ-rays and x-rays sensitivity.

Sensitivity Measurements for γ-Rays

Radiation sensitivity of the dosimeters for γ-ray, the most common radiation source used for radiotherapy, has been performed at National Research Council of Canada's Institute for National Measurement Standards (NRC-INMS) radiation testing facility in Ottawa. Cobalt-60 (^{60}Co) was used as γ radiation source. ^{60}Co is a radioactive isotope of cobalt with short half life of 5.27 years. The radioactive ^{60}Co isotope was near to its half life and was generating γ-rays at the rate of 56.96 rad/minute. Several packaged and unpackaged dosimeters with FG devices charged at different levels have been tested under five consecutive γ-ray doses of approximately 100, 100, 200, 200 and 400 rad for the total dose of 1 krad. All measurements were performed at room temperature of 23°C. The change in floating gate potential (V_{FG}) with the incident radiation dose D of the FGRADFET sensor with corresponding FGRADFET reference are shown in Figure 3.29. V_{FG} was measured indirectly as a function of the drain current (I_d) by comparing the currents with an identical size standard PMOS reference that is present on each dosimeter chip for calibration and measurement purposes.

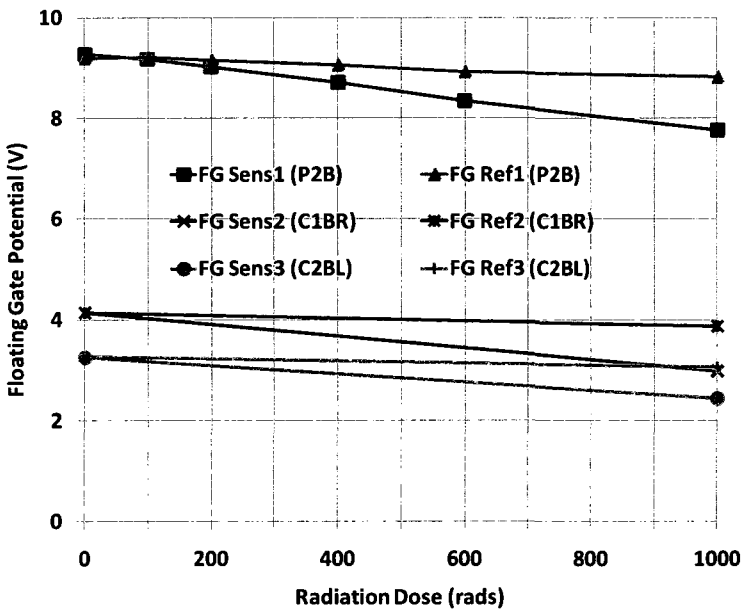


Figure 3.29 Dosimeter radiation test under γ-rays from 57 rad/minute ^{60}C radioactive isotope

The γ-ray radiation sensitivity for each FG sensor and reference, along with "initially programmed" and "after exposure" FG potentials, are listed in Table 3.1.

Table 3.1 FG Potential and γ-ray Sensitivity of New Dosimeters

	Initial FG Potential V_{FGo} (V)	V_{FG} after 1krad γ-rays dose (V)	Sensitivity (mV/rad)	Effective Sensitivity of Dosimeter (mV/rad)
FG Sens1 (P2B)	9.27	7.76	1.460	1.10
FG Ref1 (P2B)	9.20	8.83	0.357	
FG Sens2 (C1BR)	4.13	2.98	1.110	0.85
FG Ref2 (C1BR)	4.14	3.87	0.260	
FG Sens3 (C2BL)	3.26	2.45	0.781	0.58
FG Ref3 (C2BL)	3.27	3.06	0.203	

Consistent with the theory, the dosimeters are more sensitive at higher bias points (higher FG potential). Though the FG references are very small and have no FG extension over FOX, they still exhibit considerable sensitivity to the incident radiation, bringing the overall effective sensitivity of the dosimeter to a lower value. Still the advantage of low voltage operation that these FG references have provided is worth the small lost in total sensitivity.

Sensitivity and M2 vs. M3 shielding

To observe the effect on radiation sensitivity by using elevated FG metal shielding, two dosimeters with identical design have been tested for γ-ray sensitivity. Both the dosimeters were fabricated in the same process, one with metal 2 (M2) shielding, and the other with metal 3 (M3) shielding. The dosimeters were programmed at a similar level and, after achieving a stable state, were exposed to 1 krad of γ-ray dose. The results are plotted in Figure 3.31.

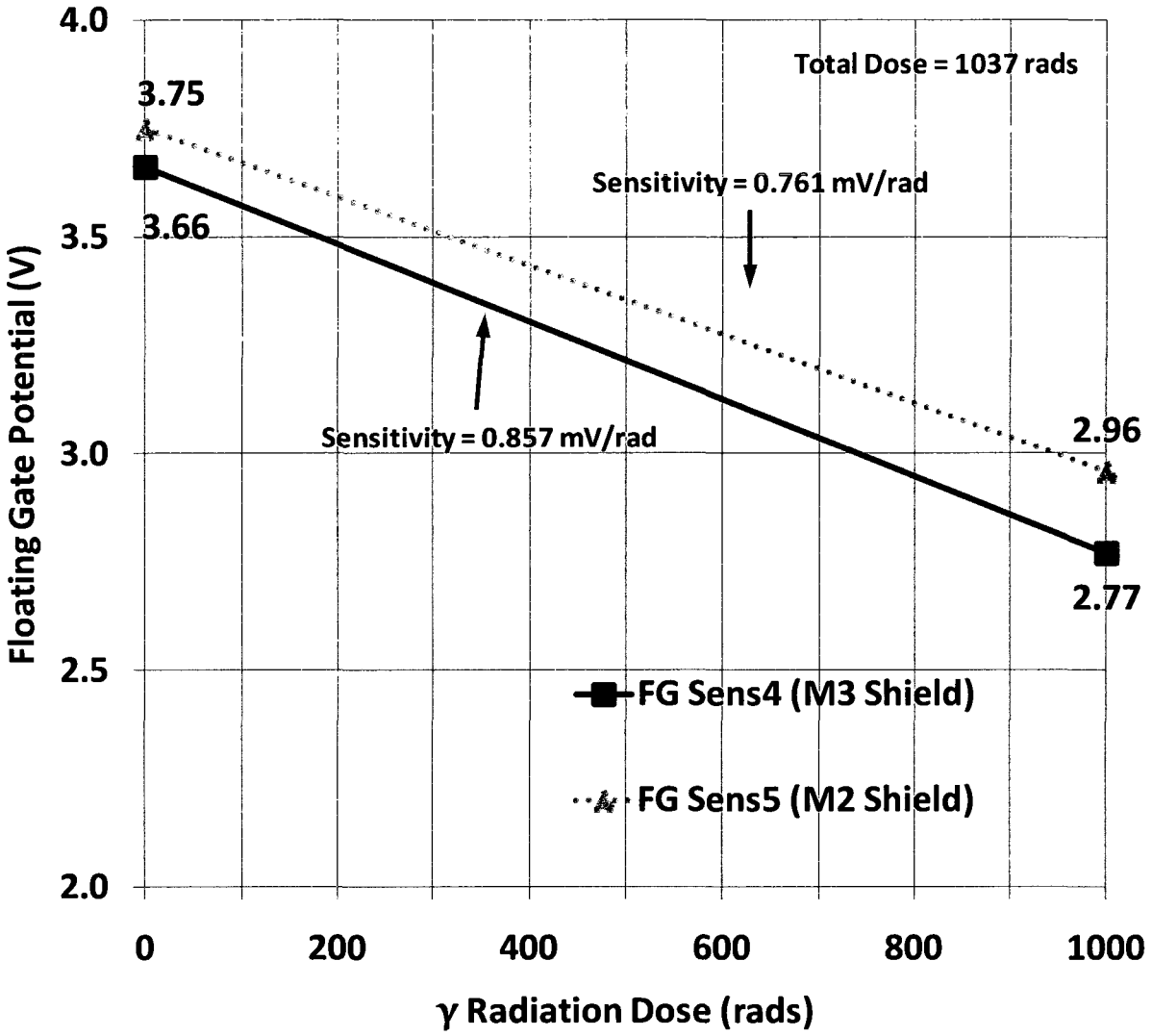


Figure 3.30 Sensitivity of dosimeter with M2 vs. M3 shield under γ-rays

More than 10% gain in sensitivity is observed in the M3 shielded FGRADFET as compared to the M2 shielded RADFET. The improvement could be greater if the devices were programmed at higher potential to attain maximum radiation sensitivity.

Sensitivity Measurements for X-Rays

Dosimeter sensitivity measurements for x-rays have been performed at the Best Medical Canada (BMC) facility. Dosimeter chips with M2 shielded FGRADFETs have been bond wired in a 8-pin DIP package and annealed at 100°C over an extended period of time to achieve stability before measurements were performed. The HP4145A semiconductor parameter analyzer with

test fixture, and custom software to control the programming and capture the measured data through a PC, have been used for programming and measurement of the dosimeter. An X-ray chamber that can deliver a dose of 1 rad/minute has been used. X-ray sensitivity of 5 mV/rad has been observed. The measurements of the FGRADFET sensor are shown in Figure 3.31.

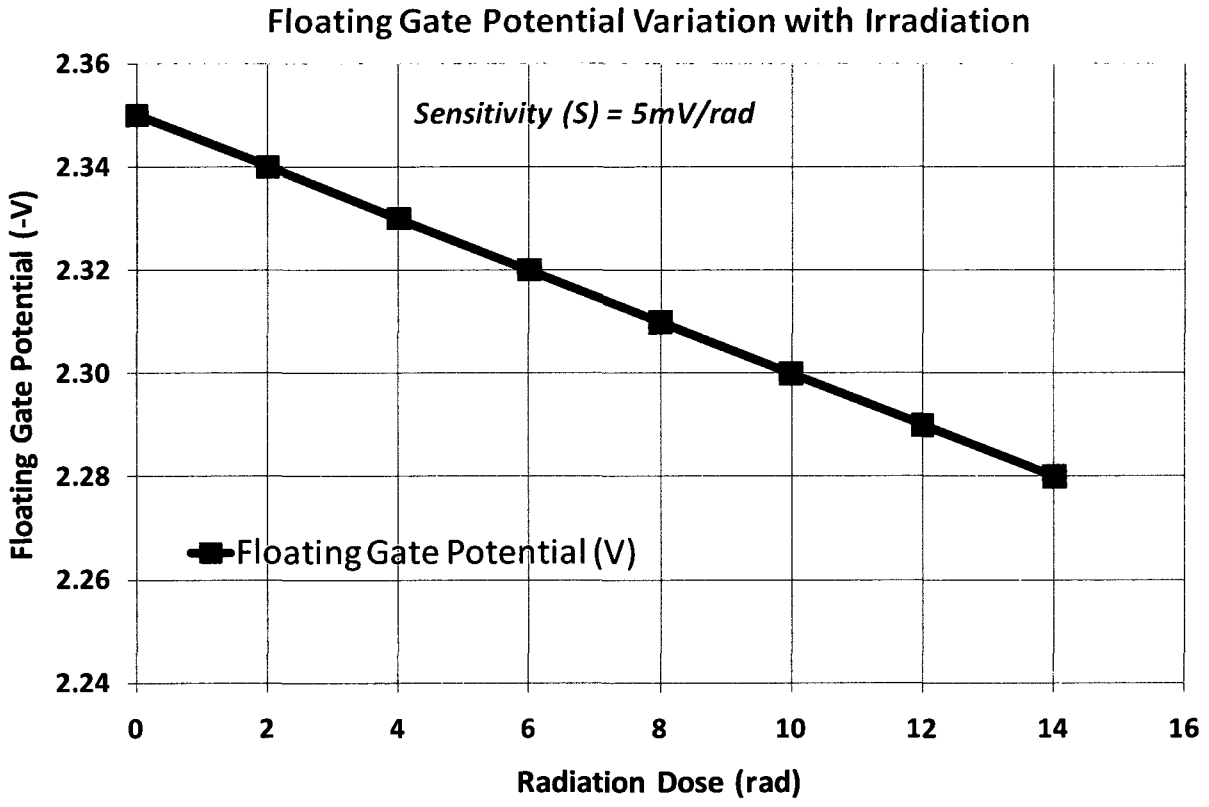


Figure 3.31 Measured x-ray sensitivity of the dosimeter

3.3 Advanced FGRADFET Dosimeter Designs

To further increase the sensitivity and accuracy of the dosimeter and to decrease the effects of noise and other environmental changes (including silicon wafer gradient effects), a few modifications and improvements have been incorporated in subsequent dosimeter designs. The concept and implementation of those improvements, along with the measured results and analysis to quantify their advantages, are as follows.

3.3.1 Design # 2: Interdigitated FGRADFET Structure

Interdigitated structures are common in high performance ASIC layouts to improve the matching of component values, especially differential circuit parameters. Interdigitated structures are useful to reject any gradient and common mode variations.

In this design, as shown in Figure 3.32, the sensor and reference FGRADFETs have been interdigitated together achieving maximum possible on-chip matching to overcome the environmental and process variations. Metal 3 shielding over the floating gate is used in this design. As mentioned in the previous section, it provides more volume for high energy particle, to generate e-h pairs, which in turn increases the radiation sensitivity.

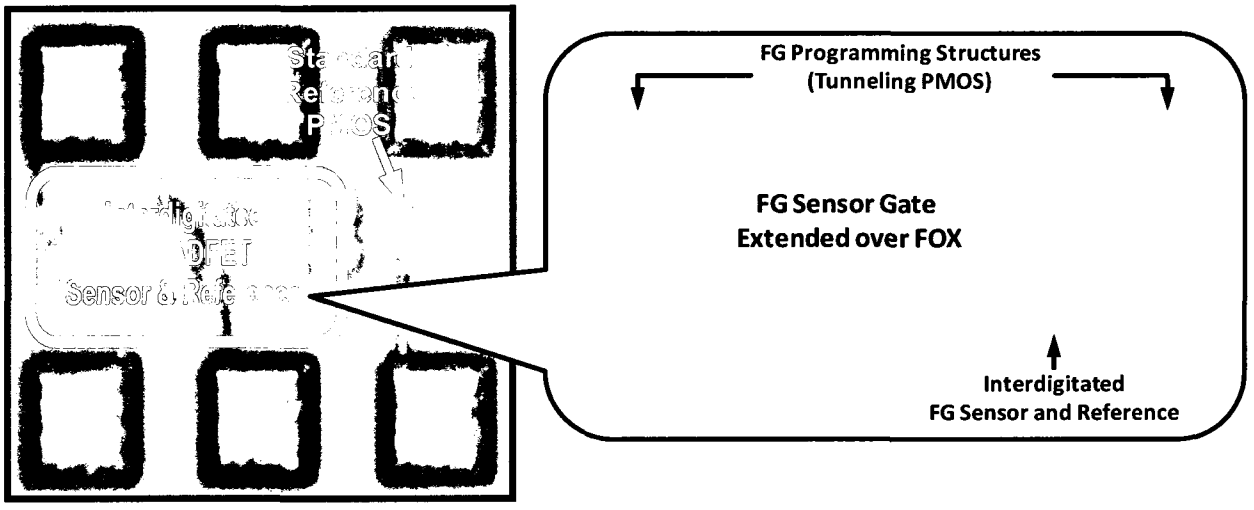


Figure 3.32 Interdigitated dosimeter microphotograph and layout

There is no increase in the absolute sensitivity of the FGRADFET devices through implementation of the interdigitated layout. The advantage it brings is in accuracy, precision and the minimum resolvable radiation sensitivity of the overall dosimeter system. Since any common mode variation is now more efficiently filtered out, smaller values of the incident radiation dose can be measured with accuracy. In Figure 3.33 the comparative performance of standard and interdigitated FGRADFETs has been evaluated by increasing the dosimeter temperature from 20°C to 50°C in steps of 5°C. Both the reference FGRADFETs are tracking the change in sensor FGRADFET very closely below 25°C. At this point the current in both reference

RADFETs start changing at a higher rate than the sensor current. But the change in interdigitated reference is smaller than in the standard reference and it follows the change in FG sensor more closely with changing temperature. This experiment confirms the improved matching and resulting performance enhancement in the dosimeter accuracy for an interdigitated RADFET structure.

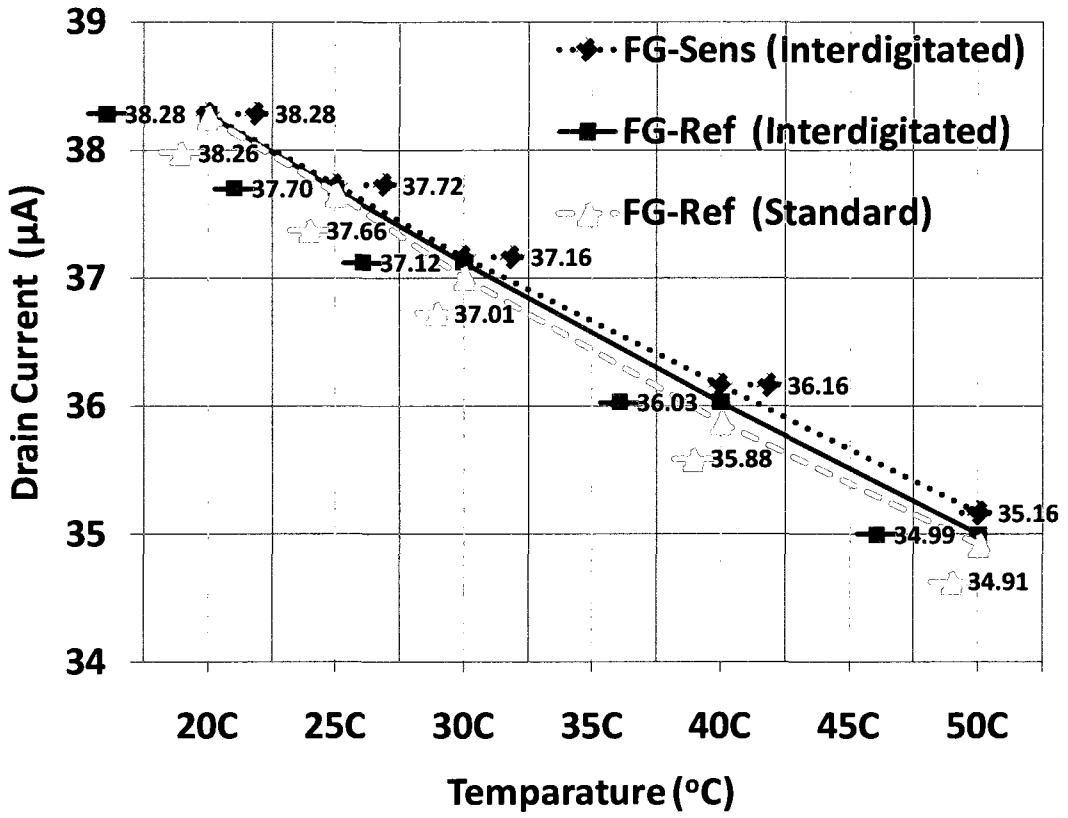


Figure 3.33 Thermal behaviour of standard vs. interdigitated FGRADFET reference

3.3.2 Design # 3: Multiple FGRADFET Structures

Results of the radiation sensor design presented in [75] suggest that stacking multiple sensors improves the sensitivity linearly with the number of stacked units. However study in [38] shows concerns that the most important factor in a RADFET to resolve minimum dose is the inherent flicker noise (1/f) of the MOSFET device. According to [38] stacking multiple sensors will increase the sensitivity but at the same time 1/f noise of individual units will accumulate to increase the minimum level of minimum resolvable dose.

To verify the results presented in [38] and [75], a variation of the first design presented in Figure 3.3 is modified to have two identical sensor and reference FGRADFETs stacked together. The difference from [75] is that the RADFETs are connected in parallel instead of in series. The microphotograph and layout of this design are given in Figure 3.34.

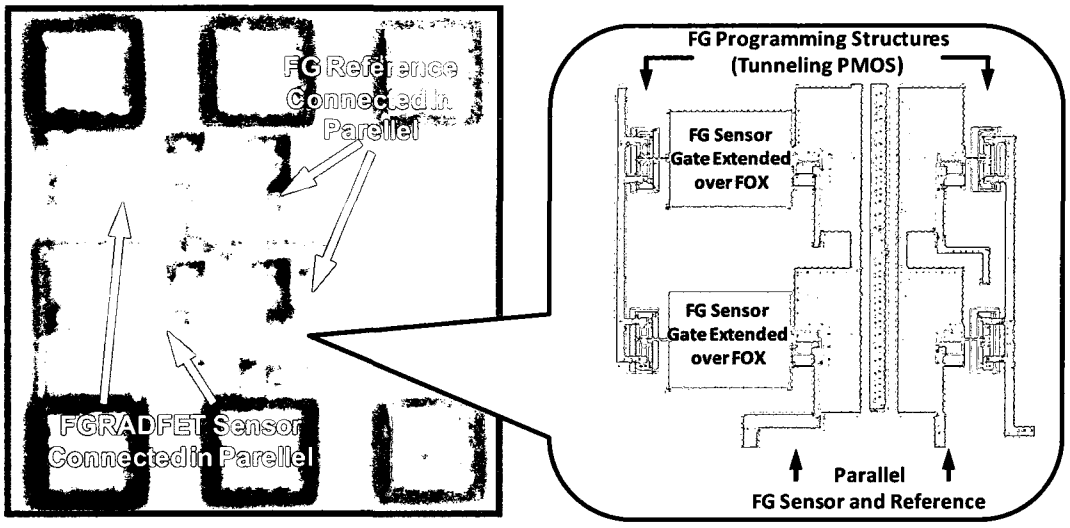


Figure 3.34 Parallel connected FGRADFET based dosimeter layout

To obtain the change in sensitivity due to multiple sensors connected in parallel, equation (3.19) can be modified as,

$$\Delta I_D = q\frac{gm_{FG}}{C_{ox}+C_{fox}+C_{fbpsg}}\frac{D}{W_{e-h}}N(f_{ox}\rho_{ox}A_{ox}t_{ox} + f_{fox}\rho_{fox}A_{fox}t_{fox} + f_{BPSG}\rho_{BPSG}A_{BPSG}t_{BPSG}) \quad (3.23)$$

where N is the number of sensors connected in parallel. For the design shown in Figure 3.34 the value of N is 2.

Comparison of Different Dosimeter Designs for Sensitivity:

A comparison of the individual devices and overall dosimeter sensitivity of a standard FG (SMFG) dosimeter, an interdigitated FG (IFG) dosimeter, and a multiple FG (MFG) dosimeter is provided in Table 3.2 and plotted in Figure 3.35.

Table 3.2 FG Potential and γ-ray Sensitivity of Interdigitated vs. Standard FG Dosimeters

	Initial FG Channel Current I_{Do} (μA)	I_D after 1krad γ-rays dose (μA)	Sensitivity (nA /rad)	Effective Sensitivity of Dosimeter (nA /rad)
MFG Sens	59.92	43.25	16.1	15.1
MFG Ref	61.06	60.09	0.934	
SFG Sens	30.66	22.18	8.18	7.75
SFG Ref	30.31	25.34	0.424	
IFG Sens	33.33	29.87	7.69	5.97
IFG Ref	33.94	32.15	1.72	

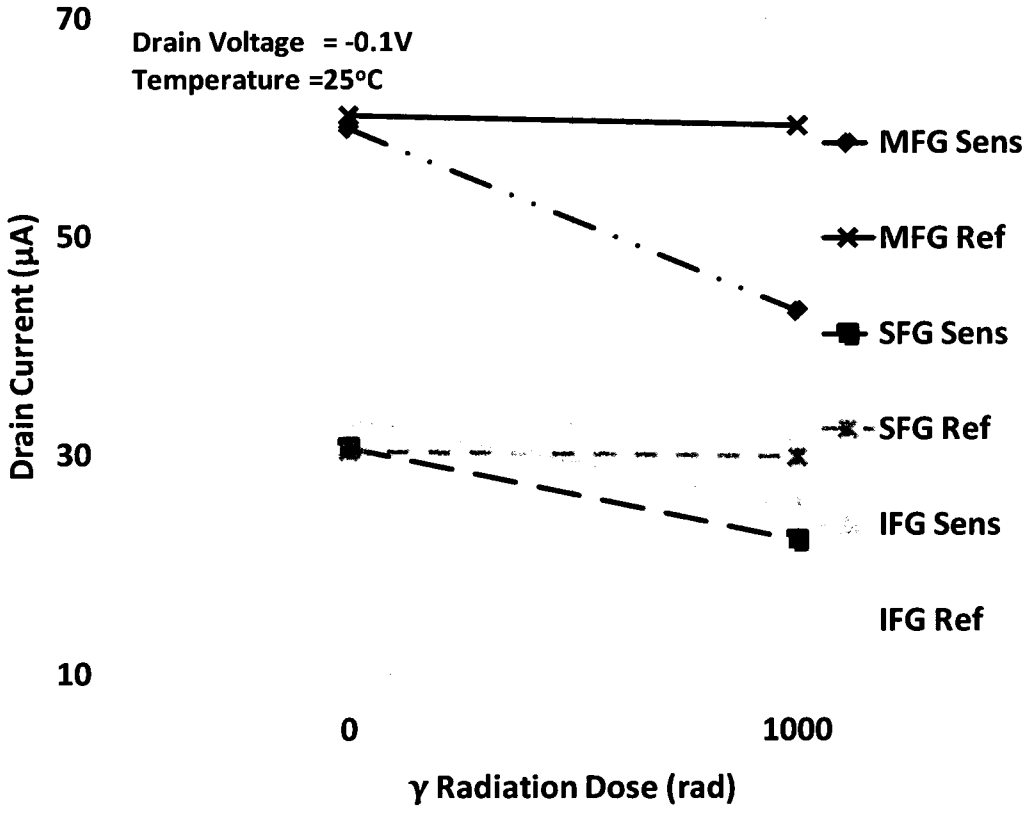


Figure 3.35 Sensitivity of different dosimeter designs

For this experiment, an unpackaged sensor chip that contains all three kinds of dosimeters was used. All FG devices were charged at 25 °C to obtain a channel current of 30 μA as closely as possible. As the MFG dosimeter contains two devices connected in parallel, the total channel current after programming was roughly 60 μA. Upon achieving stability in all FG devices, the channel current through them was measured. All of the devices were then exposed to 1k rad of γ-ray dose. After irradiation, channel currents were measured again to determine the individual device's and the overall effective sensitivity of the dosimeters. In this experiment the measurements are reported in the form of channel current (the actual quantity that is measured in FG devices) instead of FG potential. This is to accommodate the fact that on the MFG dosimeter, the standard PMOS reference was mistakenly left to be stacked. Hence in the absence of an electrically identical standard PMOS structure, the comparison presented in this section is based on channel current of the FG devices.

The results suggest a significant gain in sensitivity of the MFG dosimeter, which is about twice as high as that of a SFG. Effective sensitivity of the IFG dosimeter is lower than the other designs. If individual sensitivities are considered, they are about the same for SFG and IFG dosimeter designs. But the reference FDRADFET of the IFG dosimeter shows more sensitivity than the rest of the references. This brings the effective sensitivity of the IFG dosimeter to the lowest level. A common drain terminal for both FG sensor and reference may be the cause of the increased sensitivity of the IFG reference.

Measured vs. Calculated Sensitivity

The sensitivity of the single and double FGRADFET structures are measured under γ radiation and calculated using equation 3.23. For the measurements, all the process related parameters are obtained from the DALSA 0.8 μm model files, whereas the physical dimensions are taken from the FGRADFET layouts. The value of gm is obtained from PMOS model simulation. Electron-hole pair recombination rates, *R(E)*, of 20 % in the gate oxide, and 25 % in the field oxide and the bpsg regions are utilized to calculate *f* in the corresponding regions, where *f=(1-R(E))*. Results are compared and both measured and calculated values are found in close agreement with each other, as plotted in Figure 3.36.

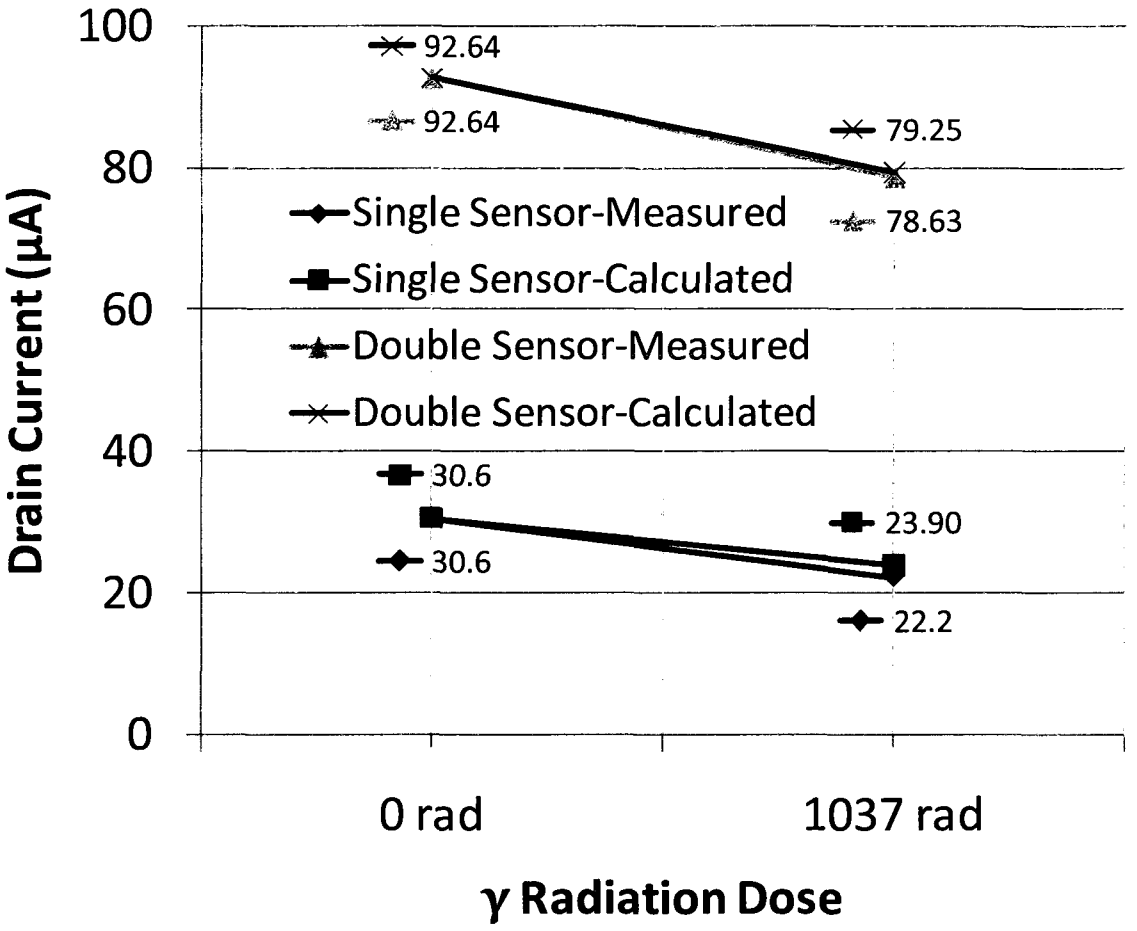


Figure 3.36 Measured vs. calculated sensitivity of single and double FGRADFET

Floating Gate Charge Bounce back:

When FGRADFETs are exposed to the ionizing radiation it is observed that the charge on the FG increased after some time. This is called bounce back. FG potential rebound of up to 6 % within 24 hrs after irradiation has been reported [36]. To observe this behaviour, two day after exposing the new dosimeters to 1 krad of γ-ray dose, the charge on FGs have been measured. The results are presented inTable 3.3. Maximum change of 0.41 % has been observed which shows a completely different and very stable post radiation behaviour of new FGRADFETs fabricated in DALSA 0.8 μm CMOS.

Table 3.3 FG Bounce back after 1 krad γ-Ray Dose

	Channel current (I_d) after 1 krad γ-ray dose (μA)	Bounce-back after 2 days (μA)	% Change
SFG Sensor	54.215	54.435	0.41
SFG Reference	57.835	57.981	0.25
IFG Sensor	57.237	57.286	0.09
IFG Reference	61.244	61.49	0.40
MFG Sensor	78.629	78.678	0.06
MFG Reference	93.496	93.365	-0.14

3.4 Comparison of Semiconductor Radiation Sensors

Table 3.4 presents a comparison of the radiation sensors found in the literature with the dosimeters developed in this work. Even with zero bias, the smallest FG area, and most importantly, the thinnest field and gate oxide, the sensitivity of the dosimeters is comparable. If the same design would be fabricated in thicker oxide processes, which are commercially available but not offered by Canadian Microelectronics Corporation (CMC), a **significant improvement in the sensitivity** would be observed by taking advantages of the techniques presented in this chapter.

Table 3.4 Comparision of Dosimeters

Parameter	[4]	[35]	[36]	[33]	[43]	[21]	This Work	This Work
Technology	Specialized Process (TOT-500)	1.5 µm, CMOS	1.5 µm CMOS	1.2 µm BICMOS	Unknown Process	Unknown Process	DALASA 0.8 µm CMOS	DALASA 0.8 µm CMOS
Irradiation Bias	0	0	0	12	5	5-20	0	0
Sensor Size (µm)	-	20x20 Active, 50x200 Fox	20x20 Active, 100x400 Fox	2.4x1.2	-	2x2mm Active 200x200	4 x 20 Active, 80 x 100 Fox	8 x 20 Active, 160 x 100 Fox
Device Type	RADFET	FG MOSFET	FG MOSFET	FG MOSFET	RADFET	RADFET	FG MOSFET	FG MOSFET
Sensitivity (mV/rad)	0.18	0.7	3	- 4 nA/rad	6	1.0 - 2.7	1.5 (7.75 nA/rad)	3 (15.1 nA/rad)
t_{ox} (nm)	250	27	27	-	1000	-	17	17
Fox (nm)	-	600	1000	-	-	-	450	450

3.5 Summary and Contributions

In fulfillment of the first four thesis objectives, this chapter has presented a novel low power dosimeter architecture. In addition, the design of enhanced sensitivity FG sensor was described. Three novel dosimeter designs for improved accuracy and radiation sensitivity were presented. Finally a performance comparison of the new dosimeters with previously reported designs was performed.

A new architecture has been adopted that enables low power operation. The resulting dosimeter can operate at voltages as low as 0.1 V. While this new architecture was initially intended to improve the accuracy, such improvement was not obtained.

A new FG sensor structure has been developed. A mathematical analysis quantifying its sensitivity has been presented for the first time.

The FG sensor's unique programming characteristics and procedures have been discussed in detail. Further, extensive thermal and stability analysis (experimental based) have been performed. A successful stabilization procedure for the sensor has been proposed. Finally, a detailed assessment of the sensor's accuracy has been carried out. It was found that the elevated metal shield (M3) increases sensitivity by 10% compared to the M2 shielded design.

The FG sensor was then employed in three novel low power dosimeter designs, all fabricated in the commercially available DALSA 0.8 μm CMOS process and experimentally validated. The first design, consisting of a dual FG structure, was fully characterized in terms of sensitivity and accuracy.

The second design employed an interdigitated FG sensor and reference and was found to exhibit improved accuracy compared to the previous design. However, its sensitivity was slightly lower.

The third design consisted of multiple sensors stacked in parallel and was seen to provide increased sensitivity proportional to the number of devices, without compromising accuracy. For the two-device sensor developed in this work, a sensitivity of 3 mV/rad (15.1 nA/rad) was achieved.

These results represent the first contribution of the thesis, namely "high sensitivity radiation sensor". The work of this chapter has led to one published journal paper [7] and another submitted journal paper [13] and one provisional patent [15].

Chapter 4

Monolithic Dosimeter and its Wireless System Implementation

Having demonstrated in Chapter 3 a low power dosimeter with attractive performance, the issues of monolithic integration of SPE and wireless system integration may now be discussed. In accordance with the fourth and fifth objectives of this thesis, a novel monolithic dosimeter suitable for wireless applications is presented in this chapter. The design of a wireless TX and the selection of an appropriate power source are presented. A system implementation of the SoC wireless dosimeter is given. Finally, a performance comparison of the new wireless dosimeter with previously reported designs is carried out.

4.1 Monolithic Dosimeter with Readout Circuitry

The most innovative part of the wireless dosimeter design is the monolithic integration of the readout circuit. The novel low power dosimeter architecture presented in chapter 3 has made it possible to achieve high sensitivity at normal chip voltages. This opens the doors for monolithic integration of the readout circuitry along with radiation sensors. The design, measurements, and analysis of a first-of-its-kind monolithic dosimeter are presented in the following sections.

4.1.1 Proposed Design of the Monolithic Dosimeter

The novel low power dosimeter architecture presented in the previous chapter is employed to design a monolithic dosimeter having integrated readout circuitry suitable for wireless dosimetry. The basic concept of the monolithic dosimeter is illustrated in Figure 4.1. Two

FGRADFETs, a sensor and a reference, are connected to on chip signal processing electronics (SPE). The SPE is responsible for producing output in the desired form and voltage level. A fully differential scheme has been adopted for the sensors and SPE circuit elements to compensate for first order variations in the current with temperature, and other on-chip gradient effects.

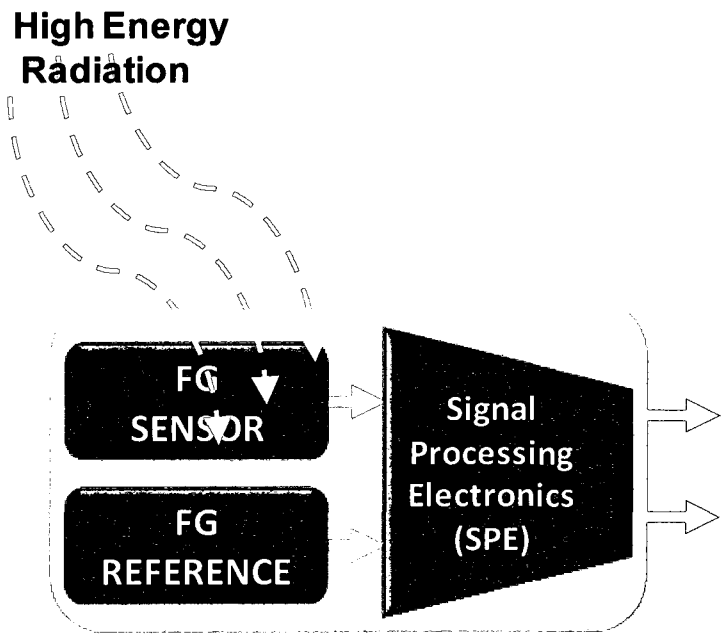


Figure 4.1 Monolithic dosimeter proposed block diagram.

As radiation falls on the dosimeter chip with pre-charged FGRADFET based sensor and reference, it discharges the FG potential which in turn decreases the current through the FGRADFETs. The change in current is proportional to the amount of discharge on the FG, which in turn is proportional to the incident radiation dose. As described in chapter 3, the FGRADFET reference has no gate extension over the FOX. Hence, it is significantly less sensitive to the radiation and, after exposure to the radiation, the change in current through the FG sensor and the reference will be different. On-chip SPE circuitry converts the currents through the sensor and reference to the equivalent voltages and produces an output in the desired range, as a function of these voltages. The chip was designed and fabricated in DALSA 0.8 μm CMOS process. A microphotograph of the fabricated dosimeter with integrated SPE is shown in Figure 4.2.

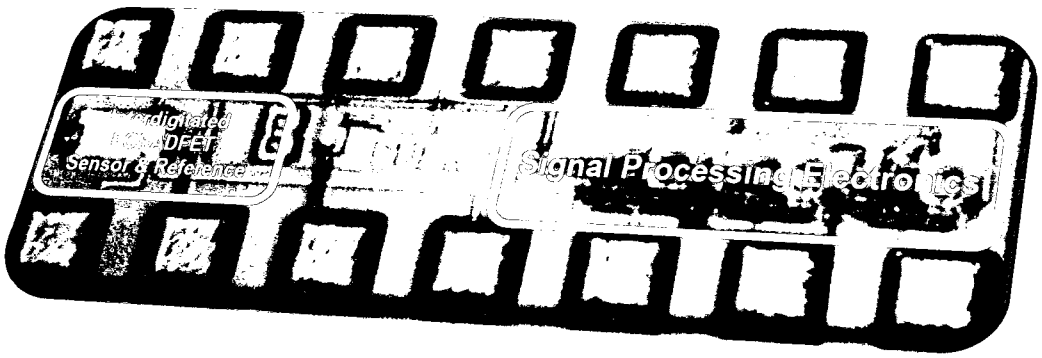


Figure 4.2 Microphotograph of the dosimeter chip.

4.1.2 Signal Processing Electronics (SPE)

The signal processing electronics (SPE) integrated with the above dosimeter is designed to work in continuous reading mode. The output of the dosimeter will reflect any change due to the incident radiation without delay. The monolithic dosimeter circuit diagram including SPE is as illustrated in Figure 4.14.

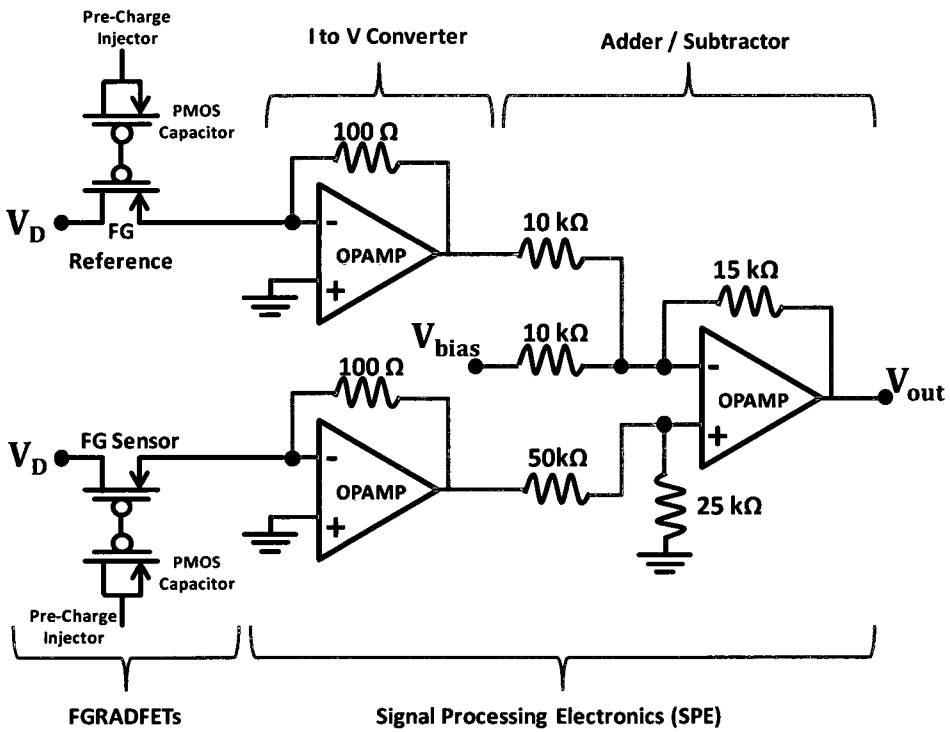


Figure 4.3 Circuit diagram of the monolithic dosimeter

The heart of the SPE is the dual supply operational amplifier (op-amp). The schematic of the op-amp is illustrated in Figure 4.4.

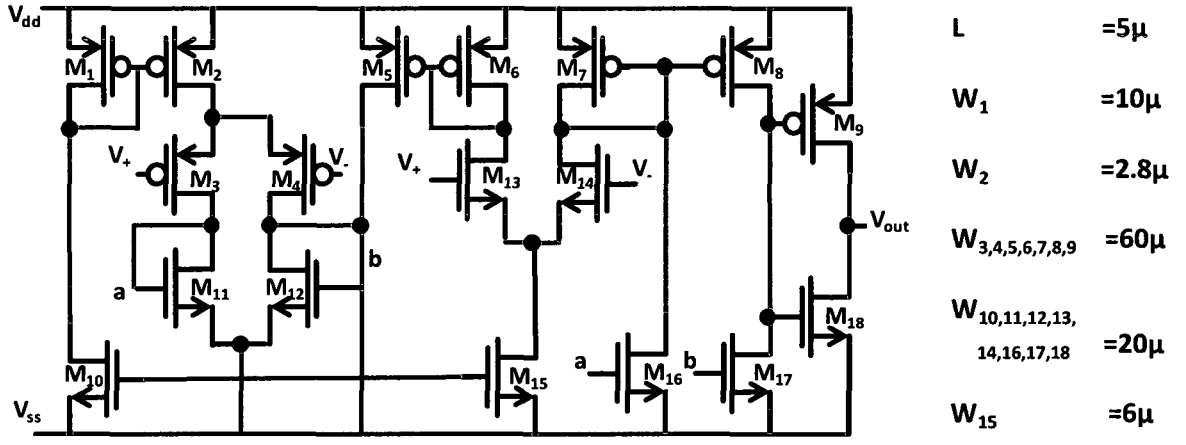


Figure 4.4 Schematic of the operational amplifier designed for SPE

This is a dual supply three stage high gain op-amp with an output buffer. The measured open loop gain is 70 dB. Dual supply op-amps have zero potential at the input terminals that help to avoid dc level shifts in the output terminal of the previous stage. As there is no feedback in this design, no compensation circuit is needed.

As illustrated in Figure 4.3, the SPE has two stages. The first stage is an active I to V converter. It converts the FGRADAT channel currents (I_{in}) into equivalent voltage ($V_{out} = -I_{in}R$, R is feedback resistor). The operation of this basic op-amp based I to V converter is illustrated in Figure 4.5 .

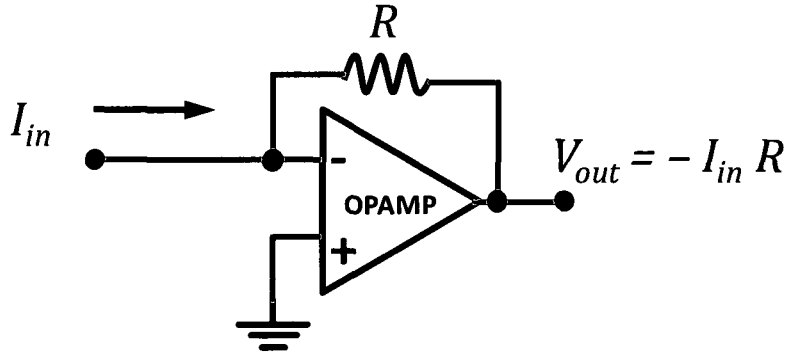


Figure 4.5 Schematic of a simple active I to V converter

The second stage of the SPE is an adder / subtractor that is designed to produce the output voltage in the desired range using converted voltage signals from FGRADFET devices. The same op-amp was used to implement the second stage. The function of the adder circuit given in Figure 4.6 as follows.

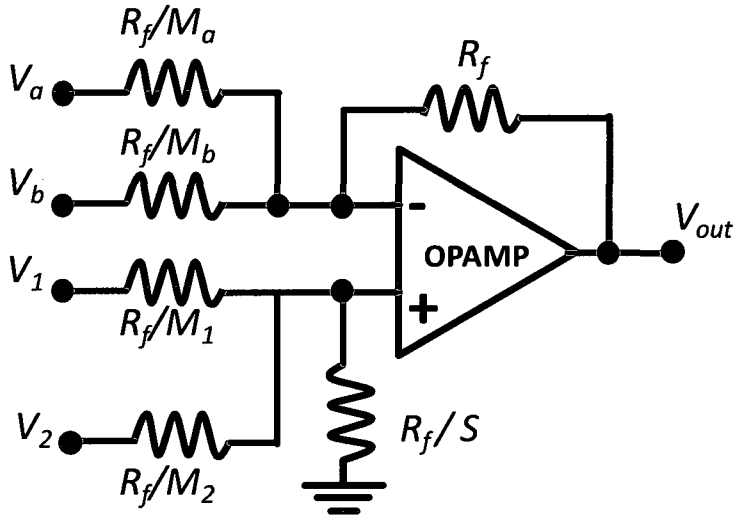


Figure 4.6 Schematic of adder subtractor used in SPE design [76]

The required output from the generic circuit presented in this figure can be achieved using basic design relationships.

$$V_{out} = (V_1M_1 + V_2M_2) - (V_aM_a + V_bM_b) \quad (4.1)$$

and

$$S = 1 + (M_a + M_b) - (M_1 + M_2) \quad (4.2)$$

where M_a, M_b, M_1, and M_2 are the gains of inputs V_a, V_b, V_1, and V_2 respectively, and R_f is the feedback resistor. Any appropriate value of R_f can be chosen and the rest of the resistor values can be calculated using this value along with the desired gain.

Combining the results from the two sub circuits, appropriate component values have been calculated for the desired output voltage (0.3 V to 0.8 V to drive the TX VCO given in Sec. 4.3) of the SPE block. The circuit of Figure 4.3 shows the resulting component values.

Layout Considerations:

The layout of the entire monolithic dosimeter with interdigitated FGRADFET structure is shown in Figure 4.7. All circuit components were carefully implemented using common centroid and interdigitated layout techniques to achieve maximum accuracy and minimize error due to on-chip circuit component mismatches. Dummy resistors were used at the corners to provide each resistor as identical operating condition as possible. For the adder / subtractor part of SPE, matching the values of resistors is very important as the output voltage shift is dependent upon ratios of resistor values, and any mismatch in the values due to poor layout may result in an error in the output voltage which eventually will be translated into incorrect radiation dose measurements.

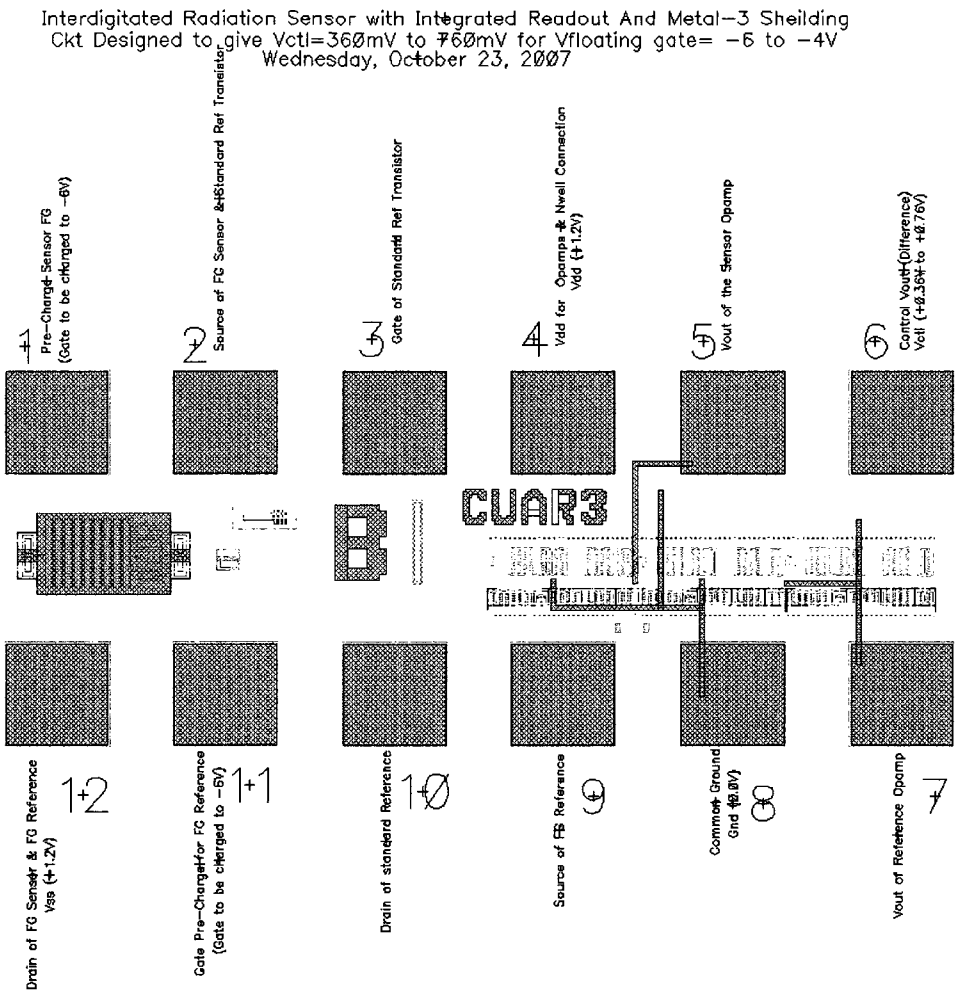


Figure 4.7 Layout of monolithic interdigitated dosimeter with SPE

4.1.3 Experimental Results

The SPE has been implemented on all three dosimeter designs discussed in chapter 3. All designs have been fabricated in DALSA's 0.8 μm process and tested at the National Research Council of Canada's Institute for National Measurement Standards (NRC-INMS) radiation testing facility to verify functionality and evaluate their performance. Cobalt-60 (^{60}Co) was used as the γ radiation source. The dose measurement setup is depicted in Figure 4.8. A plastic sheet approximately 5 mm thick was positioned in front of the dosimeter to serve as a build-up layer, and a plastic block thick enough to provide complete back scatter was placed behind the dosimeter. Irradiation was carried out in 100 rad increments.

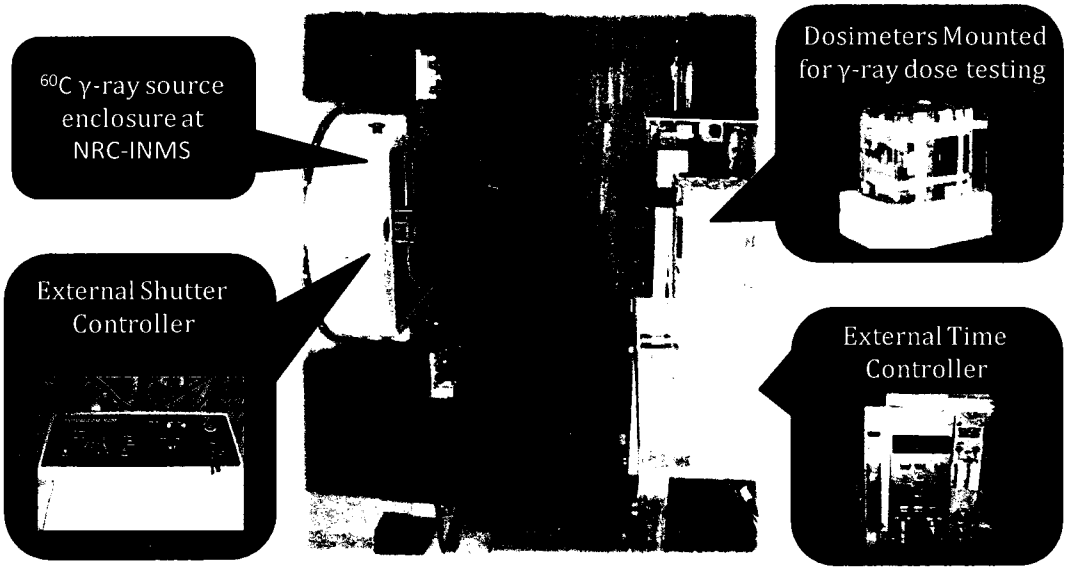


Figure 4.8 Dosimeter testing setup for γ radiation dose measurements at NRC-INMC

The SPE was designed assuming an initial programmed charge of -6 V on FGRADFETs with sensitivity of 2 mV/rad. Hence a 1 krad radiation dose is sufficient to bring the FG charge down to -4 V. The SPE was tailored to give a change in output from 350 to 750 mV for this change in the FG sensor potential. Measurement results are given in Table 4.1 showing the change in the output voltage verification of the monolithic dosimeter. The dosimeters' SPE output is also plotted in Figure 4.9. These results are very significant, marking the first ever demonstration of a monolithic dosimeter. The results show that multiple FG (MFG) dosimeter is the most sensitive of the three designs, with the interdigitated FG design (IFG) having least sensitivity.

Table 4.1 γ-ray Sensitivity of Different Monolithic FG Dosimeters with SPE

	Initial Monolithic Dosimeter Output (mV)	Monolithic Dosimeter Output after 1krad γ-rays dose (mV)	SPE Sensitivity (mV /rad)
IFG Dosimeter	325	425	0.097
SFG Dosimeter	320	447	0.122
MFG Dosimeter	350	675	0.313

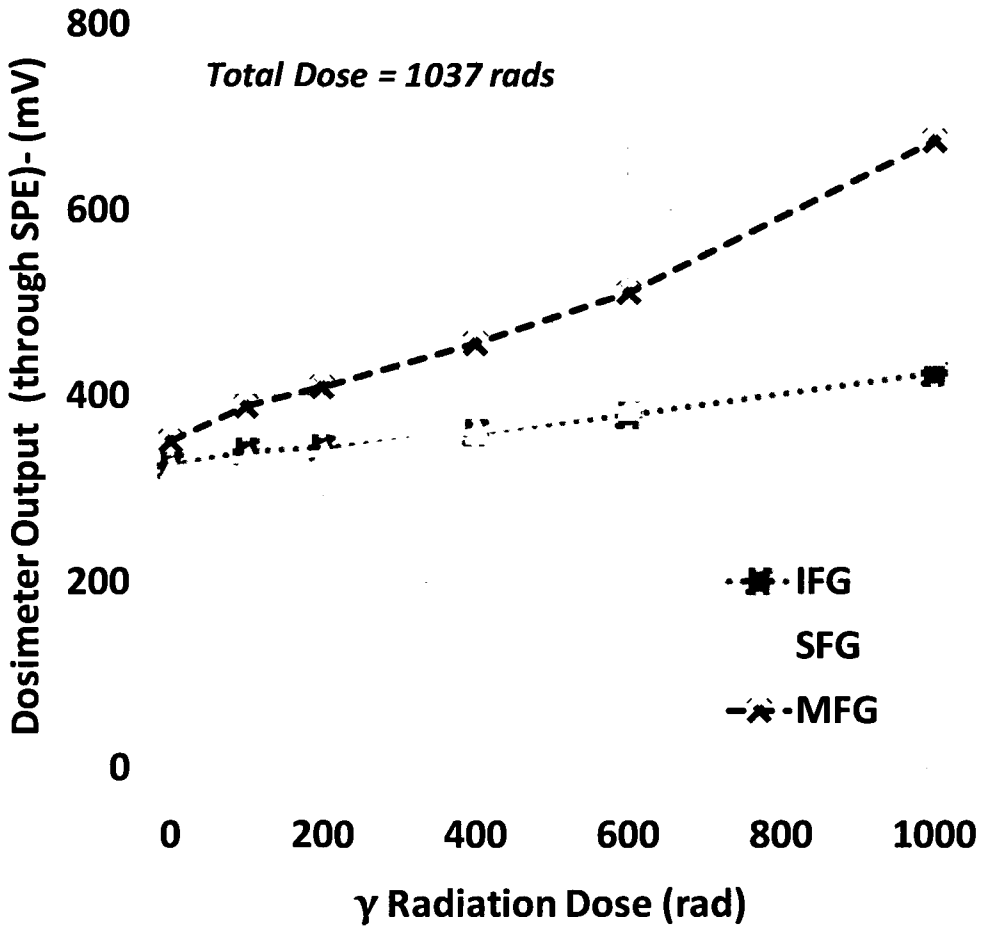


Figure 4.9 Sensitivity of different monolithic dosimeter designs

Another important observation is the reliable circuit performance under heavy radiation dose. After being exposed to total 1037 rad of γ–ray dose, all of the monolithic designs were behaving properly and generating the output as designed.

4.1.4 Negative Bias Generator (NBG)

To generate all the required bias voltages, and to facilitate integrated dosimeter programming circuits which require very high negative voltages for p-type FGRADFETs, a charge pump based negative bias generator test circuit has also been designed and implemented in DALSA 0.8 µm technology. The charge pump generates different negative voltage levels using positive supply voltage which is +1.2 V in this case. The schematic and layout of the negative voltage generator is illustrated in Figure 4.10 and Figure 4.11 respectively. The design is based on the basic Dickson architecture [77]. In the event where a clock is present in the design, this circuit can be very useful to eliminate the need for multiple biasing voltages. In absence of the clock, an on-chip ring oscillator with frequency counters can be implemented to produce the required clock for a complete self sufficient SoC solution.

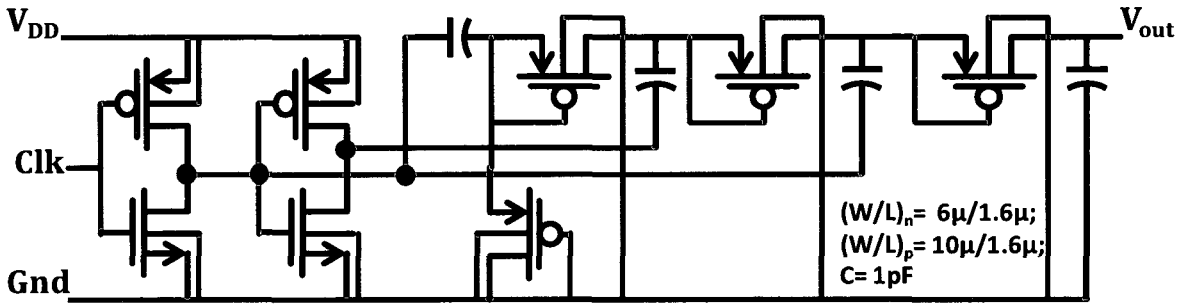


Figure 4.10 Schematic of negative bias generator (NBG)

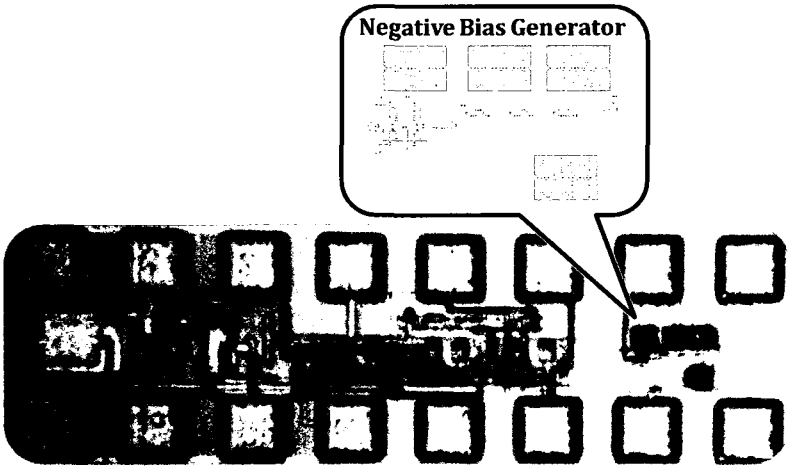


Figure 4.11 Microphotograph of monolithic dosimeter with negative bias generator (NBG)

Figure 4.12 shows the output of the NBG using +1.2 V power input and a 1MHz clock. The measured output is slightly higher than the simulated value.

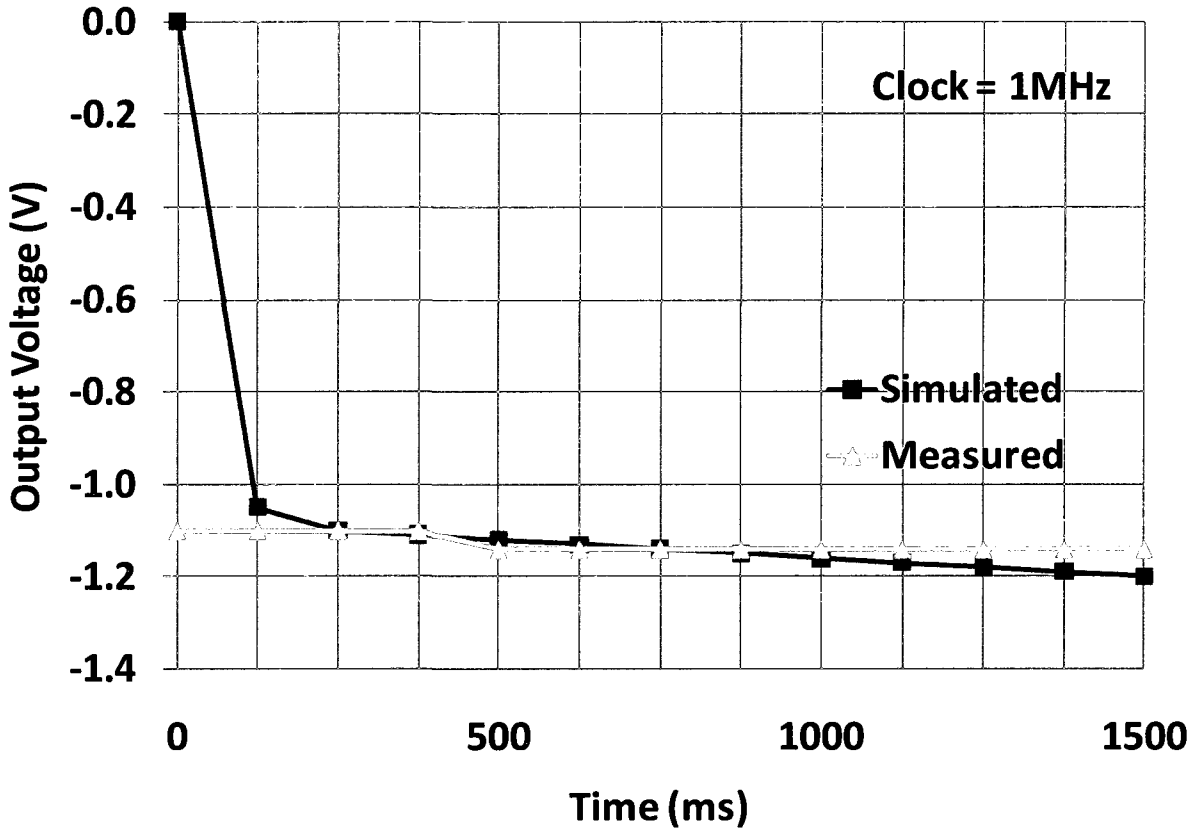


Figure 4.12 Measured vs. simulated output of NBG with clock frequency of 1 MHz

The output voltage, V_{out}, of the Dickson charge pump based NBG can be calculated as [77],

$$V_{out} = V_{DD} + n\,(V_{DD}-V_{th}) \tag{4.3}$$

where V_{DD} is supply voltage, V_{th} is the threshold voltage of MOS device used in the circuit, and n is the number of stages. This relationship is true for smaller (< 10) number of stages.

To generate low voltages such as the case above, Dickson's architecture is still usable and efficient, however for high output voltages where a large number of stages are needed , such as FG programming voltages, more efficient NBG architectures are available for example charge pump based circuit presented in [77].

4.2 Power Source

Prime requirements of a power source for the dosimeters are small size and transparency to incident radiation. A lithium polymer battery and ultra charged capacitors are the two options that fulfill these requirements and are commercially available. A brief overview of the two technologies follows.

4.2.1 Lithium Polymer Cells:

Lithium polymers (Li-polymer) are rechargeable batteries or secondary cells. Li-polymer cells are used in a wide variety of portable equipment and instruments. Lithium polymer cells have the flexibility to mould into the form factor of the application, such as cell phones, PDAs, cameras, or wireless sensors. The most important characteristic of Li-polymer that makes it usable for wireless dosimeter applications is its transparency to radiation. It is very light weight. The electrolyte is in the form of a gel instead of liquid, which enables simplified packaging. Li-polymer cells however have lower energy density compared to primary cells, but for the wireless dosimeter application where power is only needed for short period of time during the radiation exposure, this is not a main concern. Cells can be charged before each use. In Figure 4.13 a commercially available Li-poly cell is shown. The size of the cell is roughly 1.5 cm^2.

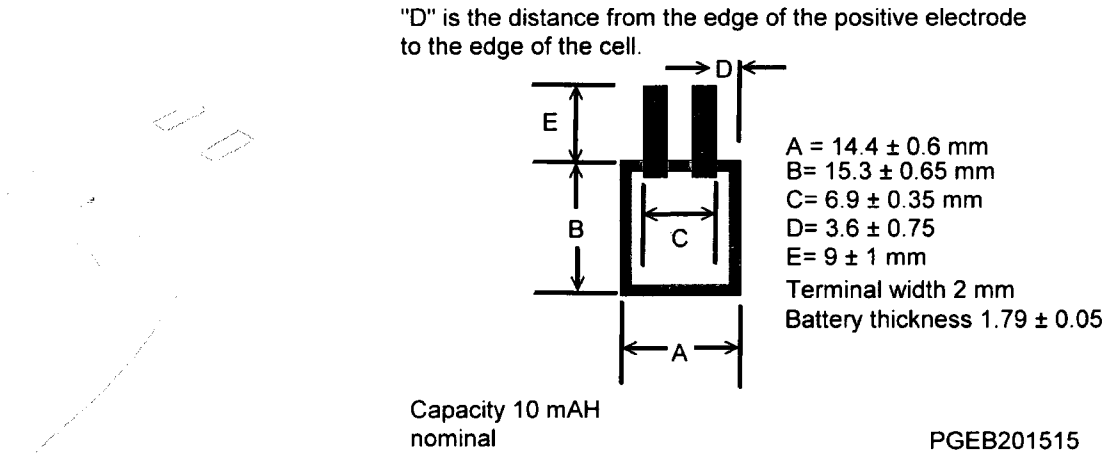


Figure 4.13 A commercially available Li-polymer battery [78]

4.2.2 Ultracapacitors

Ultracapacitors have the potential to meet the power supply requirements of a self powered wireless dosimeter. The advantages of ultracapacitors relative to conventional off-chip batteries are high power density, high efficiency, fast recharging, long shelf and cycle life. Ultracapacitors, however, have a lower energy density when compared to these batteries, especially in the case of high power requirements [79]. For the SoC dosimetry transceiver architecture, an ultracapacitor with voltage regulator circuitry can be implemented.

4.3 System Integration of Dosimeter with Wireless Transmitter

Finally, after achieving the low power and high sensitivity dosimeter in chapter 3, and successful monolithic integration of SPE on dosimeter chip earlier in this chapter, the step to achieve an SoC wireless dosimeter transmitter is the individual component integration in a single SoC wireless TX module. The schematic of the entire wireless dosimeter TX module is illustrated in Figure 4.14.

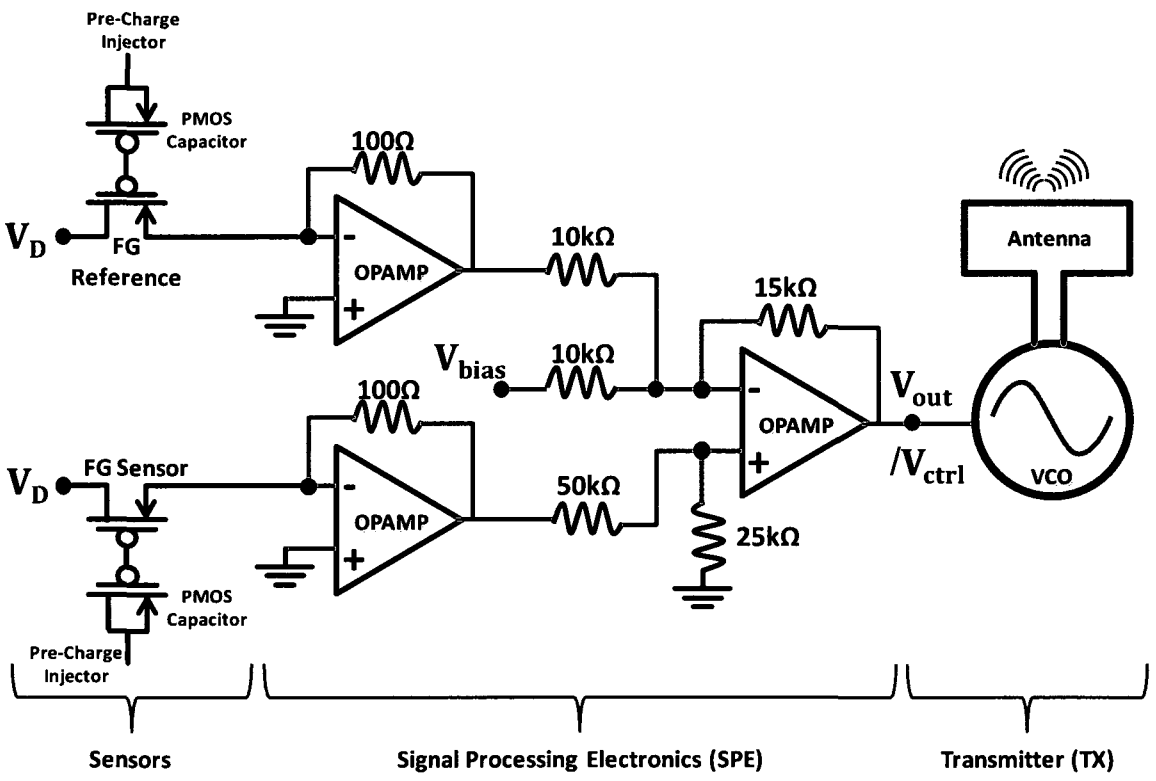


Figure 4.14 Wireless SoC dosimeter system schematic

The final link to the wireless transmitter module is the TX circuit. To show the feasibility of a wireless dosimeter, a simple voltage control oscillator (VCO) based TX has been designed with an on-chip antenna. The SPE on the monolithic dosimeter chip has been programmed to produce the output voltage to modulate the oscillating frequency of the VCO via its voltage control line. As mentioned in chapter 1, a low power TX with on-chip antenna suitable for short range wireless applications has been designed by fellow Ph.D. student Atif Shamim. A simplified schematic of VCO with on-chip antenna is given in Figure 4.15.

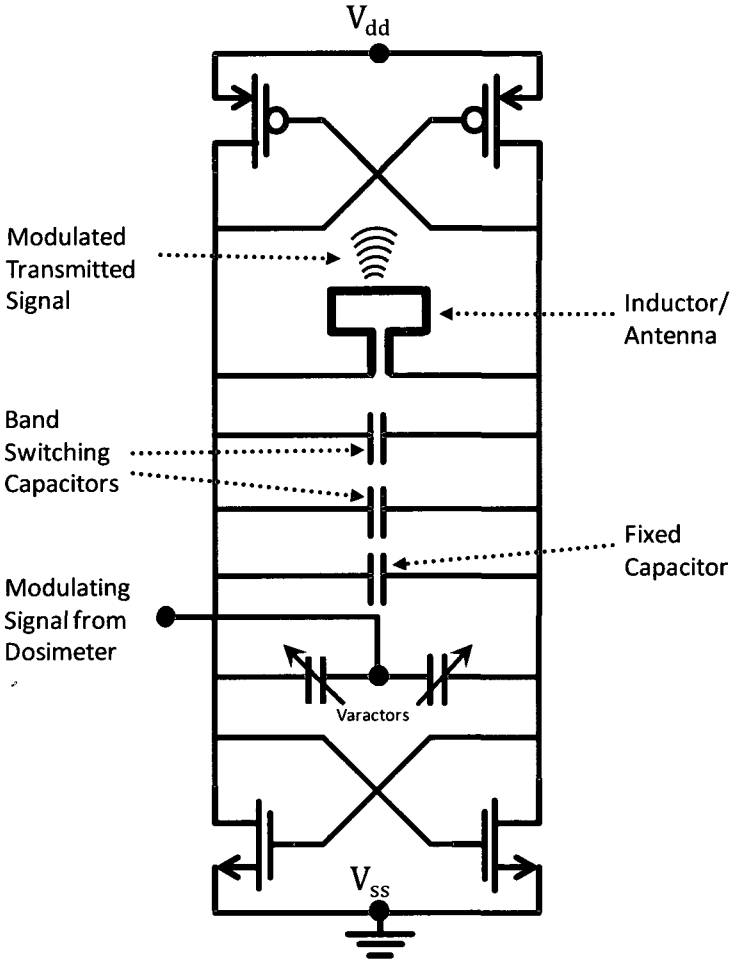


Figure 4.15 Wireless TX schematic with an on-chip antenna

The wireless dosimeter system is designed to work in the license free U-NII band (5.2 GHz). The SPE integrated with the monolithic dosimeter was custom designed to work with this TX. To begin the system level design, so that individual components will eventually fit together

without any interfacing and design issues, a few assumptions were initially made. As mentioned during the monolithic dosimeter design, it was assumed that the FG devices will be charged to -6V, have γ- ray sensitivity of 2 mV /rad, and when exposed to 1krad dose, will decrease its potential to -4 V. The SPE was designed to generate an output of 350 mV to 750 mV for this range of radiation dose. 200 MHz change in TX frequency was observed corresponding to the 350 – 750 mV change in the control voltage of the VCO. Figure 4.16 shows the output of the complete monolithic dosimeter and the TX frequency at that output. Both components are designed jointly to work with each other as a wireless dosimeter.

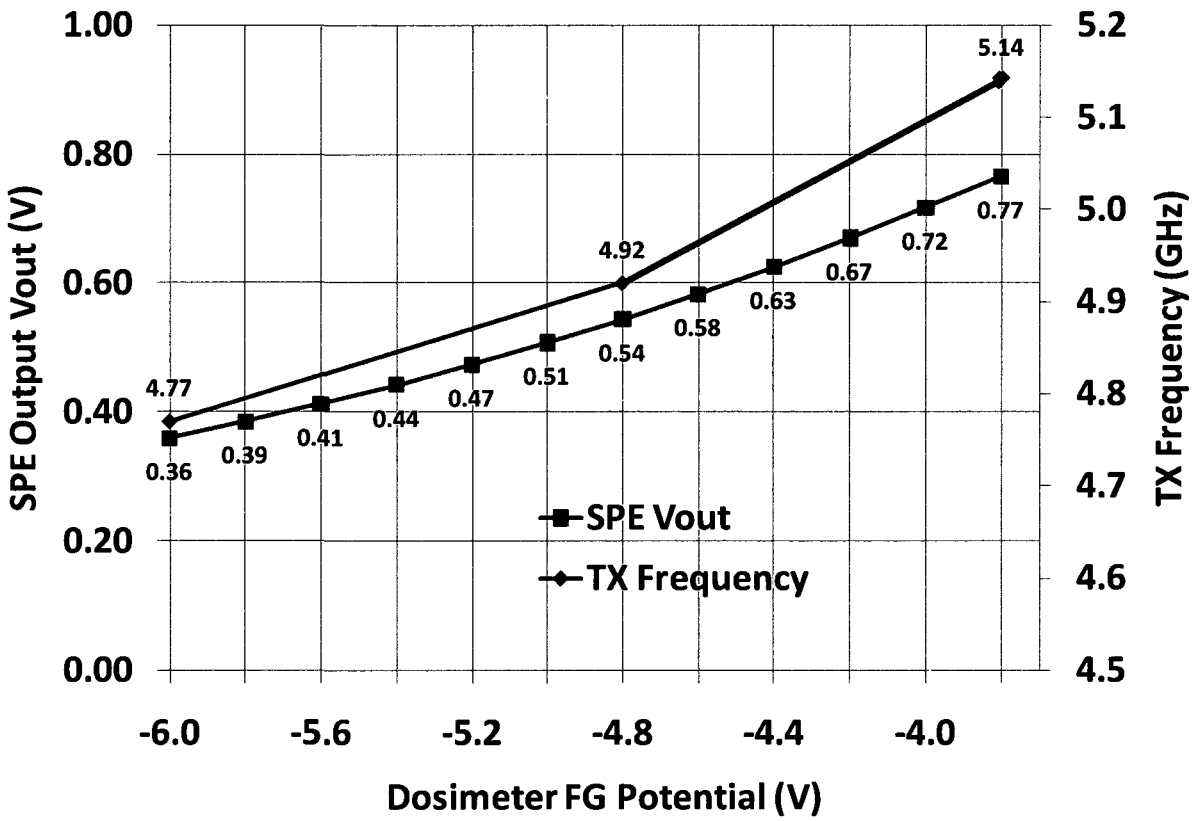


Figure 4.16 Simulated output of the dosimeter produced by SPE designed to work with TX along with change in TX frequency

Due to radiation test setup limitations, the entire system was not irradiated in the form of a single wireless dosimeter module, but extensive measurements of the individual components have been performed which prove the feasibility of a miniaturized SoC wireless radiation

sensor. Measured results of all the components are presented in Table 4.2 and Figure 4.17. The performance of individual wireless dosimeters is consistent with previous results. The change in the frequency of dosimeter with incident radiation dose can be easily measured and related to the radiation dose upon calibration.

Table 4.2 γ-ray Sensitivity of Wireless Dosimeter

	Radiation Dose = 0 (rad)		Radiation Dose = 1037 (rad)		Sensitivity (GHz/rad)
	Dosimeter Output (mV)	VCO frequency (GHz)	Dosimeter Output (mV)	VCO frequency (GHz)	
IFG Dosimeter	325	5.16	425	5.05	106×10^{-6}
SFG Dosimeter	320	5.18	447	5.0	174×10^{-6}
MFG Dosimeter	350	5.12	675	4.7	405×10^{-6}

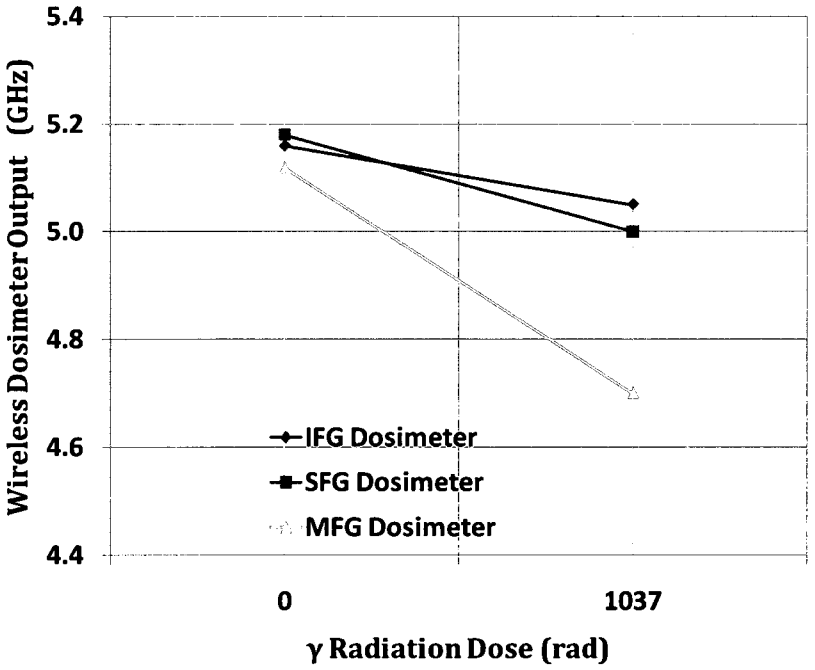
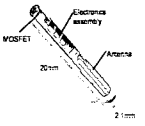
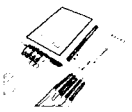
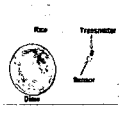


Figure 4.17 Radiation response of the new wireless dosimeters

This is the first FG wireless dosimeter for radiotherapy applications. A comparison of the new design with existing dosimeters is presented in Table 4.3. It can be concluded that the dosimeter design presented in this work is the **smallest reported wireless dosimeter** with highest sensitivity for radiotherapy applications.

Table 4.3 Comparison of Wireless Dosimeters

	[17]	[18]	[19]	[20]	This Work
					
Module Size	84 x 48 x 17.5 mm	20x2.1 mm	1.5 cm dia 3 mm thick	17.8 x 15.9 x 4.2 cm	2 mm^2 SoC
Communication Frequency	125KHz	-	7 MHz	2.4 GHz	5.2 GHz
Range	1.2-2.4 m	12 cm	3-5 cm	10 m	1.5 m
Model	DMC 2000S	DVS	-	TN-RD-70-W	SoC
Sensitivity	-	0.45 mV/rad	11.45 Hz/rad	2.7 mV/rad	3 m V/rad
Sensor Size	-	0.3x5 µm	-	0.2x0.2mm	4 µ x 20 µ
Comments	Not for Radiology	In-vivo	Extremely Insensitive	with high bias	460 µ x 1111 µ = 0.5 mm^2

A comparison of the achieved vs. target specifications of the wireless SoC dosimeter is presented in Table 4.4. It is evident from the table that all of the desired specifications have been fulfilled by the wireless SoC dosimeter design presented in dissertation.

Table 4.4 Achieved vs. Target Specifications of the Wireless SoC Dosimeter

Parameter	Target Specification	Value Achieved
Sensitivity	> 1 mV/rad	1.5 mV/rad
Power	< 10 mW	5.3 mW
Size	0.5 cm x 0.5 cm	0.5 cm x 0.5 cm
Wireless Communication Range	> 1 m	1.5 m

4.4 Summary and Contributions

This chapter has presented the monolithic integration of signal processing electronics with the new radiation sensors, and the implementation of a novel wireless dosimeter system, fulfilling the fourth and fifth thesis objectives.

A custom Adder / Subtractor circuit based on a dual supply op-amp design has been realized on the dosimeter chip in the DALSA 0.8 um CMOS process. It included a negative bias generator which eliminates the need for a second negative voltage supply and which could enable on-chip dosimeter programming in future implementations. Also, the complete wireless dosimeter employed a differential architecture to reject common mode noise and to ensure matching of critical circuit elements. The circuit produced the required control voltage to modulate the transmitted wireless signal over the 5.2 – 5.4 GHz U-NII band. Sensitivity of up to 400 KHz/rad has been achieved. The active power of the dosimeter was measured to be 2 mW. The complete wireless dosimeter system (dosimeter and wireless transmitter) consumed 5.3 mW.

Several options for the provision of a transparent power source for the dosimeter were explored including thin-film ultra capacitors, and Li polymer battery. While the thin-film solution appeared promising in terms of size and on-chip integration, the Li polymer battery

was determined to be the most suitable option that is readily available. With this choice of power source the complete wireless dosimeter could be smaller than a dime as shown in Figure 4.18.

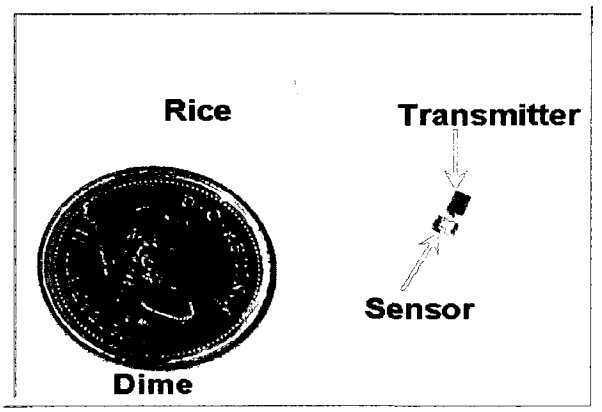


Figure 4.18 Demonstration of wireless dosimeter

This dosimeter-transmitter system was the first ever demonstration of a wireless dosimeter, and represents the second contribution of the thesis, namely "Novel wireless dosimeter" for radiotherapy.

The work in this chapter has resulted in one published [7] one submitted journal paper [13] three conference papers [8, 9, 11], and a provisional patent [15]. In addition, the novel wireless dosimeter design won the national technology innovation competition during the Canadian Microelectronics Corporation (CMC) Texpo [16].

Chapter 5

SoC Receiver

The previous chapter demonstrated a wireless dosimeter system for transmission mode only. In multisensory systems, with the need to identify and control individual sensors, a bidirectional wireless communication capability is required. The receive mode function could be integrated directly with the transmitting dosimeter to form a transceiver, or realized as a separate chip (for remote reception of dose) as shown in the proposed wireless dosimeter system of Figure 1.2. In either case, a miniaturized, low power receiver is desired. In accordance with the sixth, seventh, and eighth thesis objectives, this chapter presents a fully integrated U-NII (5.2GHz) band SoC receiver. First the LNA-antenna co-design and measured results are described. Then the DLL-based demodulator design and measured results are given.

5.1 Receiver Architecture

The receiver design, shown in Figure 5.1, is based on a fast locking fully differential DLL architecture which is capable of operating in a noisy environment. The front end of the receiver is a low power, high gain LNA that is conjugately matched to an on-chip antenna, and designed to reject noise and improve received signal strength. The LNA output is connected to the DLL input, feeding Voltage Controlled Delay Line (VCDL) and Phase and frequency detector (PFD). The design details of the individual receiver components are presented in the following sections.

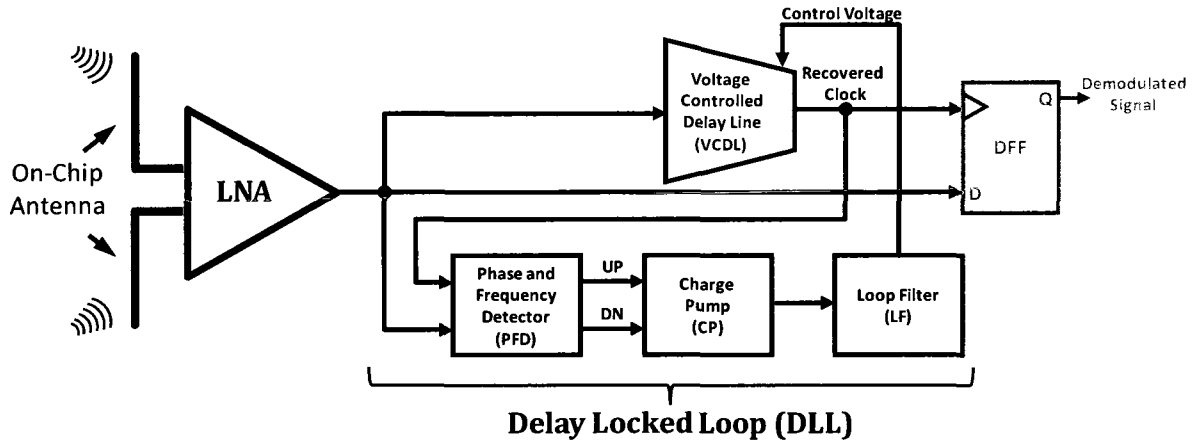


Figure 5.1 Receiver block diagram

5.2 LNA with On-chip Antenna

The monolithic receiver chip employs an on-chip antenna in standard 0.13µm CMOS process. The on-chip antenna has been conjugately matched to the differential LNA over a wide frequency range through the co-design of circuits and antenna. In order to minimize the chip area (maximum allocated space of 1.3 mm^2), the circuits are placed inside the antenna as shown in Figure 5.2.

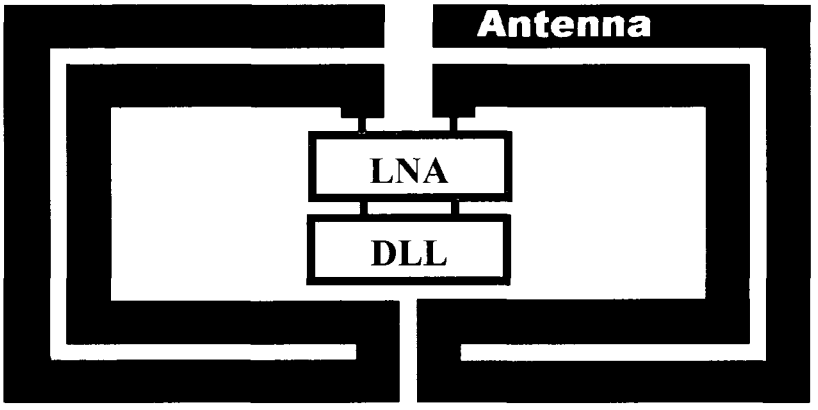


Figure 5.2 DLL based receiver with on-chip antenna

Most of the previously reported monolithic receiver implementations (as mentioned in Table 2.6) do not demonstrate on-chip antenna-LNA co-design for simultaneous low noise and input power conjugate matching, and hence rely on traditional 50Ω matching schemes. Moreover, many designs either employ non-standard high resistivity substrates or additional post

processing steps, and the antennas and chip sizes are significantly larger. This work addresses the above shortcomings through a novel miniaturized high performance design which is fully characterized.

The LNA and antenna are designed interactively to conjugately match their impedances without the need for matching components. Initially the LNA is designed for simultaneous noise figure (NF) and input power matching. This results in complex LNA impedance with a large real part. The on-chip antenna is then designed to conjugately match this complex impedance; however the real part of its impedance does not readily match that of the LNA. This is because the resistance of on-chip antennas realized in low resistivity Si is typically quite small [80]. Therefore, the LNA impedance is tuned to reduce the real part, resulting in a slightly higher NF and lower gain while easing the conjugate matching.

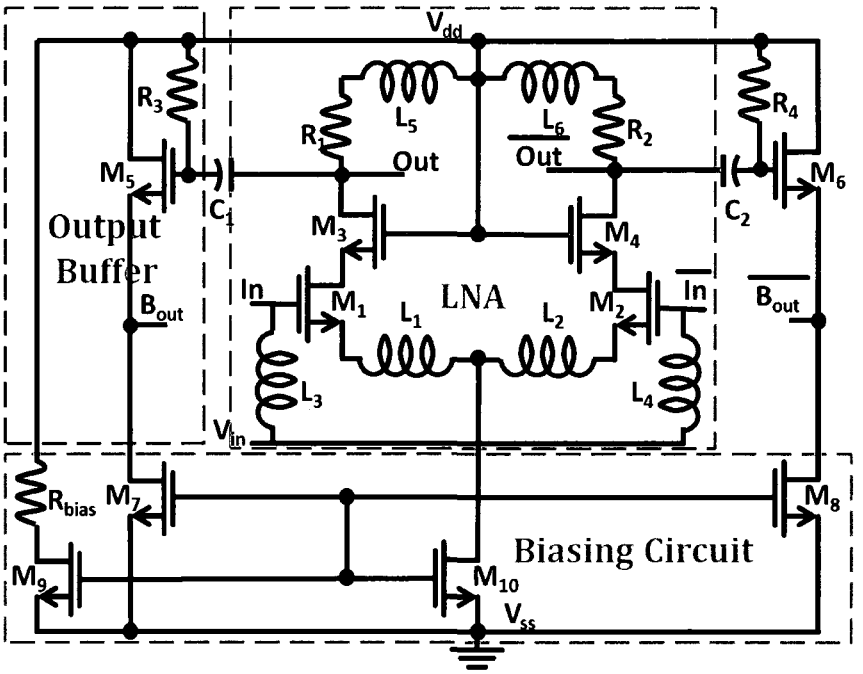
5.2.1 LNA Design

The LNA plays an important role in the receiver's noise performance. It has to provide enough gain to overcome the noise of the subsequent stages and add noise as low as possible to the signal. Based on the latest designs in the literature the target specifications have been prescribed for the proposed LNA design for the receiver front end, as shown in Table 5.1.

Table 5.1 LNA Target Specifications

LNA Target Specifications	
Bandwidth	2.4-5.8 GHz
Supply Voltage	1.2 V
Current Consumption	<10 mA
Gain	>15 dB
IIP3	>5 dBm
NF	<3 dB
Stability	Unconditional
Input Return Loss	>10 dB

The chosen topology for this work is based on the single ended wide band LNA presented in [81] which employs an inductively degenerated common-source amplifier. Better performance, in terms of LNA gain and common mode noise rejection, can be achieved by its differential implementation. The schematic for the differential LNA is shown in Figure 5.3. It consists of the differential cascode LNA block, buffers for independent testing and the biasing current mirror. The device sizes are chosen by considering the tradeoffs between power, noise and available gain. After achieving the minimum noise figure for the required current density, the LNA device sizes are adjusted to maximize gain. In post layout simulations a NF of 2.9 dB, LNA gain of 21 dB and IIP3 of -5dBm is achieved at 5.2 GHz. It should be noted that an additional bias point has been incorporated (shown as V_{in} in Figure 5.3) to provide flexibility for tuning the LNA performance.



L_1, L_2	=385nH;
L_3, L_4	=1.391nH;
L_5, L_6	=2.983nH;
R_1, R_2	=20.39Ω;
R_3, R_4	=4.0kΩ;
R_{bias}	=60Ω;
C_1, C_2	=1.0pF;
M_1, M_2	=300μm/0.13μm;
$M_3, M_4,$	
M_5, M_6	=150μm/0.130μm;
M_7, M_8	=150μm/0.26μm;
M_9, M_{10}	=300μm/0.26μm

Figure 5.3 LNA with output buffer (for measurements) and biasing circuit

Performance of the LNA in this work is compared against other recent designs operating at similar frequencies. Comparison results are tabulated and presented in Table 5.2 below. It is evident from the comparison that this LNA has the highest gain with comparable noise and power performance.

Table 5.2 Comparision of On-chip LNAs

Parameter	This Work	[81]	[82]	[83]	[84]	[85]	[86]	[87]	[88]	[89]	[90]
Freq (GHz)	2-6	2-9	2-5	5.25	5.25	5.7	5.25	2-5	3-4	5.9	5
Technology (μm)	.13	.18	.13	.18	.24	.18	.25	.18	.18	.13	.13
Voltage (V)	1.2	-	-	2.5	-	1.8	3	-	-	-	-
Current (mA)	7	-	-	-	-	8	8	-	-	-	-
Gain (dB)	21.7	9.3	9.5	18	18	12.5	14.4	9.8	16	16	15
IIP3 (dBm)	-5	-6.7	-0.8	-5	-2	-0.5	-1.5	-7	-4.5	-	-
NF (dB)	2.9	4.0	3.5	1.5	4.8	3.7	2.5	2.3	3.9	4.7	4.5
Power (mW)	8	9	16.5	-	7.2	-	24	12.6	7.2	38	-
Diff/ Single	D	S	D	S	D	D	D	S	S	D	-
S11	-	-9.9	-10	-	-12	-15	-11	-9	-10	-9	-5

5.2.2 On-chip Antenna Design

This part of the work is a collaborative effort. The on-chip antenna design has been performed by fellow researcher Atif Shamim, but is reported here for completeness.

HFSS simulations are used in designing the on-chip antenna. HFSS is a commercial finite element method solver for electromagnetic structures from Ansoft Corporation. The HFSS model for the on-chip antenna designed in CMOS 0.13 μm is shown in Figure 5.4(a). The antenna is realized in the 4 μm top Al metal layer as shown in Figure 5.4(b). For optimum performance, the antenna must be conjugately matched to the LNA. This eases the stringent requirements of matching both the antenna and LNA to 50Ω and also eliminates the need for matching elements. In this work, a 5.2 GHz on-chip antenna has been designed in conjunction

with the LNA to simultaneously obtain minimum NF and maximum power transfer. A dipole antenna is chosen in order to drive the differential LNA without a balun. The dipole arms are folded to fit into a chip space of 1.3 mm x 1 mm. Since the LNA is placed inside the dipole antenna in the final layout, it is fed through two internal lumped ports in HFSS to replicate the LNA connection with the antenna.

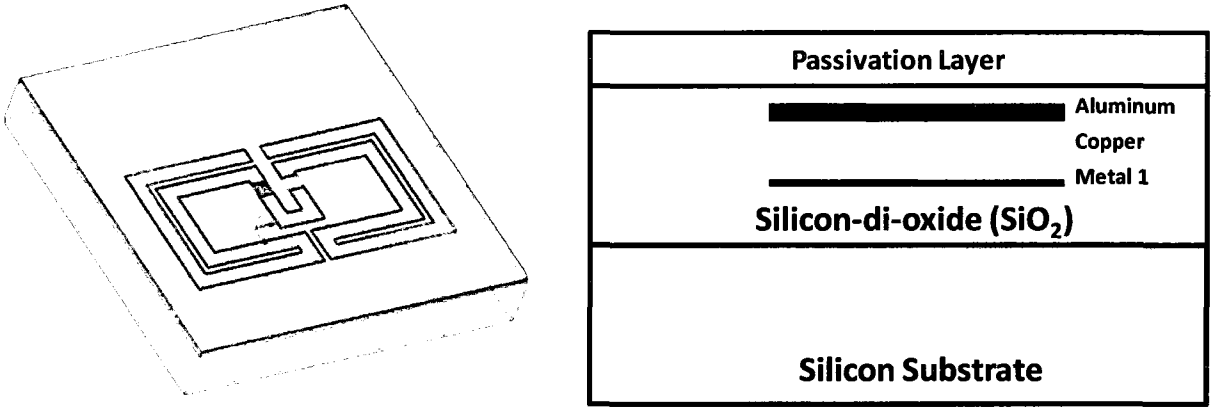


Figure 5.4 (a) RX antenna HFSS model (b) CMOS 0.13 μm metal stack up

The LNA's optimized differential impedance at 5.2 GHz is 91 + j124 Ω, and the on-chip antenna is designed to conjugately match to this impedance. This is accomplished by lengthening the dipole antenna. However, this mostly increases the loss resistance instead of the radiation resistance of the antenna. The trade-off in matching to a large LNA real impedance is a reduced antenna gain. It is observed that increasing the metal width increases the antenna gain, however due to fabrication specifications, it is limited 100 μm. Care has been taken that, in the available chip space, the gap between the conductors is sufficient so that oppositely directed current does not cancel the radiated fields. Nonetheless, due to the lossy nature of the Si substrate, this effect is minimal. In simulations, a sensitivity analysis is done to choose suitable locations of the LNA elements with respect to the antenna so as to achieve minimum spacing between the various elements. The final dimensions of the antenna 1.3 mm x 0.7 mm result in a differential impedance of 90 - j133 Ω at 5.2 GHz, which yields an excellent match between the on-chip antenna and the LNA impedances, as shown in Figure 5.5. It is worth mentioning here that the co-design of antenna and LNA has helped to achieve a wide impedance bandwidth. Simulations reveal a bore-sight maximum radiation pattern with a gain of -35 dBi as shown in

Figure 5.6. It is also observed in simulations that placing the antenna closer to the chip edges slightly increases the gain.

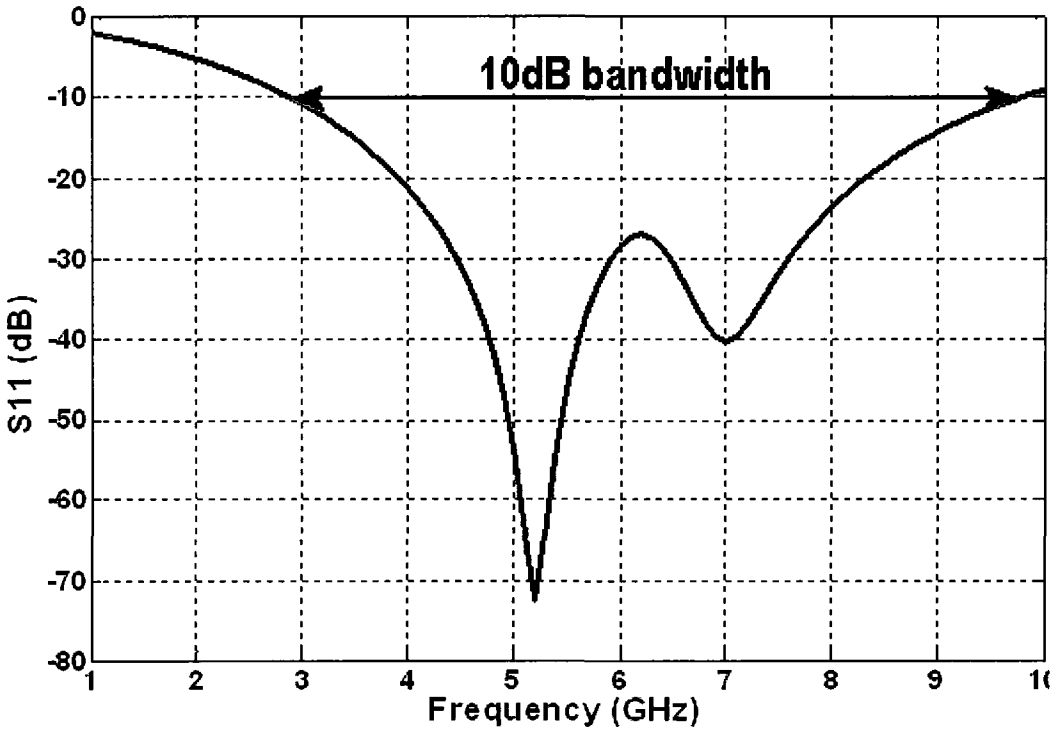


Figure 5.5. Simulated S11 of on-chip antenna (reference to complex impedance of LNA)

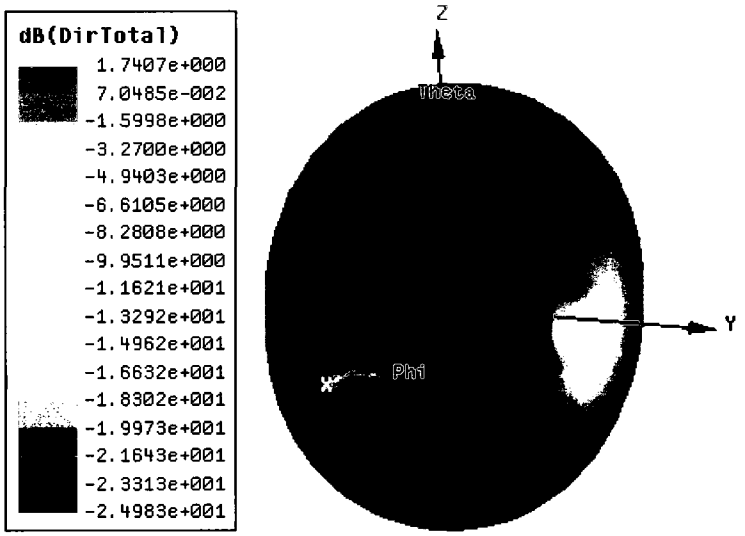


Figure 5.6 Simulated radiation pattern and the gain of the antenna

5.2.3 Fabrication and Measurements

Since the circuits are placed inside the antenna, there are several challenges associated with the layout of the chip. Placement of several inductors inside a small area without affecting the performance of the circuits or the antenna, and facilitating independent testing of different sub-modules, are the most difficult aspects. Also, routing the bias, signal and ground traces to the pads through a complex circuit without breaking any design rules, is difficult. Nonetheless, insight gained from EM and post layout circuit simulations and inclusion of microsurgery points eases some of these challenges. Another consideration is to make the layout as symmetric as possible to ensure true differential operation. As shown in the microphotograph of the realized chip (Figure 5.7), the antenna remains close to the chip edges with minimal interference from nearby metals. Arrangements have been made through microsurgery points (Figure 5.8) so that the LNA and antenna can be tested separately through the same set of standard eight RF pads.

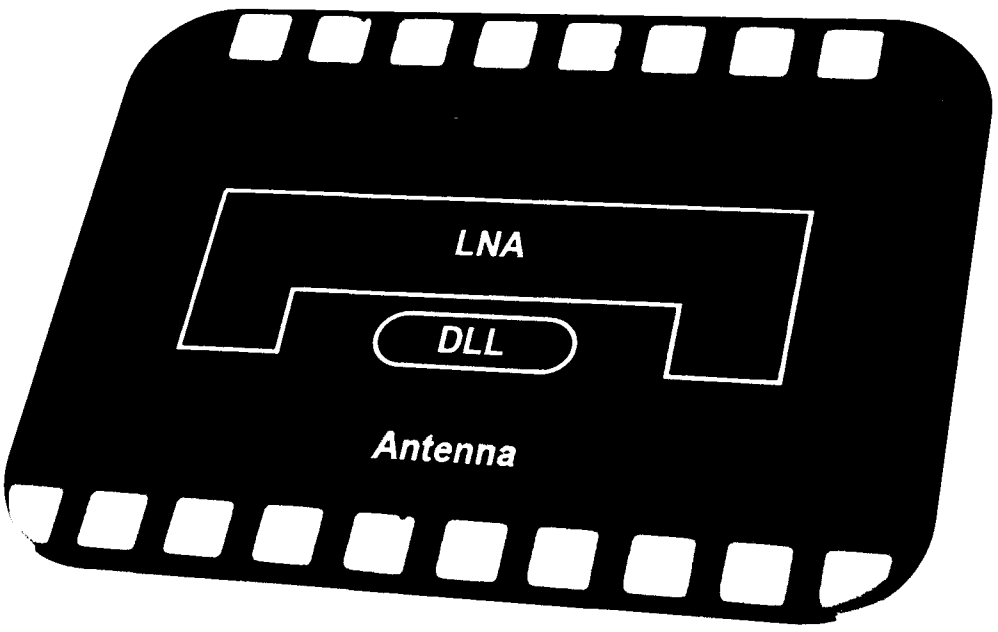


Figure 5.7 Microphotograph of presented fully integrated DLL based receiver

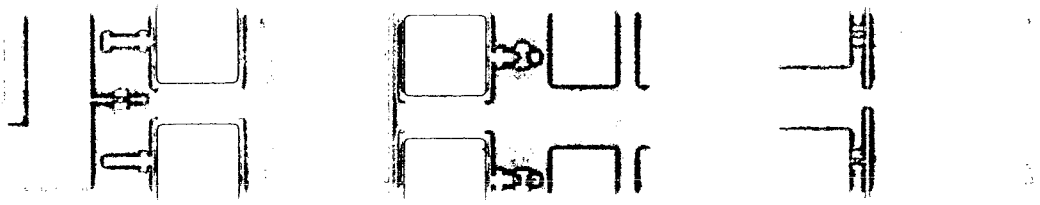


Figure 5.8 Microsurgery of RX chip for individual component testing performed at Muanalysis.

Measurements

The LNA receives the dc bias and a known input RF power through an eight pin probe. The output power from the LNA is measured through the same probe. The difference in the levels of the input and output power is equal to the gain of the LNA. A maximum gain of 21 dB has been measured for the 5 GHz range, which is very close to the simulated results as shown in Figure 5.9. The LNA's DC power consumption is 8mW.

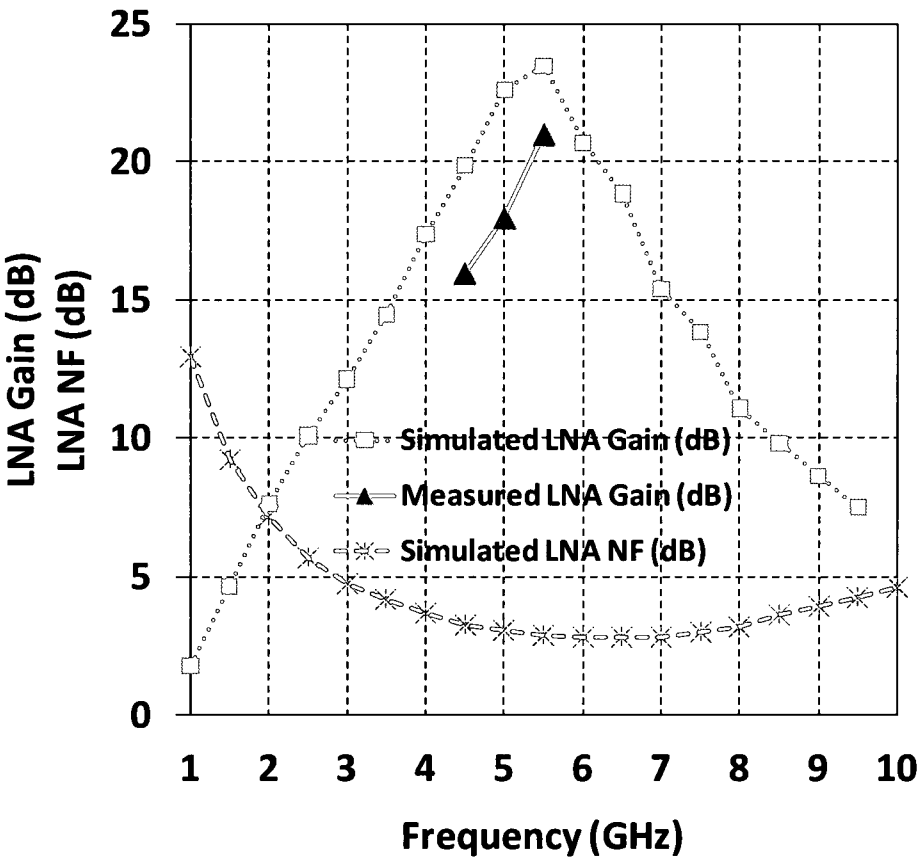


Figure 5.9 Gain and NF of the LNA

A challenging part of this work is to experimentally characterize the radiation properties of the on-chip dipole antenna. The most common method to measure the antenna radiation pattern/gain is to use transmit and receive towers in an anechoic chamber. There are multiple problems in executing the standard gain measurement procedure for on-chip dipoles that measure a few millimetres in size.

First, on-chip dipoles are fed using wafer probes, unlike other antennas with co-axial or SMA feed mechanisms. Probe tips are very sensitive and may get damaged during the antenna under test (AUT) movement. Second, Si wafers are fragile unlike other common antenna substrates. There is a higher probability that a Si wafer may be scratched or broken during measurement. Third, a microscope is essential to accurately contact the miniature on-chip antenna structures with the probes. In general, a microscope is not part of the standard equipment in an anechoic chamber. Furthermore, the presence of a microscope may affect the antenna radiation pattern or block the movement of the AUT. Fourth, a special test fixture must be designed and fabricated in order to mount the on-chip dipole in the anechoic chamber and measure its radiation pattern and gain.

In order to alleviate the above mentioned problems, a moveable microscope is used on a probe station. A custom stand is made to perform the measurements. The transmitter patch antenna with gain G_p is mounted on the stand which can rotate around the receiver chip as shown in Figure 5.10. It is fed through the signal generator with a known transmit power P_t. The power is received at bore-sight by another patch antenna placed on the probe station chuck and recorded through the spectrum analyzer as P_{rp}. The receive patch antenna is then replaced by the receiver chip while the rest of the setup remains the same. The power is now received by the on-chip antenna and after being amplified by the LNA is measured through the standard eight pin RF probe. This received power is denoted as $P_{rc.}$ The on-chip antenna gain G_c can now be calculated through (5.1), where LNA_G is the LNA gain. The measured antenna gain from (5.1) is -35 dBi, which is quite close to the simulated antenna gain. Next, the transmit antenna is rotated in steps of 15 degrees around the receiver chip and the power is recorded. The resultant normalized radiation pattern which has been created through spline interpolation of

discrete data points is shown in Figure 5.11. It can be seen that the measured radiation pattern is consistent with the simulated radiation pattern where the maximum occurs at bore-sight and the minimum is around the plane of the antenna. The dip in the radiation pattern can be attributed to manual measurements error.

$$G_c = P_{rc} - P_{rp} + G_p - LNA_G \tag{5.1}$$

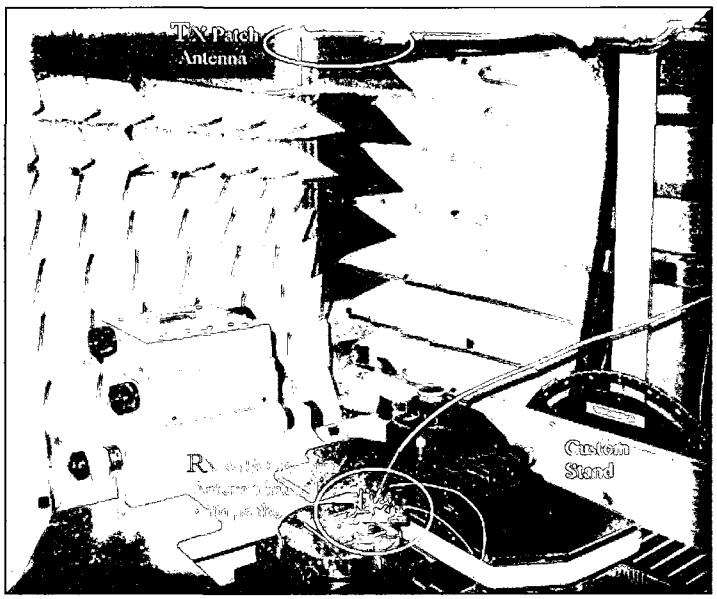


Figure 5.10 On-chip antenna measurement setup

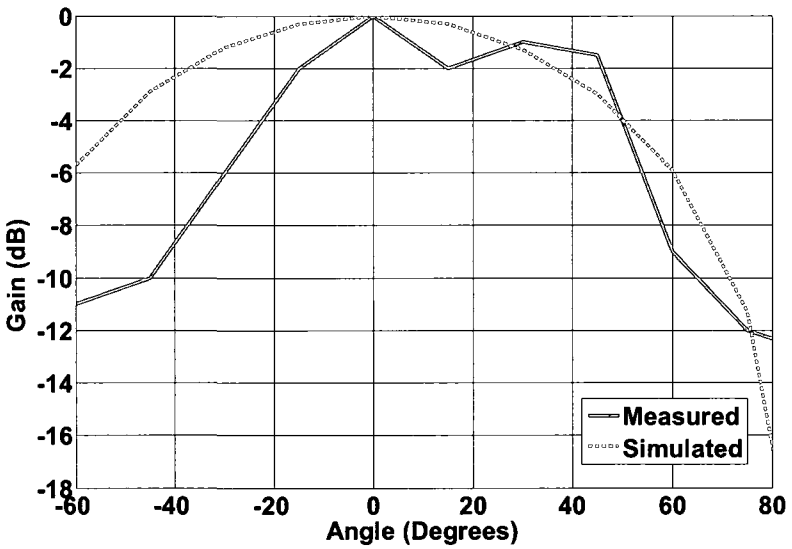


Figure 5.11 Measured radiation pattern of RX antenna

5.3 Delay Locked Loop (DLL)

A Delay Locked Loop based receiver has been designed due to the simplicity of the architecture, easier monolithic integration, along with inherent low noise and stable behaviour. A fully differential design is adopted to go hand in hand with the differential front end LNA and on-chip antenna in order to eliminate common mode noise.

5.3.1 DLL Topology

According to the results presented in [91], the analog DLL uses less power and area, and provides better timing performance and hence, smaller long-term jitter and phase resolution that enables smaller maximum phase step. Therefore an analog DLL topology is adopted for the demodulation of received signals.

5.3.2 DLL Design

The architacture of the designed fully differential DLL is illustrated in Figure 5.12. The main blocks of the DLL are,

a. Voltage Controlled Delay Line (VCDL)
b. Phase and Frequency Detector (PFD)
c. Charge Pump (CP), and
d. Loop Filter (LF)

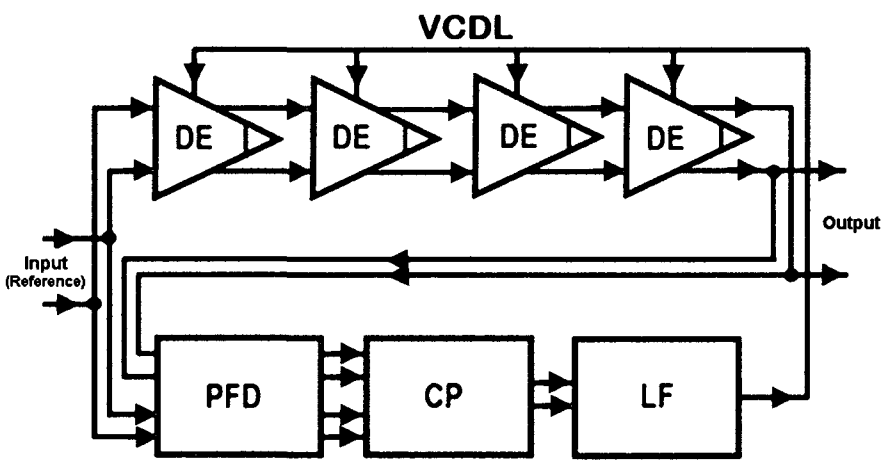


Figure 5.12 Block diagram of differential analog DLL

The design details of individual DLL blocks are described below.

Voltage Controlled Delay Line (VCDL)

Within the DLL, one of the most fundamental components is the delay element (DE). A VCDL is a series combination of these DEs. The designed differential DE along with its symbol is shown in Figure 5.13. The circuit elements of the DE were selected to provide sufficient flexibility in the delay so that DLL can lock in the desired frequency range. The targeted range for the DLL operation was 5-6 GHz. Extra bandwidth was considered to compensate for any change in the other design elements.

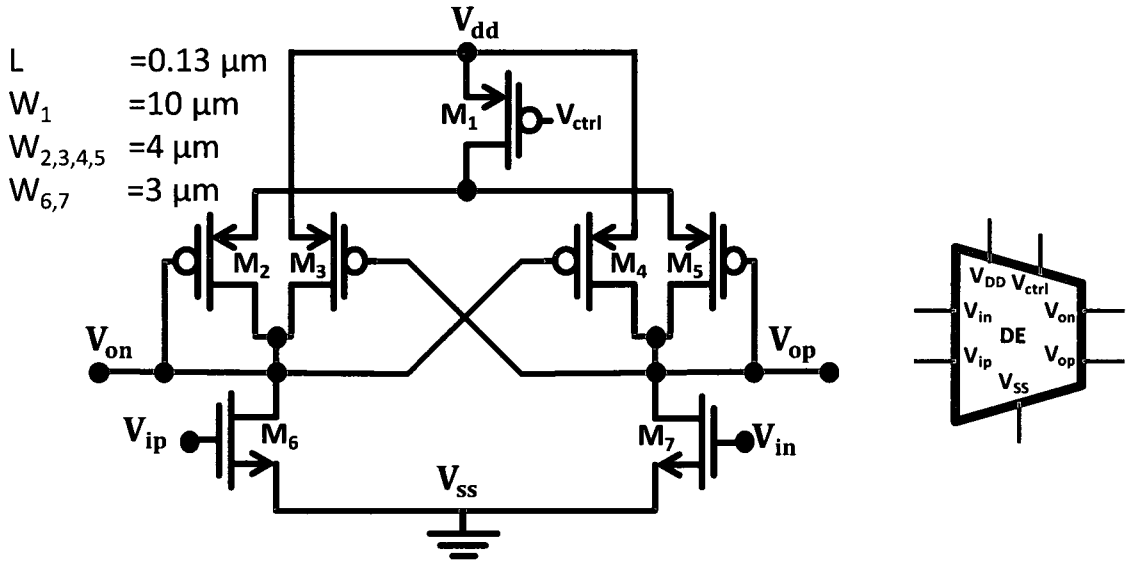


Figure 5.13 Delay Element (DE) for VCDL and its symbol

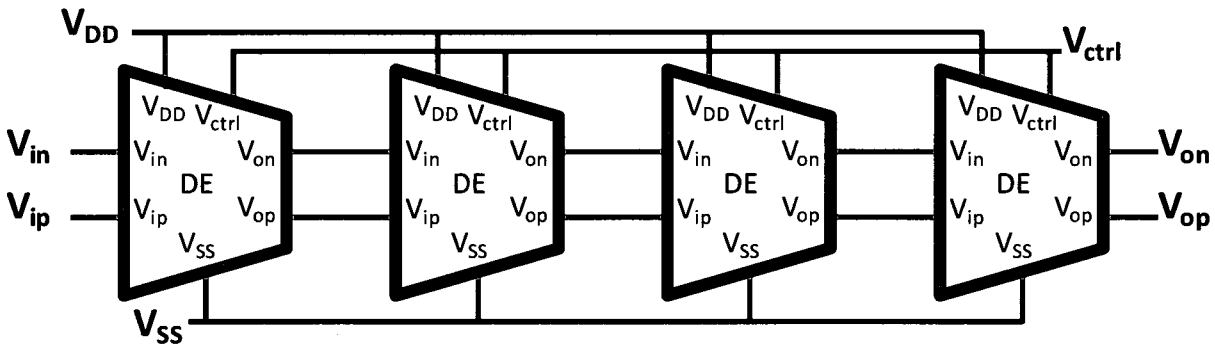


Figure 5.14 Schematic of voltage controlled delay line (VCDL)

The DLL design uses four of these DEs connected in series, as shown in Figure 5.14. Hence each of them is responsible for providing a quarter of the delay needed for the frequency of interest. In our case for circuit operation in the U-NII band, frequency shift between and within the channel could be roughly from 5 to 6 GHz. It reflects to a total delay of 200 ps (@5 GHz) to 166.67 ps (@6 GHz). In a 4-stage VCDL each DE is responsible to provide quarter of the total delay. i.e. from 50 ps to 41.66 ps. Hence the DEs are designed to have a minimum delay of 41.66 ps that can be increased via V_{ctrl} to 50 ps to fulfill the design requirement. Figure 5.15 shows the post layout performance of the VCDL.

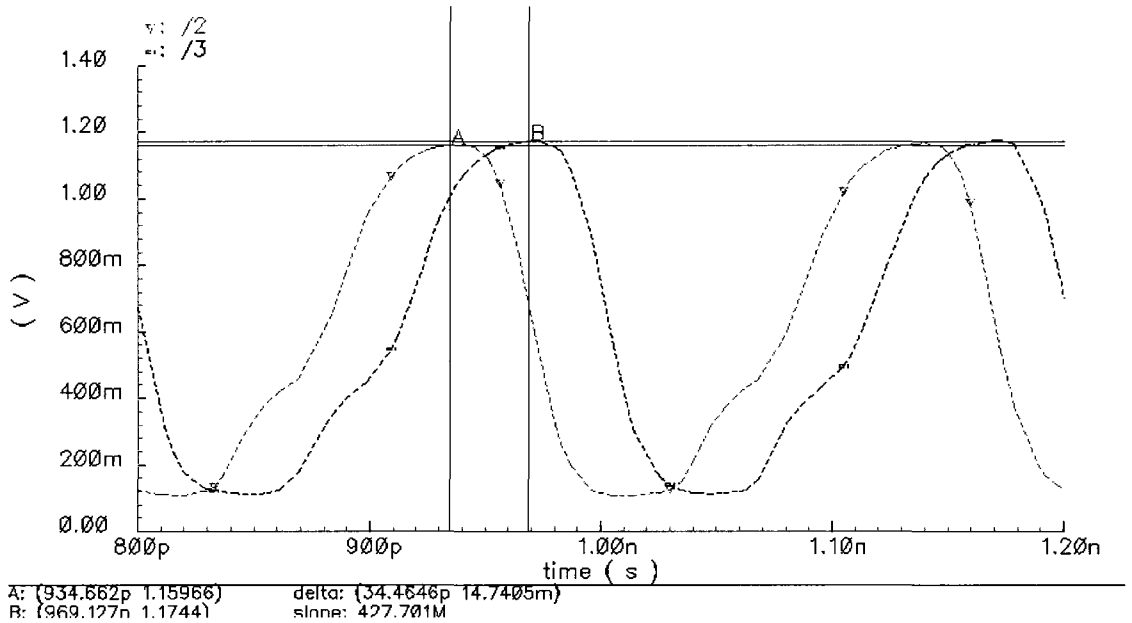


Figure 5.15 VCDL post layout simulation results

Phase Frequency Detector (PFD)

The role of PFD within DLL is to take two input clocks V_R and V_o and examines the difference of phase and frequency between them. The designed phase detector is completely differential and produces two differential outputs, Pulse-Up (U) and Pulse-Down (D). If V_R is leading V_o then the U signal will become larger than D and vice-versa. If V_R and V_o are in phase then the U and D signals will be the same. The designed PFD is an asynchronous sequential logic circuit where gates are fully differential MOS current mode logic (MCML) gates [63].

A 3-state CML based differential PFD has been designed for the proposed DLL. The circuit of the PFD is as shown in Figure 5.16 [63]. Figure 5.17and Figure 5.18 are showing the detailed design of sub-blocks of the PFD. The state machine of the PFD is illustrates in Figure 5.19 [63]. CML based architecture ensures fast response, low noise, and low power operation of the PFD at higher frequencies.

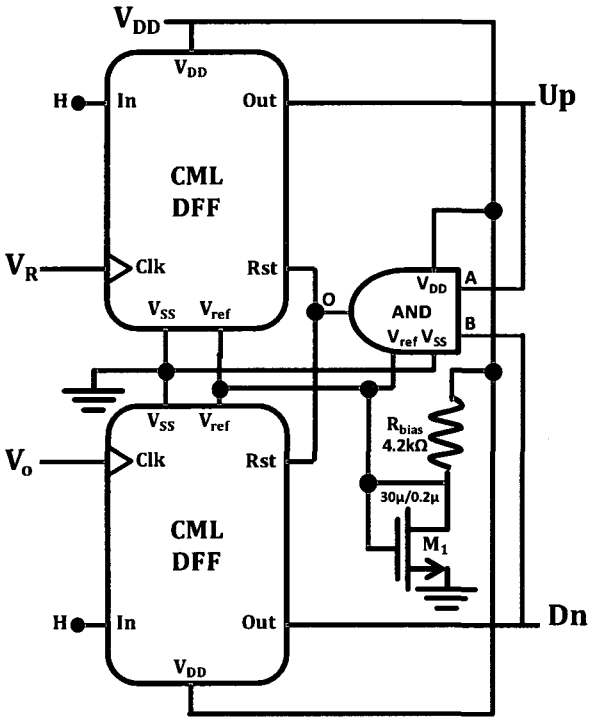


Figure 5.16 Tristate differential PFD block diagram

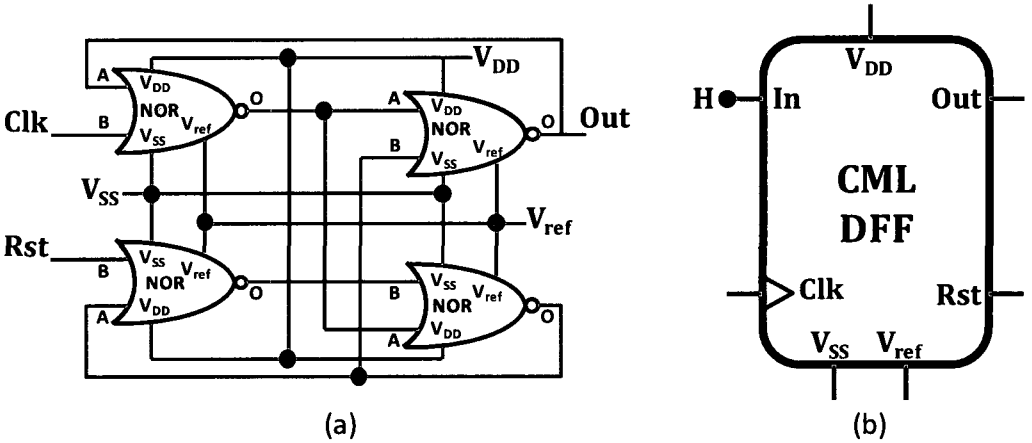


Figure 5.17 CML differential DFF (a) schematic and (b) symbol used in tristate PFD

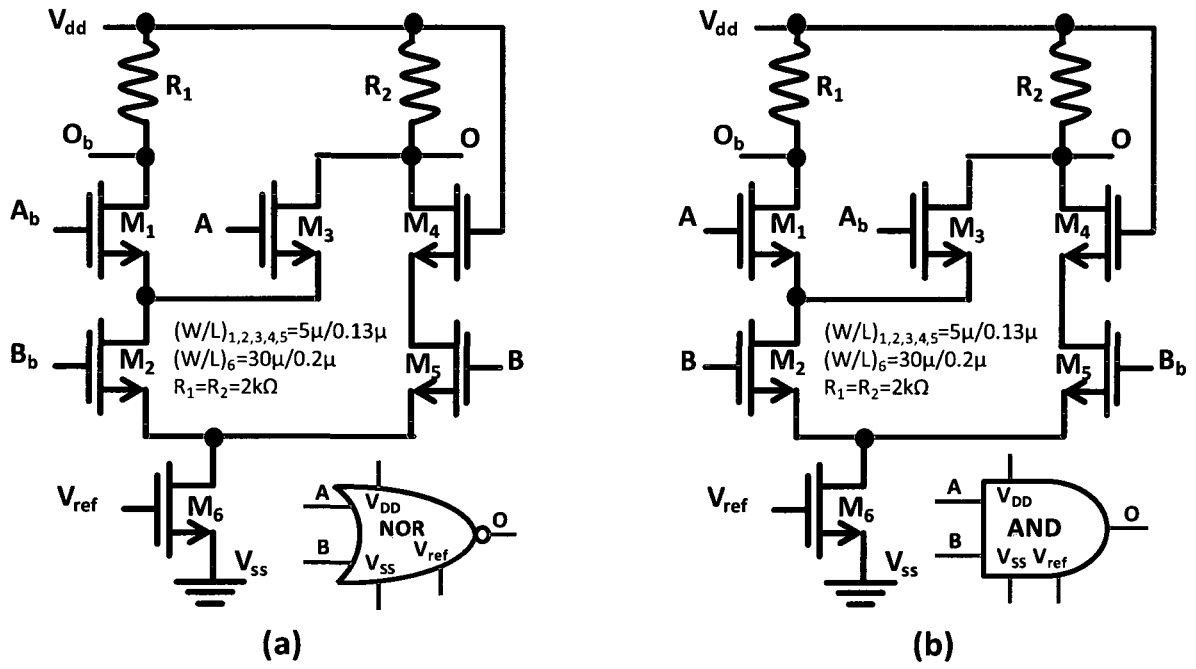


Figure 5.18 Two input CML differential (a) NOR and (b) AND logic gate schematics (with symbols) used to implement CML tristate PFD

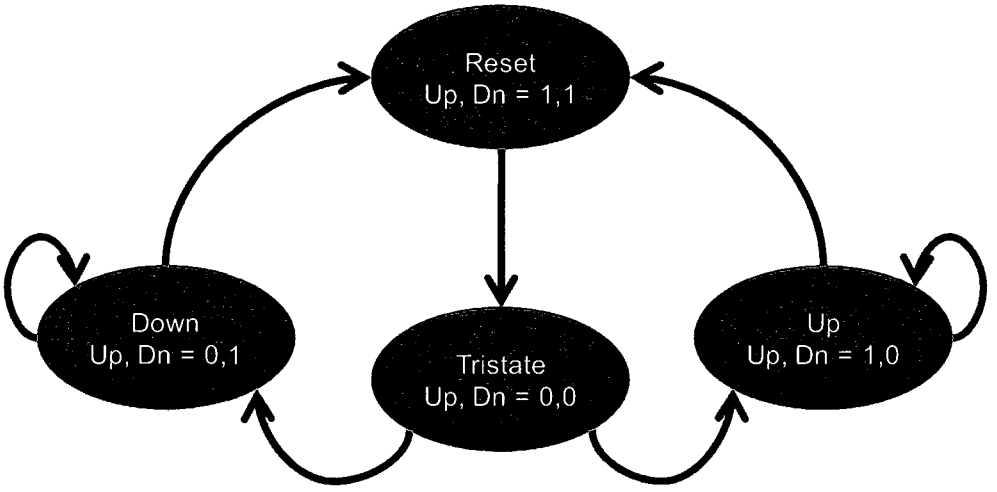


Figure 5.19 State diagram of the tristate PFD

Figure 5.20 shows the proper function of the PFD block, with up and down signals produced at the right timing to be able to drive the charge pump and lock to the input signal as quickly as possible.

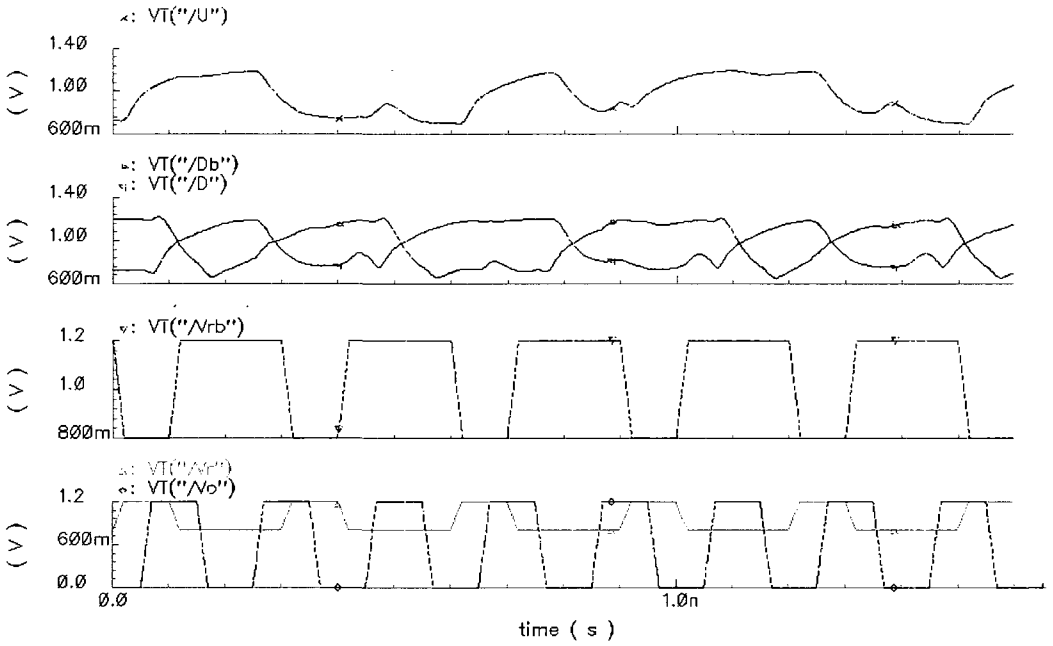


Figure 5.20 PFD post-layout simulation results

Charge Pump (CP)

A charge pump in DLL takes the U and D signals from PFD and then transfers charge onto or off the loop filter thus changing the control voltage. The designed charge pump is shown in Figure 5.21 [63]. This charge pump architecture is specifically designed to perform better with CML based PFD. This CP has good current matching due to symmetric U and D input stages.

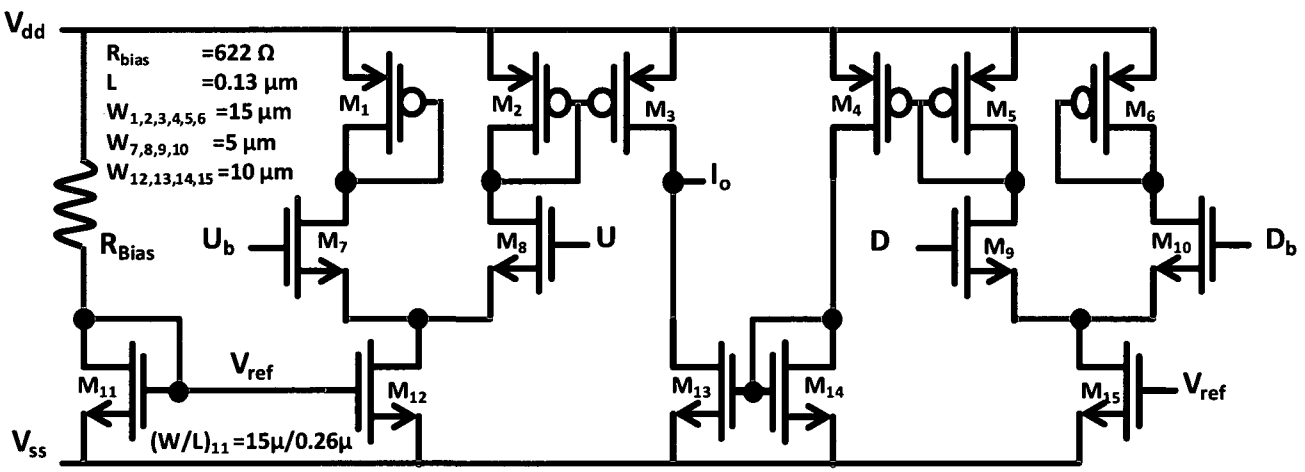


Figure 5.21 Schematic of the charge pump (CP)

Loop Filter

The loop filter at the output of the charge pump is used to integrate the net current from the charge pump and transfer it to a control voltage. The design of the LF for a DLL appears much simpler than PLL but it is still very critical for loop performance, the bandwidth, and the locking time. LF in this design consists of a capacitor functioning as an integrator.

On the receiver chip, the size of the LF capacitor can be fine tuned by means of post processing microsurgery points to fine tune the loop bandwidth and locking time response of the DLL. The layout of the implemented DLL is illustrated in Figure 5.22.

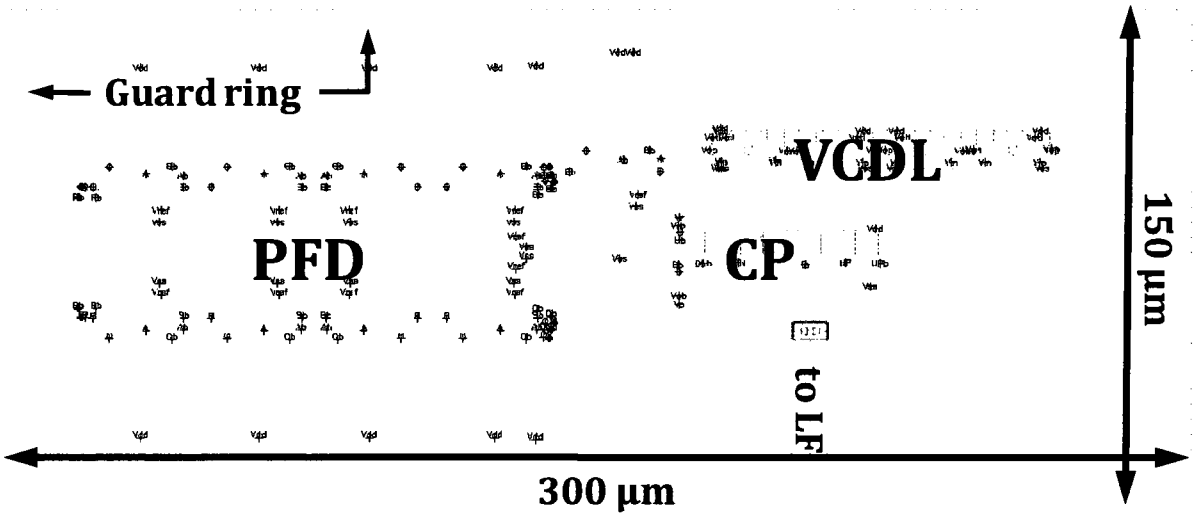


Figure 5.22 DLL layout excluding LF (300 µm x 150 µm)

5.3.3 DLL Measurements

The functionality of DLL has been fully tested and performance parameters are measured. The DLL was locking in the range of 4.7 to 5.7 GHz, as shown in Figure 5.23. The locking range was covering the desired U-NII band. The whole RX chip consumed 14 mW of power. The measured locking time of the DLL was 7.2 ns.

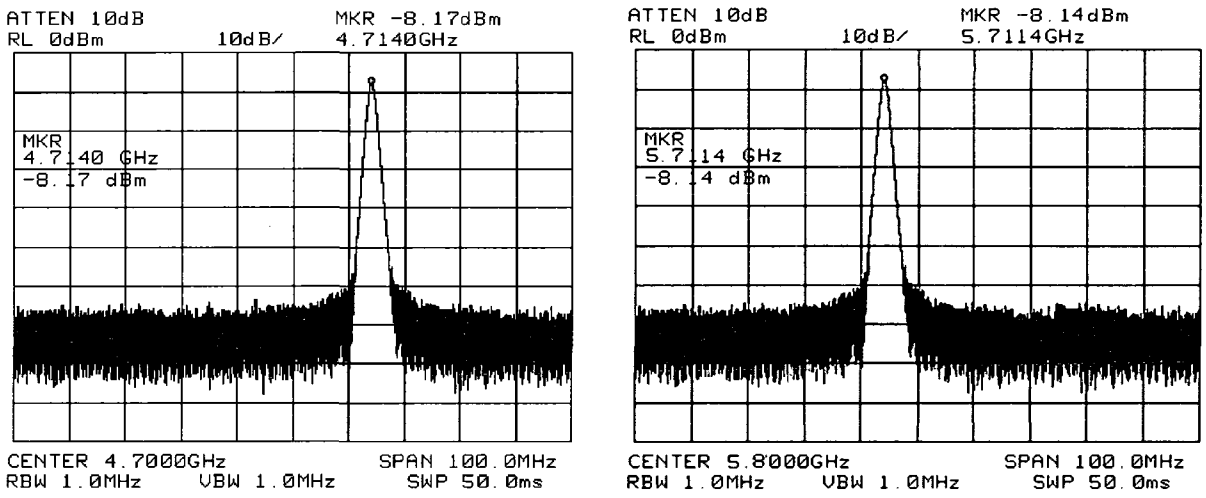


Figure 5.23 DLL locking range (4.7 – 5.7 GHz)

A performance comparison of this work with some recent DLL designs is presented in Table 5.3. The performance of this design is very promising. It is the smallest in size and at the lower end of the power consumption range. The DLL in [73] does not use a fully differential structure; hence it has an obvious low power advantage.

Table 5.3 Performance Comparision of DLL

	This Work	[70]	[71]	[72]	[73]
Process (µm)	0.13	0.13	0.09	0.18	0.18
Supply (V)	1.2	1.2	1	1.8	1.8
Frequency (GHz)	4.7-5.7	0.5-5	2-5	0.9-2.9	0.25-2
RMS Jitter (ps)	1.2 @ 5 GHz	1.06 @ 5 GHz	0.87 @ 5 GHz	1.62 @ 2.16 GHz	2.81 @ 2 GHz
Jitter-pp (ps)	7.5 @ 5 GHz	8 @ 5 GHz	7.56 @ 5 GHz	12.9 @ 2.16 GHz	20 @ 2 GHz
Power (mW)	14	36	45	19.8	6.4
Area (mm^2)	0.045	0.107	0.121	0.27	0.046

5.4 Multisensory System

The purpose of designing a DLL based receiver is to provide a logical extension to the basic wireless sensor system, making it more practical with multiple sensor modules. These must be individually identified and communicated with to send and receive both commands and data. The design of the frontend RX components in this work is flexible enough to be a part of any modern communication standard for secure and efficient communication between individual wireless sensor modules or nodes. Figure 5.24 is illustrates the concept.

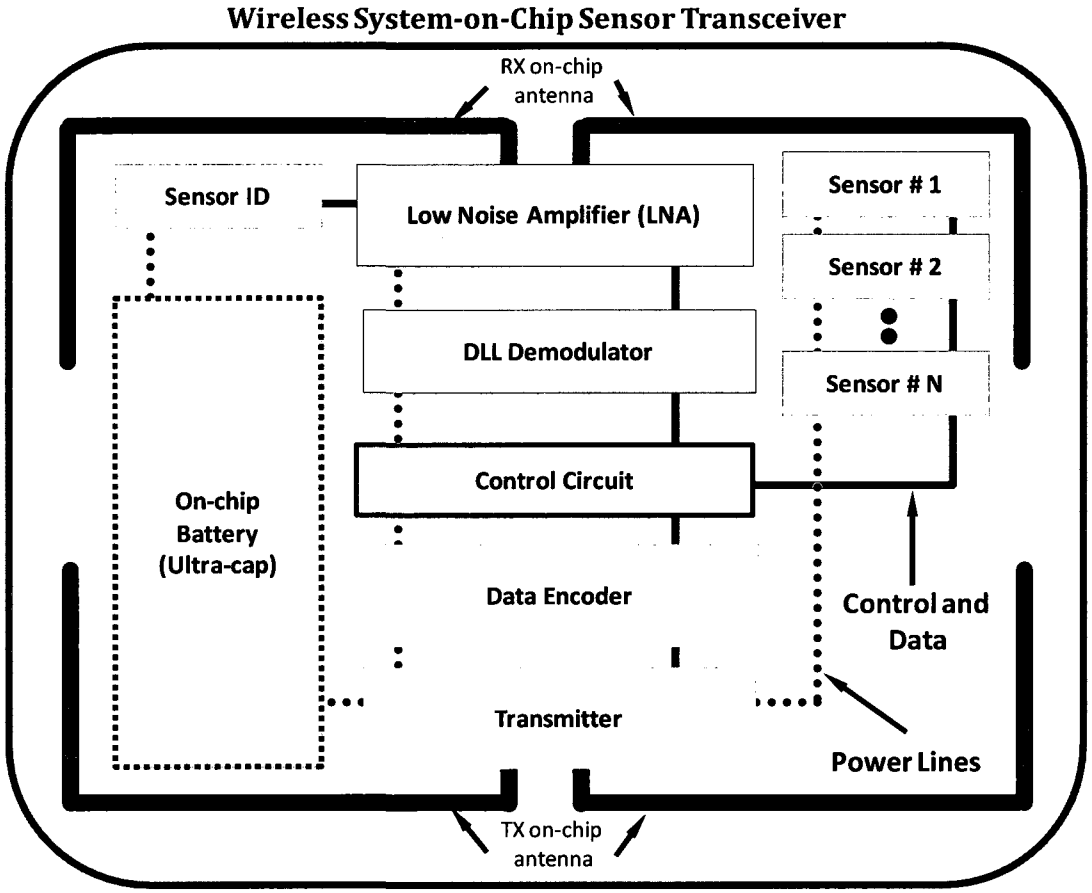


Figure 5.24 Proposed short range wireless sensor transceiver

It is a full duplex system with two on-chip antennas and separate TX and RX blocks. To show the feasibility of two on-chip antennas along with the sensors and other functional blocks, the TX and RX SoCs developed in this work were fabricated as a single transceiver unit, as depicted in Figure 5.25. This system is a single sensor demonstration only, that uses the change in the

transmitted frequency to reflect the change in a sensed parameter, which in this case is the radiation dose. With appropriate changes on the TX side and at the system level to implement an efficient data modulation scheme such as binary phase shift keying (BPSK), a full wireless multisensory transceiver system can be realized. Applications of such a system are widespread such as body area networks [7].

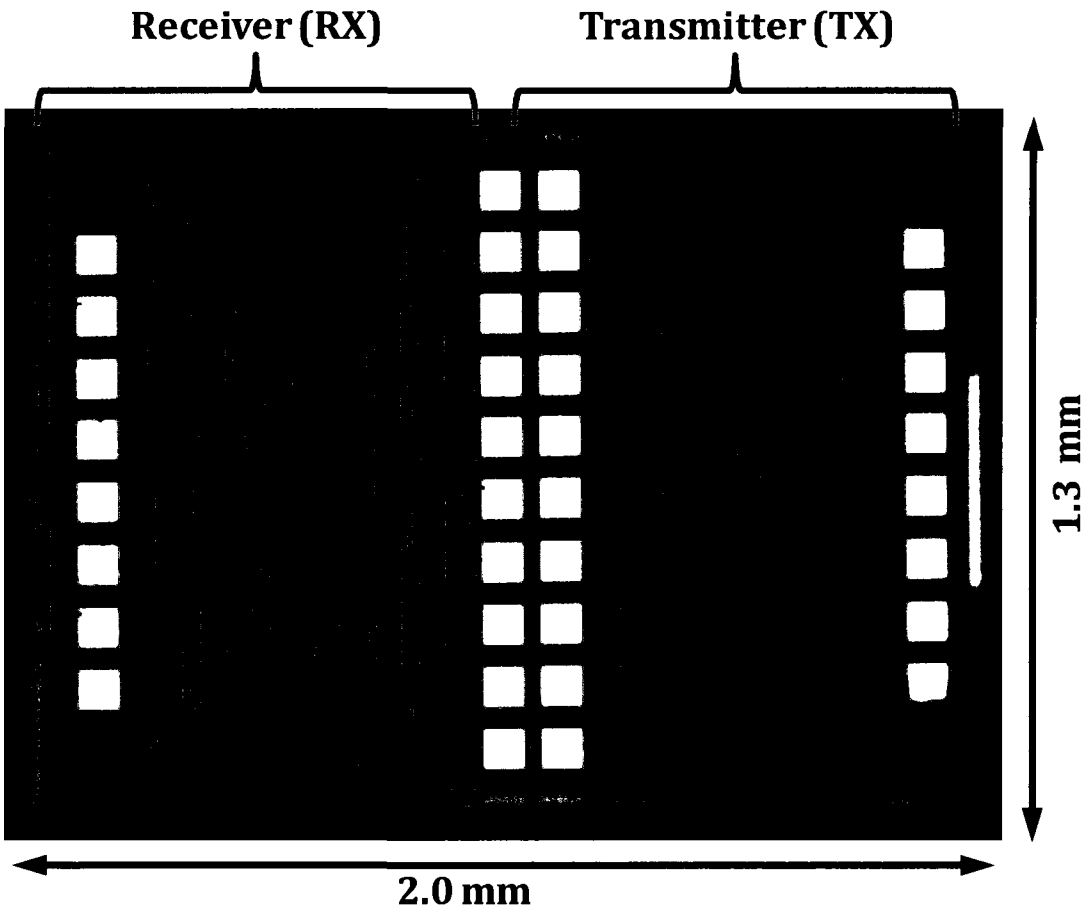


Figure 5.25 Short range wireless sensor transceiver

5.5 Summary and Contributions

In this chapter a fully integrated U-NII band SoC receiver was presented. It consisted of an LNA with an on-chip antenna and a DLL-based demodulator. The chip was realized in a standard IBM CMOS 0.13 μm process.

The co-design of the LNA-antenna combination was described in detail. The LNA was designed to conjugately match the impedance of the antenna, allowing the elimination of matching elements. This saved power and chip area, making the design the smallest reported 5 GHz SoC receiver with an on-chip antenna (1.3 mm^2). The measured LNA gain was 21 dB and the LNA-antenna co-design resulted in a very wideband impedance match, extending from 3 GHz to 10 GHz. The simulated noise figure was 2.9 dB.

The fully differential DLL demodulator was designed and its performance measured. The locking range was 4.7 – 5.7 GHz and a fast-locking time of 7.2 ns was observed. The design is inherently stable and is suitable for multisensory environments having modern digital modulation schemes such as BPSK, QPSK, etc.

This SoC receiver represents the third contribution of the thesis, namely "Miniaturized System on Chip (SoC) receiver with on-chip antenna".

The work in this chapter has resulted in one accepted journal paper [12] and a provisional patent [15].

Chapter 6

Conclusion and Future Work

This chapter summarizes the research work and the contributions of this thesis and proposes future work which will help researchers to advance the art of FG dosimeters and SoC wireless transceivers.

6.1 Conclusions

A novel low power dosimeter architecture was presented in Chapter 3, fulfilling the first four thesis objectives. In addition, the design of enhanced sensitivity FG sensor was described. Three novel dosimeter designs for improved accuracy and radiation sensitivity were presented. Finally a performance comparison of the new dosimeters with previously reported designs is performed.

A new architecture has been adopted that enables low power operation. The resulting dosimeter can operate at voltages as low as 0.1 V. While this new architecture was initially intended to improve the accuracy, such improvement was not obtained.

A new FG sensor structure has been developed. A mathematical analysis quantifying its sensitivity has been presented for the first time.

The FG sensor's unique programming characteristics and procedures have been discussed in detail. Further, extensive thermal and stability analysis (experimental based) have been performed. A successful stabilization procedure for the sensor has been proposed. Finally, a

detailed assessment of the sensor's accuracy has been carried out. It was found that the elevated metal shield (M3) increases sensitivity by 10% compared to the M2 shielded design.

The FG sensor was then employed in three novel low power dosimeter designs, all fabricated in the commercially available DALSA 0.8 μm CMOS process and experimentally validated. The first design, consisting of a dual FG structure, was fully characterized in terms of sensitivity and accuracy.

The second design employed an interdigitated FG sensor and reference and was found to exhibit improved accuracy compared to the previous design. However, its sensitivity was slightly lower.

The third design consisted of multiple sensors stacked in parallel and was seen to provide increased sensitivity proportional to the number of devices, without compromising accuracy. For the two-device sensor developed in this work, a sensitivity of 3 mV/rad (15.1 nA/rad) was achieved.

The results on the novel RADFET represent the first contribution of the thesis, namely "high sensitivity radiation sensor".

Monolithic integration of signal processing electronics with the new radiation sensors, and the implementation of a novel wireless dosimeter system, fulfilling the fourth and fifth thesis objectives, was presented in Chapter 4.

A custom Add / Subtract circuit based on a dual supply op-amp design has been realized on the dosimeter chip in the DALSA 0.8 μm CMOS process. It included a negative bias generator which eliminates the need for a second negative voltage supply and which could enable on-chip dosimeter programming in future implementations. Also, the complete wireless dosimeter employed a differential architecture to reject common mode noise and to ensure matching of critical circuit elements. The circuit produces the required control voltage to modulate the transmitted wireless signal over the 5.2 – 5.4 GHz U-NII band. Sensitivity of up to 400 KHz/rad has been achieved. The active power of the dosimeter was measured to be 2 mW. The complete wireless dosimeter system (dosimeter and wireless transmitter) consumed 5.3 mW.

Several options for the provision of a transparent power source for the dosimeter were explored, including thin-film ultra capacitors, and Li polymer battery. While the thin-film ultracapacitor solution appeared promising in terms of size and on-chip integration, the Li polymer battery was determined to be the most suitable option that is readily available. With this choice of power source the complete wireless dosimeter could be smaller than a dime.

This dosimeter-transmitter developed in this work was system is the first ever demonstration of a wireless dosimeter, and represents the second contribution of the thesis, namely "Novel wireless dosimeter" for radiotherapy.

In chapter 5 a fully integrated U-NII band SoC receiver was presented. It consisted of an LNA with an on-chip antenna and DLL-based demodulator. The chip was realized in a standard IBM CMOS 0.13 μm process.

The co-design of the LNA-antenna combination was described in detail. The LNA was designed to conjugately match the impedance of the antenna, allowing the elimination of matching elements. This saved power and chip area, making the design the smallest reported 5 GHz SoC receiver with an on-chip antenna (1.3 mm^2). The measured LNA gain was 21 dB and the LNA-antenna co-design resulted in a very wideband impedance match, extending from 3 GHz to 10 GHz. The simulated noise figure was 2.9 dB.

The fully differential DLL demodulator was designed and its performance measured. The locking range was 4.7 – 5.7 GHz and a fast-locking time of 7.2 ns was observed. The design is inherently stable and is suitable for multisensory environment having modern digital modulation schemes such as BPSK, QPSK, etc.

This SoC receiver represents the third contribution of the thesis, namely "Miniaturized System on Chip (SoC) receiver with on-chip antenna".

The work of this thesis has resulted in one published journal paper [7], one accepted journal paper [12], and one submitted journal paper [13]. Also, four publications in the conferences [8-11] and one provisional patent [15] have resulted from this research.

6.2 Proposed Future Work

To carry on the work presented in this thesis, specific recommendations for an automatic programming system and a multi-sensor extension of the presented wireless sensor work were made in chapter 3 and chapter 5 respectively. Additionally the following research direction are proposed.

1. To optimize the sensitivity of the RADFETs extensive analysis of their physical behaviour is needed. A better understanding of some of the unpredictable effects (thermal annealing/charging, stabilization etc.) will be beneficial for many other fields of research, including analog circuits, flash memories, and semiconductor sensors. This will also allow the maximum sensitivity to be obtained from the floating gate RADFET.
2. On-chip programming of FGRADFETs with standard single power source, using charge pump based bias generators and on-chip temperature sensor to actively compensate the behavioural change of the FGRADFETs may result in a more reliable, enhanced sensitivity dosimeter.
3. The work can be extended to achieve the sensitivity needed for legal dosimeters. Very large extensions of FG structures, grounded during the fabrication will probably prevent the FGRADFET from any processing damage, and can later be post processed to leave the large gate floating.
4. Fabrication the SoC system on hybrid technologies to achieve higher gain of the antenna, to save power and increase communication range is a promising area of research.
5. This work can be extended to a multi-sensor wireless system by implementing digital modulation scheme to communicate with and identify individual sensors.

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