Analog Correlation of Low Data Rate UWB Impulse Radio for Medical Applications

Submitted by

Andrea Liao, B.Eng., M. Sc.

A thesis submitted to the Department of Electronics in partial fulfillment of the requirements for the degree of Master of Applied Science in Electrical Engineering

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Professor Calvin Plett, Supervisor

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Abstract

Low data rate UWB impulse radio has become a promising candidate for short range communication in medical environment due to its simple architecture, small form factor and ultra low power consumption. Fully digital or digital intensive architectures cannot remove the fundamental ADC sampling bottleneck for the UWB system under current CMOS technology [1]. However, by moving correlation into the analog domain, overall system performance can be improved by reducing the circuit complexity, ADC sampling speed and power consumption. The main design challenges are the high performance yet low power analog correlator and alignment of the extremely narrow pulse template in the time domain.

This thesis focuses on the design and analysis of a passive clocked correlator tailored for low power IR-UWB. A test bench and its individual components are designed to test the correlator performance. For comparison, a double balanced Gilbert Cell based analog multiplier is introduced as part of an active correlator. A double balanced Gilbert Cell is designed using $\frac{g_m}{I_d} * f_t$ figure-of-merit to meet both speed and low power requirements. A specific test bench is also designed to test the active correlator's performance.

Due to UWB specific signal characteristic – signal level is very low and comparable to noise level, the correlator design needs to consider the difference between mixer/modulator and analog multiplier which deals with very small input signals. This thesis not only contributes a comparative study between a passive and an active correlator but also identifies some important design issues. For the passive correlator, nonlinearity at both RF and LO ports and extra noise generated

from clock feed through due to large LO amplitude are the main design challenges. The double balanced Gilbert Cell based active correlator is sensitive to offsets due to its nonlinear operation, device mismatches, process variations and unequal path delays in differential structure. The short channel effects further impair the linearity. These offsets reduce resolution and degrade linearity and overall system performance. These studies provide guidelines for future high efficiency and low power IR-UWB receiver design.

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I don't know how to express my appreciation to my parents, for their openness to accept me as who I am and what I enjoy doing; for their full support and patience over these years which enable me to go farther and further.

Many thanks always go to Uncle and Aunt Ho, far away in Hong Kong but always close to my heart. Without their support and encouragement, I would not have a chance to come to US for my higher education; to open my eyes only to find the world is not only round but also flat, and you can achieve a lot if you are willing to try.

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Andrea Liao

Dec. 20, 2010

To my parents, for their full support and patience through these years

To my mentors, for their encouragement to search for excellence and continuous intellectual development

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List of Abbreviations and Symbols

UWB	Ultra Wide Band
IR	Impulse Radio
IR-UWB	Ultra Wide Band Impulse Radio
ADC	Analog to Digital Converter
SNR	Signal to Noise Ratio
FCC	Federal Communications Commission
MAC	Media Access Control
PAN	Personal Area Network
BAN	Body Area Network
PSD	Power Spectrum Density
PHY	Physical Layer
EIRP	Effective Isotropic Radiated Power
OFDM	Orthogonal Frequency Division Multiplexing
TH-IR	Time Hopping Impulse Radio
OOK	On and Off Key Modulation
PPM	Pulse Position Modulation
IL-VCO	Injection Locking Voltage Controlled Oscillator
PRF	Pulse Repetition Frequency
VCDE	Voltage Controlled Delay Element
ACV	Across Chip Variation
NF	Noise Figure

LO	Local Oscillators
IF	Intermediate Frequency
RF	Radio Frequency
DLL	Delay Locked Loop
PLL	Phase Locked Loop
SAR	Specific Absorption Rate
DFF	Delay Flip Flop
CML	Current Mode Latch
f_t	Transit Frequency
$\frac{g_m}{I_d}$	Current Efficiency
ECG	Electrocardiography
EEG	Electroencephalography

Chapter 1

Introduction

The first Ultra-Wide Band (UWB) transmission experiments by Heinrich Hertz in 1887 used a spark-gap transmitter, which naturally generates impulse signals with a very wide bandwidth. Since then, UWB systems have been primarily used in military applications like radar or secure communications. Location and ranging are the initial UWB applications for military and are still very popular for human and animal rescue during disaster and mining. Due to the lack of frequency control and Media Access Control (MAC) protocol to reduce interference, narrow band communication became more popular much later. In the 1990s, the advancement of digital signal processing capability, especially the introduction of time hopping impulse radio by Robert Scholtz and Moe Z. Win [2] [3] spurred new interest in this old technology for civil use. Research efforts from both academia and industry have gained momentum in this area after the Federal Communications Commission (FCC) made 3.1GHz ~ 10.6GHz frequency band available for unlicensed UWB devices. The European Commission (EC) and Japan soon opened their own unlicensed UWB frequency band for commercial usage.

1.1 Research Motivation

IR-UWB Impulse Radio is an ideal candidate for short range communication in medical environment due to its simple architecture, small form factor and ultra low power consumption. The low data rate IR-UWB has enough bandwidth to handle the monitoring and data collection tasks with better interference immunity.

Although the non-coherent transceiver has simple architecture, its bandwidth utilization is not efficient enough and the SNR is degraded due to the low signal density level. For secured vital signal transmission, a coherent system with synchronization is still a better option to obtain reliable link, especially for locating and accurate ranging purpose. More information on coherent and non-coherent transceiver can be found in Section 2.2.1.

The fully digital coherent transceiver has the advantages of flexibility, scalability and low power. However, in the fully digital transceiver, the power consumption is dominated by ADC and matched filter banks. The ADC sampling rate needs to be at least twice the signal bandwidth and is usually in the GHz range. This type of high speed, wideband, low power ADC is very difficult to design and is power hungry as well.

By moving the signal correlation into the analog domain, the major drawbacks of the fully digital architecture mentioned above have vanished. However, the design challenges become the generation and alignment of the extremely narrow pulse template in the time domain. This is the focus of this thesis which is going to be investigated and documented.

1.2 Thesis Contribution

This research is focused on timing correlation of low data rate IR-UWB for medical sensor in Body Area Network (BAN). A passive and an active correlator are compared by multiplying the incoming pulse with three different templates, namely sine wave, clock and 5th derivative Gaussian pulse. Their individual performance and resistance to interference have been studied as well.

The intermittent characteristic of UWB pulse makes the passive correlator appropriate to reduce overall power consumption. However, the passive mixer based clocked correlator has some intrinsic issues related to linearity at both RF and LO ports which greatly affects its multiplication functionality. The differences between mixer and analog multiplier are presented in terms of their function and noise figure.

The double balanced Gilbert Cell based active correlator is carefully examined in terms of its linearity, DC offsets, power consumption. The short channel effects on the performance of the active correlator are also analyzed and discussed.

The main contribution of this thesis is that not only a comparative study of a passive clocked correlator and a double balanced Gilbert Cell based active correlator has been presented, but the most important intrinsic and potential issues about these two correlators are identified, especially nonlinearity and offset analysis in short channel devices. An ultra low power, low voltage analog multiplier with wide dynamic range is ideal for correct precise multiplication with fast response for IR-UWB analog correlation. In order to achieve these goals, compensation and calibration circuits are needed to cancel third order nonlinear components and reduce unequal path delay as well as overall power consumption.

1.3 Thesis Overview and Organization

The thesis contains six chapters and is organized as follows:

In Chapter 1, a quick review is provided, followed by a discussion of the research motivation and contributions. Finally, the research objectives and contributions are presented before the thesis organization is outlined.

The second chapter has two major parts. The first part gives a brief history background about the UWB signal characteristics such as pulse shape and FCC spectrum regulations. The comparison

between conventional narrow band communication and UWB provides extra insight about this unique communication protocol. Following that, the applications of low data rate UWB Impulse Radio especially in medical areas are given.

The second part of Chapter 2 gives a brief architecture literature review by comparing the design challenges and trade-offs between coherent and non-coherent receiver architecture, fully digital and partially analog architecture. Special emphasis is given to different analog timing synchronization mechanisms.

In the third chapter, a passive clock correlator together with its test bench is proposed. Components circuit design and performance are shown following the test bench. Analysis illustrating the weakness of the passive correlator due to the nonlinearity at the RF and LO port is also presented.

In the fourth chapter, an active double balanced Gilbert Cell based correlator and its specific test bench are designed and analyzed. Its performance is compared with the passive clocked correlator. In the correlator analysis, some important design issues have been identified, such as DC offsets due to transistor nonlinearity, unequal path delays, process variations and device mismatches. Especially, the short channel second order effects give extra third order nonlinear components in the differential output current.

In the last chapter, a summary of research contributions is outlined and future work has been identified. Suggested future work includes extending the linearity, compensating DC offsets and calibrating the circuit to cancel nonlinear components and eventually closing the synchronization loop.

Chapter 2

Background and Architecture Literature Review

Among all the existing wireless communication technologies, the Ultra Wideband Impulse Radio has many advantages over other narrow band wireless communication protocols because the spreading of transmitted power over a wide range of frequencies not only improves the noise immunity from the adjacent narrow band signals but also provides precise ranging and locating. From the hardware point of view, the circuit design has to take many factors into consideration, such as modulation scheme, power limitation, interference immunity and system complexity.

In this chapter, the history background behind this research will be discussed. Several major architectures will be introduced and their advantages and disadvantages will also be presented. But first of all, UWB signal characteristics need to be introduced because it has a big impact not only on the signal modulation but also overall architectures.

2.1 UWB Signal Characteristics

2.1.1 UWB Pulse

Today, most wireless communication systems are based on sinusoidal waves although the first communication system was in fact pulse-based. In 1893 Heinrich Hertz used a spark discharge to produce electromagnetic waves for his experiment. These waves would be called colored noise today. [4]

The UWB Impulse Radio (IR-UWB) is alternatively referred as Carrierless Ultra Wideband Pulse Radio. It is the signal transmission which carries information through extremely narrow

Gaussian pulses (extremely wide bandwidth in frequency domain) without carriers. UWB is essentially spread spectrum communication with a very large spreading factor. The pulse duration and shape determine the signal spectrum. As is shown in Figure 2-1 for the relationship between time and frequency - a narrow pulse is a direct indication of a wide bandwidth and fine range resolution [5]. This is because one frequency only gives one point of information about the object, the richness in frequency domain (a short pulse in time domain) provides wide range of information about the object. Furthermore, a wide bandwidth gives precise ranging because the ranging accuracy is proportional to the bandwidth of the emitted signal. [5]

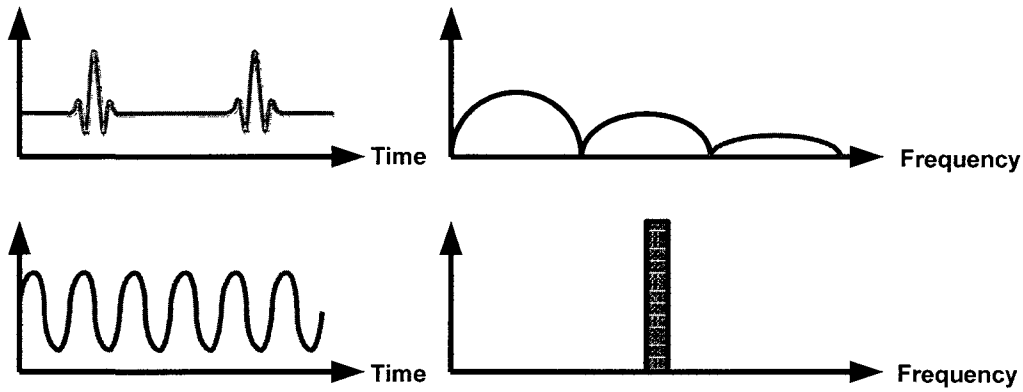


Figure 2-1 UWB Pulse in Time and Frequency Domain

A theoretical Gaussian waveform is usually modeled as

$$G(t) = \frac{1}{\sqrt{2\pi\sigma^2}} e^{-\frac{x^2}{\sqrt{2\sigma^2}}} \qquad (2\text{-}1)$$

A Gaussian monocycle has a single zero crossing. The differentiation of a Gaussian waveform produces a Gaussian monocycle pulse which has a single zero crossing. Further derivatives yield additional zero crossings, one additional zero crossing for each additional derivative [4] as shown in Figure 2-2.

The more zero crossings, the narrower the bandwidth and the higher the center frequency assuming the time between zero crossings is reduced [6]. These Gaussian waveforms can be easily generated by digital circuitry which is shown in Section 3.2.4 and Appendix I. IEEE 802.15.4a in 2007 redefined the UWB physical layer and the pulse has less restrictive requirements as long as it looks sufficiently close to the reference pulse. The pulse shape selection is more dependent on the application and system design.

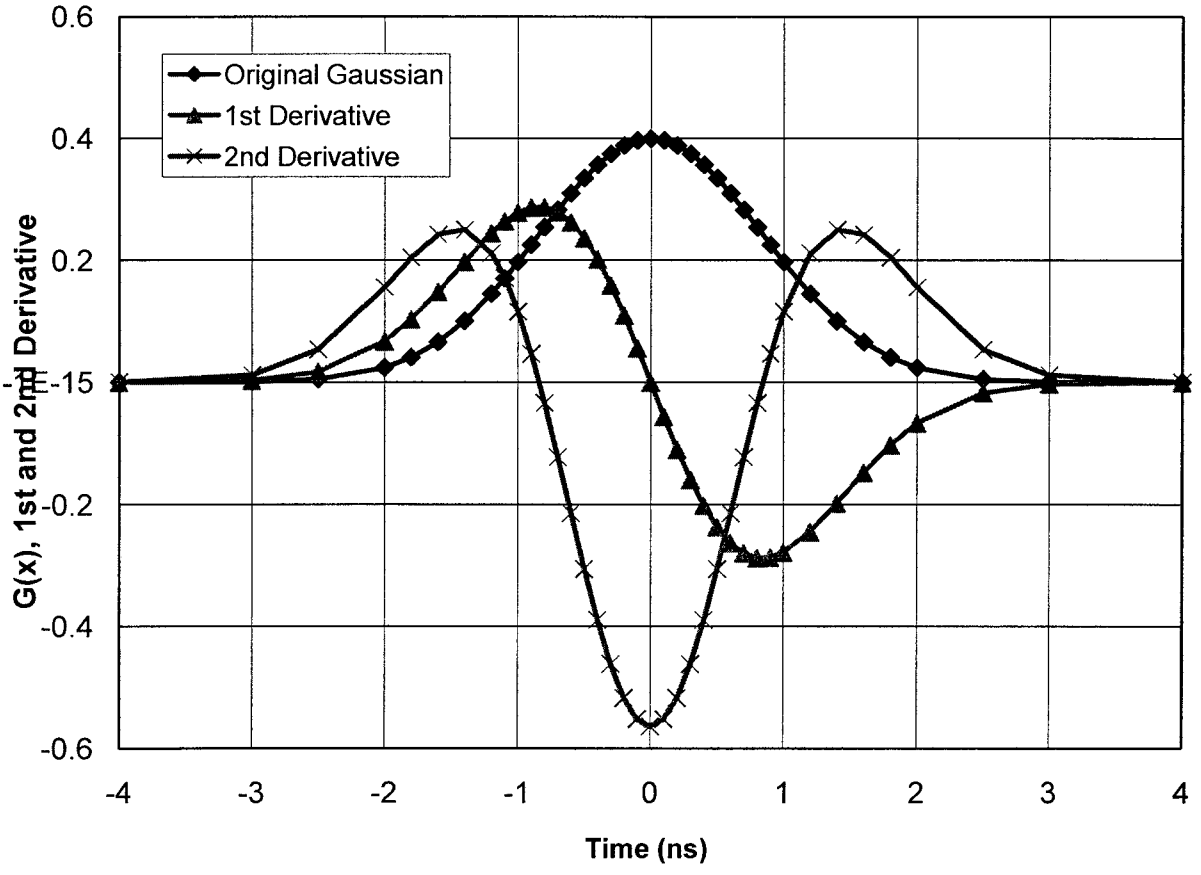


Figure 2-2 UWB Pulse Shape and its Derivatives

A fifth derivative Gaussian waveform is used to represent the UWB impulse in this thesis.

$$G_5(t) = \mathrm{A}\left(-\frac{t^5}{\sqrt{2\pi\sigma^{11}}} + \frac{10t^3}{\sqrt{2\pi\sigma^9}} - \frac{15t}{\sqrt{2\pi\sigma^7}}\right) e^{-\frac{t^2}{2\sigma^2}} \qquad (2\text{-}2)$$

A is the pulse amplitude, σ is a time constant, t is time.

2.1.2 UWB Spectrum Regulations

UWB Impulse Radio transmits extremely narrow Gaussian pulses without carrier. The transmission power can be spread over a wide bandwidth from 3.1 GHz to 10.6 GHz. FCC regulations in the United States define the Ultra Wide Band either as absolute bandwidth bigger than 500 MHz or as fractional bandwidth which meets the following requirement: [7]

$$\text{Fractional Bandwidth} = \frac{2(f_H - f_L)}{f_H + f_L} > 25\%$$

UWB regulations in Europe and Japan have different definitions. The European Commission (EU) requires that UWB devices operate between 6 GHz and 8.5 GHz. In Japan, the UWB devices are allowed to operate between 3.4 GHz and 4.8 GHz. Although the UWB operating frequencies vary in different countries and regions, their power spectral density, i.e. EIRP, has the same limits - lower than – 41.3 dBm/MHz.

IEEE Standard 802.15.4a sets strict regulations for unlicensed UWB devices worldwide [7]. The highest allowable limits for UWB emissions are based on an Equivalent Power Spectrum Density (PSD) of – 41.3 dBm/MHz. Under these limits, the allowable transmit power for a 500 MHz bandwidth UWB device would be less than –14 dBm, or about 37 μW transmit power.

For low data rate Wireless Personal Area System (PAN), an amendment was made to IEEE 802.15.4a in 2007 and a new UWB PHY was redefined at higher mandatory nominal rate of 851 kb/s and optional data rates of 110kb/s, 6.81Mb/s and as high as 27.24 Mb/s. [7]

2.1.3 UWB Modulation Scheme

For high data rate UWB system, the popular modulation scheme is multiband Orthogonal Frequency Division Multiplexing (OFDM) which forms a wideband signal through orthogonal narrow band subcarriers. OFDM system provides data rate up to hundreds of Mbps with robust channel frequency selectivity. [8]

For low data rate sensor network, OFDM is no longer appropriate since the system requires high sampling rate ADC which consumes a lot of power. Instead, time-hopping impulse radio (TH-IR) in the time domain offers better system and circuit trade-offs. TH modulation distributes more uniform RF signal power to its bandwidth. Pulse Position Modulation (PPM) and On-Off Key (OOK) Modulation are under consideration in this thesis.

2.1.4 Ultra Wide Band vs. Narrow Band Communication

Wireless systems can be divided into several subcategories according to the bandwidth: narrowband, wideband, broadband and ultra-wide band. Narrowband systems support low data rate transmission, whereas wideband systems support high data rate transmission. Narrowband transmission rates are typically below 64Kbs and wideband transmission rates are from 64 Kbps to 2 Mbps. For broadband, data rates vary from 1.5 Mbps (T1) to 45 Mbps (T3) and the bandwidth is divided in to multiple channels of which each of these channels is narrowband. However, what actually determines broadband is that the allocated bandwidths are quite specific such that Channel 1 and 4 carry data, Channel 2 and 5 carry audio and Channel 3 and 6 carry video.

Narrowband implies that the communication channel is sufficiently narrow that its frequency response can be considered flat. By the same token, a system is typically described as wideband if the bandwidth significantly exceeds the channel's coherence bandwidth. Here, the coherence

bandwidth is defined as the frequency band within which all frequency components are equally affected by fading due to multipath propagation phenomena. Narrowband systems are affected by nonselective fading, whereas wideband systems are affected by selective fading.

The UWB transmission power is spread over an extremely wide bandwidth from 3.1GHz to 10.6GHz and the low signal density is comparable to the noise floor. The large spreading not only improves the noise immunity from the adjacent narrow band signals but also provides precise ranging and locating. The extremely narrow UWB pulse width in the time domain has two meanings: one is that most signal reflection does not overlap the original pulses, therefore the traditional multipath fading of narrow band signals does not exist; the second is that the pulses can penetrate materials with little energy loss and can be recovered from very limited amount of reflected energy. [9]

In conventional communication, a low frequency wave can penetrate objects because its wavelength is much longer than the material it passes through. A high frequency wave is reflected due to it short wavelength [5]. The penetration capability of UWB comes only from the low frequency components while the reflected energy comes from the high frequency components. The reflected signals across the boundary between different dielectric media give valuable information about the property and location of the object [9]. In UWB impulse radio, the short pulse in the time domain covers a wide range of frequencies in the GHz range. Both low frequency and high frequency components provide meaningful information about the targeted object including high resolution and accuracy.

These attributes are the fundamental differences between Ultra Wide Band and narrow band communications which make it very attractive for low data communication with precise locating and ranging. In medical areas, IR-UWB is quite suitable for non-invasive medical radar imaging and early cancer detection.

Due to many sensor nodes in the Ultra Wide Band sensor network, the coexistence between the UWB transceiver and narrow band system needs to be considered seriously. For IR-UWB system, the pulse shape and the narrow band interferer frequency would strongly affect its performance. Although a single UWB interferer has negligible effect, the accumulated effect from many UWB transmitter nodes might not be ignored. Also the interference could have bigger impact when a narrow band receiver is closer to the UWB transmitter rather than to its own transmitter. Therefore, fully understanding the interference and coexistence between UWB sensor nodes and narrow band system is essential to design a robust system. [10]

2.2 IR-UWB for Medical Applications

2.2.1 Low Data Rate Communication

Due to the high medical expense, most patients have to return home after a short stay in hospital. Doctors can still monitor the patients' health situation through Wireless Personal Sensor Network linking to the sensor nodes attached to the patients. In hospital settings, the wireless sensor network needs to locate and track medical equipments, doctors, nurses and patients in a dynamic environment. This type of health care/industry monitoring sensor network only requires low data rate communication with robust performance, and the system has to be low cost as well.

As mentioned before, an amendment was made to IEEE 802.15.4a in 2007 and a new UWB physical layer redefined for Wireless Personal Area Network (PAN) at higher mandatory nomin-

al rate of 851 kb/s and optional data rates of 110kb/s, 6.81Mb/s and as high as 27.24 Mb/s. The UWB pulse has less restrictive requirements as long as it is sufficiently close to the reference pulse [7].

BAN is defined as a small scale wireless network close to human body which is made of multiple in-body implant sensors and on-body non-invasive sensors. It is a short range (2m~5m), low data rate, ultra low power wireless communication link which collects real time physiological parameters such as ECG, EEG, blood flow and pressure for timely monitoring and analysis. The presence of a body impacts the channel model and may require attention to additional regulatory issues like Specific Absorption Rate (SAR) limits. [7]

The BAN can be divided into two different categories by their working channels: on-body Wearable BAN and in-body Implantable BAN. Wearable BAN has more multipath channels while Implantable BAN experiences severe decay during transmission. Besides, Implantable BAN has more restriction on power dissipation so that devices require power scavenge techniques. These two BANs can be supported by two different PHY layers or share only one PHY with a coordinator in between. IEEE Standard 802.15.6 (BAN) physical layer is still under continuous development and IR-UWB is a viable communication option, citing all the signal and system benefits mentioned.

Both these low data communication links – PAN and BAN can be implemented by UWB Impulse Radio which provides secure and reliable data transmission. The UWB Impulse Radio is a

potent candidate for future short range communication in medical area which provides excellent signal penetration, good interference immunity and ultra low power consumption. For UWB pulse signal, the wide bandwidth directly implies fine range resolution. This characteristic can be used in the case of "camera pill" which is used to track and send patient intestine images from inside to outside doctors. These signals are very weak and location accuracy is rather important to determine the patient's condition.

Due to the specific applications and operating environments, the transceiver designs are different. For the sensor and monitoring purpose, the major design concern is low power; while for BAN transceiver, not only the power has to be kept extremely low, but also the signal decay needs to be addressed accordingly.

2.2.2 Medical Radar and Imaging

In 1996, Tomas McEwan introduced the Micropower Impulse Radar (MIR) in Lawrence Livermore National Laboratory [9]. The experiment was based on the two important features (penetration and reflection) observed in this pulse based system mentioned before. It also pointed out that MIR can be used in low cost sensor system, motion detection and microwave imaging.

In 2002, Enrico M. Staderini at University of Rome created a more accurate model which considered thickness, impedance, linear attenuation, and wave speed of six superimposed living tissues to be found by the UWB pulse [11]. Medical applications such as tissue imaging and health monitoring were prototyped in the paper.

The penetration and reflection attributes make IR-UWB perfect to be used in medical areas. The pulse has excellent penetration capability through the human body's nonlinear structure by ref-

lection and resonance. By continuously measuring the time intervals between the sent pulses and the reflected pulses, the temporal and spatial changes of the tissues can be determined depending on the characteristics of the reflected pulses. This has enormous meaning for early cancer detection imaging.

Susan C. Hagness's group at the University of Wisconsin and several other research teams are working on UWB microwave imaging for early stage breast cancer detection [12]. The scattered UWB pulse energy is collected to form a spatial image in order to identify the presence and location of the malignant lesions. The experimental feasibility of UWB imaging is demonstrated using an imaging prototype and multilayered breast phantoms [1]. In this literature review, only a brief overview of UWB microwave medical imaging research was given because this is not our research focus. But it is really worthwhile to mention this since this has been an active research area for quite some time in medical imaging field. More information can be found in Reference [8], [9], [11] and [12]

2.3 Architecture Literature Review

2.3.1 Coherent and Non-Coherent Architecture

A coherent receiver can exploit the absolute phase information of the received carrier-modulated signal, while a non-coherent energy detection receiver can only exploit the envelope, i.e. instantaneous power of the signal [13] . The coherent receiver has to recover the phase, amplitude and timing information using a local reference template, while the non-coherent receiver does not

[1] Breast phantoms is a reusable ultrasound guided biopsy training device. The reusable device heals itself and the self-healing solid gel mimics the ultrasonic characteristics of tissues found in an average human breast.

need a local reference template which significantly reduces the system complexity at the cost of lowered link margin. [14]

The main motivation behind the non-coherent suboptimal receiver is that it has very simple architecture and low power consumption. Local template generation and timing synchronization do not have to be considered in this type of receiver. However, due to its extremely narrow pulse width and low signal density, the non-coherent architecture is not suitable for UWB Impulse Radio in the noisy environment which could misinterpret the location and ranging accuracy.

Coherent versus non-coherent modulation is a key system tradeoff. A coherent system is more efficient at bandwidth utilization and has higher signal-to-noise ratio. Its frequency accuracy is normally smaller than 100ppm, while the non-coherent system is usually above 1000ppm.

2.3.2 Digital and Analog Correlation

The narrow band system usually requires a tuned structure and carrier generation circuitry which consumes a lot of power. On the other hand, UWB signal power can be spread over a wide range of frequencies which means a tuned structure and carrier generation circuitry are not necessary. The transceiver can be implemented as fully digital or partially digital architecture.

In the last decade, fully digital transceivers mainly operate in the low frequency bands less than 1GHz. In this type of system, the RF front end is usually kept very simple and signal correlation is pushed into the digital domain. The main advantages of the fully digital transceiver are its flexibility, scalability and low power. However, its power consumption is dominated by the ADC and matched filter banks. The ADC sampling rate needs to be at least twice the signal bandwidth and is usually in the GHz range [15]. This type of high speed, wideband, low power ADC is very difficult to design and power hungry as well. The ADC speed can be lowered by introduction of

parallelism such as channelized ADC and partially digital subsampling ADC structure which will be introduced shortly. However, none of these techniques could fundamentally solve the issues related to high speed ADC.

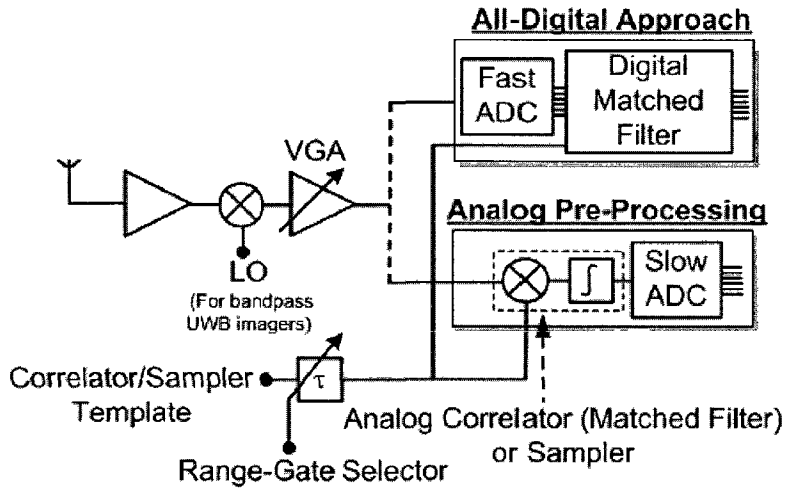


Figure 2-3 All-Digital Approach and Analog pre-processing [16]

Figure 2-3 shows the correlation difference between the all digital approach and analog pre-processing approach in a UWB radar receiver. The upper path is all digital approach in which all signal processing is done in the digital domain. In this case, the ADC sampling rate has to be at least twice the signal bandwidth. The lower path takes advantage of analog pre-processing by using an analog correlator in the front end. The ADC in this case only needs to operate at the pulse repetition rate which greatly relax the ADC design requirement.

By moving the signal correlation into the analog domain, the major drawbacks of the fully digital architecture mentioned above has vanished. However, three difficulties still remain:

i) Circuit Level - Pulse template generation in the time domain

ii) Circuit Level - Precise pulse signal alignment

iii) System Level - lack of flexibility, scalability

At the circuit level, pulse template generation becomes very critical in circuit design because the extremely narrow pulse width is in the sub-nanosecond range. The individual component needs to be designed to handle large bandwidth in the GHz range yet consume as little power as possible. In the time domain, these components have to be fast enough to detect the maximum correlation amplitude between the incoming pulse and template pulse.

A windowed-sine-wave based pulse template is proposed by Lee [17] to ease the difficulty of pulse generation. The correlation becomes the multiplication of the sine-wave pulse template and the incoming signal, followed by a windowed integration. The optimal window length is 1.2ns for the optimal SNR with the smallest processing gain loss compared to the real matched filtering. It also shows that the lowest SNR degradation is roughly 1.7dB when the template frequency is 1.25GHz and correlation time is 0.6ns. Most importantly, the degradation is quite flat over the frequency when the correlation time is +/-0.5ns. Although this system is convenient to build, for high resolution and ranging accuracy applications, it might not be an optimal option.

2.3.3 Fully Digital and Digital Intensive Architecture

The fully digital transceiver is the optimal architecture for low frequency system. In digital process, the power consumption from digital circuits decreases faster than analog circuits when the leakage current is not the dominant source. So the technology scaling would greatly benefit the low power requirement. However, as CMOS technology goes beyond 90nm, leakage current becomes a serious issue which makes the fully digital architecture not as attractive as before. Next, several architectures ranging from fully digital structure to partially analog structure will be given for comparison.

2.3.3.1 Direct Conversion Architecture

In this architecture, the incoming signal is down converted to baseband directly through quadrature structure. The signal is then sampled by two very high speed ADCs and processed by the DSP in the digital domain. This structure is able to handle parallel signal processing and has relative flexible system. However, the ADC has very high requirements in terms of speed, bandwidth and dynamic range which are detrimental to the low power purpose. Although lowering the ADC resolution would help to reduce the power consumption, the overall system performance is greatly degraded.

2.3.3.2 Bandpass Subsampling Architecure – Partially Digital

The communication theory behind the bandpass subsampling is that the receiver samples the bandpass signal at harmonic frequency which is lower than the higher end of the frequency band F_h. The bandpass spectra, the sampling pulse spectrum and sampled signal spectrum are shown in Figure 2-4.

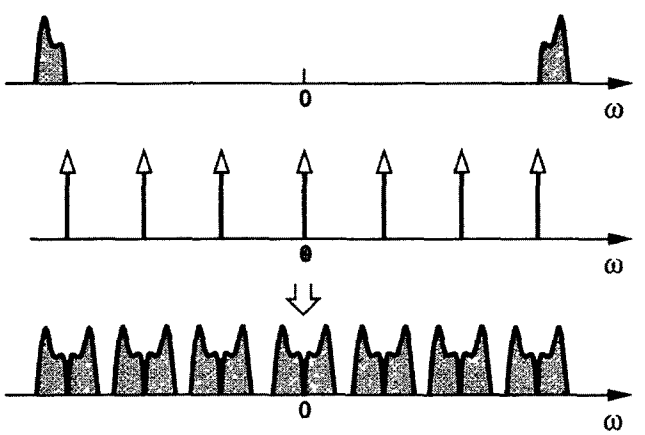


Figure 2-4 Spectra of Bandpass Sampling [18]

The signal sampling rate has to be in the range $\frac{2f_H}{n} \leq f_s \leq \frac{2f_L}{n-1}$ to avoid alias.

A band pass subsampling technique shown in Figure 2-5 is proposed by Michael Shuo-Wei Chen in Robert Brodersen's group [19]. There are two advantages in this architecture – the first is that the frequency translation can be done in the sampling process by using sub-sampling. In this case only one receiver path is needed and the component counts are dramatically reduced compared to a direct conversion architecture. The other advantage is that the ADC sampling rate can be greatly relaxed which in turn lowers the power consumption substantially. However, the ADC still samples at relatively high speed in the current CMOS technology and the power consumption problem cannot be fundamentally resolved. Besides, the receiver requires a high Q and sharp roll-off band pass filter which is very difficult to design at RF frequency. One other issue is that the noise from lower band would alias into the signal band which greatly degrades the SNR ratio.

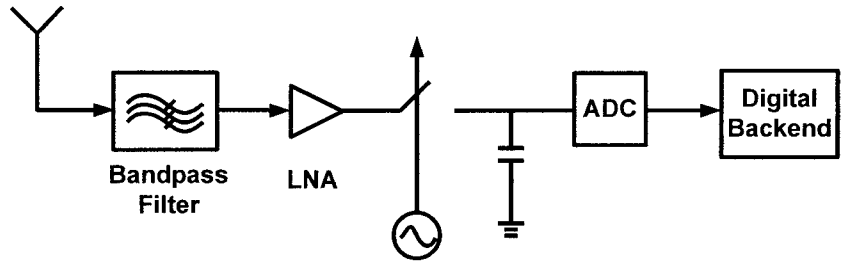


Figure 2-5 Bandpass Subsampling [19]

2.3.4 Analog Correlation Architecture

Several analog correlation architectures will be introduced based on how the pulse template is generated and how the correlator feedback loop tracks the incoming pulse. There are two main categories: Delay Line Feedback Loop based timing controller (sliding mechanism) to synchronize the data, and Injection Locking Method which eliminates the clocks and other delay cell generation circuits.

2.3.4.1 Quadrature analog correlation

A quadrature analog correlation is proposed by Julien Ryckaert in Geert V. Plas group at Katholieke University Leuven [20]. The input signal has I/Q paths and the analog correlation happened in the mixers where the LO signal is fed in, as shown in Figure 2-6. The pulse correlation operation is done in the analog domain which greatly reduces the ADC sampling rate down to the pulse repetition rate, therefore the power consumption is reduced. Instead of using an ideal UWB pulse, a rectangular window with minor loss less than 1dB is used. The correlation with this rectangular window can be achieved by integrating a time window set by the timing circuit. Figure 2-6 shows the whole system.

The timing synchronization is implemented through two cascaded delay lines of which each contains another two series delay circuits.

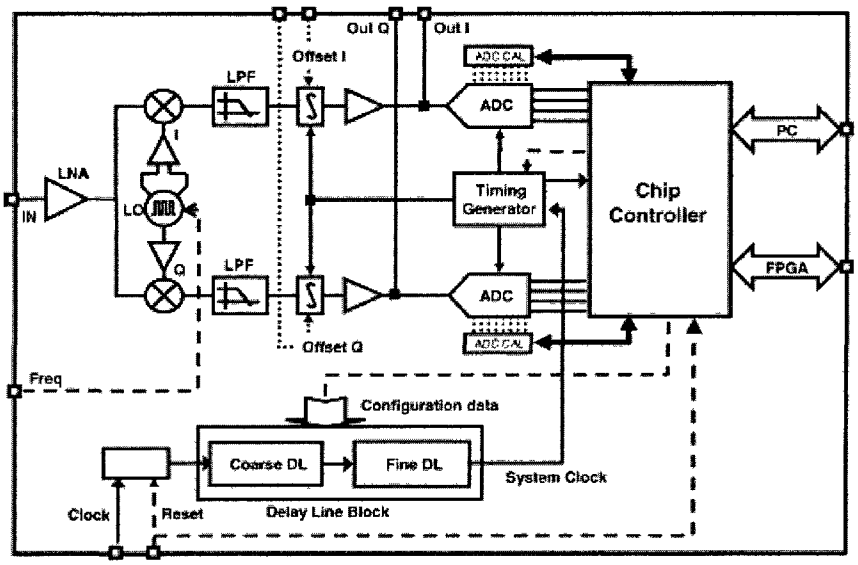


Figure 2-6 Quadrature Analog Correlation

The first delay line is to generate multi-phased signals that enable the time window for analog correlation. The block diagram is shown in Figure 2-7. The two delay line circuits inside of it are for PPM delay and time window setup.

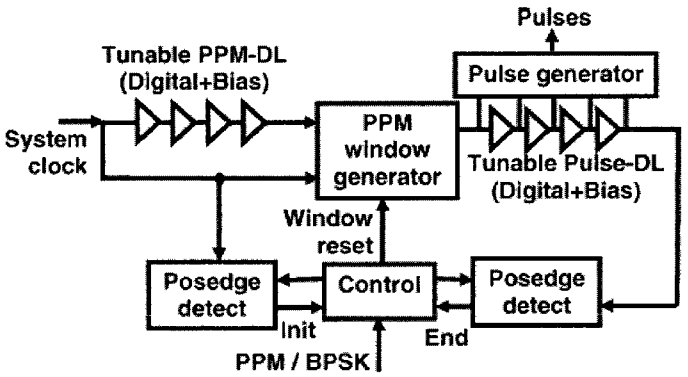


Figure 2-7 Programmable duty cycle generator (multi-phase signal generation)

The second delay line is to synchronize the receiver system clock with the received pulse stream. As shown in Figure 2-8, a coarse and a fine delay circuits are cascaded together. These circuits are controlled by the synchronization algorithm built into the digital circuit.

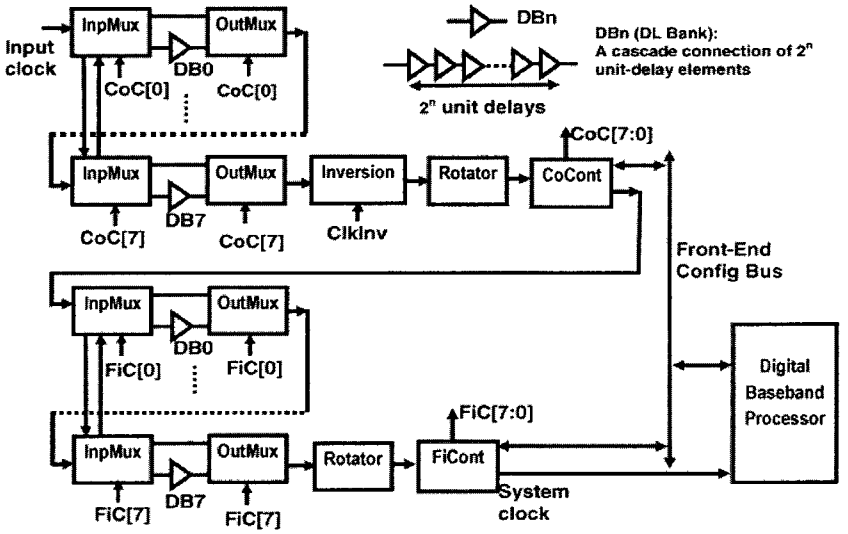


Figure 2-8 Programmable delay line for acquisition

This architecture saves power by moving the pulse correlation into the analog domain while perform the timing synchronization in the digital domain through multiple delay line circuits.

2.3.4.2 Sliding Synchronization Scheme

The first main category - analog correlation test bench using a sliding scheme for data synchronization is shown in Figure 2-9.

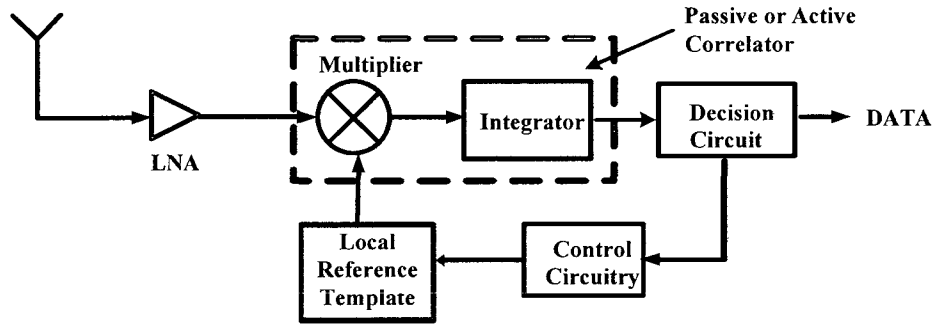


Figure 2-9 Analog Correlation Test Bench

The synchronization process involves two activities - acquisition and tracking. During acquisition process, the incoming pulse is delay adjusted roughly with respect to the template pulse. Following the coarse delay, a fine delay searching is continued in order to align the incoming pulse with the template pulse. A tracking loop is needed in this process in order to lock the template pulse delay to the received pulse and maintain the alignment. The Sliding Timing Synchronization Mechanism synchronization mechanism is shown in Figure 2-10.

During the synchronization process, two components are very crucial to the performance. One is the timing controller which is part of the tracking loop, the other one is the correlator. The correlator is made of a mixer (passive or active) and an integrator. Chapter 3 and Chapter 4 give detailed discussion about these two correlators.

The timing controller consists of multiple delay lines and a control circuit as shown in Figure 2-10 [21]. The controller selects one of the delay lines to generate a local pulse template. Acquisition is detected by evaluating whether the multiplication of incoming pulse and the local pulse

template is the maximum correlation output. If the detection is not obtained, the controller continues to search the delay lines until it finds the maximum output.

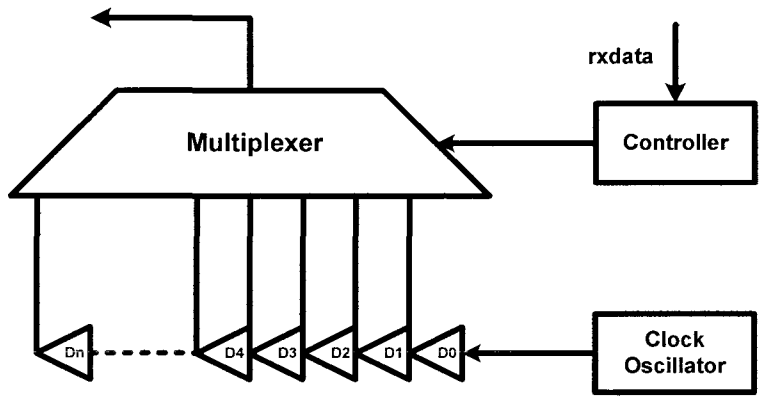


Figure 2-10 Sliding Timing Synchronization Mechanism

Next, two different timing controllers and their related synchronization scheme will be presented and compared in terms of their pros and cons. One type controller is Delay Lock Loop based Timing Controller; the other type of controller is Two-Step Multiplexer-based Timing Synchronizer.

2.3.4.3 Cascaded Delay Lock Loop based Timing Controller

The Delay Lock Loop based timing controller proposed by Yuanjin Zheng in Yong-Ping Xu's group is a cascaded implementation of the timing tracking scheme. Instead of using a large amount of delay cells, this tracking loop is made of two stages of DLL structure for coarse and fine acquisition. Figure 2-11 shows the single stage DLL structure. In the cascaded DLL architecture, the first stage DLL has ten coarse delays and each delay is 1ns. Its phase error output is fed into the 2^{nd} stage. The second DLL divides the 1ns further with 10 fine delays (0.1ns each). The cascaded two-level DLL only need 20 delay cells to implement the 10 ns time span which

greatly reduce the complexity of the circuit. But with two independent DLL structure, the total system is still very clumsy although the concept is relative simple. [22]

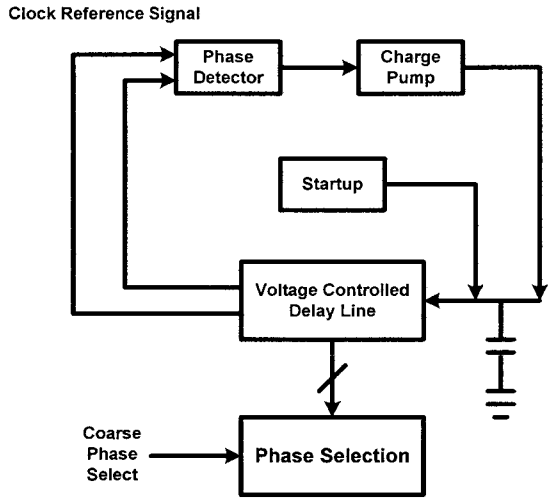


Figure 2-11 Two-stage Cascaded DLL Timing Synchronization

2.3.4.4 Two-Step Multiplexer-Based Timing Synchronizer

Lei Zhou in Payam Heydari's group proposed a similar architecture targeting 2Gbps RF correlation [23]. Although our interest is low data rate application, understanding the architecture still has some benefits. When one-step timing synchronizer is used, the synchronization resolution can be chosen to be 25ps over 500ps pulse period. Twenty CML delay cells and a 20:1 MUX are needed for searching the starting point of the 25ps resolution time frame.

The authors propose a timing synchronization scheme by using a two-step timing synchronizer in order to decrease the delay cell numbers and therefore reduce the synchronization search time. A multi-phase clock generator produces 20 CML delays (5:1 MUX and 4:1 MUX) which define 20 different fine phases. These different phase clocks trigger the pulse generator where the local template pulses are generated. The phase clock associate with the maximum correlation output is the synchronized template generation clock. Through this two-level timing synchronizer, the en-

tire 500ps pulse period can be searched efficiently. Therefore, the circuit complexity and power consumption are both greatly reduced. This architecture is shown in Figure 2-12.

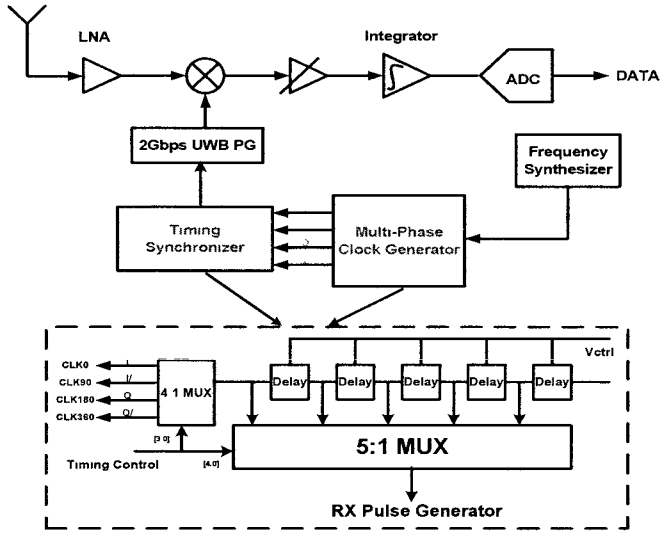


Figure 2-12 Multi-Phase Clock Timing Synchronizer

2.3.4.5 An Injection Locking Method

Although these analog correlation techniques shown above make the IR-UWB timing synchronization much simpler than the fully digital architecture, clocks and plenty of delay cells circuits are still needed in order to search for the maximum correlation output. A new phase synchronization is proposed by Changhui Hu [24]. It uses injection locking to align the phase of incoming pulse requiring no clock recovery circuit.

In VCO design, an injection locking signal is able to override the low frequency control voltage. The VCO therefore lose control of the desirable frequency. Only if intentionally employed, injection locking can significantly reduce circuit power consumption and possibly phase noise.

In the proposed circuit, the incoming pulse injects into ADC and 3.4GHz ~ 4.5GHz Injection-Locked VCO (IL-VCO) at the same time. After the IL-VCO is locked and synchronized with the

transmitter pulse, the clock is phase shifted and divided by N to provide the ADC sampling clock. At the time when ADC sampling clock is equal to the incoming data rate, it is phase locked and aligned to the peak of the incoming pulse. The circuitry is shown in Figure 2-13.

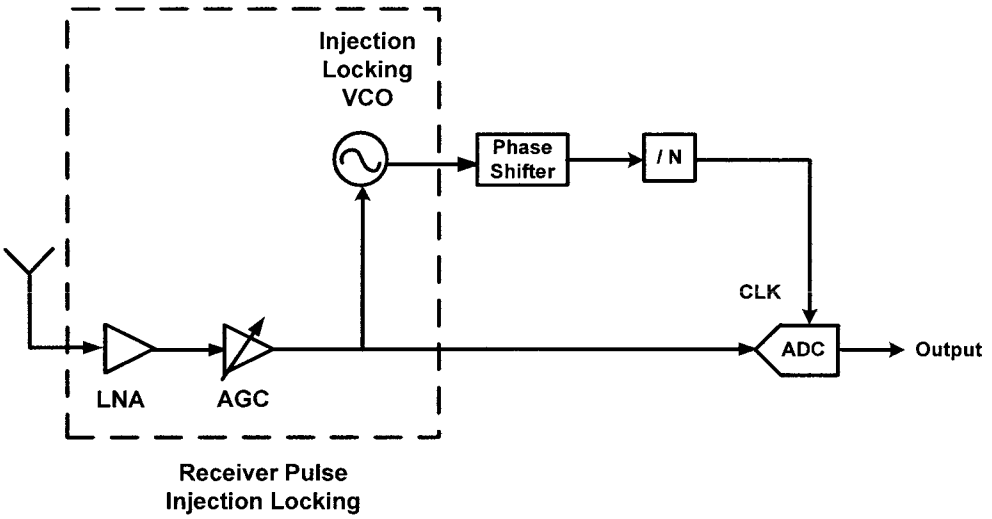


Figure 2-13 Injection Locking

The main motivation behind this architecture is its simple structure which eliminates plenty of extra circuitry for synchronization, therefore reduce power consumption. The other advantage of this architecture is that the system is feed forward without any stability issue. Its fast acquisition and low cost make this technique very attractive for certain applications. However, this method is only applicable to circuits operating at relative high frequency.

2.4 Literature Review Summary

The purpose of this chapter is to give a brief description about the UWB background and related literature review. It starts with the UWB history - signal transistion from pulse mode communication to narrow band communication to UWB system. In order to gain insight about this unique technology, the characteristics of the UWB pulse shape have been briefly described

such as the impact of the pulse shape, modulation scheme. Specifically, the comparision between UWB system and narrow band system is presented in terms of data rate, frequency response and signal characteristics. The FCC spectrum regulations about UWB system is also discussed as part of the introduction.

The UWB impulse radio applications especially in medical area has been the focus of this thesis because of its unique signal attributes – penetration and reflection. Two areas have been identified as low data rate communiation for patient monitoring in sensor network and medical radar for early cancer detection imaging.

In Section 2.3, a brief architecture literature review is given. Different architectures are discussed based on whether they are coherent or non-coherent, digital or analog, fully digital or digital intensive, and analog correlation is the emphasis of this thesis. The advantages and disadvantages have been presented in terms of speed, dynamic range and power consumption. The trade-offs between these parameters are discussed at the system level.

Because fully digital or digital intensive solutions couldn't remove the fundamental ADC sampling bottleneck for the UWB system in the current CMOS technology. Analog correlation turns out to be a promising way to improve the overall system performance by reducing the circuit complexity, ADC sampling speed and power consumption. Two main categories of timing acquisition and tracking methods were introduced for this purpose.

The first category is based on sliding synchronization scheme. In this category, timing controller is the main component for signal acquisition and tracking. There are two types of timing controllers, one is DLL based cascaded timing controller, the other is CML based delay cell

timing synchronizer. Both controllers use two levels of cascading structure to reduce the circuit complexity.

The other category is injection locking method for fast acquisition at low cost. The feed forward system has no stability issue and power consumption is very low due to its simple architecture. However, this method is not suitable for system operating at very slow speed.

This thesis focuses on the first category by using sliding synchronization scheme. In the next two chapters, a passive clocked correlator and an active double balanced Gilbert Cell correlator will be compared and discussed in detail.

Chapter 3

Passive Analog Correlation

In Chapter 2, a variety of architectures are presented to show how received signal correlates with local template. It has been shown that fully digital or digital intensive solutions can not remove the fundamental ADC sampling bottleneck for UWB Impulse Radio for the current CMOS technology. Analog correlation turns out to be a promising way to improve the overall system performance by reducing the circuit complexity, ADC sampling speed and power consumption.

In this Chapter, an analog correlation prototype is first introduced, in which a passive clocked correlator combining a passive clocked mixer and an integrator will be discussed. UWB intermittent operation means the correlation circuit only consumes power (not including the biasing and other assistive circuits) when the input pulse is correlated (includes synchronized and not perfectly synchronized cases) with the local template, therefore the overall power consumption can be reduced significantly. [21] [25]

A testbench specifically designed to test the correlator performance is then discussend. Individual components inside of the test bench, such as the differential 5^{th} derivative pulse generator (designed by Omid Abari and listed as Appendix I), differential voltage controlled delay element (VCDE) and frequency divider have been designed and analyzed.

During the correlator analysis, the difference between mixer and analog multiplier is compared. Mixer operation is mainly focused on frequency translation, the LO amplitude needs to be large enough to turn on/off the transistor as +/-1 function. This switching operation introduced noise

together with large LO feedthroughed interference would degrade the overall system SNR. Therefore, an analog multiplier with both linear inputs is highly desirable.

Next, let us first look at a general analog correlation prototype.

3.1 Analog Correlation Prototype

A general receiver architecture with analog correlation is shown in Figure 3-1. This is just a receiver prototype demonstrating the concept of analog correlation. The designed test bench will be shown and discussed in Section 3.2.

The prototype receiver is made of an antenna, a LNA, a passive or active correlator, a decision circuit, a feedback control loop, a local reference template generator. The correlator consists of a multiplier and an integrator. The multiplier could a passive multiplier or an active multiplier. The decision circuit is more or less a comparator. The feedback control loop uses search algorithm to find a better timing template. The local reference template generator can produce different types of reference template pulse, namely a clock, a sine wave, a Gaussian pulse or a switched sine wave. The functionalities of these individual components are described in a manner how the receiver works.

In this protoptype, the desired low data rate incoming pulse is modeled as a 5^{th} derivative Gaussian pulse, while interference is modeled as a sine wave [26]. The sine wave is easy to generate and is the fundamental composite waveform for other signals. These two signals enter the receiver together through the antenna, and then are amplified by a LNA. A correlator containing a multiplier and an integrator comes right after LNA in the analog domain for signal correlation. The multiplier inside of the correlator could be a passive mixer or an active mixer. The analog correlation occurs inside of the correlator where the incoming pulse multiplies with a local tem-

plate. The local template could be a clock, a sine wave, a 5th derivative Gaussian pulse template or a switched sine wave.

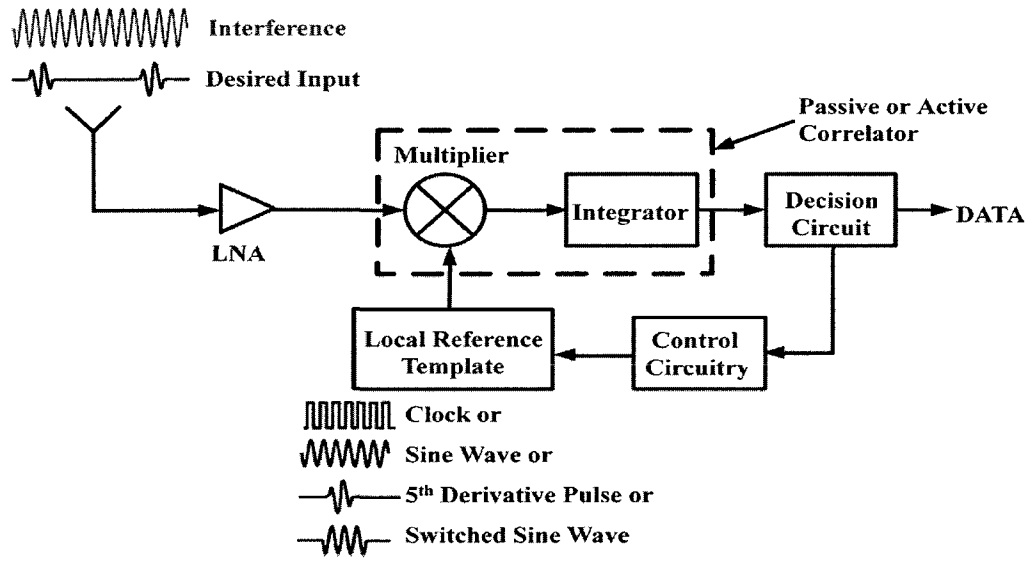


Figure 3-1 Analog Correlation Prototype

A feedback loop containing a timing control and a decision circuit keeps tracking the delay between the local template and incoming pulse in order to find the optimum delay for the maximum correlation output. Only when the input pulse is synchronized with the local template, the maximum correlation can be detected and the multiplied output will be sent to the digital domain for further processing. If the maximum correlation is not detected, the feedback loop continues its searching until the optimum delay is found.

The feedback loop tracks a delayed version of input data. After the analog/digital decision circuit and timing controller, a delayed clock would trigger the pulse generator. The generated 5th derivative pulse becomes the local pulse template. Depending on how the input correlates to the local pulse template and how the feedback loop tracks the timing information, the synchronization scheme in the analog domain varies. These timing tracking mechanisms have been illustrated in

Literature Review Section 2.3.4.

3.2 Passive Correlator Test Bench Design

As mentioned in Section 3.1, the multiplier inside of a correlator could be passive or active. For medical application such as patient monitoring sensor network, a low data rate UWB Impulse Radio has enough bandwidth to collect certain vital signals. Data transmission is not continuous and UWB pulse has very low duty cycle. The device can be operated intermittently which would lower total power consumption. [21] Instead of using a sub-optimum sinusoidal wave template as introduced in Section 2.3.3, a clock template can be used to correlate the incoming pulse, specifically for the passive correlator.

3.2.1 Passive Correlation Test Bench

The passive correlator based receiver prototype is shown in Figure 3-1 and its functionality is described in Section 3.1. In this section, the test bench implementation of the receiver prototype in Figure 3-1 is shown in Figure 3-2 as a fully differential circuit.

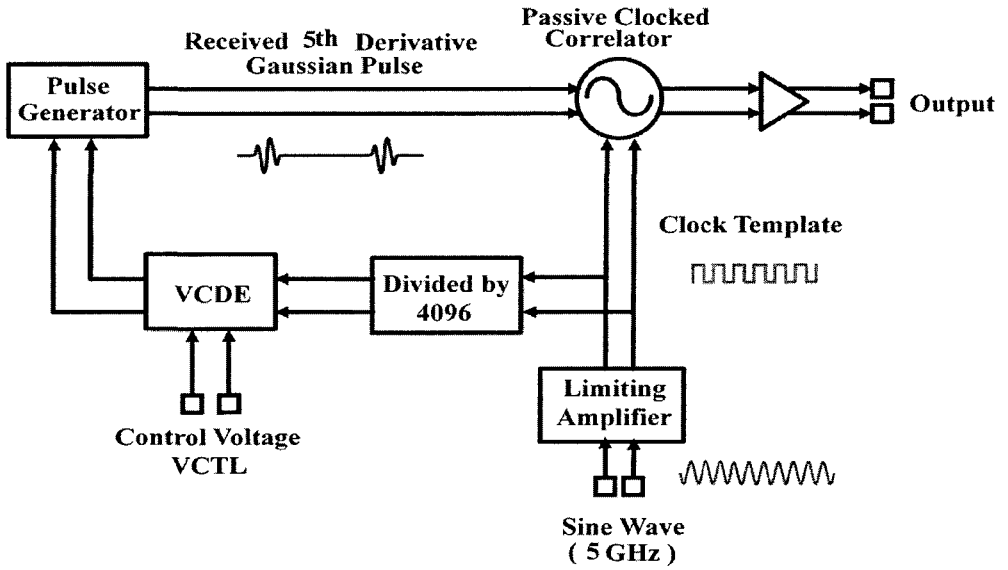


Figure 3-2 Analog Test Bench Design for Passive Correlation with Clock Template

This test is designed specifically for passive correlator in order to find out the correlation between the received UWB pulse and a clock template signal.

Since one signal was generated from another signal, a timing relationship could be developed between these two signals.

In this test bench, an incoming 5^{th} derivative Gaussian pulse has a pulse width of 0.4ns (includes 2 quasi-sine waves). A 5GHz clock signal is needed to match the Gaussian pulse width for maximum correlation. In the designed test, a 5GHz sine wave signal is fed into a limiting amplifier where it is converted to differential clock templates from a single-ended sine wave. These are the LO clock templates to be correlated with the incoming pulses.

The 5GHz template clock is then converted down to a slower clock at Pulse Repetition Rate 1.22 MHz (5GHz / 2^{10}(1024) = 1.22 MHz). After certain delay through the variable delay block which is controlled by voltage VTCL, this slower clock triggers the pulse generator. These triggered 5^{th} derivative Gaussian pulses become the low data rate incoming pulses.

As we can see, the same 5GHz sine wave signal generates both differential clock templates and the received low data rate 5^{th} derivative Gaussian pulses. Therefore, a timing relationship between them has been established. From this simplified designed test bench, the performance and effectiveness of the passive correlator can be approximately evaluated.

Next, a clocked correlator will be introduced and its operation inside of a proposed test bench will be illustrated to evaluate its performance.

3.2.2 Passive Correlator Design

A passive clocked correlator which combines a passive mixer with an integrator (from its own

parasitic capacitor) is proposed by Takahide Terada's group [21]. Beyond the power saving through the Impulse Radio intermittent operation, the lack of continuous biasing current in the passive mixer contributes to additional power reduction in the receiver. Furthermore, by combining a passive mixer with an integrator, extra power can be saved. In this architecture, the receiver consumes power only when the incoming pulse synchronizes with the local template pulse.

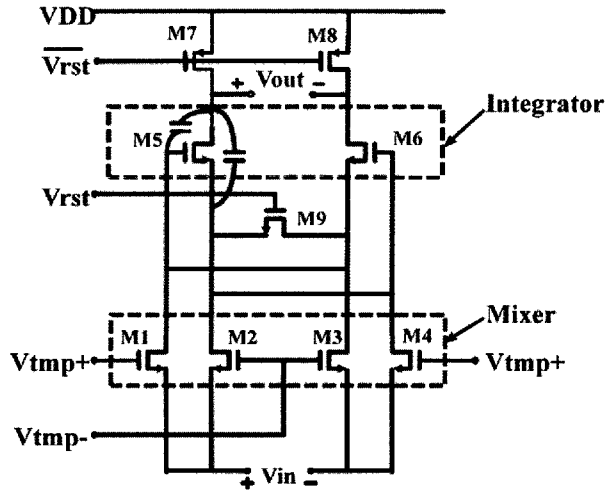


Figure 3-3 Passive Correlator

As shown in Figure 3-3, a passive mixer (M1, M2, M3, and M4) and an integrator (M5, M6) are combined together as a clocked correlator. A clock template is fed into the mixer input V_{tmp}, the received pulse signal is fed into V_{in}. Take only half circuit M1 and M2 as an example, V_{tmp} and V_{in} are multiplied in the mixer M1 and M2. The multiplied output signals are fed into the gate and source of integrator transistors M5. The maximum output is only generated when V_{tmp} and V_{in} are correlated. The large amplitude of the M1 output turns on integrators transistor M5 and the originally fully charged V_{out} node discharges through its own parasitic capacitance. As long as V_{out} is detected, $\overline{V_{rst}}$ is switched from supply voltage to ground and V_{out} is reset to supply voltage again [21]. The output of the integrated charge is sent to a comparator which determines

the threshold for maximum correlation.

To get an initial sizes for the passive mixer transistors, start with the active Gilbert Cell transistor size W= 8μm because the passive correlator cannot be designed by using the conventional circuit design methodology. Although output gain is mainly proportional to transistor channel length L, the transistor width W also has certain impact on the final output level, i.e. the output level needs to keep a relative stable level yet maintains a reasonable quick response to the input. Therefore, a range of NMOS widths are swept from 6μm to 10μm in order to find out the relationship between output voltage level (Y axis) vs. transistor width. The transient simulation results are shown in Figure 3-4. The X axis is time. The red line is for W= 6μm, blue line for 7μm, pink for 8μm and so on. For small W= 6~7μm, the output voltage declines due to the loss. For large W= 9~10μm, the output response to the input signal is too slow. Therefore, W= 8μm is a good choice of transistor width which is exactly the same size as Gilbert Quad transistors in the design for its high speed and low power attempt. Keep all the rest transistors the same width as W= 8μm.

In the passive correlator, the V_{tmp} clock signal needs to have large swing, usually full rail in order to effectively correlate the incoming pulse whose amplitude is small. Through simulation and test, the amplitude of clock template has to be more than 500mV in order to reach the desired threshold in the given amount of time. The large amplitude of clock template has some potential problems such as clock feed through introduced noise which would degrade the system performance greatly. Besides, the multiplier is no longer performing multiplication due to the nonlinearity introduced from the large clock amplitude.

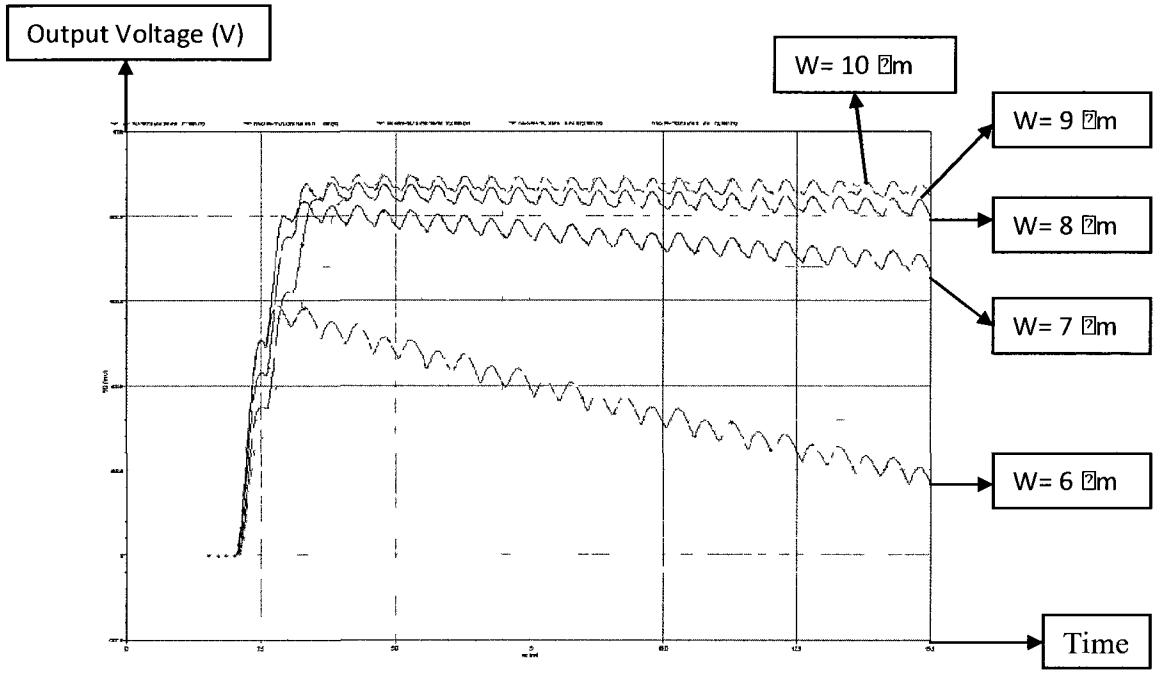


Figure 3-4 Passive Correlator Transistor Size Sweep (W=6~10um)

This clocked operation only consumes power when the input pulse is synchronized with the local template, therefore the overall power consumption can be reduced significantly, compared to a system with constant biasing current.

3.2.3 Differential 5th Gaussian Pulse Generator

Usually, differential circuits are chosen in order to reduce the effect of noise on the power supply and ground lines, while increase the signal swing. Therefore, signal-to-noise ratio has been greatly improved. This inherent error cancellation also provides better common mode rejection ration (CMRR). [27]

The 1st or 2nd derivative of a Gaussian pulse is very popular in traditional UWB pulse radio design [28] [29] [30], but its output signal needs extra filtering to satisfy the revised FCC regulation. In addition, these approaches typically consume a constant biasing power which reduces the power efficiency of the transmitter. The 5^{th} derivative of a Gaussian pulse is the most effective

pulse shape whose spectrum is within the FCC regulation without the need for constant biasing and any extra filtering [28]. The 5th derivative Gaussian pulse can be written as:

$$G_5(t) = \mathrm{A}\left(-\frac{t^5}{\sqrt{2\pi}\sigma^{11}} + \frac{10t^3}{\sqrt{2\pi}\sigma^9} - \frac{15t}{\sqrt{2\pi}\sigma^7}\right) e^{-\frac{t^2}{2\sigma^2}} \qquad \textbf{(3-1)}$$

Where A is the pulse amplitude, σ is a time constant and t is time. A and σ can be chosen to be fit with FCC power density limitation. The Gaussian pulse shape in time domain is shown in Figure 3-5 and its FCC Spectrum Mask requirement is shown in Figure 3-6.

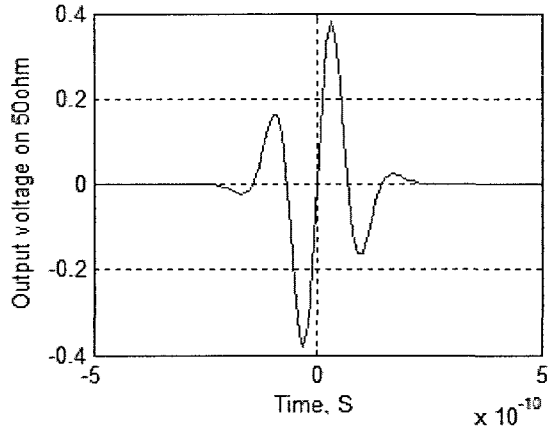


Figure 3-5 5th Derivative Gaussian Pulse

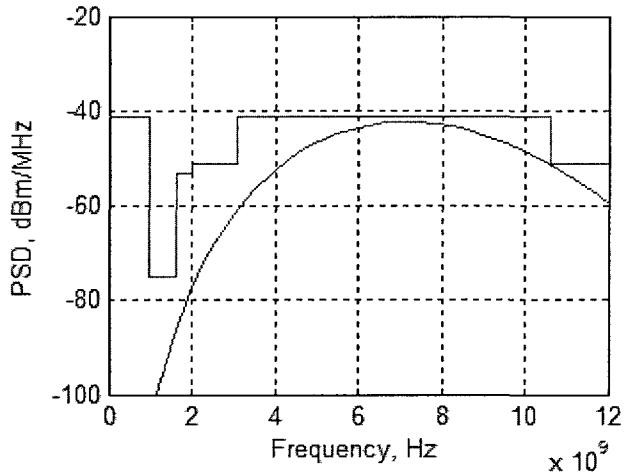


Figure 3-6 FCC Spectrum Mask

A new way of generating single-ended 5th derivative Gaussian pulse by combining four separate Gaussian pulses with specific designed amplitudes and delays [31]. Omid Salehi-Abari in our

research group built a differential pulse generator based on this method with some modification. The main motivation behind the differential pulse generator is to find an efficient way to drive a differential on-chip antenna. Integrating antenna onto a chip can improve the overall system performance by eliminating unnecessary external components, which is more suitable for low power and low cost requirements in biomedical applications. This method eliminates the need for a differential amplifier connecting between pulse generator and on-chip antenna. Therefore, the pulse generator and the on-chip antenna can be directly connected.

The design of the differential pulse generator is shown in Appendix I

3.2.4 Differential Voltage Controlled Delay Element (VCDE)

A Differential Voltage Controlled Delay Element (VCDE) shown in Figure 3-7 is designed to manually align received pulses with local clock templates for maximum outputs. The VCDE is essential a current starved delay cell which limits the current sourcing and sinking capability of the inverter by adding a current source and current sink in series with the upper PMOS and lower NMOS of the inverter cell. Transistor M2 and M3 together operate as an inverter, while M1 is a current source and M4 is a current sink. By regulating the current available to the inverter, the time to charge or discharge the load capacitance can be changed. A large current can quickly charge the capacitor which results in a small delay.

The length and width of the inverter transistors are sized to handle the varying current with M2/M3, $W_2 = W_3 = 3$ μm, while current source transistors are minimized. Another regular delay cell made of M5 and M6 has a ratio of 2 with $W_6 = 2$ μm.

An extra 30 fF capacitor is inserted between the starved delay cell and regular inverter delay cell in order to give extra delay adjustment.

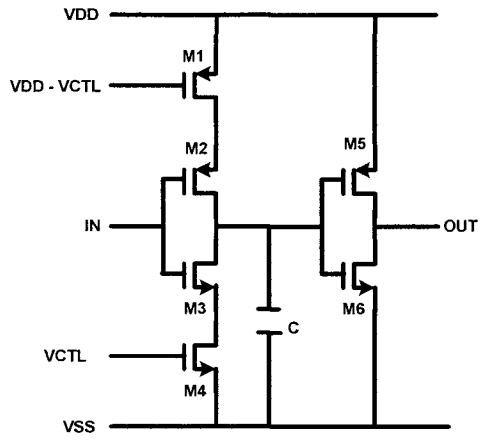


Figure 3-7 Voltage Control Delay Element (VCDE)

Part of the simulation results are shown in Figure 3-8 for VCTL range between 0.6 to 0.9 V.

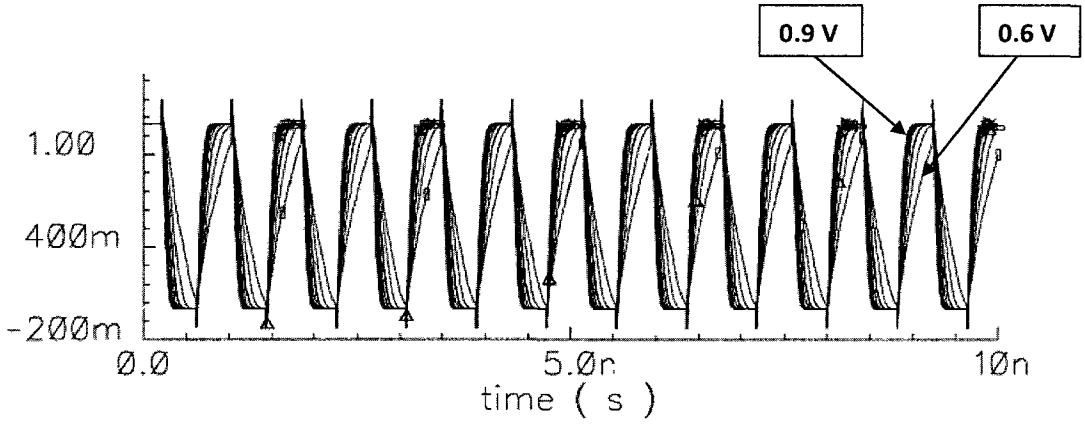


Figure 3-8 VCDE Transient Simulation

For each of such control voltage, a pulse delay is measured relative to input clock edge. The VCDE tuning range is obtained through this process where cell delay varies from 0.146 ns to 5.28 ns when the control voltage changes from 0.4V to 1.2V, the simulation results are shown in Figure 3-9.

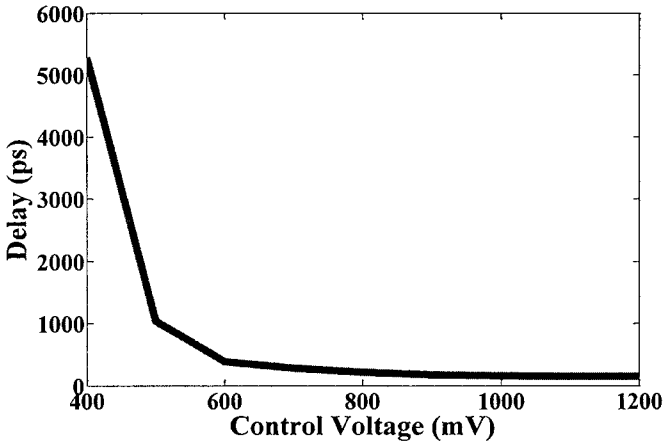


Figure 3-9 Delay Cell Tuning Range

3.2.5 Frequency Divider

Conventional frequency divider uses D-Flip Flop or Master-Slave latches as fundamental elements. Current Mode Logic (CML) is getting popular due to its supreme performance at high frequencies. As the name indicates, CML is a differential logic working in current mode. Its output cannot reach full rail-to-rail swing which makes it much faster due to quick voltage transition. Unlike the static CMOS case, CML buffers are insensitive to supply and ground bounce due to the high common-mode rejection. The load of a CML buffer is the gate capacitance of a single transistor, unlike a static CMOS gate. [32] It has relative flat power consumption curve compared to other logic styles whose power consumption increase substantially at higher frequencies. All these attributes make CML a good candidate for high speed and low power applications. [33]

A CML based D-latch is shown in Figure 3-10. There are two stages for the D-latch operation – "latch" and "hold". These two stages are controlled through differential clock inputs V_{tmp} +/- When V_{tmp} + is high, the differential pair of "latch" stage is turned on while the "hold" stage on the right is turned off. The output follows the input V_{in} as the same operation in a differential pair and the input data is "latched" onto the output. In the following hold stage, V_{temp} – becomes

high. The differential "latch" on the left is turned off and the "hold" stage on the right is turned on. Therefore, any input changes on the "latch" side would not affect the "hold" stage value. Transistor M6 and M7 are connected in a regenerative positive feedback loop, which reinforces the previous "latched" output. So between the toggle of V_{tmp} + and V_{tmp} -, input data is "latched" onto output when V_{tmp} clock is high and "hold" in D-latch when V_{tmp} clock is low.

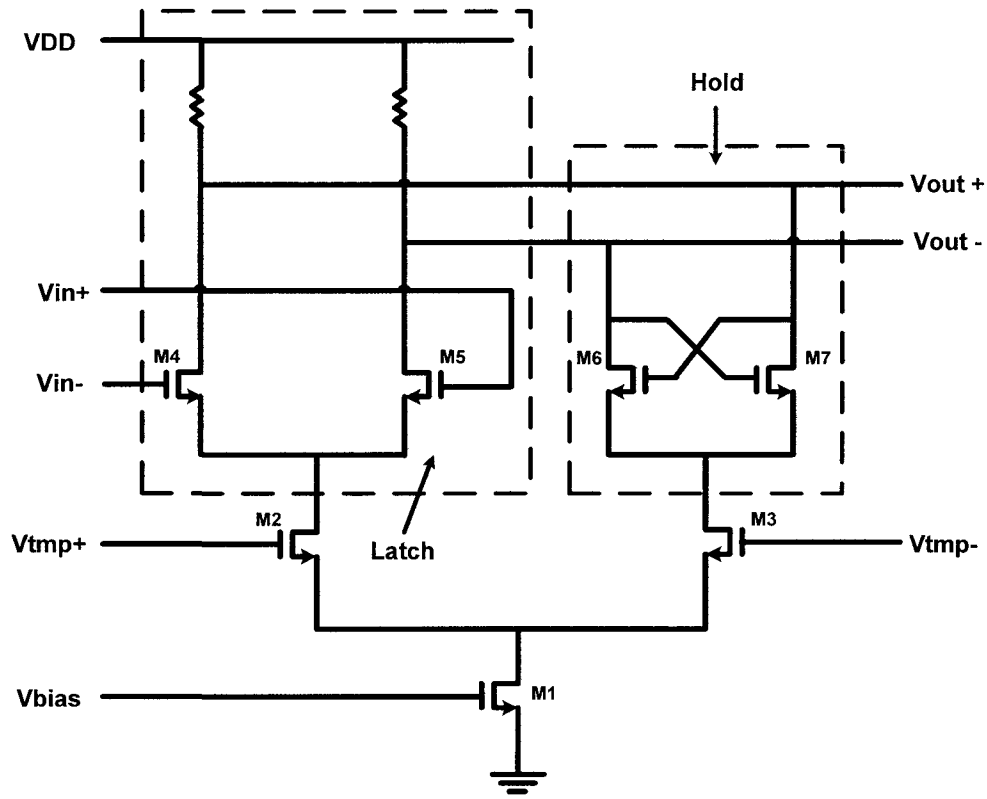


Figure 3-10 CML D-Latch [34]

Now we are going to discuss how to design the CML D-Latch in order to meet the speed and power requirement. First, let us define $V^* = 2*\frac{I_d}{g_m}$, rearrange it as

$$\frac{g_m}{I_d} = \frac{2}{V*} \qquad (3\text{-}2)$$

For long channel square law devices,

$$V_{gs} - V_{th} = V_{dsat} = V_{ov} = V^* \quad (3\text{-}3)$$

$$V_{swing} = I_{ss} * R_{load} \quad (3\text{-}4)$$

$$A_v = g_m R_{load} \quad (3\text{-}5)$$

for short channel devices, all interpretations of V^* are approximations and $V^* \neq V_{dsat}$ since square law is no longer valid due to short channel effects. However, the definition of $V^* = 2*\frac{I_d}{g_m}$ still holds and is a good estimation of V_{dsat} for 0.18 μm technology as shown in Figure 3-11.

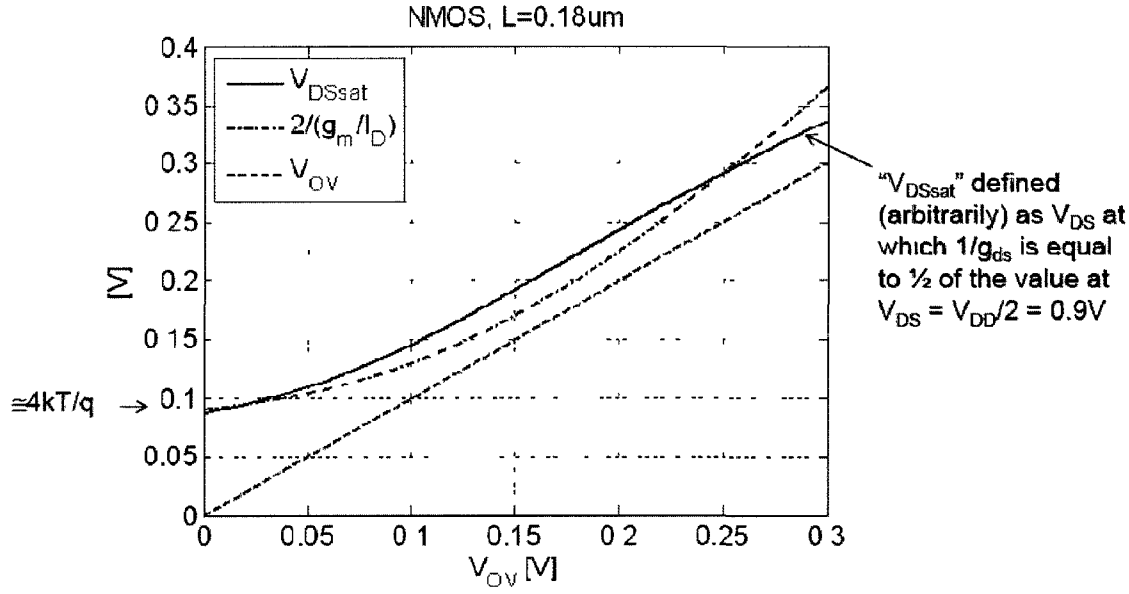


Figure 3-11 Vdsat Estimation Based on Gm/Id [35]

According to the design figure-of-merit ($f_T * \frac{g_m}{I_d}$) vs. $V^* = 2 * \frac{I_d}{g_m}$ *implies* ($V_{gs} - V_{th}$) [36] , the optimum V^* which implies overdrive ($V_{gs} - V_{th}$) is around 100mV (0.13um technology) in order to achieve maximum speed and high current efficiency as shown in Figure 3-13. In short channel devices, many second order effects such as velocity saturation, mobility degradation and threshold variation have to be taken into account, so an V^*= 200 mV is chosen to make sure transistor is in strong inversion yet maintain good linearity [37]. At V^*= 200 mV, ($f_T * \frac{g_m}{I_d}$) = 739.3 GHz/V and f_T is around 100 GHz.

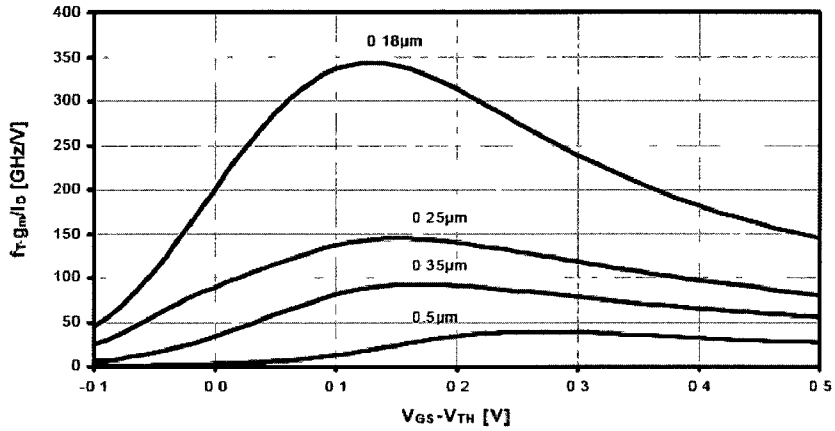


Figure 3-12 Composite Design Figure-of-Merit [35]

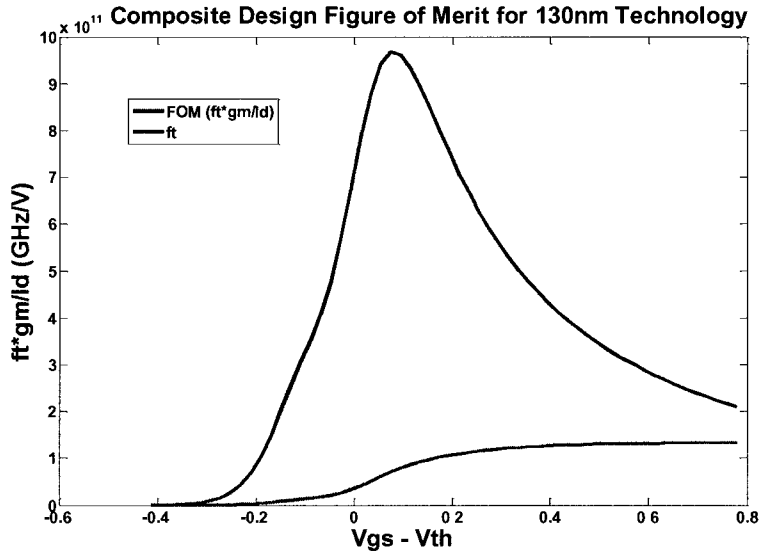


Figure 3-13 Composite Design Figure of Merit for 130nm CMOS Technology

In order to achieve fast speed, high current density is desirable in switching transistor. The load resistor needs to be chosen wisely in order to get good output voltage swing. For large output swing $V_{swing} = I_{ss} * R_{load}$, the switching transistor can fully switch the entire tail current to one side with small $\frac{W}{L}$ ratio. At the same time, a narrower transistor not only has small load capacitance but also gives higher current density, both would make circuit faster.

Choosing I_{bias} = 1mA would give good performance for three stacked transistors as shown in the example on P.267 [37]. Each transistor has 200 mV overdrive voltage V_{ov} = 200 mV as discussed.

From the relationship between $\frac{g_m}{I_d}$ and V_{ov} shown in Eqn. 3-1, the $\frac{g_m}{I_d}$ can be calculated as 10. Choose R_{load} = 600 Ω to give output swing 0.6 V from Eqn. 3-3. Choose $A_v = 2$, calculate g_m= 3.3 mA/V from Eqn. 3-4. Therefore for $\frac{g_m}{I_d}$ equals to 10, the drain current I_d = 0.33 mA for transistor M4 and M5. The current density vs. width plot is shown in Figure 3-14 for 0.13μm technology in IBM process.

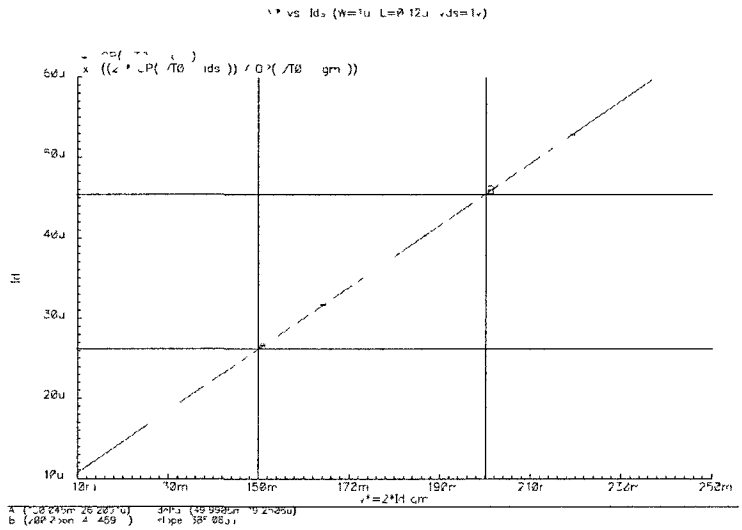


Figure 3-14 Current Density vs. V* (implies overdrive voltage)

A reference transistor $\frac{W}{L} = \frac{1\square m}{0.12\square m}$ is chosen as V_{ov} = 200 mV and V_{ds} = 1V, the unit current density is I_{ds} = 45.49 μA/μm. Therefore, for a transistor having I_d = 0.33 mA, $W_4 = W_5$ = 7.25 $\square m$. For convenience, choose $W_4 = W_5$ = 8 $\square m$. Keep the width of W_2 and W_3 same as 8 $\square m$.

However, W_6 and W_7 needs to be at least twice the size of $W_4$and W_5 so the transistors can have smaller voltage swings, therefore are easy to "latch" the previous output. Make W_4= W_5= 16μm.

For biasing transistor M_1, the length is set to be L_1= 240 μm instead of minimum length due to the channel length modulation. In this case, W_1 is sized to 16 μm.

A CML D-latch based divide-by-2 circuit is shown in Figure 3-15. Unlike Master-Slave latch based DFF, no inverters are needed in between two D-latches to toggle between "latch" and "hold" stage. Instead, V_{out} +/- are cross-coupled connected with V_{in} +/- and the two D-latches are clocked at opposite edges.

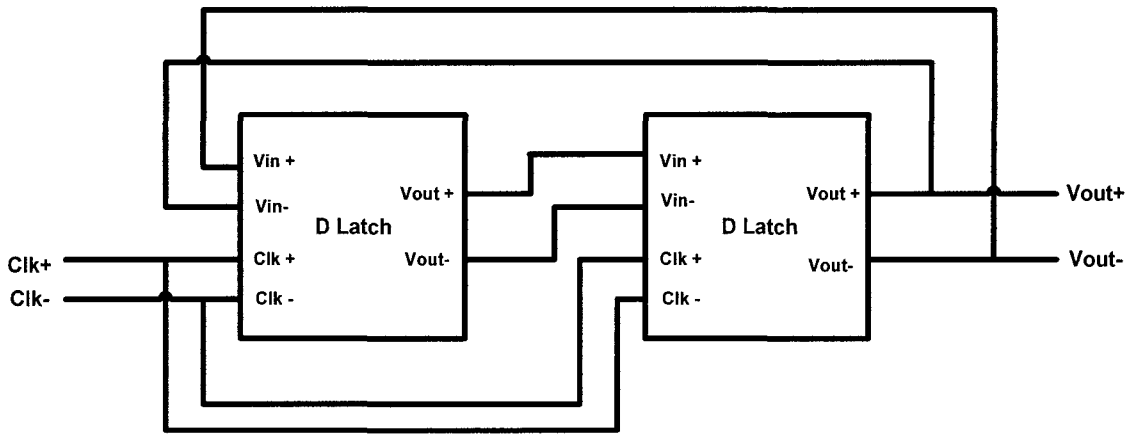


Figure 3-15 CML D-Latch based DFF

In the test bench design, the input clock needs to be down converted from 5GHz to 1.22MHz, so 10 stages (divided by 2^{10}) of divide-by-2 circuit are needed. In order to test the divider's functionality, three divider circuits are connected together to model appropriate input and output load. Figure 3-16 shows the 3-stage divide-by-2 circuit performance with differential output. The rise and fall time is 20% of the clock period 400ps. The input clock is shown at the bottom. The middle two plots are divided-by-2 and divided-by-4 wave form. The top plot is divided-by-8

waveform after 3-stage frequency dividers.

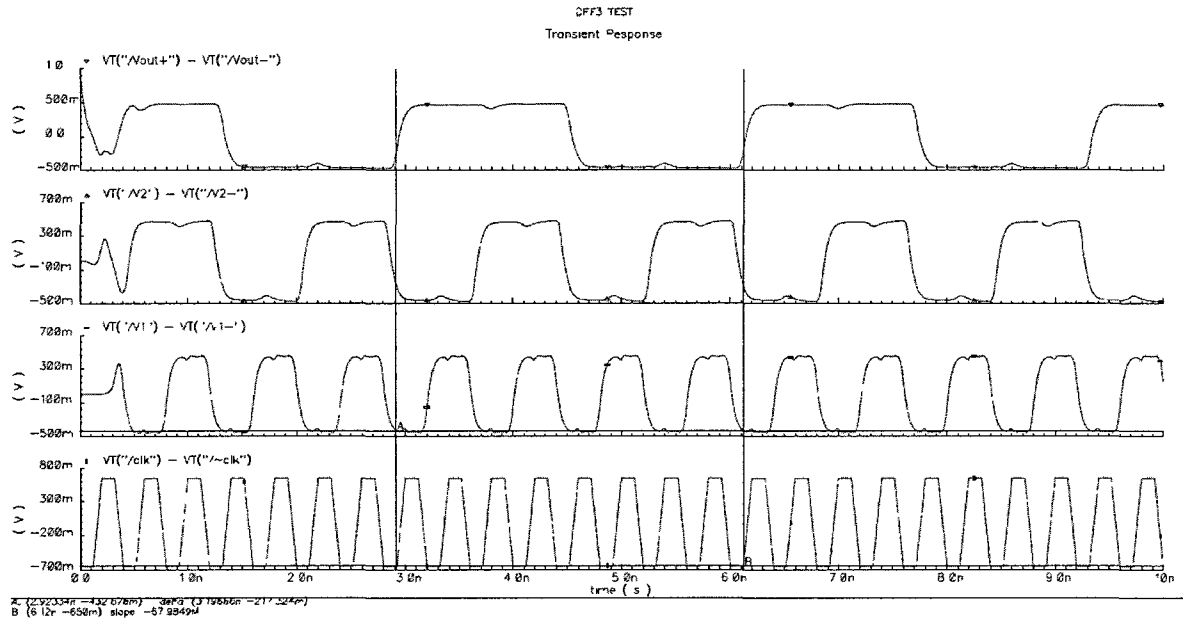


Figure 3-16 Three DFFs Test Results

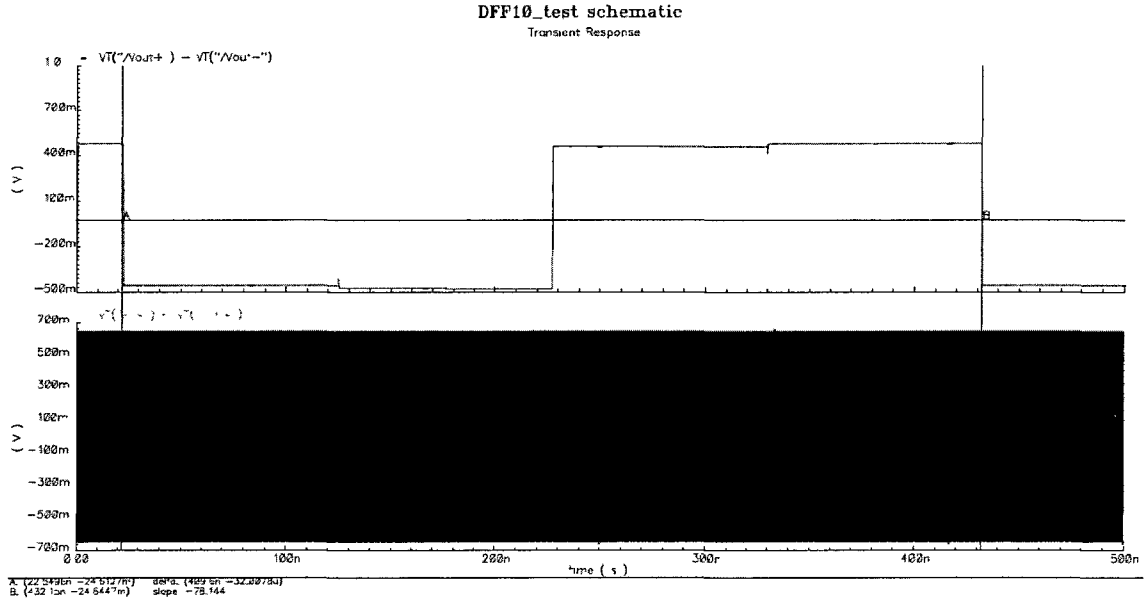


Figure 3-17 10-Stage Frequency Divider

The schematic of 10-stage frequency divider is shown Appendix II and the simulation result is in Figure 3-17. The input clock appears dark because the simulation time is relative long and clocks are "glued" to each other. The marker reader on the left bottom is 409.6ns = 0.4 ns * 2^{10} = 0.4 ns * 1024 which means the frequency divider works properly.

3.2.6 Passive Correlator Simulation

The control voltage VTCL of the variable delay cell can be carefully adjusted in order to observe the output variation due to the time shift between the clock template and the incoming Gaussian pulse. For each pulse delay, the maximum correlated output is simulated and measured after integration. The relationship between the maximum correlated output vs. pulse delay is shown in Figure 3-18. This plot is based on transient simulation, but it is not a transient plot. X Axis is not time but "pulse delay" between the received UWB pulse and clock template.

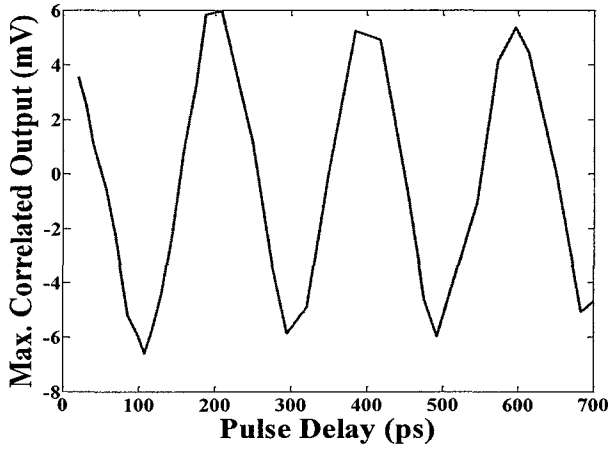


Figure 3-18 Max Correlation for Clocked Correlator

The correlated output repeats every half pulse width (0.2ns) and its output level is less than 6mV. It will be shown in Figure 4-8 of Chapter 4 that active double balanced Gilbert Cell has much

higher output level than the passive correlator, which is a good demonstration that active circuit increases the power level of output signal with extra biasing current.

3.2.7 Layout and Test chip

The test chip for the whole test bench including the passive correlator is manufactured in IBM 0.13 μm technology. It contains a 5th derivative differential Gaussian pulse generator, a passive clock correlator, limiting amplifier (converts sine wave to square clock template), voltage controlled delay elements, divide-by-1024 frequency divider and an output buffer. As shown in the pin configuration list in Table 3-1 and chip layout in Figure 3-20, the test chip contains two parts – the left part is a separate clock divider test, while the right part is the passive correlator test bench which includes the clock divider. The die photo in Figure 3-19 only shows the passive correlator test bench on the right part (on the top part in Figure 3-20)

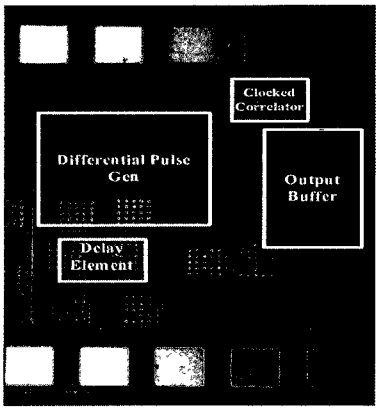


Figure 3-19 Passive Correlator Test Bench Die Photo

The test chip is designed to accommodate two 8-pin probes and one 5-pin probe. For a 8-pin probe, the pin order is P-G-S-G-S-S- G-P and P-G-S-S-G-S-G-P (P for power, G for ground, S for signal) for both sides. For a 5-pin probe, the pin order is G-S-G-S-G. The total chip size is 1mm*2mm.

Table 3-1 Clocked Correlator Test chip Pin Configuration

Pad	Type	Description
VDD	Power	1.2 V DC power supply
VSS	Ground	Ground
CLK+	Input	5GHz sine wave (+)
CLK-	Input	5GHz sine wave (-)
VCTL+	Input	Delay cell controlling voltage (+)
VCTL-	Input	Delay cell controlling voltage (-)
OUT+	Output	Correlation Output (+)
OUT-	Output	Correlation Output (-)

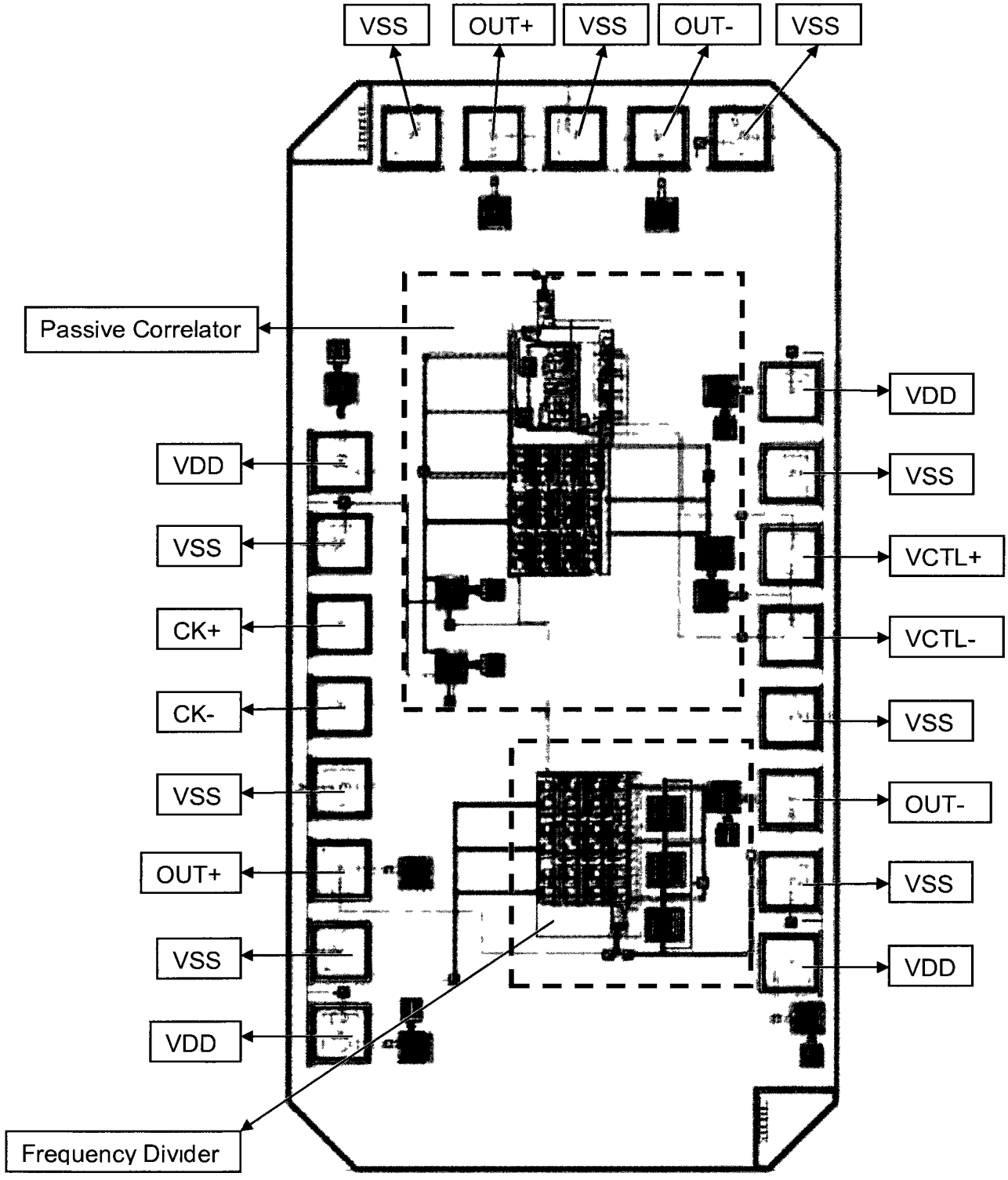


Figure 3-20 Passive Correlator Chip Layout

3.3 Correlator Analysis

3.3.1 Strength and Weakness of Passive Correlator

A passive correlator and a double balanced Gilbert Cell based active correlator are shown separately in Figure 3-21 and Figure 3-22 for comparison. These two schematics look fairly similar except the active correlator has biasing current while the passive one doesn't. The operation difference between these two passive and active circuits is the representation of RF input signal. In passive circuit, RF input is represented directly as voltage, while in active circuit RF input is in the format of current which is converted from voltage input.

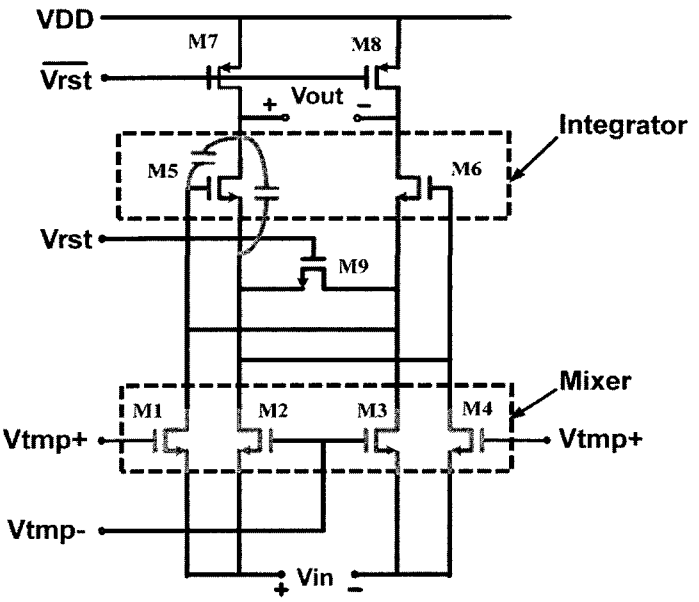


Figure 3-21 Passive Correlator

The main motivation behind the passive correlator is its low power consumption and easy local clock template generation. However, the lack of gain and undesirable nonlinear products at the output nodes becomes its drawbacks [38]. The square wave clock gives even smaller conversion gain $2/\pi$ than $\pi/4$ driven by sinusoidal wave. The input and output nonlinearities are subject to

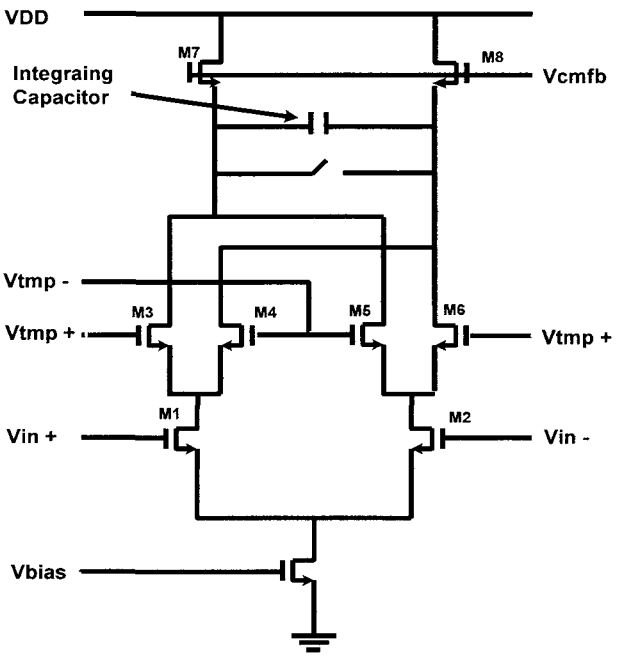


Figure 3-22 Gilbert Cell Based Active Correlator [16]

filtering and termination. In most cases, the loading capacitor at the output nodes can be used to form a low pass filter to remove the undesirable mixing components at different frequencies.

In the passive correlator shown in Figure 3-21, the mixer is made of four transistors M1 through M4 and it is the conventional switching mixer for narrow band frequency generation. V_{in} is biased to ground and there is no voltage biasing at the mixer gate. So the amplitude of V_{tmp} needs to be high enough to turn on the mixer transistor first and then multiply with V_{in}. With such high input amplitude, not only does the desired input signal get into the mixer, but also interferences from adjacent bands feed through its parasitic capacitor. Furthermore, the mixer does not perform the same function as an analog multiplier, which is going to be discussed intensively in Chapter 4.

Although the passive correlator can perform the multiplication function, due to the reasons mentioned before i.e. large amplitude of V_{in} and nonlinearity at LO port which both generates unwanted noise and interference, the overall system noise figure is degraded due to the switching activity. This is a very important issue especially in the UWB Impulse Radio system where signal level is exceedingly low and comparable to the noise level. Therefore, an analog multiplier with both linear input ports is crucial for the correlator design.

3.3.2 Interpretation of Analog Correlation

Mixing is the multiplication between two signals to achieve frequency translation. Suppose $V_x = A_{RF} * sin(\omega_{RF}t)$, $V_y = B_{LO} * sin(\omega_{LO}t)$. A_{RF} and B_{LO} is the magnitude for RF and LO signals. ω_{RF} and ω_{LO} are the RF and LO frequency.

$$V_{IF} = \frac{A_{RF}B_{LO}}{2V_u} * \boldsymbol{sin(\omega_{RF}t) * sin(\omega_{LO}t)}$$

$$= \frac{A_{RF}B_{LO}}{2V_u} * [\boldsymbol{cos(\omega_{RF}t + \omega_{LO}t) + cos(\omega_{RF}t - \omega_{LO}t)}] \qquad \textbf{(3-6)}$$

However, analog multiplier responds linearly from both inputs and provides features rarely found in mixer and linear products usually are not required in frequency translation [39]. The bilinear response leads to much higher noise level than that allowable in a mixer. The $sin(\omega_{RF}t) * sin(\omega_{LO}t)$ is rarely needed because the linearity at LO port and the use of sinusoidal wave as LO carrier do not provide extra benefits in frequency translation. So $(+/-1) * sin(\omega_{RF}t)$ can be used to provide higher conversion gain.

In the ideal case of correlation based demodulation, assume each user is represented as $\varphi_n(t)$ in the communication channel, n = 1, 2, 3…N. No additive noise and RF and LO signals are both linear input ports. The $\varphi_n(t)$ signal has the following orthogonal features:

$$\int_0^T \varphi_n(t) * \varphi_m(t)dt = constant, \quad n = m \tag{3-7}$$

$$\int_0^T \varphi_n(t) * \varphi_m(t)dt = 0, \quad n \neq m \tag{3-8}$$

The received signals can be expressed as $r_m(t) = \varphi_n(t) + n(t)$, where $m = 1, 2, \ldots N$ and $n(t)$ is the channel additive noise. $N_m(t)$ are random variables associated with the presence of the channel additive noises.

$$\int_0^T r_n(t) * \varphi_m(t)dt = constant + N_m \quad n = m \tag{3-9}$$

$$\int_0^T r_n(t) * \varphi_m(t)dt = N_m \quad n \neq m \tag{3-10}$$

If RF and LO are both linear at input ports, the correlation output contains only the desirable user information and channel noise as shown in previous equations. Those unwanted interference can be removed, therefore the SNR at the output is maximized. However, if the square wave LO signal is used, unwanted interference generated in the switching mixer would increase output noise level which degrades the SNR at the output [40]. This will be discussed in the following noise section.

3.3.3 Power Consumption

The total power consumed by the correlator consists of two parts - static power and dynamic power shown in Eqn. 3-11,

$$P_{total} = P_{static} + P_{dynamic} \tag{3-11}$$

Since there is no current biasing in the passive correlator, theoretically the static power consumption is very low due to second order effects such as subthreshold leakage and tunneling currents etc. The static power consumption simulation setup is shown in Figure 3-23.

The current drawn from VDD in simulation for the passive correlator is 2*1.317 uA = 2.634 uA, so P_{static} = 3.16 uW.

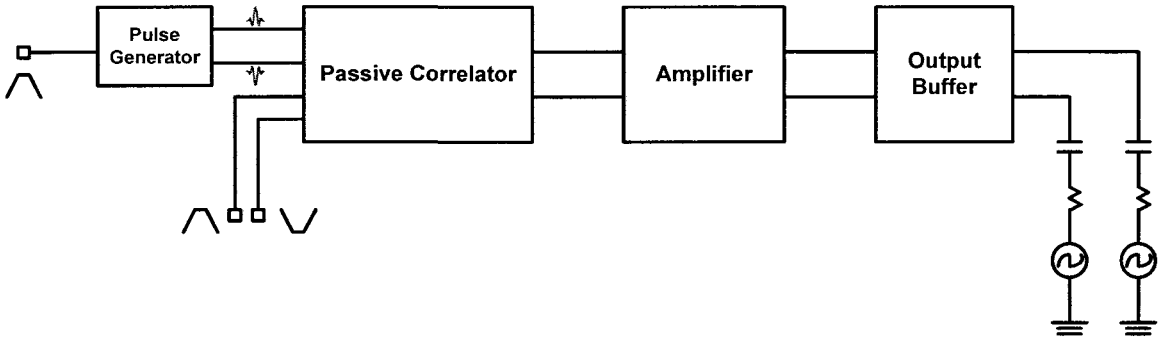


Figure 3-23 Passive Correlator Static Power Consumption Simulation Setup

The passive correlator exploits the amount of charge stored on a parasitic capacitor to detect the maximum correlation, so dynamic power consumption exists depending on capacitor switching frequency.

$$P_{dynamic} = CV_{DD}{}^2 f \qquad (3\text{-}12)$$

The total $C_{pmos} = 317fF$ for PMOS and $C_{nmos} = 330fF$, so the total capacitance at output is 647 fF. The system has a low data rate 1.22 MHz which gives dynamic power $P_{dynamic}$ of 1.12 uW. $P_{total} = 3.16\,uW + 1.12\,uW = 4.28\,uW$.

3.4 Passive Correlator Summary

A passive correlator is able to correlate with either a sinusoidal wave or a clock template. In the sinusoidal wave case, correlator consumes more power because sine wave turns on both differential transistors at the same time for a short period, which results in higher power dissipation. However, clock template has sharper rising and falling edges would not turn on differential transistors at the same time, or for a very limited time shorter than sine wave does. This behavior could reduce circuit power consumption. Besides, circuit only consumes power (not including the biasing and other assistive circuits) when the input pulse is correlated (synchronized or not

perfectly synchronized) with local template, therefore the overall power consumption can be reduced significantly.

The chapter first introduces the analog correlation concept prototype before presenting a test bench to evaluate a passive clocked correlator consists of a multiplier and an integrator. Individual components inside of the test bench, such as the passive correlator, the limiting amplifier, differential 5^{th} derivative pulse generator, differential voltage controlled delay element (VCDE) and frequency divider have been designed and analyzed.

In the test bench simulation, the control voltage VCTL of VCDE can be carefully adjusted in order to observe output variations due to time shift between clock template and received pulse. The correlated output repeats every half pulse width and its output level is less than 6mV due to the nature of passive circuit.

Power reduction and easy local clock template generation are the main motivations behind this architecture. The total power consumed in the passive correlator is only $4.28\ uW$. But the large amplitude of V_{in} required to switch on the LO transistors generates unwanted noise and interference, the overall system noise figure is degraded due to the switching activity. The passive correlator NF has not been simulated due to the difficult sampling mechanism setup, but it is estimated higher than the active correlator (see next chapter) due to the requirement of the large amplitude of the clock template input.

In the correlator analysis section, the strength and weakness of the passive clocked correlator is discussed first. The major disadvantage is the requirement for large amplitudeV_{in}. The induced noise and interference have relatively large impact on the IR-UWB system because the impulse signal is spread over a large bandwidth and comparable to noise level. Following that, a discus-

sion between the mixer and analog multiplier is presented and becomes the main contribution of this thesis. The differences between these two components are specifically discussed for the signal correlation in communication channel and this becomes the starting point of future analog correlator design.

The switching mixer based passive clocked correlator does not provide good performance, instead an analog multiplier with good linearity at both RF and LO ports are needed, which is going to be discussed intensively in the next chapter.

Chapter 4

Active Analog Correlation

In Chapter 3, a passive clocked correlator is introduced and its performance has been evaluated with the advantages and disadvantages being presented. Simulation results show that passive clocked correlator has small conversion gain, which is not desirable for signal detection after integration. An active correlator with good conversion gain, higher linearity and wide bandwidth is highly needed.

A low power highly linear analog multiplier to be used as part of analog correlator is difficult to design for UWB Impulse Radio. The original bipolar double balanced Gilbert Cell is usually a good starting point for analog multiplication due to its wide dynamic range and good high frequency performance. With the evolution of CMOS technology and increased integration capability, CMOS Gilbert Cell becomes the mainstream in circuit design.

In this chapter, a double balanced Gilbert Cell based correlator will be introduced. The Gilbert Cell analog multiplication in strong inversion, square law region (long channel device) has simple and elegant linear relationship between two input voltages and output current with limited range. Furthermore, short channel effects, such as velocity saturation and mobility degradation, on the analog multiplication for device length smaller than 1μm will be explored to address these important design issues.

Besides the discussion about the analog multiplication in long and short devices, a specific test bench is designed to test the correlation between the incoming 5^{th} Gaussian pulses with three different local templates, namely a sine wave, a clock and a 5^{th} Gaussian pulse. The difference be-

tween simulation value and measurement data prompts an important design issue – common mode and DC offset compensation and circuit calibration in any future design endeavor.

4.1 Introduction to Double Balanced Gilbert Cell

The double balanced Gilbert Cell was introduced by Barrie Gilbert in his pioneering work, "A precise four-quadrant multiplier with sub nanosecond response", published on IEEE Journal of Solid State Circuit (JSSC) in 1968. "His work showed that the dependability of a bipolar transistor's nonlinearity can be exploited to realize exceptionally linear systems and nonlinear elements can be used to create a rich variety of linear systems.", as commented by Thomas Lee in the Solid State Circuit News of Fall 2007 after 40 years of this counterintuitive work.

The double balanced Gilbert Cell consists of two single balanced differential pairs connected in cross-coupled fashion as shown in Figure 4-1. It is a current mode multiplier. Transistor M1 is the current source which supplies current to the two differential pairs. M2 and M3 are V-I G_m cell and M4/M5 and M6/M7 are also called "Gilbert Quad" which alternately switches all the tail current from one side to the other side if it works as mixer/modulator, or it multiplies with input voltage V_y if it works as an analog multiplier. A linear transconductance over a wide dynamic range is the main focus of the double balanced Gilbert Cell analog multiplier design.

4.1.1 Gilbert Cell Three Different Functions

Before the introduction of analog multiplication function, two other different usages – as mixer/modulator and phase detector, of CMOS double balanced Gilbert Cell will be discussed first. Although "Gilbert Cell" has been mentioned quite often in design, its working mechanism as a modulator and phase detector are seldom discussed. By comparing these different functions, specific requirements for precise analog multiplication are clearly illustrated in circuit design.

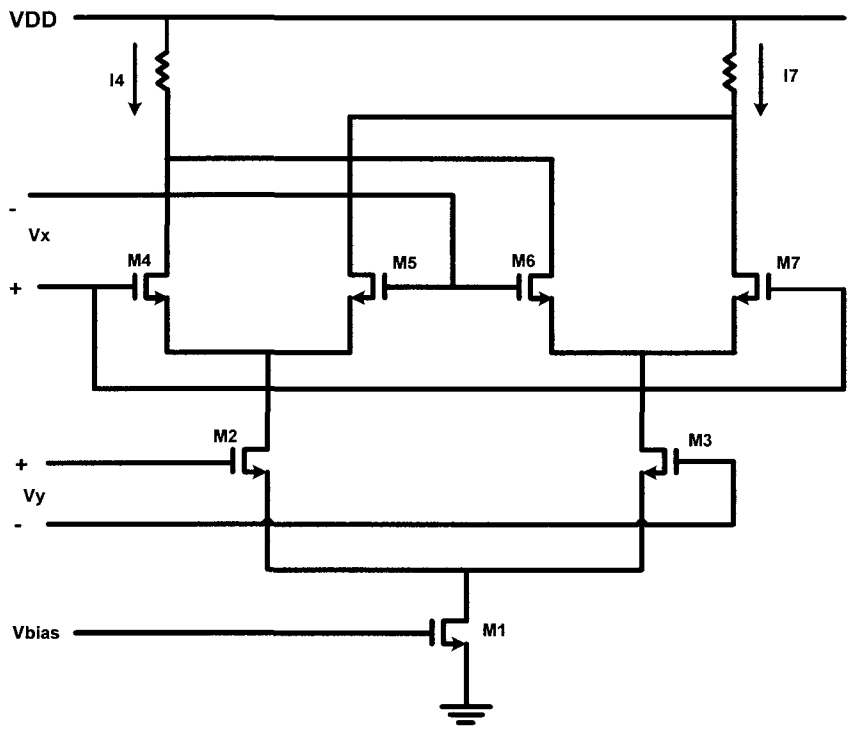


Figure 4-1 CMOS Double Balanaced Gilbert Cell

4.1.1.1 As Mixer/Modulator

Gilbert Cell has been used as mixer and modulator for frequency translation. In the ISSCC 2000 lecture, Barrie Gilbert defined the "active mixer" as "any mixer which is powered by more than the LO drive signal and uses devices in amplification modes so as to provide considerable conversion gain as well as very low noise and high overall linearity". It exploits the nonlinear functionality of Gilbert Cell to generate new frequencies at the sum and difference of two input frequencies. This operation can be divided into two parts – V-I converter (M3 and M4) and Gilbert Quad (M5 through M7) current switching. M3 and M4 are voltage-current converters which require linear transconductance.

By definition, modulation usually refers to the use of a high level mixer which imposes baseband digital signals in communication system on either an IF or RF carrier [39]. In the modulator case,

V_x (also called LO signal in mixer) needs to be much larger than V_{gs} - V_{th} so that the two differential pairs (M4 through M7) can be alternately turned on and off, behaving like a switch rather than a linear device.

In real cases, the LO signal is typically several times larger than V_{gs} - V_{th} so that the Gilbert Quad alternately turns completely off and on from both sides. Since the LO signal level is proportional to $\frac{I_{bias}}{g_m}$ [37], its switching level can be lowered to a few hundred mV by increasing the switching transistor size. However, large transistor size means lower current density which has lower f_t. At the same time, a wider transistor means bigger coupling capacitance which induces higher clock feed through. In situation where the f_t is not very important, the LO switching level has to be traded off with appropriate transistor size during design. The output is actually the multiplication of small signal input and a square wave.

4.1.1.2 As Phase Detector

Another application of Gilbert Cell is working as a phase detector. Unlike frequency translation where two different frequency signals are multiplied, phase detector inputs take two identical input signals $Acos\omega t$ and $Bcos(\omega t + \varphi)$. Both inputs V_1 and V_2 have big amplitudes and Gilbert Cell circuit simply switches from one state to the other, behaving like non-saturated switches. In phase detector operation, only the DC term ($\frac{AB}{2} * cos\varphi$) is of interest and this term which is proportional to the phase difference between the two inputs. [41]

4.1.1.3 As Analog Multiplier

The third application of Gilbert Cell is also the focus of this thesis - analog multiplier. The output voltage (output current multiplies with load resistor) is expected to be proportional to the multiplication of two inputs V_x and V_y. In a bipolar transistor, this multiplication relies on the exponen-

tial I-V relationship, while in CMOS long channel devices, the multiplication depends on the square law I-V transfer function. In this mode, the input signals have to be in a small linear range to implement the multiplication function. This is because higher order of harmonics and polynomials from nonlinear CMOS transistors need to be canceled before the linear function can be achieved. This makes the double balanced Gilbert Cell very popular due to its nonlinearity cancellation capability from its differential structure.

The double balanced Gilbert Cell shown in Figure 4-1 depends strongly on the signal path properties and application requirements such as swing linearity and bandwidth [35]. Figure 4-1 shows that analog multiplication is mainly a large signal operation. The lower part of V-I transconductors convert input voltage into current as small signal processing, while upper Gilbert Quad switch current as large signal processing.

For modulator operation, the output amplitude is actually independent of the amplitude of the square wave input as long as it is high enough to turn on/off the transistor completely. This circuit doesn't perform a linear multiplication, but only cause the output voltage being multiplied by +1 and -1 alternately with small signal input. Table 4-1 is the summary between these two different operations from signal path point of view.

Although short channel effects may greatly influence the circuit performance for device length smaller than 1μm, long channel devices is our initial focus due to its simple and illustrative characteristics. Second order short channel effects will be addressed afterwards.

Table 4-1 Four Quadrant Gilbert Cell Signal Path [35]

Examples	V1 path	V2 path	Intended Function
Mixer/Modulator	Small signal	Large signal	Frequency translation
Four-quadrant multiplier	Large signal High precision	Large signal High precision	Precise analog multiplication

4.1.2 CMOS Long Channel Double Balanced Gilbert Cell

Bipolar double balanced Gilbert Cell is generally the starting point for analog signal multiplication due to its wide dynamic range, high speed and good high frequency response. The four-quadrant Gilbert Cell multiplier containing a double balanced differential pair has been widely used in high frequency applications. It can achieve high linearity and better noise rejection from the inputs, power supplies and other clock feed through charges [42]. Furthermore, a fully differential structure provides better digital noise immunity on the chip with both analog and digital circuits. [43].

Due to continuous technology scaling and integration convenience, most systems exploit digital signal processing rather than analog signal processing. Biomedical circuits and systems are one area where analog signal processing remains an active research topic because analog preprocessing before digitization is important in lowering overall system power [44]. CMOS double balanced Gilbert Cell is one of the fundamental building blocks in this area.

Depending on different working regions, CMOS multiplier can operate in strong inversion and weak inversion. In weak inversion case, I-V characteristic of MOSFET is more like bipolar exponential relationship. Circuits consume very little power with reduced speed and dynamic range [45]. In strong inversion case, the square law I-V relationship $I_d = k * (V_{gs} - V_{th})^2$ generally ap-

plies in long channel device ≫ 1μm. In the following discussion, the long channel based Gilbert Cell will be introduced and the short channel based device will follow for continuous development. For 130nm CMOS technology, it falls into the short channel device and second order effects will be discussed extensively.

Before discussing the double balanced Gilbert Cell, consider a single differential pair working in strong inversion region first, shown in Figure 4-2. Assuming M1 and M2 are identical and their individual current are I_1 and I_2 as shown below. V_1 is differential input voltage, I_{SS} is the tail current, $k = \frac{\mu C_{ox}}{2} * \frac{W}{L}$ is the transconductor parameter for the input devices.

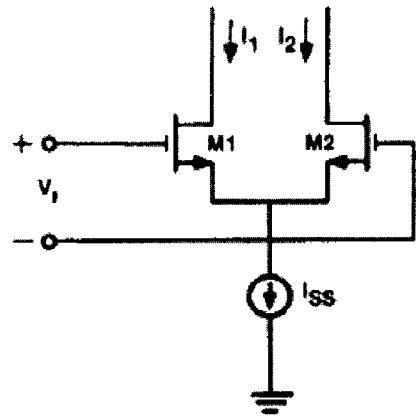


Figure 4-2 Differential Pair

$$I_1 + I_2 = I_{ss} \qquad \textbf{(4-1)}$$

$$V_{gs1} - V_{gs2} = V_{in} \qquad \textbf{(4-2)}$$

Insert the relationship Eqn. 4-2 into expanded current Eqn. 4-1. I_1 and I_2 can be expressed in terms of input voltage like

$$I_1 = \frac{k}{2} * \left(\sqrt{\frac{I_{SS}}{k} - \frac{V_{in}^2}{2}} + \frac{V_{in}}{\sqrt{2}}\right)^2 \qquad \textbf{(4-3) [46]}$$

$$I_2 = \frac{k}{2} * \left(\sqrt{\frac{I_{SS}}{k} - \frac{V_{in}^2}{2}} - \frac{V_{in}}{\sqrt{2}}\right)^2 \qquad \textbf{(4-4) [46]}$$

The differential output current is:

$$I_{od} = I_1 - I_2 = kV_{in}\sqrt{\frac{2*I_{SS}}{k} - V_{in}^2} \qquad \textbf{(4-5)}$$

This expression is only valid within limited input range, shown in Figure 4-3.

$$-\sqrt{\frac{I_{SS}}{k}} \leq V_{in} \leq \sqrt{\frac{I_{SS}}{k}}$$

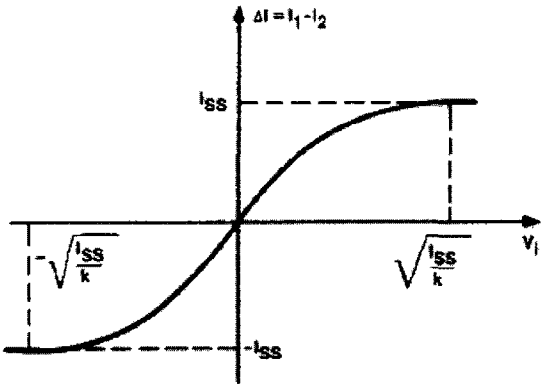


Figure 4-3 CMOS Gilbert Cell Linear Region [46]

In analog multiplier, linear multiplication is expected as $Z = \alpha * V_x * V_y$, α is multiplication gain, V_x and V_y are differential inputs. The double balanced Gilbert Cell shown in Figure 4-1 contains two differential pairs like that in Figure 4-2. For input voltage V_x within the operating range shown in Figure 4-3, drain current is related to V_x through biasing current of input transistors M3 and M4, as shown in Eqn. 4-3. This biasing current is in turn controlled by another input voltage V_y. Therefore, the final output current I_o shows relationship between both V_x and V_y, shown in Eqn. 4-6.

$$I_o = I_{o1} - I_{o2} = I_7 - I_8 = (I_3 + I_5) - (I_4 + I_6) = (I_3 - I_4) - (I_6 - I_5)$$

$$\cong kV_x\{\sqrt{(\frac{I_{SS}}{k}-\frac{{V_Y}^2}{2}+\frac{V_Y}{\sqrt{2}})^2}-\sqrt{(\frac{I_{SS}}{k}-\frac{{V_Y}^2}{2}-\frac{V_Y}{\sqrt{2}})^2}\}$$ **(assuming V_x and V_y small)**

$$=\sqrt{2}kV_xV_y \qquad \textbf{(4-6) [46]}$$

In the analog multiplication, only linear relationship is desirable by assuming V_x and V_y small, while higher order of nonlinearities and distortion should be cancelled and compensated. In this process, even order nonlinearity components are canceled through differential structure so that double balanced Gilbert Cell has larger input range than single differential pair shown in Figure 4-2. However, the linear region is still limited in the middle range around the origin. The multiplication operation needs to be performed very carefully within the suggested operating range.

4.1.3 CMOS Short Channel Effects on Double Balanced Gilbert Cell

The above analysis is based on the assumption that CMOS transistor is long channel device and I-V square law is valid in strong inversion. However, long channel assumption no long holds for 0.13um CMOS technology. Significant short channel effects become important at channel lengths of about 1um or less and MOSFET models should be modified accordingly. [41]

For devices smaller than 1μm, short channel effects such as velocity saturation, mobility degradation should be considered in the design process. Contrary to a long channel MOSFET, the short channel I-V relationship becomes rather linear than square law device, especially for higher drain current. For high $V_{gs}-V_{th}$, short channel effects tend to linearize the device, while for low $V_{gs}-V_{th}$, device does not exhibit strong short channel effects [47].

By considering velocity saturation in the horizontal field and mobility degradation from the vertical field, the I-V transfer function for drain current becomes:

$$I_{ds} = \frac{K*(V_{gs}-V_{th})^2}{1+\theta(V_{gs}-V_{th})} \qquad K = \mu_n C_{ox}\frac{W}{L}\text{ , where } \theta * L = \frac{1}{E_c} \qquad \text{(4-7)}$$

Parameter K depends on CMOS technology and size (W and L) of the device. Parameter models to the first order of source series resistance, mobility degradation due to vertical field, and velocity saturation due to the lateral field in short-channel devices. It depends on the channel length and is independent of the body effect. [47] For 0.13um technology, $\theta L \cong 0.2$ μm/V, so $\theta \cong 1.6$ V^{-1}. The large signal I-V relationship in single differential pair is:

$$I_o = \frac{K_1*(V_{gs1}-V_{th})^2}{1+\theta(V_{gs1}-V_{th})} - \frac{K_2*(V_{gs2}-V_{th})^2}{1+\theta(V_{gs2}-V_{th})} \qquad \text{(4-8)}$$

$$V_{gs1} - V_{gs2} = V_{in} \qquad \text{(4-9)}$$

$$I_{ss} = \frac{K_1*(V_{gs1}-V_{th})^2}{1+\theta(V_{gs1}-V_{th})} + \frac{K_2*(V_{gs2}-V_{th})^2}{1+\theta(V_{gs2}-V_{th})} \qquad \text{(4-10)}$$

For computation convenience, redefine U and J_{ds}

$$\text{Set } U = \theta(V_{gs}-V_{th}),\ I_{ds} = \frac{K_1 * U^2}{\theta^2(1+U)}$$

$$\text{Set } J_{ds} = \frac{\theta^2}{K_1} * I_{ds}\ ,\ J_{ds} = \frac{U^2}{(1+U)} \qquad \text{(4-11)} \quad [48]$$

Plug equation 4-7 into equation 4-9, 4-10 and 4-11

$$J_{bias} = \frac{{U_1}^2}{(1+U_1)} + \frac{{U_2}^2}{(1+U_2)} \qquad \text{(4-12)}$$

$$\theta V_{in} = U_1 - U_2 \qquad \text{(4-13)}$$

$$J_o = \frac{{U_1}^2}{(1+U_1)} - \frac{{U_2}^2}{(1+U_2)} \qquad \text{(4-14)}$$

Output current I_o can be solved through iteration:

$$I_o = I_1 - I_2 = kV_{in}\sqrt{\frac{2I_{ss}}{k} - {V_{in}}^2} - k\theta V_{in}(\frac{I_{ss}}{k} - {V_{in}}^2) \qquad \text{(4-15)}$$

Compared to its counterpart in long channel, which is shown in Eqn. 4-5, the only difference is extra term $-k\theta V_{in}(\frac{I_{ss}}{k} - {V_{in}}^2)$ due to second order short channel effects. This additional term

reduces the output current by $k\theta V_{in}(\frac{I_{ss}}{k} - {V_{in}}^2)$ which is not desirable outcome when transistor gets smaller.

The I-V relationship is the same for upper part four Gilbert Quad transistors M5/M6 and M7/M8, shown in Figure 4-4. For lower part V-I convert M3/M4 transistors,

$$J_{ss} = \frac{{U_3}^2}{(1+U_3)} = \frac{{U_4}^2}{(1+U_4)} \qquad (4\text{-}16)$$

$$\theta V_y = U_3 - U_4 \qquad (4\text{-}17)$$

$I_o = I_{o1} - I_{o2} = (I_5 + I_7) - (I_6 + I_8) = (I_5 - I_6) - (I_8 - I_7)$ would have an additional term due to $-k\theta V_{in}(\frac{I_{ss}}{k} - {V_{in}}^2)$. If V_x and V_y are made small, after certain mathematic manipulation,

$$I_o = I_{o1} - I_{o2} = \sqrt{2}\, k\, V_x V_y + k\theta V_x {V_y}^2 \qquad (4\text{-}18)$$

Compare to long channel device output current shown in Eqn. 4-6, short channel device has higher output current due to degraded third order distortion term $k\theta V_x {V_y}^2$, while the even order nonlinearities have been canceled through its differential structure.

In the calculation of differential I_o shown in Eqn. 4-17, no specific V_{gs} is needed for both differential transistors. The Gilbert Quad is independent of V_{gs}, therefore, is independent of body effect and common mode signal to the first order.

Without compensation and calibration, the input V_y has limited operating range from $\sqrt{\frac{I_{SS}}{k}} \leq V_{in} \leq \sqrt{\frac{I_{SS}}{k}}$. The output can be linearized by either having small input voltage V_y or large biasing current I_{ss}, or choosing a small k which makes the input devices M2 and M3 in Figure 4-1 long and narrow. [46]

All the methods mentioned above could only extend the linearity for certain range. For a wide dynamic range in analog multiplication, extra circuitry is needed to extend the linearity and compensate the nonlinearity distortion and offset, especially in devices smaller than $1um$.

4.1.4 Aanlog Mulitplier Design in Active Correlator

The active correlator is based on a traditional double balanced Gilbert Cell. The differential pair has their own current biasing with equal value. Its schematic is shown in Figure 4-4.

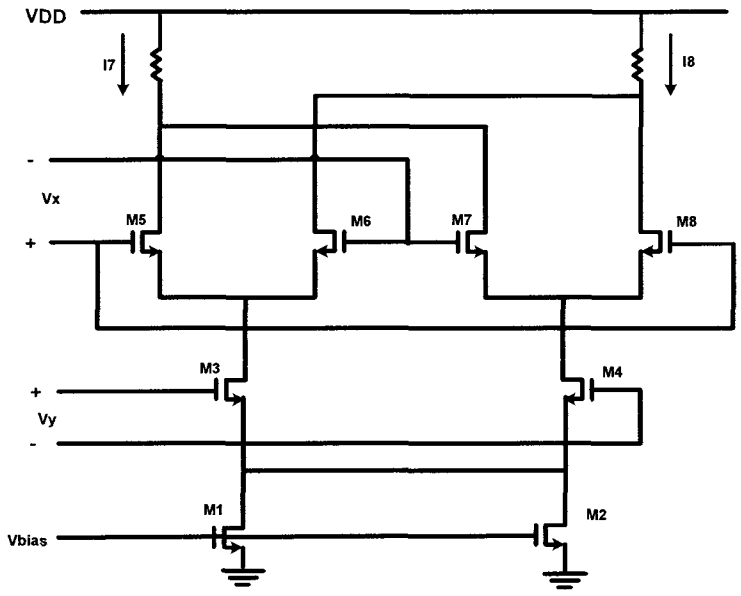


Figure 4-4 CMOS Four Quadrant Gilbert Cell [37]

As shown in Section 3.2.5 and Page 41, according to the design figure-of-merit ($f_T * \frac{g_m}{I_d}$) vs. $V^* = 2 * \frac{I_d}{g_m}$, an V^*= 200 mV is chosen to make sure transistor is in strong inversion yet maintain good linearity and also is able to achieve maximum speed and high current efficiency as shown in Figure 3-13.

From Eqn. 3-2, $\frac{g_m}{I_d}$ is set to 10 when V^*= 200 mV. A gain of 2 ~3 is desirable. In this design, a gain of 3 is chosen as $A_v = 3$ and R_{load} = 1KΩ. Double Balanced Gilbert Cell gain is

$$A_v = \frac{2}{\pi} g_m R_{load} \qquad (4\text{-}19)$$

g_m is calculated from $\frac{A_v * \pi}{2R_{load}}$ as 4.7 mA/V, therefore, I_d = 0.47 mA for transistor M5 ~ M8 by the $\frac{g_m}{I_d} = 10$ relationship. So the biasing current is $2*I_d$ = 0.94 mA ≅ 1mA.

According to the current density vs. width plot shown in Figure 3-14 for 0.13μm technology, a reference transistor $\frac{W}{L} = \frac{1\square m}{0.12\square m}$ is chosen as V_{ov} = 200 mV and V_{ds} = 1V, the current density is I_{ds} = 45.49 μA/μm.

For Gilbert Quad transistor M5 ~ M8, the designed current is transistor M5 ~ M8 so the transistor width would be $W_{5\sim8}$ = 10 μm. For biasing transistor M1~M4, the designed current is $I_{biasing}$ = 0.94 mA ≅ 1mA, so the transistor width would be $W_{1\sim4}$ = 20 μm.

4.2 Active Correlation with Different Templates

In the last section, the active double balanced Gilbert Cell working as a mixer/modulator, phase detector and analog multiplier is introduced, with emphasis on the function and limitation as an analog multiplier. Both inputs of the double balanced Gilbert Cell have to be in the linear range in order to operate in the precise multiplication mode.

In this section, the double balanced Gilbert Cell based active correlator will be investigated for analog correlation purpose. Due to the difficulty of local template pulse generation, three different local templates, namely switched sine wave, clock template and 5th Gaussian pulse will be

used to multiply the incoming 5th Gaussian pulse in order to choose the better template for correlation.

As introduced in Chapter 2, a sine wave can be used as a suboptimum template for a quick assessment of receiver performance. The system degradation is quite flat over the frequency when the correlation time is +/-0.5ns. Although this sine wave template is convenient to generate, for high resolution and ranging accuracy applications in UWB Impulse Radio, it might not be an optimal option. In this section, the sine wave is mainly used to model interference. The correlation test aims to locate the most crowded interference frequency band so that UWB operation could be avoid.

4.2.1 Correlation with Sine Wave (as interference)

Short range wireless signals such as Wi-Fi and Zigbee mainly operate around 2.4GHz and 5GHz. These nearby wireless signals can be easily picked up by UWB receiver and become interference for it. When small UWB signals enter the receiver, they are usually accompanied with higher adjacent interference. For general case, a continuous sine wave is used to model the interference [26].

In this test, two cases are studied by making the local templates as either a 5th Gaussian pulse modeled signal or an easily generated switched sine wave. Two input signals are selected from 5th derivative Gaussian pulse (peak-to-peak 0.4V) and a continuous sine wave modeled interference (peak-to-peak 1V). The output values of multiplying the desired Gaussian UWB signals with different local templates are listed in Table 4-2 and their corresponding plots are shown in Figure 4-5.

Table 4-2 Simulation Output Level for Sine Wave Interference in Gilbert Cell

Input / Output / Template	UWB Input Signal (0.4V) ~ 5 GHz	Interference Sine Wave (1V) (~ 2.4GHz)	Interference Sine Wave (1V) (3~7GHz)
Gaussian Pulse Template (0.4V)	49mV	21.6 mV	50 mV @4.6 GHz
Switched Sine Template (1V)	52mV	25 mV	136 mV @5 GHz

As shown in Figure 4-5, for about the same output signal level (49mV for 5th Gaussian Pulse Template and 52mV for Switched Sine Template), the interference difference between multiplying with the Gaussian pulse template and with the switched sine template is only a few mV (21.6 mV and 25 mV) around 2.4GHz. However, the sine template has much higher interference levels at higher frequency with a peak value around 136 mV at 5GH. So, for a quick assessment of receiver performance especially at frequency lower than 4GHz, a switched sine wave template can be used because it is easy to generate. However, in general case over the whole UWB band, a Gaussian pulse template is a better choice in particular at higher frequency.

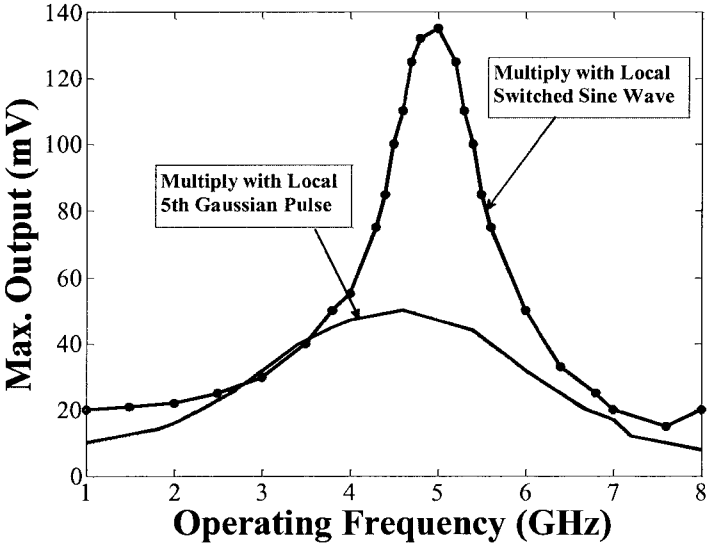


Figure 4-5 Sine Interference Correlation with Gaussian & Switched Sine Templates

4.2.2 Correlation With Clock Template

An active correlator combined with a double balanced Gilbert Cell and a RC integrator is tested in the same test bench as the passive clocked correlator shown in Figure 3-2 in order to compare their performances. A RC integrator is basically a low pass filter circuit operating in the time domain that converts the multiplied output into a triangular-like waveform output as the capacitor charges and discharges. For a first order passive RC integrator, the time constant τ = RC. If two first order RC filters are cascaded together, then a second order filter is obtained with time constant $\tau = \sqrt{R_1 R_2 C_1 C_2}$.

In this test, an RC integrator is indeed made of two low pass filters, R_1 = 2 KΩ, C_1 = 100 fp, R_2 = 2 KΩ, C_2 = 200 fp. This second order low pass integrator has a time constant $\tau = \sqrt{R_1 R_2 C_1 C_2}$ = 2.83E-10s, while the clock template has a period of 2E-10s.

An input clock template of 600mV is used for both passive and active correlator simulation. The active correlator results are shown in Figure 4-8, while the passive clocked correlator results are shown in Figure 3-18. From both simulations it is shown that active Gilbert Cell has much higher gain (peak to peak amplitude is around -70mV/+70mV) than the passive correlator (peak to peak amplitude is only -6mV/+6mV). Both output waveforms have the same period and look very similar for different pulse delays. Although both correlators perform similar function, the double balanced Gilbert Cell has higher voltage gain at the expense of higher power consumption due to its extra dc biasing circuits.

4.2.3 Correlation with 5th Gaussian Pulse Template

An ideal 5th Gaussian pulse is the best choice for local template although it is difficult to generate. A new test is designed for this purpose by correlating a 5th Gaussian pulse template with an

incoming pulse in a double balanced Gilbert Cell, as shown in Figure 4-6. The Differential Voltage Controlled Delay Element (VCDE) and the differential 5th Gaussian pulse generator were reused from those in passive clocked correlator test bench. The low pass filter and output buffer schematics are shown in Figure 4-7. $R_1 = R_2 = 667.84\,\Omega$ and $C_1 = C_2 = 77.58fF$. For M1 andd M2, $W_{1/2}/L_{1/2} = 20\ \mu m\ /120\ nm$. For M3 and M4, $W_{3/4}/L_{3/4} = 44\ \mu m\ /120\ nm$.

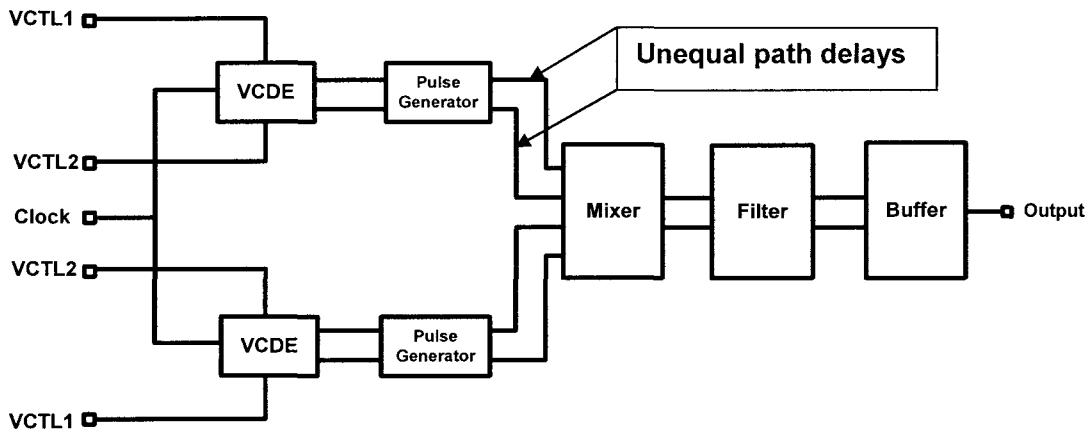


Figure 4-6 Test bench for Pulse Correlates Pulse

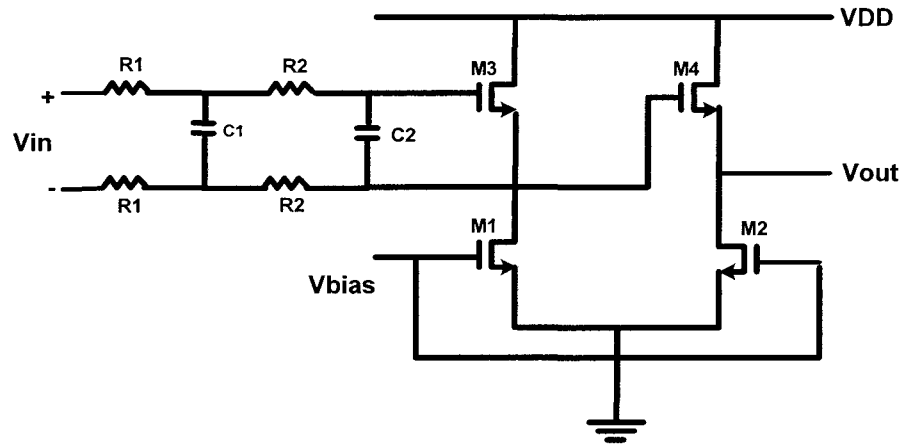


Figure 4-7 Low Pass Filter and Output Buffer

Because the pulse generator is triggered only on the rising edge of the clock, clock delay on the

rising edge in the upper path would not affect the rising edge of the clock in the lower path if VCTL1 in the upper path becomes the VCTL2 in the lower path, and vice versa. After the pulse generator, the generated pulse in the upper path moves to the right, while the other pulse in the lower path shifts to the left. Due to this specific test structure arrangement, a larger delay between two pulses could be achieved. The two pulses then get multiplied together and filtered out. For each delay, the maximum value of the correlation is simulated and recorded as shown in Figure 4-8. Like in Section 3.2.6, this plot is based on transient simulation, but it is not a transient plot. X Axis is not time but "pulse delay" between the received UWB pulse and clock template.

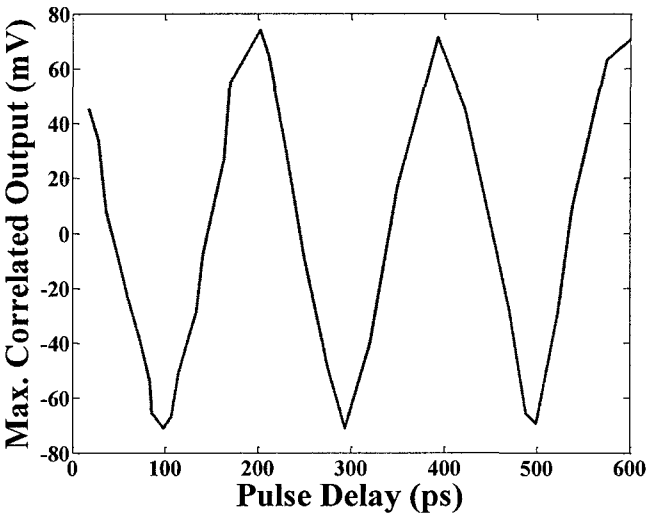


Figure 4-8 Max. Correlated Output - Gilbert Cell + Integrator

4.3 Measurements and Test Setup

Measurements were conducted by using a HP 54750A Digitizing Oscilloscope, HP 8131A Pulse Generator and Cascade Microtech Summit 7000 Probe Station. The test chip for Double Balanced Gilbert Cell has die size is 800μm by 540μm which is shown in Figure 4-9 together with the test measurement setup. The HP 8131A Pulse Generator is connected to an INPUT pad

which is part of the left Pulse Generator Chip shown in Figure 4-12. This INPUT pad is connected to two pulse generators in the upper and lower paths which generate two 5^{th} derivative Gaussian pulses. Two input pads VCTL+ and VCTL- are tied to two VCDE internally. Two voltage meters I and II are tied to VCTL+ and VCTL- externally and are used to adjust the delay between the two generated Gaussian pulses. The two pulses are multiplied in the analog multiplier and filtered out. The output is measured using a HP 54750A Digitizing Oscilloscope.

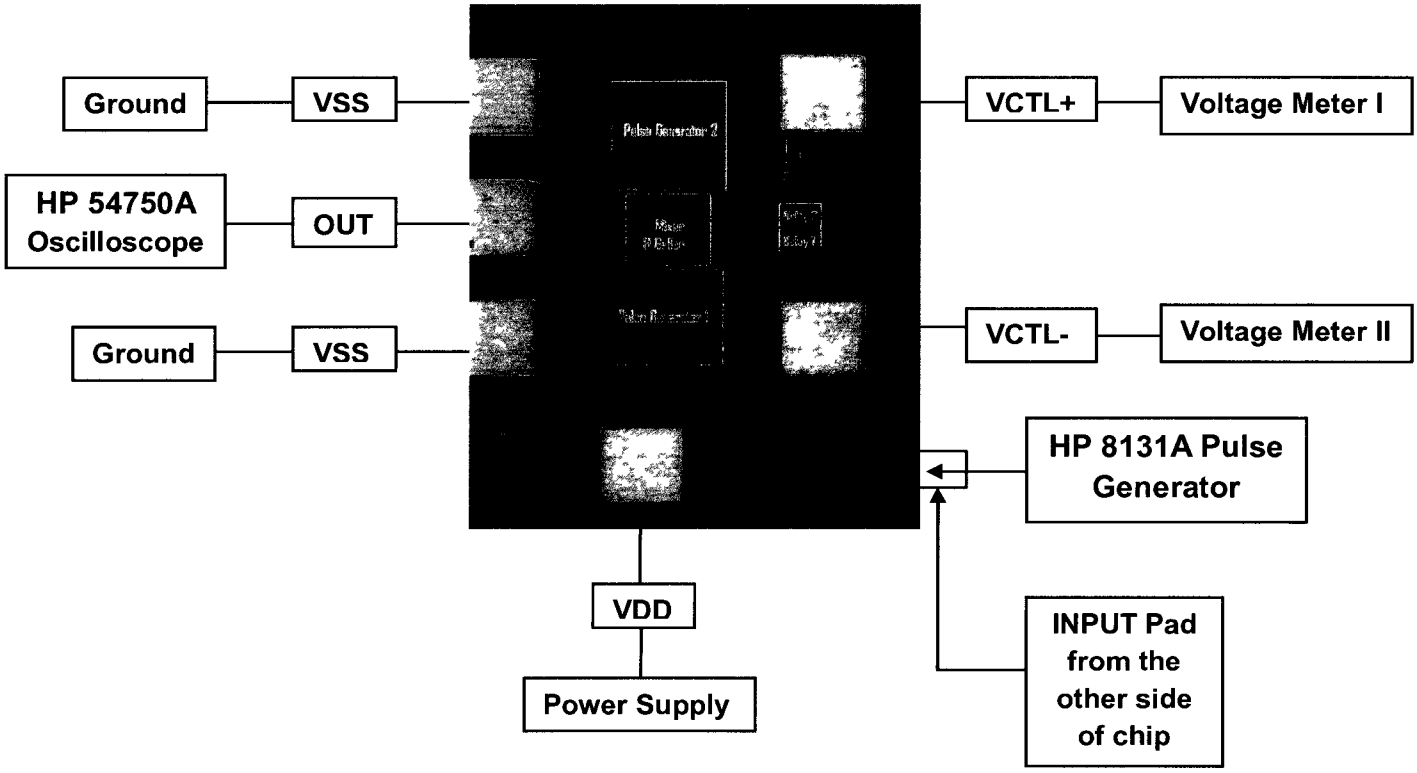


Figure 4-9 Active Correlator Die Photo and Test Measurement Setup

For the particular delay which produces the maximum output, the plot in time domain is shown in Figure 4-10 -- the picture is taken from the oscilloscope by camera. The maximum output (point A in Figure 4-11) is about 90mV below the reference level.

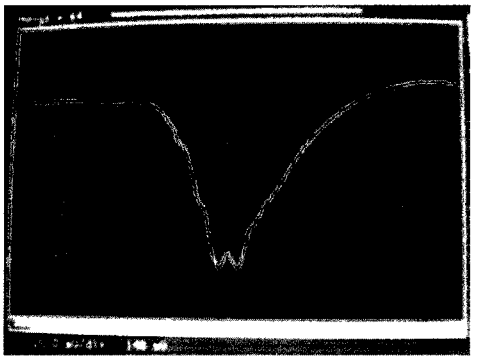


Figure 4-10 Max Correlation Plot in Measurement (picture taken from camera)

The simulated and measured peak output voltage of double balanced Gilbert Cell anlaog multiplier is shown in Figure 4-11. The X axis is pulse delay and Y axis is the peak output voltage.

The blue curve on the top is for the simulation results. When the pulse delay is 0ps, the simulated nominal DC offset is 184.4mV. For other pulse delays , the simulated DC offset is always around 184.9 mV. Furthermore, because the voltage controlled delay time can not be measured directly, one way to obtain it is through simulation between control voltage vs. time delay. In this simulation process, simulation errors always exist. These errors directly affect the correlation output shown in Figure 4-11.

Because of the AC coupling during the measurement, DC level has not been obtained. Only the relative output level is displayed on the oscilloscope, as shown in Figure 4-10. As mentioned in the last paragraph, the simulated nominal DC offset is around 184.9 mV. Although there are many other mechanisms contributed to the DC offset beyond the simulated value at 184.9 mV, this value is still used for initial estimation for the DC shift. The shifted measurement becomes the green curve which is very close to the simulated blue curve. The Monte Carlo simulation shows a range of 35mV ~ 40mV for transistor size and process variations. The gap between the

simulation and measurement could come from unequal path delay between differential lines as shown in Figure 4-6. This unequal path delay could be translated into phase errors, which introduces extra DC offset.

This offset voltage could also come from unsufficient frequency response over the GHz UWB bandwidth at its input. Although the measured results are not exactly the same as the simulation, the principle has been demonstrated.

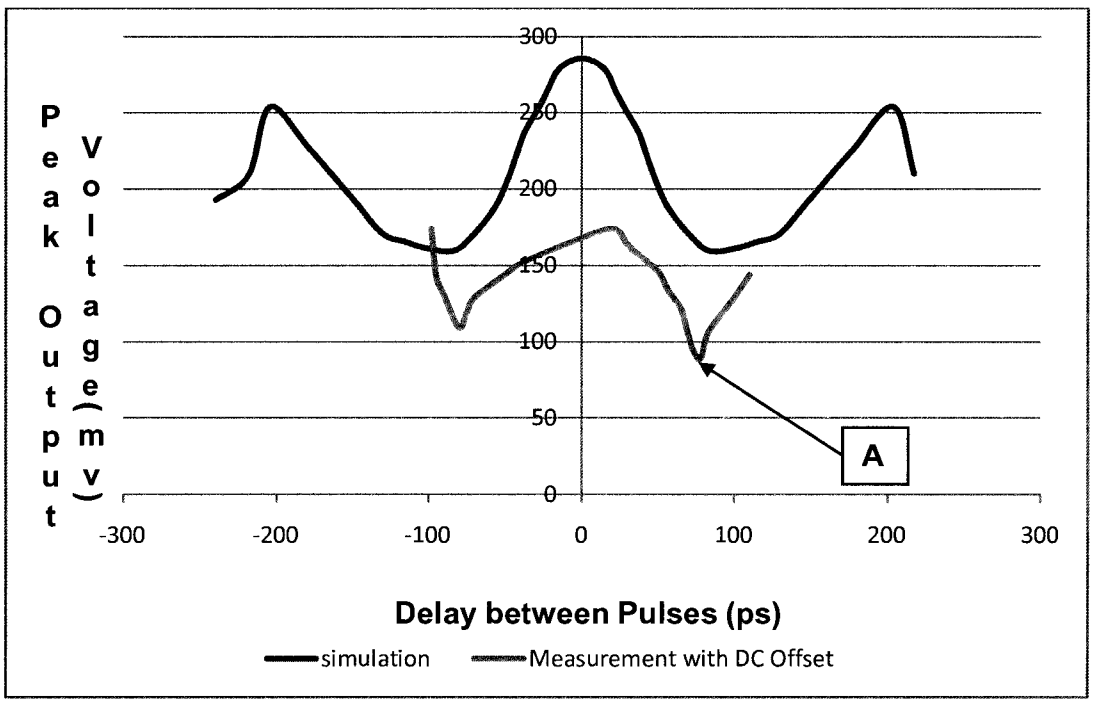


Figure 4-11 Max Correlation vs. Pulse Delay - Simulation & Measurement

The test chip layout is shown in Figure 4-12. The test chip contains two parts – on the left is the pulse generator (designed by Omid Abari), on the right is the double balanced Gilbert Cell based active correlator which I collaborated with Omid for his design. My main contribution in the active correlator is the Differential Voltage Controlled Delay Cell (VCDE).

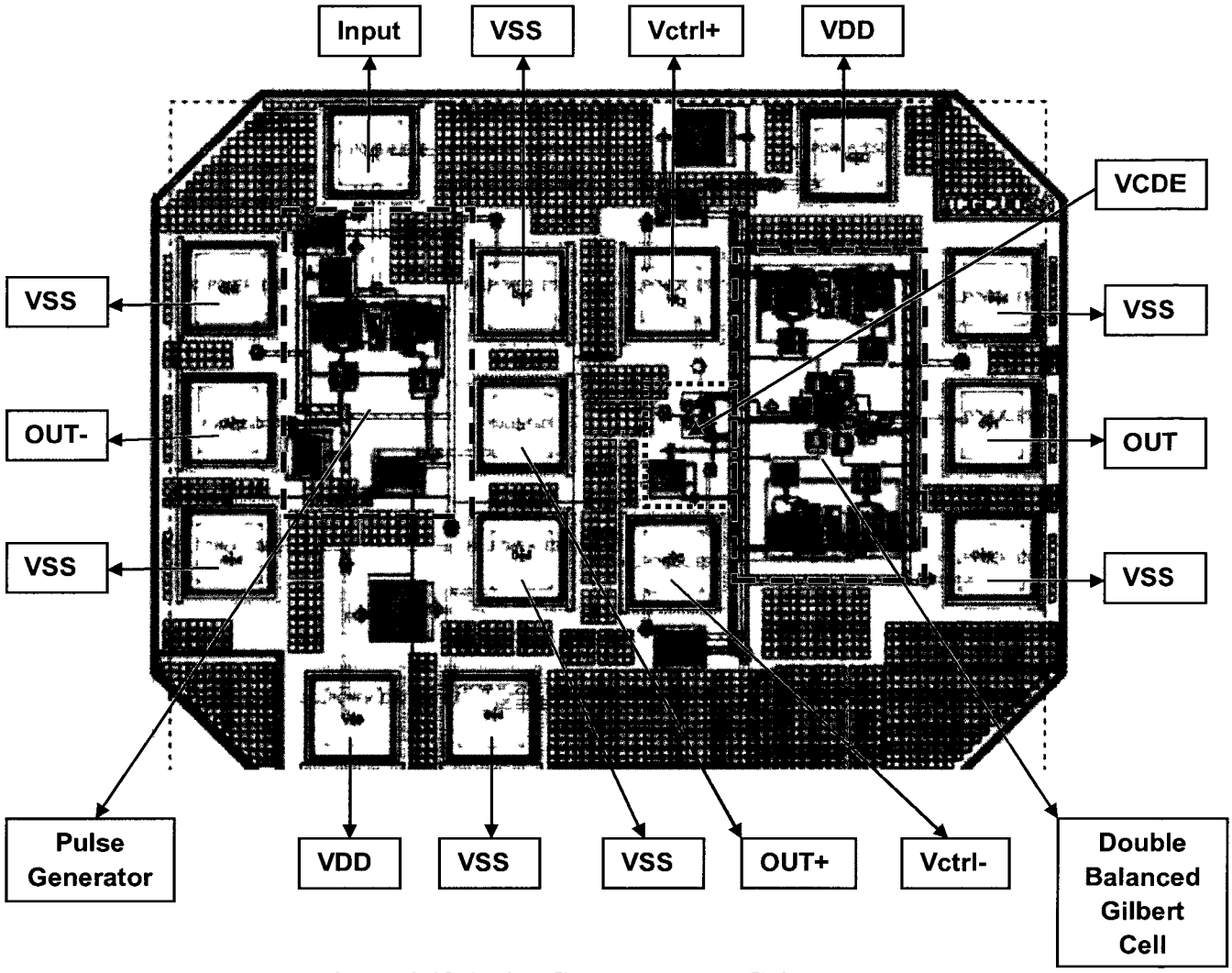


Figure 4-12 Active Correlator Test Chip Layout

4.4 Analysis and Discussion

Now, we are going to discuss the reasons and mechanisms behind the common mode mismatch and DC offset shown in simulation and measurement results Analog multiplier is sensitive to offsets due to its non-linear operation, device mismatches and process variations. These offsets would degrade the device linearity, reduce resolution and even saturate the following stages if the multiplier has a large gain.

4.4.1 Nonlinear Effects

For long channel device, I-V square law holds in strong inversion. As shown in the previous section, the double balanced Gilbert Cell working as an analog multiplier has a relative small linear range around the origin. Input voltage at both ports need to be in the linear range for desirable multiplication operation. Outside of the linear region, extra nonlinear components would degrade the multiplier performance.

For short channel devices, current-voltage relationship is more complicated by considering velocity saturation, mobility degradation and threshold variation. Although even-order nonlinearity can be cancelled through differential structure, the non-square I-V relationship gives extra third order distortion.

In this double balanced Gilbert Cell based analog multiplier, the 5th Gaussian pulse has peak-to-peak amplitude of +/- 400mV which is fairly close to the transistor threshold. The Gilbert Cell does not strictly operate in the limited linear region as in long channel device, therefore, accurate multiplication is not showed at the output.

The calculated linearity is between $+/-\sqrt{\frac{I_{ss}}{k}} =$ +/- 540 mV, and the simulated linearity for differential output current is shown in Figure 4-13. The plot suggests that the DC offset is about 0.4 V and linear region is from 206.1 mV to 640.1 mV ($\Delta = 434\ mV$) due to the nonlinear effects and other reasons which would be soon discussed in later sections. According to Figure 7.36 in [37], $2V_L = \Delta = 434\ mV$, so $V_L = 217\ mV$. From Eqn. 8.50 in [37] $V_{IP3} = 3.266\ V_L = 708.7\ mV$.

Some techniques can be used to extend the linear region, such as make input voltage at both input ports small, increase biasing current and make input devices long and narrow. In order to get stable and wide dynamic range for precise analog multiplication, extra circuits are needed to compensate these second order nonlinearities and cancel those higher order distortions as well.

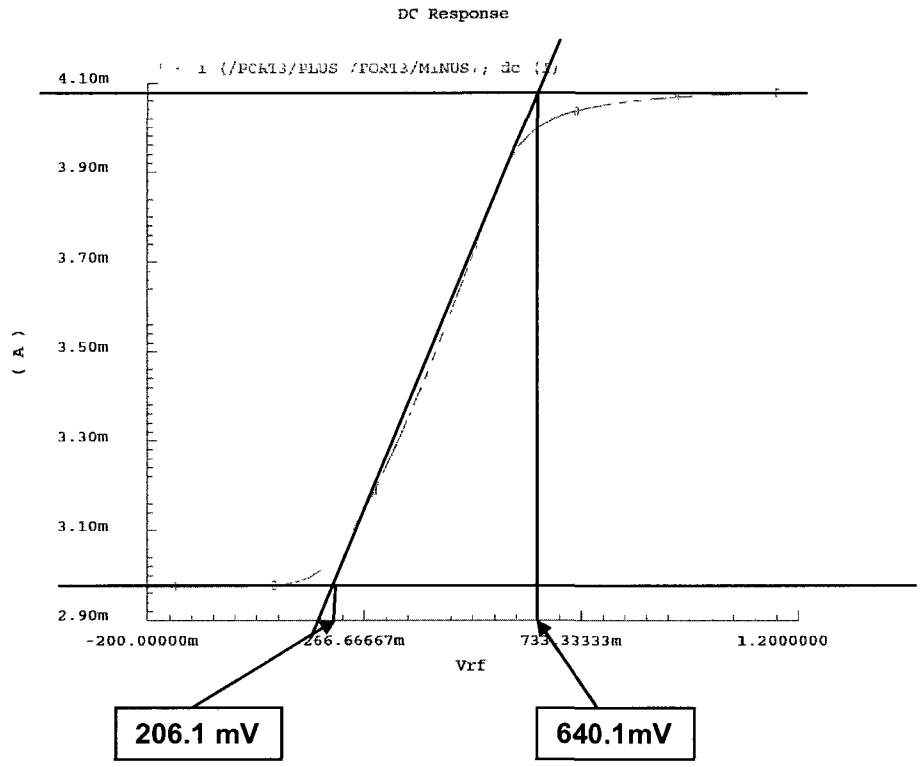


Figure 4-13 Double Balanced Gilbert Cell Linearity (Differential Output Current)

4.4.2 Unequal Path Delay on DC offset

Extra output dc voltage shift adds on top of this undesired dc offset when extra phase error is introduced with the misalignment of the two input pulses. Take one differential pulse generator as an example – one side of the generated pulse is V_{in1}, the other side is $V_{in1}{}'$ which is the delayed inverting version of V_{in1}.

When these two signals are fully differential, the common mode of the input signals - addition of both signals is zero. However, if these two signals are not fully differentially aligned, the common mode of these two input signals would shift away from zero due to phase error. After the Gilbert Cell, the maximum output could be either positive or negative depending on which output side of differential buffer (inverting buffer) is used. In our case, the multiplied maximum output is always positive.

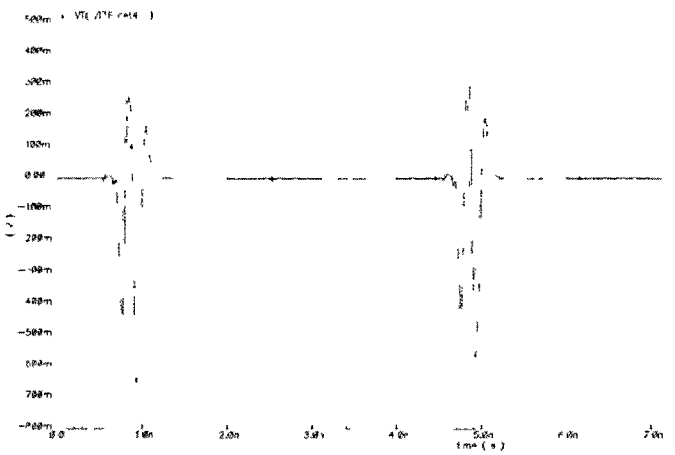


Figure 4-14 Differential Inputs with Time Delay

A series of simulations are performed for maximum correlated output when delay between two pulses varies and DC offset due to the unequal path delay is about 185 $\boldsymbol{mV}$. All this means that the four quadrant Gilbert Cell is not working properly as an analog multiplier due to phase error between two differential inputs. [49] [50] [51]

4.4.3 Device Mismatches and Process Variation on DC Offsets

Beyond nonlinear operation and unequal path delay, device mismatches also contribute to the DC offset due to double balanced Gilbert Cell differential structure. The mismatch resources come from load resistors mismatches, differential pair transistors mismatches, unequal dc currents in two branches. Furthermore, in short channel devices, threshold decreases due to small L would contribute large offset to differential pairs [36].

The errors introduced in Gilbert Cell can be expressed as differential output voltage: [46]

$$V_o = R_1(I_5 + I_7) - R_2(I_6 + I_8)$$

$$= \left(R + \frac{\Delta R}{2}\right)(I_5 + I_7) - \left(R - \frac{\Delta R}{2}\right)(I_6 + I_8)$$

$$= R[\,(I_5 - I_6) - (I_8 - I_7) + \frac{\Delta R}{2R}(I_{ss} + kV_x{}^2)] \qquad \textbf{(4-20)}$$

The DC term $\frac{\Delta R}{2}(I_{ss})$ is the extra offset at the output nodes and $\frac{\Delta R}{2R}(kV_x{}^2)$ is the input feed through to the output. Although higher biasing current would extend the linear region, however, at the same time it introduces additional DC offset at the output. The same mechanism for device parameter k, a long and narrow input transistor increases the linear region but feed extra input signal to the output. So either a good design tradeoff needs to be applied or a circuit scheme is necessary to break up these two conflict design restraints.

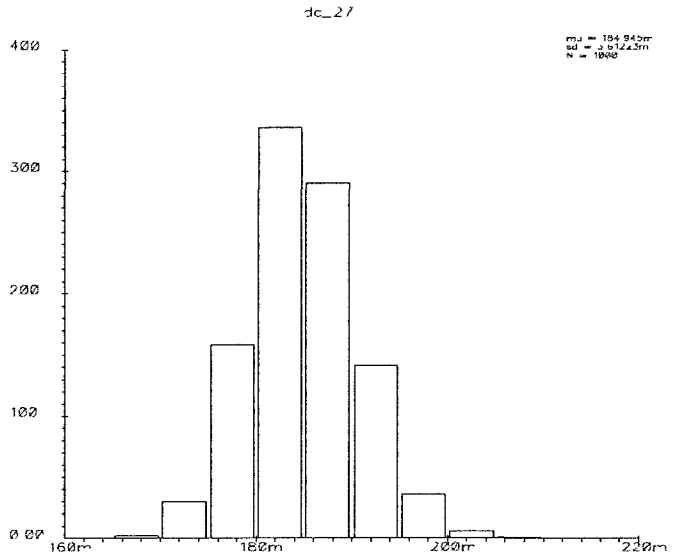


Figure 4-15 Monte Carlo Simulation for DC Offset (Transistor Size and Process Variations)

The Monte Carlo statistical simulation is conducted to account for manufacture process variations and device mismatches which is shown in Figure 4-15. The nominal DC offset is 184.9 mV with 5.6 mV standard deviation. The simulation is very close to the measurement results which are about 185 mV.

For double balanced Gilbert Cell, device mismatches are specifically simulated where device tracking is critical. There are two major mismatches - threshold and mobility variation due to local variations in doping, and geometric Across Chip Variation (ACV) due to gate length, orientation and local environment. [52] As it mentioned before, although a long and narrow input transistor can increase the linear region, extra input signals are also fed into the output. From device matching point of view, a long and narrow transistor is also difficult to match. Figure 4-16 shows statistical results from device mismatch only. The nominal DC offset is 184.4 mV with 3.6 mV standard deviation.

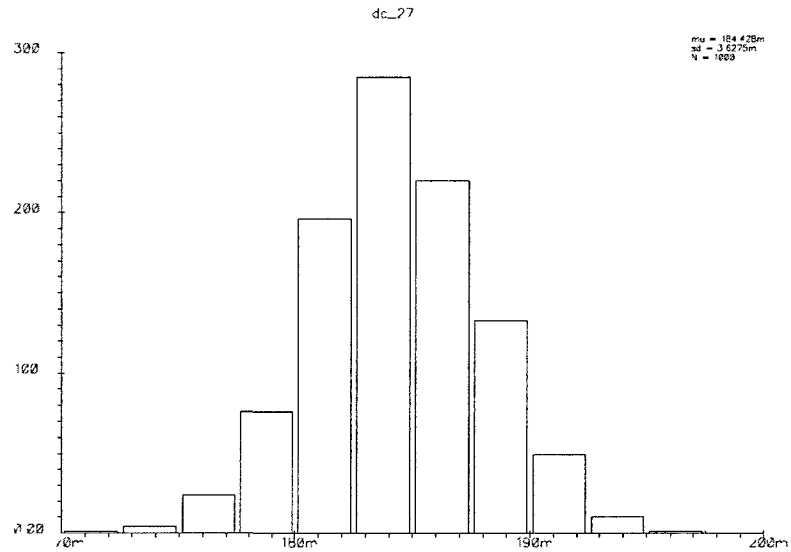


Figure 4-16 Monte Carlo Simulation for DC Offset (Device Mismatch Only)

4.4.4 Noise Figure and Power Consumption

In the double balanced Gilbert Cell, the dominant noise comes from the V-I converter. Besides, the biasing resistor and load resistor both contribute to the noise significantly. The simulated Noise Figure is about 13.2 dB to 19.6 dB within UWB bandwidth from 3.1 GHz ~ 10.6 GHz, as shown in Figure 4-17.

The power consumed in the active Gilbert Cell mainly comes from the biasing circuits and static power. The simulated Gilbert Cell power consumption is 2.6 mW. The current drawn from VDD is 2 mA so the calculated power consumption is 2 mA*1.2V = 2.4 mW.

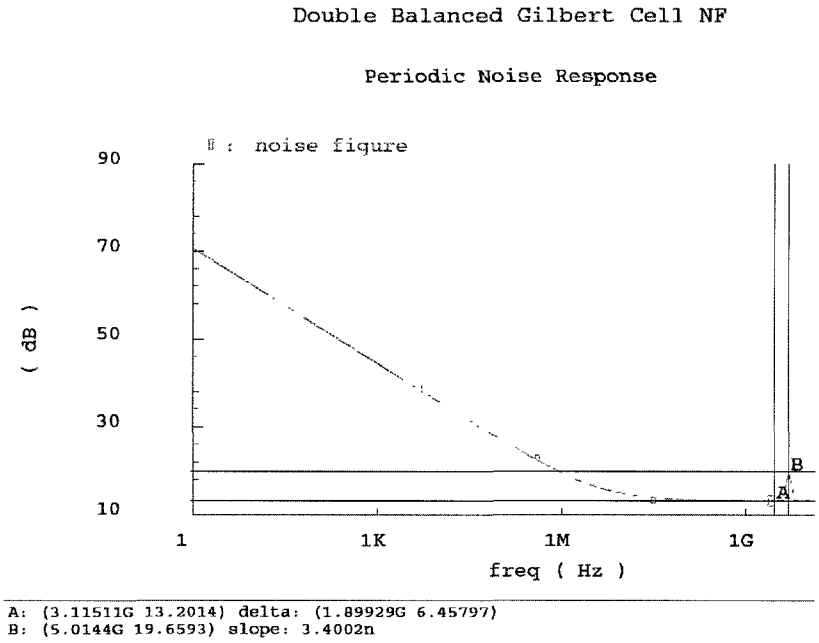


Figure 4-17 Double Balanced Gilbert Cell NF

4.4.5 Design Suggestions

In order to solve the DC offset issue due to unequal path delay between the upper and the lower branch, a varactor can be inserted in order to introduce extra delay for the alignment of two pulses. However, this is just an expedient technique to temporally solve the problem. The fundamental issue in analog multiplier design should consider a wide input frequency response so that the multiplier can handle the ultra wide band from 3.1GHz to 10.6GHz. Beyond this, low voltage low power design criteria should also be taken into consideration because Gilbert Cell has three stacked transistors. Circuits need to be designed by incorporating $\frac{g_m}{I_d} * f_t$ figure-of-merit to meet both speed and low power requirements. In order to achieve these goals, careful

choice of biasing current, passive component value, transistor size are important for the working circuit. Besides, additional compensation and calibration circuits need be added to cancel the offsets due to nonlinear circuit, device mismatches and phase errors mentioned before.

4.5 Active Correlator Summary

In this Chapter, a double balanced Gilbert Cell analog multiplier is introduced as part of an active correlator. Three different functions of Gilbert Cell, namely working as mixer/modulator, phase detector and analog multiplier, have been presented with specific applications. Especially the differences between mixer and analog multiplier have been discussed intensively in terms of their signal amplitude and noise. A double balanced Gilbert Cell is designed using $\frac{g_m}{I_d} * f_t$ composite figure-of-merit to meet both high speed and low power requirements.

The active Gilbert Cell picks up interference (modeled as sine wave) easily. At lower frequency especially between 2.5 GHz to 3.5 GHz, a local switched sine template and 5^{th} derivative Gaussian pulse template would not make much difference for the interference output level. However, interference output increases sharply at higher frequency and peaks at 5GHz for sine template. So at both lower and higher frequency, a local generated 5^{th} derivative Gaussian pulse is preferred for correlation. A sine wave template could provide a quick overview of receiver performance especially at frequency lower than 4GHz.

An active correlator combined with a double balanced Gilbert Cell and a RC integrator is tested in the same test bench as the passive clocked correlator. Active Gilbert Cell based correlator has higher output voltage gain than the passive correlator at the expense of higher power consump-

tion due to its extra dc biasing circuits. Its total power consumption is 2.6 mW while the passive correlator only consumes total 4.28 μW. The simulated Noise Figure is about 13.2 dB to 19.6 dB within UWB bandwidth from 3.1 GHz ~ 10.6 GHz.

A specific test bench has been set up for correlation between two Gaussian pulses. The double balanced Gilbert Cell in this case acts as an analog multiplier which has limited linear range around the origin. Analog multiplier is sensitive to offsets due to its non-linear operation, unequal path delay on DC offset, device mismatches and process variations. Monte Carlo Simulation shows nominal DC offset is 184.9 mV with 5.6 mV standard deviation counting both device mismatches and process variations. For device mismatches only, the nominal DC offset is 184.4 mV with 3.6 mV standard deviation.

The measurement and simulation plots look similar and are very close to each other by counting DC offset and variation range obtained through Monte Carlo simulation. One possibility of the gap between the simulation and measurement could come from unequal path delay between differential lines. This unequal path delay could be translated into phase errors, which introduces extra DC offset.

Analog multiplication is the focus of this thesis and an analysis of long channel double balanced Gilbert Cell and its counterpart short channel device is given in terms of output current and its

nonlinearity. The short channel second order effects impair the linearity furthermore. It increases the output differential current and at the same time introduces the third order nonlinearity.

Therefore, a low voltage analog multiplier with wide dynamic range is highly desirable for correct multiplication with fast response for UWB Impulse Radio. In order to achieve these goals, additional compensation and calibration circuits are needed to correct the DC offsets and cancel the third order nonlinear components. In the next chapter, some design guidelines will be given for future research and design endeavor.

Chapter 5

Conclusions

5.1 Summary of Thesis Contribution

IR-UWB Impulse Radio becomes a promising candidate for short range communication in medical area due to its simple architecture, small form factor and ultra low power consumption. Its large transmission power spreading not only improves the noise immunity from the adjacent narrow band signals but also provides precise ranging and locating. The low data rate IR-UWB has enough bandwidth to handle the monitoring and data collection tasks with better interference immunity and location accuracy.

In fully digital transceiver, signal correlation is implemented in digital domain and power consumption is dominated by the high speed and wideband ADC. However, this type of ADC is very difficult to design and power hungry as well. By moving the signal correlation into the analog domain, power consumption can be greatly reduced. The design challenges are the high performance yet low power analog correlator design and the generation and alignment of the extremely narrow pulse template in the time domain.

The intermittent characteristic of UWB pulses makes the passive correlator very attractive to reduce overall power consumption. A test bench was designed to test the passive correlator performance. Individual components inside of the test bench, such as differential 5^{th} derivative pulse

generator (designed by Omid Abari), differential voltage controlled delay element (VCDE) and frequency divider have been designed and analyzed.

However, the passive correlator has some intrinsic problems due to the nonlinearity at both RF and LO ports, which greatly affects its multiplication functionality. Although power reduction and easy local clock template generation are the main motivations behind this architecture, its overall system performance is not very desirable considering extra noise generated from clock feed through and nonlinearity at RF input port due to large input amplitude.

For comparison, a double balanced Gilbert Cell based analog multiplier was introduced as part of an active correlator. Three different functions of the Gilbert Cell, namely working as mixer/modulator, phase detector and analog multiplier, have been presented with specific applications. Among them, analog multiplication which is the core function inside of signal correlation becomes the focus of this thesis. A double balanced Gilbert Cell is designed using $\frac{g_m}{I_d} * f_t$ composite figure-of-merit to meet both high speed and low power requirements.

The double balanced Gilbert Cell based active correlator is then investigated for analog correlation purpose. Due to the difficulty of local template pulse generation, three different local templates, namely switched sine wave, clock template and 5^{th} Gaussian pulse is used to multiply the incoming 5^{th} Gaussian pulse in order to choose a better template for correlation. Their individual performance and resistance to interference have been studied as well.

Switched sine wave can be used as suboptimal local template and also can be modeled as interference. If the incoming signal is modeled as a 5^{th} Gaussian pulse, for about the same received signal and noise level, a local switched sine template and Gaussian pulse template would not make much difference for the interference output level between 2.5 GHz to 3.5 GHz,. However, interference output increases sharply at higher frequency and peaks at 5GHz for the sine template. Therefore, a sine wave template could provide a quick overview of receiver performance especially at frequency lower than 4GHz. For a system that requires high SNR such as IR-UWB, a local generated 5^{th} derivative Gaussian pulse is preferred for correlation.

For the pulse template, a specific test bench has been set up for active correlation between two Gaussian pulses. However, there are discrepancies between simulated results and measurement data attributed to the nonlinearity and unequal path delay introduced DC offset. The analog multiplier is sensitive to offsets due to its non-linear operation, device mismatches and process variations. These offsets degrade linearity, reduce resolution and could even saturate the following stages if the multiplier has a large gain. Monte Carlo Simulation shows nominal DC offset is 184.9 mV with 5.6 mV standard deviation counting both device mismatches and process variations. For device mismatches only, the nominal DC offset is 184.4 mV with 3.6 mV standard deviation.

The measurement and simulation plots look similar and are very close to each other by counting DC offset and variation range obtained through Monte Carlo simulation. One possibility of the gap between the simulation and measurement could come from unequal path delay between dif-

ferential lines. This unequal path delay could be translated into phase errors, which introduces extra DC offset.

The main contribution of this thesis is that not only a comparative study of a passive clocked correlator and a double balanced Gilbert Cell based active correlator has been presented, but some important design issues have been identified, especially the nonlinearity and offset analysis in short channel devices. An ultra low power, low voltage analog multiplier with wide dynamic range is ideal for precise multiplication with fast response for IR-UWB analog correlation. In order to achieve these goals, compensation and calibration circuits are needed to cancel third order nonlinear components and reduce unequal path delay as well as overall power consumption.

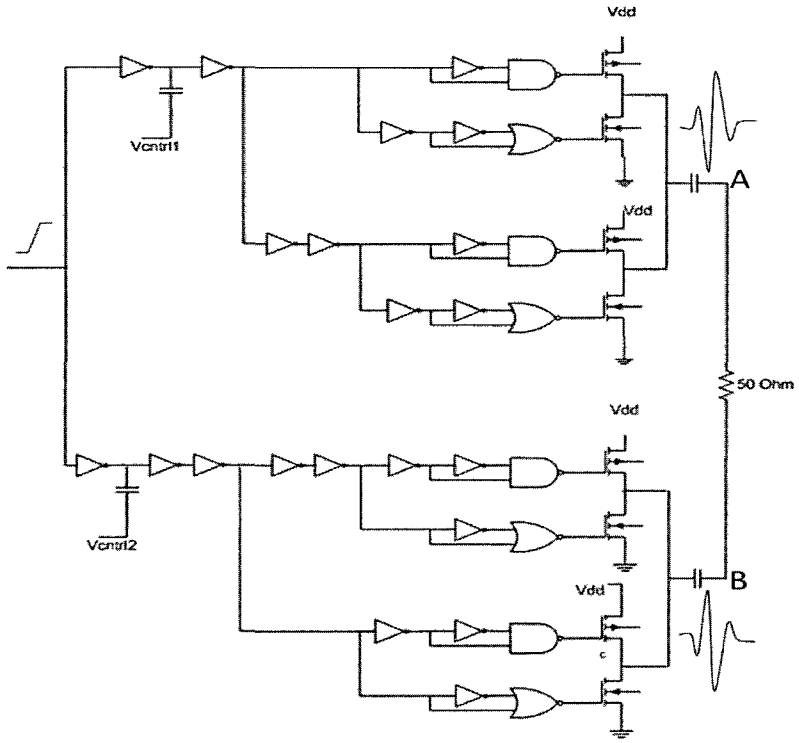
5.2 Future work

The most important contribution in this thesis showed that because the CMOS transistor is a nonlinear device, third order nonlinear components need to be canceled or compensated in order to only keep the first order linear multiplication. For analog correlator, a low voltage multiplier with wide dynamic range yet consumes as little power as possible is highly desirable. Several goals are expected through the design process of the analog multiplier:

- Improve linearity and increase wide dynamic range for both input and output
- DC offset compensation for non-linear operation, unequal path delay, device mismatches and process variations
- Compensate and calibrate circuit to cancel third order nonlinear components
- Reduce charge injection effect and increase SNR at the output
- Reduce overall power consumption

Besides, an effective feedback timing controller needs to be implemented to acquire and track the input signal so that timing synchronization could be eventually completed.

Appendix I – Differential 5th Derivative Pulse Generator



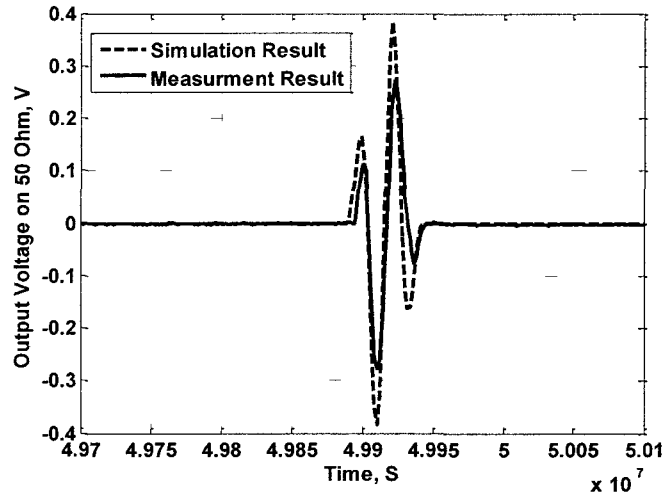
5th Differential Pulse Generator

In this design, only one transistor is turned on for a short period at any given time. Therefore, the circuit power consumption is extremely low. Besides, differential circuits intrinsically have better noise rejection ratio and increased signal swing at the output. Another purpose of using differential pulse generator is to set up an experiment for the double balanced Gilbert Cell based active correlation which is going to be shown in the following section.

As shown in the above plot, the rising edge of a clock triggers a pair of pulses 180° degree apart which pass through two pulse generators and combine at the output stage. This design approach requires a high degree of precision in delay to ensure both pulses remain precisely 180° out of phase. A varactor is added at the beginning of each path to perform fine tuning of the delay. The output stage contains two NMOS transistors and two PMOS transistors, which is designed to drive a 50 ohm load.

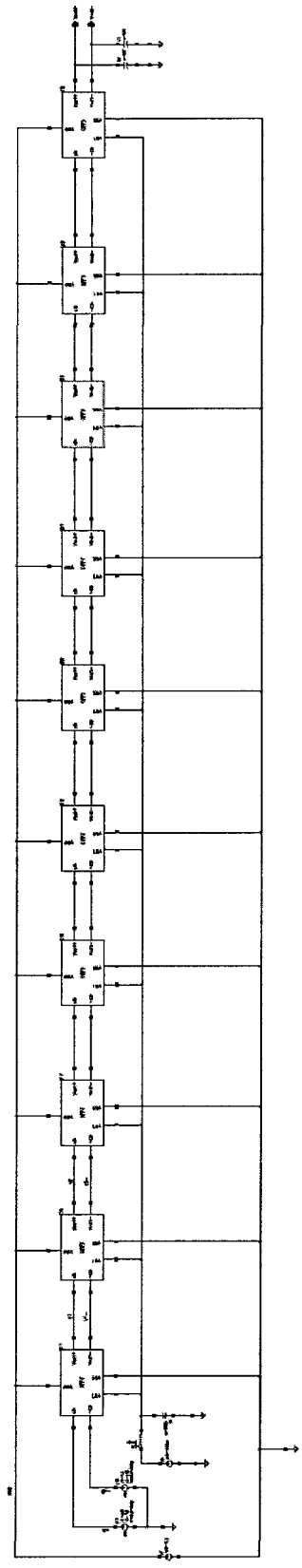
The generated Gaussian pulse has peak-to-peak voltage swing of 540mV and a pulse width of 510ps. The overall circuit has power consumption of 1.63mW at 300MHz Pulse Repeating Frequency (PRF). The generated pulse fully complies with FCC regulation.

A simulated pulse is shown together with a measurement pulse in the following plot. The pulse width matches very well between the simulated and measured data, while the measured amplitude of the pulse is about 0.1V less than the simulation due to equipment loss.



Measured Pulse and Simulated Pulse

Appendix II – 10-stage Frequency Divider



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