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The undersigned recommend to the Faculty of Graduate
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"SWITCHED CAPACITOR CIRCUITS FOR VLSI:

A DESIGN STUDY"

submitted by Peter Gillingham in partial fulfillment
of the requirements of the degree of Master of
Engineering.

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ABSTRACT

In this thesis, two major aspects of monolithic voiceband switched capacitor filtering are examined. First, a new approach to the design of op-amps, involving the operational transconductance amplifier (OTA), is discussed. The OTA features low power and has been found, in both computer simulations and measurements made on a test chip, to overcome many of the inherent problems commonly associated with short channel VLSI realizations of analog signal processing circuits. Second, the issue of overall filter structure is addressed with a differential topology intended to reduce noise and increase dynamic range. A previously unreported switched capacitor architecture, which realizes the bilinear transform in a balanced differential circuit, is presented. Finally, a complete balanced switched capacitor biquadratic filter is designed, using these principles, and laid out in a short channel CMOS process.

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LIST OF SYMBOLS AND ABBREVIATIONS

A - Amplifier Gain
B - Mos Transistor Gain Constant
BBD - Bucket Brigade Device
 C_L - Load Capacitance
 C_S - Stray Capacitance
CAD - Computer Aided Design
CCD - Charge Coupled Device
CMOS - Complementary Metal Oxide Semiconductor
CMRR - Common-Mode Rejection Ratio
DIL - Dual-in-Line (package)
DRAM - Dynamic Random Access Memory
 g_f - Forward Transconductance
 g_m - Gate Transconductance
 g_o - Output Conductance
 g_s - Source Transconductance
 I_p - Polarization Current
IC - Integrated Circuit
IIR - Infinite Impulse Response
k - Boltzman's Constant
L - Transistor Gate Length
LSI - Large Scale Integration
MOST - Metal Oxide Semiconductor Transistor
n - Body Effect Slope Factor
NMOS - n-Channel Metal Oxide Semiconductor
 ω - Frequency (rad/sec)
OTA - Operational Transconductance Amplifier
PMOS - p-Channel Metal Oxide Semiconductor
PSRR - Power Supply Rejection Ratio
q - Unit Charge (one electron)
Q - Integrated Charge Flow
s - Continuous Time Frequency Variable
SC - Switched Capacitor

T - Clock Period / Absolute Temperature

V - Common Mode Voltage

V_{cm} - Early Voltage Coefficient

V_m - Transistor Threshold Voltage

V_T - Virtual Ground Voltage

V_{vg}
VLSI - Very Large Scale Integration

W - Transistor Gate Width

y - Admittance

z - Discrete Time Frequency Variable

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1.0 INTRODUCTION

This thesis is concerned with improvements in the design of voiceband switched capacitor filters, to realize lower power and improved dynamic range in a CMOS VLSI process. Work is carried out on both an improved operational amplifier and on balanced filter structures using this amplifier. Design approaches for switched capacitor filters are also considered, including a method of using the SPICE CAD program in the filter synthesis.

1.1 HISTORICAL BACKGROUND

The technology required to produce monolithic analog filters has existed for some time. In comparison to filters built up from discrete components, whether passive LC or RC active, a filter realized entirely on a silicon chip has the obvious advantages of smaller size and lower cost, and may well consume less power, have higher reliability, and require no trimming [1]. Yet until only very recently, monolithic voiceband filters have not been widely used and the bulk of filtering requirements in communications, telephony and consumer electronics has been satisfied by discrete analog circuits.

From the time when the first monolithic operational amplifiers were produced in the 1960s the possibility of fabricating single chip RC active filters has existed. The major stumbling block to this approach has been the inability to make resistors of sufficient tolerance on chip. Fabrication technology was, and indeed still is today, such that excessive variations in resistivity occurred from sample to sample, making it virtually impossible to manufacture accurate analog filters.

The introduction of bucket-brigade devices (BBD) and charge-

2.5 THE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

The OTA [9] is an amplifier where output is modelled as a current source because it has a high output impedance. (fig.2.8) The output current is equal to the differential input voltage times the gain which must be expressed as a conductance - hence the name, operational transconductance amplifier. The cascode output stage discussed in the previous section is best described in this way. If the Thevenin equivalent of the cascode configuration were transformed to a Norton equivalent circuit, it would be represented by a current source of value $gm_1 \times v_{in}$ in parallel with the output conductance defined by eq.2.10. The high voltage gain is largely the result of high output impedance, across which the current $gm_1 \times v_{in}$ develops the output voltage. Any resistive load is likely to significantly reduce the voltage gain of the cascode stage.

With the OTA, it now becomes possible to shift the frequency compensation network from some internal node to the output itself, by virtue of the device's high output impedance. The advantages to this divergence from standard op-amp practice are the following:

1. No internal capacitor is required resulting in a savings of IC area. The compensating capacitor will be the load capacitance which, in switched capacitor circuits, is already adequate to ensure stability.
2. Reduction in the size of the output transistors and a further reduction in IC area. Since the output pole is no longer a parasitic pole, the use of huge devices to reduce the output RC product is unnecessary.
3. Reduction of power consumption. Since minimizing output impedance is no longer a concern and high currents are therefore no longer required, current demands on the power supply will drop.

$$I = \frac{V_1 - V_2}{R}$$

(a)

$$I = \frac{C(V_1 - V_2)}{T} \quad \therefore R' = T/C$$

(b)

Fig.1.1 The Switched Capacitor Resistor

and any variation in capacitance, due to processing, will not change the respective capacitor ratios. As a result, the frequency response will remain unaffected. Like BBDs and CCDs, the accuracy of a switched capacitor filter depends only on the clocking frequency and the ability to accurately define areas on the integrated circuit. The switched capacitor filter though has the advantage that a direct correspondance exists with well known and understood RC active filters, and that its design is done on a circuit level of abstraction rather than the device level on which the CCDs and BBDs are designed. The success of SC filters lies as much in their similarity to the most widely used family of discrete filters as in their good performance and low sensitivities to process variations.

1.2 STRAY FREE SWITCHED CAPACITOR FILTERS - STATE OF THE ART

Most SC filters in use today can be classed as strays insensitive. This term describes a general class of filters which uses the virtual ground of operational amplifiers and a particular type of switched capacitor to reduce the effects of parasitic capacitances on the circuit operation [4]. The two basic configurations, the inverting and non-inverting stray free integrators, are shown in fig.1.2. Since the switch through which charge passes to the integrating node of the op-amp switches between ground and virtual ground, the charge in stray capacitor C_s should be negligible, assuming the op-amp gain is sufficiently high. For this reason, the structures are stray insensitive. In contrast, the switched capacitor in fig.1.1 is not stray-free, since the parasitic capacitor is in parallel with the switched capacitor, and would result in a periodic charge transfer larger than originally intended. Using the two integrating configurations as basic components, many different stray-free switched capacitor filter topologies have been constructed. These include biquad and ladder structures [5]. Strays insensitive configurations allow the designer more freedom in that he is less concerned with the particulars of the actual IC process used.

(a)

(b)

Fig. 1.2 a. Non-Inverting Stray Free Integrator
b. Inverting Stray Free Integrator

1.3 SWITCHED CAPACITOR CIRCUITS IN VLSI

Integrated circuit process technology has advanced to the point where device dimensions on the order of 1-2 μm can be realized. In order to exploit this improvement in circuit density, the switched capacitor circuit designer will have to come to grips with some of the limitations inherent in short channel devices. First, there is a reduction in power supply voltage made necessary by reduced breakdown voltage characteristics of small transistors. This implies a reduced dynamic range for analog signals. Second, there is a reduction in the quality of the drain curves for short channel devices, which places an upper limit on the voltage gain that can be had with a given device. And third, if maximum circuit densities are indeed the goal, and a large amount of digital circuitry is to be placed on the same chip, then power consumption of the analog part must be minimized so as not to exceed the power dissipation capacity of the IC package.

The objective of this thesis is to investigate solutions to the problems encountered with VLSI switched capacitor circuits. It will address essentially two distinct areas in which improvements can be made. The first is the operational amplifier itself. Most of the power consumed in a switched capacitor filter will be dissipated in the op-amp. The problems of low-gain short-channel devices will greatly affect op-amp performance, especially since high gain is important in maintaining a strays insensitive structure. Therefore, a new operational amplifier will be investigated which provides the high gain and low power consumption which will be necessary for VLSI implementations of SC circuits.

A second area of improvement is in the filter structure itself. Since there is a loss of dynamic range in reducing supply voltages, some means of compensating for this should be found. Perhaps the dynamic range can be extended through the use of

balanced circuits, in which the signal is represented by two out-of-phase components on each side of a twin circuit. For a given supply voltage, this method would double the effective maximum signal level. It also reduces the circuit's susceptibility to common mode noise. Sources of noise, such as the power supply, could be expected to inject equal amounts of noise to both sides of a balanced circuit. Since the circuit is differential, noise of this kind is effectively cancelled. At the penalty of having twice the circuitry, balanced techniques could improve the dynamic range of switched capacitor circuits, making them suitable for VLSI voiceband signal processing.

1.4 THESIS FORMAT

In chapter 2, CMOS op-amps are considered in depth, and the applicability of operational transconductance amplifiers (OTA) in switched capacitor filters is discussed. This provides a background for chapter 3 in which an OTA is dimensioned and laid out in a 5um CMOS process. Measurements made on the test chip confirm the design methodology.

Chapter 4 introduces balanced filter topologies and includes a discussion on switched capacitor filter synthesis. The practical problems of common mode stability of differential structures are addressed in chapter 5. Then the design and layout of a balanced switched capacitor biquadratic low pass filter in a CMOS VLSI process is presented. At the time of the submission of this thesis, the integrated circuit was not yet available for testing.

Chapter 6 then concludes the report by summarizing the work accomplished and suggesting applications for analog VLSI signal processing.

2.0 DESIGN CONSIDERATIONS FOR CMOS OPERATIONAL AMPLIFIERS

Standard designs for CMOS op-amps may not be the most suitable for switched capacitor filters. This chapter examines the design of operational amplifiers in general, with particular emphasis on CMOS technology, and proposes the use of a different op-amp configuration in switched capacitor circuits. A brief discussion of frequency compensation of amplifiers provides an introduction to a discussion of the relative merits of the new design with respect to an example of a more conventional op-amp design. Then equations describing the gain and bandwidth of the new circuit are derived, and its performance in both strong and weak inversion is predicted.

2.1 FREQUENCY COMPENSATION OF AMPLIFIERS

The open loop gain of an amplifier will drop with increasing frequency as a result of capacitances, either parasitic or intentionally placed, along the signal path. These form first-order low-pass filters in conjunction with the output resistances of succeeding stages. Once the amplifier is placed in a feedback configuration, these capacitances may result in instability. To illustrate this point, consider the case of a three stage amplifier shown in fig.2.1. A first-order low-pass filter at the output of each stage causes an additional pole in the overall transfer function. The resistances represent the finite and non-zero output impedances of each amplification stage while the capacitances may be parasitics to ground, power supply lines, or any number of other fixed voltages. Assuming, then, that each stage has infinite input impedance, the gain of the three-stage amplifier can be written as follows:

Fig. 2.1 Multistage Amplifier

$$\frac{V_{out}}{V_{in}} = \frac{A_1 A_2 A_3}{(1+j\omega R_1 C_1)(1+j\omega R_2 C_2)(1+j\omega R_3 C_3)}$$

(eq.2.1)

If the three pole frequencies are widely spaced, the resulting bode plot will be something like that in fig.2.2. (assuming arbitrarily that $R_1 C_1 > R_2 C_2 > R_3 C_3$) Each pole causes a cumulative amplitude rolloff of 20dB per decade and a phase shift of -90 degrees.

Once the amplifier is used in a feedback configuration, its stability becomes a question. The criteria for instability are a loop gain greater than one and a phase shift of 180 degrees. Clearly, the larger the feedback factor, the greater the loop gain and therefore the closer the circuit is to instability. With a passive feedback network, the maximum possible feedback factor is unity. If the amplifier in fig.2.1 is to be stable in a unity-gain configuration, the phase shift at the frequency where gain has fallen to 0dB must be greater than -180 degrees. The difference between the phase at the 0dB frequency and 180 degrees is known as the phase margin [6] and is represented graphically on the bode plot. Similarly, the gain at the frequency at which the phase is equal to -180 degrees defines the gain margin. For stability, the gain margin must be greater than 0dB.

In a switched capacitor circuit the operational amplifiers are used in feedback configurations, with the largest feedback factor being unity. In the most general case, if we ensure that each operational amplifier's stability is guaranteed, and that the overall filter transfer function is stable, the circuit will not oscillate or saturate. To design an op-amp for use in switched capacitor circuits, we have only to ensure that the gain and phase margins are positive. As an aside, it should be noted that not all operational amplifiers are designed to maintain stability in unity gain configurations. An extended gain bandwidth product can be offered if an upper limit on the

Fig. 2.2 Multistage Amplifier Bode Plot

feedback factor is imposed. The RCA CA3100, for example, cannot be used in feedback configurations with gains less than 15 [7].

What can be done to ensure stability of an operational amplifier? Common practice is to introduce a dominant pole into the open loop transfer function at a frequency much lower than that of the first parasitic pole. If the rolloff due to the dominant pole has reduced the open loop gain to 0dB before the frequency of the first parasitic pole, the amplifier will have a phase margin of 90 degrees. Adding a pole to an amplifier in this manner is known as frequency compensation. Several possibilities exist for implementing frequency compensation in an amplifier. These differ in both the location of the compensating network and its type.

2.1.1 LAG COMPENSATION

This is the most straightforward form of frequency compensation. By adding an additional capacitor to the output of one of the gain stages in a multi-stage amplifier, a dominant pole can be created. The circuit remains essentially that of fig.2.1. The time constant of the compensating network can be roughly calculated given the frequency of the lowest parasitic pole and the DC open loop gain of the amplifier:

$$(RC)_{\text{comp.}} = A_{\text{DC}} \times (RC)_{\text{parasitic}} \quad (\text{eq.2.2})$$

Using this equation to determine component values for the compensation network, the unity gain frequency will occur at the same frequency as the parasitic pole. The question relative to which stage in a multi-stage amplifier the dominant pole should be placed cannot be addressed until output loading is considered. If lag compensation was done at the output of an operational amplifier the dominant pole position would change as a function of capacitive load. Furthermore, since most op-amps have low impedance outputs, this would call for large compensation

capacitors which may exclude the possibility of integrating them on chip. This problem will be addressed in greater depth further on.

2.1.2 LAG-LEAD COMPENSATION

The transfer function of an amplifier is modified by adding a zero and a pole. The zero coincides with the first parasitic pole and effectively cancels it, making it possible to extend the unity gain bandwidth to the frequency of the second parasitic pole. This method has the obvious advantage of extending a given op-amp's performance but introduces a serious problem if the intrinsic pole frequencies cannot be accurately predicted. A circuit which implements lead-lag compensation is shown in fig.2.3. Its transfer function, assuming R_1 includes the output impedance of the preceeding stage, is:

$$\frac{V_{out}}{V_{in}} = \frac{1+j\omega R_2 C}{1+j\omega(R_1+R_2)C} \quad (\text{eq.2.3})$$

The frequency of the zero must always be higher than that of the pole. Normally, the zero of the compensation network would null out the first parasitic pole. If, due to process variations, this were not the case and the zero occurred at a higher frequency than the pole, there would be a kink in the lead-lag curve in fig.2.4, and, as a result, the gain margin may drop to less than 0dB.

In the context of monolithic integrated amplifiers, the lag compensation network would be less sensitive to process variations. All the resistors for both compensating and parasitic poles are the result of transistor output impedances. If one device varied, all other devices could be expected to vary proportionally, thus keeping the pole positions relative to one another unchanged. In the lead-lag configuration, however, the resistor R_2 would be implemented as a diffused resistor and could not be expected to maintain ratios with impedances of

Fig. 2.3 Lead-lag Compensation Network

Fig. 2.4 Comparison of Bandwidth for Two Compensation Networks

other types.

2.2 AN ALTERNATE APPROACH TO FREQUENCY COMPENSATION

Most commercially available operational amplifiers, and those found on LSI integrated circuits, have been designed to satisfy a diverse range of applications. Much design effort is saved by not having to lay out a different amplifier at every point in the circuit where one is required. From the designer's point of view, this is the principal advantage of using op-amps; they can be considered as ideal gain blocks and circuit synthesis can be performed on a higher plane of abstraction than would be possible on the discrete transistor level. It is therefore only natural that the same op-amp designs used in RC active filters have been adopted for use in switched capacitor filters. Perhaps we should question the suitability of the classic operational amplifiers for SC filters with a view to improving performance. Are there features in the common garden variety op-amp which are unnecessary in SC filters? To shed light on this, the characteristics of, and the tradeoffs made in the design of, a "general purpose" operational amplifier are examined.

2.3 THE GENERAL PURPOSE OP-AMP

The general purpose operational amplifier is designed to approximate, to such an extent as is necessary and possible, an ideal op-amp. More specifically, it should have high differential gain, infinite input impedance, and an output impedance close to zero. Non-ideal effects like power supply feedthrough, noise and input offsets should be minimized. To illustrate the general purpose operational amplifier, consider its realization in a CMOS [8] process as shown in fig.2.5. Here T1, T2, T3 and T6 are n-channel (NMOS) transistors while the remainder are p-channel (PMOS). The gain of this amplifier is concentrated largely in the input stage. A slight change in current, in the input branch at

Fig. 2.5 CMOS OP-AMP

which the output is taken, will result in a large voltage change because the load for this input transistor has a very high small signal impedance. The second stage may provide some further voltage amplification but its main function is to provide a low impedance output and sufficient current-drive capability. The n-channel transistor T1 must be supplied with a DC bias, V_1 , to set input stage currents.

Frequency compensation of this amplifier is achieved at the output of the first stage. There are three fundamental reasons for this:

1. The output of the differential input stage has a high source impedance. The realization of a particular RC time constant, therefore, requires a relatively small capacitor. For an integrated circuit this is an important consideration because a low value of capacitance has a smaller area requirement.
2. The output stage has an intentionally low output impedance and would require a large compensation capacitor if the dominant pole were situated here.
3. It would be inconvenient to have the dominant pole situated at the output since its frequency would be determined, at least in part, by the load capacitance. The unity gain bandwidth would have to be curbed in order to ensure stability over a range of load capacitances.

This frequency compensation scheme is not, however, without faults. Some of the major weaknesses are:

1. Stray capacitance at the output of the first stage will most likely be less than that found at the output of the op-amp. There are several reasons for this. First, the output devices are large and will have large drain-substrate capacitances. Second, the output node may

snake across the integrated circuit and be connected to a number of loads. The input stage, in contrast, makes only one connection internal to the op-amp. Part of the capacitance required for compensation, at least, is to be found at the output.

2. If the pole at the first stage were the parasitic pole, it would be much easier to predict its frequency, as the loading on this point does not vary. Instead of compensating for the worst-case parasitic capacitance we could compensate for a known parasitic by ensuring a capacitive load on the output above some minimum value.

For applications requiring an op-amp to drive a resistive load, there is clearly a need for the type of amplifier shown in fig.2.5. But, in a switched capacitor circuit, no continuous current is required; it is only necessary that the amplifier have a slew rate sufficient to charge a capacitor within certain time limits. A low impedance output may not be needed. Another argument for modifying the output stage stems from power consumption considerations. If frequency compensation is done internally, efforts must be made to reduce the effect of the output pole so that the unity gain bandwidth can be extended. Given a load capacitance, the only thing that can be done is to reduce the effective output impedance. If transistor lengths are already minimum, the only way to achieve this is to increase current. An order-of-magnitude increase in bandwidth dictates an order-of-magnitude increase in current and power consumption. Even though an amplifier need not drive large loads, it may, nevertheless, consume a lot of power in order to maintain stability.

2.4 THE CASCODE OUTPUT STAGE

Since switched capacitor circuits do not require large currents from the op-amp outputs, a different output stage can be

investigated. The standard common source output stage examined in the previous section can be dispensed with in favor of a circuit with high output impedance. The series connection of two MOS transistors shown in fig.2.6 is called the cascode configuration. The input is fed to the gate of T1. In the small signal model this transistor is represented by a current source equal to the input voltage multiplied by the transconductance of the transistor, which is related to process parameters and device dimensions. The second transistor is biased by a DC voltage but its source is not at a constant potential. There will, therefore, be a second current source in the small signal model proportional to T2's source transconductance times the source voltage. Source transconductance differs from the gate transconductance as a result of the body effect. The derivation of this parameter is presented in Appendix A. With this information, the voltage gain of the cascode stage can be calculated.

By superposition, the effects of each source are analyzed separately. First, consider the current source $g_{m1} \times v_{in}$. The other current source is replaced by an open circuit.

$$V_s = \frac{-g_{m1} V_{in}}{g_{o1}} \quad (\text{eq.2.4})$$

Now, consider the effect of current source $g_{s2} \times V_s$ which also develops a voltage across g_{o2} is analyzed. The output voltage can be calculated:

$$V_{out} = V_s + \frac{g_{s2} V_s}{g_{o2}} \quad (\text{eq.2.5})$$

$$\therefore \frac{V_{out}}{V_{in}} = - \frac{g_{m1}}{g_{o1}} \left[1 + \frac{g_{s2}}{g_{o2}} \right]$$

$$(\text{eq.2.6})$$

Fig. 2.6 a. Cascode Configuration
b. Small Signal Model

The gain of the cascode can be seen to be very high. It is roughly equal to the gain of a single transistor squared since $g_{s2}/g_{o2} \gg 1$. Note that this is achieved with no load other than the internal impedance of output devices themselves.

Next, to calculate output impedance, a voltage source is connected to the output and the resultant current calculated. The voltage v_{in} is now set to zero. (see fig.2.7) Once again by superposition:

$$g_{out} = \frac{i_{out}}{V_{out}} = \frac{V_s g_{o1}}{V_{out}} \quad (\text{eq.2.7})$$

$$V_s = - \frac{g_{s2} V_s}{g_{o1} + g_{o2}} + \frac{g_{o2} V_{out}}{g_{o1} + g_{o2}} \quad (\text{eq.2.8})$$

$$\frac{V_s}{V_{out}} = \frac{g_{o2}}{g_{o1} + g_{o2} + g_{s2}} \quad (\text{eq.2.9})$$

$$\therefore g_{out} = \frac{g_{o1} g_{o2}}{g_{o1} + g_{o2} + g_{s2}} = \frac{g_{o1} g_{o2}}{g_{s2}} \quad (\text{eq.2.10})$$

There is an effective multiplication of T1's output impedance by the gain of the cascode transistors (g_{s2}/g_{o2}). This will become very useful especially with short channel devices where output impedances are notoriously poor. The cascode stage combines two features which could be invaluable in the final stage of an operational amplifier tailored for use in switched capacitor circuits, i.e. high gain and high output impedance.

Fig. 2.7 Cascode Small Signal Model for Calculating Output Impedance

Fig. 2.8 Transconductance Amplifier

2.5 THE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

The OTA [9] is an amplifier where output is modelled as a current source because it has a high output impedance. (fig.2.8) The output current is equal to the differential input voltage times the gain which must be expressed as a conductance - hence the name, operational transconductance amplifier. The cascode output stage discussed in the previous section is best described in this way. If the Thevenin equivalent of the cascode configuration were transformed to a Norton equivalent circuit, it would be represented by a current source of value $g_{m1} \times v_{in}$ in parallel with the output conductance defined by eq.2.10. The high voltage gain is largely the result of high output impedance, across which the current $g_{m1} \times v_{in}$ develops the output voltage. Any resistive load is likely to significantly reduce the voltage gain of the cascode stage.

With the OTA, it now becomes possible to shift the frequency compensation network from some internal node to the output itself, by virtue of the device's high output impedance. The advantages to this divergence from standard op-amp practice are the following:

1. No internal capacitor is required resulting in a savings of IC area. The compensating capacitor will be the load capacitance which, in switched capacitor circuits, is already adequate to ensure stability.
2. Reduction in the size of the output transistors and a further reduction in IC area. Since the output pole is no longer a parasitic pole, the use of huge devices to reduce the output RC product is unnecessary.
3. Reduction of power consumption. Since minimizing output impedance is no longer a concern and high currents are therefore no longer required, current demands on the power supply will drop.

An OTA circuit designed to exploit the advantages of shifting the locus of the dominant pole to the amplifier output is shown in the schematic of fig.2.9. The output features complementary cascode pairs. Provided both the n and p halves have identical gain and impedance characteristics, voltage gain of the output stage will be the same as that of a single cascode stage, assuming transistors T8 and T11 have equal and opposite signals on their gates. By connecting the small signal models of the two halves together at a common output node, it can be seen that the composite output impedance is one half that of a single stage.

The connections to the output stage are made to mirror the currents in both branches of the input stage. For the non-inverting input, the connection is direct from the load device. In the case of the inverting input, the n-channel current mirror reference must be converted to a p-channel reference. This is accomplished with transistors T6 and T7. The current in the output stage need not be identical to the input stage currents. By making transistor T11's W/L ratio b times that of T5, the output current would be b times that of the input current. So that signals to the n and p halves of the output stage remain equal in magnitude and complementary, the same ratio of input to output stage currents should be maintained for the inverting signal path. Hence $c \times d = b$.

The input devices selected are p-channel transistors since the $1/f$ noise coefficients of p-channel devices are generally much smaller than those of n-channel devices. As opposed to the op-amp in fig.2.5, the gain of the OTA's input stage is relatively low, because the load transistors have their gates connected to their drains. They will behave, for small signals, as resistors of value g_m , not go the output conductance. Most of the gain in this circuit must, therefore, come from the output stage. A further consequence of having load devices of this kind is that the frequency of internal parasitic poles will be increased, as a result of lowering the impedances driving each leg of the circuit. There should be little problem with internal poles

Fig. 2.9 CMOS OTA

causing closed-loop instability in this amplifier configuration.

The overall gain can be calculated using equation 2.6 and the following expression for input stage gain. This arises as a result of the small signal current in the input devices $g_{m3} \times v_{in}$ producing a voltage drop across the load device with a small signal conductance of g_{m5} . Since only one half of a purely differential input signal appears at each input, a additional factor of two appears in the equation for input stage gain.

$$\left[\frac{V_{out}}{V_{in}} \right]_{stage1} = \frac{g_{m3}}{2g_{m5}} \quad ; \quad g_{m2} = g_{m3} \quad ; \quad g_{m4} = g_{m5} \quad (eq.2.11)$$

$$\begin{aligned} \frac{V_{out}}{V_{in}} &= \left[\frac{V_{out}}{V_{in}} \right]_{stage1} \times \left[\frac{V_{out}}{V_{in}} \right]_{stage2} \\ &= \frac{g_{m3}}{2g_{m5}} \frac{g_{m11}}{g_{o11}} \left[1 + \frac{g_{s10}}{g_{o10}} \right] \quad (eq.2.12) \\ &\quad ; \quad g_{m11} = g_{m8} \quad ; \quad g_{o11} = g_{o8} \\ &\quad ; \quad g_{s10} = g_{s9} \quad ; \quad g_{o10} = g_{o9} \end{aligned}$$

This derivation for OTA differential gain rests on several assumptions. It assumes that the transconductances of input transistors T2 and T3 and load transistors T4 and T5 are identical. This ensures that the common mode input will, in this first approximation, have no effect on the output. Furthermore, both gate transconductance and output conductance of n- and p-channel cascode driver transistors T8 and T11 must be equal, as well as the output conductance and source transconductances of cascode transistors T9 and T10. These considerations allow the expression for OTA voltage gain to be reduced to the relatively simple expression of eq.2.12.

To get some idea of the performance that can be expected of the OTA in terms of gain and bandwidth, a design will have to be produced with actual process parameters. However, the general nature of its performance under varying bias currents can be postulated. It is useful to know how performance changes with bias current in both strong and weak inversion operation..

Since all branch currents in the OTA are proportional to the current set by V_p (the current source bias in fig.2.9), gain, bandwidth, and slew rate can be expressed as functions of branch current. Two distinct regions of operation for MOS transistors must be considered: In strong inversion the gate transconductance and source transconductance are both proportional to the root of drain current (see Appendix A). For weak inversion operation, the two conductances are directly proportional to drain current. Output conductance of MOS transistors is directly proportional to drain current in both regions of operation. Assuming that all devices in the amplifier have identical weak inversion limits, the manner in which the three selected indicators of op-amp performance vary with bias current I_p can be tabulated and displayed graphically. (see fig.s 2.10 and 2.11 respectively) The curve for DC gain can be derived by substituting into equation 2.12 the proportionalities mentioned above. Bandwidth is solely a function of output conductance, since load capacitance is fixed. Hence this curve can be derived from equation 2.10. Slew rate depends only on the maximum current which can be sourced or sunk, and the load capacitance. There is no difference between the behavior of slew rate in either strong or weak inversion. This curve is therefore a straight line.

It is interesting to note that the amplifier achieves maximum gain when all transistors operate under the weak inversion limit. The bandwidth, however, falls off in this region. In strong inversion, falling gain is compensated for by an increasing bandwidth which tends to maintain a more constant gain-bandwidth product over a range of bias currents! It will, in fact, increase

	<i>strong inversion</i>	<i>weak inversion</i>
<i>GAIN</i>	I_p^{-1}	1
<i>BANDWIDTH</i>	$I_p^{3/2}$	I_p
<i>SLEW RATE</i>	I_p	I_p

Fig. 2.10 OTA Proportionalities in strong and weak inversion

Fig. 2.11 OTA Performance vs. I_p

as the root of current, as shown in fig.2.12. That the gain-bandwidth product is so insensitive to current implies that the amplifier could remain stable over a wide range of bias currents. This may be useful in applications where the current is increased during times when a large capacitive load is to be slewed, but remains low most of the time to conserve power.

Fig. 2.12 Unity Gain Bandwidth vs. I_p

3.0 CMOS OTA TEST CHIP

This chapter outlines the design of an operational transconductance amplifier in an actual CMOS process. Utilizing the equations derived in the preceding chapter describing the behavior of the cascode output stage and the OTA as a whole, the dimensions of the amplifier's transistors are determined. Rough estimates of gain, bandwidth and other indicators of performance can be made with these initial calculations. A computer circuit simulation package, SPICE [10], is then used to more thoroughly evaluate the design. The simulations provide information which is used to adjust transistor ratios, so that there is minimum offset, i.e. the open loop output voltage of the OTA settles to zero volts when both inputs are tied to zero volts. The initial design cannot be expected to achieve that result because of channel length modulation effects on the current mirrors. From the drain curves of a transistor it is seen that, with a fixed gate voltage bias, drain current increases slightly with drain-source voltage. This departure from the ideal approximation of MOS transistor behavior means that current mirrors will actually have a slight current gain. Viewed at the OTA output, this will cause a significant offset which is rectified through the use of computer simulations.

Next, a simulation of the amplifier's open loop gain as a function of frequency is performed. This information serves to confirm the gain and rolloff frequency originally calculated, and to ensure that gain and phase margins are adequate for closed loop operation of the device. Since all parasitic capacitances are included in the simulation's input description of the OTA circuit, the effects of parasitic poles will be accurately reflected in the OTA open loop frequency response curves. Next, the amplifier is connected in a unity gain configuration and the time response to a unit step input observed. If the amplifier is close to instability, ringing and overshoot would be seen. The

slew rate can also be confirmed with this second simulation. Before the integrated circuit is fabricated, the simulations provide a comprehensive description of the circuit's performance.

Three OTAs were designed and then simulated with SPICE. One was actually fabricated and characterized. The process parameters used in the three designs represent real, existing CMOS processes, a 5 μ m design-rule production and 3 μ m and 1.5 μ m experimental preproduction processes. The OTA which has been fabricated, and for which the test results are presented, was done in the 5 μ m process. The designs in the short channel processes are discussed to point out the inherent advantages of the OTA configuration over more standard amplifier designs in VLSI technologies. They will also be used later in the layout of a balanced switched capacitor biquad.

3.1 DETERMINATION OF OTA DEVICE DIMENSIONS

One of the primary considerations in dimensioning the OTA, above and beyond those discussed in chapter 2 and which is not necessary to the operation of the device, has been to impose completely symmetrical and complementary operation of the n and p-channel halves of the cascode output stage. This restriction may not result in optimum utilization of silicon area, but it does provide a starting point for the calculations. Also, from the point of view of power supply rejection, it does tend to equalize injection from both rails, so that no one unwanted source of interference becomes dominant. A further assumption made is that the n-channel transistors in the output stage will be minimum size. Since p-channel transistors generally have lower gain, they will have to be larger than the minimum size in order to mirror the characteristics of the n-channel devices. For the 5 μ m process, the minimum sized transistor was chosen as 20 μ m x 10 μ m (WxL). The reason for such a large transistor was to insure accuracy of the computer simulations. Since the OTA design

is unconventional, it was decided that absolute assurance of the validity of the circuit took precedence over any desire to produce a compact layout. The minimum-sized devices used for the 3um and 1.5um processes were 3um x 3um and 3um x 1.5um respectively.

The underlying principle in dimensioning the transistors in the OTA is to create a true, complementary cascode output stage. First, the voltage gains from input to both n- and p-channel drivers must be equal. This implies equal current mirror ratios to both sides of the output stage. Then the gate transconductances of the cascode drivers and the source transconductances of the cascode transistors themselves must be equalized on both n- and p-sides of the circuit. Finally, output conductances for all four transistors in both halves are made identical. We now have a symmetrical output stage, in terms of both gain and output impedance, for optimum unity gain bandwidth.

Both n and p-channel devices are to have the same output conductances. In the cascode output stage this implies that the lengths of transistors T8 and T9 (in fig.2.9) depend on the lengths of the minimum sized n-channel transistors T10 and T11.

$$L_p = L_n \times \frac{(V_m)_n}{(V_m)_p}$$

(eq.3.1)

$(V_m)_n, (V_m)_p$ - early voltage coefficients for n and p devices. (in volts/um)

L_n, L_p - effective channel lengths in um

Next, the ac small-signal gain or gate transconductance of transistors T8 and T11 are equalized. (this parameter, along with other MOST characteristics, is derived in Appendix A) The following equation for the width of transistor T8 can be written in terms of the dimensions of T11.

$$\frac{W_p}{L_p} = \frac{L_p}{L_n} \frac{\frac{W_n}{L_n} \frac{B_n}{B_p}}{\frac{B_n}{B_p}} \quad (\text{eq.3.2})$$

n_n, n_p - slope factors for n and p devices

B_n, B_p - specific gain for n and p devices

Furthermore, the source transconductances of transistors T9 and T10 must be identical for symmetrical gain. Using the relationship for g_s derived in Appendix A:

$$\frac{W_p}{L_p} = \frac{L_p}{L_n} \frac{\frac{W_n}{L_n} \frac{B_n}{B_p}}{\frac{B_n}{B_p}} \quad (\text{eq.3.3})$$

With the cascode output stage fully dimensioned, we turn to the current mirror transistors. Since the most accurate current source is one with a one-to-one relationship between reference and mirrored current, the values of $b=c=d=1$ are chosen. All branch currents in the OTA circuit will be equal as a result, disregarding the minor deviations caused by channel-length modulation effects. T4, T5 and T6 will be minimum dimension devices like T11, and T7 will match T8. Finally, the input transistors T2 and T3 are chosen so that input-stage gain is sufficiently high so as to avoid aggravating input noise, and transistor T1 is made wide enough to allow a reasonable common mode swing. The transistor dimensions calculated with each of the three sets of process parameters are tabulated in fig.3.1.

The dimensions shown for transistor T7 are those adjusted with SPICE to minimize offset. A quick comparison between the W/L ratios of T7 and T8 for all three designs, indicates that T8 has the higher gain. This compensates for the fact that T7's drain voltage is greater, causing an increased drain current as a result of the finite output conductance of the device. The 1.5um and 3um amplifiers have many common dimensions. This has been

	5um WxL	3um WxL	1.5um WxL
T1	50x10	3x3	3x1.5
T2,T3	100x10	20x3	20x1.5
T4,T5,T6,T10,T11	20x10	3x3	3x1.5
T7	65x10	8.5x3	7.5x1.5
T8	209x29	19x6	19x2.5
T9	356x29	19x6	19x2.5

Fig. 3.1 OTA Device Dimensions

done purposely to facilitate the use of a single set of masks, with the exception of the gate polysilicon mask, in the fabrication of the two OTAs.

3.2 COMPUTER SIMULATION OF THE OTA DESIGNS

Once the rough calculations have been done, and all the devices in the design dimensioned, computer simulations can be used to verify performance and to make adjustments where required. Here, SPICE is used to evaluate DC gain, unity-gain bandwidth, slew rate and power dissipation of the three designs. Output conductance can also be determined by observing the frequency at which gain first starts to roll off. SPICE listings are included with this thesis in Appendix B.

The major indicators of OTA performance, as calculated by SPICE, are tabulated in fig.3.2. In addition, the open-loop frequency response of the three amplifiers is presented graphically. (fig.3.3) The power-supply voltages used are the maximum rated voltages for each process, 10 volts for the 5 μ m CMOS process, and 5 volts for the 1.5 μ m and 3 μ m technologies. Load capacitance for all cases has been set at 10pF. The amplifiers are designed to drive directly the bonding pad outputs as well as capacitive load internal to switched capacitor circuits and must, therefore, be capable of driving a capacitive load as high as 10pF. Note, however, that there is no resistive load in the simulations. The OTA is virtually incapable, in open loop, of supplying a continuous current to a resistive load. Bias current has been chosen in order to keep the transistors operating above the weak inversion limit (see Appendix A). Below this limit the circuit becomes more sensitive to bias current changes, and SPICE becomes less accurate.

Note the extremely high output resistance calculated for the OTA realized with 5 μ m design rules. This is largely the result of

	5um	3um	1.5um
DC gain	126 dB	99dB	76 dB
gain-band.	200kHz	500kHz	600kHz
R_{out}	160G Ω	3.2G Ω	1.6 G Ω
slew-rate	.14V/us	.22V/us	.23V/us
power	30uW	23uW	39uW
	$C_l = 10\text{pF}$ $V_{dd} = 5$ $V_{ss} = -5$ $I_p = 1.4\mu\text{A}$	$C_l = 10\text{pF}$ $V_{dd} = 2.5$ $V_{ss} = -2.5$ $I_p = 2\mu\text{A}$	$C_l = 10\text{pF}$ $V_{dd} = 2.5$ $V_{ss} = -2.5$ $I_p = 2\mu\text{A}$

Fig. 3.2 OTA Performance Calculated with SPICE

Fig. 3.3 OTA Open-loop Response
Calculated with SPICE

choosing a minimum-sized n-channel device of $20\mu\text{m} \times 10\mu\text{m}$. From equation 2.10, it can be seen that the output resistance of a cascode stage is that of a single transistor multiplied by the gain of the cascode transistor. Both the gain and output resistance of devices as large as those here will be high, so one would therefore expect the OTA to have an enormous output resistance. Although DC gain of the $5\mu\text{m}$ amplifier is very large, the unity gain bandwidth is small because of the effect of output resistance on the position of the dominant pole. It is futile to have so much gain accompanied by such a low rolloff frequency.

The $3\mu\text{m}$ and $1.5\mu\text{m}$ OTAs, in contrast, have lower gains but greater unity gain bandwidths by virtue of their lower output impedances. With the same capacitive loads as the $5\mu\text{m}$ OTA and as much as 50dB less open-loop DC gain, the short channel amplifiers are still able to offer higher performance. This reflects an important point in the consideration of op-amp designs for use in VLSI technologies. The OTA with cascode output stage and complementary devices lends itself to implementation in short channel processes. Using minimum sized devices, an amplifier with good performance, very low power, and small area can be designed. If an amplifier with an internal compensating pole, such as the one discussed in the previous chapter, were implemented in the same process, performance, power and area would suffer. For switched capacitor VLSI circuits, The OTA overcomes most of the inherent difficulties with short channel devices, and offers very good specifications.

3.3 THE OTA TEST CHIP

The $5\mu\text{m}$ technology OTA design has been realized in a CHOS process at Northern Telecom. The objective of this exercise was to evaluate the operational transconductance amplifier as a verification of the design methodology, and to give confidence in further efforts designing switched capacitor circuits using this amplifier. An additional complementary output has been included so that the device has balanced circuit potential. In fig.3.4,

Fig. 3.4 OTA Test Chip Schematic

the OTA test chip schematic, transistors T12-T17 form the inverted output stage and are dimensioned identically to transistors T6-T11 respectively. Cascode bias voltages are generated by sinking a single current I_c . OTA branch current I_p is set through a current mirror in much the same manner. For most of the tests, I_p has been set to 1.4uA, the same current used in the hand calculations and computer simulations

The OTA layout generated by the CALMA system at Northern Telecom is shown in fig.3.5. P-channel devices take up most of the area, with n-channel devices occupying the lower central portion of the chip. The large p-channel output devices are located to the left and right sides of the layout. To reduce the possibility of unwanted feedback paths which may cause instabilities, no interconnections have been routed over active areas. The OTA test circuit has been placed within a standard 14 pad probe array for ease of testing using standard probe cards. Fig.3.6 shows the OTA bonding pad assignments in this array. A number of the circuits has been bonded in 22 pin DIL packages.

3.3.1 DISCUSSION OF MEASUREMENTS

The circuit used to test the OTA is shown in fig.3.7. Power supply voltages of +5 and -5 volts are the maximum rated voltages for the CHOS process. The reference currents I_p and I_c are produced with resistors and an adjustable voltage source. The indicated voltage drops at each resistor represent the potentials required for the desired bias currents. The pin numbers shown on the diagram are those for the 22-pin DIL package.

The measured DC characteristics of the OTA are tabulated in Fig.3.3a. The input offset voltage, -20mV, arises as a result of differences between the parameters used in the SPICE simulation and the real parameters achieved in this particular run of the CHOS process. This was confirmed by examining a number of

Fig. 3.5 OTA Test Chip

Fig. 3.6 QTA Bonding Pad Assignment

Note: pin numbers
shown are those
on 22 pin DIP

Fig. 3.7 Test Circuit

<i>parameter</i>	<i>measured value</i>	<i>units</i>
<i>Input Offset Voltage</i>	-20	mV
<i>Input Common Mode Range</i>	+3.8 - 5.8	V
<i>Output Resistance (open loop)</i>	>100	G Ω
<i>Output Voltage Swing</i>	+4.9 - 4.9	V
<i>DC Open-Loop Gain</i>	>94	dB
<i>Power Consumption</i>	45	μ W

Fig. 3.8a DC Characteristics

($I_p=1.5\mu A$, $I_c=47\mu A$, $V_{dd}=5v$, $V_{ss}=-5v$)

samples which were all found to have offsets very close to this average value. Offset was measured as the output voltage of the OTA in a unity gain configuration with grounded input.

The OTA was found to have a large common mode input range. This is the range of voltages which can be applied in common mode to the inputs without affecting the output. The upper limit, 3.8 volts, is reached when the current source transistor, T1, is driven into the cutoff region. I_p no longer flows into the input stage and the output current drive capability is reduced. The lower limit on the common mode input range is -5.8 volts, significantly below the negative supply. Here, the input devices themselves are being driven into cutoff and currents in the rest of the circuit will fall off in the same way.

The output resistance of the OTA had to be measured in open-loop because feedback decreases the effective impedance seen at the output. The measurement was made by observing the output voltage with two different resistive loads, so that offset could be cancelled out.

Large signal output voltage swing was observed to within .1 volts of each power supply rail. With bipolar transistors such a swing would be impossible, but the MOS device behaves like a resistor in the hard-on state with small drain-source voltages. With no resistive load it is therefore possible to attain good performance in this respect. The gain of the OTA would be very low in this region of operation, where both the cascode transistor and the cascode driver transistor are operating in the cutoff region.

There was some difficulty in measuring the open-loop gain of the amplifier. The indicated value of 50 v/mv was derived from measurements in which the output varied over a range of three volts. Over a smaller range, it was evident that the gain was much larger, although it was impossible to measure. The Microsystems International Bulletin [11] offers the following explanation:

"thermal feedback effects can make the gain infinite or even have the wrong sign ... the number measured is of little practical significance"

Fig.3.8b is a tabulation of the OTA AC characteristics. Note that the load capacitance was of the order of 20pF. To this total the scope probe or true RMS meter contributes 10pF. The capacitance of the proto-board connecting strip is 5pF. A final 5pF is contributed by the bonding pad capacitance and capacitance associated with the actual OTA circuit within the IC package. This increased value of load capacitance will result in a lower unity gain bandwidth than that predicted using SPICE.

The unity gain bandwidth was much lower than expected, even considering the reduction by a factor of two caused by increased load capacitance. Fig.3.2 predicts a 200kHz bandwidth with a 10pF capacitive load. One would therefore expect to measure a 100kHz bandwidth with the 20pF load capacitance of the test apparatus. The difference by a factor of three may be explained, to a large extent, by errors in modelling resulting from the limited process information used in the extraction of SPICE level 1 parameters. Furthermore, OTA input transistors operate near the weak inversion limit with the bias currents used for these measurements. SPICE level 1 is unable to model sub-threshold behavior and will overestimate the transconductance of the input devices, resulting in an inflated unity gain bandwidth. This point is illustrated by calculating the unity gain bandwidth of the OTA using equation 2.12, the DC gain of the amplifier, and equation 2.10, the output conductance of one half of the cascode output stage.

$$f_{UGB} = \frac{v_{out}}{v_{in}} \frac{g_{out}}{2\pi C_1} = \frac{g_{m3}}{2\pi C_1} \quad (eq.3.4)$$

Unity gain bandwidth is directly proportional to the transconductance of the input transistor T3. Any error in

<i>parameter</i>	<i>measured value</i>	<i>units</i>
<i>Unity Gain Bandwidth</i>	30	<i>kHz</i>
<i>Common Mode Rejection Ratio</i>	61	<i>dB</i>
<i>Power Supply Rejection Ratio</i>	<i>see photo</i>	
<i>Slew Rate</i>	$\pm .08 - .06$	<i>V/μs</i>

Fig. 3.8b AC Characteristics
($I_p = 1.5\mu A$, $I_c = 47\mu A$, $C_l \doteq 20\mu F$)

calculating the gain of this device will be reflected in the unity gain bandwidth calculation. This inability to accurately model the OTA has led to an overestimation of its bandwidth. A photograph of the small signal response of the OTA at a frequency somewhat larger than the unity gain frequency is shown in fig.3.9a.

The common mode rejection ratio measurement was made by varying both inputs with a common signal and measuring the output. In the ideal case no effect would be seen at the output. At high frequency this figure drops as a result of capacitive coupling between the input and output stages. Photographs showing the power supply rejection ratio are shown in Fig.3.10a. The reference input level along with the observed output spectrum are included for both negative and positive rail measurements. In both cases the rejection ratio at DC is 50dB or better, but this falls off towards higher frequencies. The positive power supply is more susceptible to interference than the negative. This can be explained by the fact that both current references in the OTA depend on p-channel current mirrors, which are tied to the positive rail.

The observed slew rate was asymmetric. Depending on the direction of the output voltage waveform, different slew rates were measured. (see fig.3.9b) This indicates that the p-channel current mirrors have higher gain than predicted, and therefore a higher current can be provided from the positive power supply than from the negative. This hypothesis is supported by the negative offset voltage. From the slew rate measurement the estimated value of load capacitance in the test set-up can be substantiated. Knowing the maximum value of current the OTA can supply is related to the input bias current I_p along with the measured slew rate, a value of capacitance can be easily calculated.

The unity gain bandwidth of the OTA was measured at a number of frequencies. The results of these measurements are plotted in

in (a)

out .2v/div.
5μs/div.

in (b)

out 1v/div.
20μs/div.

Fig. 3.9a. Unity-Gain Small-Signal Response

b. Slew-Rate Limited Response

ref

out

(a)

10 dB/div.

5 kHz/div.

ref

out

(b)

Fig. 3.10a Positive Power-Supply Rejection
b. Negative Power-Supply Rejection

fig.3.11. By varying the current it is possible to tailor slew rate, gain or bandwidth for different applications or requirements. An important consideration in doing this is that the amplifier does not become unstable. The unique characteristics of the OTA allow this to be done over a wide range of currents without worry. Over the indicated range instability was not even approached, as confirmed by the absence of ringing and overshoot in the unit step response.

It is interesting to note the relationship between bandwidth and branch current in the OTA. The slope of the curve falls somewhere in between the linear relationship and the square root relationships which were postulated in chapter 2 for operation in weak and strong inversion respectively. There is no sudden transition from strong to weak inversion as current is reduced. Rather, a transition zone exists where the MOS transistor's characteristics are not accurately modelled with either of the two mathematical descriptions. In this particular case, it can be seen that the devices are operating in this region where neither model applies. As current is reduced, the slope of the graph increases as devices come closer to true weak inversion operation.

A final note concerning power dissipation: Since all branch currents are referenced to I_p , one would assume that power could be calculated very easily by multiplying branch current by six branches by the supply voltage. For the 5um OTA measured here this is indeed the case. However, for short channel processes power consumption will turn out to be somewhat higher than originally expected. This is a result of gain in the current mirrors due to the poor output conductance of short channel devices. The same argument applies to slew rates. Normally, given a load capacitance and reference current, slew rate could be calculated. However, output branch current may be unexpectedly large and a corresponding difference in slew rate will be seen.

In that it demonstrated the validity of the design and its

predicted performance, the OTA test chip was generally a success. The use of relatively large devices throughout the circuit made possible a thorough academic study, although some difficulties were created. The resulting high output impedance, for example, was a problem in the measurement of DC open loop gain. Large devices also made the unity gain bandwidth somewhat low for an audio amplifier. However, this is a direct result of the approach taken in the design of the OTA test chip, and does not invalidate the general principles for the design of operational amplifiers for low power switched capacitor filters discussed earlier. Shorter channels, such as those that could be attained in a VLSI process, will give much better gain-bandwidth products. The OTA design has been shown to function using gate lengths of 10um, but it is in future VLSI circuits, such as the balanced switched capacitor biquad described in the next two chapters, that this design is expected to show its advantages to the fullest.

Fig. 3.11 Unity-Gain Bandwidth
vs. Bias Current

4.0 DIFFERENTIAL SWITCHED CAPACITOR CIRCUITS

The problems encountered in realizing analog circuits with a VLSI technology are manifold. In addition to a general degradation in device characteristics with respect to the technologies most commonly used in analog integrated circuits, there is an attendant drop in supply voltages. Considering this fact alone, it can be seen that available dynamic range will be diminished. Another limitation to the use of small geometry devices is that both shot and thermal noise tend to be higher. Short channel devices also tend to be more susceptible to external sources of noise, as a result of larger parasitic effects. The combination of all these contributions to total noise produces a further reduction to the dynamic range available to the analog designer. In the transition from LSI to VLSI analog circuits, dynamic range will suffer from both a higher noise floor and reduced voltage supply range.

It is not possible to increase the dynamic range merely by boosting the power supply voltage. Breakdown voltages in VLSI devices are low as a result of the extremely high potential gradients across very small features. Clearly, dynamic range will have to be improved on the low end, by improving the noise performance of the circuit.

4.1 BALANCED TOPOLOGIES

A method of reducing induced noise in a wide variety of circuits has been known for some time. Instead of identifying a signal as the absolute voltage present at some point with respect to ground, it is redefined as the difference between two voltages. This is termed a differential signal. If, in two identical halves of a signal conditioning circuit, both components of a differential signal are treated exactly the same, they should

both pick up equal amounts of interference from externally coupled noise sources. The difference between the two signal components should remain unchanged, so that the effects of fed-in noise will be greatly reduced. Any noise originating in one or the other identical halves of the circuit will not be eliminated in this manner, since independent noise sources are uncorrelated. The differential technique is only effective in reducing common-mode noise. A further advantage of this differential technique is that the effective maximum signal level is doubled, adding an extra 6dB to the circuit's dynamic range.

There are several possibilities in transforming a single-sided switched capacitor circuit into a fully balanced structure. Only those single-sided circuits utilizing integrators with fixed virtual grounds and stray-free switched capacitors will be considered here. A transformation common to all the topologies that will be considered is shown in fig.4.1. The single output operational amplifier with a single integrating node is transformed into a double-output amplifier, with outputs of opposite polarities, for use in balanced SC structures. This is called a differential-in differential-out integrator. With this integrator, virtual grounds are no longer fixed, although they must remain at a voltage equal to each other due to feedback through the capacitors. The common-mode voltage on the input of the differential op-amp is set by the common-mode output voltage of the preceeding stage. Furthermore, since it is uniquely the differential output voltage of the integrator which is sampled, the overall switched capacitor circuit may be unstable to common-mode perturbations. The dual output op-amp must therefore have some form of internal common-mode feedback to maintain a zero common-mode output voltage. Otherwise, there would be nothing to hold average potentials in the circuit within the linear regions of operation of the amplifiers themselves. In the following discussion on circuit topologies, it will be assumed that common-mode voltages throughout the circuit are zero, and that it is the amplifiers themselves which insure stability in this respect.

Fig. 4.1 Op-Amp Transformation

Fig. 4.2 Simple Transformation of SC Integrator

Four switching schemes that may be used to transform single-sided switched capacitor circuits utilizing stray-free integrators will now be described. The first of these was introduced by Hsieh et. al. [12] and consists of two independent circuits.

4.1.1 SWITCHING SCHEME 1 : NO INTERCONNECTION

This is the simplest imaginable configuration for a balanced SC circuit and yet it retains the noise cancellation properties. In fig.4.2a a single-sided stray-free integrator is shown. The transformed integrator for use in balanced circuits is shown in fig.4.2b. The transfer function can be determined through charge conservation considerations.

$$V_{out,n}^{+} = V_{out,n-1}^{+} - aV_{in,n}^{+} \quad (\text{eq.4.1})$$

$$V_{out,n}^{-} = V_{out,n-1}^{-} - aV_{in,n}^{-} \quad (\text{eq.4.2})$$

$$\begin{aligned} \text{define: } V_{out} &= V_{out}^{+} - V_{out}^{-} \\ V_{in} &= V_{in}^{+} - V_{in}^{-} \end{aligned}$$

$$\therefore V_{out,n} = V_{out,n-1} - aV_{in,n} \quad (\text{eq.4.3})$$

taking Z transforms:

$$\frac{V_{out}}{V_{in}} = \frac{-az}{z-1} \quad (\text{eq.4.4})$$

The resulting transfer function is identical to that of the single-ended integrator of fig.4.2. Any switched capacitor circuit could be directly transformed without any change in frequency response. However, this circuit would require a single-ended-to-differential converter on the input, and a differential-to-single-ended one on the output. If the input converter were not used, i.e., the signal input was to one side only, the full dynamic range capability of the structure would go unused. The output converter is needed to null out the common-mode noise component. Perhaps, with a transfer of information between the two halves of the circuit, the opposite signals would be self balancing, and the input and output conditioning requirements could be made less stringent.

4.1.2 SWITCHING SCHEME 2 : PRECHARGED SCs

Instead of simply discharging the switched capacitors during the odd clock phase as was done with the first configuration, it is possible to precharge them with the other input voltage. The correct polarity is maintained because v_{in-} is now coupled through to v_{out+} through an inverting stray-free switched capacitor and vice versa. No additional components are required. This circuit is shown in fig.4.3, and is driven by the same clocks as that in fig.4.2b.

$$V_{out,n}^{+} = V_{out,n-1}^{+} - aV_{in,n}^{+} + aV_{in,n-1/2}^{-} \quad (\text{eq.4.5})$$

assuming v_{in} is sampled and held:

$$V_{in,n-1/2}^{-} = V_{in,n-1}^{-} \quad (\text{eq.4.6})$$

Fig. 4.3 Precharged SCs

Fig. 4.4 Post-discharged SCs

$$\therefore \frac{V_{out}}{V_{in}} = -a \frac{z+1}{z-1}$$

(eq.4.7)

Equation 4.7, the differential transfer function, represents the bilinear transform of a simple, continuous time integrator. This is very useful in the synthesis of switched capacitor filters because it allows the designer to use readily available analog filter-design packages. The only published example of a stray insensitive bilinear switched capacitor for use in two-phase single-ended circuits [13,14] requires two separate switched capacitors. Yet the equivalent balanced circuit seen here has the same number. As an additional benefit, the sizes of the sampling capacitors can be roughly halved relative to those required in the circuit of fig.4.2b to realize the same transfer function. The only real disadvantage in making this change is that the input voltages must be sampled and held over a full clock period. It is no longer necessary that a single-ended-to-differential converter be used on the input since charge transfers between the two halves of the circuit tend to balance the differential signals.

4.1.3 SWITCHING SCHEME 3 : POST DISCHARGED SCs

In the second topology both input voltages were sampled during each clock phase while the charge was transferred through the integrating nodes only once each period. If this were reversed and the sampling capacitor were switched between both virtual grounds, the differential integrator's structure would be that shown in fig.4.4. It is clear that the output voltages can now change twice each period. Two charge-transfer equations must therefore be written to fully describe the periodic behavior of the circuit. The output is of interest during phase 0.

$$V_{out,n}^+ = V_{out,n-1/2}^+ - aV_{in,n}^+ \quad (\text{eq.4.8})$$

$$V_{out,n-1/2}^+ = V_{out,n-1}^+ + aV_{in,n-1}^- \quad (\text{eq.4.9})$$

Substituting eq.4.9 into eq.4.8 and taking the z transform:

$$\frac{V_{out}}{V_{in}} = -a \frac{z+1}{z-1} \quad (\text{eq.4.10})$$

This circuit also realizes the bilinear transform. Unlike the previous one, though, it needs no sample and hold on the input. An analog signal which does not approach the Nyquist limit can be fed directly to the switched capacitors. Unfortunately, it will require a sample and hold on the output, unless it is being fed into another integrator of the same type. The unwanted transfer function which appears during phase 1 is effectively time-multiplexed with the bilinear transfer function and must be eliminated at the output. An additional though minor feature of this structure is that it saves power. Instead of dumping the charge stored in a switched capacitor to ground, it is saved and eventually passed on through an integrating node. This could be significant in micropower circuits.

4.1.4 SWITCHING SCHEME 4 : TRUE BILINEAR

If switching to ground is eliminated entirely, and the input sampling of the second configuration is combined with the alternating virtual ground sequence of the third, we would have the circuit of fig.4.5. Now, no matter which position the switches are in, the circuit remains electrically indistinguishable. An effective doubling of the sampling

frequency is implied, although the frequencies of the individual phases remain unchanged. Only one charge-transfer equation is necessary in calculating the circuit's transfer function, i.e. one describing the transition from one phase to the next. Note that the time delay implied by z here is half that of previous examples.

$$V_{out,n}^{+} = V_{out,n-1}^{+} - aV_{in,n}^{+} + aV_{in,n-1}^{-} \quad (\text{eq.4.11})$$

$$\therefore \frac{V_{out}}{V_{in}} = -a \frac{z+1}{z-1} \quad (\text{eq.4.12})$$

This circuit requires neither a sample and hold at the input nor the output, since it achieves all the necessary charge transfers in a single instant. The problems of interfacing to the outside world are also reduced, as the circuit is self-balancing. An input single-ended-to-differential converter is superfluous. In comparison to the first balanced integrator configuration, a fourfold reduction in switched capacitor size can be expected due to the combined effects of a double charge transfer to the integrating node and the doubled sampling frequency. Alternately, the clock frequency can be halved to get the same effective sample rate as before, and there is a twofold size reduction. A quick comparison of the four topologies is presented in fig.4.6. Clearly, the fourth circuit offers the most convenient interface requirements as well as the most efficient use of the two switched capacitors.

4.2 FILTER SYNTHESIS USING THE BILINEAR TRANSFORM

Having now a balanced switched capacitor structure which realizes the bilinear transform, an SC filter design methodology can be

Fig. 4.5 True Bilinear Balanced SC Integrator

described [4,15]. The bilinear transform (eq.4.13) is a mapping between the continuous-time "s" plane and the sampled-data domain "z" plane. The mapping which relates every point in the s-plane to one in the z-plane without any amplitude or frequency distortion is $z = \exp(j\omega T)$. If it were practical, continuous-time filters could be transformed to sampled data filters by substituting this relation into the s-domain transfer function describing the desired response. However, the substitution of $s = \ln(z)/T$ into a rational function of s would produce an irrational function of z, one that could not be realized by a finite network of switched capacitor integrators. No transform between the two planes exists which converts rational s-domain functions to rational z-domain functions without any amplitude or frequency distortion.

$$s = \frac{2}{T} \frac{z-1}{z+1}$$

(eq.4.13)

The vertical axis in the s-plane represents the locus of all possible frequencies, $j\omega$. In the z-plane the corresponding locus is a unit circle centered on the origin. The bilinear transform maps every point on the s-plane's vertical axis to a unique point on the z-plane's unit circle. There is a frequency distortion inherent in this transformation, in that the aliasing of frequencies higher than $2/T$ is not reflected, and that frequencies approaching infinity are squeezed into the region around the point $(-1,0)$. The distortion resulting from using the bilinear transform to map a continuous-time frequency ω to a discrete time frequency ω' is described by the following equation [4]:

$$\omega' = \frac{2}{T} \tan^{-1}(\omega T/2)$$

(eq.4.14)

	INTEGRATOR			
	1	2	3	4
<i>single ended to differential converter reqd. on input</i>	YES	NO	NO	NO
<i>input sample and hold reqd.</i>	NO	YES	NO	NO
<i>output sample and hold reqd.</i>	NO	NO	YES	NO
<i>differential to single ended converter reqd. on output</i>	YES	YES	YES	YES

Fig. 4.6 Comparison of 4 SC Integrators

The nonlinearity of the relationship between the two frequencies is evident from the graph of eq.4.14 in fig.4.7.

The key to design using the bilinear transform is "prewarping" the original frequency specifications outlining the required response. The cutoff frequency of a low-pass filter, for example, would be prewarped using eq.4.14 before proceeding with the synthesis of a continuous-time transfer function. Then the bilinear transform is applied, producing a transfer function in z with an effective cutoff frequency at the point originally desired, as a result of the distortion inherent in the bilinear transformation. In this way, filter synthesis and optimization techniques developed for continuous-time circuits can be applied to the design of switched capacitor filters.

4.3 ANALYSIS OF SWITCHED CAPACITOR CIRCUITS

In chapter 5 a design of a balanced switched capacitor filter is presented. For such design, methods are required to analyze the frequency domain and/or time domain performance of the filter. Some such methods are presented here.

Before committing a circuit design to silicon, a designer normally wants some assurance that the design is valid and the circuit will work as expected. One way of checking this is to construct and perform measurements on a laboratory prototype built up of discrete components. There are several problems with this approach. It is costly and time-consuming to build, debug, and test complex circuits in the lab. Furthermore, it is frequently impossible to duplicate the characteristics of IC devices with discrete transistors. For these reasons computer simulations have become the dominant methods of verifying IC designs.

When switched capacitor circuits were first recognized as the solution to monolithic analog signal processing requirements, there were no simulation packages available which could handle

Fig. 4.7 Frequency Compression
of Bilinear Transform

their time variant nature. Now, as the technology and underlying theory have matured, more and more software packages specifically dedicated to the simulation of SC circuits have become available. One of the earliest and most well known of these is DIANA [16], produced by the ESAT lab of Katholieke Universiteit, Belgium. Many others have followed, including SCOP [17] by F.Brglez of BNR, SWITCAP [18] by Y.Tsividis of Columbia University, and SCYMBAL [19]. from CNET, France. In general, these programs make heavy demands on computer resources and are geared to a single purpose, that of analysing SC circuits.

An alternate approach is available to those who do not have access to a computing facility which supports one of the dedicated switched capacitor analysis packages. A switched capacitor can be modelled with frequency dependant resistors for a frequency domain analysis [20]. Using then a readily available continuous time circuit analysis package, such as SPICE, and substituting the appropriate SC equivalent circuits, the frequency response of a switched capacitor circuit can be analysed without the aid of a dedicated program. In the following section the decomposition of a switched capacitor two-port into an analog, continuous-time equivalent is described, and the specific result for the balanced bilinear switched capacitor filter of this thesis is derived.

4.3.1 SWITCHED CAPACITOR ANALOG EQUIVALENT CIRCUITS FOR FREQUENCY DOMAIN ANALYSIS

Consider the switched capacitor two-port in fig.4.8a. This is effectively the true bilinear configuration of fig.4.5 turned on its side. Since port X samples the voltage v_1 during phase 1 only, and port Y samples the voltage v_2 during phase j, the charges Q_1 and Q_2 entering the two-port are dependant only on the voltages $v_{1,i}$ and $v_{2,j}$ in other words, the voltages present at the ports during the sampling instants. The difference equations for the charges Q_1 and Q_2 entering each port, as functions of the

voltages present at the ports, can be transformed to the z-domain to form the following relation:

$$\begin{bmatrix} Q_{1,i}(z) \\ Q_{2,j}(z) \end{bmatrix} = \begin{bmatrix} c_{11} & c_{12} \\ c_{21} & c_{22} \end{bmatrix} \begin{bmatrix} V_{1,i} \\ V_{2,j} \end{bmatrix}$$

(eq.4.15)

The c_{11} , c_{12} , c_{21} , and c_{22} terms form the C-matrix. In addition to relating port voltages to transferred charge as a function of the size of the switched capacitor, these terms may also contain delay, if i is not equal to j and the two charge transfers occur during different time instants. An equivalence between the switched capacitor two-port and a hypothetical continuous time two-port can be made by equating the integrated current flowing into each port of an analog two-port (fig.4.8b) to the charge transfer equation 4.15.

$$\begin{bmatrix} Q_{1,i}(s) \\ Q_{2,j}(s) \end{bmatrix} = \frac{1}{s} \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} V_{1,i}(s) \\ V_{2,j}(s) \end{bmatrix}$$

(eq.4.16)

equating the two charge matrices:

$$\begin{bmatrix} y_{11}(s) & y_{12}(s) \\ y_{21}(s) & y_{22}(s) \end{bmatrix} = s \begin{bmatrix} c_{11}(z) & c_{12}(z) \\ c_{21}(z) & c_{22}(z) \end{bmatrix}$$

(eq.4.17)

$$; z = e^{j\omega T} ; s = j\omega$$

Equation 4.17 remains valid only as long as the frequency ω is below the Nyquist limit. Since frequencies in the SC circuit are also restricted to this same limit to avoid aliasing, the equivalent circuit is valid over the entire usable bandwidth.

(a)

(b)

Fig. 4.8 a. SC 2-Port

b. Analog Continuous Time
Equivalent

The four admittances can be calculated and substituted for the switched capacitor as shown in fig 4.8b. The frequency response analysis is then performed as if the circuit was time-invariant for any range of frequencies up to $1/2T$. Where appropriate, a term $\sin(\omega T/2)/(\omega T/2)$ should be introduced to account for the amplitude distortion resulting from sampled and held signals.

4.3.2. ANALOG EQUIVALENT FOR BALANCED BILINEAR SWITCHED CAPACITOR

The basic switched capacitor unit in the balanced circuit topologies previously discussed has been composed of two separate switched capacitors. For the purposes of deriving an analog equivalent these two can be considered as part of the same SC two-port (fig.4.9). The charge transfer equations can be written as follows:

$$Q_{1,n} = Q_{1,n-1} + CV_{1,n} - CV_{2,n-1} \quad (\text{eq.4.18})$$

$$Q_{2,n} = Q_{2,n-1} + CV_{2,n} - CV_{1,n-1} \quad (\text{eq.4.19})$$

Equations 4.18 and 4.19 are transformed to the z-domain to derive the C-matrix in the form of equation 4.15:

$$\begin{bmatrix} Q_1(z) \\ Q_2(z) \end{bmatrix} = \begin{bmatrix} \frac{C}{z-1} & \frac{-Cz^{-1}}{z-1} \\ \frac{-Cz^{-1}}{z-1} & \frac{C}{z-1} \end{bmatrix} \begin{bmatrix} V_1(z) \\ V_2(z) \end{bmatrix} \quad (\text{eq.4.20})$$

To transform the two-port to the continuous-time equivalent as per equation 4.17, there are two complex math identities to

Fig.4.9 Balanced Bilinear 2-Port

Fig.4.10 Balanced Bilinear SC Equivalent

Circuit ;
$$R = \frac{T}{C} \frac{\tan(\omega T/2)}{(\omega T/2)}$$

solve:

$$y_{11} = y_{22} = \frac{j\omega C}{e^{j\omega T} - 1} = \frac{C}{T} \frac{(\omega T/2)}{\tan(\omega T/2)} + j\omega C/2 \quad (\text{eq.4.21})$$

$$y_{21} = y_{12} = \frac{j\omega C e^{-j\omega T}}{e^{j\omega T} - 1} = -\frac{C}{T} \frac{(\omega T/2)}{\tan(\omega T/2)} + j\omega C/2 \quad (\text{eq.4.22})$$

There are frequency-dependant resistors and capacitors in each of the four admittances y_{11} , y_{12} , y_{21} , and y_{22} . The implimentation of frequency-dependant elements may present a problem depending on the circuit simulation package used. Appendix C describes how this is accomplished in SPICE. The analog equivalent circuit for the balanced switched capacitor is shown in its entirety in fig.4.10. Note that the orientation has been changed to simplify the derivation. In previous discussions the two switched capacitors were rotated 90 degrees with respect to the way they are drawn here.

4.3.3 TIME DOMAIN ANALYSIS OF SC CIRCUITS

Switched capacitor circuit designs can also be verified in the time domain. A unit impulse can be fed into the input and the output observed as a piece-wise linear staircase function. Each discrete voltage level corresponds to one element in the power series representation of the z-domain transfer function.

Normally, these transfer functions are expressed as numerator and denominator if it is an IIR filter, but when the implied division is carried out an infinite series in z will result, with each successive term representing a further unit of delay. In this way the original transfer function for which the circuit was designed is reproduced by the computer simulation. If frequency response is desired, the unit impulse response can be

fourier transformed. Implementation of this method of analysis in SPICE is discussed in Appendix C.

Time domain analysis of SC circuits represents a departure from the more accepted forms of circuit analysis. Most designers would rather work in the frequency domain where, after all, the desired behavior of filters is most readily observed. However, many switched capacitor filters are designed by merely transforming well known and understood continuous time functions into the z-domain. One can therefore be confident that a circuit, which has an impulse response described by the z transfer function, meets the continuous-time frequency specification. Why then proceed with a complicated frequency-domain analysis when a simple time-domain simulation would suffice? In many cases, the time-domain analysis would be adequate; and the designer would no longer be concerned with s- to z-plane mappings and the associated mathematical complexities.

5.0 BALANCED SWITCHED CAPACITOR BIQUAD : A VLSI DESIGN EXERCISE

In this chapter the design and layout of a balanced switched capacitor biquad in a CMOS VLSI process is presented. Biquadratic cells are often used as building blocks in higher order filters [4,21]. The operational amplifier concepts discussed in chapters 2 and 3 are brought together with the balanced circuit ideas and switched capacitor filter synthesis methodologies of chapter 4, to design a low-power biquadratic filter. The circuit occupies a small area and is intended to maximize voiceband filter performance in a short channel VLSI technology.

A frequency response specification and clock frequency for the biquad will first be selected. Then, filter synthesis proceeds in determining the necessary capacitor ratios. These will be verified with time- and frequency-domain simulations in SPICE. Next, a practical problem to the implementation of a balanced circuit will be introduced, namely, that of common mode stability. Since each stage of the circuit communicates only the differential component of its output voltage to the next stage, the common mode voltage is not constrained by the negative feedback of the loop. This problem will be clearly defined and a practical solution in the context of balanced SC circuits proposed.

Finally, the layout of the biquadratic cell in a CMOS VLSI process will be shown. Several aspects of the process which require special consideration for analog circuitry will be discussed. Finally, the computer-generated plot of the circuit layout is presented along with a tabulation of the circuit's characteristics and expected performance.

5.1 FILTER SYNTHESIS

As an example of filter synthesis using the balanced switched-capacitor integrators, a second-order butterworth low-pass filter will be designed. The cutoff frequency is positioned in the audio band, at 2kHz with a sampling frequency of 20kHz (clock frequency of 10kHz). This implies that the actual period of each of the two phases will be 100us. A continuous-time circuit which realizes a low-pass transfer function and which can be readily transformed into a stray-free switched capacitor circuit is shown in fig.5.1. Each resistor in the circuit is replaced by a switched capacitor of type 4 and the entire circuit made fully differential. (fig.5.2)

Several switches are redundant and have been eliminated in the final circuit. The inverter in the continuous-time circuit is no longer needed because signal inversion is accomplished by merely reversing the connections to the switched capacitor resistor at this point. The z-transfer function of the circuit can be determined by reducing the block diagram of fig.5.3. Each block represents one switched capacitor and contains the z-transfer function of a bilinear switched capacitor, abbreviated here as 'F'.

$$\frac{V_{out}}{V_{in}} = \frac{-abF^2}{1 + dF + cbF^2} \quad (eq.5.1)$$

$$; F = \frac{z+1}{z-1}$$

$$\frac{V_{out}}{V_{in}} = \frac{-ab}{1+d+cb} \frac{z^2 + 2z + 1}{z^2 - \frac{(2-2cb)z}{1+d+cb} + \frac{1-d+cb}{1+d+cb}} \quad (eq.5.2)$$

Fig. 5.1 Continuous Time Low Pass Filter

Fig. 5.2 Balanced Switched Capacitor Biquad

Fig. 5.3 Determination of Biquad Transfer Function by Block Diagram Reduction

To determine the capacitor ratios a, b, c, and d, equation 5.2 is compared to the prewarped bilinear transformed continuous-time domain transfer function of a second order Butterworth low-pass filter:

$$\frac{V_{out}}{V_{in}} = \frac{w_p^2}{s^2 + 1.414w_p s + w_p^2} \quad (\text{eq.5.3})$$

where w_p = cutoff frequency in radians/second

The bilinear transform is substituted into equation 5.3 to produce a z-domain transfer function:

$$\frac{V_{out}}{V_{in}} = \frac{A(z^2 + 2z + 1)}{z^2 - \frac{(8 - 2w_p^2 T^2)z}{4 + 2.828w_p T + w_p^2 T^2} + \frac{4 - 2.828w_p T + w_p^2 T^2}{4 + 2.828w_p T + w_p^2 T^2}} \quad (\text{eq.5.4})$$

$$\text{where } A = \frac{w_p^2 T^2}{4 + 2.828w_p T + w_p^2 T^2}$$

Note that equation 5.4 is of the same form as equation 5.2. This is reassuring. Next, the desired cutoff frequency is prewarped by equation 5.5 to compensate for the distortion of the frequency plane inherent in the bilinear transform.

$$w_p' = \frac{2}{T} \tan(wT/2)$$

(eq.5.5)

Finally, the sampling period of .05ms and the warped cutoff frequency of 12996 rad/sec are substituted into equation 5.4. By equating the terms of equation 5.3 to the resultant transfer function, the actual capacitor ratios can be determined. There remains an extra degree of freedom in the synthesis which can be put to good use by equating the levels at the outputs of each integrator, thereby maximizing the biquad's dynamic range. The transfer function of the sampled analog Butterworth low-pass filter and the capacitor ratios which implement it are thus found to be:

$$\frac{V_{out}}{V_{in}} = .0675 \frac{z^2 + 2z + 1}{z^2 - 1.143z + .4129}$$

$$a=b=c=.3251$$

(eq.5.6)

$$d=.4594$$

5.2 SIMULATION OF THE BIQUAD

The balanced biquad circuit has been simulated with both methods described in the previous chapter. Appendix C contains the actual computer printouts as well as particular details as to how SPICE was used. The frequency domain analysis by the method of substitution of continuous-time switched capacitor equivalents shows a maximally flat second-order low-pass response with a cutoff frequency of 2kHz, exactly what had been synthesized.

In the time-domain analysis, the staircase characteristics of the impulse response can be clearly seen. This or, for that matter, any other sampled analog impulse response can be verified by dividing the theoretical transfer function and comparing the series of values with each discrete voltage in the staircase output. Transfer functions describing the overall biquad output

relative to its input, as well as the output of the first integrator V_{out} , are reduced to power series form:

$$\begin{aligned}\frac{V_{out}}{V_{in}} &= .0675 \frac{z^2 + 2z + 1}{z^2 - 1.143z + .4129} \\ &= .0675 + .2122z^{-1} + .2821z^{-2} + .2349z^{-3} + \dots\end{aligned}\quad (\text{eq.5.7})$$

$$\begin{aligned}\frac{V_{out}}{V_{in}} &= .3032 \frac{z^2 + 2z + 1}{z^2 - 1.143z + .4129} \\ &= .3032 + .5374z^{-1} + .3767z^{-2} + .2087z^{-3} + \dots\end{aligned}\quad (\text{eq.5.8})$$

It can be seen that the computer simulations produced identical sequences to those derived theoretically. That the biquad design produces the desired response has been doubly verified.

In general, computer simulations would not be very useful if they were used only to analyze the behavior of ideal circuits, as in this example. The technique is indispensable, however, in determining the effects of parasitic elements which would make a pencil-and paper analysis impossibly complicated. Such is the case with monolithic switched-capacitor filters, where stray capacitances, switch resistances, low op-amp gain, temperature sensitivities and a host of other non-ideal effects can cause actual circuit performance to deviate significantly from that expected. With the capability to simulate by computer, the designer can account for all these effects and adjust component values accordingly, so that the integrated circuit produced is much more likely to be within performance specifications.

5.3 THE COMMON MODE STABILITY PROBLEM

A fuller understanding of the problem of common mode instability would be useful in finding a solution. Generally, an op-amp is designed to have a very low common-mode gain. If both inputs of an open-loop operational amplifier are varied equally, the output will remain at a constant voltage. How then can the common mode output voltage of a complementary output operational amplifier be maintained mid-point between the power supply rails? This voltage can be anywhere within the two power-supply levels, depending on the balancing of device parameters, and is highly sensitive to slight process variations. Clearly, some form of negative feedback must be used. The balanced SC circuit, or any other circuit which processes a differential signal independantly of the common-mode signals present, cannot provide this feedback.

For the purposes of filter synthesis or simulation with ideal elements, this aspect of the circuit can be largely ignored. But once a topology in which feedback is used to maintain stability and prevent saturation is realized as a balanced differential circuit, the non-ideal effects of leakage, input bias currents etc. can cause perturbations in common-mode voltages for which the circuit has no means of stabilizing. A method of fixing common mode voltages throughout the circuit, while leaving differential signals unchanged, is required.

To better illustrate the problem, consider the schematics in fig.5.4, showing both a single-output op-amp and a balanced differential output amplifier in resistive feedback configurations. For simplicity, switched-capacitor elements are not used here, but the effects, vis-a-vis common-mode instability are similiar in the two cases. The common-mode gain is assumed near zero and the differential gain near infinity.

Assuming input v_{in} is zero, the differential gain in the single-ended inverting amplifier, in combination with negative feedback, keeps V_{vg} virtually equal to the voltage at the non-inverting input. From this consideration alone, the well known expression

22

OF / DE

(a)

(b)

Fig. 5.4a. Single-Ended Inverting Amplifier
 b. Differential Inverting Amplifier

for gain of an inverting op-amp configuration can be derived:

$$\frac{V_{out}}{V_{in}} = -\frac{R_1}{R_2}$$

(eq.5.9)

Considering now the differential output amplifier of Fig.5.4b, it can be seen that the high differential gain will force the two inputs to be the same voltage, assuming of course, that the amplifier operates within its linear region.

$$V_{vg}^+ = V_{vg}^- = V_{vg}$$

(eq.5.10)

What determines the value of this common-mode input voltage, and the common-mode output voltage? The analysis which follows discusses this problem further. Each individual output voltage can be expressed in the terms of the two input voltages as follows, assuming no input bias currents:

$$V_{out}^+ = V_{vg} - (V_{in}^+ - V_{vg}) \frac{R_2}{R_1}$$

(eq.5.11)

$$V_{out}^- = V_{vg} - (V_{in}^- - V_{vg}) \frac{R_2}{R_1}$$

(eq.5.12)

However, these equations can be merged into one, given the following definitions for differential input and output voltages:

$$V_{out} = V_{out}^{+} - V_{out}^{-}$$

(eq.5.13)

$$V_{in} = V_{in}^{+} - V_{in}^{-}$$

(eq.5.14)

$$\therefore \frac{V_{out}}{V_{in}} = - \frac{R_2}{R_1}$$

(eq.5.15)

All terms of the common-mode voltage V_{vg} conveniently disappear in the expression for the theoretical differential transfer function. The circuit behaves identically to the single output inverting amplifier when considering only the differential signal.

Consider now the common-mode behavior, which can be analyzed using equations 5.11 and 5.12 and the following definitions for common-mode input and output signals:

$$(V_{out})_{c.m.} = \frac{V_{out}^{+} + V_{out}^{-}}{2}$$

(eq.5.16)

$$(V_{in})_{c.m.} = \frac{V_{in}^{+} + V_{in}^{-}}{2}$$

(eq.5.17)

$$\therefore (V_{out})_{c.m.} = V_{vg} - [(V_{in})_{c.m.} - V_{vg}] \frac{R_2}{R_1}$$

(eq.5.18)

It can be seen that the common-mode output voltage is a function

of not only the input common-mode voltage, but also of some arbitrary voltage V_{vg} . Exactly what this voltage may be would depend on the non-zero common-mode gain of the op-amp. In general, it cannot be assumed that V_{vg} lies midpoint between the two power supplies. The possibility that the two outputs will saturate is very likely. If there were some circuitry internal to each op-amp which forced the two output voltages to be complimentary (ie. $V_{out+} = -V_{out-}$) without altering the differential output voltage, the problem would be solved. In terms of equation 5.18, $(V_{out})_{cm}$ would be zero and, assuming that $(V_{in})_{cm}$ came from a similar op-amp, it would also be zero. The voltages V_{vg} at the inverting and non-inverting inputs must then be zero as well. In a circuit using such a zero common-mode output operational amplifier, no common-mode voltages could exist.

To implement this form of common-mode auto-zeroing, an addition must be made to the biquadratic filter as it has been presented up to this point. First, a means of detecting the common-mode signal is required. Secondly, an additional connection to the operational amplifier which controls the common-mode output voltage must be devised. The combination of these two elements must then form a negative feedback loop. A modification to the OTA which allows the independent control of the common-mode output voltage is shown in the schematic of fig. 5.5. Identical p-channel transistors are placed in parallel with the two p-channel cascode driver transistors at each of the outputs. The gates are connected to a single common-mode bias input. Increasing the voltage at this point will decrease the current in both p-channel branches of the output drivers, thereby decreasing the common mode-output voltage of the op-amp. This added connection to the amplifier provides a negative feedback input for control of the common mode.

A number of schemes for the connection of the two outputs to the common-mode bias input could be conceived. The simplest of these is perhaps a simple resistive feedback from both outputs, with some provision for level shifting to maintain proper p-channel bias. The exact form the circuit will take is left open. When

Fig. 5.5 OTA with Common Mode Bias Transistors

the integrated circuit is fabricated, it will be possible to experiment with a number of solutions to the problem of common-mode biasing.

5.4 THE CMOS VLSI PROCESS

The IC process made available for this work by BNR is of an experimental nature. Its ultimate objective is to realize a 1.5 μ m gate-length CMOS technology intended primarily for digital circuitry. This may not be realized with the first batches of wafers processed. Rather a gradual evolution from a standard 5 μ m CMOS technology with several intermediate steps will be carried out. For the balanced switched capacitor biquad, this has several implications. In order to have a functioning chip to test as soon as possible, the biquad should be capable of operation with any of the mask sequences envisaged during the development of the VLSI process. Yet it is costly and inconvenient to produce a different set of masks for each case. One set of masks which can be used in each anticipated revision of the process, has been designed to ensure the greatest possibility of success in eventually receiving a functional chip.

One variant in the process evolution is the minimum gate-length design rule. Initially, the minimum length allowed will be 3 μ m but, as the process is refined, this will be reduced to 1.5 μ m. There are two different masks for the definition of gate polysilicon, one with 3 μ m design rules and the other with real short-channel dimensions of 1.5 μ m minimum. Since the rest of the masks remains unchanged, the overall chip dimensions remain constant for both possibilities and, as a result, the surface area savings of a true VLSI process will not be attained. However, from the point of view of electrical characteristics, the circuit will indeed be a short channel VLSI realization. The process is a good vehicle to test the refinements to analog signal processing circuits discussed in this thesis.

The only area in which changing gate lengths in the balanced biquad circuit will significantly alter its performance, is in the operational amplifiers. Arbitrarily changing gain and output conductances in the OTA could lead to instability. Both a $3\mu\text{m}$ and a $1.5\mu\text{m}$ gate-length OTA have been designed and simulated in SPICE. (see chapter 3 for transistor dimensions and Appendix B for simulations) The differences between the two gate polysilicon masks reflect the changes necessary to maintain stability and minimize voltage offset. Either of these masks will produce an op-amp of sufficient gain and bandwidth to drive the switched capacitor filter at the design clock rate.

Another problem with the process is an uncertainty as to how capacitors will be realized. They will be done in one of two ways (see fig.5.6b and c): either a second layer of polysilicon underneath the gate polysilicon, separated by gate oxide, or a special heavily doped diffusion in the substrate. It would be preferable, from the point of view of capacitor linearity and isolation in a switched capacitor circuit, to have the poly-poly capacitor. Unfortunately, this may not be made available, so the circuit should also be functional with poly-diffusion capacitors.

There is only one mask available for the definition of the capacitor's bottom plate, whether poly or diffusion. In the case of poly-poly capacitors, this mask defines a polysilicon layer and in the case of poly-diffusion capacitors, a doping mask. Some method must be devised so that functional capacitors will be realized independently of the process variation finally chosen. A basic capacitor structure which meets this requirement is shown in fig.5.6a.

A metal line makes contact with the device well and the capacitor poly/doping mask. If the capacitor is of the poly-diffusion type, there will of course be nothing to contact at this point and only the heavily doped p+ diffusion will be connected. In the case of poly-poly capacitors, the bottom plate poly will be contacted as desired and there will be an additional unwanted

Fig. 5.6 a. Capacitor Layout
 b. Poly-Poly Capacitor
 c. Poly-Diffusion Capacitor

device well contact. Since the two levels of polysilicon were present before source/drain diffusions, this device well is not connected to anything else and represents only a slight additional stray capacitance. The capacitor poly is separated from the n substrate by only the gate oxide. This capacitance to substrate is of the same order of magnitude as the poly-poly capacitor itself. For this reason the bottom plate should always be connected to the op-amp outputs as opposed to its virtual grounds. In the layout, metal must always be used to contact the bottom plate. Otherwise proper connection could not be guaranteed with both mask sequences.

5.5 BIQUAD LAYOUT

The biquad was originally laid out as in fig.5.7. This arrangement of components minimizes the lengths of interconnections, thus reducing stray capacitance and saving area. The integrating capacitors are located directly below the operational amplifiers and above the switches. Any connection from virtual ground or op-amp output to the switches is made via the integrating capacitor top plate or bottom plate respectively. This eliminates direct connections from op-amps to switches so that aluminum tracks over capacitor regions are unnecessary. Switched capacitors are located below the switches, once again in the interest of minimizing interconnections. This form of biquad lends itself to the modular construction of higher order filters. Other biquads could be located to the left or right of this one and most of the power-supply connections, clock phases and bias voltages could extend horizontally through each of the cells.

This layout had to be altered in order to fit the available test probe array. The 300um width of the original layout was too large to fit within the rather narrow rectangular area that was available. To make it fit the layout was cut in half along the boundary between the integrating capacitor and the switches. The computer generated plot of the final layout is shown in fig.5.8.

Fig. 5.7 Initial Biquad Layout

Fig. 5.8 Biquad Layout

Fig. 5.9 Pad Designations

The additional stray capacitances incurred along the aluminum tracks connecting the virtual grounds or top plates to the switches may slightly alter the biquad's transfer function. Since the filter is made in a strays-insensitive configuration and the op-amp's gain is quite large, these changes should be minimal.

The capacitors used in the layout are built from number of unit capacitors. It was decided to not to trim these capacitors to achieve the exact ratio. Rather, a slight quantization error would be tolerated so that the capacitor ratios would be completely insensitive to irregularities in fabrication. The ratios $7/16$ and $9/16$ were found to closely approximate the ratios derived in the synthesis procedure. Hence, each integrating capacitor is composed of sixteen unit capacitors while the switched capacitors consist of either seven or nine unit capacitors. In this way, edge or corner capacitances will not affect capacitor ratios, all unit capacitors being identical. Furthermore, these unit capacitors are insensitive to mask misalignments. Fig.5.10 shows a unit capacitor which is perfectly aligned alongside one which is misaligned. The overall effective capacitive area remains the same, as does the number of inside and outside corners and total edge length contributing to the capacitance. The only factors remaining, which would contribute to variations in capacitor ratios, are random defects in the oxide separating the two plates, or non-uniformities in the diffusion concentrations in the case of poly-diffusion capacitors. The error between two poly-poly capacitors depends inversely on the spacing between them and on the absolute value of the capacitance. Since these particular capacitors are all close together and cover a significant amount of area, the error in ratios and, ultimately, the biquad transfer function should be minimal.

To conclude this chapter describing the balanced switched capacitor biquad IC, the salient features of the circuit are tabulated as well as its anticipated performance, in fig.5.11.

Fig. 5.10
Unit Capacitor

(a) perfectly aligned

(b) misaligned

FILTER SPECIFICATIONS

<i>Filter Type : 2nd Order Butterworth LP</i>
<i>Cutoff Frequency : 2kHz</i>
<i>Clock Rate : 10kHz (two-phase)</i>
<i>Unit Capacitor : .037 pF</i>
<i>Switch On Resistance : 20 kΩ</i>
<i>Total Area : .197 mm² (305 mil²) (excluding bonding pads)</i>
<i>Active Area : .137 mm² (211 mil²)</i>
<i>Power Consumption (with +2.5/-2.5 volts)</i> <i>3 μm : 70 μw</i> <i>1.5 μm : 124 μw</i>

Fig. 5.11

6.0 SUMMARY

The design of two analog integrated circuits has been described in this report. The first, an operational amplifier which features low power and a novel frequency compensation scheme intended for use in switched capacitor circuits, was actually fabricated and tested. The second, a complete switched capacitor biquadratic filter, has been laid out in a CMOS VLSI process but has not yet been fabricated.

A comprehensive design, including derivation of theoretical formulae and verification by computer simulation, has been carried out for each of the two circuits. In the case of the single amplifier, measurements were made which serve to confirm the original design.

The operational amplifier, which has its dominant, frequency compensating pole at the output instead of some internal node, gave good performance. The amplifier features a DC differential gain greater than 94dB and an input offset voltage of 20mV. The common-mode input-voltage range extends from below V_{ss} to 3.8 volts with ± 5 volt supplies. The output voltage, with no resistive load, can approach the supplies to within .1 volt. An extremely low power consumption of 30uW, for single-ended output, was observed. Compared to recently published examples of internal op-amps, in which an all-enhancement NMOS device consumed 15mW [23] and depletion load NMOS consumed 1.4mW [24], the OTA is much better suited to volume applications in VLSI circuits. As for real estate requirements, the other amplifiers occupy $.32\text{mm}^2$ and $.16\text{mm}^2$ respectively compared to $.12\text{mm}^2$ for the 5um process OTA and $.0075\text{mm}^2$ for the 1.5um process OTA. If all dimensions in the experimental 1.5um gate length process were reduced to 1.5um, an even greater VLSI circuit density could be realized. It is mainly with respect to unity-gain bandwidth that the OTA studied here does not compare well with other examples. Compared to 5MHz and 1.8MHz respectively for the published circuits, the 5um OTA which

was fabricated had only a 40kHz unity gain bandwidth. If the amplifier was driving an internal capacitive load instead of the 20pF load of the test circuit, this figure would be an order of magnitude larger.

A better measure of how the OTA unity-gain bandwidth compares with those of the published circuits would be to scale OTA bias current up until a comparable bandwidth is reached. Previous discussions have indicated that unity-gain bandwidth increases as the root of the current in the output stage of the OTA. Consider the 400kHz bandwidth of an OTA driving an on-chip load. A twenty-fold increase in bias current would be required to extend the bandwidth to 1.8MHz. Power consumption would be 170uW, or approximately one-eighth that of the depletion mode NMOS amplifier. The performance of the short-channel OTA is expected to be even better.

A similar amplifier design was incorporated into the biquadratic filter layout. A total of twenty transmission gates, twelve capacitors (composed of 124 unit capacitors) and two operational amplifiers were required for this balanced second-order low-pass filter. The circuit has a total area, including interconnections, of $.197\text{mm}^2$ and its projected power consumption is 78uW. It is expected to give very good noise performance, especially with respect to external sources.

6.1 FURTHER RESEARCH

The most pressing task will be to test the balanced biquad chip once it has passed through fabrication. Measurements should be made to verify its performance, both the overall accuracy of the filter's frequency response as well as the behavior of individual components such as capacitors, switches and op-amps.

Before the chip can be made functional, a method for providing common mode feedback must be devised. Either the solution

described in chapter 5 or some entirely different circuit may be employed. In either case, the common-mode bias input that has been provided on the integrated circuit will be the ultimate means of controlling common-mode output voltage. Different time constants in the common-mode feedback loop and their effects on the overall transfer function of the filter should be investigated. At first glance, it would seem that signals in the balanced circuit should be independent of their common-mode level, since they are all differential in nature. However, through experimentation it may be found that a particular common-mode feedback circuit and loop time-constant optimizes filter performance.

Another area for further study is the analysis of capacitor tolerances. Since the capacitor sizes in the biquad are much smaller than those normally used for production circuits, some probabilistic variations in transfer function from chip to chip, as a result of random defects in capacitors, may be observed. Also, if circuits with both poly-poly and poly-diffusion capacitors become available, a comparison between the two methods can be made. One can expect a higher harmonic distortion in a filter with diffusion capacitors as a result of their non-linear nature.

6.2 APPLICATIONS

The main area of application for the operational amplifier is that of switched-capacitor circuits. The biquadratic filter is intended as a demonstration of this. As for the final end-use of the design techniques described in this thesis, which have the potential to significantly reduce power and area requirements of switched capacitor circuits, only general suggestions can be made.

Between the successful implementation of a new generation of process technology and the large-scale production of circuits which fully exploit the advances made, there is usually a lag of

several years. An example of this is the microprocessor. Although the LSI technology required had been used for years in making memory chips, the incredible range of microprocessor applications was not foreseen and its development was relatively slow. A similar situation exists with today's VLSI technologies. While digital VLSI circuits such as 64k DRAMs, graphics controllers and digital signal processing chips are currently in vogue, analog VLSI has largely been ignored.

Consider the previously impractical circuits which become distinctly possible with the introduction of an analog VLSI technology in which second-order filters occupy 100 mil**2 and consume only 50uW. High 'Q' bandpass filters could perform 128 or even 256 point "flash" Fourier transformations on a reasonably sized chip. Other real-time spectrum analysis requirements, frequency domain multiplexing modulation and demodulation circuits, as well as combination analog/digital systems can be conceived to exploit such an advance in analog integrated circuits. Analog VLSI has the potential to offer lower power, smaller size, and better performance than digital circuits in many applications.

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APPENDIX A: MOST Characteristics

This appendix is provided as a quick reference for the derivations of the equations used throughout the thesis describing the behavior of enhancement-mode, insulated-gate, field-effect transistors. The n- and p-channel devices, both of which are used in CMOS circuits, are shown in fig.A.1. Henceforth all voltages will be referenced to the substrate (bulk) potential. All currents are defined to be positive if the direction of flow is into the terminal concerned.

The drain current in a MOS transistor is a function of the drain voltage. This is shown in fig.A.2 for an n-channel device. The flat part of the curve is described by the following equation [22];

$$I_D = \frac{B}{2n} (V_G - V_T - nV_S)^2 \quad (\text{eq.A.1})$$

where V_T = threshold voltage

This region of the drain curve is the normal area of operation for MOS devices, and is termed the 'saturation region'. The small signal transconductances can be derived as follows.

$$g_m = \frac{d(I_D)}{d(V_G)} = \sqrt{\frac{2BI_D}{n}} \quad (\text{eq.A.2})$$

Fig. A.1a. *n*-channel MOST
b. *p*-channel MOST

Fig. A.2 *n*-channel Drain Curves

$$g_s = \frac{d(I_D)}{d(V_S)} = \sqrt{2BI_D n} \quad (\text{eq.A.3})$$

There is, in fact, a finite slope to the drain curves which represents an output conductance g_o . The Early voltage, shown in fig.A.3 as the x-axis intercept of the tangent to the slope of the saturation curve, defines g_o . The physical cause of this non-zero output conductance is channel length modulation. As source-drain bias is increased, the effective channel length is reduced by an expanding depletion region, so that transistor gain increases. The small signal output conductance can be written as a function of drain current and the Early voltage as follows;

$$g_o = \frac{I_D}{V_E} \quad (\text{eq.A.4})$$

A simple model for the MOS transistor, excluding capacitances and noise sources, can now be defined. (fig.A.4) If the transistor operates in strong inversion, that is, as long as the gate voltage is greater than the turn on voltage V_t , the preceding equations for the small signal parameters apply. Below this limit some current still flows in the device but a different model must be used its description. Another way of indicating when the transistor is no longer operating in strong inversion is the weak-inversion limit [25].

$$I_T = B \left| \frac{kT}{q} \right|^2 \quad (\text{eq.A.5})$$

A transistor with a drain current lower than I_t is said to be operating in weak inversion. Sub-threshold operation is

Fig. A.3 Early Voltage

Fig. A.4 MOST Small Signal Model

described by equation A.6 from which gate and source transconductances can be derived.

$$I_D = I_0 \times e^{qV_G/nkT} \times e^{-qV_S/kT} \quad (\text{eq.A.6})$$

$$g_m = \frac{d(I_D)}{d(V_G)} = \frac{qI_D}{nkT} \quad (\text{eq.A.7})$$

$$g_s = \frac{d(I_D)}{d(V_S)} = \frac{qI_D}{kT} \quad (\text{eq.A.8})$$

Output conductance in weak inversion is defined by the same equation as in strong inversion.

APPENDIX B: SPICE SIMULATIONS OF OTA

Five separate SPICE simulations are presented in this appendix. An open loop analysis of all three OTA designs has been performed. The computer printouts generated, including the SPICE input file, operating point information for each device, and the open loop frequency response of the circuit are included. Closed loop simulations were performed for the 5um and 1.5um designs. The OTA output was connected to the inverting input to form a unity gain configuration. Then a frequency response analysis was performed, followed by the transient response to a step input. Operating point information for these simulations has been omitted since it is identical to that provided with each corresponding open loop simulation.

SPICE level 1 MOS parameters for the 5um OTA simulations were supplied by Northern Telecom and were, with the exception of LAMBDA, based on the process specifications. The output conductance, from which LAMBDA was derived, was found by measuring a test device in the laboratory with a curve tracer. All SPICE parameters for the 3um and 1.5um simulations were found empirically with measurements performed on devices similar to those expected from the VLSI process.

5um OTA

Open-Loop Analysis

***** 02/17/82 ***** SPICE 2G.5 (10AUG81) ***** 17:53:22 *****

TRANSIENT ANALYSIS

**** INPUT LISTING TEMPERATURE = 27.000 DEG C

M1 3 31 1 0 P W=100U AS=600P AD=1200P
M2 4 32 1 0 P W=100U AS=600P AD=1200P
M3 3 3 3 50 50 N AS=240P AD=240P
M4 4 4 4 50 50 N AS=240P AD=240P
M6 6 4 4 50 50 N AS=240P AD=240P
M8 6 6 0 0 P W=64.58U AS=720P AD=720P
M9 9 6 0 0 P27 L=27U W=209U AS=2508P AD=1254P
M11 7 3 50 50 N AS=240P AD=240P
M13 11 21 7 50 N AS=240P AD=240P
M15 11 22 9 0 P27 L=27U W=356U AS=2136P AD=4272P
M18 1 20 0 0 P W=50U AS=600P AD=600P
VP 20 0 DC -1.2059
VCP 22 0 DC -2.3693
VON 21 0 DC -7.326
*OPTIONS DEF=8U DEFN=20U NOPAGE RELTOL=.0001 ABSTOL=.1P UNTOL=10N
*MODEL N MHOS VTO=1 KP=30.5U GAMMA=.699 LAMBDA=.0088
CGS0=400P CGD0=400P CJ=400U
*MODEL P PHOS VTO=-1 KP=10.2U GAMMA=.634 PHI=.615 LAMBDA=.03
CGSD=400P CGDO=400P CJ=180U
*MODEL P27 PHOS VTO=-1 KP=10.2U GAMMA=.634 PHI=.615 LAMBDA=.0088
CGS0=400P CGD0=400P CJ=180U
VDD 50 0 DC -10
IF 0 20 DC -1.4U
IC 22 0 DC 96U
COUT1 11 0 10P
VREF 32 0 DC -5
VBIAS 31 33 DC -5
VIN 33 0 AC 1
*AC DEC 5 .01 100HEG
*PRINT AC VDB(3) VP(3) VDB(9) VDB(11) VP(11)
*PLOT AC VDB(11) VP(11)
*END

TEMPERATURE = 27.000 DEG C

OPERATING POINT INFORMATION

*** KOSFETS

[illegible]

TEMPERATURE = 27.000 DEG C

AC ANALYSIS

LEGEND:

*: VDB(11)
+: VP(11)

5um OTA Open-Loop Frequency Response

5um OTA
Closed-Loop Analysis

***** 02/17/82 ***** SPICE 26.5 (10AUG81) ***** 17:45:43 *****

TRANSIENT ANALYSIS

*** INPUT LISTING TEMPERATURE = 27.000 DEG C

M1 3 31 1 0 P W=100U AS=600P AD=1200P
M2 4 32 1 0 P W=100U AS=600P AD=1200P
M3 3 3 50 50 N AS=240P AD=240P
M4 4 4 50 50 N AS=240P AD=240P
M5 6 4 50 50 N AS=240P AD=240P
M6 6 6 0 0 P W=64.58U AS=720P AD=720P
M7 9 6 0 0 P27 L=27U W=209U AS=2508P AD=1254P
M8 11 7 3 50 50 N AS=240P AD=240P
M9 11 21 7 50 N AS=240P AD=240P
M10 11 22 9 0 P27 L=27U W=356U AS=2136P AD=4272P
M11 1 20 0 0 P W=50U AS=600P AD=600P
VP 20 0 DC -1.2059
VCP 22 0 DC -2.3603
VCH 21 0 DC -7.326
*OPTIONS DEF=8U DEFN=20U NOPAGE RELTOL=.0001 ABSTOL=.1P UNTOL=10N
*MODEL N NMOS VTO=1 KP=30.5U GAMMA=1.42 PHI=.699 LAMBDA=.0088
CGS0=400P CGD0=400P CJ=400U
*MODEL P PMOS VTO=-1 KP=10.2U GAMMA=.634 PHI=.615 LAMBDA=.03
CGS0=400P CGD0=400P CJ=180U
*MODEL F27 FPGS VTO=-1 KP=10.2U GAMMA=.634 PHI=.615 LAMBDA=.0088
CGS0=400P CGD0=400P CJ=180U
VDD 50 0 DC -10
IP 0 20 DC -1.4U
IC 22 0 DC 96U
COUT1 11 0 10P
R 32 11 100
*BIAS 31 33 DC -5
VIN 33 0 AC 1 PWL(0 0 1U 0 1.01U -2 40U -2 40.01U 2 80U 2 80.01U -2)
*AC DEC 5 .01 100HEG
*PRINT AC VDB(3) VP(3) VDB(9) VDB(11) VP(11)
*PLOT AC VDB(11) VP(11)
*TRAN 2.5U 120U
*PRINT TRAN V(31) V(11) V(1)
*PLOT TRAN V(31) V(11)
*END

5um OTA Closed-Loop Frequency Response

TEMPERATURE = 27.000 DEG C

*** TRANSIENT ANALYSIS

LEGEND:

2: V(31)
 4: V(11)

TIME

(13) 人

5um OTA Closed-Loop Step Response

3um OTA

Open-Loop Analysis

***** 06/21/82 ***** SPICE 26.5 (10AUG81) ***** 16:58:22 *****

3 MICRON OTA

**** INPUT LISTING TEMPERATURE = 27.000 DEG C

M1 3 31 1 0 P L=2.5U W=20U AS=90P AD=180P
M2 4 32 1 0 P L=2.5U W=20U AS=90P AD=180P
M3 3 3 50 50 N L=2.5U W=3U AD=89P
M4 4 4 50 50 N L=2.5U W=3U AD=89P
M5 5 3 50 50 N L=2.5U W=3U AD=89P
M6 6 4 50 50 N L=2.5U W=3U AD=89P
M7 5 5 0 0 P L=2.5U W=8.483U AD=143P
M8 6 6 0 0 P L=2.5U W=8.483U AD=143P
M9 9 6 0 0 P L=5.5U W=19U AD=57P
M10 10 5 0 0 P L=5.5U W=19U AD=57P
M11 7 3 50 50 N L=2.5U W=3U AD=9P
M12 8 4 50 50 N L=2.5U W=3U AD=9P
M13 11 21 7 50 N L=2.5U W=3U AS=9P AD=89P
M14 12 21 8 50 N L=2.5U W=3U AS=9P AD=89P
M15 11 22 9 0 P6 L=5.5U W=19U AS=57P AD=137P
M16 12 22 10 0 P6 L=5.5U W=19U AS=57P AD=137P
M17 20 20 0 0 R L=2.5U W=3U AD=9P
M18 1 20 0 0 P L=2.5U W=3U AD=9P
*OPTIONS NOPAGE RELTOL=.00001 ABSTOL=.01P UNTOL=10N
*MODEL H PHOS VTO=.65 KP=79.5U GAMMA=.59 PHI=.663 LAMBDA=.057
TOX=50N NSUB=5E15 CJ=75U
*MODEL P PHOS VTO=-.65 KP=29.3U GAMMA=.59 PHI=.663 LAMBDA=.33
TOX=50N NSUB=5E15 CJ=75U
*MODEL P8 PHOS VTO=-.65 KP=29.3U GAMMA=.59 PHI=.663 LAMBDA=.057
TOX=50N NSUB=5E15 CJ=75U

VCP 22 0 -1
VCN 21 0 -4
VND 50 0 DC -5
IP 0 20 DC -2U
COUT1 11 0 10P
COUT2 12 0 10P
UREF 32 0 -2.5
VB1AS 31 33 DC -2.5
VIN 33 0 AC 1
*AC DEC 5 .01 100HEG
*PRINT AC VNR(3) VNR(11) VP (11)
*PLOT AC VDB(11) VP(11)
*END

**** MOSFETS

MODEL	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11	M12
IN	P	P	N	N	N	N	P	P	P6	PA	N	N
VGS	-1.12E-06	-1.12E-06	1.12E-06	1.12E-06	1.32E-06	1.32E-06	-1.32E-06	-1.32E-06	-1.08E-06	-1.08E-06	1.08E-06	1.08E-06
VDS	-1.090	-1.090	.800	.800	.800	.800	-795	-795	-795	-795	.800	.800
VBS	-2.790	-2.790	.800	.800	4.205	4.205	-795	-795	-159	-159	.154	.154
VTH	1.410	1.410	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000
VDSAT	-1.019	-1.019	.650	.650	.650	.650	-650	-650	-650	-650	.650	.650
GH	3.17E-05	3.17E-05	1.49E-05	1.49E-05	1.77E-05	1.77E-05	-145	-145	-145	-145	.150	.150
GDS	1.92E-07	1.92E-07	6.09E-08	6.09E-08	6.09E-08	6.09E-08	1.82E-05	1.82E-05	1.48E-05	1.48E-05	1.44E-05	1.44E-05
GHR	6.50E-06	6.50E-06	5.41E-06	5.41E-06	6.41E-06	6.41E-06	3.46E-07	3.46E-07	6.09E-08	6.09E-08	6.09E-08	6.09E-08
CRD	5.40E-15	5.40E-15	4.72E-15	4.72E-15	2.67E-15	2.67E-15	6.61E-06	6.61E-06	5.38E-06	5.38E-06	5.22E-06	5.22E-06
CBS	4.06E-15	4.06E-15	0.00E+00	0.00E+00	0.00E+00	0.00E+00	7.59E-15	7.59E-15	3.90E-15	3.90E-15	6.18E-16	6.18E-16
CGSOVL	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CGROVL	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CGROVL	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CGD	2.30E-14	2.30E-14	3.45E-15	3.45E-15	3.45E-15	3.45E-15	9.76E-15	9.76E-15	4.81E-14	4.81E-14	3.45E-15	3.45E-15
CGD	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CGR	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00

MODEL	M13	M14	M15	M16	M17	M18
IN	N	N	P6	P6	P	P
VGS	1.08E-06	1.08E-06	-1.08E-06	-1.08E-06	-2.00E-06	-2.23E-06
VDS	.846	.846	-.841	-.841	-.945	-.945
VBS	1.983	1.983	-2.703	-2.703	-.945	-1.410
VTH	-.154	-.154	.159	.159	.000	.000
VDSAT	.703	.703	-.705	-.705	-.650	-.650
GH	1.42	1.42	-.136	-.136	-.295	-.295
GDS	1.51E-05	1.51E-05	1.59E-05	1.59E-05	1.36E-05	1.52E-05
GDS	5.52E-08	5.52E-08	5.32E-08	5.32E-08	5.03E-07	5.03E-07
GHR	4.94E-06	4.94E-06	5.16E-06	5.16E-06	4.92E-06	5.50E-06
CRD	3.48E-15	3.48E-15	4.80E-15	4.80E-15	4.57E-16	4.06E-16
CBS	6.18E-16	6.18E-16	3.90E-15	3.90E-15	0.00E+00	0.00E+00
CGSOVL	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CGROVL	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CGROVL	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CGS	3.45E-15	3.45E-15	4.81E-14	4.81E-14	3.45E-15	3.45E-15
CGD	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CGB	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00

3um OTA Open-Loop Frequency Response

1.5um OTA

Open-Loop Analysis

***** 06/07/92 ***** SPICE 26.5 (10AUG81) ***** 15:07:06 *****

SHORT CHANNEL OTA

*** INPUT LISTING TEMPERATURE = 27.000 DEG C

```

M1 3 31 1 0 P L=.75U W=3U AS=90P AD=180P
M2 4 32 1 0 P L=.75U W=3U AS=90P AD=180P
M3 3 3 50 50 N L=.75U W=3U AD=89P
M4 4 4 50 50 N L=.75U W=3U AD=89P
M5 5 3 50 50 N L=.75U W=3U AD=89P
M6 6 4 50 50 N L=.75U W=3U AD=89P
M7 5 0 0 P L=.75U W=10.35U AD=143P
M8 6 6 0 0 P L=.75U W=10.35U AD=143P
M9 9 6 0 0 P2.5 L=1.75U W=19U AD=57P
M10 10 5 0 0 P2.5 L=1.75U W=19U AD=57P
M11 7 3 50 50 N L=.75U W=3U AD=9P
M12 8 4 50 50 N L=.75U W=3U AD=9P
M13 11 21 7 50 N L=.75U W=3U AS=9P AD=89P
M14 12 21 8 50 N L=.75U W=3U AS=9P AD=89P
M15 11 22 9 0 P2.5 L=1.75U W=19U AS=57P AD=137P
M16 12 22 10 0 P2.5 L=1.75U W=19U AS=57P AD=137P
M17 20 20 0 0 P L=.75U W=3U AD=9P
M18 1 20 0 0 P L=.75U W=3U AD=9P
.OPTIONS NOPAGE RELTOL=.00001 ARSTOL=.01P VNTOL=10M
.MODEL N NMOS VTO=.65 KP=79.5U GAMMA=.59 PHI=.663 LAMBDA=.5
.MODEL P P VTO=.65 KP=79.5U GAMMA=.59 PHI=.663 LAMBDA=.5
.MODEL NSUB=SEIS CJ=75U
.MODEL P2.5 PHOS VTO=.65 KP=29.3U GAMMA=.59 PHI=.663 LAMBDA=.5
.MODEL NSUB=SEIS CJ=75U
VCF 22 0 -1
VCN 21 0 -4
VDD 50 0 DC 5
IP 0 20 DC 120
COUT1 11 0 10P
COUT2 12 0 10P
WREF 32 0 -2.5
VBIAS 31 33 DC -2.5
VIN 33 0 AC 1
.AC DEC 5 .01 100HEG
.PRINT AC VDB(3) VDB(11) VP(11)
.PLOT AC VDB(11) VP(11)
.END

```

**** OPERATING POINT INFORMATION TEMPERATURE 100.00 DEG

**** MOSFETS

MODEL	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11	M12
IR	P	P	N	N	N	N	P	P	P2.5	P2.5	N	N
VGS	-1.51E-06	-1.51E-06	1.51E-06	1.51E-06	3.47E-06	3.47E-06	-3.47E-06	-3.47E-06	-1.23E-06	-1.23E-06	1.23E-06	1.23E-06
VDS	-1.083	-1.083	.733	.733	.733	.733	-.733	-.733	-.733	-.733	.733	.733
VRS	-2.849	-2.849	.733	.733	4.267	4.267	-.733	-.733	-.218	-.218	.216	.216
VTH	1.417	1.417	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000
VRSAT	-1.021	-1.021	.650	.650	.650	.650	-.650	-.650	-.650	-.650	.650	.650
GM	4.88E-05	4.88E-05	3.63E-05	3.63E-05	8.32E-05	8.32E-05	8.32E-05	8.32E-05	2.94E-05	2.94E-05	2.94E-05	2.94E-05
GDS	4.52E-07	4.52E-07	5.54E-07	5.54E-07	5.54E-07	5.54E-07	3.02E-05	3.02E-05	5.54E-07	5.54E-07	5.54E-07	5.54E-07
GHR	9.97E-06	9.97E-06	1.31E-05	1.31E-05	3.01E-05	3.01E-05	7.75E-15	7.75E-15	1.07E-05	1.07E-05	1.07E-05	1.07E-05
CRD	5.34E-15	5.34E-15	4.82E-15	4.82E-15	2.65E-15	2.65E-15	0.00E+00	0.00E+00	3.79E-15	3.79E-15	3.99E-16	3.99E-16
CRS	4.05E-15	4.05E-15	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CGSOVL	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CGROVL	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CGS	1E-15	1.04E-15	1.04E-15	1.04E-15	1.04E-15	1.04E-15	3.57E-15	3.57E-15	0.00E+00	0.00E+00	1.04E-15	1.04E-15
CGR	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CGR	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00

MODEL	M13	M14	M15	M16	M17	M18
IR	N	N	P2.5	P2.5	P	P
VGS	1.23E-06	1.23E-06	-1.23E-06	-1.23E-06	-2.00E-06	-3.03E-06
VDS	.784	.784	-.782	-.766	-.766	-.766
VRS	2.136	2.136	-2.430	-1.417	-1.417	-1.417
VTH	-.216	-.216	.218	.000	.000	.000
VRSAT	.723	.723	-.723	-.650	-.650	-.650
GM	4.02E-05	4.02E-05	4.16E-05	4.16E-05	3.45E-05	5.22E-05
GDS	2.97E-07	2.97E-07	2.77E-07	2.77E-07	1.58E-06	1.58E-06
GHR	1.24E-05	1.24E-05	1.31E-05	1.31E-05	1.25E-05	1.89E-05
CRD	3.36E-15	3.36E-15	4.95E-15	4.95E-15	8.2E-16	4.05E-16
CRS	5.99E-16	5.99E-16	3.79E-15	3.79E-15	0.00E+00	0.00E+00
CGSOVL	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CGROVL	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CGS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CGR	1.04E-15	1.04E-15	1.53E-14	1.53E-14	1.04E-15	1.04E-15
CGR	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CGR	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00

TEMPERATURE = 27.000 DEG C

AC ANALYSIS

LFGBND:

*: VDB(11)
+: UP(11)

FREQ VDB(11)

1.5um OTA Open-Loop Frequency Response

1.5um OTA

Closed-Loop Analysis

***** 06/07/82 ***** SPICE 26.5 (10AUG81) ***** 15:16:40 *****

SHORT CHANNEL OTA

*** INPUT LISTING TEMPERATURE = 27.000 DEG C ***

```

M1 3 31 1 0 P L=.75U W=3U AS=90P AD=180P
M2 4 32 1 0 P L=.75U W=3U AS=90P AD=180P
M3 3 3 50 50 N L=.75U W=3U AD=89P
M4 4 4 50 50 N L=.75U W=3U AD=89P
M5 3 3 50 50 N L=.75U W=3U AD=89P
M6 4 4 50 50 N L=.75U W=3U AD=89P
M7 5 5 0 0 P L=.75U W=10.35U AD=143P
M8 6 6 0 0 P L=.75U W=10.35U AD=143P
M9 9 8 0 0 P2.5 L=1.75U W=19U AD=57P
M10 10 5 0 0 P2.5 L=1.75U W=19U AD=57P
M11 7 3 50 50 N L=.75U W=3U AD=9P
M12 8 4 50 50 N L=.75U W=3U AD=9P
M13 11 21 7 50 N L=.75U W=3U AS=9P AD=89P
M14 12 21 8 50 N L=.75U W=3U AS=9P AD=89P
M15 11 22 9 0 P2.5 L=1.75U W=19U AS=57P AD=137P
M16 12 22 10 0 P2.5 L=1.75U W=19U AS=57P AD=137P
M17 20 20 0 0 P L=.75U W=3U AD=9P
M18 1 20 0 0 P L=.75U W=3U AD=9P
* OPTIONS NOPAGE RELTOL=.00001 ABSTOL=.01P UNTOL=10N
* MODEL N NMOS VTO=.65 KP=.79.5U GAMMA=.59 PHI=.663 LAMBDA=.5
TOX=.50N NSUR=SEIS CJ=75U
* MODEL P PHOS VTO=-.65 KP=.29.3U GAMMA=.59 PHI=.663 LAMBDA=.5
* MODEL P2.5 PHOS VTO=-.65 KP=.29.3U GAMMA=.59 PHI=.663 LAMBDA=.5
TOX=.50N NSUR=SEIS CJ=75U
VCP 22 0 -1
VCN 21 0 -4
VDD 50 0 DC -5
IP 0 20 DC -2U
COUT1 11 0 10P
COUT2 12 0 10P
R 32 11 100
VBIAS 31 33 DC -2.5
VIN 33 0 AC 1 PUL(0 0 1U 0 1.01U -1 40U -1 40.01U 1 80U 1 80.01U -1)
.AC DEC 5 .01 100HEG
.PRINT AC VDB(3) VDB(11) VP(11)
.PLOT AC VDB(11) VP(11)
.TRW 2.5U 120U
.PRINT TRAN V(31) V(11) V(1)
.PLOT TRAN V(11) V(31)
.END

```

XXXX AC ANALYSIS

LEGEND:

```
x: vdb(11)
t: vp(11)
```

FREQ VDB(11)

(8)-----6,000D+1

-4.0000+01

-2,000B+01

0.000000

2,000+01

(4) $-1,500D+02$

-1,000D+02

-5.0000+01

0.0000+00

5.0000+01

1.000B-02	3.309B-03
1.365B-02	3.309D-03
2.512B-02	3.309D-03
3.981B-02	3.309D-03
4.6.310B-02	3.309D-03
1.000B-01	3.309D-03
1.585B-01	3.309D-03
2.512B-01	3.309D-03
3.981B-01	3.309D-03
4.710B-01	3.309D-03
1.000B+00	3.309D-03
1.585B+00	3.309D-03
2.512B+00	3.309D-03
3.981B+00	3.309D-03
4.6.310B+00	3.309D-03
1.000B+01	3.309D-03
1.585B+01	3.309D-03
2.512B+01	3.309D-03
3.981B+01	3.309D-03
4.6.310B+01	3.309D-03
1.000B+02	3.309D-03
1.585B+02	3.309D-03
2.512B+02	3.309D-03
3.981B+02	3.309D-03
4.6.310B+02	3.309D-03
1.000B+03	3.309D-03
1.585B+03	3.309D-03
2.512B+03	3.309D-03
3.981B+03	3.309D-03
4.6.310B+03	3.309D-03
1.000B+04	3.309D-03
1.585B+04	3.309D-03
2.512B+04	3.309D-03
3.981B+04	3.309D-03
4.6.310B+04	3.309D-03
1.000B+05	3.309D-03
1.585B+05	3.309D-03
2.512B+05	3.309D-03
3.981B+05	3.309D-03
4.6.310B+05	3.309D-03
1.000B+06	3.309D-03
1.585B+06	3.309D-03
2.512B+06	3.309D-03
3.981B+06	3.309D-03
4.6.310B+06	3.309D-03
1.000B+07	3.309D-03
1.585B+07	3.309D-03
2.512B+07	3.309D-03
3.981B+07	3.309D-03
4.6.310B+07	3.309D-03
1.000B+08	3.309D-03
1.585B+08	3.309D-03
2.512B+08	3.309D-03
3.981B+08	3.309D-03
4.6.310B+08	3.309D-03

magnitude
phase

1.5um OTA Closed-Loop Frequency Response

*** TRANSIENT ANALYSIS

#: V(11)

4: V(31)

TIME 4(11)A

(8) 00-00000000-000000000000000000000000 -4,000D+00

1
2
3
4

0040005-3- (4)

[illegible]

2.5000-06
-3.0020+00
-2.3000+00
+ +

$$5,000 - 0.6 \times -3,500 + 0 = 7,000$$

7.5000-06	-3.5000+00	+
1.0000-05	-3.5000+00	+

1.2500-05	-3.5000+00	+
1.5000-05	-7.5000+00	+

1.300-03	-3.300+00	+
1.750D-05	-3.500D+00	+

2.000D-05	-3.500D+00	+
2.250D-05	-3.500D+00	+

2,500D-05 -3,500D+00 +

2,7500-05	-3,5000+00	+
3,0000-05	-3,5000+00	+

3,250D-05 -3,500D+00 +

3.5000-05	-3.5000+00	+
7.7500-05	-3.5000+00	+

4.000D-05
-3.500D+00
+ +

1.2500-05	-2.7870+00
4.5000-05	-2.2170+00

4,7500-05 -1,7350+00

5.0000-05	-1.5010+00	.
5.2500-05	-1.5000+00	.

5.500D-05 -1.500D+00

5.7500-05 -1.5000+00
6.0000-05 -1.5000+00

6.2500-05 -1.5000+00

6.5000-05 50-0000-1
6.7500-05 50-0000-1

7.0000-05
-1.5000+00

7.250D-05	-1,500D+00
7.500D-05	-1,500D+00

7.7500-05 -1.5000+00

8.0000-03 -1.3000+00 +
8.7500-05 -2.3400+00 +

8.5000-05 -3.1770400 +

8,7500-05	-3,5000+00	+
9,0000-05	-3,5000+00	+

9.2500-05 -3.5000+00

9.500D-05	-3.500D+00	+
9.750D-05	-3.500D+00	+

1.0000-04	-3.5000+00	+
1.0250-04	-3.5000+00	+

1.050D-04 -3.500D+00 +

1.0750-04	-3.5000+00	+
1.1000-04	-3.5000+00	+

1.1250-04
-3.5000+00 +

1.150D-04	-3.500D+06	+
1.175D-04	-3.500D+00	+

1.200D-04 -3.500D+00 +

1
2
3
4

input

output

1.5um OTA Closed-Loop Step Response

APPENDIX C: BALANCED BIQUAD SIMULATIONS

I. FREQUENCY DOMAIN SIMULATION BY SUBSTITUTION OF ANALOG EQUIVALENTS (see sections 4.3.1, 4.3.2, 5.1, and 5.2)

The major problem in using SPICE for this method of analysis is the implimentation of frequency dependant resistors. This can be overcome by approximating an admittance with a power series in frequency.

$$f(\omega T/2) = a_0 + a_1(\omega T/2)^2 + a_2(\omega T/2)^4 \quad (\text{eq.C.1})$$

Naturally, the more power terms used, the more accurate the analysis will be. Three terms were chosen as a compromise between accuracy and efficiency. To determine the three co-efficients the squared error of the approximated function is minimized in the frequency interval of interest. This results in a system of equations of the form [26]:

$$\begin{vmatrix} \int_1^x x^2 dx & \int_1^x x^2 x^2 dx & \int_1^x x^2 x^4 dx \\ \int_1^x x^2 x^2 dx & \int_1^x x^2 x^4 dx & \int_1^x x^2 x^6 dx \\ \int_1^x x^2 x^4 dx & \int_1^x x^2 x^6 dx & \int_1^x x^2 x^8 dx \end{vmatrix} \begin{vmatrix} a_0 \\ a_1 \\ a_2 \end{vmatrix} = \begin{vmatrix} \int_1^x x^2 f(x) dx \\ \int_1^x x^2 x^2 f(x) dx \\ \int_1^x x^2 x^4 f(x) dx \end{vmatrix}$$

where $x = (\omega T/2)$

(eq.C.2)

In SPICE powers of $(\omega T/2)$ can be generated by use of the fact that the voltage across an inductor is equal to $j\omega L$ times the current. If the current is in turn related to the voltage across another inductor, and so on, the required even powers of $(\omega T/2)$ are produced. Unfortunately, the odd powers are of no use since they are complex. In the listing of the biquad simulation subcircuit PER multiplies an input voltage by $j\omega T/2$ and subcircuit TAN sums the voltages with the coefficients calculated as per equation C.2 to realize the frequency dependant admittance. Subcircuit BBSC combines all the elements in the balanced bilinear switched capacitor derived in chapter 4. It is called with the format shown in fig.C.1.

Xname	n1	n2	n3	n4	n5	n6	BBSC
Ename	n5	n0	n1	n3	C		
Ename	n6	n0	n2	n4	C		

Fig. C.1 BBSC Subcircuit

Biquad Frequency Domain Analysis

***** 10/09/82 ***** SPICE 20.3 (10AUG81) ***** 15:35:10 *****

BALANCED BIQUAD FREQUENCY DOMAIN ANALYSIS

*** INPUT LISTING TEMPERATURE = 27.000 DEG C

UTN 1 0 AC .5
EIN 2 0 1 0 -1
XA 1 2 3 4 11 12 RBSC
EA1 11 0 1 3 .3251
EA2 12 0 2 4 .3251
C1 3 5 1P
C2 4 6 1P
E1 5 0 4 3 10K
E2 6 0 3 4 10K
XA 5 6 8 7 13 14 RBSC
ER1 13 0 5 8 .3251
ER2 14 0 6 7 .3251
C3 7 9 1P
CA 8 10 1P
E3 9 0 8 7 10K
EA 10 0 7 6 10K
XC 9 10 3 4 15 16 RBSC
EC1 15 0 9 3 .3251
EC2 16 0 10 4 .3251
XD 9 10 7 8 17 18 RBSC
ED1 17 0 9 7 .4594
ED2 18 0 10 8 .4594
EGUT1 20 0 9 10 1
EGUT2 21 0 5 6 1
R3 3 0 1E10
R4 4 0 1E10
R7 7 0 1E10
R8 8 0 1E10
R20 20 0 1E10
R21 21 0 1E10
*OPTIONS RELTOL=.01 VNTOL=100 PIVTOL=1E-16
*AC LIN 125 40 5K
*PLOT AC VDB(20) VDB(21)
*PRINT AC VDB(9) VDB(10) VDB(5) VDB(6)
*SURCAT PER 101 102
G 0 101 102 0 .5
L 101 0 50U
*ENDS PER
*SURCAT TAN 81 80 83
X1 91 83 PER
X2 92 91 PER
X3 93 92 PER
X4 94 93 PER
G 81 80 POLY(3) 83 0 92 0 0 94 0 1.00000025 .3332575 .0234389
R 81 80 1E10
RX 83 0 1E10
*ENDS TAN
*SURCAT RBSC 1 2 3 4 5 6

XTP 5 7 50 TAN
ETP 50 0 5 7 20N
CP 5 9 .5P
V7 7 0 0
V9 9 0 0
XTN 6 8 52 TAN
ETN 52 0 6 8 20N
CN 6 10 .5P
V8 8 0 0
V10 10 0 0
FP 1 3 POLY(4) V7 V9 V8 V10 0 1 1 -1 1
FN 2 4 POLY(4) V7 V9 V8 V10 0 -1 1 1 1
*ENDS BBSC
*END

II. TIME DOMAIN SIMULATION (see sections 4.3.3, 5.1 and 5.2)

The only difficulty here is in the implementation of an ideal switch. This is accomplished by defining a current source between two points which is proportional to the voltage between those points and an additional control voltage. Without the control voltage there would simply be a constant resistance between the nodes; with it there is a modulated resistance. The control voltage is essentially the clock phase associated with that particular switch. Switch resistance varies from infinity in the off state to 10Ω in the on state. Fig.C.2 describes the switch model.

Xname $n1$ $n2$ 90 P

Xname $n1$ $n2$ 91 P

Fig.C.2 Switch Subcircuit

Biquad Time-Domain Analysis

POOR PRINT
Epreuve illisible

***** 10/09/82 ***** SPICE 26.5 (10AUG81) ***** 15:50:50 *****

BALANCED BIQUAD

*** INPUT LISTING TEMPERATURE = 27.000 DEG C

```

X1 1 5 90 P
X2 1 6 91 P
X3 0 6 90 P
X4 0 5 91 P
C1 5 7 .3251N
C2 6 8 .3251N
X5 7 9 90 P
X6 7 10 91 P
X7 8 10 90 P
X8 8 9 91 P
E1 11 0 POLY(2) 9 0 10 0 0 -10K 10K
E2 12 0 POLY(2) 9 0 10 0 0 10K -10K
C3 9 11 1N
C4 10 12 1N
X9 11 13 91 P
X10 11 14 90 P
X11 12 14 91 P
X12 12 13 90 P
C5 13 15 .3251N
C6 14 16 .3251N
X13 15 17 90 P
X14 15 18 91 P
X15 16 18 90 P
X16 16 17 91 P
E3 19 0 POLY(2) 17 0 18 0 0 -10K 10K
E4 20 0 POLY(2) 17 0 18 0 0 10K -10K
X17 19 21 90 P
X18 19 22 91 P
X19 20 22 90 P
X20 20 21 91 P
C7 17 19 1N
C8 18 20 1N
C9 15 21 .4594N
C10 16 22 .4594N
C11 7 21 .3251N
C12 8 22 .3251N
R101 30 0 POLY(2) 19 0 20 0 0 1 -1
R102 31 0 POLY(2) 11 0 12 0 0 1 -1
R103 31 0 1E9
R104 30 0 1E9
V10 90 0 PULSE(0 1 .5U .1U .1U 1U 4U)
V1 91 0 PULSE(0 1 2.5U .1U .1U 1U 4U)
R10 90 0 1E9
R1 91 0 1E9
V1N 1 0 PULSE(0 1 .1U .1U .1U 2U .2H)
R10CAT 1 1 2 3
C1 1 2 POLY(2) 1 2 3 0 0 0 0 1
R1 1 0 1E9

```

REP 2 0 1E9
ENDS P
OPTIONS ILS=7500
TRAN 1U 100U
PLGT TRAN VC(30) V(31)
END

Epreuve illisible

Biquad Unit-Impulse Response

output of 1st integrator

Indno pambiq.

[illegible]

LECD:	#	TIME	W(30)
1	1	01	0.0000+00
2	2	01	0.0000+00
3	3	01	0.0000+00
4	4	01	0.0000+00
5	5	01	0.0000+00
6	6	01	0.0000+00
7	7	01	0.0000+00
8	8	01	0.0000+00
9	9	01	0.0000+00
10	10	01	0.0000+00

BALANCED BUDGET
10/09/82 ***** SPICE 20.5 (10AUG81) *****

TEMPERATURE = 27.000 DEG C

TRANSIENT ANALYSIS

END

0	6	H	0	9	H	8	4
---	---	---	---	---	---	---	---

FIN