Using Oscillator Gain and Injection-Locking to Measure On-Chip Inductor Coupling

by

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Abstract

The theoretical behaviour of oscillators is explored using the $-g_m$ model. Mathematical derivations based on the model show that the frequency response of an LC oscillator resembles that of a high Q band pass filter with exceptionally high, but finite, pass band gain. The linear derivations predict a 20 dB/dec roll-off beyond the loaded 3 dB corner which is consistent with the accepted phase noise model of the oscillator. The non-linear sampling of the transconductor explains the aliasing behaviour and the generally symmetrical phase noise response of an oscillator. The theoretical response is supported by time-domain simulation results of the same model, that show the response of the oscillator to injected tones at both low powers and powers great enough to injection-lock the oscillator. The measured response of a real oscillator is presented, confirming the theoretical response predicted by the simple model. The demonstrated oscillator gain shows how oscillators can be used in non-traditional roles such as active filters or amplifiers. As an oscillator has gain within a determinable bandwidth and an injection-locked oscillator has the same output power as an identical oscillator operated free-running, on-chip inductor coupling can easily be measured using oscillators.

Simulations of near-field on-chip inductor coupling are discussed and the design, implementation, and measurements of a unique experimental test chip and PCB for measuring on-chip inductor coupling easily and accurately are presented. The experiment requires no calibration, matching, or probe de-embedding and makes use of an injection-locked bipolar oscillator acting as a transmitter and a free-running bipolar oscillator behaving as a receiver. As the experiment makes use of the high gain of an oscillator, the experiment is very sensitive and can be used to measure small levels of coupling. Inductor coupling of -35 dB was measured with ease, while lengthy EM simulations and oscillator theory predict -36 dB of coupling, virtually the same result for the 1.3 nH, three turn inductors spaced 175 μm apart. The measurement is accurate and supports the theoretical gain response of the oscillator to coupled tones. The observed high level of coupling attests to the importance of considering inductor

coupling in typical RFIC designs. The results of the experiment provide insight into the magnitude of inductor coupling versus both frequency and inductor separation. The success of the experiment lays the groundwork for similar future experiments which could be used to evaluate the effectiveness of isolation techniques such as deep trench.

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List of Abbreviations and Symbols

AC	Alternating Current
ADS	Advanced Design System (a software package from Agilent Technologies)
AM	Amplitude Modulation
BiCMOS	Bipolar Complimentary Metal Oxide Semiconductor (a manufacturing process enabling both bipolar and CMOS transistors on the same chip)
BPF	Band Pass Filter
CAD	Computer Aided Design
CMOS	Complementary Metal-Oxide Semiconductor
Cu	Copper
DC	Direct Current (zero frequency)
DFT	Discrete Fourier Transform
EM	Electro-Magnetic (fields or waves)
ESD	Electro-Static Discharge
F	noise factor
FFT	Fast Fourier Transform
FM	Frequency Modulation
FR4	a material made of fibreglass & epoxy used as a substrate for a PCB
IC	Integrated Circuit
IF	Intermediate Frequency
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Low Pass Filter
MIM	Metal-Insulator-Metal (capacitor)
NF	Noise Figure (F in decibels)
PA	Power Amplifier

PCB	Printed Circuit Board
PN	refers to the junction between positively doped and negatively doped regions (of silicon)
RBW	Resolution Bandwidth (of a spectrum analyzer)
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
RMS or rms	Root Mean Squared
SMA	Sub-Miniature type ‘A’ (cable connector)
SNR	Signal-to-Noise Ratio
VCC or VDD	upper voltage supply rail
VCO	Voltage Controlled Oscillator
VSS	lower voltage supply rail
WLAN	Wireless Local Area Network

Chapter 1

Introduction

1.1 Motivation

The world of today is adopting new technology at an ever increasing rate with the sales of high-tech gadgets and gizmos rising steadily. While most technology users are pleased by the increased capabilities of modern devices, the majority would happily go without the wires that connect to these devices if the functionality could be maintained using a wireless link. Devices which were previously wired such as mice, keyboards, and telephones are now readily available in wireless formats. Even wires that transmit with large signal bandwidths, such as in computer networks, are being replaced by wireless solutions. In short, the world is going wireless.

With the recent proliferation of radio frequency integrated circuits (RFICs) into the wireless marketplace, competition is fierce and manufacturers are constantly struggling to introduce added functionality while at the same time reducing costs to maximize both sales and profits. Many RFICs have historically made use of off-chip inductors for tuned and filtered circuits, but modern IC fabrication techniques have facilitated the implementation of high quality inductors on-chip. This integration reduces the final expense of a product, and consequently increases profits, by negating the need for discrete inductors. While the use of integrated inductors may reduce the overall size of a product and be financially advantageous, on-chip inductors still suffer from lower quality, or “ Q ” factors, than their discrete counterparts, and placing multiple inductors on the same chip introduces a number of coupling effects.

Much like spiral antennas, inductors radiate and absorb EM fields. In addition to coupling through the air above the chip, integrated inductors on the same chip

are essentially capacitively coupled to the substrate, and signals consequently couple from one inductor to another through the common substrate. Inductor coupling is poorly modelled by most radio frequency (RF) design tools posing difficulties for both system and circuit designers to incorporate the effect into the design process and necessitating the use of complicated and tedious EM simulation tools. Isolation mechanisms such as guard rings are frequently added to circuit layouts, increasing the manufacturing expense of the chip. Such precautions are often based on little more than empirical assumptions in the hope of minimizing the coupling between blocks. A strong understanding of the inductor coupling mechanism would enable RFIC designers to quickly predict inductor coupling and its effects, and modify their designs appropriately to avoid unwanted coupling or maximize beneficial inductor coupling. The first step to such understanding is the creation of techniques to accurately measure on-chip inductor coupling. This thesis presents an experiment for making quantitative measurements of on-chip inductor coupling. The experiment makes use of integrated bipolar oscillators that can be injection-locked, making the experiment accurate without the need for any circuit matching, calibration, or de-embedding.

1.2 Previous Work and Thesis Objectives

Previous experiments by [1], [2] and [3] have shown that coupling between on-chip inductors can be significant and that the magnitude of the coupling is affected by spacing and orientation of the inductors. While successful in determining the factors that affect coupling, these experiments require careful matching and de-embedding in order to achieve quantitative results. The final objective of the work described in this thesis is to achieve a method of accurately measuring on-chip inductor coupling, while at the same time studying some of the issues surrounding the inductor coupling phenomenon. However, the experiment that is presented in the thesis relies heavily on an injection-locked oscillator acting as an on-chip transmitter and a free-running oscillator behaving as a receiver. Consequently, understanding the fundamental behaviour of a voltage controlled oscillator (VCO) and the injection-locking phenomenon is essential to the interpretation of the results of the experiment. Although measuring inductor coupling is the final goal of the research work, studying VCO behaviour and oscillator injection-locking is the means of achieving that goal. In addition to

serving the purpose of the experiment, modelling the oscillator as a high gain, high Q , non-linear filter demonstrates the oscillator's potential for use in non-traditional roles such as active filters [4] and gain stages, or in emerging technologies such as ultra-low power (or self-powered) radios [5]. Consequently, the contribution to the scientific community of the work presented in this thesis is twofold.

- The gain versus frequency response of an oscillator is derived mathematically and simulated using a simplified circuit model. The accuracy of the model is verified through comparison with measured results demonstrating oscillator gain, phase noise, and injection-locking.
- A novel experiment is presented which makes use of injection-lockable bipolar oscillators to measure on-chip coupling between integrated inductors. The experiment is accurate and unique in that no matching, probe de-embedding, or calibration is necessary as the ratio of two on-chip signals is measured to yield the results. Theoretical and simulated models of injection-locked oscillators and inductor coupling are discussed and compared to results measured using the test chip to validate the experiment.

1.3 Thesis Organization

This thesis has been organized to explain the motivation behind the research, to explain the theory necessary for understanding the experiment, to discuss the design of the experimental test chip and printed circuit board (PCB), and finally, to present the results of the research experiment.

Chapter 2, the background section, elaborates on the motivation for the work, giving examples of standard RF circuits that are affected by inductor coupling. Anyone implementing an RF circuit design should be interested in the results of the inductor coupling experiment.

Chapter 3 presents the derivation of an oscillator's gain response versus frequency using a simple circuit model. Credit is given to Robins [6], a pioneer of the high Q oscillator model, whose work is the inspiration for this derivation. The concepts of loaded and unloaded Q and bandwidth are introduced, and some theoretical insight into the injection-locking phenomenon is presented.

Chapter 4 demonstrates that the simple circuit model can be simulated in the time-domain and shown to model an oscillator's behaviour effectively, complete with injection-locking. Results of the simulations are compared to the theoretical derivation, confirming its validity.

Chapter 5 presents the design of the experimental test chip and the PCB to which it is mounted. Measured results of the integrated oscillators on the test chip are discussed and compared to the simulated results achieved with the simple model.

Chapter 6 outlines the unique experiment for measuring inductor coupling using an injection-locked oscillator and a free-running oscillator. A brief review of on-chip inductor coupling theory is presented, along with simulated results of inductor coupling using an EM simulator. The design of the on-chip LC resonators used for measuring coupling versus inductor separation are discussed along with the experimental coupling results. The measured results are compared to the results achieved with the EM simulator.

In Chapter 7, the conclusion, the research work is summarized and the key achievements are highlighted. Future work and extensions of the research experiment are discussed. Publications that were a direct result of this work are listed.

A brief review of noise, signal-to-noise ratio, noise figure, and equivalent noise bandwidth is included in Appendix A as the theory involved is needed for the theoretical derivation of the VCO's gain versus frequency. The MATLAB code used for plotting the rectangular and Hanning windowed fast Fourier transforms (FFTs) of the time-domain simulation outputs is included in Appendix B, and the MATLAB code for determining the instantaneous frequency versus time of the simulated oscillator is included in Appendix C. The Gerber layout views of the different layers of the PCB are included in Appendix D.

Chapter 2

Background and Examples from Literature

2.1 On-Chip Inductor Coupling in Silicon

The effects of on-chip inductor coupling are directly applicable to many facets of integrated circuit design. A typical RFIC chip could have many inductors with significant coupling between independent functional blocks as shown in Figure 2.1.

Figure 2.1: Coupling Between RF Blocks

The output power of a power amplifier (PA) is typically high compared to that of a low-noise amplifier (LNA) or a VCO and even low levels of coupling could seriously impair the performance of these sensitive blocks. Consider the single chip complementary metal-oxide semiconductor (CMOS) transceiver for 802.11 a/b/g wireless local area network (WLAN) standards [7] shown in Figure 2.2. This transceiver has

30 spiral inductors on the same chip, which will definitely result in coupling between the different functional blocks.

Figure 2.2: CMOS Transceiver for 802.11 a/b/g WLANs

Architectures such as the direct conversion transmitter shown in Figure 2.3 are particularly sensitive to the ill-effects of inductor coupling.

In the case of the direct transmitter, the local oscillator (LO) is operating at the same frequency as the nominal output of the PA. The output of the PA is a frequency modulated signal. Coupling (feedback) between the PA block and the LO block could have significant effects on the transmitter's operation. If the instantaneous frequency

Figure 2.3: Direct Transmitter Architecture

of the PA is $\Delta\omega$ away from the frequency of the LO, the LO frequency could be pulled towards the frequency of the PA if the coupling is strong enough, and even at lesser levels of coupling, a sideband “spur” will be introduced into the spectrum of the LO. In the first case, a direct change in the LO’s frequency will result in a shifted nominal output frequency, possibly moving the transmitted message signal out of band. In the case of a spur, the modulating signal will mix with both the spur and the carrier tone, introducing noise to the output signal, possibly in and or out of band, and potentially interfering with reception of the transmitted signal or signals in other frequency bands. Given these effects, designers of direct transmitters would benefit greatly from being able to measure inductor coupling accurately. By measuring the coupling of different layouts, an RF designer is able to predict the ramifications of coupling such that appropriate steps can be taken to minimize or eliminate the effects.

The example presented showed how a transmitter, comprised of many separate functional blocks, could suffer in performance due to on-chip coupling, but a single functional block's performance could just as easily be degraded by internal coupling within the circuit. Consider the simple, inductively degenerated cascode amplifier circuit in Figure 2.4. The circuit, shown without the DC biasing details, is commonly used in LNA designs for RF applications. Coupling from L_e to L_c could increase or decrease the gain of the amplifier, depending on the phase difference between the coupled signal and the output, as the two signals could add constructively or destructively. Similarly, feedback coupling between L_e and L_b or L_c and L_b could cause the circuit to become unstable. The simulated gain responses of a cascode LNA circuit very similar to the topology shown in Figure 2.4 are shown in Figure 2.5. Figure 2.5 shows the amplifier's gain both with and without inductor coupling being modelled using the models developed through this research work [8].

Figure 2.4: Coupling in Cascode Amplifiers

Figure 2.5 shows that coupling within the LNA circuit decreases the peak gain by 3 or 4 dB, and shifts the optimal operating frequency from 4.7 GHz to about 5.3 GHz. Both are undesirable effects in this case, assuming the input signal is at 4.7 GHz and that maximum gain is required.

Figure 2.5: Coupling Effects on a Cascode LNA's Gain

Recall that inductor coupling is poorly modelled by most RF design tools, causing difficulty for designers to incorporate the effect into the design process. As a result, designers must resort to using complicated and tedious electro-magnetic (EM) simulation tools if the effects of inductor coupling are to be considered. Isolation mechanisms such as guard rings take extra layout area, and fabrication processes with deep trench are not cost efficient. Clearly the design community would benefit from being able to model readily the results of inductor coupling. Such capability would allow for optimal usage of expensive isolation techniques.

The design of an accurate calibration-free experiment for measuring integrated inductor coupling, one aspect of the research herein reported, should be of benefit to a wide range of integrated circuit (IC) designers. The topology that is presented could be used by others to characterize inductor coupling in a particular process, and the results of the research experiment which was implemented in the IBM5HP BiCMOS process give insight into the magnitude of inductor coupling versus frequency, and inductor coupling versus inductor separation.

2.2 Oscillator Gain and Injection-Locking

Recall that the research experiment makes use of oscillator gain and oscillator injection-locking. The overly simplistic, yet popular view of the oscillator as a source generating block with no input signal and near perfect sinusoidal output is limiting. In fact, an

oscillator can be shown to behave much like a narrow band pass filter (BPF) with high gain.

Modelling the oscillator in such a fashion is not new. Authors such as Robins [6] have published, more than twenty years ago, detailed derivations of the pass band gain response of the oscillator, and Adler [9] derived expressions for predicting injection-locking bandwidth back in 1973. In the same year, Kurokawa published measured results of a solid-state oscillator showing the output spectrum of the oscillator as it approaches the injection-locked state, clearly demonstrating the oscillator's gain to injected tones.

The standard and logical use for an oscillator is as a signal source, but many designers who appreciate the pass band gain of the oscillator are making use of the topology as an active filter or gain block.

Figure 2.6: Eleventh Sub-Harmonic Injection-Locked Oscillator

Ahmed [10] demonstrated that injection-locked oscillators can fill traditional roles such as signal sources with low phase noise while consuming exceptionally little power. Ahmed's circuit is shown in Figure 2.6, where a differential cascode amplifier circuit's output is directly connected to the VCO tank circuit. Applying a 100 MHz

square-wave input to the amplifier stage, with the VCO's center frequency tuned to 1.1 GHz, results in the oscillator injection-locking to the eleventh harmonic of the input. The circuit has respectable phase noise of ≈ -100 dBc/Hz at a 50 kHz offset, and consumes only $690 \mu\text{W}$ from a 1.6 V supply.

DeVries [11] used a very similar circuit topology to the injection-locked oscillator in Figure 2.6 to create a high Q filter with digital tuning, shown in Figure 2.7.

Fig. 2: Simplified Circuit Diagram

Figure 2.7: Q -Enhanced Filter with Digital Tuning

Like the oscillator circuit, the filter circuit is comprised of a gain stage and an LC tank stage with negative resistance. The primary difference between the filter and the oscillator is that the g_m of the filter circuit is smaller than g_0 , the admittance of the tank. To make the circuit an oscillator, g_m is made larger than g_0 . DeVries designed the filter to be used at an intermediate frequency (IF) in an RF receiver as shown in Figure 2.8. The design showed promising results, demonstrating a $Q \approx 650$ at 500 MHz with a 750 kHz bandwidth while consuming a total power of only 1.02 mW from a 1.8 V supply.

Main [12] devised a simple FM-demodulator using an injection-locked oscillator, and Tokumitsu [13] designed a wide band combiner/divider amplifier with an injection-locked oscillator at the circuit's core. Wong [14] showed how injection-locked oscillators can be used to enable phase tuning beyond 180 degrees in a phased array antenna.

These examples among others, documented and published, show how versatile the oscillator circuit can be when its behaviour is properly understood. Consequently,

Figure 2.8: RF Back End with Q -Enhanced Filter

the theoretical analysis of VCO behaviour and the injection-locking phenomenon covered in the research for this thesis should appeal to a wide range of circuit designers. Understanding the VCO's true gain response opens the door to new design possibilities which would be impossible with only the traditional view of the oscillator.

Chapter 3

Theoretical Oscillator Frequency Response

An oscillator is often viewed as a tuned circuit that produces a dominant output tone at the resonant frequency ω_0 of the tank circuit with instantaneous deviations regarded as phase noise. The phase noise power at an offset $\Delta\omega$ from the oscillator's center frequency at ω_0 is well known to roll-off at 20 dB/dec where $\Delta\omega$ is large, yet little has been published about phase noise levels very close in to ω_0 . In fact, a common misconception is that the phase noise increases without bound as the offset frequency from ω_0 is arbitrarily reduced. Excluding the power supply, the only input to an ideal oscillator circuit is white noise. In order to produce what appears as a single output tone at ω_0 , the oscillator must behave as an extremely high Q band pass filter with exceptionally high, but finite, pass band gain. The commonly accepted phase noise model [15] which was presented without derivation is believed to have been derived first by Robins [6] and has been reformulated by Cloutier [16]. Robins derived expressions for the loaded bandwidth of the oscillator as a function of the free-running oscillator output power and the unloaded Q of the oscillator tank circuit. A similar derivation for the oscillator's loaded bandwidth and Q , with the help of a simple oscillator model, will be presented, and the frequency response outlined by the derived equations will be discussed.

3.1 A Simple Oscillator Model

An oscillator's time varying transconductor $g_m(t)$ coherently samples half the thermal noise in the presence of an anti-alias filter (the resonator), resulting in a high

gain transfer function with very narrow bandwidth. The integral of the phase noise versus frequency is equal to the square of the oscillator output time-domain waveform. Although some details of the linear oscillator model in Figure 3.1, which makes use of a constant time-averaged g_m , are debated in literature [17], [18], the model is surprisingly accurate for a high Q resonator as a high Q resonator reduces the effects of harmonics and aliasing not predicted by the linear model. The model lumps all input circuit losses and the input resistance of the transconductor into the resistor R_{in} while any reactive components at the input are assumed to have been tuned out by a circuit with low Q relative to that of the output tank. Similarly, R_L represents all output losses including that of the tank and the output conductance of the transconductor. Only for simplicity, the input impedance of the transconductor is assumed to be matched to the load impedance, i.e., $R_{in} = R_L$. For analysis, the feedback loop can be broken and the thermal noise of the load resistance represented by source V_N in series with R_L . The total input referred noise voltage density is called $V_{N,in}$. The noise factor of the equivalent amplifier (including R_{in}) is referred to as F .

Figure 3.1: Simple Oscillator Model

3.2 Oscillator Gains at Resonance

Recall that R_{in} and R_L are matched such that the impedance seen at the output of the transconductor at resonance is $R_L/2$. Therefore, the open loop voltage gain at

resonance is

$$\begin{aligned} G_V &= \frac{V_{out}}{V_{in}} \\ &= g_m \left(\frac{R_L}{2} \right) \end{aligned} \quad (3.1)$$

At resonance, the noise source sees impedance $2R_L$ and so the noise source contributes $V_N/2$ across the input of the transconductor. Thus, accounting for the noise contributed by R_{in} , the total input referred noise voltage density is

$$V_{N,in} = \sqrt{FkTR_L} \quad (3.2)$$

With the output of the oscillator applied to the input, $V_{in} = V_{out} + V_{N,in}$, and the output at resonance will be

$$\begin{aligned} V_{out} &= (V_{out} + V_{N,in}) \frac{g_m R_L}{2} \\ V_{out} \left(1 - \frac{g_m R_L}{2} \right) &= V_{N,in} \frac{g_m R_L}{2} \\ V_{out} &= \frac{\sqrt{FkTR_L} \frac{g_m R_L}{2}}{1 - \frac{g_m R_L}{2}} \\ V_{out}(\omega_0) &= \frac{V_{N,in} G_V}{1 - G_V} \end{aligned} \quad (3.3)$$

which is similar to the result obtained by Robins. Therefore, the output power spectral density of the oscillator at resonance is

$$P_{out,SD} = \frac{(G_V V_{N,in})^2}{R_L (1 - G_V)^2} \quad (3.4)$$

Since the only input to the oscillator is noise, the input power spectral density, accounting for the white noise from R_L and the noise contributed by the transconductor with noise factor F , is

$$\begin{aligned} P_{in,SD} &= \frac{(V_{N,in})^2}{R_{in}} \\ &= FkT \end{aligned} \quad (3.5)$$

Consequently, the power gain of the oscillator at resonance, when $R_{in} = R_L$, is

$$\begin{aligned} G_P &= \frac{(G_V)^2}{(1 - G_V)^2} \\ &= \frac{\left(\frac{g_m R_L}{2}\right)^2}{\left(1 - \frac{g_m R_L}{2}\right)^2} \end{aligned} \quad (3.6)$$

As an oscillator is simply a high Q band pass filter with exceptional pass band gain, B_L is used to represent the 3 dB bandwidth while Q_L represents the quality factor of the loaded oscillator. In contrast, B_U represents the 3 dB bandwidth of the unloaded tank circuit with quality factor Q_U . Recall that the noise bandwidth of a filter with 3 dB bandwidth B is $B\pi/2$, which is equal to the frequency span of a brick wall filter with the same output noise for an identical input noise - see Appendix A. Thus the integrated input power to the oscillator is

$$P_{in} = FkTB_L \frac{\pi}{2} \quad (3.7)$$

An alternative expression to (3.6), for the power gain of the oscillator at resonance, is

$$\begin{aligned} G_P &= \frac{P_{out}}{P_{in}} \\ &= \frac{P_{out}}{FkTB_L \frac{\pi}{2}} \end{aligned} \quad (3.8)$$

3.3 Tank Impedance Near Resonance

Consider again the tank circuit in Figure 3.1 with L , C and R_L in parallel with R_{in} , where $R_{in} = R_L$. The equivalent admittance is $Y_{tank} = 2/R_L + j\omega C + 1/(j\omega L)$. As $(\omega_0)^2 = 1/LC$, $1/L = C(\omega_0)^2$

$$Y_{tank}(\omega) = \frac{2}{R_L} + j\omega C \left[1 - \left(\frac{\omega_0}{\omega} \right)^2 \right] \quad (3.9)$$

Recalling that $B_U = 2/CR_L = \omega_0/Q_U$, $2Q_U/\omega_0 R_L$ can be substituted into (3.9) for C . The result is

$$Y_{tank}(\omega) = \frac{2}{R_L} \left(1 + jQ_U \frac{\omega}{\omega_0} \left[1 - \left(\frac{\omega_0}{\omega} \right)^2 \right] \right) \quad (3.10)$$

If ω is modelled as the summation of the resonant tank frequency ω_0 and an offset $\Delta\omega$, then (3.10) can be written as

$$Y_{tank}(\omega) = \frac{2}{R_L} \left(1 + jQ_U \frac{\omega_0 + \Delta\omega}{\omega_0} \left[1 - \left(\frac{\omega_0}{\omega_0 + \Delta\omega} \right)^2 \right] \right) \quad (3.11)$$

For small offset frequencies relative to the resonant tank frequency (i.e., when $\Delta\omega \ll \omega_0$), this equation simplifies as $1/(1+x) \approx 1-x$ for small values of x . To understand this simplification, consider the term $\left[1 - \left(\frac{\omega_0}{\omega_0 + \Delta\omega} \right)^2 \right]$ in (3.11). Rearranging yields $\left[1 - \left(\frac{1}{1 + \frac{\Delta\omega}{\omega_0}} \right)^2 \right]$, and applying the $1/(1+x) \approx 1-x$ simplification yields $\left[1 - \left(1 - \frac{\Delta\omega}{\omega_0} \right)^2 \right] = \left[1 - 1 + 2\frac{\Delta\omega}{\omega_0} - \left(\frac{\Delta\omega}{\omega_0} \right)^2 \right]$. Recognizing that $\left(\frac{\Delta\omega}{\omega_0} \right)^2 \ll 2\frac{\Delta\omega}{\omega_0}$, the term simplifies to $2\frac{\Delta\omega}{\omega_0}$. Substituting $2\frac{\Delta\omega}{\omega_0}$ into (3.11) for the original term yields

$$\begin{aligned} Y_{tank}(\omega) &= \frac{2}{R_L} \left(1 + jQ_U \left[1 + \frac{\Delta\omega}{\omega_0} \right] \left[2\frac{\Delta\omega}{\omega_0} \right] \right) \\ &= \frac{2}{R_L} \left(1 + j2Q_U \left[\frac{\Delta\omega}{\omega_0} + \left(\frac{\Delta\omega}{\omega_0} \right)^2 \right] \right) \end{aligned} \quad (3.12)$$

Recognizing that $\left(\frac{\Delta\omega}{\omega_0} \right) \gg \left(\frac{\Delta\omega}{\omega_0} \right)^2$, then

$$Y_{tank}(\omega) = \frac{2}{R_L} \left(1 + j2Q_U \frac{\Delta\omega}{\omega_0} \right) \quad (3.13)$$

As $Z_{tank}(\omega) = 1/Y_{tank}(\omega)$, the tank impedance near resonance is

$$Z_{tank}(\omega) = \frac{R_L}{2 \left(1 + j2Q_U \frac{\Delta\omega}{\omega_0} \right)} \quad (3.14)$$

3.4 Gains Near Resonance, Q , and Bandwidth

Taking the expression for V_{out} at resonance (3.3) and noting, that at a small $\Delta\omega$ from ω_0 the tank admittance is given by (3.13) and not simply $2/R_L$, the expression for V_{out} near resonance is

$$V_{out}(\omega) = \frac{\sqrt{FkTR_L} \left(\frac{g_m R_L}{2} \right)}{\left(1 - \frac{g_m R_L}{2} + j2Q_U \frac{\Delta\omega}{\omega_0} \right)} \quad (3.15)$$

This is an important result, similar to that obtained by Robins, which will be discussed shortly. The power spectral density, $P_{out}(\omega)$, is 3 dB down from the peak power spectral density, $P_{out}(\omega_0)$, when $2Q_U \Delta\omega/\omega_0 = 1 - (g_m R_L/2)$. As Q_L will be high, $B_L \approx 2\Delta\omega$ and as $B_U = \omega_0/Q_U$,

$$B_L = B_U \left(1 - \frac{g_m R_L}{2} \right) \quad (3.16)$$

Similarly, as $Q_L = \omega_0/B_L$,

$$Q_L = \frac{Q_U}{1 - \frac{g_m R_L}{2}} \quad (3.17)$$

Equating (3.6) with (3.8) and substituting for B_L gives

$$B_L = (B_U)^2 \frac{FkT}{P_{out}} \frac{\pi}{2} \left(\frac{g_m R_L}{2} \right)^2 \quad (3.18)$$

Noting that $g_m R_L/2$ is the loop gain of the limiting oscillator and is about 1 in steady state, (3.18) simplifies to

$$B_L = (B_U)^2 \frac{FkT}{P_{out}} \frac{\pi}{2} \quad (3.19)$$

which is the expression derived by Robins. Similarly,

$$Q_L = \frac{Q_U P_{out}}{FkTB_U} \frac{2}{\pi} \quad (3.20)$$

Equations (3.15), (3.19) and (3.20) are important, showing clearly that the output response of the oscillator resembles a band pass filter with high gain and a loaded bandwidth and Q factor that are simple functions of the output power and the Q of

the unloaded tank of the oscillator. This representation of the free-running oscillator supports the commonly accepted phase noise model [15]. Figure 3.2 summarizes the results pictorially. Solving (3.15) at $\Delta\omega = \omega_0/2Q_U$ with $g_m R_L/2 \approx 1$, corresponding

Figure 3.2: Oscillator Frequency Response (Power Spectral Density)

to an offset from ω_0 equal to the 3 dB corner of the unloaded tank circuit, yields a voltage spectral density gain of magnitude 1 which is equivalent to a power gain of 0 dB. Note that the simplified “s-domain” analysis applied here is essentially a linear analysis and yields correct average noise densities by assuming a constant time-averaged value for g_m . As a result of this assumption, the model fails to recognize the exponential nature of $g_m(t)$ which leads to compression, steady state operation, and spectral aliasing. For this reason the model is often criticized in literature [17], [18], although the small-signal linear model still gives insight into the fact that the phase noise, which can be measured, represents the transfer function of the oscillator, or its gain versus offset. This insight is useful in understanding the response of the oscillator to injected signals or coupled tones at low powers or at powers sufficient to injection-lock the oscillator.

The analysis just presented shows how the oscillator can be used as a gain agent so long as the applied input signal falls within the bandwidth of the oscillator. This concept is fundamental to the success of the oscillator coupling experiment which will be presented in Chapter 6. The experiment makes use of the gain of an integrated oscillator to measure a signal that is coupled from an injection-locked oscillator into the spectrum of a free-running oscillator by way of the oscillator tank inductors. In Chapter 4, time-domain simulations of the same simple oscillator model, on which the

derivation in this chapter was based, will confirm the gain response predicted by the theory. Similarly in Chapter 5, the measured behaviour of the integrated oscillators used in the experiment will be shown to follow the theoretical response predicted in this chapter. After such confirmations, the equations derived in this chapter can be used with confidence to extract the gain of the oscillator to the coupled tones measured in the experiment presented in Chapter 6, such that the amount of inductor coupling can be isolated and stated quantitatively.

Chapter 4

Simulated Oscillator Behaviour and Injection-Locking

In the case of an oscillator having injected tones at ω , an offset of $\Delta\omega$ from ω_0 , the linear model in Figure 3.1 with time-averaged g_m predicts gain but not spectral aliasing. Tones so small that the oscillator is not injection-locked, experience gain without having much effect on the oscillator feedback system. However, once the power in the injected tone is sufficient to lock the oscillator, the frequency response changes drastically as the time varying transconductance, $g_m(V_{out}(t)|_{\omega_0})$, is no longer correlated to ω_0 and instead follows $g_m(V_{out}(t)|_{\omega})$. The power at ω_0 falls to the noise floor as the tone is no longer coherently integrated by the large-signal oscillator. To demonstrate these behaviours, a similar model to the one used for the derivations in Chapter 3, shown in Figure 3.1, can be simulated in the time-domain.

4.1 A Time-Domain Simulation Model with Thermal Noise

To simulate the frequency response of the oscillator model shown in Figure 3.1, the circuit shown in Figure 4.1 is constructed in Agilent Technologies' ADS [19] software. To model the thermal noise of the load impedance, a pseudo-random noise voltage (SRC2) is placed in series with the load impedance as shown.

The oscillator model is tuned to a relatively low center frequency of 10 MHz to simplify simulation times and increase the accuracy of the fast Fourier transform (FFT) analysis performed on the time-domain signal. If the oscillator is tuned to

Figure 4.1: Time-Domain Oscillator Model with Thermal Noise

a higher frequency, plotting the phase noise of the oscillator versus offset frequency with a resolution of a few kHz would require extremely long simulation times. As the oscillation frequency is defined by $f_0 = 1/(2\pi\sqrt{LC})$, choosing $C = 200 \text{ pF}$ results in $L \approx 1.267 \mu\text{H}$. The oscillator model's tank circuit is assumed to have an unloaded quality factor of $Q_U = 10$ and, as $R_p = Q_U 2\pi f_0 L$, the resulting load impedance is $R_p \approx 796 \Omega$. As the noise voltage spectral density of resistor R_p can be calculated from $V_n = \sqrt{4kTR_p}$, the noise voltage density that needs to be represented in the simulation is $V_n \approx 3.56 \text{ nV}/\sqrt{\text{Hz}}$. As ADS will not model the thermal noise of a resistor in a time-domain simulation (doing it only in an AC or frequency domain noise simulation), a pseudo-random noise voltage is created using the VtDataset component, shown as voltage source SRC3 in Figure 4.1. Using MATLAB [20], a vector of 500 001 random Gaussian distributed voltages is created. The vector is used to define the voltage of the VtDataset component in the ADS simulation. The ADS time-domain simulation is conducted with a total simulation time of $500 \mu\text{s}$ and a time step of 1 nsec . The VtDataset component updates the voltage across its

terminals every 1 nsec with a new value from the vector of random numbers. The sampling frequency of the simulation is thus $f_s = 1/1 \text{ nsec} = 1 \text{ GHz}$. Hence, the noise voltage spectral density to be represented is $V_n = \sigma/\sqrt{f_s} \approx 3.56 \text{ nV}/\sqrt{\text{Hz}}$. Thus, the variance of the vector of voltage values created in MATLAB is set to $\sigma = 112.57 \mu\text{V}$, and the appropriate noise voltage spectral density of R_p is modelled in the time-domain simulation. Figure 4.2 shows the output voltage of the VtDataset component versus time, confirming the appropriate noise level of the circuit. Figure 4.3 shows a zoomed in view of the VtDataset voltage confirming a random noise voltage that changes every 1 nsec.

Figure 4.2: Modelled Noise Voltage Spectral Density of R_p

Figure 4.3: Zoomed View of Modelled Noise Voltage Spectral Density of R_p

Contrary to the linear simple model in Figure 3.1 which assumes a time-averaged g_m , the simulation model uses a voltage controlled current source defined by $I_{out} = 5e^{-3} (V_{in} - \frac{1}{10}(V_{in})^3)$ to represent the oscillator's transconductance. Figure 4.4 shows a plot of I_{out} versus V_{in} for the transconductor. When the output voltage swing of the oscillator is small, $g_m = 5$ mS, the slope of the curve in the linear region, which is larger than $1/R_L$ and the output voltage grows.

Figure 4.4: Transconductor Model Response

However, as the output voltage increases, the transconductance decreases as the slope approaches zero, and the output voltage of the oscillator ceases to grow at the point where $g_m - 1/R_L$ approaches zero. This behaviour closely resembles the transconductance of a transistor approaching saturation, often the main factor in limiting the output swing of an oscillator.

To simulate a tone that is injected or coupled into the oscillator, a sinusoidal voltage source (SRC3) is placed in series with the load impedance. With the injection source (SRC3) set to zero amplitude (which results in no injection), the time-domain output waveform of the simulated oscillator appears as shown in Figure 4.5.

To display the output spectrum of the oscillator, the time-domain simulation data from ADS is imported into MATLAB to provide added flexibility in conducting discrete Fourier transform (DFT) analysis on the waveform. Figure 4.6 shows the

Figure 4.5: Free-Running Time-Domain Simulated Oscillator Output

output spectrum of the oscillator calculated using both a DFT with a rectangular window and a DFT with a Hanning Window [21], [22] and [23] (also known as a Hann window, named after Austrian meteorologist, Julius von Hann). In both cases, the time-domain output data from the ADS simulation is truncated to eliminate the startup transient, where the waveform amplitude is growing and has yet to reach steady state, and the start and end points of the truncated data are chosen to minimize “phase step” error. In other words, the DFT analysis is always conducted on a time-domain waveform with steady state amplitude where the first recorded data point is right at the zero crossing of a rising edge and the last recorded data point is one data point before the zero crossing point of a rising edge. The MATLAB code for plotting both the rectangular windowed FFT and the Hanning windowed FFT is included in Appendix B for reference.

Figure 4.6 shows clearly the effects of using the Hanning window. Using the Hanning window reduces the numerical error caused by the small phase step between the first and last data points and decreases the noise floor of the output. A drawback of the Hanning window is that the spectrum shows some bin spillage of voltage from

Figure 4.6: Free-Running Frequency-Domain Simulated Oscillator Output

the bin with the highest voltage to the adjacent bins. The apparent result is less output voltage in the center bin with the Hanning windowed output than there is with the rectangular windowed output. To compensate for this drawback, an algorithm is written in MATLAB to sum all the voltages of the bins consecutively adjacent to the dominant bin and within 20 dB of the voltage in the dominant bin. This summation of voltages is printed to the plot window along with the frequency of the dominant bin. The output voltage and frequency of the dominant bin with the rectangular window is also printed to the plot window. Figure 4.6 shows a peak output measurement of 10 dBV using both windows, while the noise floor of the Hanning windowed transform is substantially lower. Consequently, the Hanning window is preferred over the rectangular window for measuring low power injected tones sufficiently offset from the carrier to avoid the bin spillage.

4.2 Oscillator Response to Low Injected Power

Injecting a sinusoidal tone with amplitude of $500\ \mu\text{V}$ at an offset of 50 kHz from the carrier results in the output spectrum shown in Figure 4.7.

Figure 4.7: Oscillator Spectrum with a Tone Injected at a 50 kHz Offset

The voltage levels indicated on Figure 4.7 for the Hanning window plot are calculated by the previously mentioned algorithm which adds the voltages of all the adjacent bins with voltages within 20 dB of the dominant bin voltage to account for bin spillage. The voltage levels indicated for the rectangular window plot are simply the voltages in the dominant bins. Figure 4.7 shows that by using the algorithm the voltages indicated at the dominant tones are virtually identical for both plots. The plot that was calculated using the Hanning window has a lower noise floor and more accurately measures the low voltages in the bins between the dominant tones, with the exception of the three or four bins right next to the dominant bin.

Figure 4.7 shows that the voltage at the injected tone is about 62 dBc relative to the voltage in the free-running tone at 9.94 MHz.

Figure 4.8 shows the output spectrum of the VCO with an injected tone of $500\text{ }\mu\text{V}$ amplitude at an offset of 500 kHz from the carrier, one decade further away than is the injected tone in Figure 4.7. The injected tone is about 81.5 dBc relative to the free-running tone, or 19.5 dB lower than the injected tone shown in Figure 4.7 which is one decade closer to the carrier. Therefore, the simulated response agrees with the theoretical frequency response of the oscillator derived in Chapter 3 and summarized in Figure 3.2, where the gain of the oscillator to injected tones rolls off at 20 dB/decade beyond the loaded 3 dB corner.

Figure 4.8: Oscillator Spectrum with a Tone Injected at a 500 kHz Offset

The benefit of using the Hanning window on the time-domain waveform is demonstrated in Figure 4.8 as the injected tone's voltage is so low that it is not visible using the standard rectangular window.

Both Figure 4.7 and Figure 4.8 show that there is an alias tone of equal amplitude to the injected tone on the other side of the carrier tone, equidistant from the carrier with the injected tone. Basic sampling theory predicts this alias tone.

As the injected tones, shown in Figure 4.7 and Figure 4.8, are so low in amplitude compared to the carrier, the amplitude of the carrier appears unchanged. As the

oscillator's limiting action always limits the oscillator amplitude at the same point, where $g_m - 2/R_L \approx 0$, the oscillator will always maintain constant output amplitude. As the sum of the powers in the oscillator's output tones is always the same, the simulations are in agreement with this statement.

4.3 Nearly Locked Oscillator Response to Injected Tones

Injecting a tone at a 20 kHz offset to the carrier with an amplitude of 100 mV results in the spectrum shown in Figure 4.9.

Figure 4.9: Oscillator Spectrum with a 100 mV Tone Injected at a 20 kHz Offset

Contrary to the simulation results shown in Figure 4.7 and Figure 4.8, the injected voltage amplitude shown in Figure 4.9 is large enough that the dominant tone of the oscillator is pulled towards the injected tone. Figure 4.9 shows that the injected tone at 9.92 MHz has pulled the dominant oscillator tone to 9.93 MHz from 9.94 MHz. In addition to this disruption, the voltage in the dominant tone has

dropped from 10 dBV to 7.6 dBV. The voltage in the injected and alias tones are large enough that in order to maintain constant output amplitude, the voltage at the dominant tone must decrease. The voltage in the injected tone is 3.9 dBV and the voltage in the first alias tone is 1.4 dBV. Summing only these three largest amplitudes yields an output level of 9.8 dBV, and summing all of the tones results in exactly 10 dBV, reinforcing the statement that the output level of the oscillator will remain unchanged at 10 dBV.

While basic sampling theory predicts the first alias tone to the injected tone on the other side of the carrier, the spectrum shown in Figure 4.9 has many alias tones which are very asymmetric. The asymmetry reflects the measured results published by Kurokawa [24]. To facilitate understanding this asymmetry, the output spectrum shown in Figure 4.9 can be down-converted to baseband in I and Q components and low pass filtered. The inverse tangent of the quotient of the two quadrature signals gives the instantaneous phase of the signal shown in Figure 4.9, and the time derivative of the instantaneous phase is the instantaneous frequency. Figure 4.10 shows this conversion process pictorially. This operation is performed on the voltage versus time data using MATLAB. For reference, the MATLAB code is included in Appendix C. Note that the simulation results showing asymmetric sidebands are a result of simulating the simplified model shown in Figure 4.1 which includes a non-linear transconductor.

Figure 4.10: Down-Conversion Process Yielding Frequency vs. Time

The result of this conversion process, the instantaneous VCO frequency relative to the pulled center frequency (at 9.93 MHz) versus time, is shown in Figure 4.11.

Figure 4.11: Instantaneous VCO Frequency vs. Time

Recall that the injected tone is 20 kHz below the free running frequency of the oscillator which is 9.94 MHz. The average frequency of the pulled oscillator is shown in Figure 4.9 to be 9.93 MHz and the instantaneous frequency shown in Figure 4.11 is plotted with reference to this 9.93 MHz average. Figure 4.11 shows that the VCO is slowly pulled towards the injected tone (at -10 kHz relative to 9.93 MHz) to be quickly snapped back towards the center frequency of the tank (at +10 kHz relative to 9.93 MHz). The oscillator overshoots the free-running frequency before being pulled back in, quickly, towards the injected tone. The average instantaneous frequency is 0 Hz relative to 9.93 MHz, or 9.93 MHz exactly. Figure 4.11 shows that the VCO spends more time at frequencies below the 9.93 MHz average than it does above it, demonstrating a sort of asymmetric form of FM modulation. At first glance, this observation would appear at odds with what is illustrated in Figure 4.9 which shows that even though the oscillator spends more time with an instantaneous frequency below 9.93 MHz, there is more power in the spectrum above 9.93 MHz. A brief review

of FM modulation helps to tie together what is illustrated in Figure 4.9 and Figure 4.11.

Recall that a signal with sinusoidal FM modulation can be represented by the time domain equation

$$s(t) = A_c \cos[2\pi f_c t + \beta \sin(2\pi f_m t)] \quad (4.1)$$

where β is the modulation index [25]. The modulation index is a ratio of the maximum frequency deviation (Δf) from the carrier (f_c) to the modulation frequency (f_m). Consequently, β can be calculated as

$$\beta = \frac{\Delta f}{f_m} \quad (4.2)$$

Expanding (4.1) yields

$$s(t) = A_c \cos(2\pi f_c t) \cos[\beta \sin(2\pi f_m t)] - A_c \sin(2\pi f_c t) \sin[\beta \sin(2\pi f_m t)] \quad (4.3)$$

If β is small relative to one radian, then the signal is said to be narrow-band frequency modulated. With $\beta \ll 1$, (4.3) simplifies to

$$s(t) \approx A_c \cos(2\pi f_c t) - \beta A_c \sin(2\pi f_c t) \sin(2\pi f_m t) \quad (4.4)$$

using the following approximations

$$\cos[\beta \sin(2\pi f_m t)] \approx 1 \quad (4.5)$$

and

$$\sin[\beta \sin(2\pi f_m t)] \approx \beta \sin(2\pi f_m t) \quad (4.6)$$

Finally, expanding (4.4) gives

$$s(t) \approx A_c \cos(2\pi f_c t) + \frac{1}{2} \beta A_c \{ \cos[2\pi(f_c + f_m)t] - \cos[2\pi(f_c - f_m)t] \} \quad (4.7)$$

Equation (4.7) shows that for perfectly sinusoidal, narrow-band, FM modulation, the amplitude of each sideband is proportional to $\beta/2$. This result can be applied to the

analysis of the nearly locked oscillator spectrum, shown in Figure 4.9, to make an interesting observation. Figure 4.11 shows that when the oscillator is pulled towards the injected tone at a relative frequency (to the 9.93 MHz average frequency) of -10 kHz, the maximum frequency deviation is about 6 kHz. When the oscillator quickly snaps forward in frequency towards the free-running frequency and beyond it, the maximum frequency deviation is about 17 kHz. Thus, while the oscillator frequency is below the average, the output signal can be said to have a smaller modulation bandwidth (β) than it does when it is momentarily above the average frequency. As the amplitudes of a sinusoidal FM modulated signal's sidebands are directly proportional to β , the nearly locked oscillator would be expected to have larger amplitude upper sidebands than lower sidebands. Thus, the high and low side maximum instantaneous frequency deviations of the oscillator from its average frequency, shown in Figure 4.11, appear to explain the asymmetry seen in Figure 4.9, despite the greater amount of time the oscillator spends with an instantaneous frequency below average.

If the fm modulation were sinusoidal, a symmetrical frequency response would be expected. A more detailed analysis is required to thoroughly explain the amplitude of each tone, yet the results shown in Figure 4.9 and Figure 4.11 prove that the simple oscillator model behaves much like the published behaviour of real oscillators as they approach lock. This consistency gives confidence to the theoretical model of the oscillator which will later be used to predict the gain of the oscillator to coupled tones in the inductor coupling experiment.

4.4 Injection-Locked Oscillator Response

If the injected voltage amplitude is increased to 200 mV at a 20 kHz offset from the carrier, the oscillator is injection-locked. Figure 4.12 shows the output spectrum of the injection-locked oscillator, oscillating at 9.92 MHz with the same 10 dBv output amplitude as the free-running oscillator.

Figure 4.12 shows that the voltage in the free-running tone and the alias tones falls to the noise floor when the oscillator is injection-locked.

The results presented have shown that simulating the simple model, which was used as the basis for the theoretical VCO gain response derived in Chapter 3,

Figure 4.12: Oscillator Spectrum with a 200 mV Tone Injected at a 20 kHz Offset

yields a gain response that agrees with the theoretical one. This agreement gives confidence to the theory which will later be used in Chapter 6 to extract the inductor coupling ratio from the measured data. The gain of the VCO to coupled tones has been shown to roll-off at 20 dB/dec as the coupled tone increases in offset from the VCO center frequency. This simulated result agrees with the theory. By adding a non-linear transconductor to the model, the simulation results show that injecting a tone on one side of the oscillator results in an alias tone on the other side of the oscillator. The simple model of the oscillator also demonstrated the injection locking phenomenon and confirmed that the total output power of the oscillator remains constant. Knowing that the output power of the injection-locked oscillator is identical to that of the free-running oscillator is important to understanding the methodology for the inductor coupling experiment. This methodology will be discussed in Chapter 6. In Chapter 5, the measured behaviour of the integrated oscillators used in the experiment will be presented and compared to the results shown in this chapter which were simulated using the simple model. Showing that the behaviour is the same in both cases confirms that the derivation in Chapter 3, which is based on the same

simple model simulated in Chapter 4, can be used to extract the oscillator gain from the tones measured in the experiment.

Chapter 5

Chip and Circuit Board Design and Measured Oscillator Behaviour

To validate the theoretical oscillator response to injected tones derived in Chapter 3 and simulated in Chapter 4, a test chip with two identical cross-coupled bipolar oscillators was designed and fabricated in the IBM5HP BiCMOS process with three metal layers. The purpose of the test chip was twofold: firstly, allowing for the response of a physical oscillator to injected signals to be measured, and secondly, providing a unique method of quantitatively measuring on-chip inductor coupling without the need for matching circuits, probe de-embedding, or difficult and time consuming calibrations. While the coupling experiment will be discussed in Chapter 6 along with the design and implementation of the on-chip resonator circuits, the design and implementation of the VCO/LNA pairs, the buffer circuits, and the printed circuit board (PCB) are presented as follows in Chapter 5. The measured inductor coupling results will be discussed in Chapter 6, while the presentation of measured oscillator behaviour follows in Chapter 5.

5.1 Experimental Chip Design

The actual schematic for the LNA/VCO pairs used in the experiment was designed using the Cadence Design Systems' suite of CAD tools. Specifically, SpectreRF [26] was used to simulate the RF schematic. The LNA/VCO pair schematic is shown in Figure 5.1. The two LNA/VCO pairs on the chip are identical and were constructed using a simple cross coupled negative resistance configuration as shown in Figure 5.1. The circuits were implemented using the IBM5HP BiCMOS process.

Figure 5.1: Low Noise Amplifier/Oscillator Schematic

5.1.1 LNA Design

The LNA used to injection-lock the VCO to an input signal is a very simple cascode topology with no degeneration and off-chip bias. As such, an off-chip bias-T (series capacitor and parallel inductance) is required to apply both the required DC bias level and the RF input signal to the LNA. The upper transistor in the cascode pair has a simple resistive bias and the base is AC grounded by a 650 fF metal-insulator-metal (MIM) capacitor to VSS. The LNA has a 1.0 k Ω load in parallel with the oscillator tank. The LNA design is deliberately not matched in order to avoid reducing the bandwidth over which the circuit will work. Therefore, the gain and noise of the amplifier are not optimal, but these factors are not critical to the success of the experiment. The goal of the LNA design is for the circuit to be simple and adequate for the purpose of the experiment, and the circuit meets this goal.

Notice that neither the input nor the output of the LNA is tuned to any particular frequency, giving the amplifier a wide operating bandwidth. This wide band design turned out to be crucial to the success of the experiment, as will be discussed in Chapter 6 in the section entitled *Oscillator Frequency Shift*, as the frequency of the oscillators turned out to be 3.7 GHz and not 5.0 GHz.

The output of the LNA is coupled to the tank of the VCO by a 650 fF MIM capacitor. While this coupling capacitance was intended to be small relative to the varactor diode capacitance of the oscillator tank, the nominal simulated varactor capacitance is only 629 fF (measured at 5 GHz with $V_{\text{ctrl}} = 2\text{V}$). Therefore, the circuit which was intended to be loosely-coupled is actually strongly-coupled. Nevertheless, a brief analysis proves that this phenomenon alone is not responsible for the oscillator frequency change. Figure 5.2 shows the small-signal equivalent circuit for the oscillator tank. The two varactors each contribute 629 fF and the center-tapped inductor is

Figure 5.2: Small-Signal Strongly-Coupled Resonator Equivalent Circuit

equivalent to two 650 pH inductors in parallel. Coupling capacitor C_c is 650 fF and the LNA load impedance is $1 \text{ k}\Omega$. A high impedance is seen looking into the cascode transistor of the LNA.

The approximate resonant frequency of the tank, determined from the varactor capacitances and the size of the center-tapped inductor, is

$$f_0 = \frac{1}{2\pi\sqrt{L_{tot}C_{tot}}} \approx 7.74\text{GHz} \quad (5.1)$$

This calculated result deviates from simulation results showing that the oscillator, with buffer connected but LNA disconnected, oscillates at 5.16 GHz as the input capacitance of the oscillator transistors have been neglected. Thus, in reality $C_{tot} \approx 2.93$ pF meaning that the transistor inputs and parasitics from the layout contribute an added capacitance of 1.63 pF in parallel with the circuit shown in Figure 5.2.

Consider the effect of the 650 fF coupling capacitor C_c and the 1 k Ω output load of the LNA. An equivalent parallel RC circuit to the series RC circuit can be found [27]. This equivalence is depicted in Figure 5.3. The equivalent parallel circuit's

Figure 5.3: Equivalent Series RC and Parallel RC Circuits

capacitance, where C_s and R_s are the capacitance and resistance of the series circuit, can be calculated as

$$C_p = \frac{C_s}{1 + (\omega C_s R_s)^2} \approx 1.56\text{fF} \quad (5.2)$$

Similarly, the parallel resistance is

$$\begin{aligned} R_p &= \frac{1 + (\omega C_s R_s)^2}{(\omega C_s)^2 R_s} \\ &\approx 1\text{k}\Omega \end{aligned} \quad (5.3)$$

The effect on the tank is that C_{tot} increases but slightly and consequently, the oscillation frequency will be decreased by a negligible amount.

Consider the effect of the parallel resistance, R_p , on the Q of the tank circuit. The simulated Q of the inductors (treating the center-tapped inductor as two inductors in parallel) is about 7.5 at 5 GHz and each inductor is about 650 pH. Thus, the parallel resistance of the inductors can be calculated as

$$\begin{aligned} R_{p,ind} &= Q\omega L \\ &\approx 76.6\Omega \end{aligned} \quad (5.4)$$

Therefore, with the R_p from the equivalent circuit for the coupling capacitor and LNA load, the total resistance in parallel with the LC tank is about 71.2 Ω . This means that having the LNA strongly-coupled to the VCO will effectively lower the Q of the VCO tank from 7.5 to about 7.0 which will widen the gain response of the VCO only slightly. Therefore, having the LNA output strongly-coupled to the VCO has little effect on the circuit's performance.

5.1.2 VCO and Buffer Design

Like the LNA, the VCO was designed with simplicity in mind. At the core of the VCO is an LC tank circuit made up of a center-tapped inductor and two varactors. The center-tapped inductor, being a customized layout, was modelled in ASITIC [28] and an equivalent circuit was used to represent the inductor's behaviour in Cadence simulations. Figure 5.4 shows the equivalent circuit (pi model) for the center-tapped inductor as determined through ASITIC simulations. Note that the model is not quite symmetrical, reflecting the asymmetry in the layout caused by the crossed metal layer sections. The layout is shown in Figure 6.1 which will be discussed in Chapter 6.

Figure 5.4: Center-Tapped Inductor Equivalent Circuit Schematic

The VCO uses cross coupled bipolar transistors, and the bias current for the block is set by a simple NMOS current mirror with a 2:1 size (and current) ratio. The VCO design is simple, and has not been optimized to minimize phase noise. Recall that the role of the VCOs in this experiment is to serve as a gain block to coupled tones at an offset from the VCO center frequency. The resulting poor (or high) phase noise is actually somewhat favourable, increasing the gain to coupled tones and making their output power more measurable. The simulated phase noise of the VCO with nominal tuning ($V_{\text{cntl}} = 2 \text{ V}$, $f_0 = 5 \text{ GHz}$) is shown in Figure 5.5. The simulated phase noise of the oscillator is -85 dBc at 100 kHz, with a bias current of 2 mA.

An emitter-follower buffer between the VCO tank and the output protects the oscillator tank from possible low load impedances which would decrease the Q of the tank and directly affect the gain response of the oscillator. In order to keep the oscillator loading as symmetrical as possible, an identical emitter-follower buffer is connected to the opposite side of the tank from the output. Two amplifier/oscillator circuits were implemented on the chip.

5.1.3 Chip Layout

Figure 5.6 shows the layout view of the final design and Figure 5.7 shows a microphotograph of the fabricated chip. Figure 5.6 shows how the resonators, which will be

Figure 5.5: Simulated Nominal VCO Phase Noise at 5 GHz

discussed further in Chapter 6, are located on the test chip in relation to the oscillators. With respect to the inductors, Resonator₁ is spaced 175 μm from Resonator₂, 305 μm from VCO₁ and 400 μm from VCO₂. All measurements are quoted from inductor center to inductor center. Similarly, Resonator₂ is spaced 305 μm from VCO₂ and 400 μm from VCO₁. The inductor for VCO₁ is spaced 175 μm from the inductor for VCO₂. The inductor for Resonator₂ was rotated 90 degrees with respect to the inductor for Resonator₁ to allow for coupling measurements to be made with a variety of inductor to inductor orientations.

5.2 Printed Circuit Board Design

To facilitate robust and repeatable testing of the experimental chip, a PCB was designed and fabricated so that the test chips could be mounted (chip on board) and wire-bonded to a board. Although this step increased the design and fabrication time as well as the cost of the experiment, it was deemed necessary for numerous reasons. The pad spacing and configuration shown in Figure 5.6 was originally designed with the intentions that each LNA/VCO pair would be contacted using an 8-pin RF probe while the resonators would be contacted with a 3-pin probe. While testing the chips using probes would be much faster than making and using a PCB, this method

Figure 5.6: Coupling Test Chip Layout

Figure 5.7: Coupling Test Chip Microphotograph

introduces many variables and difficulties into the measurement process. Landing probes onto an integrated circuit (IC) is a tricky and time consuming task, and ensuring all pins on a 3-pin or 8-pin probe are simultaneously in good contact with the IC is difficult. In a crowded test environment like a university laboratory, probe stations must be shared between many users necessitating that the time consuming process of setting up the probes and contacting the board must be repeated almost daily. At the same time, the pads on the IC tend to get scratched and damaged with repeated probing adversely affecting the repeatability of testing with the same chip.

The schematic for the PCB was designed using the OrCAD family of PCB design software tools. Specifically, OrCAD CaptureCIS [29] was used to design the schematic for the PCB and OrCAD Layout [30] was used to produce the layout for the PCB, including the Gerber files that were sent to the PCB foundry which fabricated the boards. The PCB is essentially divided into three sections, the supply decoupling circuit, the bias adjustment circuit, and the chip footprint and bondwire connection circuit.

5.2.1 PCB Supply Decoupling Circuit

The supply decoupling circuit produces the VCC voltage for the chip and shunts AC signals on VCC to ground at most frequencies. Figure 5.8 shows the schematic for this circuit. The circuit is comprised of lossy (to AC currents) ferrite bead inductors

Figure 5.8: PCB Supply Decoupling Circuit

in series with each of the three DC connections - positive supply, negative supply, and external ground. These inductors have very low DC resistance and have a 100 pF capacitance between the throughput and the third terminal; consequently the lines are further decoupled. On either side of the ferrite inductors in the positive and negative supply lines is an array of three decoupling capacitors with varying self-resonant frequencies. That the chassis ground from the power supply is only connected to the negative supply terminal at the far right of the circuit ensures that the negative supply line is the only return path to the power supply, and at the same time, keeps VCC and board ground from floating. The alternative, to short the negative supply and ground right at the power supply, would imbalance the current flow between the positive and negative paths. A series ferrite inductor on the chassis ground line is lossy to AC signals and the third terminal is left floating in order to further preserve the balance between the positive and negative supply lines. The ground of the sub-miniature type 'A' (SMA) connectors on the board (which are connected to the board ground only via 5.0 GHz self-resonant caps) will be connected to chassis ground at the signal generator and spectrum analyzer ends of the cables during testing. Thus, the SMA (and coaxial cable) ground will short chassis ground to board ground only at the target operating frequency of the experiment. This setup helps to ensure that the positive and negative supply line currents are matched with minimal to no DC current flow to chassis ground, while at the same time reducing the impact that small signals on chassis ground will have on the experiment.

5.2.2 PCB Bias Adjustment Circuit

The bias adjustment circuit enables the bias current for both the LNA/VCO pairs to be adjusted independently, as well as providing similar independence and adjustability for the varactor control voltage of each VCO. This circuit also enables the bias current, control voltage, and Vdd for each LNA/VCO to be nulled using separate 3-pin jumpers. The circuit is shown in Figure 5.9.

The Vdd bias circuit, like the chassis ground connection in the decoupling circuit, uses two lossy ferrite inductors in series close to the chip to supply Vdd1 and Vdd2 in an effort to minimize AC signals on the DC lines. Two jumpers are used to connect or disconnect the Vdd paths to VCC from the decoupling circuit.

Figure 5.9: PCB Bias Circuit

A footprint for series 0603 sized resistors (shown as $5.1\ \Omega$ resistors in Figure 5.9) is implemented to allow the possibility of adding small resistors to further dampen AC signals. These resistors were not needed and the footprint pads were shorted on the measured boards.

To set the control voltage of each VCO, a $2.4\ \text{k}\Omega$ resistor is connected in series with a $5\ \text{k}\Omega$ potentiometer and another $2.4\ \text{k}\Omega$ resistor between VCC and board ground. The connections enable the control voltage to be adjusted between $0.75\ \text{V}$ and $2.25\ \text{V}$. Like the Vdd paths, the control lines can be quickly enabled and disabled using jumpers.

Multi-turn $10\ \text{k}\Omega$ potentiometers are used between VCC and board ground, for fine adjustment of the bias current for each of the VCO/buffer pairs. Again, these lines are quickly enabled or disabled using jumpers.

5.2.3 PCB Chip Connection Circuit

The chip footprint and connection circuit is shown in Figure 5.10. This circuit defines the routing order to the chip, the chip to board ground connections, the DC connections, and the SMA connections to all RF ports. As previously stated, all four ground

Figure 5.10: PCB Chip Connection Circuit

connections on the SMA connectors are connected to board ground using 1.2 pF (5.0 GHz self-resonant) capacitors. Each DC supply line is decoupled to board ground using an array of three capacitors with varying self-resonant frequencies, the most important being the 1.2 pF cap (with a resonant frequency near the target operating frequency of the chip) placed closest to the chip. Notice that the control lines for the VCO, which are very sensitive to low frequency noise, which would modulate the VCO frequency, have larger decoupling caps with lower self-resonant frequencies than

the DC supply lines have. At the same time, the control lines enter the chip right next to the RF output line from the VCO, and consequently, a 1.2 pF decoupling cap is used close to the chip in order to ensure that the control line is grounded at the operating frequency of the chip. Without this cap, the integrity of the coplanar line connecting to the VCO output would be affected. This capacitor keeps the ground-signal-ground (at 5 GHz) integrity right from the SMA connector to the bondpad. The surface of the board to which the chip will be bonded, referred to as the paddle, is also grounded as shown in Figure 5.10.

5.2.4 PCB Construction and Coplanar Line Design

Once the PCB schematic is completed in OrCAD's CaptureCIS program, the design is exported to OrCAD's Layout program where the footprints for the known components are automatically generated. The footprint for the chip is created manually, and the routing for the DC lines and the coplanar RF lines are designed.

Figure 5.11: PCB Cross Section

The PCB is made of two sandwiched layers of FR4 separated by prepreg to achieve the desired final thickness. Figure 5.11 shows a detailed cross section of the PCB board with all layers and thicknesses.

The coplanar lines, which connect the RF ports of the chip to the SMA connectors, are designed using Agilent Technologies' LineCalc software tool within ADS [19]. Figure 5.12 shows the LineCalc results which claim that the 20 mils wide lines with 8 mils spacing to the ground plane have a characteristic impedance of about 50 Ω .

Figure 5.12: Coplanar Line LineCalc Result

The Gerber files, defining the layout of all layers for the PCB are shown in Appendix D. Figure 5.13 shows a photograph of the PCB, complete with the wire bonded test chip and all soldered components.

Figure 5.13: Photograph of Populated PCB with Test Chip

5.3 Measured Oscillator Behaviour

Figure 5.14 shows the circuit diagram for the two oscillators with integrated inductors spaced $175\text{ }\mu\text{m}$ apart from center-to-center. The response of one free-running oscillator to coupled tones from the other oscillator which is injection-locked and tunable will be discussed.

Figure 5.14: Coupled Oscillator Schematic

5.3.1 Free-Running Oscillator Response

The measured response of the free-running oscillator, VCO_2 , with nominal bias is shown in Figure 5.15. All measurements were made on a Rohde & Schwarz spectrum analyzer, model # FSIQ7. The center frequency of the oscillator is tunable from 2.35 GHz to 3.85 GHz across a 300 mV control voltage range adjusted using on-board

potentiometers. The supply voltage is 3 volts and the nominal current consumed by one VCO/LNA pair is 25 mA with no input signal to the LNA, that is, with the bottom device in the cascode LNA at 0 volts bias.

Figure 5.15: Free-Running Oscillator Phase Noise

Figure 5.15 shows the center frequency of the free-running oscillator tuned to 3.71 GHz with a measured phase noise of about -80 dBc/Hz at a 100 kHz offset. The output power of the free-running oscillator is about -8.8 dBm. At a 1 MHz offset, the measured phase noise is about -100 dBc/Hz, or 20 dB lower than the phase noise measured one decade closer to the carrier. This result strongly supports the 20 dB/decade gain roll-off predicted by the derivations and simulations in Chapter 3 and Chapter 4, which were based on the simple model.

5.3.2 VCO Response to Injected Tones with Low Power

With VCO₂ left free-running, VCO₁ is injection-locked to an external signal source applied to LNA₁ such that VCO₁ is both stable and tunable. The output power of VCO₁ is identical to that of VCO₂ at roughly -9 dBm. With VCO₁ tuned to 38 MHz below the free-running frequency of VCO₂, Figure 5.16 shows the output spectrum of VCO₂ with the coupled tone from VCO₁ at a power of -27 dBc. Figure 5.17 through Figure 5.19 show the output spectrum of VCO₂ with the frequency of VCO₁ increased such that the Δf between the two oscillator frequencies is 18 MHz, 9 MHz and 3.8 MHz respectively.

Figure 5.16: Oscillator Spectrum with 38 MHz Injection Offset

Figure 5.17: Oscillator Spectrum with 18 MHz Injection Offset

The progression towards oscillator injection-locking, shown from Figure 5.17 to Figure 5.19, proves clearly the 20 dB/decade (or 6 dB/octave) roll-off in oscillator gain beyond the loaded 3 dB corner. In Figure 5.18, VCO_1 is one octave closer to VCO_2 than it is in Figure 5.17 and the coupled tone is just over 6 dB higher in power. Similarly, Δf is one decade less in Figure 5.19 than it is in Figure 5.16 and the coupled power is about 20 dB higher. In all cases, the first alias tone (which is on the high-side of f_0 as the injection is on the low-side) is similar in power to the coupled tone. The second and higher order alias tones are highly asymmetric with the high-side tones being more powerful. Note the replication of the exact same response seen with the simulated oscillator in Chapter 4 and claimed by Kurokawa [24].

Figure 5.18: Oscillator Spectrum with 9 MHz Injection Offset

Figure 5.19: Oscillator Spectrum with 3.8 MHz Injection Offset

5.3.3 Nearly Locked Oscillator Response to Injected Tones

Figure 5.20 shows the output spectrum of VCO₂ with the injected tone from VCO₁ at $\Delta f = 1.5$ MHz below the dominant tone of VCO₂.

Figure 5.20: Oscillator Spectrum with 1.5 MHz Injection Offset

The spectrum shows extremely asymmetric alias tones and the injected tone is even at a higher power level than the tone at f_0 . As the power in the coupled tone and the alias tones is substantial, the power at f_0 has decreased from the previous measurements in order to maintain constant total output power for the oscillator. While the simulated oscillator in Chapter 4 showed that the dominant oscillator tone was attracted to the injected tone for injected powers that approach that of the free-running oscillator power, the dominant oscillator tone in the measured case appears

constant. This constancy is likely not legitimate, however, as the measured oscillator is powered by batteries and, consequently, the oscillator frequency tends to drift. During the measurements shown, the oscillator frequency tended to drift upwards appearing to cancel any attraction to the low-side injection.

Figure 5.21: Oscillator with Constant Power Source and Coupled Tone

Figure 5.22: Pulled Oscillator with Constant Power Source and Coupled Tone

To confirm that real oscillators do experience the attraction phenomenon shown in the simulations, Figure 5.21 and Figure 5.22 show the spectrum of a different integrated oscillator powered by a constant power source and subject to an injected

tone. In Figure 5.21, the oscillator frequency is $f_0 = 1.6905$ GHz and the high-side injected tone is 1.6 MHz away. In Figure 5.22, the injected tone is a decade closer to f_0 , only 165 kHz away, and the oscillator has been pulled to a center frequency of 1.6913 GHz. These measurements show that real oscillators do exhibit the attraction phenomenon.

Consider again the oscillator measured in Figure 5.20. Increasing the low-side injection frequency even further produces the output spectrum in Figure 5.23 where the oscillator is nearly injection-locked. Figure 5.23 shows that as the oscillator

Figure 5.23: Oscillator Spectrum Near Lock

approaches lock, the spectrum is still asymmetric. The power in the injected tone is substantially larger than at any other frequency as the transconductance approaches correlation with the injected tone rather than the free-running oscillator tone, f_0 .

5.3.4 Injection-Locked Oscillator Response

If the injected frequency is increased ever so slightly from the scenario shown in Figure 5.23, the oscillator is injection-locked, the transconductor is correlated to the injected tone, and the power in all other tones falls to the noise floor as shown in Figure 5.24. From Figure 5.23 to Figure 5.24, the window span and the resolution bandwidth (RBW) of the spectrum analyzer is reduced to facilitate a phase noise measurement of the injection-locked oscillator.

Figure 5.24: Injection-Locked Oscillator Spectrum

Figure 5.24 shows that the injection-locked oscillator has an output power of -9 dBm and a phase noise of about -100 dBc/Hz at an offset of 100 kHz from the carrier. Compare Figure 5.24 with Figure 5.15, showing the phase noise of the free-running

oscillator. Note that the output power of the oscillator is the same in both cases while the phase noise of the injection-locked oscillator is 20 dB better at the same offset. This observation is consistent with the model's prediction that the gain of the oscillator must decrease in order to keep the same total oscillator output power if there is an input tone within the loaded 3 dB bandwidth of the oscillator.

To further test this theory, VCO₂ is returned to the free-running state, and a tone is injected right at the center of the free-running oscillator response, f_0 , thereby injection-locking the oscillator at its free-running frequency. The injected power can be lowered substantially and the oscillator will remain injection-locked because of the extremely high gain at the center of the free-running oscillator. The injected power is varied and the total power of the oscillator is measured using an RBW of 10 MHz, while the power at the injected tone (at the center of the oscillator) is measured using an RBW of 1 Hz at zero span. The total (integral of the) phase noise can be calculated by subtracting the power at the injected tone from the total output power of the oscillator. This calculation is necessary because measuring the phase noise directly is impossible when the injected power is low. The phase noise is low enough that it falls well below the noise floor of the spectrum analyzer and is consequently unmeasurable. Figure 5.25 shows a summary of the measured results, where the horizontal axis corresponds to the injected power read off the signal generator at the input to LNA₂.

Figure 5.25 shows that the oscillator output power remains constant regardless of the injected power. As the injected power is increased, the gain of the oscillator saturates much like any other amplifier. In fact, the dotted line in Figure 5.25 very much resembles the 1 dB compression curve used to characterize an amplifier. When the injected power is low, the gain of the oscillator must be high in order to maintain constant output power and the phase noise (which is simply the output power of the noise subject to the gain response of the oscillator) is high. Conversely, when the injected power is increased, the gain of the oscillator is lowered in order to achieve unchanged output power and the phase noise is lower as a result. Note that the total output power of the oscillator in Figure 5.25 is only -14.5 dBm while it was measured to be around -9 dBm in Figure 5.16 through Figure 5.24. The power is lower because the batteries used while making the measurements for Figure 5.25 were partially spent and the bias conditions changed accordingly.

Figure 5.25: Injection-Locked Oscillator Phase Noise vs. Input Power

The measured results discussed in this chapter have shown that the integrated oscillators on the test chip, which are used in the inductor coupling experiment, follow the behaviour of the simulated simple model presented in Chapter 4 and the theory discussed in Chapter 3. With a strong correlation between theory, the simulated oscillator's behaviour, and the measured oscillator's behaviour, the theoretical model of the oscillator can be used with confidence to extract the oscillator gain out of the measured power of the coupled tone in the experiment. With the oscillator gain extracted from the measurement, the result is the amount of inductor coupling.

Specifically, the measured results shown in this chapter have demonstrated that, like the simulated oscillator model, real oscillators have a 20 dB/dec roll-off in gain beyond their loaded 3 dB corner. As well, the oscillator can be injection-locked to an injected tone and the output power is the same as that of the free-running oscillator. The measured oscillators also behaved like the simulated model by showing

an attraction towards the frequency of injected tones with high power, and asymmetric alias tones. Injection-locking the oscillator at the free-running frequency for various input power levels confirmed that the gain of the oscillator will adjust to keep the total output power constant at all times. This understanding of the fundamental behaviour of an oscillator is needed to fully appreciate the results of the coupling experiment which will be presented in Chapter 6.

Chapter 6

Using Oscillators to Measure Inductor Coupling

In the introductory chapter, the numerous effects that on-chip inductor coupling can have on the operation of an integrated circuit were discussed. EM fields can couple not only through the substrate but in the air surrounding the chip as the inductors behave much like two dimensional integrated spiral antennas. Previous experiments by [1], [2] and [3] have shown that coupling between on-chip inductors can be significant and that the magnitude of the coupling is affected by the spacing and orientation of the inductors. While successful in determining the factors that affect coupling, these experiments require careful matching and de-embedding in order to achieve quantitative results. The experiment presented in Chapter 6 is accurate, making use of oscillators and resonators with on-chip inductors in order to quantitatively analyze the coupling between inductors without the need to match or de-embed any circuits. The absolute ratio between two signals on-chip that experience similar losses is indicative of the coupling magnitude. The experiment uses an injection-locked on-chip oscillator acting as a transmitter and a free-running oscillator acting as a receiver. In this chapter, a brief summary of the EM theory involved in estimating inductor coupling and a review of the methods and tools used to simulate the amount of inductor coupling is presented. While the design and implementation of most of the ICs and the PCB used in the experiment were presented in Chapter 5, the purpose for each block is reviewed in Chapter 6, and the design and implementation of the on-chip resonators are presented in detail. Finally, the measured coupling results are presented and compared to the results of the EM simulations.

6.1 Near Field Inductor Analysis and Simulation

Consider an electrically small (circumference $< \lambda/10$) circular loop antenna of radius a , centered around the z -axis in the x - y plane. By means of using a spherical coordinate system, the radiated fields have been shown [31] to follow

$$H_r = j \frac{ka^2 I_0 \cos\theta}{2} \left(1 + \frac{1}{jkr}\right) \frac{\exp(-jkr)}{r^2} \quad (6.1)$$

$$H_\theta = -\frac{(ka)^2 I_0 \sin\theta}{4} \left(1 + \frac{1}{jkr} - \frac{1}{(kr)^2}\right) \frac{\exp(-jkr)}{r} \quad (6.2)$$

$$H_\phi = 0 \quad (6.3)$$

$$E_r = E_\theta = 0 \quad (6.4)$$

$$E_\phi = \eta \frac{(ka)^2 I_0 \sin\theta}{4} \left(1 + \frac{1}{jkr}\right) \frac{\exp(-jkr)}{r} \quad (6.5)$$

where I_0 is the current in the loop, $k = 2\pi/\lambda$, and r is the distance from the loop's center. Traditional analysis for antenna communication assumes a far field region of operation, where $1/r \gg 1/r^2$ (and $1/r \gg 1/r^3$) and thus the magnitudes of both the $\vec{E}$ and $\vec{H}$ fields drop off at a rate proportional to $\frac{1}{r}$. Careful analysis at frequencies below 10 GHz suggests, however, that for silicon based passive devices which use SiO_2 as the dielectric ($\epsilon_r \approx 4$), far field assumptions are invalid [32], [33]. The boundary between the near and far field regions of operation is defined by $kr = 1$ and occurs at $\lambda/2\pi$. This boundary is shown in Table 6.1 for a range of frequencies where λ_g represents the wavelength in SiO_2 and r_b corresponds to the separation at which the near field and far field regions of operation meet.

Table 6.1: Near/Far Field Boundary for Various Frequencies

Frequency (GHz)	r_b (cm)
1.0	15
2.0	7.5
5.0	3
10.0	1.5

On-chip separations between inductors can be $100\text{ }\mu\text{m}$ to 3 mm for 5 GHz applications. These separations correspond to $\frac{r_b}{300}$ and $\frac{r_b}{10}$, outlining unmistakably that on-chip coupling requires a near field analysis for all practical ICs. Modelling the interactions between on-chip inductors mathematically becomes complex, and accurate analysis is best performed using EM simulation tools such as Agilent's Momentum [34].

The on-chip inductors in the oscillators and resonators used for the experiment are three turn inductors with an outside diameter of $150\text{ }\mu\text{m}$, a turn width of $8\text{ }\mu\text{m}$, and a turn separation of $5\text{ }\mu\text{m}$. The separation between the two inductors in the oscillators is $175\text{ }\mu\text{m}$ from center-to-center. The two inductors are analyzed in Momentum [33] to yield an s-parameter model which can be simulated in ADS. Figure 6.1 shows the four port inductor model used in Momentum (including via models) and Figure 6.2 shows the results of the ADS simulation of the s-parameter model produced by Momentum. The coupling is calculated as the ratio between the output signal power

Figure 6.1: Momentum Inductor Model

at the terminals of one inductor and the input signal power being applied across the

Figure 6.2: Simulated Oscillator Coupling vs. Frequency

terminals of the other inductor. Note that the simulated coupling is essentially s_{21} of the s-parameter model, not to be confused with coupling coefficient k which refers only to the energy transfer between ideal inductors, neglecting the effects of parasitic and interwinding capacitances which are modelled by s_{21} .

For the given inductor layout, Momentum predicts that the coupling between the inductors in the oscillators is about -36 dB at 3.5 GHz.

6.2 A Novel Calibration Free Experiment

Figure 6.3 shows a block level diagram of the coupling experiment while the pseudo-schematic was shown in Figure 5.14 in Chapter 5. The use of two closely matched oscillators on the same chip allows the amount of inductor coupling to be measured without matching the input or output of the circuit or making absolute power measurements. The experiment uses an injection-locked on-chip oscillator acting as a transmitter and a free-running oscillator acting as a receiver.

To conduct the experiment, VCO_1 is injection-locked to an external input signal at $f_{LNA} = f_0 - \Delta f$ by way of an LNA with output coupled to VCO_1 's tapped resonator. Recall that the total output power of an injection-locked oscillator is

Figure 6.3: Experiment Setup

identical to the total output power of the same oscillator when it is operated free-running. The output spectrum of VCO₁ will couple into VCO₂ by way of the tank inductors. The output spectrum of VCO₂ is monitored with a spectrum analyzer and the ratio between the signal strength at f_0 and that at f_{LNA} is indicative of the inductor coupling magnitude. The total output power of both oscillators is the same and the gain applied by VCO₂ to the coupled tone at f_{LNA} can be calculated using the model or determined by measuring the phase noise of VCO₂. The only unknown, which can now be determined, is the magnitude of the inductor coupling.

The design and implementation of most of the integrated circuits on the test chip were discussed in Chapter 5, along with the design of the PCB. In addition to these circuits, two on-chip resonators were also used in the experiment. The design of the resonators is presented in section 6.3, and the measured results of the coupling experiment are shown in section 6.4.

6.3 Integrated Resonator Design

In order to be able to measure inductor coupling at more than one inductor separation and orientation, two stand-alone LC resonators were implemented on the test chip in close proximity to the oscillators. The resonators consist of the same 1.3 nH inductor used in the oscillators, but without the center-tap, and three 437 fF capacitors. The resonator's schematic is shown in Figure 6.4.

Figure 6.4: Resonator Schematic

The three capacitors are connected in series with each other and the inductor for a resonant frequency of 5.3 GHz. Note that a quick calculation using (5.1) predicts that the center frequency of the resonator should be about 11.5 GHz, yet simulations with the extracted layout which includes all parasitic and pad capacitances yield a center frequency of about 5.0 GHz. This large discrepancy is primarily due to the inductor's interwinding capacitance (of 259 fF) which is in parallel with the inductor and the three capacitors. Figure 6.5 shows a detailed simulation model of the resonator.

Figure 6.5: Detailed Resonator Schematic Model

Including the parasitic capacitances from the layout (pcell of the MIM cap), the actual value for each of the three MIM caps is modelled more closely as 487 fF, as seen at the top of Figure 6.5. The 0.11 pF and 0.22 pF capacitors in the center of the schematic represent the capacitance of the probe pads, but note that the 0.22 pF capacitance (of the two pads connected in parallel) is actually grounded on both sides and is consequently irrelevant. The 259 fF capacitance across the inductor represents the sum of all inter-winding capacitances and the 2.27 Ω resistors represent the series resistance of the metal. The 205 fF and 255 fF capacitors in Figure 6.5 represent the oxide capacitances while the substrate is modelled by the parallel RC networks at the bottom of the figure. The 80 fF capacitors were added to model the parasitic capacitances of the interconnects between the components. This circuit model is created by modelling the actual inductor structure using Momentum,

yielding a two port s-parameter model. The s-parameter model is imported into Applied Waves Research's Microwave Office software product [35], where a solution of best fit to Yue's inductor circuit model [36], commonly referred to as the compact model, is found to match the s-parameter model generated by Momentum. Some manual tweaking of component values is required to match the s-parameter model exactly. Note that Microwave Office assigns an inductance of 1.74 nH to the model. Figure 6.6 shows the simulated inductor response versus frequency using the detailed circuit model. At 5 GHz, the inductance is 1.74 nH and the self-resonance frequency is near 18.6 GHz.

$$\text{Eqn } L_{\text{eff}} = \text{imag}(1/Y(1,1)) / (2 * 3.1416 * \text{freq})$$

Figure 6.6: Inductance vs. Frequency

The MIM capacitors, pad capacitances, and routing capacitances are added to the model to create the model for the complete resonator. The real part of the input impedance of the resonator, simulated in ADS using the model in Figure 6.5, is shown in Figure 6.7. Figure 6.7 shows that the real part of the resonator's impedance is maximum near 5.4 GHz, corresponding to the point where the inductance and

capacitance cancel exactly leaving only the real resistance of the finite Q tank. This is the resonant frequency of the tank.

Figure 6.7: Resonator Real Input Impedance vs. Frequency

One side of the middle capacitor is grounded and the other side is connected to an output pad where the circuit will be probed. As a result of arranging the capacitors in this manner, the probing impedance will have minimal effect on the resonator Q . Consider the case where the probing impedance is $50\ \Omega$. An equivalent resistance across the inductor to the $50\ \Omega$ resistance across the middle capacitor can be found [27]. Figure 6.8 shows the equivalent circuits.

The equivalent resistance in parallel with the inductor (neglecting the parasitics) is calculated as

$$\begin{aligned}
 R_{eq} &= R \left(\frac{C_1 + C_2 + C_3}{C_1} \right)^2 \\
 &= 9R \\
 &= 450\Omega
 \end{aligned} \tag{6.6}$$

Figure 6.8: Tapped Capacitor Equivalent Circuit

Note once again that, with a simulated inductor $Q = 7.5$ at 5 GHz, the parallel resistance of the 1.3 nH resonator inductor can be calculated using (5.4) as

$$\begin{aligned} R_{p,res} &= Q\omega L \\ &\approx 306\Omega \end{aligned}$$

Thus, probing the resonator with a $50\ \Omega$ probe results in an equivalent total resistance of about $182\ \Omega$ in parallel with the resonator's inductor, and effectively lowers the Q of the resonator from 7.5 to 4.5, at 5 GHz. Had the resonator probing pads been connected directly across the inductor, the equivalent total resistance in parallel with the inductor during probing would have been approximately $43\ \Omega$ and the Q of the resonator would have been lowered from 7.5 to about 1. Therefore, the three capacitor design with the probe across the center capacitor helps to maximize the resonator Q during probing while maintaining a symmetric structure.

6.4 Measured Results

6.4.1 Oscillator Frequency Shift

The measured oscillator behaviour presented in Chapter 5 showed that, despite the oscillators being designed to resonate near 5.0 GHz, the actual frequency of the oscillators is only tunable from 2.35 GHz to 3.85 GHz when the on-chip varactors are

used. The reason for this deviation from the intended performance is somewhat puzzling. In the following paragraphs, an attempt will be made to provide some possible explanations for the deviation.

A previous analysis in Chapter 5 has shown that the LNA being strongly-coupled to the VCO should not significantly affect the center frequency of the oscillator. Even if the coupling capacitor had affected the frequency of the VCO, the effect should have been visible during simulation.

Each of the pads on the chip, including the pad for the varactor control voltage, is protected from electro-static discharge (ESD) by two diodes. The configuration used is standard in RF circuits. A reverse biased (under normal operation) diode between the pad and VSS, and a reverse biased diode between VDD and the pad protect the circuit from high and low voltages applied at the pad. High and low voltages are shunted to VDD and VSS respectively. These diodes undoubtedly contribute capacitances to the circuit, but all devices were extracted and simulated post layout. The extracted simulations suggested an oscillator center frequency near 5.0 GHz.

Bondwires are used to connect the pads on the chip to the PCB and a standard assumption is that each 1 mm of bondwire behaves like a 1 nH inductance. However, the only bondwire that is anywhere close to the tank of the VCOs is the one that connects VDD for the chip to the board, and each VCO tank connects to VDD at the center-tap of the differential inductor. This point is an AC ground point and, therefore, a series inductance from there to VDD should have no effect on the frequency of oscillation. Thus, the inductance of the bondwires is unlikely to have caused a change in the oscillation frequency.

The most likely explanation for the change in oscillation frequency is that the ASITIC model used in the VCO simulations did not accurately account for the interwinding capacitances of the inductors. Figure 6.5 and Figure 6.7 showed the use of Microwave Office to fit the Momentum s-parameter data for the inductors to the Yue model. The fitted Yue model identifies a 259 fF interwinding capacitance that greatly affects the center frequency of the resonators. As the VCO tank was thought to be adequately tunable using the varactors, less care was put into determining the exact frequency of oscillation and the simple ASITIC model was used. In retrospect, there is no reason that the Microwave Office model for the inductors could not have

been incorporated into the VCO simulations. After measuring the test chip, re-extracting the exact layout and simulating the VCO frequency became impossible due to system changes at Skyworks (where the layout was designed) which removed access to p-cells for the ESD diodes and the power clamp circuits, as well as models for the IBM5HP process components which were used on the chip.

Although slightly disappointing, the change in VCO frequency actually has only minor effects on the success of the experiment. Not tuned to any particular frequency, the LNA circuit offers adequate gain at 3.7 GHz to make the experiment possible at this new frequency. The only circuits that are tuned to 5.0 GHz are the on-chip resonators; consequently, coupling measurements made between the resonators and the oscillators are not ideal.

6.4.2 Inductor Coupling

Prior to conducting the coupling experiment, both oscillators are characterized to ensure identical behaviours. Recall that all measurements are made on a Rohde and Schwarz spectrum analyzer, model # FSIQ7.

The center frequency of both oscillators is tunable from 2.35 GHz to 3.85 GHz across a 300 mV control voltage range adjusted through the use of on-board potentiometers. The supply voltage is 3 volts and the nominal current consumed by one VCO/LNA pair is 25 mA with no input signal to the LNA, that is, with the bottom device in the cascode LNA at 0 volts bias.

To measure the coupling between inductors, one oscillator is injection-locked to a signal generator. Therefore, the offset relative to the second oscillator, which is free-running, is tunable. The power ratio between the free-running tone and the coupled tone from the injection-locked oscillator is measured at the output of the second oscillator. As the gain of the second oscillator to the coupled tone can be determined from the phase noise, the inductor coupling magnitude can be extracted. Figure 6.9 shows a typical spectrum of a coupled oscillator output. Figure 6.9 shows the free-running oscillator tuned to 3.322 GHz, the high-side injected tone 115 MHz away at 3.437 GHz, and the alias tones clearly visible.

The coupled tone's power is measured at numerous offset frequencies from the free-running tone. Figure 6.10 summarizes the measured power ratios between the free-running tone and the coupled tone as a function of offset frequency.

Figure 6.9: Oscillator Spectrum with Coupled Tone

The theoretical oscillator response, shown in Figure 3.2, suggests that the coupled power rolls off at approximately 20 dB/decade. The solid line in Figure 6.10 shows the theoretical coupling of -36 dB predicted by the oscillator theory and the Momentum simulation results shown in Figure 6.2.

The predicted response is based on a simulated inductor Q of 6.3 at 3.5 GHz. In keeping with the assumption that $R_{in} = R_L$, $Q_U \approx 3.15$, and the unloaded 3 dB corner of the oscillator is at an offset of about 550 MHz. Therefore, the expected power of the coupled tone is -36 dBc at an offset of 550 MHz where the gain of the oscillator is 0 dB. The power at the coupled tone increases at 20 dB/decade as the offset is decreased due to the gain of the amplifier as shown in Figure 3.2. The measured results suggest that the inductor coupling is closer to -35 dB, only 1

Figure 6.10: Summary of Coupled Power Ratio vs. Offset

dB higher than that predicted by the simulations, providing confirmation that the experiment is accurate.

A source of error is that the predicted response assumes matched oscillator input and output impedances which is almost certainly not the case. In addition, the inductor Q used in the prediction is obtained from simulation and could differ somewhat from the actual Q . The oscillator gain which is subtracted from the coupled power measurement to yield the inductor coupling is based on the simulated inductor Q and an assumed noise floor of -174 dBm/Hz. For improved accuracy, the noise floor could be measured to determine the oscillator gain experimentally from the measured phase noise shown in Figure 5.15, although the Rohde & Schwarz spectrum analyzer which is used for measuring the results has a lowest possible displayed average noise floor of about -150 dBc/Hz [37] which is too high to be able to measure the noise floor of the oscillator. Note that Figure 3.2 shows that the theoretical noise floor is actually at FKT and not $KT = -174$ dBm/Hz which was assumed. Assuming that $R_{in} = R_L$, which would suggest an $F \approx 2$, means that the noise floor was underestimated by 3 dB. However, the fact that the gain of the oscillator to a coupled tone is split evenly between the coupled tone and its alias tone was also neglected. These omissions mean that the oscillator gain versus frequency was underestimated by 3 dB (because of starting with 0 dB gain at the intersection of the noise floor and the unloaded 3

dB corner of the oscillator, and working up at 20 dB/dec), but overestimated by 3 dB (by neglecting the 3 dB power split between the coupled tone and its alias) at the same time. Thus, the two errors seemingly cancel.

As all the oscillator to oscillator measurements are made with a fixed inductor separation of 175 μm , coupling between one of the on-chip resonators and an oscillator is measured to provide results at a different separation. Figure 6.11 shows the relationship between inductor coupling and inductor separation from center-to-center at a frequency of 3.5 GHz. The solid line in Figure 6.11 represents simulated results of coupling versus inductor separation in Momentum, when the model of the on-chip inductors shown in Figure 6.5 and a signal frequency of 3.5 GHz are used. The data measured with the injection-locked oscillator coupling into the spectrum of the free-running oscillator is in strong agreement with the simulated coupling for the implemented inductors with 175 μm separation. An uncalibrated *LC* resonator spaced 305 μm from a test oscillator is used to measure coupling at a greater separation. A tone is injected into the on-chip resonator and the coupled tone is measured at the output of the free-running oscillator as before. When the gain of the oscillator is accounted for, the measured coupling is -56 dB which is about 6 dB lower than the predicted result. This deviation is understandable as, unlike the oscillator to oscillator test, the resonator to oscillator measurement's accuracy is affected by input mismatches and unknown on-chip losses. This result further attests to the need for the oscillator to oscillator test. Unfortunately, the resonators were designed to resonate near 5 GHz, consequently, there is significant input mismatch (necessary because of the center frequency of the oscillators being shifted) when connected to the signal generator operating near 3.5 GHz.

The results presented in Chapter 6 have demonstrated the success of the on-chip inductor coupling experiment. The measured coupling between the two 1.3 nH inductors spaced 175 μm apart is -35 dB, which is very close to the simulated coupling of -36 dB which was achieved using Momentum. In Chapter 5, the integrated oscillators used in the experiment were shown to have a gain response that agreed strongly with the theoretical one which was derived in Chapter 3 and simulated in Chapter 4. Therefore, the expected behaviour of the on-chip oscillators allowed for the oscillator model to be used to extract the theoretical oscillator gain from the measured data, leaving only the inductor coupling magnitude. Had measuring the noise floor

Figure 6.11: Inductor Coupling vs. Separation at 3.5 GHz

of the oscillator been possible, the gain of the oscillator could have been determined experimentally (for comparison) by measuring the phase noise and the noise floor of the oscillator and subtracting the two measurements. The experiment proved to measure inductor coupling accurately without the need for matching circuits, or any probe de-embedding or measurement calibrations. As the experiment makes use of the high gain of an oscillator, the experiment is very sensitive and can be used to measure small levels of coupling. The success of the experiment also attests to the robustness of the oscillator, used here in a nontraditional role as an active filter with high gain.

As a result of the oscillators oscillating at 3.5 GHz instead of 5.0 GHz (where they were designed to operate), the on-chip resonators were of little use for measuring inductor coupling versus separation and orientation. As the resonators did operate at 5.0 GHz, injecting an input tone near 3.5 GHz to the resonators in order to measure the coupling to a 3.5 GHz oscillator meant that the measured result was subject to unknown mismatch losses. However, the results did show that the coupling could be measured between a resonator and an oscillator and future experiments could build on the success of this experiment to accurately model the effects of inductor separation and orientation on coupling.

Chapter 7

Conclusion

7.1 Summary

The goal of the research work, to measure on-chip inductor coupling easily and accurately, was achieved indirectly through a study of the frequency response of *LC* oscillators.

The theoretical response of an oscillator has been derived using a linear circuit model. The linear derivations predict the frequency response of the oscillator to resemble a very narrow band pass filter with high gain, flat pass band response, and 20 dB/dec roll-off beyond the loaded 3 dB corner. The non-linear sampling of the transconductor explains the aliasing behaviour and the generally symmetrical phase noise response of an oscillator. Simulating the model yields results that support the band pass response, the 20 dB/dec roll-off in gain, and constant total output power. Measurements of an integrated oscillator in silicon suggest the same behaviour, and confirm that the gain of a locked oscillator, and thus the phase noise, decreases with increased injected power while the total output power remains constant. This understanding is crucial to making use of the oscillator's gain response in new technologies. As an oscillator has gain within a determinable bandwidth and an injection-locked oscillator has the same output power as an identical oscillator operated free-running, on-chip inductor coupling can be measured easily.

The design, implementation, and measurements of a unique experimental test chip and PCB for measuring on-chip inductor coupling has been presented. The research experiment requires no calibration, matching, or probe de-embedding and makes use of an injection-locked bipolar oscillator acting as a transmitter and a free-running bipolar oscillator behaving as a receiver. As the experiment makes use of the

high gain of an oscillator, the experiment is very sensitive and can be used to measure small levels of coupling. Inductor coupling of -35 dB was measured with ease, while lengthy EM simulations and oscillator theory predict -36 dB of coupling, virtually the same result for the 1.3 nH, three turn inductors spaced 175 μm apart. The measurement is accurate and supports the theoretical gain response of the oscillator to coupled tones. The observed high level of coupling further attests to the importance of considering inductor coupling in RFIC designs. The results of the experiment provide insight into the magnitude of inductor coupling versus both frequency and inductor separation.

7.2 Thesis Contributions

The primary contributions of this thesis to the RFIC design community can be summarized as follows.

- A simplified linear model of an LC oscillator has been used to derive expressions for oscillator gain versus frequency. Time-domain simulations of the simple model confirm the response predicted by the expressions.
- Measurements of integrated oscillators confirm the oscillator gain response predicted by the linear model. The demonstrated oscillator gain shows how oscillators can be used in non-traditional roles such as active filters or amplifiers.
- Simulations of the simple model and measurements of a real oscillator also confirm that the injection-locking phenomenon can be predicted, and that an injection-locked oscillator has the same output power as its free-running counterpart. These behavioural traits, and the high gain of the oscillator make the oscillator useful for measuring on-chip inductor coupling.
- The design and implementation of a calibration-free experiment which uses oscillators to measure integrated inductor coupling has been presented. The measured levels of inductor coupling are in strong agreement with the levels predicted by tedious EM simulations. The experimental results attest to the strong levels of on-chip inductor coupling present in RFICs implemented on silicon substrates.

- The success of the experiment shows that inductor coupling can be measured accurately using oscillators, and modifications to the experimental circuit could be made in order to evaluate the effectiveness of isolation techniques, such as deep trench, on a future test chip. As the experiment makes use of the high gain of an oscillator, the experiment is very sensitive and can be used to measure small levels of coupling.

7.3 Publications Resulting from this Work

As a direct result of the work presented here, the following papers were accepted for publication and will be presented at international conferences on integrated circuit design.

- [33] P. H. R. Popplewell, R. E. Amaya, M. Cloutier, and C. Plett, "Calibration-free on-chip inductor coupling experiment with injection-lockable VCOs," *To be presented at the IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, September, 2004
- [8] R. E. Amaya, P. H. R. Popplewell, M. Cloutier, and C. Plett, "On-chip passive coupling in Si substrates for RFIC applications," *To be presented at the IEEE Custom Integrated Circuits Conference*, October, 2004
- [38] P. H. R. Popplewell, R. E. Amaya, M. Cloutier, and C. Plett, "Analysis and measurements of injection-lockable oscillators for high-gain, high-Q applications," *To be presented at the IEEE International Analog VLSI Workshop*, October, 2004

7.4 Recommendations and Future Work

All in all, the coupling experiment was very successful, yet layout space constraints and an unexpected VCO center frequency error have left room for future work and improvements.

Although the inductor coupling experiment was successful in quantifying the coupling between the two inductors in the VCOs, a followup experiment could be

designed to expand on the results. For example, a similar test chip with multiple identical VCOs with different spacings and orientations to each other would help to quantify, more accurately, inductor coupling versus spacing and orientation. Due to constraints on the size of the layout for this experimental chip, there was only room for the two VCOs, and the resonators were added to provide some, albeit limited, experimental flexibility. As the VCOs on the chip resonated unexpectedly at 3.7 GHz while the resonators were tuned to 5.0 GHz, the results were not accurate. Multiple oscillators on the same chip would have been an improvement.

Another improvement on the test chip would be to put quiet grounds or deep trench between two VCOs for direct comparison with two identically arranged VCOs without any isolation mechanisms. This improvement would enable a quantitative analysis of some of the common techniques used to reduce inductor coupling in RFICs, and provide feedback as to the value of fabrication processes that provide expensive isolation options.

Yet another idea for a future experiment would be to take advantage of the strong levels of on-chip inductor coupling seen in this experiment. Perhaps coupled signals from one area of a die to another, or from one die to another, could be used to facilitate self-tests for integrated circuits. This idea was confirmed by primitive experiments in the lab, using two separate chips mounted on separate PCBs, which showed that coupling could be seen from one board to another, with signals coupling only through the air. This result, demonstrating that inductors can be used as integrated antennas, has many application possibilities such as in RF identification tags where producing small and cheap radios is desired.

Appendix A

Noise, SNR, NF, and Equivalent Noise Bandwidth

The information in this section is primarily a review of numerous elementary topics related to the theoretical oscillator derivation presented in Chapter 3. These integrated circuit fundamentals are available from many popular sources such as [39], [40], and [41] and are included here only to serve as a quick reference for the reader.

Noise in analog circuits can be defined primarily as either inherent noise or interference noise. Interference noise refers to the noise in a circuit which is a result of signal coupling from other parts of the same circuit or from other circuits in the surrounding environment. Inherent noise refers to the noise in the circuit which is a property of the devices and components that make up the circuit itself. Examples of inherent noise which are typically of concern are the thermal noise produced by a resistor, shot noise from PN junctions such as in a bipolar transistor, and flicker noise (also known as $1/f$ noise) which is typically larger in MOS transistors than it is in bipolar ones. As inherent noise is random, it is usually quantified by its root mean squared (rms) level.

A.1 Root Mean Squared and Power

Consider the time-domain noise voltage shown in Figure A.1. The average voltage is actually 0 V, but the instantaneous voltage has a Gaussian distribution with a σ level of $112\ \mu\text{V}$.

Figure A.1: Random Noise Voltage in the Time-Domain

Typically, as the average voltage is often 0 V as in Figure A.1, the magnitude of a random noise signal is referred to by its rms level. The rms level of a random noise voltage signal is calculated as

$$V_{n,rms} = \sqrt{\frac{1}{T} \int_0^T V_n^2(t) dt} \quad (\text{A.1})$$

Similarly, the rms level of a random noise current is

$$I_{n,rms} = \sqrt{\frac{1}{T} \int_0^T I_n^2(t) dt} \quad (\text{A.2})$$

Given the rms level of a noise voltage, the average power dissipated can be calculated. The average power dissipated by an rms voltage applied across a resistance ‘ R ’ can be calculated as

$$Power = V_{n,rms}^2(t) / R \quad (\text{A.3})$$

Similarly, the power dissipated by an rms current passing through a resistance ‘ R ’ is

$$Power = I_{n,rms}^2(t) * R \quad (\text{A.4})$$

With many sources of inherent noise in most circuits, the total noise power usually is dependent on the summation of numerous random sources.

A.2 Adding Random Sources

If two random noise sources, $V_{n1}(t)$ and $V_{n2}(t)$ are in series, then by (A.1) the total rms voltage across the two sources is defined as

$$V_{ntotal,rms} = \sqrt{\frac{1}{T} \int_0^T [V_{n1}(t) + V_{n2}(t)]^2 \partial t} \quad (\text{A.5})$$

Expanding (A.5) gives

$$[V_{ntotal,rms}]^2 = [V_{n1,rms}]^2 + [V_{n2,rms}]^2 + \frac{2}{T} \int_0^T [V_{n1}(t) + V_{n2}(t)] \partial t \quad (\text{A.6})$$

If $V_{n1}(t)$ and $V_{n2}(t)$ are uncorrelated, as is usually the case with random sources, then (A.6) reduces to

$$[V_{ntotal,rms}]^2 = [V_{n1,rms}]^2 + [V_{n2,rms}]^2 \quad (\text{A.7})$$

Once the total noise in the circuit has been added together to yield an equivalent total noise source, the total noise power can be found from (A.3) or (A.4). This result can be used to find the signal to noise ratio (SNR) at a circuit's input and output, and the noise figure of the circuit which is a commonly used figure of merit.

A.3 Signal to Noise Ratio, Noise Figure, and Cascaded Noise Figures

The SNR at any point in a circuit is equal to the signal power divided by the noise power and is usually stated in dB. To borrow an example from [39], assume a particular node in a circuit has a normalized (to a 1Ω resistor) signal power of $(V_{x,rms})^2$ and a normalized noise power of $(V_{n,rms})^2$. The SNR in dB at this node can be calculated as

$$\begin{aligned}
SNR &= 10 \log \frac{(V_{x,rms})^2}{(V_{n,rms})^2} \\
&= 20 \log \frac{V_{x,rms}}{V_{n,rms}}
\end{aligned} \tag{A.8}$$

Given the SNR at the input and output of a circuit, the noise factor and noise figure can be calculated. The noise factor of a circuit serves as an indication of how well the circuit amplifies or transmits a signal without introducing additional noise to it. The noise factor (F) can be calculated [27] as

$$\begin{aligned}
F &= \frac{SNR_{input}}{SNR_{output}} \\
&= \frac{\frac{S_i}{N_i}}{\frac{S_o}{N_o}} \\
&= \frac{\frac{S_i}{N_i}}{\frac{S_i G}{N_o}} \\
&= \frac{N_o}{G N_i}
\end{aligned} \tag{A.9}$$

where S_i and S_o are the input and output signal power respectively, N_i and N_o are the input and output noise power and G is the power gain of the circuit from input to output. The noise factor of a circuit is often stated in dB which is otherwise known as the noise figure of the circuit. Given the noise factor of a circuit, the noise figure can be calculated as

$$NF = 10 \log F \tag{A.10}$$

Note that in (A.9), the denominator is simply the noise at the output that originated at the source and has been amplified by the power gain of the circuit. If this component of the total noise power at the output is referred to as $N_{o,source}$ while the noise at the output that was added by the circuit is $N_{o,added}$ and the total output noise power is $N_{o,total}$, then (A.9) can be re-written as

$$\begin{aligned}
F &= \frac{N_{o,total}}{N_{o,source}} \\
&= \frac{N_{o,source} + N_{o,added}}{N_{o,source}} \\
&= 1 + \frac{N_{o,added}}{N_{o,source}}
\end{aligned} \tag{A.11}$$

To borrow an example from [27], consider the series chain of circuits shown in Figure A.2 at the block level.

Figure A.2: Cascaded Noise Figure Example

The total noise power at the output is

$$N_{o,total} = N_i G_1 G_2 G_3 + N_{o,added1} G_2 G_3 + N_{o,added2} G_3 + N_{o,added3} \tag{A.12}$$

and the component of the output noise power that's due to the source is

$$N_{o,source} = N_i G_1 G_2 G_3 \tag{A.13}$$

Thus, from (A.11), the noise factor of the cascaded circuit can be calculated as

$$\begin{aligned}
F &= \frac{N_{o,total}}{N_{o,source}} \\
&= 1 + \frac{N_{o,added1}}{N_i G_1} + \frac{N_{o,added2}}{N_i G_1 G_2} + \frac{N_{o,added3}}{N_i G_1 G_2 G_3} \\
&= F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2}
\end{aligned} \tag{A.14}$$

For a cascade of N blocks, the noise factor of the cascaded circuit is therefore

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \dots + \frac{F_N - 1}{G_1 G_2 \dots G_{N-1}} \quad (\text{A.15})$$

A.4 Noise Spectral Density

Unlike periodic signals such as sinusoids which have power at a distinct frequency, random noise signals have their power spread out over a wide frequency spectrum. By definition of being a random signal, the actual power of a random noise signal at one precise frequency is zero. Thus, random noise signals are quantified by their root spectral density. The root spectral density of a random voltage noise source is commonly measured in units of $V/\sqrt{\text{Hz}}$, and therefore, the normalized (power) spectral density is stated in units of V^2/Hz . Similarly, the root spectral density of a random current noise source is measured commonly in units of $A/\sqrt{\text{Hz}}$. The spectral density is an average normalized measurement of a signal's power within a 1 Hz bandwidth, referred to as $V_n^2(f)$ and $I_n^2(f)$ for voltage and current noise sources respectively.

Note that in a lab environment, noise signals are commonly measured with a spectrum analyzer which displays the power of a measured signal within the resolution bandwidth (RBW) of the instrument. Thus, increasing the RBW of the spectrum analyzer while measuring the power of a signal seemingly will increase the measured power. Understandably, this effect is a result of more noise passing through the spectrum analyzer's (now wider) band pass filter - the integral of which is the measured power of the signal. Normalizing the measured signal at any RBW back to a 1 Hz bandwidth should always give the same result, regardless of the RBW setting used when making the measurement.

A.5 White Noise

As previously mentioned, the spectral density of a noise signal is an average normalized measurement. Hence the spectral density is the average power within a 1 Hz bandwidth over an infinite frequency spectrum. White noise refers to a noise source which has the same power within a given bandwidth anywhere within an infinite

spectrum. Figure A.3 illustrates the comparison between an ideal, perfectly measured white noise signal and a noise signal where the power within a 1 Hz bandwidth appears to vary with frequency.

Figure A.3: White Noise Spectral Density Comparison

In both cases, the normalized spectral density is the same ($10 \mu\text{V}/\text{Hz}$), but in the case of the ideal white noise signal, the power within a 1 Hz bandwidth anywhere within the spectrum is equal to the spectral density of the signal. White noise gains its name from white light which is comprised of an equal weighting of the visible spectral components of light. Recall that the colour white is made up of an equal amount of all visible colours (frequencies) mixed together.

A.6 Equivalent Noise Bandwidth

The spectral density of a noise signal is an average level normalized to a 1 Hz bandwidth. To measure the spectral density of a noise signal with a spectrum analyzer without having to normalize the measurement later (or have the instrument normalize the reading for you) would require a RBW setting of 1 Hz. This measurement would be accurate only if the band pass filter used by the instrument was a “brick-wall” filter (or if the instrument accounts for filter roll-off in the reading). A brick-wall filter is a filter that has constant gain (usually one) within the pass band of the filter, while all other frequency components of a signal being filtered are eliminated entirely. In practice, a brick-wall filter is virtually impossible to build. Higher order filters are required to approach the response of the brick-wall filter at the cost of complexity. Thus, practical filters are often characterized by their equivalent noise bandwidth. The equivalent noise bandwidth of a filter is the frequency span of an ideal brick-wall filter which would produce the same rms output noise as the real filter having had the same white noise input applied to both filters. The pass band gains are the same for both filters.

As an example, consider the low pass RC filter shown in Figure A.4. The filter has a 3 dB bandwidth defined by

$$f_0 = \frac{1}{2\pi RC} \quad (\text{A.16})$$

Figure A.4: RC Low Pass Filter

The transfer function of the filter, $A(j2\pi f)$, is defined by

$$\begin{aligned}
A(j2\pi f) &= \frac{1}{1 + j\frac{f}{f_0}} \\
&= \frac{1 - j\frac{f}{f_0}}{1 + \left(\frac{f}{f_0}\right)^2} \\
&= \frac{1}{1 + \left(\frac{f}{f_0}\right)^2} - j\frac{\frac{f}{f_0}}{1 + \left(\frac{f}{f_0}\right)^2}
\end{aligned} \tag{A.17}$$

Recalling that the magnitude of a complex value $y = a + jb$ is $|y| = \sqrt{a^2 + b^2}$, the magnitude of the filter's transfer function can be calculated as

$$\begin{aligned}
|A(j2\pi f)| &= \sqrt{\frac{1}{\left[1 + \left(\frac{f}{f_0}\right)^2\right]^2} + \frac{\frac{f}{f_0}}{\left[1 + \left(\frac{f}{f_0}\right)^2\right]^2}} \\
&= \frac{1 + \left(\frac{f}{f_0}\right)^2}{\left[1 + \left(\frac{f}{f_0}\right)^2\right]^2} \\
&= \sqrt{\frac{1}{1 + \left(\frac{f}{f_0}\right)^2}}
\end{aligned} \tag{A.18}$$

Thus, if a white noise voltage source $V_{n,in}(f) = V_n$, where V_n is constant at all frequencies, is applied to the input of the filter, the rms output noise voltage can be calculated as

$$\begin{aligned}
V_{RC,out(rms)}^2 &= \int_0^\infty \frac{V_{n,in}^2}{1 + \left(\frac{f}{f_0}\right)^2} \partial f \\
&= V_{n,in}^2 f_0 \arctan\left(\frac{f}{f_0}\right) \Big|_0^\infty \\
&= \frac{\pi V_{n,in}^2 f_0}{2}
\end{aligned} \tag{A.19}$$

If the same input signal is applied to a brick-wall filter with bandwidth of f_x , the rms output noise voltage can be calculated as

$$\begin{aligned} V_{brick,out(rms)}^2 &= \int_0^{f_x} V_{n,in}^2 \partial f \\ &= V_{n,in}^2 f_x \end{aligned} \quad (A.20)$$

Thus, the output of the brick-wall filter is the same as that of the RC filter if $f_x = \frac{\pi}{2} f_0$. The gain responses of the RC filter and the equivalent brick-wall filter are shown in Figure A.5.

Figure A.5: LPF and Equivalent Brick Wall Filter Gain Responses

Appendix B

MATLAB Code for Windowed FFTs

```
%Peter Popplewell, July 22, 2003
clear all;
close all;

%Load the data to be analyzed, already truncated to best
%minimize phase error between first and last point
load tobefftd.txt;

%Determine step size and fft bin size from length of data
Vout=tobefftd(:,2);
tstep=tobefftd(2,1)-tobefftd(1,1);
Nfft=length(Vout);
fstep=1/(Nfft*tstep);

%Setup axis, perform fft and plot the result
%Multiply by 2 to fold over negative frequencies
%Get rid of any DC component that could be the max level
Freq=(0:fstep:fstep*(Nfft-1));
Spectrum=2*abs(fft(Vout)/Nfft);
Spectrum(1:5)=0;
figure;
plot(Freq(1:floor(Nfft/2))/1e6,20*log10(Spectrum(1:floor(Nfft/2))),
```

```

'r-o');
xlabel('Frequency (MHz)');
msg = sprintf('Spectrum (dBV/%2.0f kHz bin)',fstep/1000);
ylabel(msg);
axis([2100 2200 -180 0]);
grid on;

%Mark the maximum of the rectangular fft on the graph
[Max,IndexMax]=max(Spectrum(1:floor(Nfft/2)));
Fmax=Freq(IndexMax);
msg = sprintf('%2.2f dBV at %2.2f MHz',20*log10(Max),Fmax/1e6);
h=text((Fmax)/1e6,(20*log10(Max))+5,msg);
set(h,'Color','r');

%Mark the maximum upper sideband of the rectangular fft on the graph
[Max2,IndexMax2]=max(Spectrum(1:IndexMax-10));
Fmax2=Freq(IndexMax2);
msg = sprintf('%2.2f dBV at %2.2f MHz',20*log10(Max2),Fmax2/1e6);
h=text((Fmax2)/1e6,(20*log10(Max2))+5,msg);
set(h,'Color','r');

%Mark the maximum lower sideband of the rectangular fft on the graph
[Max3,IndexMax3]=max(Spectrum(IndexMax+10:IndexMax+300));
IndexMax3=IndexMax3+IndexMax+9;
Fmax3=Freq(IndexMax3);
msg = sprintf('%2.2f dBV at %2.2f MHz',20*log10(Max3),Fmax3/1e6);
h=text((Fmax3)/1e6,(20*log10(Max3))+5,msg);
set(h,'Color','r');

%Use Hanning window and plot to compare
%Multiply by 4 to account for negative frequencies and that
%psd returns volts squared
hold on;

```

```

Han_ans=psd(Vout,Nfft,1/tstep,Nfft)/Nfft;
Han_ans=Han_ans*4;
plot(Freq(1:length(Han_ans))/1e6,10*log10(Han_ans),'b-*');

%Get rid of any DC component that could be the max level
Han_ans(1:5)=0;

%Mark the maximum of the Hanning windowed fft on the graph,
%accounting for bin spillage
[MaxH,IndexMaxH]=max(Han_ans);
FmaxH=Freq(IndexMaxH);
i=1;
while(Han_ans(IndexMaxH-i)>=(0.01*Han_ans(IndexMaxH)))|
(Han_ans(IndexMaxH+i)>=(0.01*Han_ans(IndexMaxH)))
    if (Han_ans(IndexMaxH-i)>=(0.01*Han_ans(IndexMaxH)))
        MaxH=MaxH+Han_ans(IndexMaxH-i);
    end
    if (Han_ans(IndexMaxH+i)>=(0.01*Han_ans(IndexMaxH)))
        MaxH=MaxH+Han_ans(IndexMaxH+i);
    end
    i=i+1;
end
msg = sprintf('%2.2f dBV at %2.2f MHz',10*log10(MaxH),FmaxH/1e6);
h=text((FmaxH)/1e6,(10*log10(MaxH))+12,msg);
set(h,'Color','b');

%Mark the maximum 3 lower sidebands of the Hanning windowed fft on
%the graph, accounting for bin spillage
%Note that the vector indexing has to be tweaked to bracket the
%peak to be evaluated, i.e., the '-1000 to -5' below
[Max2H,IndexMax2H]=max(Han_ans(IndexMaxH-1000:IndexMaxH-5));
IndexMax2H=IndexMaxH-1001+IndexMax2H;
Fmax2H=Freq(IndexMax2H);

```

```

i=1;
while(Han_ans(IndexMax2H-i)>=(0.01*Han_ans(IndexMax2H))) |
(Han_ans(IndexMax2H+i)>=(0.01*Han_ans(IndexMax2H)))
    if (Han_ans(IndexMax2H-i)>=(0.01*Han_ans(IndexMax2H)))
        Max2H=Max2H+Han_ans(IndexMax2H-i);
    end
    if (Han_ans(IndexMax2H+i)>=(0.01*Han_ans(IndexMax2H)))
        Max2H=Max2H+Han_ans(IndexMax2H+i);
    end
    i=i+1;
end
msg = sprintf('%2.2f dBV at %2.2f MHz',10*log10(Max2H),Fmax2H/1e6);
h=text((Fmax2H)/1e6,(10*log10(Max2H))+12,msg);
set(h,'Color','b');

[Max4H,IndexMax4H]=max(Han_ans(IndexMax2H-1000:IndexMax2H-5));
IndexMax4H=IndexMax2H-1001+IndexMax4H;
Fmax4H=Freq(IndexMax4H);
i=1;
while(Han_ans(IndexMax4H-i)>=(0.01*Han_ans(IndexMax4H))) |
(Han_ans(IndexMax4H+i)>=(0.01*Han_ans(IndexMax4H)))
    if (Han_ans(IndexMax4H-i)>=(0.01*Han_ans(IndexMax4H)))
        Max4H=Max4H+Han_ans(IndexMax4H-i);
    end
    if (Han_ans(IndexMax4H+i)>=(0.01*Han_ans(IndexMax4H)))
        Max4H=Max4H+Han_ans(IndexMax4H+i);
    end
    i=i+1;
end
msg = sprintf('%2.2f dBV at %2.2f MHz',10*log10(Max4H),Fmax4H/1e6);
h=text((Fmax4H)/1e6,(10*log10(Max4H))+12,msg);
set(h,'Color','b');

```

```

[Max5H, IndexMax5H]=max(Han_ans(IndexMax4H-1000:IndexMax4H-2));
IndexMax5H=IndexMax4H-1001+IndexMax5H;
Fmax5H=Freq(IndexMax5H);
i=1;
while(Han_ans(IndexMax5H-i)>=(0.01*Han_ans(IndexMax5H))) |
(Han_ans(IndexMax5H+i)>=(0.01*Han_ans(IndexMax5H)))
    if (Han_ans(IndexMax5H-i)>=(0.01*Han_ans(IndexMax5H)))
        Max5H=Max5H+Han_ans(IndexMax5H-i);
    end
    if (Han_ans(IndexMax5H+i)>=(0.01*Han_ans(IndexMax5H)))
        Max5H=Max5H+Han_ans(IndexMax5H+i);
    end
    i=i+1;
end
msg = sprintf('%2.2f dBV at %2.2f MHz',10*log10(Max5H),Fmax5H/1e6);
h=text((Fmax5H)/1e6,(10*log10(Max5H))+12,msg);
set(h,'Color','b');

%Mark the maximum 3 upper sidebands of the Hanning windowed fft on
%the graph, accounting for bin spillage
%Note that the vector indexing has to be tweaked to bracket the
%peak to be evaluated, i.e., the '+5 to +1000' below
[Max3H, IndexMax3H]=max(Han_ans(IndexMaxH+5:IndexMaxH+1000));
IndexMax3H=IndexMax3H+IndexMaxH+4;
Fmax3H=Freq(IndexMax3H);
i=1;
while(Han_ans(IndexMax3H-i)>=(0.01*Han_ans(IndexMax3H))) |
(Han_ans(IndexMax3H+i)>=(0.01*Han_ans(IndexMax3H)))
    if (Han_ans(IndexMax3H-i)>=(0.01*Han_ans(IndexMax3H)))
        Max3H=Max3H+Han_ans(IndexMax3H-i);
    end
    if (Han_ans(IndexMax3H+i)>=(0.01*Han_ans(IndexMax3H)))
        Max3H=Max3H+Han_ans(IndexMax3H+i);
    end
end

```



```

        end
        i=i+1;
    end
    msg = sprintf('%2.2f dBV at %2.2f MHz',10*log10(Max3H),Fmax3H/1e6);
    h=text((Fmax3H)/1e6,(10*log10(Max3H))+12,msg);
    set(h,'Color','b');

    [Max6H,IndexMax6H]=max(Han_ans(IndexMax3H+5:IndexMax3H+1000));
    IndexMax6H=IndexMax6H+IndexMax3H+4;
    Fmax6H=Freq(IndexMax6H);
    i=1;
    while(Han_ans(IndexMax6H-i)>=(0.01*Han_ans(IndexMax6H))) |
        (Han_ans(IndexMax6H+i)>=(0.01*Han_ans(IndexMax6H)))
        if (Han_ans(IndexMax6H-i)>=(0.01*Han_ans(IndexMax6H)))
            Max6H=Max6H+Han_ans(IndexMax6H-i);
        end
        if (Han_ans(IndexMax6H+i)>=(0.01*Han_ans(IndexMax6H)))
            Max6H=Max6H+Han_ans(IndexMax6H+i);
        end
        i=i+1;
    end
    msg = sprintf('%2.2f dBV at %2.2f MHz',10*log10(Max6H),Fmax6H/1e6);
    h=text((Fmax6H)/1e6,(10*log10(Max6H))+12,msg);
    set(h,'Color','b');

    [Max7H,IndexMax7H]=max(Han_ans(IndexMax6H+5:IndexMax6H+1000));
    IndexMax7H=IndexMax7H+IndexMax6H+4;
    Fmax7H=Freq(IndexMax7H);
    i=1;
    while(Han_ans(IndexMax7H-i)>=(0.01*Han_ans(IndexMax7H))) |
        (Han_ans(IndexMax7H+i)>=(0.01*Han_ans(IndexMax7H)))
        if (Han_ans(IndexMax7H-i)>=(0.01*Han_ans(IndexMax7H)))
            Max7H=Max7H+Han_ans(IndexMax7H-i);
        end
        if (Han_ans(IndexMax7H+i)>=(0.01*Han_ans(IndexMax7H)))
            Max7H=Max7H+Han_ans(IndexMax7H+i);
        end
        i=i+1;
    end
    msg = sprintf('%2.2f dBV at %2.2f MHz',10*log10(Max7H),Fmax7H/1e6);
    h=text((Fmax7H)/1e6,(10*log10(Max7H))+12,msg);
    set(h,'Color','b');

```

```

end
if (Han_ans(IndexMax7H+i)>=(0.01*Han_ans(IndexMax7H)))
    Max7H=Max7H+Han_ans(IndexMax7H+i);
end
i=i+1;
end
msg = sprintf('%2.2f dBV at %2.2f MHz',10*log10(Max7H),Fmax7H/1e6);
h=text((Fmax7H)/1e6,(10*log10(Max7H))+12,msg);
set(h,'Color','b');

%Plot voltage vs. offset from carrier
figure;
semilogx((Freq(IndexMaxH:length(Han_ans)))-Freq(IndexMaxH),
(10*log10(Han_ans(IndexMaxH:length(Han_ans))))-(10*log10(MaxH)),'b-*');
xlabel('Offset Frequency from Carrier (Hz)');
msg = sprintf('Voltage Relative to Carrier (dBc/%2.0f kHz bin)',
fstep/1000);
ylabel(msg);
axis([50e3 5e6 -200 -100]);
grid on;

```

Appendix C

MATLAB Code for Instantaneous VCO Frequency

```
%Peter Popplewell, June 22, 2004
clear all;
close all;

%Load the voltage vs. time data to be analyzed, already truncated
%to best minimize phase error between first and last points
load tobefftd.txt;

%Determine step size and fft bin size from length of data
Vout=tobefftd(:,2);
tstep=tobefftd(2,1)-tobefftd(1,1);
Nfft=length(Vout);
fstep=1/(Nfft*tstep);

%Perform fft to find the average frequency
Freq=(0:fstep:fstep*(Nfft-1));
Spectrum=2*abs(fft(Vout)/Nfft);

%Find the maximum frequency, and thus the LO frequency for
%down-conversion
[Max,IndexMax]=max(Spectrum(1:floor(Nfft/2)));
Fmax=Freq(IndexMax);
```

```

omegaL0=2*pi*Fmax;

%Create I and Q
t=tstep*[0:1:Nfft-1];
sinL0=sin(t*omegaL0);
cosL0=cos(t*omegaL0);
I=Vout'.*sinL0; Q=Vout'.*cosL0;

%Design a Butterworth LPF and multiply to eliminate the 2*omegaL0
%components
[B,A]=butter(6,(2*pi*Fmax)/(10*(2*(1/tstep))));
Ifiltered=filter(B,A,I);
Qfiltered=filter(B,A,Q);

%Shift I component to eliminate divide by zero error
Ifiltered=Ifiltered+0.8;

%Calculate phase vs. time
Vout_phase=atan(Qfiltered./Ifiltered);

%Plot the derivative of the phase vs. time which is the
%instantaneous frequency
figure;
plot(t(2:length(t))/1e-6,diff(Vout_phase)/(1e3*2*pi*tstep));
xlabel('Time (usec)');
msg = sprintf('Instantaneous Frequency Relative to %2.2f MHz LO
(kHz)',Fmax/1e6);
ylabel(msg);
axis([0 500 -20 20]);

```

Appendix D

PCB Layout and Gerber Files

The following series of figures shows the Gerber layout views of the various layers that make up the printed circuit board (PCB) used in the experiment. Figure D.1 shows the top metal layer, made of 1/2 oz copper (Cu), which is used to route the 50 Ω coplanar lines that connect the RF inputs and outputs of the chip to the SMA connectors. The dark areas indicate where a layer of copper is deposited.

Figure D.1: PCB Top Metal Gerber View

The RF lines are the six lines in Figure D.1 with rounded corners which minimize fringing effects and keep the current density relatively constant across the width of the lines. Also, the top layer shown in Figure D.1 is used to route some of the DC bias and control lines and a metal ground pour fills the unused areas of the layer. All along the RF lines, vias are placed to ensure a solid ground connection between the

ground pour and the ground plane so that the coplanar lines have a good ground. The ground pads of the SMA connector footprints are connected to the ground pour only by way of 1.2 pF capacitors as explained in Chapter 6. The paddle for the chip is connected to the ground pour.

Note that many of the pads for components that connect to board ground are not covered directly by the ground pour although they are supposed to be connected to board ground. This connection style is known as “thermal relief” and is implemented on the left pad for the three pin jumper, shown in Figure D.2, which connects to board ground. The technique of connecting the pad to the ground pour with four small lines allows the pad to be heated easily by the soldering iron when the component is being mounted. Without the thermal relief, the iron would have to heat the entire ground plane and soldering the component to the board would take a long time.

Figure D.2: PCB Thermal Relief

Figure D.3: PCB Ground Plane Gerber View

Figure 5.11 shows that the ground plane of the board, which also is made of 1/2 oz Cu, sits below the first layer of FR4 as layer 2. The Gerber layout view of this layer is shown in Figure D.3. The small dots in Figure D.3 indicate a drill hole right

through the finished board, that is through all layers, where a via connects another layer to this plane. In the case of this layout view, white space represents the metal pour and the solid circles, referred to as knockouts, indicate an absence of metal around a via which is connecting two other layers together and is not supposed to connect to the ground plane. Therefore, the black outline around the view indicates the end of the metal pour. The wide dark outline indicates the edge of the board. Recall that the thermal relief technique is used to connect the pads of components that must be soldered to the board, and which are to connect to the metal pour (in this case the ground plane).

Figure D.4: PCB Power Plane Gerber View

Figure D.4 shows the power plane, layer 3 in Figure 5.11, that is divided into three sections. As in the ground plane view, white space indicates metal fill, dark circles indicate knockouts, and the small dots indicate vias connecting to the plane. The lower section of the plane is the general board VCC produced by the supply decoupling circuit. The upper left section is Vdd1 produced by the bias adjustment circuit for supplying LNA1 and VCO1 on the left side of the chip. Similarly, the top right section is Vdd2 for LNA2 and VCO2.

The bottom metal layer serves a purpose similar to that of the top layer as it is used for routing DC connections and mounting surface components. The bottom layer is made also of 1/2 oz Cu and is shown in Figure D.5. Unlike the top metal

layer, the bottom metal layer does not have any coplanar RF lines. The dark space represents the metal ground pour. Notice that the SMA connectors connect to the PCB on the sides with four prongs, consequently, there are two pads on both the top and bottom metal layers to solder to the connector. Like the pads on the top layer, the pads on the bottom layer are connected to the ground pour through 1.2 pF capacitors.

Figure D.5: PCB Bottom Metal Gerber View

Figure D.6 shows the top solder resistant layer. As in the ground and power plane views, the white space indicates the area of interest. A solder resistant coating is placed in the white space leaving the Cu of the top metal layer exposed in the solid dark regions such that surface components can be soldered to these regions.

The bottom solder resistant layer is shown in Figure D.7.

Figure D.8 shows the board's top silk screen layer which labels all of the components to be mounted on the top of the board and displays the purpose of the board and the names and affiliation of those persons involved in the experiment. Note that there is no similar silk screen for the bottom of the board. This omission was simply an error, albeit, a minor one. Luckily, as there are only a few components mounted to the bottom of the board, determining which component was to be mounted where was not a difficult task.

Figure D.6: PCB Top Solder Resist Gerber View

Figure D.7: PCB Bottom Solder Resist Gerber View

Figure D.8: PCB Top Silk Screen Gerber View

Figure D.9 shows an outline layer of all the components mounted to the top of the PCB and this outline served only as a tool in designing the board. This outline is not a layer that has any physical representation of the board. Note that the SMA connectors are easily visible in Figure D.9, overhanging the edges of the board. There is no such view for the bottom of the board.

Figure D.10 is the drill plan for the board. This view shows the locations on the board where a hole is drilled through all layers. A legend at the bottom of the view indicates the diameter of each hole and the number of holes with each diameter that are to be drilled through all layers of the finished board. These holes are used where vias connect one layer to another. Notice that, where convenient, vias surround the outer edges of the board to ensure a strong ground connection between the metal pour grounds of the top and bottom metal layers, and the ground plane of the board.

Figure D.9: PCB Top Component Outline Gerber View

DRILL CHART				
SYM	DIAM	TOL	QTY	NOTE
+	0.013		121	
x	0.031		6	
o	0.038		21	
TOTAL			148	

Figure D.10: PCB Drill Hole Plan Gerber View

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