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HIGH FREQUENCY INTEGRATED CIRCUIT DESIGN IN BICMOS
FOR MONOLITHIC TIMING RECOVERY

by

John R. Long, B.Sc.

A thesis submitted to the Faculty of Graduate Studies and Research
in partial fulfilment of the requirements for the degree of
Master of Engineering

Department of Electronics

Carleton University

Ottawa, Ontario

January, 1992

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submitted by John R. Long, B.Sc
in partial fulfilment of the requirements for
the degree of Master of Engineering

A handwritten signature in cursive script, reading "M. A. Copeland", positioned above a horizontal line.

Thesis Co-Supervisor

A handwritten signature in cursive script, reading "R. Hadaway", positioned above a horizontal line.

Thesis Co-Supervisor

A handwritten signature in cursive script, reading "J. Wright", positioned above a horizontal line.

Chair, Department of Electronics

Carleton University
January 13, 1992.

ABSTRACT

The implementation of a monolithic timing recovery circuit in silicon BiCMOS technology for baseband data transmission systems is explored in this thesis. The operating characteristics of the phase-locked loop (PLL) and the impact of timing recovery design constraints upon the selection of PLL components are outlined. Various PLL architectures are analyzed and a structure which is suitable for implementation of a fully-monolithic timing recovery circuit is selected as a basis for further investigation. A high speed phase detector circuit which is based upon the ECL latching comparator is proposed, and an experimental master/slave flip-flop circuit, which has been designed and fabricated in a sub-micron BiCMOS process in order to investigate the performance capabilities of the latching comparator circuit, is discussed in detail. Two alternatives to the implementation of a monolithic voltage-controlled oscillator (VCO) are considered. A broadband microwave amplifier and monolithic inductors which could be applied to the design of a high frequency oscillator have been designed, fabricated and tested. Also, the design and characterization of a monolithic phase-shift ring oscillator circuit is described. A modification to the active phase-shift network of this oscillator is introduced, which could improve the spectral purity of the ring oscillator output signal.

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1. Introduction

Monolithic integrated circuits which can operate at frequencies in the GHz range are required for applications such as wireless digital communications and fibre-optic data transmission. The design and implementation of circuits which could be used in many high frequency applications will be investigated in this thesis. A monolithic timing recovery circuit capable of operation above 1 GHz has been chosen as the application context for this circuit work. However, it should be noted that the circuits developed here will have a much broader applicability.

1.1 The Challenge in Silicon BiCMOS Technology

Discrete circuit components are often used at frequencies above 100 MHz because of the performance limitations of integrated devices, and because of circuit tuning and impedance matching requirements. Gallium Arsenide (GaAs) circuit technology has been developed for high frequency applications but the complexity of these circuits is limited by high power consumption. Also, GaAs analog circuit performance is limited by poor device matching, low active device transconductance and high $1/f$ noise [1]. Recent advances in silicon bipolar devices have resulted in the development of polysilicon emitter bipolar transistors which have high transconductance, wide bandwidth (f_T between 5 and 12 GHz) and CMOS process compatibility with only minor process modifications [2]. This combined bipolar and CMOS (BiCMOS) technology allows integration of dense, low power CMOS circuits and high frequency bipolar circuitry on the same chip. The opportunities offered by the unique capabilities of BiCMOS technology in the design of monolithic timing recovery circuits will be explored in this study.

1.2 Timing Recovery in Digital Communications

The application chosen for the high-speed circuit work in this thesis is timing recovery in repeatered fibre-optic communications systems. Digital signal transmission is preferred for high-speed fibre-optic channels because of the poor linearity of electro-optic sources such as light-emitting diodes and Lasers [3]. An important feature of digital transmission is the

ability to reconstruct the transmitted pulse train almost perfectly and remove the effects of noise and distortion. This process, called signal regeneration, uses a regenerative repeater which consists of equalizer, timing recovery, and regenerator circuits as illustrated in Figure 1.1. Repeaters are placed at uniform intervals along the transmission path, making it possible to transmit a digital signal over long distances without introducing significant impairment of the signal quality. The preamplifier and equalizer compensate for distortion introduced during transmission, and amplify the signal to the level required by the regenerator circuit. The regenerator is triggered by the timing clock in order to sample the received signal and decide whether a 1 or 0 pulse was transmitted. The function of the timing recovery circuit is to maintain uniform spacing of the regenerated pulses and to define the best time to sample the equalized pulse train in terms of the received signal-to-noise ratio. Timing information is derived directly from the received signal in order to reduce hardware complexity, transmission bandwidth, and power consumption.

Figure 1.1 : Block diagram of a regenerative repeater.

If interference due to noise and improper equalization is sufficiently large, an incorrect decision can be made by the regenerator and the retimed pulse train will contain an error. Also, the pulses at the regenerator output are not uniformly spaced because of phase variations in the recovered timing clock. A practical timing recovery circuit cannot perfectly duplicate the timing clock used at the remote transmitter. However, the average frequency of the recovered clock must match the transmitter clock in order to successfully regenerate the received data stream without errors. Timing jitter, which is a fluctuation in the phase of the recovered clock, is caused by a combination of random noise and other systematic sources such as a circuit response to specific data patterns. Although timing jitter is always present in practical timing recovery circuits, it can be reduced to any level desired by

improved design or through the use of additional synchronizers. The bit stream emerging from the regenerator will have the same timing jitter as the timing clock. Systems such as data terminals and computers are tolerant of moderate amounts of timing jitter. However, pulse code modulated (PCM) speech is distorted by the non-uniform sampling introduced by timing jitter. Also, long-haul communications systems accumulate timing jitter contributed by each repeater, which must be accounted for in the timing recovery circuit design.

The phase alignment between received data and recovered clock is an important consideration in the circuit design at high frequencies. The path length between the timing recovery circuit output and the regenerator circuit introduces a phase shift which can result in non-optimal sampling of the received signal, due to temperature changes and component variations caused by aging and manufacturing tolerances. The phase alignment of the transitions in the received signal and the sampling clock should be optimized for the anticipated range of operating conditions. This requires some means of phase shifting the clock with respect to the received data.

Figure 1.2: Deductive timing recovery.

Timing recovery methods can be classified as either deductive or inductive. In a deductive timing recovery circuit, the timing clock is directly extracted from the received signal, as shown in Figure 1.2. A non-linear circuit generates a periodic signal called the timing tone from the received data signal. The average frequency of the timing tone is equal to the incoming bit-rate, and timing jitter in the extracted tone can be filtered using a narrowband (high-Q) passive filter or a phase-locked loop (PLL). This filtered timing tone is used as a clock to synchronize the received data stream. A phase-shifting network at the filter output is used to ensure correct phase alignment of the recovered clock with the received data at

the data regenerator. High frequency timing recovery circuits have traditionally used this approach because of design simplicity, and circuits operating at frequencies exceeding 5 GHz [4] have been built using this technique.

Figure 1.3 shows an inductive timing recovery system, which uses the phase-locked loop to recover timing information indirectly. In this circuit, the PLL is not used as a narrowband post-filter but rather as an integral part of the timing recovery method [5]. The phase relationship between zero-crossings in the locally generated timing clock and zero-crossings in the received data is measured to derive an estimate of the phase error. The error signal is fed-back to update the phase of the timing clock, attempting to reduce the error to zero. When the error signal is minimized, the timing clock will be synchronized to the transitions in the received waveform and synchronization is maintained by the feedback loop regardless of temperature and component variations. Practical inductive timing recoveries are limited in operating frequency either by the bandwidth of the phase detection circuit or the upper frequency limit of the timing clock generator [6].

Figure 1.3 : Inductive timing recovery.

Although complete phase-locked loop circuits have been monolithically integrated for specific applications, the requirements of high frequency timing recovery make complete monolithic integration impossible with classical circuit topologies. Device or circuit bandwidth is only one of the requirements which must be satisfied in development of a viable design. The system architecture must also be considered in order to fully exploit the capabilities offered by BiCMOS technology.

1.3 Thesis Objectives and Scope

One of the objectives of this work is to investigate the opportunities provided by this new circuit technology to advance the performance of circuits and systems. Timing recovery in baseband data transmission has been chosen as the applications context for this work. The level of system integration in data transmission systems could be improved through the development of a single-chip timing recovery circuit. BiCMOS circuit technology may offer the circuit design flexibility and level of device integration required to achieve this goal. The high-speed capability of this technology will be exploited in the design of experimental circuits. A clock rate greater than 1 GHz has been chosen as the design objective, because it is compatible with the current state-of-the-art in fibre-optic transmitter and receiver technology. This represents an almost order of magnitude increase in operating speed for monolithic loops in silicon technology.

The phase-locked loop (PLL) is considered to be a key component in the design of a single-chip or monolithic circuit because the PLL can operate at higher frequencies than other narrowband active or passive IC filters. Various PLL designs are examined and a viable architecture for a completely monolithic timing recovery circuit is selected for further study.

The design, layout and experimental measurement of the entire timing recovery circuit is beyond the scope of this work. Aside from the design of high frequency circuitry, many complex system and circuit design issues must be resolved before a timing recovery circuit can be implemented with a reasonable probability of success. Issues such as system simulation, high frequency device modelling and the integration of sensitive analog and digital circuits operating at radio frequencies are just a few examples. Therefore this work has concentrated on the key high-speed elements of the timing recovery PLL, which have been designed and implemented in a sub-micron BiCMOS process. The experimental results of this study could be used to further define the solution for monolithic timing recovery and form a basis for future work in this area.

1.4 Thesis Outline

The operating characteristics of the phase-locked loop and the impact of timing recovery design constraints upon the selection of PLL components will be outlined in Chapter 2 of this thesis. These design constraints are defined within the context of repeated data

transmission applications. Various PLL architectures which can meet the timing recovery circuit design goals are then analyzed in Chapter 3. A PLL structure which could be used to implement a fully-monolithic timing recovery circuit is selected as the basis for further investigation.

The operating frequency of a PLL in timing recovery applications is limited by either the frequency range of the local clock source (i.e., voltage-controlled oscillator) or the bandwidth of the phase detector circuit. In the remaining chapters of the thesis, the design of these frequency limiting components will be studied in detail and novel circuits which can be monolithically implemented in BiCMOS technology are proposed.

The process technology used to implement the circuit designs studied in this thesis was provided by Northern Telecom Electronics. High performance npn bipolar and complementary MOS transistors can both be fabricated within this BiCMOS process. It features a polysilicon emitter bipolar transistor with a $0.8\text{ }\mu\text{m}$ wide emitter and (minimum) $7\text{ }\mu\text{m}$ base-to-base pitch, junction and field oxide device isolation, polysilicon resistors, and three layer metallization for device interconnection [7]. Minimum geometry bipolar transistors with a unity gain frequency (f_T) of between 8 and 10 GHz at a collector-emitter bias voltage of one Volt ($V_{CE} = 1\text{ V}$) can be fabricated with this technology.

The design of a high-speed phase detector is considered in the Chapter 4. An ECL latching comparator forms the basis of the phase detector design, and an experimental flip-flop circuit was designed and fabricated in order to investigate the performance capabilities of the latching comparator. A flip-flop has been chosen as the experimental test circuit because it can be used as a performance benchmark when comparing the capabilities of different IC technologies. The design methodology is described and experimental results are compared to the performance predicted by a circuit simulator. Based upon these results, the performance of the phase detector is projected using circuit simulation techniques.

Two possible methods of implementing a monolithic oscillator are investigated in Chapters 5 and 6. High frequency oscillator design techniques for discrete component circuits have been widely developed, where a broadband amplifier and a narrowband filter network are connected in a positive feedback configuration. An LC resonant circuit consisting of an inductor and capacitor connected in parallel is commonly used in the oscillator feedback

network. For a monolithic implementation, inductors that are compatible with a production integrated circuit process have been designed and fabricated, and these inductors could be used to realize such an LC resonant feedback network. Also, a wideband radio frequency (RF) gain element has been designed and fabricated which will provide a useful benchmark of the BiCMOS technology capability. The experimental results reported in Chapter 5 of this thesis could be applied to the design of a monolithic oscillator based on conventional design techniques.

An alternative approach to the monolithic integration of a voltage-controlled oscillator that is capable of operation at frequencies above 1 GHz is described in Chapter 6 of this thesis. Experimental measurements of a preliminary test circuit are reported in detail and compared to circuit simulations of the oscillator performance. A modification to the feedback network is introduced, which exploits the frequency selective characteristics of an active phase-shift network to potentially improve the spectral purity of the oscillator output signal.

Finally, some concluding remarks and recommendations for further research in this area are presented in Chapter 7.

2. Phase-Locked Loops

Timing recovery narrowband filters are often implemented using a phase-locked loop (PLL). The basic PLL does not require components which are difficult to integrate, such as high quality inductors or the special substrate materials required to fabricate high frequency surface acoustic wave (SAW) filters, so it is possible to completely integrate the timing recovery and regenerator circuitry onto the same IC. This is desirable not only for the traditional cost and reliability benefits of monolithic integration, but also because of the excessive cost of packaging high frequency components and the power consumed by package interconnections in a 50 Ohm environment. This chapter reviews the performance of both the analog and discrete-time PLL. Specifications which are important in the design of a timing recovery circuit for use in baseband data transmission systems are emphasized.

2.1 Analog Phase-Locked Loops

The theory of phase-locked loops has been the subject of numerous papers and several books [8]. The design parameters of the PLL usually refer to the linear model, which describes the steady-state in-lock behaviour of the system. Component imperfections introduce non-linearities that complicate the analysis of the closed-loop system. If only small perturbations about the in-lock condition are assumed, then the linear model can be used to provide valuable insight into the behaviour and predict the performance of the PLL. Design of the discrete-time PLL is often based upon an analogy to the linear, continuous-time model.

A block diagram representation of a continuous-time PLL is shown in Figure 2.1. A phase detector, loop filter, and voltage-controlled oscillator (VCO) are connected in a negative feedback configuration. The phase detector measures the phase difference between the input signal, $\Phi_i(s)$, and that of the VCO ($\Phi_o(s)$). In equilibrium (when the loop is phase-locked), the frequency of the VCO is exactly equal to the average frequency of the input signal. Transients or variations in the input frequency should be rejected by the timing

recovery PLL, because a frequency change cannot be introduced by most transmission media.

Figure 2.1 : Block diagram of a linear, continuous-time PLL.

The transfer function of the linearized loop can be written as [9]

$$H(s) = \frac{\Phi_o(s)}{\Phi_i(s)} = \frac{K_o K_d F(s)}{s + K_o K_d F(s)} \quad (2.1)$$

The loop gain ($K_o K_d F(s)$) completely defines the small-signal loop dynamics.

PLLs are often classified according to type and order. Type refers to the number of perfect integrators in the forward path (minimum of 1 because of the VCO). Additional integrators can be introduced by the loop filter. The order describes the number of poles in the closed-loop transfer function. In practice, PLLs are almost always higher than second order, because of parasitic poles in the loop filter amplifier and the pole at the modulation input of the VCO. The effects of parasitic poles must be examined carefully to ensure system stability.

The important performance specifications for timing recovery PLLs are: phase error, noise bandwidth, acquisition range, and acquisition time. It will be shown that the loop design parameters cannot be chosen to optimize all aspects of circuit performance, and so design trade-offs must be considered.

2.1.1 Steady-State Phase Error

The phase of the timing clock at the regenerator in a data transmission system is affected by any phase error between input and output. Steady-state phase error is a static offset between input and output phase, which should be minimized to achieve optimum sampling of the received data signal. The steady-state or static phase error (Φ_{cs}) due to a step frequency input ($\Delta\omega$) can be expressed as [9] :

$$\Phi_{cs} = \frac{V_c}{K_d} + \frac{\Delta\omega}{K_o K_d F(0)} \quad (2.2)$$

The error can only be considered quasi-static because it is influenced by factors such as temperature and component aging. The first component of the error described by equation 2.2 is due to offset voltages (V_c) in the phase detector and loop filter amplifier. Static errors due to offset voltages can be kept within acceptable limits through proper component selection and care in design.

The d.c. gain of the loop (defined as $K_o K_d F(0)$) determines the magnitude of the second component of the error in equation 2.2. If a VCO with a wide tuning range is used, the initial frequency offset ($\Delta\omega$) can be large, and a very high d.c. gain is required to achieve low steady-state error. Assuming a 1 GHz VCO with a linear tuning range of $\pm 5\%$ with respect to the centre frequency and a dynamic range of 5 Volts at the oscillator modulation input, gives the following maximum initial frequency offset:

$$\Delta\omega = 2\pi(0.1)(1 \times 10^9) = 2\pi \times 10^8 \text{ rads/s}$$

and

$$K_o = \frac{\Delta\omega}{\Delta v_m} = \frac{2\pi \times 10^8}{5} = 4\pi \times 10^7 \text{ rads/Volt}\cdot\text{s}$$

If an analog multiplier-type phase detector (such as a balanced modulator) is assumed, then the phase detector gain constant is typically

$$K_d = 0.3 \text{ Volts/rad} \quad (\text{typical analog phase detector})$$

and the component of the small-signal phase error due to finite loop gain at d.c. (from equation 2.2) is

$$\Phi_{es} \text{ (due to finite d.c. gain)} = \frac{2\pi \times 10^8}{1.2\pi \times 10^7 F(0)} = \frac{17}{F(0)} \text{ rads}$$

The d.c. gain of the loop filter must be greater than 950 to achieve a steady-state phase error of 1 degree. A large d.c. loop gain will be necessary in order to minimize the steady-state phase error in a timing recovery PLL. The first-order loop, where $F(s) = 1$, will be unsuitable for timing recovery applications because of the difficulty in achieving a low steady-state phase error. Higher order loops such as the second-order PLL allow the designer greater flexibility in the choice of loop components.

2.1.2 The Second-Order PLL

The second-order PLL has been an important element in modern communications systems for over 30 years. The theory of operation for the second-order loop is well documented in many papers and texts [9,10] and will not be repeated here.

A perfect integrator in the loop filter of a phase-locked loop will (theoretically) result in an infinite d.c. open-loop gain. An almost perfect integrator can be realized in practice using an active filter, which has the following transfer function

$$F(s) = - \frac{s\tau_2 + 1}{s\tau_1} \quad (2.3)$$

The extremely large d.c. gain of the second-order PLL ($K_0 K_d F(0)$) will minimize the static phase error and also helps to minimize the timing jitter present at the PLL output

The transfer function of the second-order loop with an active loop filter can be written in a form commonly used in servo control design as

$$H(s) = \frac{\Phi_o(s)}{\Phi_i(s)} = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (2.4)$$

There are two independent parameters available to the designer :

- ω_n : the undamped natural frequency, in rads/s
- ζ : the loop damping factor

The second-order PLL exhibits a lowpass filter response which is underdamped for $\zeta < 1$.

2.1.3 Dynamic Phase Error

Dynamic phase error or timing jitter is caused by noise at the PLL input and noise generated within the loop itself. Any noise generated within the loop which is outside the loop bandwidth cannot be reduced by negative feedback action. The timing jitter at the output of the PLL due to input noise has been derived by Roza [11] as

$$\phi_{ed} = \alpha \frac{(\phi_{es})}{Q_{eff}} + \beta \frac{1}{Q_{eff}} \quad (2.5)$$

where :

α is a constant which depends on the data sequence.

β is a constant which depends only on the input signal phase, t .

ϕ_{es} is the static phase error.

Q_{eff} is the effective quality factor of the PLL, analogous to a resonant circuit Q .

The constants in equation 2.5 depend upon systematic sources (i.e., the data pattern) and random noise which introduces fluctuations in the input phase to the PLL. The dynamic phase error at the PLL output can be made as small as desired by increasing Q_{eff} and reducing the static phase error. Choosing a second-order PLL can almost eliminate the static phase error (there will still be an error due to offsets, etc.) and thereby reduce the dynamic phase error.

The effective Q of the PLL is related to the loop noise bandwidth (B_L) and has been defined by Roza as [11]

$$Q_{\text{eff}} = \frac{\pi}{4TB_L} \quad (2.6)$$

where T is the clock period or bit interval of the transmitted data. The noise bandwidth for a normalized transfer function, $H(j\omega)$ or $H(j2\pi f)$, is by definition

$$B_L = \int_{-\infty}^{+\infty} |H(j2\pi f)|^2 df \quad (2.7)$$

It should be noted that as a result of normalization, $H(0)$ is unity. The noise bandwidth of the second-order loop with an active loop filter is given by [9]

$$B_L = \frac{\omega_n \left(\zeta + \frac{1}{4\zeta} \right)}{2} \quad (2.8)$$

which is determined by the design parameters of the loop, ζ and ω_n . The minimum noise bandwidth for a given undamped natural frequency, ω_n , requires an underdamped second-order loop with a damping factor of one-half. However, the underdamped PLL has a significant peak in the closed-loop frequency response which can cause exponential growth of timing jitter in repeater chains.

2.1.4 Jitter Accumulation in Repeated Data Transmission Systems

Data regeneration in digital transmission systems prevents the accumulation of noise and distortion through the transmission medium. However, the timing jitter of the recovered clock signal will tend to grow or accumulate when data is transmitted through a chain of regenerative repeaters. Jitter is caused by random components in the transmitted signal which are either truly random (e.g., white noise) or systematic (e.g., random components in the data pattern, which is usually a pseudo-random sequence of bits). The jitter caused by systematic sources is reproduced at each repeater in a transmission system and will

accumulate much faster than random jitter. Jitter accumulation limits the number of repeaters of a given design which can be cascaded in a transmission system.

The timing jitter accumulation is exacerbated by peaking in the closed-loop transfer function of the timing recovery circuit. Although the d.c. gain of the second-order closed-loop transfer function is always unity (refer to equation 2.4), the closed-loop gain can be greater than unity in some frequency range. This peaking in the PLL transfer function causes some components of the phase at the loop input to be amplified, which can result in exponential growth of timing jitter in the transmission system. Assuming that each repeater in the system is identical, it is possible to determine the total accumulated jitter and the maximum number of repeaters which can be cascaded for a given repeater design.

The effect of the second-order loop damping factor (ζ) on jitter accumulation is illustrated in Figure 2.2. The normalized relative jitter shown in this figure is defined as the root-mean-square (rms) relative timing jitter introduced by the M^{th} repeater in a chain, normalized to the jitter at the output of the first repeater (i.e., $M=1$). Figure 2.2 shows that if the minimum noise bandwidth is chosen for the second-order PLL ($\zeta = 0.5$) then exponential jitter accumulation will severely limit the number of repeaters in the system.

It can be shown that the second-order PLL with an active loop filter (the type 2 second-order loop) always exhibits peaking in the closed-loop transfer function regardless of the loop damping factor [5]. The closed-loop transfer function of the second-order PLL with only one perfect integrator (i.e., due to the VCO) does not show peaking if the magnitude of the closed-loop system zero is made greater than the magnitude of the closed-loop poles. However, a very low d.c. loop gain is required to achieve this, which increases both the static and dynamic phase errors. Fortunately, the peaking of the second-order PLL with an active loop filter and the resulting jitter accumulation can be controlled. From equation 2.4, the magnitude of the transfer function at ω_n is

$$|H(j\omega_n)| = \sqrt{1 + \frac{1}{4\zeta^2}} > 1 \quad (2.9)$$

Equation 2.9 indicates that peaking of the PLL transfer function and subsequent jitter accumulation can be controlled by choosing a large damping factor. Damping factors of 5 or more are often used in practice [11, 12].

Figure 2.2 : Jitter accumulation with high-gain PLLs [11].

2.1.5 PLL Stability and the Acquisition of Phase Lock

The second-order PLL is unconditionally stable. However, parasitic circuit elements within the loop cause the loop to be of a much higher order. Parasitic poles are introduced by the finite bandwidth of the filter amplifier, any pre-filtering used to reduce switching noise at the output of the phase detector and the modulation pole of the VCO. Although the loop can now be as high as fifth order, it can still be analyzed as a second-order loop if the parasitic poles lie at a much higher frequency than the transfer function zero. If the parasitic poles cannot be minimized, they will interfere with the low frequency poles and affect the loop damping and bandwidth. In such cases the PLL design should assume a higher order loop to ensure stability, control of transfer function peaking and low noise bandwidth.

The specifications which define the operating and stability limits of the PLL are shown in Figure 2.3. Hold range is defined as the input frequency range which a PLL can statically

phase track. The loop is conditionally stable in this range. Hold range of the second-order PLL with a perfect integrator in the loop filter is theoretically infinite, because of the infinite d.c. loop gain. In actual circuits, hold range is usually limited by the dynamic range of the loop filter output and the VCO modulation input. The dynamic limit for phase tracking is smaller than the hold range, and is defined as the pull-out range. Exceeding the pull-out range is unlikely in timing recovery if line jitter is kept to a tolerable level (less than 20 degrees rms).

Figure 2.3 : Operating limits of the PLL defined [10].

The PLL will capture the input signal and lock with a simple phase transient for input signals within the lock-in range, which is the normal operating frequency range for the loop as shown in Figure 2.3. The lock-in range is less than the hold range for all loops higher than first order. The pull-in range defines the input signal frequencies which the PLL can lock onto. However, the process can be slow and is unreliable when a significant amount of noise is present at the loop input. Acquisition of input signals within the lock-in range is a phase acquisition process while input signals outside this range require frequency acquisition (a non-linear process).

2.1.6 Selection of Loop Parameters for the Timing Recovery PLL

Consideration of the static and dynamic phase error performance requirements of a timing recovery PLL has shown that a second-order loop with high d.c. loop gain is preferred. Another advantage of the second-order PLL as a narrowband timing recovery filter is the ability to independently minimize both the static and dynamic phase errors using the two

loop design parameters, ζ and ω_n . In resonant filter circuits (e.g., LC tanks) the static phase error and the circuit Q are strongly coupled, and both cannot be optimized to minimize the timing jitter [3].

Higher order loops are not normally considered for many reasons. The closed-loop parameters of higher order loops are sensitive to gain variations and component tolerances, making consistent performance difficult to maintain. Timing recovery filtering requires minimization of phase errors due to a step change in frequency at the input, and higher order loops do not offer significant performance improvement for the additional circuit complexity.

Dynamic and steady-state phase error are specifications which directly affect the timing phase at the data regenerator. However, other performance aspects of the loop such as stability and acquisition capability must also be considered in the design of the PLL. For example, output timing jitter and the range of input frequencies which the PLL can acquire are both influenced by the choice of loop filter bandwidth. The performance trade-offs inherent in the selection of the loop parameters, ζ and ω_n , and the restrictions which must be placed on loop components in order to meet design specifications are subtle aspects of timing recovery design.

As previously outlined, the loop damping factor must be kept large to control jitter accumulation. Therefore the undamped natural frequency of the loop (ω_n) must be reduced to attenuate input noise. The undamped natural frequency required to meet the jitter performance specifications in a repeatered system is between 5 and 10 kHz [12]. This narrow bandwidth causes attenuation of high frequency components through the loop filter which could modulate the VCO, thereby reducing the timing jitter. However, harmonics or beats at the phase detector output modulate the VCO and pull it towards the input signal frequency. This beat tone will also be attenuated by the loop filter, reducing the range of frequencies which the PLL will acquire. Consequently, the initial frequency offset of the VCO output with respect to the bit-rate must be within the lock-in range so that the PLL can lock-on to the input signal under all conditions. Achieving a low initial frequency offset of the VCO can place unnecessary restrictions on the oscillator's free-running stability. Stable high frequency oscillators require highly selective resonant circuits (e.g., LC tanks) in the positive feedback path of the oscillator, which cannot be monolithically integrated.

The requirement for a large loop damping factor ($\zeta > 5$) and low undamped natural frequency ($\omega_n < 10$ kHz) results in two fundamental problems when attempting to monolithically integrate the second-order analog PLL for timing recovery applications :

1. Narrow loop bandwidth. This requires a loop filter with time constants that are difficult to implement using monolithic components.
2. Minimizing the free-running VCO frequency offset, $\Delta\omega$. This can be achieved by designing a very stable VCO with a narrow modulation bandwidth, but stable oscillators are also difficult to implement using monolithic components.

With only two design parameters available to the designer of a second-order loop (ζ and ω_n), there is little that can be done to optimize phase and frequency acquisition performance that does not compromise static or dynamic phase error.

2.2 Discrete-Time Phase-Locked Loops

The linear analog PLL has traditionally referred to circuits constructed entirely from analog functional blocks. The term digital PLL has often been used to refer to circuits in which analog functional blocks are used (such as the VCO and loop filter) but some signals are processed by digital components, such as a phase detector made from digital logic gates. A discrete-time PLL or DPLL consists of digital components, but it will also be defined as a circuit possessing the following properties :

1. Output phase is quantized. The transitions in the output waveform are synchronous with a system clock and therefore the output phase cannot vary continuously.
2. The phase error signal is binary encoded (i.e., a binary word), not an analog voltage.

The input to a discrete-time PLL can be an analog signal with a continuous time-varying phase. However, other signals processed within the system are quantized discrete-time signals. Therefore an analog-to-digital (A/D) conversion must be performed by the DPLL

phase detector. The discrete-time PLL is built exclusively from digital functional blocks. The input and output signals of a functional block (e.g., digital loop filter) can be a binary signal representing 2 states or an n -bit binary word representing 2^n states.

The DPLL shown in Figure 2.4 is a discrete-time equivalent of the continuous-time analog PLL. A sampling phase detector at the input detects the phase error between the input signal and the local phase estimate. Bandlimiting of the input signal is required to prevent aliasing introduced by the sampling process. A digital clock generator (DCO) corrects any error detected based upon a weighting function applied to the error samples by the discrete-time loop filter. Long filter time constants, which are difficult to realize in monolithic IC technology using analog filtering can be achieved here using digital filtering techniques. This is a significant advantage when attempting to implement a timing recovery PLL circuit. The DPLL can be implemented either in software or hardware. Software implementations cannot be seriously considered for a high frequency DPLL design because of the speed limitations of current microcomputer technology (on the order of tens of MHz). Therefore the following discussion will be limited to hardware DPLL implementations.

Figure 2.4 : DPLL block diagram.

2.2.1 Digitally-Controlled Oscillators

The digitally-controlled oscillator output is phase-quantized. The phase of the oscillator is controlled by an n -bit binary word, which is output by the digital loop filter. A hardware

DCO can be implemented using a programmable counting circuit, an increment/decrement counter, or a digital waveform synthesizer.

Figure 2.5 : Programmable-count DCO.

A programmable counting circuit implementation is illustrated in Figure 2.5. A stable, high frequency oscillator (f_s) is used to drive a counter circuit which is incremented each cycle of the high frequency clock. The state of the counter and the digital control input (the desired count modulus, N) are compared and when matched a reset pulse is generated. The reset pulse drives the sampling phase detector and resets the counter. The open-loop or free-running output frequency of the DCO is f_s/N . The oscillator output is phase modulated by incrementing or decrementing the terminal count (N). The PLL must therefore be designed for an input frequency equal to f_s/N . Phase quantization of the DCO output adds a source of timing jitter which is not present in an analog PLL. Incrementing or decrementing the terminal count (N) causes a quantized change in the oscillator phase. By making the terminal count large, the phase jumps caused by incrementing or decrementing N can be made as small as desired. However, this limits the output frequency of the DCO to a small fraction of the high frequency clock.

The digital loop filter can output an n -bit word to the DCO, or a binary signal to increment or decrement the DCO phase. The increment/decrement counter DCO shown in Figure 2.6 is controlled by two binary streams which can advance, retard, or maintain a constant output phase. The increment/decrement counter normally divides the fixed frequency clock input by two. Thus the DCO output is at a much higher fraction of the high frequency

clock than is possible with a programmable-count DCO. If an advance pulse is received from the loop filter, the counter adds a cycle to the output signal. A retard pulse causes the counter to remove a cycle from the DCO output. In this way, the output signal frequency can be controlled within a range determined by the frequency of the advance and retard pulses. The output phase is coarsely quantized, however, which results in significant timing jitter when the PLL is phase-locked. The increment/decrement DCO has been used in a commercially available DPLL (the SN74LS249 from Texas Instruments [10]).

Figure 2.6 : Increment/Decrement counter DCO.

The digital waveform synthesizer is a third type of digitally-controlled oscillator. Digital waveform synthesizers produce a sinusoidal signal by numerical computation or cycling through a ROM look-up table. State-of-the-art direct digital waveform synthesizers can operate at output frequencies up to 500 MHz [13]. A system clock frequency which is at least 4 times the output frequency (i.e., 2 GHz for a 500 MHz output) is required.

2.2.2 DPLL Implementations

To analyze the DPLL dynamics, it is assumed that the phase error is small enough so that the phase detector transfer function is approximately linear, which is similar to the approach used in the analysis of continuous-time PLLs. At d.c., the closed-loop gain is unity, similar to the continuous-time PLL. Unlike the continuous-time PLL, however, there is an upper limit on the open-loop gain imposed by stability requirements for first- and second-order DPLLs [5].

The static phase error of a DPLL will be zero only if the filter has a pole at $z = 1$, which is analogous to the requirement for a filter pole at $s = 0$ for the continuous-time PLL. Therefore the loop filter will have a large d.c. gain.

A wide bandwidth phase detector will be a key component of a timing recovery PLL for high-speed data channels. DPLL hardware implementations have been classified according to the type of phase detector as follows [14] :

- A. Flip-flop DPLL : A set-reset flip-flop is triggered by the zero-crossings in the input and DCO output waveforms. The phase error is derived by analog-to-digital conversion of the flip-flop output pulse duration.
- B. Nyquist-rate DPLL : The input signal is sampled at the Nyquist rate (at least twice the highest frequency component in the input signal).
- C. Zero-crossing DPLL : The loop attempts to sample at the zero-crossings in the input signal.
- D. Lead/lag DPLL : The phase detector determines if the VCO clock leads or lags each zero-crossing in the input signal.

The hardware required to implement each of these DPLL phase detectors and the bandwidth limitations of each design will be outlined.

A. Flip-flop phase detector

A flip-flop phase detector is shown in Figure 2.7. The set/reset flip-flop is triggered by zero-crossings of the signals at the S and R inputs. The output pulse duration at Q is proportional to the phase error between the input signal and the DCO output. The error signal from the output of the flip-flop is used to gate a counter which counts the pulses from a stable high frequency clock. This converts the analog pulse width corresponding to the phase error to a digital word. If the input signals to the phase detector are 50% duty cycle square waves, then an exclusive-OR gate can be used instead of an edge-triggered flip-flop to measure the phase error.

Figure 2.7 : Set/Reset flip-flop phase detector.

The input clock (f_0) is related to the high-rate clock by

$$\text{H.F. clock} = 2^M f_0 \quad (2.10)$$

The phase error estimate is accurate to within $\frac{\pm\pi}{2^M}$ which restricts the operating frequency when low jitter is required. Assuming ± 1 degree accuracy :

$$2^M = 180, \text{ therefore } M \geq 8 \quad (2.11)$$

and

$$\text{H.F. clock} = 180 \cdot f_0$$

Thus a 900 MHz clock would be required to process a 5 MHz input signal with ± 1 degree accuracy.

B. Nyquist-rate phase detector

A Nyquist rate sampling phase detector is shown in Figure 2.8. The bandlimited input signal is periodically sampled using a uniform sampling clock derived from a master timing source. The sampled input signal is then converted to an n -bit digital word by an A/D converter. The sampling clock rate must be greater than or equal to the Nyquist rate (at

least twice the highest frequency component in the input signal). In practice, the sampling clock rate is usually chosen to be many times higher than the Nyquist rate. The DCO generates an n-bit digital word at a rate which is also controlled by the master timing clock. Direct waveform synthesis from a ROM look-up table could be used to generate the DCO samples as shown in Figure 2.8. The two n-bit words are multiplied together by a hardware (or possibly software) multiplier to derive the phase error estimate.

Figure 2.8 : Nyquist rate phase detector.

The input signal is uniformly sampled by a clock which is synchronized with the DCO samples. Therefore the Nyquist rate phase detector is a discrete-time version of an analog multiplier phase detector. Circuit performance is limited by the resolution and speed of the A/D converter.

C. Zero-crossing phase detector

A zero-crossing phase detector is illustrated in Figure 2.9. The sampling switch is driven by short sampling pulses output by a zero crossing detector circuit. Thus the bandlimited input signal is sampled once every clock cycle of the DCO output. A sinusoidal input signal will be assumed which is sampled by a sampling switch at discrete instants in time ($t = \tau_k$, which are defined by the positive transitions in the DCO output)

$$\text{input signal} = A_i \cos[\omega_v(t) + \theta(t)] \quad (2.12)$$

Figure 2.9 : Zero-crossing phase detector.

The sampling pulses from the zero-crossing detector are assumed to be at the same average frequency as the input signal but in phase quadrature. The zero-crossings in the DCO output therefore satisfy the relation

$$\omega_v \tau_k + \phi(\tau_k) = k(2\pi) - \frac{\pi}{2} \quad (2.13)$$

where $\phi(\tau_k)$ is the DCO phase. The low frequency component of the sampled input signal (which is the phase error, $\epsilon(\tau_k)$) can be then be written as

$$\begin{aligned} \epsilon(\tau_k) &= A_i \cos[\theta(\tau_k) - k(2\pi) - \frac{\pi}{2} - \phi(\tau_k)] \\ &= A_i \sin[\theta(\tau_k) - \phi(\tau_k)] \end{aligned} \quad (2.14)$$

The phase error at the sampling switch output varies as a sine function of the input and DCO phase difference. This is also a discrete-time equivalent of a continuous-time multiplier, except that the sampling times are non-uniform because they are controlled by the DCO output. The effects of non-uniform sampling have been characterized by Weinberg and Liu [15], and it has been shown that if the input phase is varying slowly compared to the sampling rate, then uniform sampling can be assumed.

For small phase errors, filtering the sampled input signal gives an estimate of the phase error between the input and DCO output signals (i.e., $\sin(x)$ is approximately equal to x for small arguments). The input samples are then converted to an n -bit digital word by an A/D converter. The n -bit word at the A/D output is subsequently filtered by the digital loop filter to estimate the phase error between the input and DCO signals. The bandwidth of high-resolution A/D converters (at least 8 bits are required for ± 1 degree accuracy in the phase estimate, from equation 2.11) limits this technique to below 100 MHz with present state-of-the-art in converter technology.

D. Lead/lag phase detector

The lead/lag phase detector is a zero-crossing phase detector with a binary (i.e., one bit) phase error quantization. The phase detector output indicates that the phase of the DCO clock is either leading or lagging the input signal. However, filtering the harshly quantized error signal requires a special class of digital loop filters called sequential filters. For this reason, a DPLL which uses the lead/lag phase detector is considered separately from the zero-crossing DPLL.

Other DPLL implementations which are built using the flip-flop, Nyquist rate or zero-crossing phase detection methods are limited by current IC technology to input frequencies less than 100 MHz. These phase detectors are limited in operating speed because n -bit quantization of the phase error between the local timing clock and the input signal is required. Reducing the phase error quantization to a binary decision simplifies the phase detection circuit, allowing higher frequency operation. A DPLL which uses the lead/lag phase detector is suitable for high frequency applications because coarse quantization of the input phase error drastically increases the input frequency range. Therefore the binary quantized DPLL will be examined in greater detail.

2.2.3 Binary Quantized DPLL

Quantizing the input phase error to high precision decreases the input frequency range of a DPLL. By limiting the quantization of the phase error between the input signal and the locally generated timing clock (i.e., the DCO output) to a single bit, the operating bandwidth of the phase detector can be maximized. The binary quantized DPLL (see Figure 2.10) consists of a phase detector which quantizes the phase error to only one bit, a

digital filter which is suited to filtering the coarsely quantized error signal, and a variable frequency oscillator which can be phase-locked to the input signal.

Figure 2.10 : Lead/Lag DPLL.

The binary quantized DPLL was devised independently by Cessna and Holmes [16, 17] as a means of data synchronization for aerospace applications. The advantages of reliability and simplicity of the binary quantized DPLL over other analog or digital implementations was the prime motivation behind its development.

The loop designed by Cessna used a mid-phase/in-phase (MI) type phase detector which requires an analog integrate-and-dump circuit. While offering the advantage of matched filter detection of the received data, this circuit would be difficult to implement monolithically for use at high bit-rates.

The phase detection and filtering method reported by Holmes is illustrated in Figure 2.11(a). It consists of an A/D converter which samples the input waveform at each transition and a transition detector. A timing error between the sampling clock and the received signal is illustrated in Figure 2.11(b) as the time between the sample taken by the A/D converter and the input signal transition. The sampled value of the signal labelled with a (+) is interpreted as a positive control signal by the PLL while sampling after the transition (indicated by a minus sign) will result in a negative control signal. The correct polarity of the phase error samples is maintained by a transition sample selection circuit which flips the sign of the samples according to whether a positive or negative input transition is detected. A lowpass filter at the PLL input removes all the non-essential frequency components in the input signal and prevents aliasing.

a) block diagram of phase detector and filter

b) square wave input signal with negative timing error

Figure 2.11 : Transition sampling DPLL [17].

The digitally-controlled oscillator proposed by both Cessna and Holmes was an increment/decrement-type DCO followed by a clock divider circuit. The divider reduces the system clock rate down to the sampling clock rate. The DCO accumulates the phase error adjustments output by the loop filter (the increment and decrement pulses) in a manner analogous to the perfect integration of an analog VCO in a continuous-time PLL.

The first-order DPLL with a binary phase detector can be analyzed by modelling the phase error states of the loop as a discrete parameter Markov chain. Additive noise at the input to the loop causes uncertainty about whether lead or lag output pulses will be produced by the phase detector. If the statistics of the noise are assumed to be Gaussian, then the state probabilities of the Markov chain will be independent and the steady-state operation of the loop is similar to the random walk from statistical theory. Difference equations for the

system can be written in order to determine the steady-state phase error and average transient time of the DPLL.

The transient response of the binary quantized DPLL approximates the response of a first-order continuous-time PLL. For high signal-to-noise ratios the steady-state phase error reaches a minimum value which is limited by the phase quantization of the DCO. This phase quantization can be set as low as desired by increasing the clock divider length.

Figure 2.12 : Random-walk sequential filter.

A loop filter is not required for closed-loop operation but some filtering is desirable in order to reduce the jitter of the DPLL clock output. A fixed length accumulator was used by Holmes as a discrete-time integrate-and-dump loop filter. A more sophisticated loop filter structure was devised by Cessna which he called sequential filtering after the sequential threshold test in estimation theory. One of the possible sequential filter implementations described by Cessna is the random-walk filter shown in Figure 2.12. The filter consists of a $2N$ stage UP/DOWN counter and a reset-to- N circuit. The lead/lag outputs of the phase detector clock the counter either up or down. The content of the UP/DOWN counter is a weighted sum of the lead and lag pulses where lead pulses are assigned a weight of $+1$ and lag pulses are assigned a weight of -1 . The counter is a digital integrator of the phase error pulses from the phase detector. This is only an approximation of the filter behaviour, because the lead and lag pulses do not carry any information about the magnitude of the

phase error, they only indicate a leading or lagging phase relationship between the DCO clock and the input signals. A terminal count of $2N$ or 0 causes an output from the filter to advance or retard the phase of the DCO clock and reset the counter to count N . The digitally-controlled oscillator phase represents an accumulation of the advance and retard phase corrections output by the loop filter. Therefore there is an overall integration or weighted summation of the pulses produced by the phase detector and the loop behaves like a first-order continuous-time PLL.

Figure 2.13 : Second-order binary quantized DPLL.

Random noise introduces some uncertainty into the phase error measured by the binary quantizer. The random-walk filter has been designed so that the filter output makes phase corrections to the DCO which have a higher probability of being correct than if the phase detector outputs were used to control the DCO phase directly. This method of filtering is intuitively appealing, since the corrections of the clock phase are made less frequently when the uncertainty in the phase error measurement increases. More sophisticated sequential filter structures have been devised which improve the lock-in range and reduce the timing jitter of the binary quantized loop [18].

It is also possible to design a second-order DPLL using coarse quantization [19]. The second-order loop is preferred for timing recovery applications because static and dynamic phase errors can be minimized. A block diagram of a second-order structure is shown in Figure 2.13. One possible method of predicting the loop behaviour is to model the DPLL

by an equivalent analog PLL so that the analytical results from the analog loop can be applied. Analysis of the second-order loop based on the Markov chain model is difficult because multiple step sizes are possible for the phase error in the steady state.

2.3 Hybrid PLL

The hybrid phase-locked loop is usually an analog PLL where one or more of the loop components (but not all) are digital. Digital phase detectors are often used in PLL frequency synthesizers because the frequency acquisition capability of the hybrid PLL is superior to the performance of a purely analog PLL. Thus hybrid loops are often designed in order to improve some aspect of PLL performance.

The output frequency of the digitally-controlled oscillator (DCO) in a DPLL is usually a small fraction of the system clock frequency because a variable length frequency divider is often used to control the DCO output. Large divider ratios are necessary to achieve fine control of the local clock phase and reduce timing jitter due to phase quantization effects.

An analog VCO controlled by a digital-to-analog (D/A) converter can be used to implement a digitally-controlled analog oscillator with a much higher output frequency capability than can be achieved with the DCOs discussed in section 2.2.1. The quantization interval of the oscillator output frequency is determined by the resolution of the D/A converter which drives the modulation input of the oscillator, and the modulation sensitivity of the VCO. This hybrid approach has been used in some high frequency timing recovery PLL circuit implementations, which have otherwise consisted of mainly digital circuit components [20].

2.4 Summary

The performance parameters of the analog PLL when used as a narrowband filter in a timing recovery circuit have been reviewed. It has been shown that a high-gain second-order PLL with a narrow loop bandwidth is required to minimize static phase error and timing jitter. This places restrictions on the design of PLL components such as the loop filter time constants and the spectral purity of the voltage-controlled oscillator, and makes complete monolithic integration difficult.

Discrete-time implementations of the PLL (DPLLs) have also been discussed. Long filter time constants, which are difficult to achieve on-chip with continuous-time filter circuits, can be implemented using discrete-time or digital filtering. This is the primary motivation for considering the discrete-time PLL in timing recovery applications. For a high frequency phase-locked loop design, the lead/lag DPLL has been identified as a potentially useful circuit. Low resolution quantization of phase error in the loop increases operational bandwidth of the DPLL phase detector. However, the operating frequency range of a DPLL is also restricted by conventional DCO designs. Hybrid loops using a combination of analog and digital components can be designed in order to improve the performance of a purely analog or purely digital PLL.

The next chapter will discuss the architectures which could be considered for a monolithic timing recovery PLL circuit. A viable architecture for monolithic circuit implementation is examined.

3. PLL Timing Recovery Architectures

High frequency phase-locked loop circuits are usually fabricated using numerous discrete components, and even the most highly-integrated commercially available PLL circuits require some external components with the present state-of-the-art. High frequency applications, such as closed-circuit video transmission using fibre-optic data links or hand-held wireless telecommunications terminals, will require synchronization circuits capable of operation at frequencies up to and exceeding 1 GHz. These circuits must be inexpensive and suitable for high volume manufacturing, because both products are intended for the consumer market. Operation from limited power sources will require a circuit with low power consumption, and size and packaging restrictions will require that the circuit use a minimum number of external components. A monolithic PLL timing recovery circuit can meet these design objectives. However, complete integration of the PLL onto a single integrated circuit is a difficult technical challenge. The requirement for high frequency operation further complicates the design problem because of the performance limits imposed by currently available monolithic circuit technology.

Architectures which can be used to develop high frequency timing recovery PLLs will be discussed in this chapter. The important issues in the design of a high frequency monolithic circuit will be reviewed. A classical high frequency analog timing recovery PLL circuit will be outlined to illustrate the technical difficulties in monolithic implementation of a completely analog version. A novel PLL architecture which has been used to overcome some of the key limitations of the classical approach is then discussed. A PLL architecture which is capable of high frequency operation and monolithic integration is then presented, and this provides the system context for the circuit designs discussed in subsequent chapters of this thesis. This architecture is proposed as the basis for a fully-monolithic timing recovery PLL which could be used in repeated or point-to-point data transmission applications.

3.1 Barriers to Monolithic Integration

The constraints on the design of a phase-locked loop imposed by the timing recovery application have been broadly discussed in Chapter 2. These design issues will be summarized to highlight some of the difficulties encountered in attempting monolithic integration.

The steady-state phase error of the PLL must be minimized in order to ensure proper phase alignment between the received data and filtered clock at the data regenerator of a data transmission system. A low steady-state error will also reduce the dynamic phase error or timing jitter present on the filtered clock output of the PLL as discussed previously in section 2.1.3. The steady-state and dynamic phase errors can both be minimized by choosing a high-gain PLL of at least second-order. However, the loop damping factor must be large enough to limit the jitter accumulation (normally, $\zeta > 5$) in a repeated transmission system.

Timing recovery for telecommunications applications requires a narrow bandwidth PLL so that frequency components other than the desired timing clock frequency are rejected. The jitter on the clock signal at the output of the PLL is directly proportional to the loop bandwidth and the undamped natural frequency of the loop. Typically an undamped natural frequency (ω_n) less than 10 kHz is required. A narrow loop bandwidth will limit output timing jitter but also reduces the range of frequencies at the input of the loop which the PLL can lock-onto or acquire. The limited frequency acquisition capability of the narrowband PLL restricts the allowable free-running frequency offset between the oscillator output and the unfiltered clock signal at the loop input. This condition forces a design restriction on the spectral purity of the VCO, since there is a relationship between tuning range and spectral purity of the oscillator output.

Monolithic oscillator circuits are in general less stable than hybrid or discrete component implementations. Oscillator circuits can be placed into two general classes: tuned circuit oscillators and RC oscillators. The frequency selective feedback network of a tuned circuit oscillator can be implemented using an LC tank circuit, surface acoustic wave (SAW) or crystal resonator. SAW and crystal resonators require special substrates which are incompatible with most silicon processing technologies, and narrow bandwidth LC tanks

are difficult to fabricate for operation at frequencies above a few hundred MHz with the required quality and reproducibility. The tolerances on monolithic components due to process variation makes reproducibility difficult and requires some frequency adjustment capability.

RC oscillators are normally relaxation or ring oscillators which are broadband switching circuits. There is no energy storage element such as an inductor in these circuits to promote a stable, single mode of oscillation, and consequently the free-running stability of these circuits is poor. Therefore the PLL architecture must in some way accommodate the wide tuning range of a low-stability monolithic oscillator.

Monolithic implementation of a continuous-time lowpass filter with the time constants required to meet the loop damping factor and undamped natural frequency specifications is not practical. The components available to the filter designer in a monolithic technology are limited in size (e.g., capacitance values typically less than 30 pF) and have a tolerance of between 10% and 20% of the nominal value. A digital loop filter can meet the time constant requirements and constraints on reproducibility, but the phase detector and oscillator must be compatible with digital technology.

3.2 Deductive Timing Recovery

A classical deductive timing recovery circuit often used at frequencies above 100 MHz is illustrated in Figure 3.1. This type of circuit is commonly used in fiber-optic receivers [4] and operation in the GHz range is possible. Deductive timing recovery circuits generate a timing tone through non-linear processing of the received data signal. The filtered timing tone is used as a timing clock to synchronize the received data stream.

Often the bandwidth of a fibre transmission channel is wide enough that the rise and fall times of the received pulses are less than one-half of the bit period [21]. Therefore the transitions in the received signal are fast enough to drive a simple transition detector, consisting of an exclusive-OR (XOR) gate and a broadband delay line. The transition detector recovers the timing tone from the received data by generating a pulse for every transition in the received data, as illustrated in Figure 3.2. Setting the delay time equal to one-half of the bit period (i.e., $t_d = T/2$) increases the fundamental component in the output, and maximizes the signal-to-noise ratio of the recovered clock tone.

Figure 3.1 : PLL deductive timing recovery.

The exclusive-OR gate output can be partitioned into a deterministic component and a data dependent component. A narrowband filter tuned to the bit-rate will filter out the timing clock, which is then used to clock the data regenerator flip-flop. The amplitude of the timing tone at the transition detector output depends upon the frequency of transitions in the received data, and consequently data scrambling or line coding is required to ensure a sufficient number of data transitions.

A low quality ($Q=10$) bandpass filter tuned to the timing clock frequency follows the tone recovery circuit. The bandpass filter rejects noise and increases the signal-to-noise ratio of the recovered timing clock. Filtering the noise on the recovered clock also reduces the amplitude variations of the input signal to the phase-locked loop. Amplitude modulation of the signal at the input to an analog phase detector will affect both the phase detector gain and the PLL parameters (loop damping ratio and undamped natural frequency). The circuit components required to implement a passive bandpass filter are difficult to monolithically integrate, and active filter technology cannot achieve the high frequencies required for this application (centre frequency of about 1 GHz).

Figure 3.2 : Transition detected data.

The PLL is a high-gain second-order circuit using an analog multiplier phase detector. The low signal-to-noise ratio at the transition detector output precludes the use of a digital phase detector. The loop filter time constants must be large enough to achieve the high loop damping and low noise bandwidth required by repeated data transmission applications. Therefore the lock-in range of the loop is small and a high stability VCO is necessary to minimize the free-running offset at the PLL output.

Alignment of the filtered clock and the received data requires a second delay line between the VCO output and the flip-flop to adjust the static timing phase.

Some component reduction is possible through monolithic integration, but many of the key elements cannot be implemented in IC form. Significant problems are caused by delay variation with temperature and aging, and the duration of the time delay required. Any parameter variations in the time delays results in unwanted timing jitter. Therefore active circuit delay lines which are sensitive to noise, supply voltage, and temperature are unsuitable. The transition detector requires a broadband, low-loss delay line while the delay line between the VCO and the data regenerator could be narrowband. A passive, low-loss time delay is usually realized using transmission lines (i.e., a distributed parameter delay line) or with lumped-element LC delays. Passive delay circuits are impossible to integrate on a silicon chip with the required attenuation characteristics and delay time.

Typically, the loop filter time constants are of the order of milliseconds, which cannot be integrated using a continuous-time active filter or with a charge pump loop filter [22]. Also, the VCO tuning range must be very narrow to allow unaided acquisition of the input signal, and this forces strict requirements on the phase stability (or spectral purity) of the oscillator. The frequency stabilizing components which are required to implement an oscillator of the required spectral purity (e.g., a high quality inductor) are not available to the designer of monolithic circuits in silicon technology.

Some of the difficulties encountered in attempting to integrate a deductive PLL timing recovery circuit can be solved by using an inductive timing recovery loop.

3.3 Inductive Timing Recovery

An inductive timing recovery circuit must be implemented using a PLL. The received data signal is sampled using a locally generated timing clock. From these samples, the phase relationship between transitions in the received data and the locally generated timing clock is determined. Any error detected is fed-back to alter the phase of the local clock and reduce the error to zero.

Phase alignment of the timing waveform and the received data at the data regenerator can be controlled by the feedback action of the PLL if an inductive timing recovery circuit is used. This eliminates the need for a delay line between the PLL output and the data regenerator. Another circuit simplification of the inductive timing recovery is the elimination of the tone recovery circuit.

An example of a high frequency inductive timing recovery circuit is shown in Figure 3.3 [23]. The incoming data signal provides a reference (R) and transitions in the local clock (VCO) will be phase-locked to the data signal transitions. Normally, the VCO is connected directly to the variable phase (V) input of the phase/frequency detector (PFD) in PLL applications such as frequency synthesis. However, the data signal at the reference phase (R) input is not a square wave. The phase/frequency detector will interpret multiple ones or zeros (transitionless data strings) as the VCO phase leading the reference (R) signal phase because of the missing data transitions. Therefore a clocked data scheme is used to overcome this problem as shown in Figure 3.3.

Figure 3.3 : PLL inductive timing recovery circuit.

The edge-triggered D-type flip-flop is clocked by the output of a high frequency analog VCO. The flip-flop acts as a phase shifter and regenerator for the received data. The phase of the flip-flop Q output follows the phase of the clocking signal, provided that the set up and hold time limits of the device are not violated. Transitions in the received data are phase-shifted by a one-half bit delay (t_d) and compared with the resynchronized data at the flip-flop output using the phase/frequency detector.

A differential integrator is used to filter the pulses produced by the phase/frequency detector. This is usually implemented using a charge pump circuit [24] or a continuous-time active filter [10]. The filtered phase error modulates the analog VCO in order to phase lock the clock transitions to the received data transitions.

The relative phase of the V input with respect to the R input is sensed by the phase/frequency detector, which is an edge-triggered digital logic circuit. The PFD produces pulses at the U output when the reference signal at the R input leads the signal at the variable phase or V input, and pulses at the D output when transitions at the V input lead the signal transitions at the R input. The width of the output pulses are equal to the time duration by which R leads or lags V. Because only the input signal transitions are used to measure the phase error, the duty cycle of the input signal does not affect the output

waveforms. Only one output can be active at a time, although in practical circuit realizations short pulses appear at both outputs for zero phase error at the inputs. The output signals of the PFD are digital pulses (i.e., quantized in amplitude). However, the duty cycle of the output pulses is proportional to the phase difference at the inputs, which is a continuous-time or analog measure of the phase error. The PFD output pulses depend upon the sequence of transitions at the input, and so false triggering which can be caused by low signal-to-noise ratio input signals must be avoided. This can be achieved by hard-limiting the received data pulses to ensure adequate signal amplitude and well defined signal transitions.

The phase error, which is the difference in duty cycle between the U and D output pulses of the PFD is fed-back to the VCO through an appropriate loop filter. The error signal shifts the VCO phase in order to correct any phase offset at the PFD inputs. When the loop is phase-locked, the positive transitions in the received data at input R are synchronized with the positive transitions in the local timing clock (VCO). Choosing the delay time $t_d = T/2$ ensures that the data regenerator is clocked at the centre of each data bit in order to optimally sample the received data. The phase alignment between the clock and data signals will be maintained despite perturbations in temperature, power supply variations, and component aging.

The phase/frequency detector is often used in frequency synthesizer PLLs because the transfer function of the device is aperiodic. Any difference in frequency between transitions at the R and V inputs results in a constant error signal which sweeps the VCO toward the phase-locked condition. This results in a very wide pull-in range for the PLL. As a result, a lower quality VCO can be used because a large initial offset between the free-running VCO frequency and the input signal (previously defined as $\Delta\omega$) can be tolerated.

Unfortunately the transfer characteristic of the PFD relating VCO phase to the received data phase is not the same as the transfer characteristic of the PFD for square wave input signals. This is because the data regenerating flip-flop cannot continuously phase-shift the received data but can only phase-shift within a range defined by the period of the clock. Analysis of frequency acquisition is therefore complicated by the transfer function of the phase/frequency detector when used in this circuit configuration. Other factors which complicate the analysis are the non-linear large signal behaviour of the PLL and the fact that the phase error is only measured at transitions in the received data. This makes acquisition

time dependent on the statistics of the input data. Acquisition time is also influenced by the loop filter bandwidth, loop gain, and the choice of time delay, t_d [23].

A phase comparison between the R and V input signals of the PFD cannot be made unless a transition in the received data occurs, and therefore the phase detector gain (K_d) is a function of the transition density in the received data. The effective phase detector gain (K'_d) becomes :

$$K'_d = \frac{K_d}{2} \cdot P \quad (3.1)$$

where P is the probability of a data transition. The effective phase detector gain is a maximum of one-half the normal phase detector gain for deterministic signal inputs (K_d), because the maximum number of data transitions is one-half the number of VCO clock transitions (e.g., an alternating 1's and 0's NRZ-coded data signal at 500 Mbits/s is a 250 MHz square wave). The probability of a data transition depends upon the statistics of the transmitted data. The timing information in the received data is derived from the detection of transitions in the data, and data coding or scrambling is required to ensure adequate timing information. There is a similar requirement in deductive timing recovery for sufficient transitions in the received data to generate a timing tone.

Equation 3.1 predicts a reduction in loop gain for data patterns with few transitions, which will cause a change in the loop parameters. The effect of decreasing the data transition probability (P) on the PLL is analogous to the effect of increasing the divide ratio (N) in a frequency synthesizer PLL. The undamped natural frequency and the damping factor will decrease as P decreases, which reduces the noise bandwidth of the PLL or results in a higher Q_{eff} . This allows the PLL to quickly reacquire phase-lock of the input signal when the transition density increases again.

Circuit components such as the delay line and the continuous-time active loop filter (long time constants are required for large Q_{eff}) cannot be monolithically integrated. The acquisition performance of the loop is improved, but it is not clear what magnitude of initial VCO frequency offset can be tolerated. Also, parameter dependence of the PLL on data pattern will require knowledge of the input signal statistics in order to properly design the

timing recovery. Some of these difficulties can be overcome if discrete time components are used in the inductive timing recovery design.

3.4 Monolithic PLL Timing Recovery

The inductive timing recovery method eliminates the tone recovery circuit required to explicitly generate a timing tone, and provides for feedback control of clock and data phase alignment at the data regenerator. These features are important in the design of a timing recovery circuit suitable for monolithic integration. However, passive filter components and a broadband phase delay element must remain external to a monolithic implementation of the circuit shown in Figure 3.3.

A hybrid PLL circuit consisting of both analog and digital components and using one-bit quantization of the phase error could be designed to overcome these limitations. The development of monolithic timing recovery circuits for high-speed point-to-point communications in computer data networks has demonstrated the feasibility of this architecture [25]. A single-chip timing recovery circuit has been implemented in a GaAs technology which was designed to synchronize a 1250 Mbit/s data stream [20]. The transmitted data was scrambled using a 2^7-1 pseudo-random binary sequence. Scrambling of the data is a widely used method of limiting the length of transitionless data strings. Timing jitter measured on the recovered clock was less than 25 ps rms (11 degrees rms) and the lock-in range of the PLL was $\pm 10\%$ of the nominal bit-rate (i.e., ± 125 MHz). Although no circuit details have been published, it was reported that a second-order binary quantized DPLL with an analog VCO was used to achieve these results. A similar approach is proposed as the basis for a fully-monolithic timing recovery which could be used in repeated data transmission systems.

A block diagram of the proposed monolithic timing recovery PLL structure is shown in Figure 3.4. Coarse quantization (1 bit) of phase error simplifies the phase detector function and extends the operational bandwidth of the PLL. The binary quantizing phase detector estimates the phase error by determining whether the transitions in the local timing clock lead or lag the transitions in the received data. A sequential digital loop filter is connected to the phase detector output. Corrections to the local timing phase are accumulated by an UP/DOWN counter, and the digital phase estimate is converted to an analog signal which modulates a high frequency analog VCO. A second-order loop (note feed-forward path

Gf) is chosen so that static and dynamic phase errors at the regenerating flip-flop can both be minimized. Positive transitions in the received data and the local timing clock are aligned when the PLL is in-lock and therefore clocking the data regenerator with the negative clock transitions optimally samples the received data.

Figure 3.4 : Proposed monolithic PLL timing recovery structure.

A digital-to-analog converter is used to interface the filter output to a high frequency analog VCO. A conventional digitally-controlled oscillator design cannot be used because division of the system clock cannot be tolerated. The PLL is no longer a purely digital loop but a hybrid analog/digital PLL. The loop dynamics are not seriously affected if the D/A converter speed is sufficiently high (on the order of 10 MHz).

A large acquisition range will be required if the PLL is to lock onto the desired input signal, because the free-running frequency range of a monolithic oscillator is large. However, a narrow loop bandwidth is necessary to reduce jitter on the timing clock. Switching of the loop filter parameters could be used to vary the loop bandwidth. This can be easily implemented by changing the counter length (N) of the sequential digital filter. A user programmable counter length could be used to tailor the loop performance to a particular application. Also, a simple digital trimming technique could be used to set the centre

frequency and dynamic range of the analog VCO because it is modulated by the output of a D/A converter.

Telecommunications transmission systems generally require that the timing jitter should be less than 10 ps or 3.5 degrees rms at a 1 GHz data rate. This level of performance has not yet been demonstrated by monolithic timing recovery circuits but performance improvements are possible. The circuit designed by researchers at IBM [20] was implemented in a GaAs MESFET technology which is limited to data rates of less than 2 Gbits/s. This technology was developed for digital circuit applications and the device noise (e.g., $1/f$ noise, which has a significant impact on the frequency stability of an analog VCO) and voltage offsets are much higher than for bipolar-junction transistors fabricated in silicon technology. Therefore it is expected that a significant improvement in the performance of the analog and mixed analog/digital circuits such as the phase detector, D/A or A/D converter, and analog VCO should be achievable in silicon. Recent developments in silicon technology have demonstrated digital circuit performance which is comparable to or exceeds the clock rates possible in commercially available GaAs IC technologies [26]. The availability of low-power, high density CMOS logic in a BiCMOS process can be used to advantage in the design of the digital filter and D/A converter interface to the analog VCO. Bipolar devices will be required to implement the high frequency circuits such as the phase detector and analog VCO.

The ultimate performance which can be obtained in a repeatered transmission system depends on the quality of the monolithic components. Digital filters can be implemented using easily integrated circuit elements (digital logic gates). Such filters have excellent reproducibility and stability with parameter variations, and are capable of achieving long on-chip time constants without external components. The critical loop components are the VCO and the phase detector, because they operate at the system clock frequency where the bandwidth of the active devices will limit performance. Also, these components are influenced by analog variables such as phase noise, crosstalk, power supply fluctuations, and circuit parasitics. The sequential digital filter circuit is insensitive to many of these factors because it functions as an arithmetic processor of a well-defined digital bit stream. The design of a monolithic VCO and a binary quantized phase detector will be the subject of the remainder of this study.

3.5 Summary

The difficulties involved in the monolithic integration of a timing recovery circuit operating at GHz clock rates are probably insurmountable with present analog PLL technology. An inductive timing recovery architecture is a viable approach to monolithic integration, but the long time constants required by a continuous-time loop filter cannot be realized without external components. The second-order binary quantized PLL structure has been selected over the other design alternatives. This is because it has been recently demonstrated that a high frequency PLL can be integrated with no external components using this design. An inductive timing recovery circuit based on the binary quantized PLL has been proposed for further study with the underlying assumption that the performance reported in the literature can be duplicated if not exceeded in silicon technology.

Analysis of the static and dynamic performance of the hybrid PLL as a means of justifying this selection is beyond the scope of this thesis. This analysis would be required if the entire PLL were to be implemented. The intention of the further work in this study is to explore the feasibility of monolithic implementation by demonstrating that it is possible to realize the analog VCO and binary quantizing phase detector in a silicon BiCMOS technology.

4. Phase Detector

A phase detector circuit which could be monolithically integrated as part of a single-chip PLL timing recovery circuit is discussed in this chapter. Binary quantization of the phase error between the received data stream and a locally generated timing clock greatly simplifies the number of components required in the design.

The phase detector design proposed in this chapter consists of interconnected emitter-coupled logic (ECL) latching comparator circuits. A method of optimizing the switching speed of the ECL inverter has been used in the development of the ECL latching comparator circuit and this optimization procedure is discussed in detail. In order to evaluate the performance capability of the latching comparator fabricated in BiCMOS technology, a D-type master/slave flip-flop has been designed and fabricated. A flip-flop was chosen as the test circuit because it is a functional block in the phase detector design and also because the performance of the flip-flop can be easily compared with the performance of similar circuits fabricated in other technologies. Experimental measurements of the flip-flop test chip have been used to verify the circuit behaviour predicted by circuit simulations. The good agreement obtained between the simulated and experimental results for the flip-flop circuit indicates that simulation methods can be used to reliably predict the high frequency operating characteristics of the phase detector.

4.1 The Transition-Sampling Phase Detector

The transition-sampling method proposed by Holmes [17] and discussed in Chapter 2 of this thesis is a simple method of detecting the phase relationship between the locally generated timing clock and the received data stream, which can be implemented using digital logic circuits. Since the number of transitions in the two input signals to the phase detector are not equal (see the clock and data signals shown in Figure 4.2, for example), the circuit cannot directly measure the data/clock phase relationship if it is triggered by transitions in the local timing clock. However, a data synchronizer or flip-flop can be used to align the transitions in the received data stream to the local timing clock, similar to the

method used by the inductive timing recovery circuit discussed in section 3.2. The phase shift of the resynchronized data will depend upon the phase of the timing clock that is used to drive the flip-flop. Observation of the phase relationship between the data synchronized by both the positive and the negative transitions in the timing clock can be used to derive the lead/lag phase estimate. In this way, a binary quantized estimate of the phase error between transitions in the received data and local clock can be obtained.

Figure 4.1 : Flip-flop synchronizers driven by anti-phase clocks.

Consider the two flip-flop regenerators F1 and F2 shown in Figure 4.1, which are edge-triggered by opposite phases of the local timing clock. It will be assumed in the following discussion that the flip-flop behaviour is ideal; the state of the signal at the D-input is both sampled and transferred to the Q output at the moment when there is a positive going transition in the signal applied to the clock input of the flip-flop. The flip-flops are assumed to be triggered by the positive going clock transition for the purposes of this discussion, because the circuits which will be considered later for the phase detector implementation operate in this manner. It is also assumed for the purposes of the following discussion that the local timing clock is frequency-locked to the received data stream (i.e., the data rate and the timing clock frequency are identical). Consideration of the lock-in process is beyond the scope of this study, however, a discussion of the lock-in behaviour of the binary quantizing PLL is given in Yamamoto et al [18].

1. In-phase clock lags received data.

2. In-phase clock leads received data.

Figure 4.2 : Synchronizer waveforms.

Given the previous assumptions, the following two examples illustrate that observation of the phase relationship between the two synchronizer outputs (Q_1 and Q_2) can be used to determine the phase relationship between the local clock and the received data in a binary sense:

- Case 1 : If the positive zero-crossings of the in-phase clock lag the positive zero-crossings in the received data, then the synchronized data from flip-flop F1 will lead the output of flip-flop F2 as shown at the top of Figure 4.2.
- Case 2 : If the positive zero-crossings in the inverted clock lag the positive zero-crossings in the received data, then the output of flip-flop F2 will lead the data regenerated by flip-flop F1 as shown at the bottom of Figure 4.2.

These phase relationships can be observed by an appropriately designed logic circuit to produce an output pulse indicating a clock-lagging or a clock-leading phase condition.

In practice, the input waveforms to the phase detector will have finite rise and fall-times and the flip-flop synchronizer circuits will have finite bandwidth. Aside from circuit noise sources, these non-idealities will determine the minimum timing error that can be clearly identified as a phase-lead or phase-lag error state, and this causes timing jitter. Therefore a synchronizing circuit with the widest possible operating bandwidth is required to minimize this jitter.

Another important consideration is the response of the synchronizer when driven into a metastable state. Metastability of flip-flop synchronizers driven by asynchronous data and clock input signals is a well known phenomenon [27, 28]. When synchronized, the probability of a lead or lag output from the binary quantizing phase detector will be 50% (i.e., lead or lag output pulses are equally likely), and the zero-crossings in the local clock will be phase-aligned with the zero-crossings in the received data. Under these conditions the synchronizing circuit can enter a metastable state, and therefore the type of metastable response and the probability of entering the metastable state should be considered.

There are two types of metastability which can occur in synchronizing circuits: analog and oscillatory. Analog metastability causes the output of the circuit to remain at or near the input threshold voltage. Oscillatory metastability causes the outputs to toggle repeatedly between two logic states. An oscillatory response in the metastable state at the output of the synchronizing flip-flop would disrupt the operation of a phase-locked loop. If the output of the circuit remains at the logic threshold level (i.e., analog metastability), the operation of digital circuitry driven by the flip-flop output could also be disrupted. Therefore the response to a metastable event must be non-oscillatory and the logic state at the end of a measurement interval must be well defined in order to properly drive other circuits.

4.2 Binary Quantizing Phase Detector Design

Binary quantization of the phase error between a data stream and the local timing clock can be implemented using two edge-triggered flip-flops as described in the previous section. The flip-flops are driven by opposite phases of the timing clock, and each flip-flop samples the input data stream when triggered by the appropriate clock phase. A simple non-return-to-zero bit stream could be used to drive the phase detector with this scheme since preconditioning of the data is not required. However, it should be noted that coding of the data stream may be necessary to guarantee that there are a sufficient number of transitions in the received data. The ECL master/slave flip-flop (which will be discussed in greater detail in section 4.3) behaves like an edge-triggered device and could be used as a data sampler at bit-rates above 1 Gbit/s. The flip-flop, when combined with some additional circuitry, can be used to implement a complete phase detector design. The circuit design and performance predicted by computer simulation will be the subject of the following discussion.

4.2.1 Phase Detector Functional Description

The inputs to the phase detector circuit are the received data stream and the local timing clock. Two output signals are required which will indicate whether the input clock is leading or lagging the transitions in the received data. The input data is sampled by two master/slave flip-flops driven by anti-phase clocks. This transition sampling process has been described in section 4.1. After the input data has been sampled, the phase offset between the bit streams at the flip-flop outputs must be determined in order to derive the lead and lag output signals.

One method of implementing the transition-sampling phase detector is illustrated in Figure 4.3. A master/slave flip-flop can be implemented as a cascade of latch circuits driven by anti-phase clocks. The ECL latching comparator will be preferred for this application because very high clock rates can be achieved using this circuit topology. Circuit details of the latching comparator will be discussed in subsequent sections of this chapter. The flip-flop is shown as an interconnection of two latching comparators (labeled LC in Figure 4.3) called master and slave. Two additional latching comparators are required, which can be asynchronously disabled via the inputs H and HB (labelled LC+H in Figure 4.3). These circuits can also be reset when in the latched mode, by applying a signal to the RST input. The asynchronous reset function is required to ensure that the LEAD and LAG outputs can never be set to a logical high level at the same time.

Figure 4.3 : Binary Quantizing Phase Detector.

The received data stream is connected to the differential data inputs Data and Datab, and the local timing clock is connected to the differential signal inputs Clk and Clkb. Binary

signals indicating a phase-leading or phase-lagging relationship between the input clock and data are produced at the LEAD and LAG outputs respectively.

The operation of the circuit will be described assuming all latches are in the reset state (e.g., this would be the case if two or more zero bits have been received) and the phase relationship of the applied data and clock waveforms is similar to the diagram illustrating Case 1 in Figure 4.2. Thus a positive transition (i.e., a transition from zero to one state) of the clock signal occurs which lags the positive transition of the input data signal by less than 180 degrees, and the outputs of master/slave flip-flop F1 will be set one-half clock cycle before the outputs of flip-flop F2. Therefore the lag output of the phase detector (lag latch) will be set one-half cycle before the latch connected to the lead output (lead latch) is clocked, because the lead and lag output latches simply shift the retimed data streams by one-half of a clock cycle. When the lag output is set it triggers the hold and reset inputs of the lead latch and this prevents the lead output from being set until the lag latch is cleared. Both lead and lag latches are reset and the cycle is completed by the reception of a zero data bit. Similarly, if the phase relationship between data and clock is such that the signal appears at the output of F2, before the signal appears at the output of F1, a phase lead condition exists. This phase relationship corresponds to the waveforms shown at the bottom of Figure 4.2 (i.e., Case 2). The lead output of the circuit will be set and it will remain in the set state until cleared by the reception of a zero data bit. The lag latch will be disabled during the time that the lead output remains high.

It should be noted that the phase detector circuit shown in Figure 4.3 will only detect the phase relationship between the positive transitions in the received data and the timing clock, or the phase relationship at every second transition in the received data stream. A complementary set of output latches could be added to determine the data/clock phase relationship at the negative transitions of the received data. This additional circuit complexity (i.e., two more latches are required) has not been shown in Figure 4.3, and it will not be considered further in order to simplify the discussion. However, this functional improvement would be desirable in an actual circuit realization in order to maximize the phase detector gain.

4.2.2 The ECL Latching Comparator

The ECL latching comparator circuit can be used to develop a high-speed, high-precision data sampler and quantizer, and it is therefore ideally suited to the digital phase detector application. A schematic diagram of the latching comparator circuit is shown in Figure 4.4. The switching transistors in this circuit never enter the saturation region, and therefore switching delay caused by stored base charge is minimized. The use of differential signals in both the data and clock paths leads to a fully symmetric topology. For a given signal-to-noise ratio, smaller voltage swings across the circuit load resistors (R_1 and R_2 in Figure 4.4) can be achieved by using differential rather than single-ended input and output signals. Flow of the bias current in the circuit can be directed through a number of possible paths by cascoding differential transistor pairs. This current steering is an efficient method of increasing the functional capability of ECL circuits without severely degrading the switching speed or increasing the overall power dissipation. The effect of parasitic capacitance at critical nodes in the signal path is minimized by the low impedance levels between cascoded circuits (note that the load resistance is usually kept small).

Differential-mode operation will reduce the circuit sensitivity to common-mode noise sources such as power supply interference and crosstalk. However, there are some digital logic functions which cannot be directly implemented as differential-mode versions of the single-ended logic circuit, such as the NOR function. Other disadvantages of a fully differential circuit topology are higher circuit and interconnect complexity. Complexity is not an important factor in this work, since these circuits would be fabricated in a sub-micron LSI process with multi-level interconnect technology.

There are two operating modes for the latching comparator, the transparent mode and the latched mode. The circuit alternates between transparent and latched modes depending upon the state of the clock inputs. A clock signal (CK, CKB), driving the differential pair formed by Q_5 and Q_6 , steers current between two cascoded differential circuits with shared collector resistors (Q_1 to Q_4). In the transparent mode, differential pair Q_1 and Q_2 buffers the D-inputs (D, DB) to provide an initial bias condition for the latch stage. The other differential pair (formed by transistors Q_3 and Q_4) is activated by a change in the state of the clocking signal, and latches the initial condition present at the collector by positive feedback action through emitter followers Q_7 to Q_8 . Therefore the latching comparator acts as a data sampler and one-bit A/D converter. Precision of the sampling action is improved

Figure 4.4 : ECL latching comparator.

over a FET design due to the higher transconductance and lower input offset voltages of the bipolar transistors. Accurate sampling of the input signal reduces timing jitter caused by non-ideality of the phase detector. The emitter follower buffers in the latch stage minimize circuit loading and increase the circuit speed, at the expense of increased power dissipation. Bias current for the stage (I_{CS}) is set by the bias voltage applied to the input of the transistor current source, Q9.

A metastable state is possible in any practical synchronizer circuit, and the response of the circuit in the metastable state must be considered. Oscillatory metastability only occurs in circuits where the delay in the positive feedback path of the latch is sufficiently long compared to the rise or fall-time of the latch outputs [29]. It is induced either by applying a short duration pulse to one of the latch inputs or by a time skew between the inputs to the latch. The ECL latching comparator should not produce an oscillatory response in the metastable state. This is because the delay around the feedback path of the latch (e.g., transistors Q₃ and Q₇ in Figure 4.4) is very small; equal to the propagation delay of a single differential mode ECL inverter. Also, the latch is differentially driven so that there can be no timing skew between set and reset inputs. The set input to the latch is the base of transistor Q₃ and the base terminal of transistor Q₄ is the reset input of the latching stage. These inputs are driven by the differential signal developed at the collectors of the input pair when (Q₁ and Q₂ in Figure 4.4) in the transparent mode, so these inputs are not really "pulse" driven. Therefore an oscillatory response is usually not observed with this circuit.

However, there are three equilibrium points for the ECL latch. Two of them are the stable logic states and the third is a metastable point. Analog metastability will occur if the set and reset inputs are biased at the same potential when the circuit is switched from the transparent mode to the latched mode. The circuit will eventually reach one of the stable operating points due to noise at the latch inputs or a change of state at the clock inputs (i.e., change from transparent to latched mode). When functioning as a component in a binary quantizing phase detector, the actual logic decision is irrelevant because a lead output or a lag output are equally likely when the local clock and received data are phase-locked. Therefore an "incorrect" logic outcome or error due to a metastable event, which can be catastrophic in other digital circuit applications, is unimportant here. It is possible that a short duration pulse (i.e., a pulse shorter than the clock period) could be produced by the phase detector in response to a metastable event. A short pulse could trigger metastability or otherwise disrupt the operation of other circuits such as the digital filter. Therefore a pulse conditioning circuit which would reject short duration pulses may be required in order to properly interface the phase detector to the digital loop filter. One possible implementation for such a circuit is given in Best [10].

4.2.3 The Resettable Latching Comparator

The latching comparator circuit can be easily modified to implement the asynchronous hold and reset functions. When the hold input is active, the current latch state must be held or frozen at the circuit outputs. One possible implementation of such a latching comparator is illustrated in Figure 4.5. Another stage of current steering logic (Q_{10} and Q_{11}) has been added in series with the data input tree of the comparator. This circuit gates the clock signal so that the clock will be inhibited when the hold inputs are active (inputs H and HB), and therefore the circuit will remain in the latched mode. The state of the latch when the hold input is activated will be frozen until the hold signal is removed. The hold inputs are differentially driven to improve the circuit noise immunity and to eliminate the need for a reference voltage at one input to the differential pair. The collector-emitter voltage drop across all of the devices connected in the current path between V_{CC} and V_{EE} is reduced by adding another differential pair in series. However, this causes only a slight degradation in the switching speed of the transistors and the maximum toggle rate of the latch. The common-mode voltage required to properly drive the hold inputs is lower than the common-mode voltage at the data inputs to the latch. Therefore diodes have been added in series with the emitter follower buffers to level shift the output signal to the desired level.

Transistor Q_{12} will asynchronously reset the latch output when the circuit is in the latched mode. This feature is required to ensure that the outputs of the phase detector cannot both be at a logical high level. If such a condition were allowed to occur, the circuit would not respond to changes at the data inputs, which is undesirable. The reset and hold inputs require different d.c. bias levels for proper circuit operation. The d.c. level at the output q_1 as shown in Figure 4.5 is compatible with the reset input (RST) of the latch and the outputs q_2 and q_{2b} are compatible with the hold inputs of this modified latching comparator.

The switching speed of the ECL latching comparator is related to the switching behaviour of the basic building block of the circuit, which is the differential pair. A method of optimizing the switching speed of the differential amplifier or ECL inverting gate will be presented in the following section. The results of this analysis will then be applied to the design of the phase detector.

Figure 4.5: ECL latching comparator with asynchronous hold inputs

4.2.4 Optimization of an ECL Gate

The schematic diagram of a differential-mode ECL inverter is illustrated in Figure 4.6. The operation and design of standard ECL circuits has been adequately described elsewhere and will not be reviewed here [30].

The propagation delay time (t_{pd}) of a logic gate is often used as a figure-of-merit when discussing the performance of digital logic. It is defined as the time delay between the 50% point in the low-to-high transition point of the input waveform and the 50% point in the high-to-low transition of the output waveform. The propagation delay time (τ_{pd}) of the inverter and the circuit parameters are related by the following expression

$$\tau_{pd} \propto R_L C_{eff} = \frac{\Delta V}{I_{CS}} C_{eff} = \frac{\Delta V (V_{CC} - V_{EE})}{P} C_{eff} \quad (4.1)$$

where R_L , I_{CS} , and V_{EE} are load resistance, bias current and supply voltage for the differential pair Q_1 , Q_2 (see Figure 4.6). The inverter power dissipation is given by P in equation 4.1 (note that $P = I_{CS} \cdot V_{EE}$, assuming that V_{CC} is connected to ground) and power dissipated in the emitter follower buffers Q_3 and Q_4 has been ignored in the development of this expression. Capacitance C_{eff} is the effective capacitance at the collector of each switching transistor due to device and interconnect capacitance, and ΔV is the difference between high and low logic levels (i.e., the output voltage swing).

From this equation it can be seen that either the circuit switching speed can be increased or the power dissipation of the circuit can be decreased, if the circuit is designed with a small logic voltage swing. The logic voltage swing of the inverter is determined by the selection of the bias current (I_{CS}) and the load resistance (R_L). Equation 4.1 also shows that the propagation delay can be reduced by choosing a logic voltage swing (ΔV) which is as small as possible for a given supply voltage and power dissipation. This equation illustrates a relationship between power consumption and switching speed for ECL which is consistent with other digital logic families [31].

Analytical expressions relating the propagation delay time of the inverter to a circuit model of the bipolar transistor have been derived by various authors [32]. However, these expressions are often inaccurate in predicting the propagation delay time for circuits

fabricated with a given process technology. It has been shown that an accurate equation for the gate delay can be derived based on a sensitivity analysis of the inverter circuit using computer simulations [33, 34]. The resulting expression is a linear summation of time constants which are weighted by a factor that depends upon the circuit topology and the transistor circuit model. Similar expressions have also been derived based on a linearized charge-control model for the bipolar transistor [32].

Figure 4.6 : Differential-mode ECL inverter.

Sensitivity analysis will be used here to optimize the switching speed of the differential mode ECL inverter shown in Figure 4.6. The npn transistors are represented by the Gummel-Poon model of the bipolar junction transistor in the HSPICE circuit simulator, as shown in Figure 4.7. An accurate equation relating all the time constants of the equivalent circuit for the ECL inverter to the propagation delay would necessarily involve a large number of terms because of the transistor model complexity. A few assumptions can be made which will simplify this expression, and these assumptions have a negligible impact on the accuracy of the resulting delay equation. Second-order effects in the transistor

Figure 4.7 : Transistor equivalent circuit used in HSPICE [93].

model, most notably the effect of high current densities on the behaviour of the transistor, will be neglected. It will be assumed that the bias current of the inverter will be below the high-level current injection region, but the bias point will be chosen so that the transition frequency (f_T) of the active devices is almost at its maximum value. In this region of operation the transit time and current gain are not strongly dependent on the bias current. The extrinsic and intrinsic base resistances will be lumped together into a single parameter by neglecting the current dependence of the intrinsic base resistance. The base-collector junction of the active devices in the inverter are always reverse biased and so the effects of reverse transit time and collector-base diffusion capacitance will be ignored. The resulting equation [34] which relates the significant circuit time constants to the inverter propagation delay can then be written as

$$\tau_{pd} \approx K_1 \tau_F + K_2 (R_B C_{JC}) + K_3 (R_B C_{JE}) + K_4 (R_L C_{JC}) + K_5 (R_L C_{JS}) + K_6 (R_L C_L) + K_7 (R_E C_{JC}) + K_8 (R_B C_{DE}) + K_9 (R_L C_{JCX}) + K_{10} (R_L C_{JCX}) \quad (4.2)$$

where τ_F is the forward transit time of the bipolar transistor, the factors K_x are proportionality constants, and the various other parameters are as defined by Figures 4.6

and 4.7. These delay terms do not represent time constants of the inverter circuit in the conventional sense often used in analytical descriptions of circuit behaviour. Each delay term represents the average contribution of a resistance or capacitance (which for the semiconductor devices will be time dependent) to the inverter propagation delay as the circuit is switched between logic states.

Examination of the time constants in equation 4.2 reveals that the following factors make a significant contribution to the propagation delay of the circuit:

1. Components in the equivalent circuit which share a common circuit connection and are connected in the signal path. An example of this is the time constant associated with factor K_5 in equation 4.2, $R_L C_{JS}$.
2. Components which are related by feedback interaction. An example of this is the delay term associated with constant K_7 . The extrinsic emitter resistance, R_E , affects the gain of the inverter because it is an emitter degeneration resistor. The inverter gain and the feedback capacitance from collector to base (C_{JC}) are influenced significantly by the Miller effect. This interaction is represented by three terms in equation 4.2; the terms with constants K_4 , K_7 , and K_{10} .
3. Factors which represent the intrinsic device delay, such as the transit time for current flowing between emitter and collector terminals, τ_f .

It should be noted that the time constant $R_L C_{DE}$ is redundant and does not appear in equation 4.2. This is because the base-emitter diffusion capacitance of the transistor model can be written as [35]

$$C_{DE} = \frac{\tau_f I_{EE}}{\Delta V_{BE}} \quad (4.3)$$

The change in base-emitter voltage (ΔV_{BE}) is equal to the logic voltage swing of the inverter if the effects of the transistor extrinsic resistances are neglected, and equation 4.3 can be re-written as

$$C_{DE} = \frac{\tau_F I_{EE}}{I_{CS} R_L} = \frac{\tau_F}{R_L} \quad (4.4)$$

Therefore the effect of the diffusion capacitance-load resistance time constant is included in the propagation delay expression by the $K_1 \tau_F$ term in equation 4.2. It should be noted that I_{EE} is equal to I_{CS} for the ECL inverter circuit of Figure 4.6.

Figure 4.8 : ECL inverter chain.

The proportionality constants in equation 4.2 can be determined by a sensitivity analysis using the HSPICE [93] circuit simulator. The circuit shown in Figure 4.8 was used for these simulations. Inverter I2 is embedded in a chain of identical inverters in order to properly simulate the input waveforms applied to the inverter and output loading effects. The circuit parameters of inverter I2 are varied while the parameters of the input source and inverters I1, I3 and I4 are kept constant, and the effect of the parameter variation on the propagation delay of the inverter is measured. For example, the proportionality constant for the term $R_B C_{JC1}$ can be computed as follows:

1. Using HSPICE evaluate the difference in inverter propagation delay ($\Delta\tau_{pd1}$) when the base resistance (R_B) is increased to a value slightly larger than nominal (R_{Bp}).
2. Repeat step 1 to find a delay difference, $\Delta\tau_{pd2}$, using a value of intrinsic base-collector capacitance (C_{JC1p}) which is higher than the nominal value, C_{JC1} .

It can be shown that the proportionality constant is given by

$$\frac{\partial \tau_{pd}}{\partial R_B \partial C_{JCI}} = K_2 \approx \frac{\Delta(\Delta \tau_{pd})}{\Delta R_B \Delta C_{JCI}} = \frac{\Delta \tau_{pd2} - \Delta \tau_{pd1}}{(R_{Bp} - R_B)(C_{JCIp} - C_{JCI})} \quad (4.5)$$

The other constants can be found using a similar procedure. However, constants K_1 and K_8 must be computed jointly because these terms both involve the forward transit time, τ_F . After each simulation run, a plot of the inverter output waveform was examined to ensure that the circuit operation was not significantly altered by the change in a given circuit parameter.

An expression for the propagation delay of an ECL inverter using minimum geometry devices in the BiCMOS process has been computed using this method. Nominal parameters for the bipolar transistor model were assumed for this analysis (note that C_{JCX} for the nominal parameters provided was zero). The device parameters are proprietary information and unfortunately cannot be listed here. A load resistance (R_L) of 600 Ohms and a bias current (I_{CS}) of 400 μA were assumed, which gives a logic voltage swing of 240 mV for the inverter. The emitter resistance (R_{EF} in Figure 4.6) is related to the current flowing through the resistor (I_{EF}) by the equation

$$R_{EF} = \frac{V_{CC} - V_{EE} - V_{BE} - (\Delta V/2)}{I_{EF}} \quad (4.6)$$

assuming an output voltage at the mid-point of the logic swing. For the inverter design the following assumptions are also made in the calculation of R_{EF} :

follower bias current : $I_{EF} = 400 \mu A$
 logic voltage swing : $\Delta V = 240 \text{ mV}$
 base-emitter voltage : $V_{BE} \approx 0.85 \text{ V}$
 supply voltage : $V_{CC} - V_{EE} = 5 \text{ V}$

Then from equation 4.6

$$R_{EF} = \frac{5 - 0.85 - 0.12}{400 \times 10^{-6}} = 10.1 \text{ k}\Omega$$

A sensitivity analysis of the inverter circuit using these parameters resulted in the following propagation delay expression

$$\begin{aligned} \tau_{pd} = & 1.76\tau_F + 2.61(R_B C_{JC1}) + 0.95(R_B C_{JE}) + 1.96(R_L C_{JC1}) + \\ & 0.38(R_L C_{JS}) + 3.33 \times 10^{-2}(R_L C_L) + 4.35(R_E C_{JC}) + \\ & 1.48(R_B C_{DE}) \end{aligned} \quad (4.7)$$

The contributions of each term to the total propagation delay time are illustrated by the bar graph of Figure 4.9. The contribution of the load capacitance to the total propagation delay (given by the term $K_6 R_L C_L$) is negligible because of the light load assumed for the simulation. The nominal propagation delay predicted by HSPICE for the circuit is 115 ps and the propagation delay predicted by equation 4.2 for the same circuit is 114.9 ps. This excellent agreement shows that the simplified expression for propagation delay gives accurate results for the inverter circuit configuration.

Equation 4.7 can also be used to predict the propagation delay of an inverter consisting of other transistor geometries within the same technology. If active devices which are four times the minimum size geometry (4X devices) are chosen for the circuit design, then the bias current must be increased so that operation in the region close to the peak f_T of the transistor is maintained. Also, as the bias current is increased, the load resistance must be decreased by the same factor so that the logic voltage swing remains constant. If a load resistance of 150 Ohms and a bias current of 1.6 mA are assumed for the inverter circuit with 4X active devices, equation 4.6 predicts a propagation delay of 78 ps. An inverter delay of 84 ps was predicted by HSPICE for the same circuit.

The good agreement between predicted and simulated results makes the propagation delay equation a useful aid when designing the ECL inverter to achieve minimum delay time. Careful examination of the contributions made to the overall delay time by each parameter in the device model can also be used by device designers when optimizing the transistor layouts and the fabrication process for a given technology. For example, Figure 4.9 graphically illustrates that, aside from propagation delay due to the device transit time, the delay terms involving the base resistance (R_B) make the most significant contribution to the total inverter delay. Thus it would be desirable to lower the base resistance in order to improve the circuit performance. Base resistance can be lowered by making some adjustment to the fabrication process (e.g., higher concentration of dopant in the extrinsic

base), but process changes which affect R_B can also have an effect on other device parameters, such as junction capacitances. A new set of device parameters can be computed which will reflect the modified process. Since all the relevant parameters are accounted for in equation 4.7, the change in circuit performance caused by a change in R_B and any other related parameters can be accurately modelled. Therefore the relationship between a process variable and the circuit behaviour can be described in a way which allows the circuit performance to be optimized.

Figure 4.9: Weighted delay components for the ECL inverter from equation 4.7.

A similar procedure can be used to determine the load resistance for the inverter circuit. An expression which gives the optimum load resistance of the inverter as a function of the device model and circuit parameters can be derived from equation 4.2 as follows

$$\frac{\partial \tau_{pd}}{\partial R_L} = K_4 C_{JC} + K_5 C_{JS} + K_6 C_L + \frac{K_8 R_B \tau_F}{R_L^2} = 0 \quad (4.8)$$

Solving for the minimum propagation delay as a function of load resistance gives

$$R_{Lopt} = \sqrt{\frac{K_8 R_B \tau_F}{K_4 C_{JC} + K_5 C_{JS} + K_6 C_L}} \quad (4.9)$$

Equation 4.9 has been used to compute the optimum load resistance for two different transistor geometries. The results are summarized in Table 4.1 along with the propagation delays predicted using equation 4.7 and HSPICE.

Table 4.1: Comparison of inverter performance using HSPICE and equation. 4.7.

Transistor geometry	Bias Current, I_{CS}	R_L	t_{pd} from HSPICE	t_{pd} from Eq. 4.7	Error in t_{pd} , $\Delta\%$	R_{Lopt}
minimum size	400 μA	600 Ω	115 ps	114.9 ps	-0.1%	434 Ω
4 X minimum size	1600 μA	150 Ω	84 ps	78 ps	-6.6%	147 Ω

The voltage swing at the gate input must be sufficient to switch the bias current of the differential pair including a margin for noise and interference. The logic voltage swing is set by the product of the bias current and the load resistance (i.e., $I_{CS} \cdot R_L$). The unity gain-bandwidth of the bipolar transistor (which is related to the device f_T) is dependent upon the bias current of the device, but this dependence can be neglected if operation in the high current regime is avoided over the anticipated range of temperature and power supply voltage. Therefore the load resistance cannot be chosen solely on the basis of minimizing propagation delay, since the bias current is fixed by device bandwidth considerations.

The differential input voltage required to fully switch the current through the differential pair (assuming no emitter degeneration) is five times the thermal voltage ($5V_T \approx 5T/11600$, where T is the device temperature in Kelvin) [36]. Small geometry polysilicon emitter transistors have a significant extrinsic emitter resistance and will require a larger input voltage than $5V_T$. Also, some margin is necessary to account for the effects of random noise and the noise induced by current switching.

For a maximum junction temperature of 125 C,

$$5V_T = \frac{5(125+273)}{11600} = 172 \text{ mV}$$

Assuming a bias current of 500 μA and an extrinsic emitter resistance of 25 Ω ,

$$\text{emitter degeneration} = I_{CS}R_E = 500 \cdot 25 = 12.5 \text{ mV}$$

Adding a 10% margin for noise gives a total logic voltage swing of

$$\Delta V = 1.1(172 + 12.5) = 203 \text{ mV}$$

A typical logic swing for custom ECL integrated circuits is 450 mV if single ended signals and an input reference voltage are used. A differential-mode circuit would require one-half of this value, or 225 mV. Since differential-mode operation is less susceptible to power supply interference and crosstalk, a logic swing of 200 mV should be adequate. It should be noted that for the inverter design with a 400 μ A bias current (refer to Table 4.1), the load resistor required for a 200 mV swing is larger than the R_{Lopt} calculated from equation 4.9. Therefore there is a strong motivation to use the smallest voltage swing possible, and internal logic swings as small as 150 mV have been used in some experimental ECL circuitry designed for very high-speed applications [26].

In summary, a propagation delay equation for the ECL inverter has been developed using sensitivity analysis of the circuit with the HSPICE circuit simulator. This resulting equation has been used to show that for a given bias current (which should be chosen to minimize device switching time) there will be an optimum value of load resistance which minimizes the switching delay. Also, it has been shown that there is another constraint on the load resistance because the logic voltage swing must be large enough to guarantee proper switching under all anticipated operating conditions. These design criterion will now be applied to the design of the ECL latching comparator circuit and the binary quantizing phase detector.

4.2.5 Phase Detector Circuit Design

The phase detector circuit consists of six ECL latching comparators and has been described in section 4.2 of this chapter. In order to minimize the layout area and power dissipation of the phase detector, the minimum geometry transistors available in the BiCMOS process (a device with a 4 μ m X 0.8 μ m emitter area, also called a 1X device) will be used in this design. Bias and load resistor values for the latches shown in Figures 4.4 and 4.5 will be chosen so that the switching speed of the circuit is optimized.

From preliminary measurements and device modelling, a bias current of 500 μA for the 1X devices was chosen to avoid performance degradation of the switching devices at the maximum operating temperature of 125 C. At this bias current, the switching transistors will operate at a bias point corresponding to almost the maximum device f_T over the desired range of operating conditions (i.e., temperature, supply voltage and process variations). Device switching time can be adversely affected by high current effects at elevated temperatures, unless the bias current is carefully selected. A junction temperature of 125 C corresponds to an ambient temperature between 85 and 95 C, assuming a 30 to 40 C difference between the junction and ambient temperatures. This specification for maximum ambient temperature has been demanded by many telecommunications operating companies for new data transmission equipment and many manufacturers are designing new equipment to meet this specification.

For a logic voltage swing of 200 mV,

$$R_1, R_2 \text{ (see fig 4.4)} = \frac{\Delta V}{I_{CS}} = \frac{0.2}{500 \times 10^{-6}} = 400 \, \Omega \quad (4.10)$$

and this is only slightly lower than the optimum load resistance calculated for the ECL inverter using sensitivity analysis of the gate propagation delay. The same value of load resistance will be used for both types of latching comparator circuits (i.e., simple latch and the resettable latch with hold inputs). The slight increase in bias current (I_{CS}) from 400 to 500 μA will cause the R_{Lopt} as given by equation 4.9 to decrease slightly, because the forward transit time is the dominant term in the propagation delay equation, and the transit time decreases with increasing bias current. Therefore the optimum load resistance should be close to 400 Ohms at a bias current of 500 μA .

Minimum size transistors were also chosen for the emitter follower buffer stage of the latch (Q7 and Q8) in order to minimize the capacitive loading of the buffer transistors on the differential amplifier. Assuming the following conditions:

follower bias current : $I_{EF} = 400 \, \mu\text{A}$

logic voltage swing : $\Delta V = 200 \, \text{mV}$

base-emitter voltage : $V_{BE} \approx 0.85 \, \text{V}$

supply voltage : $V_{CC} - V_{EE} = 5 \text{ V}$

Then from equation 4.6,

$$R_3, R_4 \text{ (latch)} = \frac{5 - 0.85 - 0.1}{400 \times 10^{-6}} = 10 \text{ k}\Omega$$

It was determined by circuit simulation using HSPICE that a change in follower bias current between 400 and 500 μA had little effect on the circuit performance. A bias current of 400 μA was chosen to reduce power dissipation without seriously degrading the circuit performance over the desired operating temperature range.

The latch with asynchronous hold inputs (see Figure 4.5) has a level shift at the output due to the diode connected in series with the output follower. Therefore the value of the bias resistor must be slightly reduced so that the follower bias current remains at 400 μA . Assuming that the voltage drop across the diode connected transistor is equal to one base emitter voltage drop,

$$R_3, R_4 \text{ (resettable latch)} = \frac{5 - 2(0.85) - 0.1}{400 \times 10^{-6}} = 8 \text{ k}\Omega$$

The bias current source for the latching comparator (Q_9 in Figure 4.4) was implemented as a single transistor with emitter degeneration. A bipolar transistor current source was chosen as the active device for the current source, because of the small parasitic capacitance and high output resistance of the device compared to an NMOS transistor operated at the same bias current. This improves the rejection of undesired common-mode signals by the differential amplifier current switch. The current density of the source transistor was made consistent with the current density of the switching transistors in the circuit and therefore a minimum size transistor is required. The degeneration resistance R_{CS} was made equal to the value of the latching comparator load resistance (R_1, R_2 in Figure 4.4).

A schematic diagram of the current source bias circuit is shown in Figure 4.10. A reference voltage

$$V_r = I_b \cdot R_2 + 2V_{BE} \quad (4.11)$$

is generated by current I_b flowing through diode connected transistors D_1, D_2 and resistor R_1 . The bleeder current (I_b) is much greater than the base current drawn by transistor Q_1 , because of the high transistor current gain ($\beta > 50$), and so the current flowing through R_2 is approximately equal to the bleeder current. The current source reference voltage, V_{CS} , is equal to V_T minus the base-emitter voltage drop of transistor Q_1 . Current I_e is chosen so that the emitter current of transistor Q_1 is almost equal to the current flowing through the two diodes.

Figure 4.10 : Bias voltage generator.

When the bias network output is connected to a current source transistor (such as Q_9 in Figure 4.4) the emitter current of the current source will be

$$I_{CS} = \frac{V_T - 2V_{BE}}{R_{CS}} = \frac{I_b R_2}{R_{CS}} \quad (4.12)$$

and current I_b weighted by the resistor ratio R_2/R_{CS} flows through the bipolar transistor current source. Computation of the actual component values for the bias network is straightforward and will not be detailed here.

The use of emitter degeneration increases the output resistance of the current source. Also, any voltage drop due to current flow through the power supply connection between the current source and the bias network will have less effect on the bias current if emitter degeneration is used.

The temperature coefficient of the base-emitter voltage drop across Q_1 and the current source transistor (between -1.5 and -2.0 mV/C) is compensated for by the voltage drop across diodes D_1 and D_2 in Figure 4.10. Any change in V_{BE} does not affect the source current given by equation 4.12 because of a compensating shift in the bias network output voltage. However, if the input to the bias network is a voltage source (i.e., a constant voltage (V_b) rather than a constant current (I_b)), then the bleeder current and mirrored current will have a temperature coefficient caused by a change in V_{BE} with temperature. In general, the transistor current gain (β) and the resistor values also have some temperature dependence, but the temperature variations of these parameters tend to cancel the change in base-emitter voltage with temperature [30]. The net effect is a slight increase in the mirrored bias current with increasing temperature.

4.2.6 Phase Detector Circuit Simulations

The performance of the binary quantizing phase detector proposed in section 4.2.1 of this chapter has been investigated using the HSPICE circuit simulator. The latching comparator and resettable latching comparator designs (see Figures 4.4 and 4.5) have been chosen for the proposed circuit implementation. The component values calculated in section 4.2.5 for the latching comparators have been used in the circuit simulations of the phase detector. Model parameters for the bipolar transistors corresponding to the nominal BiCMOS process have been used in all of the following circuit simulations.

A block diagram of the simulated network is shown in Figure 4.11. The phase detector is driven by the differential data and clock signals V_{data} and V_{clk} . The waveforms applied to the data and clock inputs for all of the simulations were unfiltered with 200 ps rise and fall-times and a differential signal amplitude of 200 mVolts p-p unless otherwise noted. An

ECL inverter circuit (refer to Figure 4.6) was used to buffer the lead and lag outputs of the phase detector. The smallest geometry bipolar devices available in the BiCMOS process were used for the inverter design. A load resistance of 400 Ohms and an output logic voltage swing of 200 mVolts were chosen for the phase detector buffer design.

A single bias network was used to set the bias current in the latching comparators and the output buffer inverters. The bias network shown in Figure 4.10 was used for this purpose and the following set of components were selected for this design:

$$R_1 = 6200 \, \Omega$$

$$R_2 = 400 \, \Omega$$

$$R_3 = 3600 \, \Omega$$

Diodes D_1 and D_2 have been realized using diode connected transistors and the minimum geometry bipolar devices available in the BiCMOS process (i.e., 1X transistors) have been used in the design of the bias circuit.

Figure 4.11 : Block diagram of the network used for HSPICE simulation.

When the clock is synchronized or phase-locked to the received data, the phase relationship between the data and clock signals will be controlled by the PLL so that the average

frequency of the timing clock is equal to the bit-rate of the received data stream. If the average clock frequency deviates slightly then the phase relationship between transitions in the clock and data pulses will vary with time. This effect has been used to investigate the behaviour of the phase detector circuit as the phase relationship between the data and clock signals changes from the one state (either lead or lag) to the other state.

The period of the clock signal was altered by a small time increment with respect to the bit interval of the data signal. The plot shown in Figure 4.12 illustrates the response of the phase detector to an alternating data bit stream at 1 Gbit/s and a 1.0005 GHz clock signal. The positive transition of the clock is shifted by 0.5 ps with respect to the data transitions every clock cycle. A time delay is added to the clock signal so that the positive transitions of the clock signal initially lag the positive transitions of the data signal. As the simulation progresses, the phase lag between the clock and data streams decreases because the clock period is smaller than the data bit-interval. The output pulses produced by the phase detector indicate a phase-lagging condition until a simulation time of 20 ns is reached, as shown in Figure 4.12. At this point, the circuit detects that the clock/data phase relationship has changed to a phase-leading condition and pulses are produced at the lead output of the phase detector. The width of the output pulses is equal to the pulse width of the incoming data bits. It should be noted that only one of the differential inputs or outputs is plotted for each signal.

There is a delay of one clock cycle between the sampling of the input data and the generation of an output pulse by the phase detector. Also, the circuit generates an output pulse only when there is a positive transition in the received data. Thus the transition between the generation of lag and lead pulse trains corresponds to a measurement of the clock/data phase relationship at a simulation time of 20 ns. Although it is difficult to discern from the plot shown in Figure 4.12, the time difference between the positive-going clock and data edges (Δt) can be calculated from the following equation:

$$\Delta t (\text{data-clock}) = t_d - (n_t \cdot \Delta T) \quad (4.13)$$

The time delay, t_d , is the initial delay added to the clock signal and the parameter, n_t , is the number of data bits between the start of the simulation and the change of state in the phase detector output. The time difference between the bit-interval of the data stream and the clock period is given by ΔT in equation 4.13.

Figure 4.12 : Response of the phase detector circuit to an input phase error transition from phase-lagging to phase-leading ($\Delta T = 0.5 \text{ ps}$).

Figure 4.13: Response of the phase detector circuit to an input phase error transition from phase-leading to phase-lagging ($\Delta T = 0.5 \text{ ps}$).

Figure 4.14 : Response of the phase detector circuit to an input phase error transition from phase-lagging to phase-leading ($\Delta T = 0.1 \text{ ps}$).

For the simulation shown in Figure 4.12, the transition between lag and lead states can be calculated using equation 4.13 for an initial t_i - delay (t_d) of 25 ps as

$$\Delta t = 25 \text{ ps} - (20 \text{ bits} \cdot 0.5 \text{ ps/bit}) = 15 \text{ ps}$$

Thus there is a 15 ps time difference between the actual transition from a lagging to leading phase condition between the clock and data streams and the phase relationship measured by the phase detector. This timing offset will lead to a static phase error in the phase-locked loop and is an undesirable source of timing jitter. Also, there is a glitching at the lag output when the outputs of the phase detector change state. The effect of a short pulse or glitch on the digital loop filter would have to be considered in the overall PLL design, and additional circuitry to remove glitching may be required.

The response of the phase detector circuit during the transition from a phase-leading to lagging condition is shown in Figure 4.13. This is the "reverse" of the simulation shown in Figure 4.12. Because of marginal timing between the clock and data streams, a zero bit in the data stream is not detected and consequently a lag pulse which is three data bit intervals long is generated at the lag output. The clock is lagging the data signal by 14 ps at the point where the phase detector outputs change state from lead to lag. This compares favorably with the 15 ps time delay for a lag-to-lead phase transition from the previous simulation, and thus the behaviour of the circuit is consistent for both lead-to-lag and lag-to-lead phase transitions.

A smaller timing difference ($\Delta T = 0.1$ ps) was used to produce the simulation shown in Figure 4.14. The data bit pattern chosen for this simulation was two consecutive one bits followed by two zero bits, which results in a 250 MHz square wave. The clock signal shown in Figure 4.14 is offset by -0.5 Volts to improve the clarity of the plotted waveforms. The outputs are well-behaved with almost no glitching, and the two phase detector outputs are mutually exclusive. There is some uncertainty in the phase detector output in the range from 26 ns to 74 ns. The clock signal is lagging the data signal by between 11.8 and 15.2 ps in this region. It can be concluded from the results of this simulation that there will be uncertainty in the output of the phase detector even when the effects of noise and voltage offsets are neglected. The finite rise-time of the data signal is one of the major sources of this measurement uncertainty.

Figure 4.15 : Response of the phase detector circuit to an input phase error transition from phase-lagging to phase-leading ($\Delta T = 0.5 \text{ ps}$, $V_{clk} = 300 \text{ mV p-p}$).

Figure 4.16 : Response of the phase detector circuit to an input phase error transition from phase-lagging to phase-leading ($\Delta T = 0.5 \text{ ps}$, $V_{data} = 300 \text{ mV p-p}$).

The effects of the input signal slew rate on the phase detector response are illustrated in Figures 4.15 and 4.16. The signal slew rate was varied by changing the signal amplitude while keeping the rise-time and fall-time constant. The first simulation shown in Figure 4.12 was repeated with the clock amplitude increased from 200 mVolts p-p to 300 mVolts p-p and the results are shown in Figure 4.15. As the slew rate of the clock increases, the pulses output by the phase detector become ill-defined close to the transition point between lag and lead output states. Also, the timing lag of the clock signal at the transition point increases when the slew rate of the clock signal is increased (i.e., Δt increase from 15 ps to 20 ps). This indicates that the error in phase measurement is related to the slew rate of the clock signal. Feedthrough of the clock signal, from the clock inputs to sensitive circuit nodes such as the inputs of the latch stage, is probably one of the causes of this error. The fundamental and higher harmonics of the clock signal can be easily coupled from the inputs to other circuit nodes via device parasitics.

The measurement accuracy can be improved by increasing the slew rate of the data signal as shown in Figure 4.16. The behaviour of the phase detector at the transition point in the circuit output is improved when compared the circuit performance in the previous simulations. The transition or change in the output state occurs when the clock lags the data by only 2 ps, which is a considerable improvement in phase measurement accuracy.

Figure 4.17 : Graph of phase error versus input signal amplitude.

The effects of clock and data slew rate on the input phase error at the transition point in the phase detector outputs are illustrated in Figure 4.17. The slew rate of the signals is varied by changing the signal amplitude while maintaining a constant rise and fall-time of 200 ps for each signal transition. Therefore the slew rate of the signal is directly proportional to the signal amplitude. The phase measurement error decreases with increasing data amplitude, because the ambiguity in the data transitions decreases as the amplitude of the signal transitions is increased. However, feedthrough of signal transients on the data inputs also affects the phase measurement error, and for large data amplitudes (or higher slew rate input signals) this error becomes significant (e.g., the error is -15 ps for a data signal amplitude of 600 mV p-p). The optimum data signal amplitude is approximately 300 mV p-p, given a clock signal amplitude of 200 mV p-p and 200 ps signal rise and fall-times.

Increasing the slew rate of the clock signal tends to increase the measurement error because of clock feedthrough effects. Coupling of transients in the clock signal from the clock inputs to the internal nodes of the circuit through parasitic capacitances, alters the point at which the latching comparator switches from the transparent mode to the latched mode. The clock signal amplitude must be at least 200 mVolts p-p in order to achieve an adequate noise margin and proper operation of the phase detector circuit. Therefore it would be desirable to use the minimum amplitude clock signal and the optimum data signal amplitude for the expected on-chip signal rise and fall-times, in order to minimize the phase measurement error.

The maximum operating frequency of the phase detector was also determined using the HSPICE circuit simulator. For clock frequencies greater than 2.4 GHz, the output pulses produced by the circuit were inconsistent. The effects of process variability and parasitics introduced by the circuit layout and interconnections will cause a decrease in the maximum operating frequency. However, an operating margin greater than 2:1 in clock rate for application of the phase detector to a 1 GHz timing recovery PLL should be adequate.

Oscillatory metastability of the latching comparators has not been observed in the simulations of this design, although the effects of metastability on the behaviour of the circuit is an area where further study in simulation and on an experimental prototype would be desirable.

The performance of the phase detector predicted by the circuit simulator has not been verified experimentally. The phase detector circuit consists of a serial connection of latching comparators which is only slightly more elaborate than a master/slave flip-flop circuit. Therefore a benchmark of the performance which could be expected for the ECL latching comparator can be obtained through the study of a flip-flop circuit. The design, simulated behaviour and measured circuit performance of an ECL master/slave flip-flop will be the subject of the remaining sections of this chapter.

4.3 ECL Master/Slave Flip-Flop

An ECL master/slave flip-flop has been designed and fabricated in order to evaluate the performance capability of the latching comparator. The master/slave flip-flop is a digital functional block commonly used in more complex circuits such as multiplexers and demultiplexers, and the flip-flop also is an important part of the binary quantizing phase detector discussed earlier in this chapter. A block diagram of the master/slave flip-flop test circuit is shown in Figure 4.18. The circuit consists of a data (D) input buffer circuit, cascaded emitter-coupled logic (ECL) latching comparators, an output buffer and driver with open collector outputs, and a bias circuit to generate on-chip bias voltages.

Power is supplied at the V_{CC} and V_{EE} pads with a nominal supply voltage of 5 Volts (V_{CC} with respect to V_{EE}). Separate bias connections allow independent adjustment of the bias currents in the master/slave and output stages (normally V_{b1} and V_{b0} are connected to V_{CC}).

The master/slave flip-flop is realized by interconnecting two ECL latching comparators driven by anti-phase clock signals. The design objective for the demonstration circuit was to achieve the fastest possible operating speed without requiring excessive amounts of power or circuit area. It was determined by circuit simulation that the maximum clock speed of the ECL latching comparator could be increased by using two emitter followers in the positive feedback path of the latch. This modification to the basic design is shown in Figure 4.19. The penalties for this speed increase are an increase in power consumption due to the additional emitter follower stages and a slight increase in circuit area. However, these penalties were justified by a 50% increase in the maximum clock rate of the latch, as predicted by HSPICE simulations of the circuit.

Figure 4.18 : Block diagram of the master/slave flip-flop

4.3.1 Circuit Design

Standard transistor layouts were used throughout the latching comparator design for the flip-flop test circuit. The smallest geometry bipolar devices available in the BiCMOS process (1X devices) were used wherever possible to minimize power consumption and layout area. A demonstration circuit consisting mainly of minimum geometry devices is useful in establishing a performance benchmark for a new IC fabrication process. Therefore the minimum device size was used for switching transistors Q_3 to Q_8 shown in Figure 4.19.

A bias current of $500\ \mu\text{A}$ and a logic voltage swing of $200\ \text{mV}$ were chosen for the latch design. Consequently, the load resistance required for the latch and bias resistors for the first emitter follower stage are identical to the values computed in section 4.2.5 for the basic

2

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ECL latching comparator. Thus 400 Ohms will be used for resistors R_7 , R_9 , and R_{10} , and 10 kOhm resistors will be used for R_3 and R_5 in Figure 4.19.

Figure 4.19 : Modified ECL latching comparator used in the master/slave flip flop

A larger area device has been used in the second emitter follower stage of the latch shown in Figure 4.19, which is formed by transistors Q_{10} and Q_{12} . For a given load capacitance, a greater slew rate of the output signal can be achieved when a larger device is used. Also, the second-order effects which cause ringing of fast pulse transitions can be reduced by using a larger device geometry. The output inductance of the follower stage is directly proportional to the base resistance of the emitter follower circuit. By reducing the base resistance of the transistor, the resonance between the load capacitance and output inductance can be shifted to a higher frequency. The effect of making this resonant frequency much higher than the lower order harmonics of the pulse waveform is a reduction of ringing during signal transients. The intrinsic and extrinsic base resistance of the bipolar transistor are both inversely proportional to the emitter length, and therefore the device geometry chosen for Q_{10} and Q_{12} has a long emitter stripe ($16\text{ }\mu\text{m} \times 0.8\text{ }\mu\text{m}$). In order to maintain a constant current density through the larger device area, the follower bias current must be increased to $1600\text{ }\mu\text{A}$. Accounting for the extra base-emitter voltage drop across the first buffer stage, the bias resistors can be calculated in a similar manner as

$$R_4, R_6 = \frac{5 - 2(0.85) - 0.1}{1600 \times 10^{-6}} = 2\text{ k}\Omega$$

Figure 4.19 also shows the emitter follower buffers, Q_1 and Q_2 , which were added to the clock inputs of the latch to level shift and buffer the clock signal. The clock buffer decreases the circuit loading at the clock input, which reduces transmission line reflections and pulse ringing when the input signal lines are properly terminated. The bias resistor values were calculated assuming a bias current of $400\text{ }\mu\text{A}$ and a common voltage at the clock input of -2.5 Volts . The design value of resistors R_1 and R_2 used in the circuit of Figure 4.19 is $4.1\text{ k}\Omega$ ms.

Isolation between the two current paths can be modified by resistor R_8 . Reducing the isolation between the collectors of transistors Q_3 and Q_4 allows some bias current to flow in the cascoded differential pair that would otherwise be completely switched off. This bias technique reduces the time required to change the state of the latch as the bias current is steered from one pair to another. However, the latch will not function properly if the resistor is made too small. It was found from circuit simulations that the maximum clock rate of the latch could be improved by approximately 15%, if a $15\text{ k}\Omega$ resistor is connected between the collectors of Q_3 and Q_4 .

The output buffer is a differential amplifier stage with open-collector outputs, which can maintain fast signal transients when driving a 50 Ohm load (see Figure 4.20). The open-collector output buffer has sufficient gain and bandwidth to shape the output pulse without the undesirable second-order effects of a capacitively loaded emitter follower. It has been shown that in high-speed digital circuits the bandwidth of an emitter follower buffer is inferior to the open-collector driver [37]. The circuit shown in Figure 4.20 can directly drive a 50 Ω load (or matched 50 Ω transmission line) with a voltage swing proportional to the bias current of the output pair (I_0). This open-collector driver also has the advantages of lower power dissipation and a simpler interface to test equipment or other circuitry when compared to the follower configuration. Also, the circuit induces less switching noise on power supply lines and does not require an additional supply voltage when driving a low impedance load. However, the output levels are incompatible with commercially available ECL circuits.

Figure 4.20 : Open collector output buffer.

The bias current for the switching transistor Q_3 and Q_4 was chosen so that a differential output voltage swing of 600 mV p-p could be realized across a $50\ \Omega$ load. Device geometries were chosen so that the current density through each of the active devices was consistent with the latching comparator design.

4.3.2 Circuit Simulations

The performance of the flip-flop was investigated using the HSPICE circuit simulator. Nominal device models (rather than worst or best-case models) were used for all the simulations presented here as a basis for comparison with the experimental measurements. In order to perform realistic simulations, interconnect loading effects were included in the circuit description. A capacitance of 5 fF was added at each node in the circuit, which is a conservative estimate of loading due to component interconnections. It should be noted that a $10\ \mu\text{m}^2$ connection using the first level of interconnect metal in a typical BiCMOS process has a parasitic capacitance of less than 1 fF. Optimization of the IC layout ensures that the interconnect length is minimized at sensitive circuit nodes. However, a few lengthy interconnections are unavoidable in most circuit layouts and therefore a conservative estimate of the loading capacitance has been used in the simulations.

Figure 4.21 : Block diagram of the flip-flop circuit simulated using HSPICE.

The block diagram in Figure 4.21 illustrates the simulated network. A random sequence of pulses was input to the data (D) inputs to the flip-flop. The output of an ideal pulse generator was filtered by an RC lowpass filter, in order to limit the signal rise and fall-times to about 110 ps. The clock inputs are connected to a sinusoidal source. This is a good approximation of the timing signal in a high frequency system. A parasitic capacitance of 0.25 pF was assumed in parallel with the 50 Ohm load connected to each output.

Simulation results at clock frequencies ranging from 2.5 to 4.5 GHz are shown in Figures 4.22 to 4.24. The differential data and clock input waveforms are plotted along with the differential output signal (e.g., V_{out} in Figure 4.12). The average value of the differential signals is zero, and therefore a d.c. offset has been deliberately added to the input signals in order to improve the clarity of the plotted waveforms.

At a clock frequency of 2.5 GHz, the output signal reaches its full swing of 0.6 Volts peak-to-peak. However, the bandwidth of the open collector buffer circuit is approximately 1.2 GHz, which causes attenuation of high frequency components at clock frequencies greater than 2.5 GHz. This results in attenuation of higher harmonics at the output for the alternating 1 and 0 pulse sequence, as shown in Figures 4.23 and 4.24. The signals plotted in Figure 4.23 are the result of simulations at a junction temperature of 27 °C and at the worst-case operating temperature of 125 °C, with the flip-flop driven by a 4 GHz clock. There is a slight degradation in performance at high temperature, mainly due to the performance limitations of the output buffer. The output of the first latch stage is also plotted in Figure 4.24 for a 4.5 GHz clock input. Although the buffered signal is somewhat distorted, the internal signals have fast transitions and little distortion, indicating that the latching comparators operate properly at high frequency.

4.3.3 Experimental Measurements

The master/slave flip-flop has been fabricated as part of a test chip in the BiCMOS process. A photomicrograph of the circuit is shown in Figure 4.25. A number of samples have been tested using the experimental apparatus shown in Figure 4.26. A high-speed pseudorandom pulse generator was unavailable for testing, and therefore a simple alternating 1-0 pattern was used as the data input. This signal was generated using a variable frequency microwave source with an output frequency range of 300 kHz to 3 GHz. It should be noted that the signal source produces a sinewave which has relatively

Figure 4.22 : HSPICE simulation of the master/slave flip-flop, $f_{clk} = 2.5 \text{ GHz}$.

Figure 4.23 : HSPICE simulation of the master/slave flip-flop, fclk = 4.0 GHz.

Figure 4.24 : HSPICE simulation of the master/slave flip-flop, $f_{clk} = 4.5$ GHz.

slow rise and fall-times compared to a pulse generator operating at the same frequency. This limits the range of the clock input phase over which the circuit will properly synchronize the signal at the D-input of the flip-flop.

Figure 4.25 : Photomicrograph of the ECL master/slave flip-flop circuit.

The output of the microwave source was coupled through an attenuator and bias circuit to the D-input of the flip-flop. This allowed adjustment of both the amplitude and d.c. level of the input signal. The clock signal was derived by doubling the data signal, and therefore the frequency doubler output was a sinusoidal signal with a maximum frequency of 6 GHz. A passive phase shifter was used to adjust the phase relationship between the data and clock signals applied to the flip-flop. The doubler output was used to drive a high frequency pulse generator, which produced pulses at rates in excess of 5 GHz. The amplitude and d.c. level of the pulse generator outputs were varied independently, and passive phase shifters were used to adjust the phase relationship between the CLK and CLKB signals applied to the testchip.

The sampling oscilloscope must be triggered by a sub-harmonic of the clock or data signal. The trigger signal was derived by division of the data signal through a variable modulus divider circuit. The input termination resistance of the oscilloscope was used as the load resistance for the open collector buffer (a 50 Ohm load).

The circuit specifications determined from computer simulations are summarized in Table 4.2. The results of experimental measurements are also given in parentheses where applicable. Additional experimental measurements are listed in Table 4.3. Ten circuit

Figure 4.26 : Master/slave flip-flop test apparatus.

samples were tested, and 8 of these circuits operated at clock frequencies greater than 5 GHz. The maximum operating frequency observed was 5.3 GHz. Two of the circuits did not function; one chip had an obvious defect in metallization, and the other circuit drew no current from the power supply.

Table 4.2 : Master/slave flip-flop specifications.*

Chip size	1.5 X 0.5 mm ²	
Supply voltage	-5	Volts
Total power dissipation	128	mW (132.5 mW)
Power dissipation excluding input and output buffers	46	mW
Total number of components	39 transistors, 28 resistors	
Set-up time	30	ps
Hold time	0	ps
Propagation delay (clock falling edge to output)	370	ps

Current switch output (50 Ohm load)

Differential output voltage	600 mV p-p	(560 mV p-p)
Output pulse rise and fall-time (20 to 80 percent)	120 ps	(122 ps)

*Note that experimental results are shown in parentheses.

The clock phase margin was measured by adjusting the phase of the frequency doubler output, which changes the phase relationship between the clock and data input signals. The clock phase was varied until a change in pulse shape at the flip flop output was noted. The distortion of the output signal indicated that the data input was not being properly synchronized at that clock phase. The data input can be synchronized with the clock signal over a phase range equal to the clock phase margin. Ideally, the clock phase margin is 360

Table 4.3 : Measured performance of the master/slave flip-flop.

Maximum clock frequency (alternating 1-0
pattern)

5.3 GHz

Clock phase margin

Frequency	Clock amplitude	Data amplitude	Phase margin
2.5 Gb/s	250 mV p-p	250 mV p-p	185 degrees
5.0 Gb/s	500 mV p-p	500 mV p-p	117 degrees

Minimum clock amplitude
(differential clock input)

200 mV p-p (@ 2.5 Gb/s)

600 mV p-p (@ 5.0 Gb/s)

D-input sensitivity
(single-ended sinusoidal input)

< 100 mV p-p (@ 2.5 Gb/s)

< 200 mV p-p (@ 5.0 Gb/s)

degrees (i.e., degrees of clock phase). However, circuit imperfections and practical input signal waveshapes can cause a significant reduction in phase margin. The sinusoidal data signal used for the measurement had relatively slow rise and fall-times and this reduced the phase margin compared to pulse inputs, which typically have steeper edges. It was observed that the clock phase margin depended upon the amplitude of the D-input signal, indicating that the phase margin was restricted by the slow transitions of the sinusoidal waveshape. A large phase margin is desirable in order to accommodate timing variations caused by noise, temperature variations and pulse pattern effects.

Similarly, the data and clock waveshapes influence the input sensitivity measurement. Measuring the response of the circuit at different signal levels using a sinusoidal input is somewhat pessimistic, because the circuit behaviour also depends upon the rate of change of the input signal. Therefore it is reasonable to expect that the sensitivity of the circuit to

Figure 4.27: Testchip input signals and output response at fclk = 2.5 GHz.

Figure 4.28 : HSPICE simulation of the flip-flop for a sinewave data input at $f_{clk} = 2.5$ GHz.

Figure 4.29: Testchip input signals and output response at fclk = 5.0 GHz.

Figure 4.30 : HSPICE simulation of the flip-flop for a sine wave data input at $f_{clk} = 4.0$ GHz.

the pulses in a real bit stream will be better than the measured data for a sinusoidal input listed in Table 4.3.

Plots of the clock input, D-input, and testchip output signals are shown in Figures 4.27 and 4.29 for clock frequencies of 2.5 and 5 GHz. These experimental measurements can be compared with the plots obtained from HSPICE circuit simulations in Figures 4.28 and 4.30. The response to sinusoidal input signals is shown at clock frequencies of 2.5 and 4 GHz. The agreement between the circuit simulations and experimental results is excellent, although the maximum clock frequency measured in the laboratory is about 20% higher than that predicted by circuit simulation. This is consistent with experimental measurements of ECL gate propagation delay from circuits fabricated on the same wafer.

4.4 Summary

A binary quantizing phase detector consisting of serially connected ECL latching comparators has been proposed in this chapter. Simulations of the circuit behaviour using the HSPICE simulator have shown that the phase relationship between a 1 Gbit/s non-return-to-zero coded data stream and a 1 GHz timing clock can be consistently measured by the phase detector circuit and the clock/data phase error can be quantized to a single bit. The phase error quantization is encoded into two bit streams at the lead and lag outputs of the circuit, and the pulses generated by the phase detector are well-defined. Very little glitching is predicted, even at small phase errors between transitions in the clock and data signals. Some additional pulse conditioning may be required in order to properly interface the phase detector to a digital filter circuit. The effects of voltage offsets and device noise have also not been considered here, although these factors will introduce some degradation in the accuracy of the phase measurement. These effects should be studied within the context of the overall PLL design.

The accuracy of the phase measurement has been shown to be related to the slew rate of the clock and data input signals. Feedthrough of the clock signal appears to adversely affect the measurement accuracy. The effects of clock feedthrough can be reduced by increasing the signal amplitude for a given signal rise-time or fall-time. A minimum differential input signal amplitude of 200 mVolts p-p is required at the clock inputs to ensure proper circuit operation. For input signals with 200 ps rise and fall-times (which could be easily realized

on-chip), a data input amplitude of approximately 300 mVolts p-p (differential mode) is recommended.

The maximum clock rate for the phase detector was determined to be 2.4 GHz in simulation. High clocking speed was achieved through a design method based describing the propagation delay time of a basic ECL inverter gate using sensitivity analysis. The circuit components which optimized the gate performance were calculated using the resulting delay equation. The predictions of the delay equation were verified using the HSPICE circuit simulator. An expression of the circuit propagation delay as a sum of circuit time constants should also apply more generally to a class of pulse driven circuits consisting of cascoded differential amplifiers, such as ECL. The extension of this design method to more complex ECL circuits is an area for further investigation.

A high-speed master/slave D-type flip-flop has been designed which has demonstrated the multi-GHz signal processing capability of the bipolar devices fabricated in a BiCMOS process. The predictions made by computer simulation have been verified by experimental measurements, and it is encouraging to see such close agreement. The circuit performed better than predicted by the circuit simulator, indicating that the devices currently being fabricated exceed the performance predicted by the nominal device models. This has also been verified by high frequency measurements of individual transistors.

The performance of the circuit is limited by the bandwidth of the output buffer circuit, which reduces the amplitude of the output signal at higher clock rates. An alternating 1-0 data pattern applied to the flip-flop D-input was synchronized up to a maximum clock rate of 5.3 GHz, but full logic swing at the output was not achieved at that frequency. Computer simulations have shown that the maximum operating frequency of the circuit for a pseudorandom data input is also limited by the bandwidth of the output buffer circuit, which is consistent with the experimental observations.

5. Monolithic Microwave Components

An oscillator which is capable of generating a sinusoidal or quasi-sinusoidal output signal at microwave frequencies is most often realized using a linear feedback network. A block diagram of such a linear oscillator is shown in Figure 5.1, where the oscillator is modelled as an amplifier which is connected to a frequency determining network in a positive feedback loop. Oscillation of the circuit can be initiated by a small amount of noise at the circuit input (modelled as the source kT in the block diagram), and the output signal will increase in amplitude until it is limited by some non-linearity in the signal path or by an automatic gain control (AGC) mechanism. Although the oscillator is called "linear", the signal amplitude is usually constrained by the saturation limit of the amplifier in simple oscillator circuits which do not use AGC. The feedback network can be assumed to be linear, however, and the oscillation frequency (f_c) is determined by the frequency selective characteristics of the feedback network. A passive resonant circuit consisting of an inductor and capacitor could be used to implement the feedback network although other types of high frequency filters, such as surface-acoustic wave (SAW) and dielectric resonator filters, are often used in high-quality oscillators designed for microwave signal generation. Unfortunately, the SAW and other types of high quality passive microwave filters are incompatible with monolithic silicon IC technology.

Figure 5.1 : Block diagram of a linear microwave oscillator

The linear microwave oscillator circuit has not been considered practical for monolithic implementation in silicon because passive inductors of sufficient quality are difficult to realize as on-chip components. However, inductors which are useful at microwave frequencies and which are compatible with planar fabrication technology can be designed using coupled microstrip transmission lines. This design approach will be discussed in this chapter, and the measured performance of two inductor designs which have been fabricated in the BiCMOS process will be presented. Also, the performance of a high frequency amplifier has been designed as a demonstration of the capability of BiCMOS technology in a linear circuit application at microwave frequencies will be discussed. The actual design of a linear oscillator is not the objective of this work. However, the design information and experimental results that are presented for the microstrip inductors and the broadband amplifier will provide a basis for further design work in this area.

5.1 Microstrip Inductors

For microwave circuit applications, passive inductors which are compatible with planar fabrication technology have been fabricated using various dielectric materials (e.g., Alumina, Quartz, GaAs, etc.). Some early work was reported in the mid 1960's [38] on the characterization of silicon as a substrate material for microwave transmission lines, but it was found that high resistivity substrates were required in order to minimize the losses at high frequencies caused by finite conductivity of the material.

A figure-of-merit often quoted for passive inductors is the quality factor or Q . It is defined as the ratio of the energy stored to the energy dissipated per cycle for sinusoidal excitation. A simple low frequency equivalent circuit of the discrete component inductor models the losses as a resistor in series with an ideal inductance. Therefore for low frequency sinusoidal input signals, the Q -factor indicates the relative size of the inductive reactance and series resistance of the component :

$$Q = \frac{\omega L}{r_s} \quad (5.1)$$

High quality inductors have $r_s \ll \omega L$ over the useable frequency range for the component.

Recently, it has been reported that inductors have been successfully fabricated in a production IC technology using low-resistivity silicon substrates [39]. The Q-factor of these monolithic inductors was reported to be about 5 in the low GHz frequency range. The component Q was reported to be limited by metal and contact resistance with little effect from the conductive substrate.

The inductors which were fabricated are similar to the designs reported by Nguyen in [39] in order to have a basis for performance comparison between the BiCMOS process and another silicon technology. The purpose of this investigation was to examine the design procedure and to measure the electrical characteristics of the inductor. This will establish whether or not it is feasible to consider designing a monolithic circuit using these inductors in a BiCMOS process. Also, the theory underlying the operation of the inductor will be reviewed, because a theoretical understanding of the device can indicate areas where the performance of the inductor might be improved.

The planar structure which has been used by microwave circuit designers, consists of a microwave transmission line which can be wrapped in either a circular or rectangular spiral configuration. The dimensions of the structure can be reduced by using a transmission line with a high characteristic impedance, because a narrower conductor linewidth is required to fabricate such a structure. The number of turns in the spiral can be increased if the transmission line width is reduced, which increases the magnitude of the inductance that can be realized within a given layout area.

The transmission properties of a microstrip line which can be fabricated in a modern silicon IC technology is of fundamental importance to the performance of these inductors. Therefore these properties will be examined further.

5.1.1 Microstrip Transmission Lines

The microstrip line is used extensively in hybrid and monolithic microwave circuits because it can be fabricated using planar processing technology and it can be easily connected to other active and passive devices. The physical geometry of the microstrip line is shown in Figure 5.2. The electrical behaviour of the line is determined by the top conductor width (a), the metal thickness (t), the substrate thickness (b) and the properties of the dielectric substrate material. The transmission line can be viewed as a distorted coaxial transmission

line where the top conducting microstrip corresponds to the centre conductor and the outer shield of the coaxial line is transformed to a flat ground plane. A portion of the electric field (E) is in the dielectric and a few fringe electric field lines travel through the air and dielectric. The orientation of the magnetic field intensity (H) is also shown on the drawing.

Figure 5.2 : Microstrip line geometry.

If the loss due to finite conductivity and polarization of the dielectric material is very low, then the transmission mode for an electromagnetic wave is characterized as quasi-transverse electromagnetic, or quasi-TEM [40]. A quasi-TEM mode wave has some small field components in the direction of propagation, but these components are negligible compared to the TEM fields at lower microwave frequencies (typically < 10 GHz).

Silicon dioxide (SiO_2) is an excellent insulator which exhibits very low losses due to dielectric polarization effects. A microstrip line could be fabricated in an IC process which consisted of two metal conducting layers separated by a dielectric layer of pure SiO_2 . Losses due to the conductive silicon substrate would not be a factor if this structure were used, because the substrate functions only as a mechanical support for the microstrip line. Unfortunately, the dielectric thickness between metal layers is only a few micrometers. The width of the top conductor must be less than approximately $5\text{ }\mu\text{m}$ if a characteristic impedance of $50\text{ }\Omega$ is desired. A larger characteristic impedance (Z_0), which is usually used for microstrip inductor designs, would require an even narrower top conductor width. As the length of the transmission line increases, the d.c. resistance of the metal line becomes very large for such narrow linewidths in a typical integrated circuit fabrication process, because the metallization thickness is often less than $2\text{ }\mu\text{m}$. Therefore in order to reduce the d.c. resistance of the inductor and obtain an acceptable inductor Q-factor, both

the top metal width and the dielectric thickness should be increased. The spacing between the conducting strip and the ground plane can only be increased by moving the ground plane toward the bottom of the semiconductor substrate. If the resistivity of the semiconductor material is large (e.g., semi-insulating GaAs) then the behaviour of the microstrip line will not be seriously affected. However, low resistivity substrates are preferred in silicon processing for ease of device fabrication. The conductive silicon (Si) layer has a significant impact on the electrical behaviour of the microstrip transmission line.

Figure 5.3 : A microstrip line in the SiO_2 -Si system.

A microstrip line consisting of a multi-layered SiO_2 -Si structure is shown in Figure 5.3. Exact theoretical analysis of the wave propagation along this structure is complicated by the microstrip geometry and the finite conductivity of the substrate. Hasegawa [41] used a rectangular waveguide approximation in order to simplify the solution of this problem. The width of the conducting strip ('a' in Figure 5.3) is assumed to be comparable to the total substrate thickness and the effects of fringing at the edges of the top conductor are completely neglected. Three fundamental forms for the lowest order mode of propagation were predicted theoretically and verified by experimental measurements. These different modes arise from the different behaviour of the substrate when its resistivity and frequency are varied.

For a silicon dielectric, the losses due to polarization damping are small and the loss is mainly due to the conduction current in the silicon substrate. The ratio of the conduction

current and displacement current densities is defined as the loss tangent of the material, which for this case can be expressed as

$$\text{loss tangent} = \tan \delta = \frac{1}{\rho \omega \epsilon'} \quad (5.2)$$

where

ρ is the substrate resistivity, in $\Omega\cdot\text{m}$

ω is the frequency of the propagating wave, in radians/s

ϵ' is the real part of the dielectric constant, in F/m

The product $\rho\omega$ is of importance in defining the various propagating modes in the SiO_2 -Si filled rectangular waveguide. When the $\rho\omega$ product is such that the loss tangent is small, the fundamental propagating mode is a quasi-TEM mode wave because the effects of the finite substrate conductivity are negligible. At very high frequencies, where the guided wavelength approaches the thickness of the double layer (i.e., wavelength approaches $b_1 + b_2$) then the TEM approximation becomes invalid and the transmission line becomes dispersive.

In addition to this "dielectric" mode, there is also a "metallic" mode which can exist when the $\rho\omega$ product is small, so that the skin depth in the silicon substrate is small. The substrate then behaves like a lossy conducting boundary and there is significant dispersion of the propagating wave due to the skin effect in the imperfect silicon ground plane.

Neither of these limiting cases are applicable to the range of frequency and substrate resistivity that is of interest to the RF circuit designer using a production IC process. However, a third propagating mode can exist when the substrate resistivity is moderate (i.e., resistivity between 0.1 and 1 $\Omega\cdot\text{cm}$). In this case a slow surface wave can propagate along the microstrip line at excitation frequencies below approximately 1 GHz. This "slow-wave" mode is not severely attenuated by the finite conductivity of the substrate, but there is a significant dispersion of the propagating signal.

Hasegawa's analysis of the rectangular waveguide model for the SiO_2 -Si system defined the following (approximate) frequency ranges for two of the fundamental propagating modes:

Slow-wave mode	$f < 0.3f_0$
Dielectric (quasi-TEM) mode	$f > 1.5f_0$

where f_0 is the characteristic frequency of the slow-wave mode and f_c is the dielectric relaxation frequency of the silicon layer. For the BiCMOS process, the dielectric layers of the microstrip line have the following parameters:

b_1	$= 5 \mu\text{m}$	thickness of the SiO_2 layer
b_2	$= 500 \mu\text{m}$	thickness of Si layer
ϵ_{SiO_2}	$= 3.9$	relative dielectric constant for SiO_2
ϵ_{Si}	$= 11.7$	relative dielectric constant for Si
ρ_{Si}	$= 15 \Omega\text{-cm}$	resistivity of the unprocessed silicon wafers

It can be shown that for this set of parameters, the metallic or skin effect mode will not propagate in the rectangular waveguide model. The rectangular waveguide analysis is valid provided that

$$\epsilon_{\text{Si}} b_1 \ll \epsilon_{\text{SiO}_2} b_2$$

which is satisfied for the BiCMOS process parameters previously given.

The characteristic frequency for the slow-wave mode, f_0 , is given by the following equation [41]:

$$\begin{aligned}
 f_0 &\approx \frac{1}{2\pi \frac{\rho_{\text{Si}} \epsilon_0 \epsilon_{\text{SiO}_2} b_2}{b_1}} & (5.3) \\
 &= \frac{1}{2\pi \frac{0.15 (8.85 \times 10^{-12}) (3.9) (500)}{5}} \approx 307 \text{ MHz}
 \end{aligned}$$

assuming that the permittivity of free space (ϵ_0) is 8.85×10^{-12} F/m. The slow-wave mode will dominate for frequencies less than approximately one-third of f_0 , or

$$f_{sw} < 92.3 \text{ MHz} \quad (\text{slow-wave regime})$$

The frequency limit for the quasi-TEM mode can be determined from the following equation for the relaxation frequency of silicon (f_c), which is given by [41]

$$\begin{aligned} f_c &= \frac{1}{2\pi (\rho_{Si} \epsilon_0 \epsilon_{Si})} \\ &= \frac{1}{2\pi (0.15) (8.85 \times 10^{-12}) (11.7)} = 10.2 \text{ GHz} \end{aligned} \quad (5.4)$$

The propagating mode can be characterized as a quasi-TEM wave for frequencies greater than $1.5(f_c)$ or 15.4 GHz.

Between the two frequency limits for the slow-wave and quasi-TEM modes there is a transition region (f_t) defined by the range:

$$0.3f_0 < f_t < 1.5f_c$$

or

$$92.3 \text{ MHz} < f_t < 15.4 \text{ GHz}$$

for the BiCMOS process.

Within this frequency range the propagating wave will exhibit characteristics of both the slow-wave and quasi-TEM modes, because there is a continuous transition between these two mode regimes. Therefore in the low GHz region, the propagating signal will undergo less attenuation than a quasi-TEM wave and there will be less dispersion of the propagating signal than for a pure slow-wave mode. The dispersion characteristics of the transmission line will determine the signal bandwidth which can be transmitted.

The BiCMOS fabrication process places some additional restrictions on the structure and composition of the microstrip line. Consequently, some of the assumptions made in the rectangular waveguide analysis of the Si-SiO₂ transmission medium should be reviewed.

The impurity concentration in the silicon substrate after processing, which was assumed constant, varies with distance from the dielectric interface. Within a few micrometers of the interface between the silicon and silicon-dioxide the substrate resistivity is much lower than $15 \Omega\text{-cm}$, because the concentration of dopant in this region must be large in order to facilitate device fabrication. These steps in the fabrication process cannot be eliminated without adding extra photomasking steps and adding to the cost of circuit processing. Also, the metal layer on the bottom surface of the silicon wafer is not used to contact the substrate. The substrate contact is made at the top surface of the silicon wafer in the BiCMOS process and therefore the ground plane is not clearly defined. Because the precise position of the ground plane is unknown, the thickness of the silicon layer which should be used in the analysis (b_2 in Figure 5.3) is unclear. The assumption of a wide top metal conducting strip in order to neglect fringing fields is really not valid in general, because the conductor width is generally not comparable to the combined thickness of the dielectric layers. The effect of these modifications on the results of the rectangular waveguide analysis is unclear. Therefore further investigation of the transmission properties of a microstrip line fabricated in a production IC process is required.

5.1.2 Microstrip Inductor Design

Two planar rectangular microstrip inductors have been designed and fabricated in the BiCMOS process: a 1.8 nH inductor and a 10 nH inductor. Both of these inductor designs have been configured connected for one-port RF characterization. The linear microwave CAD tool, Touchstone [42], was used to optimize the inductor designs. This program can simulate the electrical performance of a rectangular spiral inductor for a given substrate material and inductor layout, using the design algorithm proposed by Greenhouse [43]. This algorithm assumes that the dielectric material is homogeneous in order to simplify the problem and perform a two-dimensional analysis. It should be noted that the complete analysis of a microstrip inductor with a multi-layer dielectric is really a three dimensional problem, and consequently the behaviour predicted by Touchstone (and other microwave CAD tools such as SuperCompact) will not be completely accurate.

The following parameters are required by Touchstone in order to define the characteristic of the substrate material and the microstrip conductor:

$$\epsilon_r \quad \text{relative permittivity} \quad = 11.7$$

necessary for a linear oscillator design. A simple RF amplifier which has been designed and fabricated as an analog performance benchmark for the BiCMOS process will be described in the next section of this chapter.

5.2 Broadband Amplifier

A broadband negative feedback amplifier has been designed in order to study and demonstrate the capability of the BiCMOS process in an analog circuit application. Broadband amplifiers are a fundamental building block in RF wireless and fibre-optic communications systems where signal amplification is required. The addition of passive filtering at the input or output can be used to modify the frequency response of a broadband amplifier for frequency selective applications such as the linear oscillator.

5.2.1 Broadband Amplifier Design

An amplifier is less sensitive to transistor parameter variations when negative feedback is applied. This is important in monolithic circuit implementations where the trimming of component parameters in order to adjust the circuit performance is difficult and costly. Also, negative feedback reduces an amplifier's non-linear distortion products such as intermodulation distortion.

Negative feedback implies that a portion of the output signal is subtracted from the input. When positive feedback is used, the gain of a circuit increases because the feedback tends to increase the signal at the input. Positive feedback is often used as a method of modifying the high frequency response of an amplifier or in design of oscillator circuits.

The noise figure (NF) is often used as a figure-of-merit for high frequency amplifier designs. The noise figure is defined as the ratio of the available signal-to-noise power at the input to the signal-to-noise power ratio at the output

$$NF = \frac{(S/N)_{input}}{(S/N)_{output}} \geq 1 \quad (5.10)$$

Usually, the noise figure of an amplifier increases when feedback is used, unless the feedback elements are lossless. Transformers have often been used in low-noise or high

a) Spiral inductor layout

b) Lumped equivalent circuit

Figure 5.4 : Inductor layout and lumped equivalent circuit.

parameter format in order to conveniently compare the predictions of a computer simulation and the network analyzer measurements.

The Smith's chart shows contours of constant resistance and constant reactance [44]. The impedance represented on the chart could be either an input or a load impedance. The Smith's chart was originally devised as an aid in the solution of transmission line problems which involve the manipulation of complex numbers and it has become the customary format for display of reflection coefficients such as the scattering parameters S_{11} and S_{22} . The contours on the chart are derived from the basic equation for the reflection coefficient (Γ) of a transmission line

$$\Gamma = \frac{z - 1}{z + 1} \quad (5.5)$$

where z is the load or input impedance normalized to the system characteristic impedance, Z_0 . For a normalized impedance with real component, r , and imaginary component, x ,

$$z = r + jx \quad (5.6)$$

the real (Γ_r) and imaginary (Γ_i) components of the reflection coefficient are

$$\left(\Gamma_r - \frac{r}{1+r}\right)^2 + \Gamma_i^2 = \left(\frac{1}{1+r}\right)^2 \quad (5.7)$$

Equation 5.7 describes a family of circles where each circle is associated with a specific value of resistance, r . The radius of the circles is specified by the right-hand side of equation 5.7 and the origin of the circles is given by

$$\Gamma_r = \frac{r}{r+1}, \quad \Gamma_i = 0 \quad (5.8)$$

(coordinates of the origin for circles of constant resistance)

which defines a point on the real axis. Some examples of constant resistance circles are shown in Figure 5.5. The radius of a constant resistance circle corresponding to $r = 0$ is unity and it is centered at the origin of the chart. As the resistance increases, the constant resistance circles on the chart decrease in radius and the origin shifts towards the right-hand

side of the Smith's chart. In the limit as the resistance approaches infinity, the circular contour shrinks to a single point on the real axis at the rightmost edge of the chart.

Figure 5.5 : Contours of constant resistance from a Smith's chart.

For an inductive reactance

$$z = j\omega L$$

where L is the normalized inductance, the reflection coefficient defined by equation 5.5 will have a magnitude of unity and the phase angle will vary over the range from 0 to 180 degrees. The resistance, r , is zero and therefore the reflection coefficient corresponding to a purely inductive reactance traces a semi-circular contour on the Smith's chart. The contour ranges from the point $r = 0$ at the left-hand side of the chart at frequencies close to d.c., towards the right-hand side of the chart as the frequency, ω , approaches infinity. The locus a - a' shown in Figure 5.5 is an example of the reflection coefficient for an ideal inductor when the measurement frequency is swept from d.c. to some frequency f_m . For constant values of resistance other than zero (i.e., $z = r + j\omega L$) the reflection coefficient will follow a similar semi-circular contour within the upper portion of the Smith's chart as the frequency varies. The locus b - b' illustrates the the reflection coefficient of an ideal

inductance in series with a resistor, which models the low frequency loss of the component, where parasitic capacitances can be neglected. Again, a circular contour is traced by the change in reflection coefficient with frequency. The origin and radius of the contour are given by equations 5.7 and 5.8 .

The characteristics of the inductor alone are required in order to accurately investigate and model the component behaviour for use in an integrated circuit. Unfortunately, a significant parasitic capacitance is introduced by the interconnect wiring and the bond-pads. The impedance of the bond-pad and wiring parasitics is a complex combination of capacitance and resistance because of the conductive substrate, and it cannot be accounted for in the network analyzer calibration procedure. However, this parasitic impedance appears in parallel with the impedance of the inductor and it is possible to measure the effects of the bond-pad and interconnect wiring alone, and then subtract them from the measurements made for the entire test circuit. This technique of de-embedding the device under test from the layout and interconnect parasitics is called the ISS calibration and subtract y-parameters (ISS-Y) method [45]. The following steps were followed in the application of this correction procedure:

1. The network analyzer (including the wafer probing apparatus) was calibrated at the measurement probe tips using a set of commercially available impedance standards. The impedance standards substrate (ISS) has a sets of calibration standards (i.e., open and short circuit, 50 Ohm load and a through connection) which matches the physical configuration of the wafer probes used to connect the network analyzer to the test circuit.
2. On-wafer s-parameter measurements were made on the inductor test circuits. These measurements include the parasitics of the bond-pads and interconnect wiring.
3. A set of s-parameter measurements was then taken on a similar set of bond-pads and interconnect. The inductor was disconnected from this test layout.
4. The s-parameters measured in steps two and three were then converted to y-parameters, and the y-parameters representing the admittance of the bond-pads and interconnect wiring was subtracted from the y-parameters corresponding to

the original device measurements. This operation removes the effects of the parasitics from the device measurements, and therefore the resulting set of parameters represent the characteristics of the inductor alone. These y-parameters were then converted back to s-parameters and plotted on a Smith's chart.

Unfortunately space restrictions limited the test structure layouts to one-port designs. It can be seen from the inductor lumped equivalent circuit shown in Figure 5.4 (b) that one-half of the shunt parasitic capacitance is short-circuited to ground when a single or one-port measurement configuration is used. However, an approximate circuit model of the inductor can be derived from the one-port measurements, and the performance of floating inductor connections can be investigated through the use of a circuit simulator in conjunction with the inductor equivalent circuit.

Plots of the measured reflection coefficient for both the 1.8 and 10 nH inductors are shown in Figure 5.6 along with the behaviour predicted by the microstrip inductor model in Touchstone. The frequency of the source was swept over the range from 10 MHz to 3 GHz for each curve plotted in the Figure. The source power of the network analyzer was varied over the range from -40 to 0 dBm, but a change in the measured data due to applied signal levels was not observed. A source power of 0 dBm was used to obtain the measurements shown in Figure 5.6. The effects of the bond-pad and interconnect parasitics were removed from the measurements using the ISS-Y procedure described previously and the corrected data have been plotted on the Smith's chart in Figure 5.6.

Self-resonance of the inductors was not observed over the frequency range used in these measurements because of the limits on the source frequency of the HP-8753B network analyzer. However, subsequent measurements of the large (10 nH) inductor on an HP-8510B network analyzer showed that the inductor was self-resonant at approximately 8 GHz which is close to the predicted value of 8.3 GHz listed in Table 5.1. The measured data for both inductor designs follows an almost circular contour on the Smith's chart over the frequency range of the measurement. This indicates that losses due to the conductive effects of the silicon substrate are negligible in this frequency range.

The measured d.c. resistance of the 1.8 nH inductor is significantly greater than the predicted d.c. resistance (a difference of 1.8 Ohms). This error can be attributed to losses

Figure 5.6 : Measured and predicted reflection coefficient (S_{11}) for two microstrip inductors fabricated in the BiCMOS process.

in a section of interconnect wiring which was not be included in the ISS-Y correction procedure because this interconnect was not accounted for in the computer simulations. The measured d.c. resistance of the 10 nH inductor was also affected by a systematic error introduced by the interconnect wiring, and the measured d.c. resistance of the large inductor is 1.3 Ohms greater than the resistance predicted by the simulator. The slight difference between these two measurement errors can be attributed to the slightly different layout geometry of the two inductor designs

It can be seen on the Smith's chart of Figure 5.6 that the measured data at 3 GHz (the endpoint of the frequency sweep) does not coincide with the endpoint of the contour corresponding to the computer simulation of the inductor. This occurs because the measured inductance of both coils is greater than the inductance predicted by computer simulation. This error is also partly due to the interconnect wiring which was unaccounted for in the measurement correction procedure. Additional sources of error in the experimental measurements are caused by imperfect calibration of the test equipment and errors introduced by the correction for the bond-pad and interconnect capacitances. However, the measured data shown is representative of 10 samples tested for each inductance value and there was little variation noted between the measured samples. The assumption of a single dielectric layer also contributes some error to the prediction of the RF performance and the inductance value. Therefore the accuracy of the computer simulations could be improved by accounting for the effects of the multi-layer dielectric on the component behaviour.

The parameters of the lumped equivalent circuit for the inductor shown in Figure 5.4 (b) have been extracted from the measured data for the 10 nH inductor. The effects of coupling capacitance between metal segments caused by fringing of the electric field can be ignored at lower frequencies because the dielectric constant of silicon dioxide is reasonably large (which tends to reduce fringing), the conductors are widely spaced, and the frequency range of interest is well below the self-resonant frequency of the inductor (i.e., a frequency range from 0.1 to 3 GHz). Therefore the capacitance which models this effect (C_0 in Figure 5.4) will be neglected. The losses introduced by the finite resistance of the top conductor metallization is modelled by resistor r_s in the lumped equivalent model shown in Figure 5.4 (b), and the self and mutual inductance of the coil is modelled as the lumped inductance, L . These two parameters can be easily determined from measurements of the

d.c. resistance and the inductance at low frequency where the effects of shunt capacitance (given by capacitor C_p in the model) can be ignored.

The structure of the spiral inductor is asymmetric and therefore the two shunt capacitors in the model are really not equal. However, the difference between these two values is small [46] and for the purposes of this study the two capacitances will be assumed to be identical. An estimate of the shunt capacitance can be made from consideration of the microstrip transmission line models for the Si-SiO₂ system proposed by Hasegawa [41] which are illustrated in Figure 5.7. Capacitance C_d , which appears in the model for both the slow-wave and quasi-TEM modes, is given by the parallel plate capacitance per unit length of the silicon dioxide layer. Similarly, the shunt capacitance C_{Si} in the model proposed for the quasi-TEM mode is the parallel plate capacitance per unit length of the silicon layer between the dielectric interface and the back metallization of the substrate. The length of the top conductor of the 10 nH inductor is 3.8 mm, and the corresponding values of the shunt capacitances for this inductor are given as follows

$$C_d = 170 \text{ fF}$$

$$C_{Si} = 51 \text{ fF}$$

Figure 5.7 : Microstrip transmission line equivalent circuits [41].

It was shown in section 5.1.1 of this chapter that over the range of frequency from approximately 100 MHz to 15 GHz the mode of propagation predicted by the rectangular

waveguide analysis is a hybrid of both the slow-wave and quasi-TEM modes. However, at frequencies up to few GHz the effect of the shunt capacitance in the quasi-TEM model (C_{sj} in Figure 5.7-b) will be small and the slow-wave mode model of the transmission line can be used. Also, if the wavelength of the applied signal is much smaller than the length of the transmission line (which in this case implies an applied frequency $\ll 38$ GHz), then the lumped equivalent circuit can be approximated by two sections of the transmission line model. The shunt capacitances in the lumped equivalent model for the 10 nH inductor are given by

$$C_p = \frac{C_d}{2} = 85 \text{ fF}$$

The dissipative component of the shunt capacitance is modelled by the resistance, r_d , in Figure 5.7 which represents the effect of the finite substrate resistivity. This is difficult to estimate for a microstrip transmission line fabricated in the BiCMOS process because the substrate contact is made at the top surface of the wafer, which complicates the geometry of the problem, and also because the resistivity of the silicon material varies as a function of distance from the dielectric interface. The dissipation resistance in the inductor model (r_p in Figure 5.4) can also be estimated from the self resonant frequency (ω_R) of the inductor. The dissipation and the other parameters of the model are related to the self-resonant frequency by the following equation [39]

$$r_p = \sqrt{\frac{L}{C_p} - \frac{1}{LC_p\omega_R^2} \left[\frac{L}{C_p} - r_s^2 \right]} \quad (5.9)$$

since the other parameters are known. Note that the capacitance C_p in equation 5.9 refers to the shunt capacitance in the lumped equivalent model of the inductor. For the measured self-resonant frequency of 7.9 GHz and using the other measured and calculated model parameters, the dissipation resistance r_p that is calculated from equation 5.9 is 270 Ohms.

The parameters of the lumped equivalent circuit model for the 10 nH inductor fabricated in the BiCMOS process and the parameters extracted for a similar inductor designed by Nguyen (referred to as the UCB inductor) at the University of California [39] are compared in Table 5.2. The inductor geometries are identical, however, the parameters of the substrate are different because the UCB inductor was fabricated by Signetics Corporation

using their HS3 silicon process. Aluminium top metallization was also used to fabricate the UCB inductor, however, the metal thickness for the HS3 process is $1.8\text{ }\mu\text{m}$ over a $1.7\text{ }\mu\text{m}$ thick layer of oxide compared to a metal thickness of $1\text{ }\mu\text{m}$ over a $5\text{ }\mu\text{m}$ thick oxide layer for the BiCMOS process. This accounts for the differences in the series resistance and shunt capacitances in the lumped element model as listed in Table 5.2. The substrate thickness is identical for both inductors, and the undoped substrate resistivity for the UCB inductor is $14\text{ }\Omega\text{-cm}$, which is virtually identical to the $15\text{ }\Omega\text{-cm}$ specified for the BiCMOS process. As shown in the Table, the self-resonant frequency of the inductor fabricated in the BiCMOS process is significantly higher than for the UCB inductor, which accounts for the large difference in the shunt dissipation, r_p , for the two coils. The main factor in the improved performance of the BiCMOS inductor is the thicker oxide layer, which leads to a much lower value of shunt capacitance in the lumped equivalent model. However, the Q-factor of the UCB inductor at 900 MHz is slightly larger than the Q-factor of the BiCMOS inductor, which is mainly due to the thicker top metal available in the HS3 process and the resulting lower d.c. losses.

Table 5.2 : Inductor model parameters.

Parameter	BiCMOS inductor	UCB inductor [39]
D.C. resistance, r_s	$22.8\text{ }\Omega$	$15.4\text{ }\Omega$
Inductance, L	11.1 nH	9.7 nH
Shunt capacitance, C_p	85 fF	590 fF
Shunt dissipation, r_p	$270\text{ }\Omega$	$70\text{ }\Omega$
Q-factor at 900 MHz	2.8	3.0
Self-resonant frequency	7.9 GHz	2.5 GHz

A photomicrograph of the two inductors fabricated in the BiCMOS process is shown in Figure 5.8. The 10 nH design is the large rectangular spiral of top metal on the left side of the photo. The broadband amplifier described in section 5.2 of this chapter is shown in the centre of the photograph, and the 1.8 nH microstrip inductor appears at the right side of the photo.

The reflection coefficient or S_{11} of the UCB and BiCMOS 10 nH inductors predicted by the lumped equivalent models can be compared in Figure 5.9. The reflection coefficient of

the BiCMOS design follows a contour on the Smith's chart which is closer to the ideal inductor behaviour than the UCB inductor. This is a result of the lower parasitic capacitance in the BiCMOS process compared to the Signetics HS3 process, which increases the self-resonant frequency of the inductor design. The frequency range over which the BiCMOS inductor can be used in an actual circuit design is much greater than the UCB inductor because of the larger self-resonant frequency.

Figure 5.8 : Photomicrograph of the microstrip inductor/broadband amplifier circuits.

The measured data for the 10 nH BiCMOS inductor is also plotted on the Smith's chart. A simple lumped element model predicts the behaviour of the inductor well at lower frequencies but it is inadequate for accurate design at frequencies above approximately 1 GHz. The model accuracy could be improved if a number of transmission line sections were used to characterize the behaviour of the microstrip inductor, because a multi-section transmission line model reflects the behaviour of this structure more accurately than a lumped element equivalent circuit. The electrical equivalent circuit for the slow-wave mode could be used as the model for each transmission line section, and the modelling accuracy required for a given design could be achieved by choosing the appropriate number of sections used in the complete equivalent circuit. Although a more complex model is required to describe the high frequency behaviour of the inductor, the accuracy for RF circuit design would be improved and a trade-off could be made between the model complexity and the time required to simulate a larger number of circuit elements, if

Figure 5.9 : Comparison of UCB and BiCMOS microstrip inductors.

necessary. Computer optimization of the model parameters in order to fit the measured data could also be used in the development of an accurate inductor model, however, a large number of component measurements would be required as a basis for optimization in order to margin the circuit model for tolerances introduced by circuit processing.

5.1.4 Summary

The design and measured performance of two microstrip inductor designs has been presented. The results obtained for the inductors fabricated in the BiCMOS process have compared favorably with an identical layout published recently in the literature and the behaviour predicted by computer simulation. The RF characteristics of these inductors indicate that the losses involved are mainly due to the conduction losses in the top conductor metallization and that there is little impairment of the inductor performance due to the effects of the conductive substrate. It should also be noted that frequency dependent losses due to the skin effect do not seriously degrade the performance of these inductors at frequencies below approximately 3 GHz, because of the thin top conductor metallization.

However, the magnitude of the d.c. loss seriously degrades the Q-factor of these inductors, which is important for an actual circuit design. Therefore a significant improvement in the performance and utility of the silicon microstrip inductor could be realized if the top conductor resistance were lowered either by increasing the metal thickness, increasing the width of the top conductor or by using a combination of these two modifications. Increasing the thickness of the metal layer could not be achieved without modifying the existing fabrication process, which is not a viable option. Some improvement could be realized by decreasing the conductor spacing to the minimum spacing possible for the BiCMOS process and increasing the conductor width. Widening the top conductor would decrease the resistive losses of the top conductor if the total length of top metal was not significantly increased. The conductor spacing must also be reduced in order to limit the increase in the outer dimensions of the coil. Unfortunately, widening the top conductor metal would also increase the parasitic capacitance of the inductor thereby lowering the self-resonant frequency of the component. However, a decrease in the self-resonant frequency could be tolerated if the Q-factor of the inductor could be significantly improved.

Inductors are useful components in the development of a stable, passive feedback network for a monolithic VCO. An amplifier which has adequate power gain and bandwidth is also

necessary for a linear oscillator design. A simple RF amplifier which has been designed and fabricated as an analog performance benchmark for the BiCMOS process will be described in the next section of this chapter.

5.2 Broadband Amplifier

A broadband negative feedback amplifier has been designed in order to study and demonstrate the capability of the BiCMOS process in an analog circuit application. Broadband amplifiers are a fundamental building block in RF wireless and fibre-optic communications systems where signal amplification is required. The addition of passive filtering at the input or output can be used to modify the frequency response of a broadband amplifier for frequency selective applications such as the linear oscillator.

5.2.1 Broadband Amplifier Design

An amplifier is less sensitive to transistor parameter variations when negative feedback is applied. This is important in monolithic circuit implementations where the trimming of component parameters in order to adjust the circuit performance is difficult and costly. Also, negative feedback reduces an amplifier's non-linear distortion products such as intermodulation distortion.

Negative feedback implies that a portion of the output signal is subtracted from the input. When positive feedback is used, the gain of a circuit increases because the feedback tends to increase the signal at the input. Positive feedback is often used as a method of modifying the high frequency response of an amplifier or in design of oscillator circuits.

The noise figure (NF) is often used as a figure-of-merit for high frequency amplifier designs. The noise figure is defined as the ratio of the available signal-to-noise power at the input to the signal-to-noise power ratio at the output

$$NF = \frac{(S/N)_{input}}{(S/N)_{output}} \geq 1 \quad (5.10)$$

Usually, the noise figure of an amplifier increases when feedback is used, unless the feedback elements are lossless. Transformers have often been used in low-noise or high

power amplifier designs as a method of implementing a lossless feedback network. A monolithic transformer can be designed using two mutually coupled microstrip inductors, however, this technique will not be considered in this work. In this design, two types of negative feedback, called shunt and series feedback, will be used. Shunt and series feedback are alternatives to the use of transformers, and these feedback methods are widely used in the design of low frequency amplifiers. When series or current feedback is used the terminal impedances of the amplifier increase. A common example of series feedback is emitter degeneration. Shunt or voltage feedback tends to decrease terminal impedances, and resistive feedback from the collector-to-base of a single transistor amplifier stage is a common example of shunt feedback. The noise figure of an amplifier using shunt and/or series feedback will be considerably larger than for a true low-noise amplifier design which uses a transformer or some other form of lossless feedback, because resistors are used to implement the feedback networks.

Broadband amplifiers are often feedback amplifiers, because an increase in the circuit bandwidth can be easily realized by increasing the negative feedback to lower the amplifier gain (i.e., the gain-bandwidth product of the amplifier is constant). If the circuit design is kept simple so that parasitic elements are minimized, amplifier bandwidths close to the transition frequency (f_T) of the active devices can be achieved. If larger gains are required, this can be realized by cascading amplifier circuits.

Figure 5.10 : Broadband feedback amplifier.

The combination of series and shunt feedback shown in the schematic diagram of Figure 5.10 has been chosen, assuming that some degradation in amplifier noise figure is acceptable for this monolithic design. This circuit configuration uses two bipolar transistors connected in a Darlington configuration to obtain a large transconductance, and it offers the advantage of broadband gain with good matching of the input and output impedance to a 50 Ohm environment [47]. Large area devices would be required to achieve the desired transconductance if FET devices were used, which would result in poorer performance than this bipolar design. It should be noted that the bias network and the load and source impedances are not shown in Figure 5.10. A bias circuit (or Bias 'T') must be connected between the amplifier output and the load in order to properly bias transistors Q_1 and Q_2 .

The amplifier components will be chosen to meet specifications for low-frequency gain and the desired input and output impedances. In this case, the amplifier can be analyzed using a simplified low frequency model, which is shown in Figure 5.11. This equivalent circuit has been derived assuming that the Darlington pair behaves like an ideal voltage-dependent current source at low frequencies. The effect of the input bias resistor R_B has been ignored for the purposes of this analysis.

Figure 5.11 : Low frequency equivalent circuit of the feedback amplifier

If the input resistance of the amplifier at low frequency is assumed to be very large (i.e., $R_{in} \rightarrow \infty$ in Figure 5.11), the small-signal y-parameters of the circuit can be written as the following set of matrix equations:

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \cdot \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} G_F & -G_F \\ (g_m' - G_F) & G_F \end{bmatrix} \cdot \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \quad (5.11)$$

where the currents (i) and voltages (v) are defined in Figure 5.11, and G_F is the conductance of the feedback resistor, R_F . The effective transconductance parameter, g_m' , is given by

$$g_m' = \frac{g_m}{1 + g_m R_{E2}} \quad (5.12)$$

and the transconductance is reduced by the emitter degeneration, R_{E2} .

For matched input and output impedances, the s-parameters S_{11} and S_{22} must equal zero. The small-signal s-parameters can be computed from the small-signal y-parameters for the circuit, which are defined in equation 5.11. For the input reflection coefficient, S_{11} ,

$$S_{11} = (1 - y_{11}')/(1 + y_{22}') + y_{12}'y_{21}' = 0 \quad (5.13)$$

where the reflection coefficient must be zero if the input is properly matched to a transmission line. The y-parameters written in equation 5.13 are the small-signal y-parameters normalized to the characteristic impedance of the system, Z_0 . Substituting the y-parameters from equation 5.11, normalized to Z_0 , gives the following:

$$(1 - G_F Z_0)(1 + G_F Z_0) - (g_m' Z_0 - G_F Z_0) G_F Z_0 = 0 \quad (5.14)$$

and solving this equation for G_F gives

$$G_F = \frac{1}{g_m' Z_0^2}$$

or

$$R_F = g_m' Z_O^2 \quad (5.15)$$

A similar calculation can be performed assuming that the output impedance is matched to the system impedance (i.e., setting the output reflection coefficient, S_{22} , to zero), which gives an identical result.

The low frequency input and output impedances have been made equal to the system impedance and therefore

$$Z_{in} = Z_{out} = Z_O = \sqrt{R_F / g_m'} \quad (5.16)$$

The low frequency amplifier gain can be calculated from the definition of the forward transmission coefficient, S_{21} , written in terms of the normalized y-parameters of the network as

$$S_{21} = \frac{2 y_{21}'}{(1 + y_{11}')(1 + y_{22}') - y_{12}' y_{21}'} \quad (5.17)$$

Substitution of the y-parameters for the amplifier circuit normalized to the system impedance gives

$$S_{21} = -(Z_O g_m' - 1) \quad (5.18)$$

and replacing Z_O in equation 5.18 with the expression given in equation 5.16 gives the low frequency gain expression

$$\text{l.f. gain} = 1 - \sqrt{R_F / g_m'} \quad (5.19)$$

The desired specifications for the amplifier test circuit are:

low frequency gain	= 13 dB	
input and output impedances	= 50 Ω	($Z_o = 50 \Omega$)
D.C. collector voltage (Q_1 and Q_2)	= 4 Volts	

The transconductance of the Darlington pair is approximately equal to the transconductance of transistor Q_2 shown in Figure 5.10 [36]. Assuming an emitter current of 20 mA for transistor Q_2 (i.e., $I_{E2} = 20$ mA), the amplifier transconductance can be calculated from the following equation

$$g_m = \frac{I_{E2}}{26} = \frac{20}{26} = 0.77 \text{ S} \quad (5.20)$$

For a low frequency gain of 13 dB, the feedback resistor, R_F , and the emitter degeneration resistor, R_{E2} , can be calculated using equations 5.16 and 5.19 as

$$\text{l.f. gain} = 13 \text{ dB} = -4.47 = 1 - \sqrt{R_F g_m}$$

The sign of the gain must be negative because of the phase inversion between the input and output of the circuit at low frequencies. The feedback resistance can therefore be expressed in terms of the effective transconductance as

$$R_F = \frac{(5.47)^2}{g_m} \quad (5.21)$$

and from equation 5.16

$$g_m = \frac{R_F}{Z_o^2} = \frac{R_F}{(50)^2} \quad (5.22)$$

Substituting equation 5.22 into 5.21 gives

$$R_F = (5.47) (50) = 274 \Omega$$

and

$$g_m = \frac{274}{(50)^2} = 0.11$$

The emitter resistance, R_{E2} , can be calculated from equation 5.12, using g_m and g_m' ,

$$R_{E2} = \frac{1}{g_m} + \frac{1}{g_m'} = \frac{1}{0.11} + \frac{1}{0.77} = 10.4 \, \Omega$$

This is the total emitter degeneration resistance including the extrinsic emitter resistance of the bipolar transistor, Q_2 .

Bias resistors R_B and R_{E1} can be calculated by first assuming a base-emitter voltage drop (V_{BE}) of 0.85 V for the bipolar transistors and then writing equations for the voltage across the resistors as

$$V_{RE1} = I_{E2} R_{E2} + V_{BE2} = 0.02(10.4) + 0.85 = 1.06 \, \text{V} \quad (5.23)$$

$$V_{RB} = V_{RE1} + V_{BE1} = 1.06 + 0.85 = 1.91 \, \text{V} \quad (5.24)$$

Assuming an emitter current for Q_1 of 7 mA (i.e., $I_{E1} = 7 \, \text{mA}$), the resistor R_{E1} can be calculated using 5.23,

$$R_{E1} = \frac{V_{RE1}}{I_{E1}} = \frac{1.06}{0.007} = 150 \, \Omega$$

The bias current flowing through resistors R_F and R_B is sufficiently large to neglect the base current drawn by Q_1 . Therefore the voltage drop across R_B will be approximately equal to

$$V_{RB} = \frac{V_C \cdot R_B}{R_B + R_F} = \frac{4(R_B)}{R_B + 274}$$

and solving this equation for R_B using the base resistor voltage from equation 5.24 gives the result

$$R_B = 250 \, \Omega$$

The calculated resistor values for the broadband amplifier are summarized in Table 5.3. Due to tolerances in the pre-production BiCMOS fabrication process, some of the resistor values in the actual circuit were significantly higher than the design values. The actual resistor values were estimated from sheet resistance measurements of test structures fabricated on the same wafer as the broadband amplifier. These actual resistor values are also listed in Table 5.3. The emitter degeneration resistor was fabricated using a polysilicon layer with lower resistivity than for the other resistors, because of the small value required. Consequently the input and output impedance of the experimental amplifier were not 50 Ohms (the design target for the input and output impedances at low frequencies). Also, the low frequency gain of the amplifier was slightly affected by the change in feedback resistors. Therefore the amplifier performance predicted from circuit simulations, which is compared to the experimental measurements in the following section, was based upon the actual resistance values for the circuit given in Table 5.3.

Table 5.3 : Resistance values for the broadband amplifier.

Resistor	Design Value, in Ohms	Actual Value, in Ohms
R_F	274	290
R_{E1}	150	160
R_{E2}^*	9.0	9.5
R_B	250	270

*Note that the value of R_{E2} entered in the Table does not include the $1.4 \, \Omega$ extrinsic emitter resistance of the bipolar transistor.

5.2.2 Circuit Simulations and Experimental Results

The broadband amplifier circuit requires input and output coupling capacitors in order to isolate the bias circuitry from the signal path, as shown in Figure 5.12. D.C. bias current is supplied by a bias-T circuit, and the current-limiting resistor, R_{bias} , can be altered to accommodate a wide range of power supply voltages. The forward transmission

coefficient or s-parameter S_{21} of the circuit was measured using an HP-8753B network analyzer and companion s-parameter test set. The parameter S_{21} is equivalent to the gain of the amplifier when the test circuit is driven by a 50 Ohm source into a 50 Ohm load. The bias choke and decoupling capacitors shown in Figure 5.12 are an integral part of the s-parameter test set which simplifies the connections required to perform a measurement. A high frequency wafer probing apparatus which has a bandwidth greater than 26.5 GHz was used to connect the test circuit to the s-parameter test set. Therefore any degradation in the RF characteristics of the amplifier introduced by the circuit probing apparatus was assumed to be minimal.

Figure 5.12 : Amplifier bias configuration for experimental measurements.

Circuit simulations, using EESOF's Libra [42] harmonic balance simulator with the Gummel-Poon model for the bipolar transistor predicted a low frequency gain of 11.1 dB and a -3 dB bandwidth of 3.44 GHz assuming the actual resistor values from Table 5.3. The best-case device parameters were used for the simulations and the performance predicted by the circuit simulator agrees well with the measured results as shown in Figure 5.13. This is consistent with the experimental results for the master/slave flip-flop discussed in Chapter 4 of this thesis, where the simulated circuit performance using best-case device parameters gave the best agreement with the measured circuit performance. The measured and predicted circuit specifications are summarized in Table 5.4 along with the specifications from two commercially available amplifiers manufactured by Avantek and Hewlett-Packard [48, 49]. These commercial amplifiers are manufactured in pure bipolar

silicon technology (not BiCMOS) and both amplifier designs use Darlington connected transistors with compound feedback. The Avantek amplifier is an industry standard introduced in the early 1980's, while the Hewlett-Packard amplifier is fabricated in a newer technology and was introduced to the market in 1990. The performance of the feedback amplifier produced in the BiCMOS process compares favorably with the current state-of-the-art in pure bipolar silicon technology. A photomicrograph of the broadband amplifier fabricated in the BiCMOS process is shown in the centre of Figure 5.8, situated between the two microstrip spiral inductors.

Table 5.4 : Broadband amplifier specifications.

	Gain at 100 MHz	-3 dB bandwidth	1dB gain comp. point	Bias current	Power dissipation
Predicted BiCMOS*	11.1 dB	3.44 GHz	4.5 dBm	29.7 mA	119 mW
Measured BiCMOS	10.9 dB	3.77 GHz	3.8 dBm	30.5 mA	125 mW
Avantek MSA-0735	13.5 dB	2.4 GHz	5.5 dBm	22.0 mA	88 mW
HPMA-0435	8.8 dB	3.8 GHz	-	-	-

*Note : Best-case process and the actual resistance values from Table 5.3 were assumed for the simulations.

The input power level at the one dB gain compression point is also listed in Table 5.4. The one dB gain compression point (G_{1dB}) is a figure-of-merit which is often used to characterize the large-signal performance of power amplifiers. It is defined as the power gain of an amplifier where the non-linearities inherent in the circuit reduce the power gain by one dB, compared to the small-signal linear power gain. The gain compression point is often used to specify the power handling capabilities of active devices, and large signal parameters of a device are most often measured and quoted at the one dB compression point. It can be seen from the results that a large input signal level (3.8 dBm or a 1 V p-p sinewave) was required to reach the one dB gain compression point, which indicates that the amplifier can handle a wide dynamic range of input signals. This is important in the linear oscillator application, where it is desirable to use a large signal level in order to minimize the effects of circuit noise sources on the oscillator output.

Some additional work would be necessary in order to fully characterize the noise properties of the polysilicon emitter bipolar devices. Unfortunately, the test equipment required to

measure the noise figure of the amplifier was unavailable. A noise figure of 4.5 dB at 1 GHz is specified by Avantek for the MSA-0735 amplifier and it is expected that the BiCMOS amplifier will match this performance.

Figure 5.13 : Frequency response of the broadband amplifier

5.3 Summary

The capabilities of the BiCMOS process in linear microwave circuit applications have been explored in this chapter. The results of this study have demonstrated that it is possible to realize passive monolithic inductors and broadband linear microwave amplifiers in an advanced silicon IC technology.

The gain and bandwidth achieved by the broadband amplifier fabricated in BiCMOS technology clearly demonstrates that the amplification requirements of a linear microwave oscillator circuit designed for operation in the giga-Hertz frequency range can be realized.

The performance of the BiCMOS broadband amplifier is comparable to the performance which can be achieved in other pure bipolar technologies. However, a lower noise amplifier design would be desirable for the linear oscillator application. Nevertheless the results of this design study provide a basis for further study and development in this area.

Passive monolithic inductors are used in a wide variety of microwave circuits which are currently implemented in technologies such as GaAs. It would be very attractive to be able to adapt some of these existing circuits and design techniques to silicon technology in order to achieve greater system integration, reliability, and also to reduce component costs. The results of the study and experiments in this chapter on two microstrip inductors which were fabricated in the BiCMOS technology are very encouraging. Microstrip inductors were designed and fabricated that exhibit nearly ideal behaviour over the lower RF range (i.e., 100 MHz - 3 GHz), and the low quality factor (Q) of these inductors was shown to be almost entirely due to the thickness of the top conductor metallization.

Since it has been demonstrated that the RF losses due to the conductive silicon substrate are small (at least in the frequency range from 100 MHz to 3 GHz), it is possible that good quality microstrip components could be realized in silicon BiCMOS technology. However, a considerable amount of study and experimentation is still required in this area. The geometry and process technology must be optimized in order to improve the performance of the inductors to the point where these components can be used in the design of higher quality circuits. This will require an understanding of the high frequency behaviour of the microstrip transmission line fabricated in the Si-SiO₂ system and the effect of processing parameters such as oxide layer thickness and substrate doping on the performance of the transmission line. The accuracy of the computer-aided design algorithms used to design and analyze the microstrip inductor appears to be adequate, however, more accurate modelling of the component behaviour than has been demonstrated in this study will be required for circuit design purposes. Better model accuracy is necessary in order to reduce the number of iterations required to complete a design.

The development of a design and fabrication capability in microstrip components on silicon could be applied to many more circuits than the microwave oscillator application discussed in this chapter. Microstrip transformers can be realized using two interwound spiral inductors to form the primary and secondary windings. These devices can be used in the implementation of low-loss feedback networks for low-noise amplifiers, output coupling

circuits for power amplifiers, and in the design of low-noise RF and microwave mixers. The capability to fabricate these types of circuits combined with the other circuit capabilities of both CMOS and bipolar silicon technology would provide a unique opportunity for designers in the development of high-frequency circuits and systems.

6. Voltage-Controlled Oscillators

Monolithic circuit design in silicon technology utilizes a limited set of components which can be integrated on-chip (such as resistors, capacitors and active devices). The advantages offered by the monolithic context must be exploited in order to realize low cost and manufacturable circuits. The main performance advantages of this technology, when compared to discrete circuits, are the close thermal matching of components and low tolerances on the ratio of component parameters when fabricated together on the same IC. Within the limitations of current silicon technology, the potential of implementing a high frequency monolithic voltage-controlled oscillator (VCO) will be investigated in this chapter. The design objective is to produce a high frequency (greater than 1 GHz) fully-monolithic circuit suitable for use in a timing recovery PLL. The performance specifications of a voltage-controlled oscillator are defined and the circuits representative of the current state-of-the-art in monolithic technology are reviewed. A circuit topology capable of achieving the desired operating frequency is then discussed, and some experimental results will be presented for a prototype circuit fabricated in the BiCMOS process. Improvements to the VCO design which could enhance the oscillator performance and manufacturability of the circuit will also be presented.

6.1 VCO Specifications

The VCO in a timing recovery circuit must output a stable, periodic timing signal which can be used to drive a data regenerator. The important oscillator specifications for timing recovery are [50]:

1. Spectral purity (phase stability)
2. Frequency stability
3. Modulation sensitivity, K_o
4. Modulation bandwidth
5. Frequency control characteristics (e.g., monotonicity)

Phase noise inevitably accompanies the desired oscillation frequency at the output, and spectral purity is a measure of the phase stability of the oscillator output when the oscillator is free-running (i.e., uncontrolled by the PLL). Frequency stability describes the change in free-running frequency with temperature, supply voltage, aging, etc. Modulation sensitivity is the oscillator gain factor (K_o , in radians/Volt) and the modulation bandwidth describes the dynamic range of the oscillation frequency. Oscillator stability must be sacrificed to obtain high sensitivity, wide modulation bandwidth or high linearity. A linear frequency control characteristic is desirable for PLL FM demodulators, but is less important in timing recovery applications. This is because the timing recovery PLL is attempting to track the average frequency of the input signal and so the frequency deviations of the output are small when the loop is in-lock. Also, monotonicity of the frequency control characteristic is necessary to achieve loop stability.

The spectral purity of the free-running VCO will have a significant impact on the performance of a PLL design. The output signal from the VCO is mixed by the phase detector to baseband when the PLL is in-lock. The phase noise components which lie close to the loop centre frequency will fall within the loop filter bandwidth and the resulting error signal at the filter output will act to suppress these noise components. Phase noise components in the oscillator output which are at frequencies sufficiently far away from the centre frequency will lie outside the loop filter bandwidth. No error signal will be derived in order to correct for these fluctuations in frequency. Therefore phase noise in the oscillator output which lies outside the loop bandwidth is unaffected by the operation of the PLL, and so the oscillator phase noise should be kept as low as possible.

The phase noise at the free-running oscillator output is mainly caused by noise from active devices (such as $1/f$ noise), which mixes with the oscillating signal through circuit non-linearities and appears as phase noise on the timing clock. The phase noise decreases for frequencies further away from the desired oscillating frequency, and this limits the total contribution of noise which is outside the loop bandwidth. Low-stability oscillators (e.g., RC oscillators) will produce high levels of phase noise outside the narrow loop bandwidth required for timing recovery. Therefore the contribution of the internally generated noise from the VCO to the total timing jitter should be considered. Noise outside the loop bandwidth cannot accumulate in repeater chains because the overall jitter transfer function attenuates high frequency jitter components. However, the internally generated noise does

affect the total jitter at any one repeater, degrading the transmission link bit-error performance.

6.2 Monolithic VCO Circuits

Tuned circuit oscillators such as the linear microwave oscillator briefly discussed in Chapter 5 of this thesis are often implemented with high quality passive feedback networks such as crystal, SAW or ceramic bandpass filters, and these networks are incompatible with silicon process technology. A passive inductor could be used in the feedback circuit realization, but the microstrip inductor described in the previous chapter will require further development in order to accurately predict the component behaviour and improve the electrical characteristics of the coil. RC oscillator designs which use only resistors (R), capacitors (C) and active devices to realize the circuit can be completely fabricated on a single chip. Both linear (phase-shift oscillator) and non-linear (relaxation oscillator) RC circuit designs are possible and the configurations suitable for the design of a high frequency VCO will be examined in this chapter.

Figure 6.1 : RC phase-shift oscillator.

An RC phase-shift oscillator (see Figure 6.1) is similar to a tuned circuit oscillator (refer to Figure 5.1) and is usually implemented using discrete components. The bandwidth of the feedback network is much wider than the bandwidth of a resonant tuned circuit, which results in higher phase noise at the oscillator output. A feedback network provides the phase shift necessary to sustain oscillation, and a gain stage compensates for losses in the feedback network and loss due to output loading. Typically, three highpass RC filter

sections are used as a feedback network to phase shift the output of an inverting gain stage by 180 degrees [51]. Ideally, a gain of at least 29 is required to compensate for the loss through the feedback network, which can be difficult to achieve at high frequencies without adding significant phase shift to the amplified signal. The variation in phase shift caused by component tolerances results in a change in oscillation frequency, which is undesirable. Tuning of the oscillator is usually accomplished by ganging the feedback network capacitors. A monolithic implementation would require varactor diodes as variable capacitors, which must be d.c. isolated from the amplifier circuit in order to vary the filter capacitor values. This requires a.c. coupling capacitors that are difficult to fabricate on-chip. Also, the bias circuitry for the varactor diodes complicates the circuit design because the bias network must be isolated from the oscillation signal path.

Figure 6.2 : Emitter-coupled multivibrator.

A second type of oscillator, which is easily fabricated using monolithic circuit technology, is the RC relaxation oscillator. An example of this class of circuit is the emitter coupled multivibrator shown in Figure 6.2. These oscillators usually operate by charging or discharging a capacitor at a known rate using a constant current. Frequency tuning is

accomplished by varying a voltage or current, which simplifies external trimming of the circuit. The circuit outputs are compatible with digital logic circuits without the use of limiting amplifiers. However, the frequency stability of the circuit is poor at high frequencies, because the switching time of the active devices becomes a significant portion of the oscillation period. This makes the output frequency susceptible to temperature, process and supply variations. The spectral purity of the oscillator is degraded by noise sources that affect switching thresholds and bias currents. Consequently, the stability of a free-running relaxation oscillator is generally inferior to the stability of a free-running tuned circuit oscillator.

The maximum oscillation frequency of an RC relaxation oscillator is limited by the switching speed of the active devices and the load impedance at each node in the signal path of the circuit. Low voltage swings across circuit loads increase the switching speed and reduce the circuit power consumption. In order to achieve low signal swings and maintain adequate signal-to-noise ratio, differential-mode circuits are preferred. This also reduces the interaction within the circuit such as crosstalk and improves rejection of common-mode noise. Minimizing noise in an RC oscillator circuit is desirable because the wider bandwidth of these circuits results in higher phase noise in the oscillator output. Noise is introduced in relaxation oscillators by regenerative switching between charge and discharge regimes. The abrupt change in device operating point results in intermodulation between baseband noise (such as device $1/f$ noise) and the high frequency signal. This mechanism causes low frequency noise from baseband to appear as phase noise sidebands in the oscillator output spectrum.

The conventional RC relaxation oscillator circuits which are suitable for monolithic integration and high frequency operation will be reviewed.

6.2.1 Emitter-Coupled Multivibrator

The emitter-coupled multivibrator shown in Figure 6.2 is a commonly used RC relaxation oscillator circuit in monolithic PLLs, and a detailed description of the circuit has been written by Grebene [22]. It is a completely symmetric circuit (i.e., in Figure 6.2, $R_1=R_2$, $R_3=R_6$, etc.) using all-npn bipolar switching devices, and it is therefore suited to high frequency operation. Circuit symmetry guarantees a duty cycle close to 50 percent and the differential output signal at the emitters of Q_3 and Q_4 are compatible with ECL circuits.

The timing capacitor, C , is alternately charged and discharged by a constant current, I_0 , supplied by current sources Q_5 and Q_6 . The peak voltage across the timing capacitor alternates between $+V_{BE}$ and $-V_{BE}$ as the circuit oscillates between two astable states. The switching threshold is defined by the voltage drop across the collector catch diodes (D_1 and D_2), the feedback buffers (Q_3 and Q_4), and the switching devices (Q_1 and Q_2). Current flow through the load resistor of a switching device in the "on" state must be sufficient to forward bias the collector diode.

The oscillation period is determined by the change in potential across the capacitor due to the constant current

$$I = C \frac{dV_c}{dt} \quad (6.1)$$

Regenerative feedback quickly reverses the flow of current through the capacitor every half-cycle, resulting a voltage change of $2V_{BE}$ across the capacitor. Therefore equation 6.1 can be rewritten as

$$I = I_0 = C \frac{2V_{BE}}{(T/2)} \quad (6.2)$$

and the oscillation period is

$$T = \frac{4V_{BE}C}{I_0} + 2t_s \quad (6.3)$$

where t_s is the time required by regenerative switching of the circuit. The oscillation frequency is therefore

$$f_{osc} = \frac{1}{T} = \frac{I_0}{4V_{BE}C + 2I_0t_s} \quad (6.4)$$

If the switching time of Q_1 (or Q_2) is negligible compared to the charging or discharging time of the capacitor then the oscillation frequency is linearly related to the current I_0 . However, as the oscillation period is decreased, the switching time of the active devices becomes the limiting factor, and the frequency control characteristic becomes non-linear.

For this reason, the oscillation period is usually chosen at least ten times greater than the switching time of the transistors.

The oscillation frequency exhibits a strong temperature dependence caused by the switching threshold which is defined by V_{BE} (V_{BE} has a negative temp. coefficient of about 2 mV/C) and the temperature dependence of the current source resistors R_3 and R_6 . If the switching time of the active devices can be neglected, then temperature compensation can be achieved by making I_0 directly proportional to V_{BE} [52].

The regenerative switching action of the circuit causes current transients from the power supply, which result in unwanted crosstalk and noise.

The circuit requires a floating timing capacitor (C) and any stray capacitance at the emitters of Q_1 or Q_2 disrupts the operation of the oscillator. Stray capacitance is difficult to avoid with an on-chip capacitor, especially for the small values of capacitance required at high frequencies (i.e., less than 1 pF). Using an off-chip timing capacitor at high frequencies is impractical because bondwire and packaging inductance and resistance degrade the circuit performance.

The voltage drop across the collector resistors R_1 and R_2 must be large enough to forward bias the collector catch diode of the "on" transistor, which restricts the dynamic range of the tuning current I_0 . Replacing the fixed collector resistors with variable resistors that can track changes in I_0 has been used to achieve a multi-octave tuning range [52], but this introduces additional parasitic capacitance at a critical switching node in the circuit, which increases t_s . Current state-of-the-art limits the maximum oscillation frequency of the emitter-coupled multivibrator to below 250 MHz [53].

6.2.2 Schmitt Trigger Oscillator

Another popular high frequency monolithic circuit configuration is the Schmitt trigger relaxation oscillator which uses a grounded timing capacitor (see Figure 6.3). The grounded timing capacitor can be fabricated on-chip with a smaller value than an external capacitance, and grounding one terminal of the timing capacitor has been shown to reduce oscillator phase noise [88]. Operation at frequencies greater than 100 MHz has been demonstrated for this circuit configuration [54].

Two emitter-coupled pairs (Q₁, Q₂ and Q₃, Q₄) are connected in a ring configuration with the odd number of inversions required for oscillation. Feedback through Q₁₀ to the base of Q₄ forms a Schmitt trigger circuit with input at the base of Q₃. The difference in trigger points for the Schmitt circuit is approximately $I_3(R_1+R_3)$.

The oscillation period is determined by the time required to charge the capacitor through a voltage difference $I_3(R_1+R_3)$ using current I_O (via current source Q₁₁). Therefore the oscillation period is

$$T = \frac{C \cdot I_3(R_1+R_3)}{I_O} + t_r \quad (6.5)$$

and

$$f_{osc} = \frac{I_O}{C \cdot I_3(R_1+R_3) + I_O t_r} \quad (6.6)$$

where t_r is the switching time of the circuit required to discharge the timing capacitor and reset the Schmitt trigger circuit.

The circuit is fast because it is an all-npn design. The period is independent of V_{BE} if t_r is negligible and the oscillation can be made temperature insensitive by making $I_3(R_1+R_3)$ independent of temperature using bandgap reference design techniques. The operating frequency range can be made very wide; the frequency limits are determined by the range of bias current, I_O , and the finite base current required by Q₃. Connecting the timing capacitor to the V_{CC} supply minimizes supply crosstalk because the other terminal is clamped to V_{CC} via Q₅. The timing capacitor is usually integrated on-chip to minimize external noise pick-up. However, the oscillator produces current spikes during switching as the timing capacitor is quickly charged up by emitter follower Q₅, which adds significant noise to the output.

Unfortunately, the output waveform of the oscillator is not symmetric and the duty cycle is significantly different from 50 percent. To correct this a dual-slope design can be used to produce a triangular waveform across the timing capacitor, rather than the sawtooth

waveform produced by the circuit of Figure 6.3. However, the duty cycle in such a design depends upon the matching of charging and discharging current sources. A toggle flip-flop at the oscillator output could also be used to produce a 50 percent duty cycle waveform, but this reduces the maximum oscillating frequency by a factor of two.

Figure 6.3 : Schmitt trigger RC oscillator.

The bandwidth of the Schmitt trigger oscillator is limited by the speed of the regenerative switching circuit which toggles between two astable states. The minimum value of the timing capacitance is determined by the parasitic capacitances of devices connected to the base of transistor Q3. When operating at maximum frequency, the Schmitt trigger oscillator is equivalent to a non-linear switching stage with positive feedback between the output and input. The circuit becomes a single stage ring oscillator circuit.

6.2.3 Ring Oscillators

Attempting to increase the operating frequency of an RC relaxation oscillator circuit minimizes the timing capacitance and reduces the circuit topology to a ring oscillator configuration. Therefore ring oscillator topologies will be considered as the basis for the design of a high frequency monolithic RC oscillator.

Ring oscillators are widely used in integrated circuit development and manufacturing to characterize the propagation delay of digital logic circuits. The oscillator consists of a chain of logic gates which is closed back upon itself (see Figure 6.4). An odd number of logic inversions (i.e., an odd number of logic inverter circuits) are required to form the oscillator. The oscillation frequency is related to the propagation delay of each gate and the number of logic inverters by the following equation

$$f_o = \frac{1}{n \cdot t_{pd}} \quad (6.7)$$

where

- n is the number of inverting logic gates (n , odd)
- t_{pd} is the propagation delay of each gate (assumed identical)

Figure 6.4 : Ring oscillator.

In order to control the frequency of the ring oscillator output, some electrical parameter which controls the propagation delay of each inverting stage must be used.

Reducing the timing capacitance in a RC relaxation oscillator will reduce the frequency stability of the oscillator because the switching time of the circuit active devices becomes a significant portion of the oscillation period. This is because device switching time is sensitive to variations in semiconductor processing and temperature. The oscillation period of a ring oscillator is therefore particularly sensitive to process and temperature variations, which is why the circuit is used as a process monitor in circuit manufacturing. The variation of the oscillation frequency must be accounted for in the circuit design by making the modulation bandwidth of the oscillator wider than the anticipated output frequency range. The anticipated change in frequency due to process and temperature variables can then be accommodated in order to operate the VCO at the desired frequency.

The electrical parameters of a logic circuit are not usually linearly related to the switching time of the circuit and so the frequency control characteristic of a ring oscillator is usually non-linear. The modulation characteristics of the circuit must be characterized in order to determine the modulation sensitivity (K_o) and the relationship between output frequency and the frequency control input voltage. The influence of circuit noise sources on the spectral purity of the oscillator must also be considered. The circuit topology should be chosen in order to minimize the effects of noise caused by power supply fluctuations, $1/f$ and shot noise in active devices and thermal noise sources on the oscillator output. The PLL will reject internally generated frequency instability which falls within the loop bandwidth, however, noise which lies outside the loop bandwidth will appear at the VCO output.

6.2.4 Ring Oscillator Noise Considerations

The analysis of the phase noise at the output of a ring oscillator is complicated by the non-linear switching of the logic inverters in the ring. Linear analytical tools cannot be used. However, the analysis of noise in multivibrators by Boon [55] and the analysis of noise in feedback oscillators by Leeson [56] can be considered in order to make some qualitative comments about the noise performance expected from a ring oscillator.

A. Multi-stage ring oscillators

Consider the multi-stage ring oscillator shown in Figure 6.5. Assuming that the total propagation delay around the ring is large compared with the propagation delay of a single

gate, each inverter in the ring will switch fully on or off in a small fraction of the total oscillation period. Single-ended input logic inverters are assumed. The noise sources present in each inverter are modelled by equivalent noise sources at the gate input. When the gate is switched off, the gain between the input and output is small and only a small amount of noise from the noise source at the input appears at the gate output. However, when the gate is switched on the gain of the inverter becomes large, and noise at the inverting gate input is amplified by the inverter power gain and appears at the output. Therefore the output noise can be modelled by an equivalent input noise source which is multiplied by the time varying gain of the logic inverter. The periodic gain variation is analogous to sampling of the equivalent noise source at the input, and the result is aliasing in the output noise spectrum. Boon and Snee [54, 55] have experimentally verified this for relaxation oscillators where the time varying gain is periodic and of short duration (similar to sampling by an impulse function). The replication of the input noise spectrum at the output due to sampling by the time varying gain results in significant output noise sidebands.

Figure 6.5 : Multistage ring oscillator.

B. Short ring oscillators

The output of a single logic inverter in a ring oscillator with many stages is fed-back to the inverter input through a long chain of inverters, and the phase shift between the gate output and input is a large integer multiple of 180 degrees. Therefore the gain in the feedback path can be assumed to be very small because a significant number of inverters in the feedback chain will be switched off. As the ring is shortened, the gain between input and output will

eventually increase, and there will be a continuous connection between input and output. The effect of continuous positive feedback on the output noise spectrum of a ring oscillator with only one or two stages will be considered by analogy to the tuned circuit oscillator.

Figure 6.6 : Noise model of an amplifier with input signal.

Noise sources in a bipolar transistor amplifier are modelled by a voltage source in series with the input (corresponding to the thermal noise generated by the base resistance), and a current generator in parallel with the input (corresponding to the noise caused by shot noise on the base current). The phase noise at the amplifier output can be modelled by a noise-free amplifier and a phase modulator at the input which is driven by an composite noise source, $S_{\phi}(f_d)$ (see Figure 6.6). The input signal is assumed to be a pure sinusoid at frequency f_0 . The noise source ($S_{\phi}(f_d)$) will have two components. One component is due to phase modulation of the input signal caused by additive white noise (from thermal noise sources). This noise component decreases as the input signal level increases, because additive noise has less effect on the phase of the input signal as the input slew rate increases (note that slew rate is directly proportional to signal amplitude for a sinusoid). The second component is due to large amplitude noise sources at low frequency such as $1/f$ noise, which also affect the phase shift through an amplifier because of intermodulation resulting from circuit non-linearities. This non-linear mixing causes a $1/f$ phase noise spectrum about the carrier (f_0 , or the desired output signal). These noise sources are assumed to produce only small fluctuations in signal phase. As a result, the amplitude of the spectral components at the amplifier output (called modulation sidebands) are linearly related to the phase deviation of the amplifier input signal caused by the noise. The resulting output noise spectrum is illustrated in Figure 6.7.

Figure 6.7 : Noise spectrum of a transistor amplifier.

The phase noise at the input of the amplifier is modified by positive feedback through the tuned circuit feedback network in an oscillator. The tuned circuit or resonator (with quality factor Q) acts as a bandpass filter which rejects undesired noise components and feeds the desired frequency component from the oscillator output back to the input. For fluctuations in output frequency measured with respect to the carrier frequency, the transfer function of the tuned circuit can be described by a lowpass filter response ($H(f_d)$), where

$$H(f_d) = \frac{1}{1 + j \frac{2Qf_d}{f_0}} \quad (6.8)$$

and

$f_0/2Q$ is the half-bandwidth of the bandpass filter with quality factor, Q .

$f_d = f - f_0$, which is the frequency deviation with respect to the carrier at f_0 .

Equation 6.8 describes the transfer function of the feedback network. The amplitude of spectral components in the amplifier output, produced by phase fluctuations at the input (i.e., the phase modulation sidebands) will pass unattenuated up to the half-bandwidth of the tuned circuit. The phase response of the resonator is given by

$$\theta(f_d) = -\arctan\left(\frac{2Qf_d}{f_0}\right) \approx -\left(\frac{2Qf_d}{f_0}\right), \text{ for small } f_d \quad (6.9)$$

Equation 6.9 shows that if the frequency deviation is small, the phase of the resonator output is linearly related to the frequency deviation. If the deviation is large, then the output phase approaches a constant value which is independent of frequency deviation (f_d).

Leeson's model of a tuned circuit oscillator is illustrated in Figure 6.8 [56, 57]. A noise-free amplifier (assumed to be unity gain at f_0) and a resonant circuit (which is assumed to be lossless in the passband) are connected in a positive feedback loop. The amplifier is assumed to be linear, although it is non-linearity in the amplifier which causes noise from baseband sources (such as $1/f$ noise) to phase modulate the carrier. This assumption of constant loop gain is valid because most linear oscillators use an automatic gain control circuit to maintain the amplifier gain at the level required to sustain oscillations. The amplifier gain will be large when the circuit is switched on so that the oscillation can build-up to the required output level. However, after the circuit has been switched on for some time, the fluctuations in amplifier gain will be small and will occur slowly. Thus the circuit behaviour can be assumed to be linear over many cycles of the output waveform and no single cycle will be distorted.

Figure 6.8 : Leeson's model of oscillator phase noise.

The open-loop phase noise spectrum ($\Delta\phi_{in}(f_d)$) is produced by the effect of circuit noise sources on the amplifier input signal. The equivalent lowpass transfer function for the resonator ($H(f_d)$) given by eq. 6.8) is used to model the feedback network effects on the phase noise. Most of the oscillator noise close to the carrier in a well-designed tuned circuit

oscillator is phase or FM noise, because oscillator limiting mechanisms (e.g., an AGC circuit to control the amplifier gain) tend to eliminate AM noise [58].

The closed-loop response of the phase feedback loop is given by

$$\Delta\phi_{out}(f_d) = [1 + j \frac{f_o}{2Qf_d}] \Delta\phi_{in}(f_d) \quad (6.10)$$

Equation 6.10 describes the phase modulation due to noise (or phase noise) at the amplifier output. The phase noise at the input to the amplifier ($\Delta\phi_{in}$) is enhanced by positive feedback because for small frequency deviations (small f_d) the output phase noise will be greater than the input phase noise. Or, as described by equation 6.9, feedback through the resonator forces the phase change at the amplifier input (resonator output) to be linearly related to the frequency deviation at the amplifier output (resonator input) within the resonator bandwidth. Outside of this bandwidth, the feedback through the resonator approaches zero as f_d increases and the output phase noise ($\Delta\phi_{out}$) is the same as the input phase noise ($\Delta\phi_{in}$) because the amplifier gain is unity.

Leeson's model can be used to predict the spectral characteristics of a feedback oscillator in terms of known circuit parameters (the equivalent input noise of the amplifier, the tuned circuit Q, etc.). It has been confirmed by experimental measurements on high quality microwave signal sources [56]. The model predicts that phase noise can be minimized if the following conditions are met :

1. Minimize the bandwidth of the feedback network (i.e., large Q).
2. Avoid non-linearity Non-linearity in the oscillator will increase the amplitude of noise components at frequencies close to the carrier, thereby increasing the phase modulation of the input signal ($\Delta\phi_{in}$).
3. The signal voltage relative to the equivalent noise voltage should be made as high as possible to reduce the phase modulation caused by additive noise sources.
4. Choose active devices which have low flicker (1/f) noise.

The Leeson model cannot be directly applied to a ring oscillator design. The feedback network in a ring oscillator is an active circuit with a lowpass response, not a bandpass resonator. Also the gain of the logic inverter is non-linear because it is a limiting amplifier. Therefore an equation predicting the phase noise spectrum at the output of a ring oscillator cannot be derived using linear analytical tools because of the non-linear behaviour of the circuit. However, the application of positive feedback to the short ring oscillator can be expected to cause phase noise enhancement of internally generated noise sources close to the carrier frequency. Therefore internally generated noise should be minimized, especially noise caused by $1/f$ sources. Circuit topologies for a high frequency ring oscillator VCO will now be considered.

6.3 High Frequency Oscillator Topologies

The emitter-coupled logic (ECL) inverter has been chosen as the switching element for the design of a high frequency ring oscillator. The propagation delay time of a properly designed ECL inverter is shorter than the delay time achievable using other logic families in silicon technology. The differential-mode ECL logic inverter circuit was discussed in Chapter 4 of this thesis and the schematic diagram of a single-ended inverter circuit is shown in Figure 6.9. The inverter is an all-npn transistor design which uses active devices Q_1 and Q_2 to steer current I_0 through one of the load resistors R_{L1} or R_{L2} , depending upon the logic state at the input, v_{in} . The transistors cannot enter saturation because R_L and I_0 are chosen so that the base-collector junctions of the devices are always reverse biased. This eliminates the degradation in switching time caused by stored charge effects in other bipolar transistor logic families such as TTL. The emitter follower buffer (Q_3) can supply a large output current to quickly charge and discharge output load capacitance due to other device inputs and interconnect loading. The logic level swing ($\Delta V = I_0 R_L$) can be made small because of the large transconductance of the bipolar transistor. A MOS transistor requires a larger voltage swing and large device size compared to a bipolar transistor because the MOSFET has a lower transconductance, which limits the operating speed of CMOS and other MOS logic families.

Current steering by the active devices in an ECL gate reduces power supply transient currents, and thereby reduces circuit switching noise. However, current transients are also

caused by the emitter follower buffer transistors when driving a large output capacitance. Normally, V_{CC} is chosen as the circuit ground so that noise from the power supply is attenuated at the output and across the load resistors. The emitter follower output and the collector loads are low impedance nodes with respect to V_{CC} and so noise present on the power supply (V_{EE}) will be attenuated at the output.

Figure 6.9 : Single-ended ECL inverter.

A differential input and output signal configuration for the ECL inverter is desirable for a number of reasons. Replacing V_{ref} with a complementary signal input eliminates the need for a reference voltage source. Any common-mode noise at the inputs or on the power supplies will be attenuated at the outputs of the differential pair Q_1, Q_2 . The voltage swing (ΔV) required to switch the inverter on and off is reduced if differential signals are used and therefore the size of the load resistors (R_L) can be reduced, which increases the switching speed of the circuit.

The ECL inverter circuit must be configured in a ring with positive feedback in order to form an oscillator. Sustained oscillations will occur when the closed-loop gain of an oscillator circuit is greater than unity at a total loop phase shift of 360 degrees. Two feedback configurations which complement the differential ECL inverter will be

considered. Figure 6.10(a) shows two differential inverters (shown symbolically as gain blocks) connected in a ring configuration. It should be noted that an odd number of inverting logic gates, usually required in order to obtain the correct feedback for oscillations, are not necessary if differential input and output signals are available. The four ECL outputs are in phase quadrature (i.e., phase shifted by 90 degrees), which could be useful in digital communications applications using modulation schemes such as DPSK (differential phase shift keying). Figure 6.10(b) illustrates an alternative feedback network for a single ECL inverter, which uses emitter follower buffers to provide the phase shift necessary to sustain oscillations. The logic inverter provides at least 180 degrees of phase shift and the emitter followers cause an additional time delay to the inverter output for a total loop phase shift of 360 degrees. The followers also level shift the signal from the output of the inverter. This circuit configuration can be considered as a phase shift oscillator with an active feedback network.

Figure 6.10 : Ring oscillator configurations.

Noise sources present in a ring oscillator circuit have a significant effect on the spectral purity of the output, because the feedback network does not have the frequency selectivity of a tuned circuit oscillator to filter out unwanted noise components. Choosing a fully differential switching circuit as the core of the oscillator helps to attenuate common mode noise sources, and proper choice of V_{CC} and V_{EE} connections attenuates noise introduced by power supply fluctuations.

6.4 Ring Oscillator Analysis

The performance of the two ring oscillator circuits shown in Figure 6.10 have been simulated using the HSPICE circuit simulator. The bipolar transistor models for the nominal BiCMOS process were used for the simulations. The differential-mode ECL inverter circuit discussed in Chapter 4 of this thesis, which is shown Figure 6.11, was used as the logic inverter in both ring oscillator designs (note that the current source bias voltage, V_{CS} , was adjusted to set the d.c. bias current, I_{CS} , for the differential pair Q_1, Q_2).

Figure 6.11 : Differential-mode logic inverter circuit.

The minimum size bipolar transistor available in the BiCMOS process (the 1X device) was selected for each the active devices in the inverter circuit. A load resistance (R_L) of 600 Ohms and a bias current of 400 μA (I_{CS}) were chosen in order to achieve a peak-to-peak differential output voltage swing close to 500 mV. The output logic swing must be made large enough to achieve an adequate signal-to-noise ratio at the inverter input but small enough to allow high frequency operation. A logic voltage swing of 500 mV was chosen as a compromise between these two constraints. The bias currents for the differential pair and the emitter follower output buffers of the logic gate were chosen to maximize the bandwidth of the bipolar transistor. Selecting a collector current of 400 μA (at a temperature of 27 C) ensures that the operating point of the transistor will be close to the maximum unity gain frequency (f_T) of the device over a wide operating temperature range.

The phase-shift ring oscillator also requires an emitter follower buffer to provide feedback around the logic inverter circuit as shown in Figure 6.10(b). The emitter follower feedback network chosen for the phase-shift oscillator is illustrated in Figure 6.12. A bias current of 1600 μA for each of the followers was chosen to maximize the feedback circuit bandwidth. Active devices Q_1 to Q_4 were made four times the minimum size bipolar transistor (i.e., a 4X device).

Figure 6.12 : Emitter follower feedback network used in ring oscillator simulations

A large-signal (transient) analysis and a small-signal (a.c.) analysis of each ring oscillator were performed. For small-signal analysis, the feedback to the input of each oscillator circuit was disconnected as shown in Figure 6.13. The d.c. bias at the circuit input was set to the average value seen in the transient analysis simulations. The oscillator output was connected to another ECL inverter in order to simulate circuit loading effects. The results of the small-signal and transient analyses are compared in Table 6.1.

a) 2-Inverter Oscillator

b) Phase-Shift Oscillator

Figure 6.13 : Ring oscillator circuit connections for small signal analysis.

At the oscillation frequency determined by the transient analysis, the phase shift between the input and output determined by small signal simulation of the phase-shift oscillator was very close to 360 degrees (note that the simulator restricts the phase shift results to within ± 180 degrees). This excellent agreement (within 0.5%) between the small and large-signal simulations shows that small-signal analysis can be used as a tool in the design of the phase-shift ring oscillator circuit.

Table 6.1 : HSPICE simulation results for 2 ring oscillator topologies.

Oscillator	Analysis Type				
	Transient	Small-Signal (a.c.)			
	Period, in ps	f_{osc} , in GHz	f , in GHz	Gain, in dB	Phase Shift
2-inverter	538.5	1.857	1.564	5.05	0°
Phase-Shift	355.7	2.811	2.824	6.70	0°

One of the objectives of this study is to investigate the performance capabilities of BiCMOS technology. The ring oscillator circuit can be used to provide valuable information concerning the accuracy of the device models and CAD circuit analysis tools, as well as demonstrate the high frequency capabilities of the process. The phase-shift oscillator circuit has been chosen for further investigation in order to explore and characterize the behaviour of circuits fabricated in the BiCMOS process at the highest possible operating frequency.

6.5 Phase-Shift Ring Oscillator Test Circuit

A phase-shift oscillator test circuit similar to the circuit described in the previous section has been designed and fabricated in the BiCMOS process. Experimental measurement of a ring oscillator circuit can provide data which relates the effects of device parameter variation caused by changes in the fabrication process, to the performance of a high frequency circuits. The noise produced by various circuit samples can also be easily compared using spectral analysis.

A few design guidelines for the design of low-noise oscillators were outlined in section 6.2.4 of this chapter. Unfortunately, when the ring oscillator test circuit was designed, the main objective of the design exercise was to produce a circuit which would demonstrate the speed capability of the bipolar devices in the BiCMOS process. However, a study of this test circuit and an analysis of the circuit behaviour provides information which can be applied to the refinement and improvement of the phase-shift oscillator design.

The phase noise at the output of the ring oscillator test circuit was also measured. Noise voltages and currents generated by active and passive devices modulate the signal produced by the oscillator and appear as phase noise at the circuit output. The simplest technique for measuring oscillator noise is to measure the oscillator frequency spectrum using a spectrum analyzer. Noise measured in this way will usually require a number of correction factors in order to obtain the oscillator phase noise, which is defined as

$$\text{phase noise} = \frac{\text{corrected noise per unit bandwidth at } f_m}{\text{carrier power}} \quad (6.13)$$

The phase noise is given by the ratio of the corrected noise power per unit (i.e., 1 Hz) bandwidth at a given measurement frequency (f_m) to the carrier or fundamental signal power. It is most often quoted in decibels (i.e., n dBc/Hz).

Corrections to the signal power measured on a spectrum analyzer are required in order to compensate for effects of the analyzer's signal processing circuitry on the oscillator output spectrum [57, 60]. The signal detector in a spectrum analyzer is usually not a true rms detector and therefore a correction factor must be applied to determine the correct signal power. Bandpass filtering in the analyzer is not an ideal square bandpass shape and thus the filter shape as well as the actual filter bandwidth must be accounted for in order to determine the noise power per unit bandwidth.

The spectral analysis technique is only useful when the noise produced by the oscillator under test is much larger than the internal local oscillator of the spectrum analyzer, because it is impossible to identify the source of noise components in the measured frequency spectrum. Also, it is impossible to tell whether the power at different frequencies in the measured spectrum is produced by amplitude or phase fluctuations when measured with a spectrum analyzer. The phase-shift ring oscillator operates in saturation which limits amplitude fluctuations in the oscillator output and therefore it will be assumed that the noise sidebands in the measured spectrum are mainly due to oscillator phase fluctuations.

A Rohde and Schwarz model FSB spectrum analyzer was used to measure the phase noise of the ring oscillator. The FSB spectrum analyzer has a single-sideband phase noise measurement feature which applies the appropriate correction factors to the measured

identical in geometry to the current switching devices, are also biased with a 400 μA current. A fixed resistor was used to bias each follower because it was determined from a small signal noise analysis that the thermal noise contributed by a bias resistor is less than the total noise contribution of a transistor current source. A bipolar transistor current source (Q5) was chosen as the active device for the current source, because of the higher output impedance (small parasitic capacitance, high output resistance) of the bipolar device compared to an NMOS transistor operated at the same bias current. This improves the rejection of undesired common-mode signals by the differential amplifier in the ECL inverter. The smallest active devices available in the process (1X geometry devices) were used to reduce the power consumption and layout area of the circuit and also to demonstrate the performance of the minimum size transistors in an ECL-type circuit.

The bias network has been described in section 4.2.5 of this thesis and a schematic diagram of the circuit is shown in Figure 4.10 (refer to Chapter 4). The input to the bias network, which controls the bias current flowing through the emitter followers in the active feedback network, could be either a bias voltage V_t , or a bias current I_t . The other bias current, I_0 , sets the bias current flowing through the differential pair of the logic inverter (bias current I_{CS} in Figure 6.11).

The active feedback network for the phase-shift ring oscillator consists of two emitter followers in cascade as shown in Figure 6.12 (refer to section 6.4 of this chapter). The transistors used in the feedback circuit are larger than the devices used in the logic inverter design. Larger devices were used to reduce thermal noise caused by the base resistance of the bipolar transistor, because the thermal noise at the output of the 4X emitter follower is dominated by the noise due to the extrinsic and intrinsic base resistances [59]. The increased shot noise caused by an increase in the bias current required by a larger device (i.e., a 4X bipolar transistor compared to a minimum geometry 1X device) is less significant than the decrease in thermal noise due to the smaller base resistance of the 4X transistor. The propagation delay through the emitter follower buffers (a total of 3 including the emitter follower at the output of the ECL inverter) provides the phase shift necessary to sustain oscillation. The delay time through the feedback circuit can be varied by changing the emitter current flowing through the followers. The current available to discharge any parasitic capacitance at the output of the emitter follower is provided by the current sources Q3 and Q4 shown in Figure 6.12. Therefore an increase in the bias current

reduces the propagation delay of the buffer and increases the oscillation frequency. A bias network provides the bias voltage for the emitter current sources, and therefore the voltage input to the bias network can be used to control the phase shift through the feedback network and vary the oscillation frequency.

Polysilicon resistors were used throughout the circuit design because of the low parasitic capacitance of these devices compared to diffused resistors. The resistivity of the polysilicon material used to fabricate the resistors is of the order of 1000 Ohms/square. Therefore accurate small value resistors cannot be designed as a single component, but must be composed of a number of larger resistors in parallel, which will have a larger total parasitic capacitance. Unlike diffused resistors, the power dissipation of the polysilicon resistor must be considered because an oxide layer insulates the resistor from the substrate, thereby reducing the power handling capability of the resistor.

A block diagram of the complete phase-shift oscillator test circuit is shown in Fig 6.15. The three circuit blocks: the phase-shift ring oscillator (VCO), the frequency divider and the output buffer share the same supply voltages (i.e., $V_{CC} = 0$ V and $V_{EE} = -5$ V). The differential signal outputs of the ring oscillator drive a frequency scaling circuit which divides the oscillator output signal by a factor of four. The divider circuit consists of two cascaded D-type master/slave flip-flops, each of which are connected in a divide-by-two configuration. The individual flip-flop circuits are similar to the design described in Chapter 4 of this thesis. A frequency divider is required to lower the output frequency of the oscillator, so that a simple output driver design can be used to interface the output signal to a low impedance load. The buffer circuit interfaces a low level logic signal from the frequency divider output to a 50 Ohm load. A simple emitter follower is used to drive the output, and the output buffer has an overall -3 dB bandwidth of approximately 800 MHz.

6.5.2 Circuit Simulation and Experimental Results

The HSPICE circuit simulator has been used to predict the performance of the phase-shift ring oscillator circuit. The oscillator modulation characteristics and also the frequency stability of the oscillator for changes in temperature, power supply voltage and device parameters were determined from simulation. A block diagram of the test circuit which was fabricated in the BiCMOS process is shown in Figure 6.15, and the circuit output

frequency spectrum and it will display the corrected phase noise measured at the desired frequency offset from the fundamental or carrier signal. A plot of the measured frequency spectrum for the phase-shift ring oscillator test circuit is shown in Figure 6.21. The corrected phase noise at the output of the oscillator for a frequency offset of 100 kHz from the fundamental signal frequency of 632 MHz was -58.4 dBc/Hz. The phase noise produced by the front-end local oscillator in the FSB spectrum analyzer is far below this level (specified at -107 dBc/Hz, with the instrument settings shown in Figure 6.21 [61]) and therefore the error introduced in the measurement by the spectrum analyzer local oscillator can be considered negligible.

A correction factor must be applied in order to determine the phase noise at the oscillator output, because the frequency divider circuit lowers the frequency of the measured signal while the phase variation in the signal remains unchanged [58]. Thus the phase noise at the ring oscillator output will be

$$\begin{aligned}\text{oscillator phase noise} &= \text{measured phase noise} + 20 \log_{10}(\text{divide ratio}) \quad (6.14) \\ &= (-58.4) + 20 \log_{10}(4) = -46.4 \text{ dBc/Hz}\end{aligned}$$

A typical hybrid VCO designed for operation in the 2 to 3 GHz range of frequency (i.e., the Avantek VTO-8200 oscillator) has an output phase noise of approximately -90 dBc/Hz at a 100 kHz offset from the carrier [62]. The ring oscillator phase noise performance is considerably poorer than the present state-of-the-art in low-cost hybrid VCOs, but it is likely that some improvements in the performance of this simple monolithic ring oscillator can be realized. The effect of a poor quality connection between the frequency divider and the output buffer cannot be simply evaluated, but it is likely that some degradation in the quality of the output spectrum was caused by the modifications to the interconnect metallization.

There are other factors which also contribute to the noise level at the oscillator output. The minimum size bipolar devices are well suited to digital logic applications where fast switching at low values of collector current is desired in order to limit circuit power dissipation. However, these small area devices have poorer 1/f and thermal noise performance than larger area bipolar devices [63, 64]. Therefore it would be possible to reduce the circuit noise produced by the active devices by using larger area transistors; the

off during transient analysis), and the sequence of analysis used by the simulator (i.e., solving for a d.c. operating point before commencing transient analysis). In HSPICE, the oscillator can be started by ramping the power supply (the initial d.c. solution will be the trivial solution) or by intentionally introducing asymmetry into the circuit (e.g., making the inverter load resistor R_{L1} slightly larger than load resistor R_{L2}). However, the d.c. solution is useful for circuit analysis and debugging, so a short transient pulse generator was connected in series with one input of the logic inverter (a 0.1 Volt amplitude pulse with a time duration of 100 ps) which starts the oscillation. The transient due to the start pulse dies out after only a few cycles at the oscillator output.

The effect of a change in the emitter follower current on the oscillation frequency (follower current tuning) was simulated and the results are shown in Figure 6.16 for the nominal device parameters in the BiCMOS process. The measured data plotted in the Figure has been corrected for the effect of the frequency divider connected between the phase-shift oscillator and the output buffer in the test circuit, which divides the oscillator output by four. A strong non-linear frequency control characteristic was observed with the largest

Figure 6.16 : Phase-shift oscillator frequency as a function of the control voltage, V_t .

incremental change in frequency occurring at low bias currents. However, the curve is monotonic over a wide range of tuning voltage, which is necessary for closed-loop stability in a PLL. Curve fitting of the data gives the following relationships between the oscillation frequency (f_{osc}) and the input control voltage, V_t :

$$f_{osc} \text{ (HSPICE simulation)} = 2.92 + (5.75 \times 10^{-2}) V_t, \text{ GHz} \quad (6.11)$$

$$f_{osc} \text{ (measured)} = 2.64 + (5.31 \times 10^{-2}) V_t, \text{ GHz} \quad (6.12)$$

It should be noted that only the first two terms in the curve fitting polynomial are given in both equations 6.11 and 6.12. The complete polynomial fit to the data is plotted as a smooth curve connecting the data points shown in Figure 6.16.

The measured and simulated curves describing the change in oscillation frequency for a change in the input tuning voltage are similar in shape, but there is significant error between the two curves as described by equations 6.11 and 6.12. The zero-bias oscillation frequency is given by the first term in equations 6.11 and 6.12, and the modulation sensitivity of the oscillator (K_0 , which is the first derivative of equation 6.11 and 6.12 with respect to the tuning voltage, V_t) is given by the second term in equations 6.11 and 6.12. There is an error of approximately 10% between the simulated and measured results for the oscillator. Device parameters for the bipolar transistors measured on the same wafer as the oscillator test circuit were actually better than the nominal device parameters for the BiCMOS process which should have resulted in a measured oscillation frequency which was greater than the frequency predicted by computer simulation. However, the sheet resistivity of the polysilicon used to fabricate the resistors on these wafers was greater than the nominal specification for the process, and polysilicon resistor test structures on the same wafer exhibited some non-linear behaviour due to non-ohmic (i.e., rectifying) contacts between the interconnect metallization and the polysilicon layer. Resistor values which are larger than the nominal values in the bias network of the oscillator cause a reduction in the bias current for a given input voltage, V_t . Therefore the oscillation frequency for a given input voltage is lower than predicted for the nominal process parameters. Also, larger than nominal resistance values in the bias network will cause a reduction in the modulation sensitivity of the circuit, because the change in bias current (and therefore the change in oscillation frequency) for a change in input voltage is inversely

proportional to the magnitude of the resistors in the bias network (i.e., resistors R_1 and R_2 as shown in Figure 4.10).

The modulation sensitivity of the oscillator is not constant because of the non-linear relationship between the oscillation frequency and the input tuning voltage as shown in Figure 6.16. The modulation sensitivity of the VCO is assumed to be constant (i.e., independent of the input tuning voltage) in the linear theory of the PLL, which was discussed in Chapter 2 of this thesis. In timing recovery applications, the phase-locked loop normally operates at the desired timing clock frequency and does not deviate significantly from this operating point if the timing jitter is small. Therefore when designing the timing recovery PLL, an average value of K_0 can be assumed because the frequency deviation from the timing clock frequency will be small when the circuit is in-lock. However, in order to apply the linear PLL design and analysis methods some additional linearization circuitry may be required in order to reduce the dependence of K_0 on the absolute value of the tuning voltage.

The oscillator can also be frequency modulated by changing the bias current flowing through the differential pair of the logic inverter (inverter bias current tuning). This alters the propagation delay of the inverter circuit because the switching speed of the active devices changes as the inverter bias current varies. The output logic voltage swing (ΔV) changes in direct proportion to the change in bias current, which is a disadvantage of this tuning method. Variable load resistors could be implemented which would vary in inverse proportion to the inverter bias current, thereby maintaining a constant signal level at the inverter output [52]. However, the variable load resistors (which could be easily implemented using a MOSFET in a BiCMOS process) would reduce the bandwidth of the logic inverter and limit the maximum oscillation frequency of the circuit. Also, the design and layout of the oscillator would become more complex due to the additional circuitry and layout area required to implement the bias current dependent loads.

The effect of varying the differential pair bias current was simulated using a fixed logic voltage swing and the simulation results are shown in Figure 6.17. The value of the load resistance was chosen so that the maximum voltage swing at the output remained constant at 240 mV. The modulation sensitivity of the oscillation frequency to a change in bias current is about double the modulation sensitivity of the oscillator to changes in the emitter follower bias current. However, the total modulation bandwidth achievable with inverter

bias current tuning is lower than the modulation bandwidth that was achieved by varying the bias current flow through the emitter follower stages in the feedback network (about 300 MHz vs. 500 MHz bandwidth from HSPICE simulations using the nominal BiCMOS process parameters). The inverter bias current tuning curve is also monotonic and non-linear. A larger modulation bandwidth is possible if both the emitter follower and inverter bias currents are varied in order to change the oscillation frequency. It was not possible to independently vary the inverter bias current in the ring oscillator test circuit so the modulation curve shown in Figure 6.17 could not be experimentally verified.

Figure 6.17 : Inverting gate bias current modulation of the ring oscillator.

Long term frequency stability and manufacturability of the ring oscillator can be investigated by examining the dependence of the oscillation frequency (at a given bias

current) on changes in the power supply voltage, ambient temperature and process variables. The simulation results over a temperature range from 0 to 100 C are shown in Figure 6.18. The temperature behaviour of the polysilicon resistors in the BiCMOS process was not included in these simulations.

Figure 6.18 : Effect of temperature variation on the oscillation frequency.

The main effects of temperature on the transistor parameters are an increase in current gain (β), a decrease in the transconductance (g_m) and a decrease in the base-emitter voltage (V_{BE}). The oscillation frequency as a function of temperature (normalized to the frequency output at $T = 0$ C) follows an approximately linear relationship as shown in Figure 6.18. The simulation results predict a 5% change in the output frequency for a 100 degree change in junction temperature of the active devices. It would appear that the change in base-emitter voltage with temperature is responsible for the temperature dependence of the oscillator output. The base-emitter voltage of a bipolar transistor decreases almost linearly as the junction temperature of the device increases [22]. The total propagation delay time of the signal through the emitter follower stages in the feedback path of the ring oscillator is

small compared to the signal propagation delay time through the inverter stage. Therefore the temperature dependence of the inverter stage propagation delay largely determines the overall behaviour of the ring oscillator with changes in temperature. As the base emitter voltage of the emitter follower transistors in the feedback path of the oscillator decrease with increasing temperature, the d.c. bias voltage at the input to the logic inverter will increase (shift toward V_{CC}). This change in bias point causes an increase in the propagation delay of the inverter as the forward transit time and base-collector capacitances of the switching devices increase with the change in input bias (refer to the propagation delay analysis of the ECL inverter given in Chapter 4 of this thesis). Thus the oscillation frequency drops as the temperature increases. Compensating the change in bias voltage with temperature could improve the frequency stability of the oscillator. A thermal chuck for the circuit probing apparatus was not available, so the behaviour of the ring oscillator with variations in temperature could not be experimentally verified.

The change in oscillation frequency caused by a 10% change in the power supply voltage ($V_{CC}-V_{EE}$) is illustrated in Figure 6.19. The change in supply voltage causes only a slight change in the bias currents and a small change in the parasitic capacitances of the active devices, because the inverter differential pair and the 4X-size emitter followers in the feedback network are biased by current sources. The emitter followers at the outputs of the logic inverter are biased by a single resistor, and therefore any change in power supply voltage will modulate the current through these followers and change the output frequency.

However, further simulations of the circuit using a current source to bias these followers did not show a significant change in the results. The main cause of the change in output frequency as the supply voltage varies, is the dependence of the collector-to-substrate capacitance of the current source transistors on the substrate bias (V_{EE}). As the magnitude of V_{EE} is increased, the parasitic capacitance from the collector to the substrate of the current source transistor decreases, which increases the output impedance of the transistor current source. This reduces the propagation delay of the signal through the feedback network and results in an increase in the oscillation frequency. The change in frequency with changing supply voltage is significant (about 80 MHz/Volt change in the supply voltage) and it is approximately linear. This modulation of the output frequency which could arise from noise or other power supply disturbances is undesirable and should be minimized if possible.

Figure 6.19 : Effect of power supply variation on oscillator frequency.

The measured change in oscillator frequency for a change in power supply voltage, which is shown in Figure 6.19, is about 200 MHz/Volt, which is 2.5 times larger than supply sensitivity predicted by HSPICE, however, the relationship is still approximately linear. This indicates that the output impedance of the current sources is lower in the actual circuit than predicted by the simulator, which increases the sensitivity of the circuit to variations in the power supply voltage.

The frequency modulation characteristic of the oscillator for the worst-case and best-case device parameters was also simulated. Processing variations cause device parameters such as current gain (β), junction capacitances, and the unity-gain frequency (f_T) to change from lot to lot of fabricated circuits. For example, the β of an npn transistor can vary by a factor of two. The worst-case transistor model reflects the process extreme which results in larger parasitic capacitances, higher extrinsic resistances, higher leakage currents, and lower current gain than the nominal device model. The best-case transistor model has lower junction capacitances, lower extrinsic resistances, lower leakage currents, and higher current gain than the nominal model. As a result, the worst-case devices are slower than the nominal transistors and the best-case devices outperform the nominal transistors. The simulations of the phase-shift oscillator modulation characteristic for the worst-case, best-case, and nominal device parameters are compared in Figure 6.20. A large change in the

oscillation frequency was observed, which cannot be accommodated for by adjusting the bias current through the emitter followers using the tuning input voltage, V_t . Also, the modulation sensitivity (i.e., slope of the modulation characteristic curve) changes with process variations although the shape of the three curves are similar.

A tuning range of almost 2 GHz would be required to cover the anticipated change in frequency due to process, temperature, and supply variations. The modulation bandwidth of the oscillator could be widened by changing the bias current in all three emitter followers and the differential amplifier. However, the entire range of oscillation frequency due to process variation could not be accommodated. Also, a large modulation sensitivity leads to an increase in the phase noise at the oscillator output, due to an increase in the circuit sensitivity to any noise at the modulation input of the oscillator. Rejecting the working circuits which fall outside the desired frequency range would severely limit the circuit yield. Therefore a practical (i.e., manufacturable) circuit must be desensitized to process variations in order to fabricate circuits which will perform to a desired specification.

Figure 6.20 : Effect of process variation on the modulation characteristics of the VCO.

The phase noise at the output of the ring oscillator test circuit was also measured. Noise voltages and currents generated by active and passive devices modulate the signal produced by the oscillator and appear as phase noise at the circuit output. The simplest technique for measuring oscillator noise is to measure the oscillator frequency spectrum using a spectrum analyzer. Noise measured in this way will usually require a number of correction factors in order to obtain the oscillator phase noise, which is defined as

$$\text{phase noise} = \frac{\text{corrected noise per unit bandwidth at } f_m}{\text{carrier power}} \quad (6.13)$$

The phase noise is given by the ratio of the corrected noise power per unit (i.e., 1 Hz) bandwidth at a given measurement frequency (f_m) to the carrier or fundamental signal power. It is most often quoted in decibels (i.e., in dBc/Hz).

Corrections to the signal power measured on a spectrum analyzer are required in order to compensate for effects of the analyzer's signal processing circuitry on the oscillator output spectrum [57, 60]. The signal detector in a spectrum analyzer is usually not a true rms detector and therefore a correction factor must be applied to determine the correct signal power. Bandpass filtering in the analyzer is not an ideal square bandpass shape and thus the filter shape as well as the actual filter bandwidth must be accounted for in order to determine the noise power per unit bandwidth.

The spectral analysis technique is only useful when the noise produced by the oscillator under test is much larger than the internal local oscillator of the spectrum analyzer, because it is impossible to identify the source of noise components in the measured frequency spectrum. Also, it is impossible to tell whether the power at different frequencies in the measured spectrum is produced by amplitude or phase fluctuations when measured with a spectrum analyzer. The phase-shift ring oscillator operates in saturation which limits amplitude fluctuations in the oscillator output and therefore it will be assumed that the noise sidebands in the measured spectrum are mainly due to oscillator phase fluctuations.

A Rohde and Schwarz model FSB spectrum analyzer was used to measure the phase noise of the ring oscillator. The FSB spectrum analyzer has a single-sideband phase noise measurement feature which applies the appropriate correction factors to the measured

frequency spectrum and it will display the corrected phase noise measured at the desired frequency offset from the fundamental or carrier signal. A plot of the measured frequency spectrum for the phase-shift ring oscillator test circuit is shown in Figure 6.21. The corrected phase noise at the output of the oscillator for a frequency offset of 100 kHz from the fundamental signal frequency of 632 MHz was -58.4 dBc/Hz. The phase noise produced by the front-end local oscillator in the FSB spectrum analyzer is far below this level (specified at -107 dBc/Hz, with the instrument settings shown in Figure 6.21 [61]) and therefore the error introduced in the measurement by the spectrum analyzer local oscillator can be considered negligible.

A correction factor must be applied in order to determine the phase noise at the oscillator output, because the frequency divider circuit lowers the frequency of the measured signal while the phase variation in the signal remains unchanged [58]. Thus the phase noise at the ring oscillator output will be

$$\begin{aligned}\text{oscillator phase noise} &= \text{measured phase noise} + 20 \log_{10}(\text{divide ratio}) \quad (6.14) \\ &= (-58.4) + 20 \log_{10}(4) = -46.4 \text{ dBc/Hz}\end{aligned}$$

A typical hybrid VCO designed for operation in the 2 to 3 GHz range of frequency (i.e., the Avantek VTO-8200 oscillator) has an output phase noise of approximately -90 dBc/Hz at a 100 kHz offset from the carrier [62]. The ring oscillator phase noise performance is considerably poorer than the present state-of-the-art in low-cost hybrid VCOs, but it is likely that some improvements in the performance of this simple monolithic ring oscillator can be realized. The effect of a poor quality connection between the frequency divider and the output buffer cannot be simply evaluated, but it is likely that some degradation in the quality of the output spectrum was caused by the modifications to the interconnect metallization.

There are other factors which also contribute to the noise level at the oscillator output. The minimum size bipolar devices are well suited to digital logic applications where fast switching at low values of collector current is desired in order to limit circuit power dissipation. However, these small area devices have poorer $1/f$ and thermal noise performance than larger area bipolar devices [63, 64]. Therefore it would be possible to reduce the circuit noise produced by the active devices by using larger area transistors; the

Figure 6.21 : Measured frequency spectrum of the phase-shifting ring oscillator test circuit.

penalty for a reduction in noise is an increase in current required to bias the larger devices and the resultant increase in the oscillator power dissipation.

The ECL inverter circuit acts as a limiting amplifier which restricts the amplitude of the oscillator output. This non-linearity increases the amplitude of phase noise components at frequencies close to the fundamental output signal of the oscillator. A means for controlling the amplitude of the oscillator output and reducing the circuit non-linearity (such as automatic gain control or AGC) would help to reduce the phase noise at the oscillator output. However, a substantial increase in circuit complexity and design effort would be required to implement such a scheme.

The signal-to-noise ratio at the oscillator output could be improved by increasing the signal amplitude. The dynamic range of the oscillation signal is limited by the emitter followers in the feedback network to about 1 Volt p-p for the present ring oscillator design. Therefore only a small improvement in performance could be realized by increasing the signal amplitude with the present design. It should also be noted that an increase in signal amplitude will cause a reduction in the maximum frequency of oscillation of the circuit.

The oscillator output can be modulated by any noise present on the power supply connections to the test chip. The digital frequency divider and output buffer circuits contribute power supply noise as a result of current transients, such as current switching in emitter followers. The noise contributed by the activity of the other circuits on the test chip cannot be measured, however, the modulation sensitivity of the ring oscillator to supply variations is quite large (200 MHz/Volt from experimental measurements) and therefore improved isolation of the oscillator circuit could reduce phase noise in the oscillator output caused by power supply variations.

Another reason for the poor phase noise performance of the ring oscillator is the lack of selectivity in the feedback network. The phase response of the emitter follower circuits in the feedback network changes slowly as the frequency of the oscillation signal varies and therefore the oscillator is easily modulated by circuit noise sources. Some modifications to the basic ring oscillator which could improve the selectivity of the active feedback network, and possibly result in an improvement in the phase noise performance of the phase-shift oscillator will be considered in the next section of this chapter.

6.6 Modified Phase-Shift VCO

The phase-shift ring oscillator circuit topology was selected for investigation in this study because it is capable of oscillation at frequencies in excess of 2 GHz. However, the sensitivity of the phase-shift oscillator to variations in active device parameters and temperature limits the potential applications. The objective of this section is to outline some modifications to the basic oscillator design which could reduce the sensitivity of the circuit to variations in the manufacturing process and possibly improve the oscillator performance.

The active feedback network of the phase-shift oscillator (i.e., the emitter follower) will be examined in detail. Linear analysis techniques will be used to predict and optimize the performance of the emitter follower. Reducing the oscillator sensitivity to changes in device parameters, ambient temperature and power supply voltage is one of the main objectives of this study. Also, minimization of the oscillator phase noise through the control of the feedback network frequency response will be investigated. An output frequency greater than 1 GHz is still the design goal for applications such as high-speed timing recovery in fibre-optic networks, frequency synthesizers and portable radio receivers.

6.6.1 Emitter Follower Feedback Circuit

The emitter follower feedback circuit performs two functions in the phase-shift oscillator. It alters the phase of the output signal of the inverting amplifier by the amount required to sustain oscillations (a phase shift of slightly less than 180 degrees). The feedback network also provides the level shifting required to properly interface the inverting stage output and input ports. The total phase shift around the feedback loop can be adjusted by changing the bias current of the emitter followers, thereby controlling the frequency of the oscillator output. It was shown in the previous section that the change in oscillation frequency caused by the expected variations in device parameters exceeds the modulation bandwidth of the monolithic VCO. A small-signal analysis of the emitter follower circuit will be used to predict the feedback network performance as a function of the circuit parameters. This information can then be used to design and optimize the feedback network for the desired operating frequency, and possibly improve the oscillator stability with respect to variations in circuit parameters and processing.

6.6.2 Small-Signal Model

The small-signal (a.c.) model of a single transistor emitter follower is shown in Figure 6.22. The low frequency response of the emitter follower circuit has been analyzed by many authors [22, 36]. The effect of C_μ on the response of the circuit can be neglected at low frequency, and the capacitive loading (C_L) is also usually ignored in the analysis. However, the effect of the load capacitance on the circuit performance is often significant and cannot be ignored at higher frequencies. The transfer function for the simplified circuit is given as [36]

$$A_v(s) = \frac{V_{out}}{V_{in}} = A_{v0} \frac{1 - \frac{s}{z1}}{1 - \frac{s}{p1}} \quad (6.15)$$

Figure 6.22 : Linear small-signal model of an emitter follower.

where

$$A_{v0} = \frac{R_E (1 + \beta_0)}{r_b + r_{\pi} + (1 + \beta_0) R_E} \approx 1.0, \text{ assuming } \beta_0 R_E \gg r_b + r_{\pi} \quad (6.16)$$

$$z_1 = - \frac{g_m}{C_\pi} \approx - \omega_T \quad (6.17)$$

$$p_1 \approx - \frac{R_E \omega_T}{R_E + r_b} \quad (6.18)$$

ω_T is the unity gain frequency of the transistor, in rads/s.

β_o is the small signal current gain.

This simple model predicts a pole which lies at a lower frequency than the zero (although for a small base series resistance, $p_1 \approx z_1$). The low frequency gain (A_{VO}) is nearly unity if $(1+\beta_o)R_E \gg (r_b + r_\pi)$, which is usually the case.

Grebene [22] has also calculated the output impedance of the emitter follower circuit shown in Figure 6.22. For the condition

$$\frac{1}{g_m} < r_b \quad (6.19)$$

the output impedance of the follower can be approximated by the equivalent circuit shown in Figure 6.23, where

$$R_1 = \frac{1}{g_m} + \frac{r_b}{\beta_o} \quad (6.20)$$

$$R_2 = r_b \quad (6.21)$$

$$L = \frac{r_b}{\omega_T} \quad (6.22)$$

A large transconductance (g_m) is necessary to satisfy condition (6.19) and also to reduce R_1 . The transconductance is given by the ratio of the transistor bias current to the thermal voltage (which is constant at a given temperature), and so the transistor bias current must be large enough to obtain the desired transconductance.

If the emitter follower is driving a capacitive load, the inductive output impedance and load capacitance (C_L) will form a resonant circuit, therefore an underdamped response is possible. Peaking of the emitter follower frequency response is undesirable in most applications because it causes excess phase shift and transient instability in the output response. However, the resonant circuit formed by the emitter follower driving a capacitive load could be used to optimize the frequency response of the phase-shift oscillator feedback network. The rapid change in the phase response of a second-order circuit with frequency will increase the frequency selectivity of the feedback network and reduce the oscillator phase noise. This would result in a significant improvement in the phase stability of the ring oscillator VCO.

Figure 6.23 : Circuit model of the emitter follower output impedance [22].

Resistors R_1 and R_2 shown in Figure 6.23 degrade the quality factor (Q) of the resonant circuit formed by the inductor (L) and the load capacitance (C_L). Quality factor is defined as the ratio of the resonant frequency to the -3 dB bandwidth of the parallel resonant circuit. The Q -factor is lowered by energy dissipation in the resistors R_1 and R_2 . Increasing the resistance in series with the base (r_b) will tend to increase the resistor R_2 and improve the resonant circuit Q . However, the dissipation of the inductor (R_1) is also directly proportional to r_b , although the effect of an increase in the series base resistance on R_1 is reduced by the small-signal current gain of the transistor (see eq. 6.20). Therefore there is an optimum base resistance which will maximize the Q and minimize the -3dB bandwidth of the resonant circuit.

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The simplified analysis of the emitter follower at low frequencies does not predict an underdamped circuit response because the load capacitance (C_L) is excluded from the small-signal model. Also, the low frequency analysis of the emitter follower does not account for the effect of the collector-base feedback capacitance (C_μ), which shunts some of the base signal to ground at higher frequencies. The transfer function of the emitter follower circuit including the collector-base parasitic capacitance and a capacitive load has been derived in Appendix 1. The resulting transfer function is of the form

$$A_v(s) = \frac{V_{out}}{V_{in}} = \frac{A_{vo} (1 - z_1)}{\left(\frac{s}{\omega_{ef}}\right)^2 + \frac{2\zeta_{ef}}{\omega_{ef}} s + 1} \quad (6.23)$$

where A_{vo} and z_1 have been defined previously and ω_{ef} is the undamped natural frequency, which is given by

$$\omega_{ef}^2 = \frac{g_m}{r_b(C_\pi C_L + C_\mu C_L + C_\pi C_\mu)} \quad (6.24)$$

and ζ_{ef} is the damping factor

$$\zeta_{ef} = \frac{\omega_{ef}}{2} \left[\frac{(C_\pi + C_L)}{g_m} + r_b \left(C_\mu + \frac{C_\pi}{g_m R_E} + \frac{C_L}{1 + \beta_o} \right) \right] \quad (6.25)$$

Assuming that the load and collector-base capacitances are equal to zero reduces equation 6.23 to the low frequency transfer function given by equation 6.15.

A pole-zero analysis of the single emitter follower circuit shown in Figure 6.24 was performed using the HSPICE circuit simulator. The results of the circuit simulation and the theoretical calculations using equation 6.23 are summarized in Table 6.2.

Figure 6.24 : Emitter follower circuit configuration used for pole/zero analysis.

Table 6.2 : Comparison of simulated and calculated pole-zero locations for the circuit of Figure 6.24.

HSPICE pole-zero analysis		Theoretical calculation (eq. 6.23)	
Poles, in GHz	Zeros, in GHz	Poles, in GHz	Zero, in GHz
$9.4 \pm j5.01$	8.09	$9.9 \pm j5.0$	7.97
81.7	65.6	-	-

The higher order poles and zeros found by computer simulation are caused by circuit elements in the HSPICE bipolar transistor model which are not accounted for in the simplified equivalent circuit shown in Figure 6.22 (i.e., extrinsic collector and emitter resistances, collector-to-substrate parasitic capacitance, etc.). The dominant poles and zeros are predicted by the simplified model, and the calculated results compare favourably with the dominant poles and zeros found by computer simulation. It should be noted that the dominant pole lies at a higher frequency than the dominant zero, contrary to the predictions of the low frequency analysis. The inductive output impedance of the emitter follower interacts with the load capacitance producing an underdamped response to transient inputs. This effect is undesirable in logic circuits and is usually suppressed by adding a small damping resistor between the load (R_{CO}, C_L in Figure 6.24) and the emitter contact of the transistor, or by increasing the area of the bipolar transistor in order to decrease the base resistance, r_b .

An underdamped frequency response is desirable for the feedback network of the phase-shift oscillator. It was shown in section 6.2.4 of this chapter that the feedback network transfer function is one of the key factors which determines the phase stability of an oscillator. Within the bandwidth of the feedback circuit, the frequency deviation at the oscillator output ($\Delta\omega_{osc}$) is related to the phase uncertainty at the amplifier input by the slope of the phase response, or

$$\Delta\omega_{osc} = \frac{\Delta\theta_{in}}{\partial\theta/\partial\omega} \quad (6.26)$$

For a small frequency deviation at the oscillator output, the phase slope ($\partial\theta/\partial\omega$) must be large. The slope of the phase response for a second-order lowpass transfer function is inversely proportional to the damping coefficient (ζ) [65]. Therefore the stability of the phase-shift oscillator can be improved by minimizing the damping coefficient (ζ_{ef}) of the capacitively loaded emitter follower.

The phase response of a single emitter follower circuit (such as the circuit shown in Figure 6.24) due to the complex conjugate poles can be written as

$$\theta_p(\omega) = - \arctan \left[\frac{(2\zeta_{ef}/\omega_{ef}) \omega}{1 - (\omega/\omega_{ef})^2} \right] \quad (6.27)$$

The slope of the phase response is largest when the excitation frequency (ω) is equal to the natural resonant frequency, ω_{ef} . Therefore it is desirable to design the oscillator for operation at a frequency close to ω_{ef} , where the phase shift contributed by each emitter follower stage will be equal to almost ninety degrees, since the transfer function is second order. Thus only two emitter follower feedback stages are required to achieve a phase shift of 180 degrees. The effect of the zero at the transistor unity gain frequency (f_T) on the feedback network phase shift will be slight if the oscillator is operating at 1 GHz, because the zero at the unity gain frequency (approximately 8 GHz, from Table 6.2) will be almost a decade higher. The phase shift caused by the feedback network zeros will be offset by the effect of the dominant pole in the inverting stage. Therefore the oscillation frequency will be close to the undamped natural frequency of the feedback emitter follower, ω_{ef} .

It can be shown that the first derivative of the phase response at frequency ω_{ef} is given by the equation [65],

$$\frac{\partial \theta}{\partial \omega} = - \frac{1}{\zeta_{ef} \omega_{ef}}, \text{ at } \omega = \omega_{ef} \quad (6.28)$$

and the slope of the phase response is minimized by minimizing the damping coefficient, ζ_{ef} .

6.6.3 Minimizing Damping Coefficient (ζ_{ef})

The damping coefficient of the capacitively loaded emitter follower circuit is given by equation 6.25 in terms of the circuit parameters of the small-signal model. For a given base resistance (r_b , which includes any source resistance), equation 6.25 can be rewritten in the form

$$\zeta_{ef} = \left[\frac{A}{\sqrt{r_b}} + \frac{\sqrt{r_b}}{B} \right] \cdot \left[\frac{g_m}{4 (C_\pi C_L + C_\mu C_L + C_\pi C_\mu)} \right]^{\frac{1}{2}} \quad (6.29)$$

where

$$A = \frac{C_\pi + C_L}{g_m} \quad (6.30)$$

$$B = \left(C_\mu + \frac{C_\pi}{g_m R_E} + \frac{C_L}{1 + \beta_o} \right) \quad (6.31)$$

The optimum base resistance ($r_{b \text{ opt}}$) which minimizes the damping coefficient can be found by setting the first derivative of equation 6.29 equal to zero and solving for $r_{b \text{ opt}}$

$$\frac{\partial \zeta_{ef}}{\partial r_b} = - \frac{A}{2(\sqrt{r_b})^3} + \frac{B}{2\sqrt{r_b}} = 0 \quad (6.32)$$

and

$$r_{b \text{ opt}} = \frac{A}{B} \quad (6.33)$$

The optimum base resistance can now be found by substitution for the constants A and B in equation 6.33, which gives the result

$$r_{b \text{ opt}} = \frac{C_{\pi} + C_L}{g_m \left(C_{\mu} + \frac{C_{\pi}}{g_m R_E} + \frac{C_L}{1 + \beta_o} \right)} \quad (6.34)$$

As the load capacitance (C_L) on the emitter follower increases, the optimum base resistance which minimizes the damping coefficient (ζ_{ef}) also increases. For a given set of circuit parameters, the relationship between the load capacitance and optimum base resistance can be determined using equation 6.34, and a sample plot of this relationship is shown in Figure 6.25 for a 4X bipolar transistor in the BiCMOS process. Worst-case device

Figure 6.25 : Optimum base resistance versus load capacitance for a single 4X emitter follower circuit.

parameters were assumed for the device and the small-signal model parameters were computed assuming an emitter current of 1600 μA and a base-collector bias voltage of -1 Volt. It should be noted that for small values of load capacitance the relationship is approximately linear. However, as the load capacitance becomes significantly larger than the base-emitter capacitance of the transistor (C_π in eq. 6.34), the optimum base resistance approaches a limiting value which is approximately equal to r_π of the bipolar transistor.

The output frequency of the oscillator will also be affected by the choice of base resistance and load capacitance. Assuming that the phase shift introduced by the inverting gain stage is small so that the desired oscillation frequency (ω_{osc}) is approximately equal to ω_{ef} and using the result from equation 6.24 gives

$$r_b \cdot C_L \approx \frac{g_m}{\omega_{\text{osc}}^2 C_\pi}, \text{ for } C_\pi, C_L \gg C_\mu \quad (6.35)$$

Capacitances C_π and C_L are at least an order of magnitude greater than the parasitic capacitance C_μ for the designs considered in this study. Therefore the error made by neglecting the effect of C_μ will be small. For the 4X bipolar transistor biased by a 1600 μA current source (see Figure 6.26) and operating at an frequency ω_{ef} (assumed equal to ω_{osc}) of 1.3 GHz, the time constant given by equation 6.35 is given by

$$r_b \cdot C_L = 0.632 \text{ ns} \quad (6.36)$$

This time constant corresponds to an optimum base resistance of approximately 670 Ohms and a load capacitance of 950 fF from the plot shown in Figure 6.25. The performance of the single emitter follower circuit shown in Figure 6.26 was simulated for three values of base resistance (r_b) at a load capacitance of 950 fF. The amplitude response of the circuit is shown in Figure 6.27 (note that the base resistance is equal to the extrinsic base resistance of the transistor plus the external resistor, R_b , in Figure 6.26). The peak gain of the circuit (3.8 dB) occurs at 1.07 GHz and the peaking of the transfer function is maximized for a total base resistance of 670 Ohms. A phase lag of 90 degrees between the output and input occurred at 1.302 GHz, which is within 0.2% of the design value of 1.3 GHz.

Figure 6.26 : Circuit configuration used to demonstrate the effect of base resistance on the transfer function of an emitter follower.

Increasing the resistance in series with the base of the emitter follower has two advantages. It maximizes the slope of the phase response with respect to frequency ($\partial\theta/\partial\omega$), which increases the phase stability of the oscillator when the emitter follower is used as a feedback circuit. Also, the additional resistance in series with the extrinsic base resistance of the transistor helps to reduce the effects of processing variations on the performance of the circuit. This of course assumes that the tolerance of the additional base resistance, R_b , is less than the tolerance of the extrinsic base resistance. Thin film resistors or resistor trimming could be used to reduce the tolerance of the monolithic resistor, R_b .

A disadvantage of increasing the base resistance is the additional noise penalty arising from the thermally generated noise of the resistor itself, and the noise contribution of shot noise present on the base current which will flow through the resistor. The phase noise spectrum of an oscillator at small frequency offsets from the carrier is dominated by low frequency ($1/f$) noise sources. Improving the oscillator phase stability by increasing the frequency selectivity of the oscillator feedback network (i.e., increasing $\partial\theta/\partial\omega$) will reduce the effect of low frequency noise, improving the quality of the oscillator. The increase in broadband noise caused by an increase in base resistance is therefore offset by the benefit of an increase in the frequency selectivity of the feedback network. The selection of the base resistance which optimizes the oscillator noise performance is an area which should be addressed through further study.

Figure 6.27 : Effect of varying base resistance on the magnitude response of a single emitter follower stage driving a capacitive load.

6.6.4 Effect of Emitter Current on ω_{ef}

The emitter bias current (I_{EE}) can affect the circuit parameters of the bipolar transistor and alter the phase delay of the emitter follower. This effect was used to control the oscillation frequency of the test VCO discussed in section 6.5 of this chapter. The relationship between the phase response and the emitter bias current of the capacitively loaded emitter follower circuit will be examined in order to predict the oscillation frequency as a function of bias current. The magnitude response of the emitter follower is also affected by the emitter bias current. This will also be investigated.

The undamped natural frequency (ω_{ef}) of a single emitter follower driving a capacitive load is given by equation 6.24. Assuming that only a small additional phase shift is caused by the dominant pole of the inverting amplifier in the oscillator positive feedback loop, the oscillator will operate at a frequency (ω_{osc}) close to ω_{ef} , given by

$$\omega_{osc}^2 \approx \frac{1}{r_b \cdot C_L \left(\frac{C_\pi}{g_m} \right)}, \text{ for } C_\mu \ll C_\pi, C_L \quad (6.37)$$

The effect of C_μ on the oscillation frequency is negligible because the load and the base-emitter capacitances (C_L and C_π) are both at least an order of magnitude larger in a practical circuit. The base-emitter capacitance can be expressed as the sum of the diffusion and depletion capacitances

$$C_\pi = C_D + C_{je} = g_m \tau_f + C_{je} \quad (6.38)$$

where

C_D is the diffusion capacitance of the emitter-base junction.

C_{je} is the capacitance of the emitter-base junction depletion layer.

τ_f is the base transit time of the transistor in the forward active region.

g_m is the transconductance of the bipolar transistor.

The transconductance of the bipolar transistor is defined as the ratio of the emitter current (I_{EE}) to the thermal voltage

$$g_m = \frac{I_{EE}}{V_T} \quad (6.39)$$

where V_T is the thermal voltage, in Volts

Equations 6.38 and 6.39 can be combined with equation 6.37 to give

$$\omega_{osc}^2 \approx \frac{1}{r_b \left(\tau_f + \frac{C_{je} V_T}{I_{EE}} \right) C_L} \quad (6.40)$$

At large emitter currents the diffusion capacitance (related to τ_f) is much greater than the depletion capacitance and equation 6.40 can be simplified to

$$\omega_{osc}^2 \approx \frac{1}{r_b \tau_f C_L} \quad (6.41)$$

which is insensitive to changes in the emitter current, I_{EE} , since there is a range of emitter current over which the forward transit time, τ_f , does not strongly depend upon I_{EE} . This explains the decrease in the modulation sensitivity of the test oscillator at large emitter currents (see section 6.5.2 of this thesis, Figure 6.16). For low emitter currents, the diffusion capacitance decreases and the oscillation frequency can be modulated by the change in the term $(C_{je} V_T / I_{EE})$ with emitter current (see equation 6.40). The non-linearity in the oscillator frequency control characteristic at low emitter currents is also immediately apparent from examination of equation 6.40.

The poles of the emitter follower transfer function (see equation 6.23) can be written as

$$s_1, s_2 = -\zeta_{ef} \omega_{ef} \pm j \omega_{ef} \sqrt{1 - \zeta_{ef}^2} \quad (6.42)$$

The locations of the poles in the complex plane are illustrated in the diagram of Figure 6.28. The magnitude of the emitter follower transfer function (ignoring the effect of the

zero at the unity gain frequency of the transistor) is inversely proportional to the lengths of the phasors M1 and M2. The magnitude of the transfer function is greatest when the phasor M1 is of minimum length, which occurs at

$$\omega = \omega_{ef} \sqrt{1 - \zeta_{ef}^2} \quad (6.43)$$

Figure 6.28 : Plot of the emitter follower dominant poles.

At this frequency the magnitude of the transfer function (again ignoring the effect of the zero) is given by

$$|A_v|_{\max} = \frac{1}{\zeta_{ef} \sqrt{4 - 3\zeta_{ef}^2}} \approx \frac{1}{2\zeta_{ef}}, \text{ for small } \zeta_{ef} \quad (6.44)$$

which is inversely proportional to the damping coefficient. Ignoring the effect of C_{μ} , the damping coefficient can be written in terms of the circuit parameters using the result of equation 6.25 as

$$\zeta_{ef} = \frac{\omega_{ef} V_T (C_\pi + C_L)}{2I_{EE}} \quad (6.45)$$

At large emitter currents the undamped natural frequency (ω_{ef}) is approximately constant (since $\omega_{osc} = \omega_{ef}$) and the maximum gain (A_v) will vary in direct proportion to the change in emitter current. However, at low emitter currents, ω_{ef} will also vary as I_{EE} changes, which causes a larger variation in the peak of the magnitude response with changing emitter current. This effect is illustrated in Figure 6.29 for four values of emitter current.

Thus at large emitter current the phase response is almost independent of changes in I_{EE} and the peak in the magnitude response is directly proportional to the emitter current. This is illustrated by the slight change in the peak gain between emitter bias currents of 1400 μA and 1600 μA in Figure 6.29. As the emitter current decreases, both the phase response and the peak gain of the emitter follower become proportional to the bias current, which results in a large shift in the frequency response (such as the shift between 200 μA and 400 μA emitter currents in Figure 6.29). Therefore the sensitivity of the circuit gain to a change in I_{EE} increases at lower emitter currents. Also, at low emitter currents the damping coefficient rises rapidly and the stability of the phase-shift oscillator is degraded. The emitter current should be kept large so that the damping factor of the resonant circuit is low, although the ability to tune the frequency of the oscillator by varying the bias current will be lost. However, it would be possible to vary the gain of the emitter follower at the resonant frequency by changing the emitter bias current.

6.6.5 Effect of Temperature and Process Variations

The variation of the undamped natural frequency due to the strong temperature dependence of the thermal voltage (V_T), and changes in the depletion capacitance of the base-emitter junction (C_{je}) with temperature can be minimized by making the emitter current large. However, the parameters r_b , τ_f , and C_L , which determine the oscillation frequency at high emitter bias currents also exhibit some temperature dependence which must be characterized.

The base resistance is composed of the external resistor (R_b in Figure 6.26) and the extrinsic base resistance of the transistor (r_{bx}). The resistor temperature coefficient depends upon the fabrication process used. Both implanted and diffused resistors have a

Figure 6.29 : Emitter follower magnitude response as a function of emitter current.

significant positive temperature coefficient (1000 to 4000 ppm/°C) and an absolute value tolerance of about ± 20 percent [22]. An external resistor which is stable with both temperature and process variations could be fabricated using thin film technology, however, thin film resistors are not available in most silicon BiCMOS processes. The advantages of thin film resistors are low temperature coefficient (± 100 ppm/°C) as well as low stray capacitance and tighter control of the absolute value (e.g., ± 5 % tolerance for NiCr thin film resistors) [22].

The temperature dependence of the forward transit time (τ_f) can be derived from consideration of the physics of the semiconductor device [35]. Therefore the behaviour of the transit time as a function of temperature can be modelled and characterized for a given device, and the effect of thermal variations in τ_f on the oscillator frequency determined. The transit time is also affected by the change in the d.c. bias of the emitter follower with temperature. The base-emitter voltage of the transistor decreases with increasing temperature, which causes the base-collector voltage to decrease because the collector is connected to a fixed potential (i.e., V_{CC}). Therefore the base widens as the base-collector voltage decreases which causes an increase in base transit time.

The load capacitance (C_L) will also exhibit a temperature dependence which depends upon the fabrication technology used. Monolithic capacitors generally have a weak positive temperature coefficient of capacitance and an absolute value tolerance between 10 and 30 percent [22]. A good quality capacitor is required (i.e., the capacitor must have a low dissipation factor) so that the Q-factor of the resonant circuit at the emitter follower output is not degraded.

Therefore as the ambient temperature rises, the parameters r_b , τ_f and C_L will all increase in value which will cause a decrease in the oscillation frequency as given by equation 6.41. The temperature dependence of each component can be characterized for a given process technology, and once the total temperature variation has been determined, compensation for the shift in oscillation frequency can be applied.

The undamped natural frequency of the emitter follower will also vary with changes in the semiconductor fabrication process. The three main parameters from equation 6.41 which determine ω_{ef} at high emitter bias currents will vary due to slight variations in the production process. Trimming of the base resistor, R_b , may be possible in order to

compensate for production tolerances. Also, the capacitance C_L could be made variable (e.g., a varactor diode) in order to allow adjustment of all or a portion of the load capacitance. The emitter bias current could also be varied to compensate for the change in oscillation frequency due to processing changes. Therefore it is possible to compensate for processing variations by trimming any or all of the circuit parameters R_B , C_L and I_{EE} .

The fabrication of monolithic thin-film or polysilicon resistors and monolithic thin film capacitors (i.e., not junction capacitors) is independent of the processing steps used to fabricate the transistors. Therefore the fabrication of devices which correspond to either the worst or best-case parameter sets are unlikely to coincide with the worst case or best-case tolerances on the other monolithic components. A statistical approach to the analysis of parameter variations on the design (such as a Monte-Carlo analysis) might give a more realistic projection of the impact of process variability on the circuit performance and yield. This approach is suggested for further investigation in this area.

6.7 Summary

The RC oscillator circuits which could be used to implement a high frequency monolithic VCO have been reviewed, and the ring oscillator configuration was selected as the basis for a 1 GHz design. The noise mechanisms in ring oscillators were treated by analogy to the tuned circuit oscillator (Leeson's model) and the regenerative feedback (i.e., signal feedback is not continuous in time) oscillator models. The phase noise enhancement caused by positive feedback was discussed and the dependence of the phase noise on the feedback transfer function and the circuit non-linearity was outlined.

Two ring oscillator topologies (the phase-shift and 2-inverter oscillators) that are suitable for high frequency operation were compared. The phase-shift ring oscillator was chosen as the basis for a test circuit in order to demonstrate the high frequency capability of the bipolar devices fabricated in the BiCMOS process.

The results of HSPICE circuit simulations and some limited measurement on the ring oscillator test circuit were then presented and discussed. The number of samples available to test were limited by an error in the original circuit layout, however, some useful results were obtained from the experimental measurements. An output frequency range between

2.25 and 2.65 GHz was measured, which was about 10% lower than the frequency range predicted by the circuit simulator. It was suggested that this difference was mainly due to circuit resistor values that were higher than expected, which increased the phase delay of the signal inverting stage of the circuit and reduced the oscillator bias currents. The modulation characteristics predicted by HSPICE were confirmed by experimental measurements for modulation of the bias current flow in the active feedback stages of the oscillator.

The behaviour of the phase-shift oscillator with variations in junction temperature and circuit processing were investigated using the circuit simulator. It was shown that the oscillator stability with changes in process parameters, temperature, and power supply voltage requires some improvement in order to ensure a satisfactory yield of circuits which can meet the desired specifications.

The oscillator output spectrum was also measured. The sensitivity of the oscillation frequency to fluctuations in the supply voltage, which was quite large (200 MHz/Volt), caused some degradation in the measured circuit performance. A number of other factors that were not carefully considered in the design of the test circuit also contributed to the noise level at the oscillator output. Additional testing is required in order to properly identify the dominant sources of circuit noise and completely characterize the circuit performance.

The high level of phase noise present at the output of the test oscillator would be unacceptable for the application intended in this thesis, which is timing recovery in a long-haul data transmission system. VCO frequency or phase instability outside of the loop bandwidth cannot be controlled by the feedback action of the phase-locked loop. The loop filter bandwidth requirement for a timing recovery PLL is on the order of 10 kHz or less, and the measured phase noise at frequency deviations from the carrier above 10 kHz is quite large. The noise components in the test oscillator output spectrum which cannot be tracked by the PLL will result in timing jitter at the loop output that will severely degrade the performance of a digital transmission link.

A modification to the active feedback network was described which could improve the oscillator stability and performance. The behaviour of the capacitively loaded emitter follower circuit was analyzed and it was shown that a resonant peak in the frequency

response exists, which is caused by a feedback interaction between the follower load capacitance and the resistance in series with the base of the bipolar transistor. The feedback network of the phase-shift oscillator can therefore be realized by connecting two capacitively loaded emitter follower circuits in series, which eliminates one of the emitter follower stages used in the test oscillator design. By selecting the appropriate load capacitance and base resistance for each follower circuit, the transfer function of the feedback network can be altered to improve the performance of the oscillator by increasing the slope of the phase response.

Some further investigation will be required in order to establish the benefits and limitations of this proposal. There are a number of design issues which must be addressed, such as interfacing the feedback network to the inverting amplifier stage of the oscillator, investigating the large-signal behaviour of the capacitively loaded emitter follower, and methods of frequency modulating and trimming the oscillator output frequency. The complete phase-shift oscillator circuit must be analyzed in order to predict the operating point, modulation bandwidth, and the variation of the oscillation frequency with changes in process parameters and temperature.

7. Conclusions and Recommendations

The design, simulation and experimental characterization of high frequency integrated circuits fabricated in a sub-micron silicon BiCMOS technology have been investigated in this thesis. A number of test circuits have been fabricated which have demonstrated the feasibility of producing digital and analog circuits capable of operating at frequencies in the low-GHz range. The proposed application for these circuit designs is a monolithic timing recovery circuit capable of operation at a clock rate above 1 GHz. Although the complete monolithic timing recovery circuit described in this thesis was not demonstrated experimentally, the preliminary results presented in this study may encourage further work in this area.

7.1 The Timing Recovery PLL

The constraints on the design of the timing recovery PLL are unique, and tight design requirements are placed on the loop bandwidth and the free-running stability of the voltage-controlled oscillator. These restrictions make complete monolithic integration of an analog circuit which can meet the desired specifications a difficult challenge with the present state-of-the-art in monolithic circuit technology. Long-time-constant filtering, which is difficult to achieve on-chip with a continuous-time filter circuit, can be implemented using discrete-time or digital filtering techniques. The binary quantizing PLL structure could be used as the basis for a high frequency PLL circuit because only one-bit quantization of the input phase error is required, which increases the operating bandwidth of the PLL phase detector. A hybrid analog/digital PLL architecture was proposed for implementation of a timing recovery circuit in BiCMOS technology intended for long-haul transmission applications. The binary quantizing phase detector and the analog voltage-controlled oscillator were identified as the key high frequency components required for this application. The design and characterization of a monolithic phase detector and a voltage-controlled oscillator were then considered.

7.2 The Phase Detector

A phase detector circuit designed in silicon bipolar technology which is based upon the ECL latching comparator circuit was described in Chapter 4 of this thesis. The propagation delay characteristics of the ECL inverter circuit were studied, and an equation describing the propagation delay was developed using the HSPICE circuit simulator through a sensitivity analysis of the circuit. The resulting equation was used to optimize the design of the inverter circuit, and the design criteria developed for the inverter circuit were applied to the design of the ECL latching comparator circuit and a binary quantizing phase detector. The characterization and optimization of other high-speed circuit topologies using sensitivity analysis and circuit simulation is recommended for further study. The results of such a study could be applied to optimization of transistor layouts and the fabrication process as well as high-speed digital circuit design.

A binary quantizing phase detector consisting of serially connected ECL latching comparators was designed and simulated. The simulations showed that single-bit quantization of the input phase relationship between a 1 Gbit/s non-return-to-zero (NRZ) coded data stream and a 1 GHz timing clock could be achieved. The output pulses produced by the phase detector were well-defined with little glitching, even at small phase errors between transitions in the clock and data signals. However, some additional pulse conditioning may be required in order to properly interface the phase detector to a digital filter circuit. The effects of voltage offsets and device noise were not considered, but these effects should be studied within the context of the overall PLL design.

The accuracy of the phase measurement made by the phase detector was shown to be related to the slew rate of the clock and data input signals. Circuit simulations showed that the measurement accuracy could be optimized by adjusting the amplitude of the received data signal. Experimental verification of the simulation results through the characterization of a test circuit would be a useful step in the future development of the timing recovery PLL.

The maximum clock rate for the phase detector was determined to be 2.4 GHz in simulation. A high-speed D-type flip-flop test circuit was used to demonstrate the performance capabilities of the ECL latching comparator fabricated in a BiCMOS process. The predictions made by computer simulation were verified by experimental measurements,

and the measurement results provided an experimental validation of the device models. An alternating 1-0 data pattern was applied to the flip-flop D-input which was synchronized up to a maximum clock rate of 5.3 GHz, although the full logic voltage swing at the output was not achieved at that clock frequency. Computer simulations showed that the maximum operating frequency of the circuit for a pseudorandom data input was limited by the bandwidth of the output buffer circuit. This behaviour was consistent with the experimental observations. Therefore it is expected that the circuit performance could be further improved by some refinement of the experimental circuit.

7.3 The Voltage-Controlled Oscillator

The feasibility of implementing a monolithic voltage-controlled oscillator (VCO) which could be used in a timing recovery PLL was investigated through the study of two monolithic microwave components (the spiral microstrip inductor and a broadband amplifier) and a monolithic ring oscillator circuit. The study of these components provided some performance benchmarks for the BiCMOS process. The results of this study have shown that it is possible to realize passive monolithic inductors which do not suffer significant losses from the conductive substrate, for excitation frequencies up to 3 GHz. Also, a broadband amplifier with a low frequency gain of 11.1 dB and a -3 dB bandwidth greater than 3.4 GHz was fabricated in the silicon BiCMOS process. The development of a linear microwave VCO utilizing a passive LC feedback network is recommended as an area for further development in this area.

The gain and bandwidth achieved by the broadband amplifier fabricated in BiCMOS technology has demonstrated that the amplification requirements of an oscillator circuit designed for operation in the GHz frequency range can be realized. The performance of the BiCMOS broadband amplifier is comparable to the performance which can be achieved in other pure bipolar technologies. A low-noise amplifier design for the linear oscillator and other radio frequency applications is recommended for further study and development.

The measured behaviour of the microstrip inductors fabricated in the BiCMOS process was close to ideal over the lower RF range (i.e., 100 MHz - 3 GHz), and the low quality-factor (Q) of these inductors was shown to be almost entirely due to the limited thickness of the top conductor metallization. Therefore it is possible that good quality microstrip components could be realized in silicon BiCMOS technology, however, a considerable

amount of study and experimentation is still required in this area. The component dimensions and process technology must be optimized in order to improve the performance of the inductors to the point where these components can be used in the design of higher quality circuits. This will require an understanding of the high frequency behaviour of the microstrip transmission line fabricated in the Si-SiO₂ system and the effect of processing parameters such as oxide layer thickness and substrate doping on the performance of the transmission line. The accuracy of the computer-aided design algorithms used to design and analyze the microstrip inductor appears to be adequate, however, more effort is required in the area of component modelling for circuit design purposes.

The development of a design and fabrication capability in microstrip components on silicon could be applied to a variety of applications. Microstrip transformers and couplers are two examples of components which could be used in the implementation of feedback networks for low-noise amplifiers, input and output coupling circuits, and in the design of low-noise RF and microwave mixers. However, the effect of the conductive substrate on component isolation is one issue which must be addressed if microstrip components and active circuits are to be successfully integrated.

An alternative to the linear microwave oscillator for the implementation a monolithic VCO is the resistor-capacitor or RC oscillator circuit. A number of design alternatives for a monolithic VCO implementation were examined in Chapter 6 of this thesis, and the phase-shift ring oscillator configuration was selected as the basis for a design capable of operating at GHz frequencies. The noise mechanisms in ring oscillators were treated by analogy to the tuned circuit oscillator and the regenerative feedback oscillator models. These models provided some qualitative criteria which can be applied to the design of a monolithic oscillator, however, further investigation into the quantitative effects of circuit noise sources on the phase noise at the ring oscillator output is necessary. Relating the results of Leeson's and the regenerative oscillator noise models would be an interesting area for further investigation.

The performance of a phase-shift oscillator test circuit was investigated using circuit simulation and some experimental measurement. The test circuit was originally designed as a demonstration of the frequency capability of the bipolar devices in the BiCMOS process; low phase noise at the oscillator output was not a major design objective for the test circuit.

However, the test results established some bounds on the circuit performance which could be improved in future designs.

An output frequency range between 2.25 and 2.65 GHz was measured for the phase-shift ring oscillator test circuit. The modulation characteristics and the effect of supply variations on the oscillation frequency were predicted by the circuit simulator and compared to the circuit measurements. Close agreement between the measured and predicted results was not found, however, a wide variation in circuit performance was expected due to tolerances in circuit fabrication and a number of other possible sources of error were identified.

The high level of phase noise measured at the output of the test oscillator is unacceptable for the timing recovery application. It was also shown through simulation that the oscillator stability with changes in process parameters, temperature, and power supply voltage requires some improvement in order to make the circuit manufacturable. The phase noise performance of the test oscillator design could be improved by applying some low-noise design principles to this circuit, such as improving the circuit isolation and minimizing the $1/f$ noise in the active devices.

A modification to the emitter follower feedback network of the phase-shift ring oscillator was proposed which could also improve the performance of the circuit. It was shown that the capacitively loaded emitter follower circuit exhibits a resonant peak in the frequency response which is caused by a feedback interaction between the load capacitance and the resistance in series with the base of the bipolar transistor. The slope of the feedback network phase response can be increased through the proper selection of circuit components, which leads to an improvement in the frequency stability of the phase-shift oscillator. The theoretical study of the capacitively loaded emitter follower circuit was verified through the use of circuit simulation, but there are still many design issues which must be addressed in order to develop a manufacturable VCO circuit design. The complete oscillator circuit must be analyzed in order to predict the operating point, modulation bandwidth, and the variation of the oscillation frequency with changes in process parameters and temperature. Further study in this area may also lead to other applications for the modified emitter follower circuit, such as monolithic RF filtering.

The capabilities of an advanced silicon BiCMOS process have been demonstrated in both high-speed digital and high frequency analog circuit applications. The ability to combine

these types of circuits with the high density and low power circuit capabilities of CMOS technology, offers unique opportunities in the area of timing recovery design and the design of other high frequency circuits and systems.

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APPENDIX 1 : Frequency Response of the Emitter Follower

Figure A1-1 : Small-signal model of an emitter follower.

The small-signal circuit model of the emitter follower is shown in Figure A1-1. A Thevenin equivalent circuit of the input source (v_{in}) and components r_b and C_μ will have the following parameters :

$$v_{th} = \frac{v_{in}}{1 + s\tau_i} \quad (A1-1)$$

$$Z_{th} = r_b \parallel \frac{1}{sC_\mu} = \frac{r_b}{1 + s\tau_i} \quad (A1-2)$$

The output voltage is developed by the emitter current flowing through the load Z_L , which can be written as

$$v_o = (g_m + 1/Z_\pi) V \cdot Z_L \quad (A1-3)$$

The voltage developed across the base-emitter impedance (Z_π) is determined by Kirchoff's voltage law as

$$-v_{th} + i_b Z_{th} + V + v_o = 0 \quad (A1-4)$$

and

$$V = \frac{v_{th} Z_\pi}{Z_\pi + Z_{th} + (g_m Z_\pi + 1) Z_L} \quad (A1-5)$$

by substitution for the base current (i_b) and v_o from equation A1-3. Substitution of equation A1-1 into A1-5 for v_{th} results in the following expression for the voltage gain

$$A_v = \frac{v_o}{v_i} = \frac{Z_L (g_m Z_\pi + 1) / (1 + s\tau_i)}{Z_\pi + Z_{th} + (g_m Z_\pi + 1) Z_L} \quad (A1-6)$$

where

$$Z_L = R_E \parallel C_L$$

$$Z_\pi = r_\pi \parallel C_\pi$$

Z_{th} is given by equation A1-2.

The numerator of equation A1-6 can be re-written as

$$N(s) = \frac{R_E (1 + g_m r_\pi) (1 - s/z_1)}{(1 + s\tau_i)(1 + s\tau_\pi)(1 + s\tau_L)} \quad (A1-7)$$

and

$$z_1 = \frac{1 + g_m r_\pi}{\tau_\pi} \approx \omega_T$$

$$\tau_i = C_\mu r_b$$

$$\tau_L = C_L R_E$$

$$\tau_\pi = C_\pi r_\pi$$

The denominator of equation A1-6 can be written in the form

$$D(s) = \frac{As^2 + Bs + C}{(1+s\tau_i)(1+s\tau_\pi)(1+s\tau_L)} \quad (A1-8)$$

The terms A, B, and C, in equation A1-8 are given by

$$A = r_b(\tau_\pi\tau_L) + r_\pi(\tau_i\tau_L) + R_E(\tau_\pi\tau_i) \quad (A1-9)$$

$$B = r_b(\tau_\pi + \tau_L) + r_\pi(\tau_i + \tau_L) + R_E(\tau_\pi + \tau_i) + g_m r_\pi R_E \tau_i \quad (A1-10)$$

$$C = r_b + r_\pi + R_E + g_m r_\pi R_E \quad (A1-11)$$

By definition

$$\omega_{ef}^2 = \frac{C}{A} \quad (A1-12)$$

$$\zeta_{ef} = \frac{\omega_{ef} B}{2C} \quad (A1-13)$$

The d.c. gain is given by the ratio of equations A1-7 and A1-8 at $s = 0$, which is

$$A_{vo} = \frac{R_E(1+g_m r_\pi)}{C} = \frac{(1+\beta_o)R_E}{r_b + r_\pi + (1+\beta_o)R_E} \quad (A1-14)$$

since $g_m r_\pi = \beta_o$ by definition.

By substitution of equations A1-9 and A1-11 into A1-12

$$\omega_{ef}^2 = \frac{r_b + r_\pi + R_E + g_m r_\pi R_E}{r_b(\tau_\pi\tau_L) + r_\pi(\tau_i\tau_L) + R_E(\tau_\pi\tau_i)} \quad (A1-15)$$

For $(1+g_m r_\pi)R_E = (1+\beta_o)R_E \gg r_b r_\pi$, which is normally the case, equation A1-15 can be simplified to

$$\omega_{ef}^2 = \frac{1+\beta_o}{r_\pi r_b (C_\pi C_L + C_\mu C_L + C_\pi C_\mu)} \quad (A1-16)$$

but $(1+\beta_o)/r_\pi = g_m$ and so A1-16 can be re-written as

$$\omega_{ef}^2 = \frac{g_m}{r_b (C_\pi C_L + C_\mu C_L + C_\pi C_\mu)} \quad (A1-17)$$

The ratio of equations A1-10 and A1-11 is

$$\frac{B}{C} = \frac{r_b(\tau_\pi + \tau_L) + r_\pi(\tau_i + \tau_L) + R_E(\tau_\pi + \tau_i) + g_m r_\pi R_E \tau_i}{r_b + r_\pi + R_E + g_m r_\pi R_E} \quad (A1-18)$$

Assuming that

$$(1+g_m r_\pi) R_E = (1+\beta_o) R_E \gg r_b + r_\pi$$

$$C_L R_E \gg r_b C_\mu$$

$$C_\pi r_\pi \gg r_b C_\mu$$

equation A1-18 can be simplified to

$$\frac{B}{C} = \frac{r_b(C_\pi r_\pi + C_L R_E) + r_\pi(C_L R_E) + R_E(C_\pi r_\pi) + g_m r_\pi R_E \tau_i}{R_E(1+g_m r_\pi)} \quad (A1-19)$$

and for $g_m r_\pi \gg 1$:

$$\frac{B}{C} = \left[\frac{(C_\pi + C_L)}{g_m} + r_b \left(C_\mu + \frac{C_\pi}{g_m R_E} + \frac{C_L}{1+\beta_o} \right) \right] \quad (A1-20)$$

From equation A1-13

$$\zeta_{ef} = \frac{\omega_{ef}}{2} \left[\frac{(C_\pi + C_L)}{g_m} + r_b \left(C_\mu + \frac{C_\pi}{g_m R_E} + \frac{C_L}{1+\beta_o} \right) \right] \quad (A1-21)$$

END

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