10

Resolution Test Chart Labels:

- 1.0
- 1.1
- 1.25
- 1.4
- 1.6
- 1.8
- 2.0
- 2.2
- 2.5
- 2.8
- 3.2
- 3.6
- 4.0

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A High-Speed CMOS Dual-Modulus Frequency Divider for Mobile Radio Frequency Synthesizers

by

NAVID FOROUDI, B.Sc.

**A thesis submitted to the Faculty of Graduate Studies and Research
in partial fulfillment of the requirements for the degree of**

Master of Engineering

Department of Electronics

Carleton University

Ottawa, Ontario

November 1991

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submitted by Navid Foroudi, B.Sc.
in partial fulfillment of the requirements for
the degree of Master of Engineering

Thesis Supervisor

Chair, Department of Electronics

Carleton University

January 1992

Abstract

The design of a high-speed CMOS dual-modulus frequency divider, meant to be used as a component in a single-chip frequency synthesizer which is a part of a mobile communications system, is described. Latches instead of flip-flops have been used in the construction of the frequency divider to achieve high operating frequency. The divider (divide-by-15/16) has been fabricated with both 3 and 1.2- μm -gate-length technologies, the one fabricated with the 1.2- μm -gate-length process operating at 1.4 GHz with 12.7 mW power consumption.

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Symbols and Abbreviations

0-volt reference, GND
Supply voltage, V_{dd}
Resistor
Adjustable resistor
Capacitor
p-channel MOS transistor
n-channel MOS transistor
Inverter
Buffer
AND
OR
NOR
A logic block with an edge-triggered input

ac Alternating current

Amp Amplifier

BICMOS		Bipolar-CMOS
BNC		Bayonet nut coupling
CMOS		Complimentary metal-oxide semiconductor
CT2		Cordless Telephone – Second generation digital
DAC		Digital-to-analog convertor
dc		Direct current
DDS		Direct digital synthesis
DECT		Digital European Cordless Telephone System
DQPSK		Differential quadriphase-shift keying
FDMA		Frequency-division multiple access
GaAs		Gallium-Arsenide
GMSK		Gaussian minimum shift keying
GSM		Groupe Speciale Mobile
IS-54		Electronics Industry Association Interim Standard 54
PLL		Phase-locked loop
Poly		Polysilicon
RF		Radio frequency
rms		Root-mean-square
ROM		Read-only memory
SRAM		Static random-access memory
TDMA		Time-division multiple access
VCO		Voltage-controlled oscillator

Chapter 1

Introduction

Today's technology makes it possible to plan for a universally available cordless mobile communications system. However, several problems have to be overcome, one of which is to implement a special frequency synthesizer as a key component in mobile transceivers. This thesis is a step in that direction.

Chapter 2 provides an introduction to frequency synthesis techniques for mobile radio. Popular frequency synthesizers are examined in the search for an appropriate technique for a monolithic high-frequency high-resolution synthesizer. The fractional-division phase-locked loop is selected as the best option. The dual-modulus frequency divider, a block of the fractional-division phase-locked loop, is studied in Chapter 3 and the expected characteristics from such a divider are introduced. Different frequency division techniques are also compared. Chapter 4 concentrates on the speed factor in frequency dividers. Problems facing the designer and possible ways to overcome them are explored, and a novel high-speed

dual-modulus frequency divider design proposed. The test results for the two fabricated dividers are reported in Chapter 5. Chapter 6 presents a review and conclusion of the thesis.

Chapter 2

Mobile Radio Frequency Synthesizer

A block diagram of a typical hand-held terminal [1] is shown in Figure 2.1. The frequency synthesizer generates the RF frequency needed by the radio section for frequency conversions to (transmitter) and from (receiver) the carrier band. Frequency switching for the synthesizer is necessary every time a new carrier frequency is accessed. One occasion when this occurs is when the incoming signal quality degrades due to fading [2]. In that case, the synthesizer is switched to a channel which carries the same message with a stronger amplitude (for details refer to [2, pp. 117–120]). The communication on the new channel continues until the receiving signal begins to fade again, which makes the synthesizer switch once more to another channel.

A number of standards have been created for mobile communications, some of which are summarized in Table 2.1 [3, 4, 5].

Figure 2.1 Hand-held terminal block diagram.

Table 2.1 Summary of standards

	GSM	DECT	CT-2	IS-54
RF band (MHz)	935–960 890–915	1880–1900	864–868	869–894 824–849
Carrier spacing (kHz)	200	1728	100	30
Users per carrier	8	12	1	3
Multiple access	TDMA	TDMA	FDMA	TDMA
Modulation	GMSK	GMSK	GMSK	DQPSK

Using GSM as an example, the following requirements will have to be met by the frequency synthesizer of Figure 2.1:

- Maximum output frequency ≥ 960 MHz.
- Output frequency step ≤ 200 kHz.
- Frequency-switching time $\leq 30 \mu\text{s}$ (calculated from the information given in [3, 4]).

These figures suggest that a high-frequency high-resolution agile frequency synthesizer is needed. Since the hand-held communications systems will be battery operated, low power consumption is another requirement of the synthesizer. Monolithic implementation is essential for the reduction of power and cost.

In this chapter, different frequency synthesis techniques are reviewed in the search for the most suitable method for the application under discussion. The following desired characteristics comprise the basis for evaluation:

- Easy to implement on a single chip.
- High resolution.
- High output frequency.
- Pure output spectral.
- Short switching time.

According to how the synthesized output is related to the reference signal, frequency synthesis techniques can be divided into two general groups: direct synthesis and indirect synthesis.

2.1. Direct synthesis

In direct frequency synthesis, the output frequency is obtained directly from a reference frequency. This can be done by using mixers, frequency dividers, frequency multipliers and filters (Direct Analog Synthesis) [6, 7], as shown in Figure 2.2. Frequencies f_1 , f_2 and f_3 are derived from a reference frequency by generating a line spectrum, then using a bank of filters to select individual component frequencies. For the example shown:

$$f_o = f_1 + f_2/10 + f_3/100 \quad (2.1)$$

Direct analog synthesizers deliver fast frequency switching, fine resolution and spectral

Figure 2.2 Typical direct analog synthesis.

purity, but too much circuitry, including filters and mixers, makes them unattractive for monolithic integrated circuits.

Another type of direct frequency synthesis consists of generating a digital representation of the desired signal, using logic circuitry, and then using a digital-to-analog converter (DAC) to convert the digital representation to an analog waveform (direct digital synthesis) [8, 9]. Direct digital synthesis (DDS) uses the reference signal as its clock. An example of DDS is shown in Figure 2.3. The sinusoidal amplitude coefficients for successive phase

Figure 2.3 Direct digital synthesis.

increments are stored in the memory. In each clock cycle, which lasts $1/f_r$ seconds, K is added to the content of the accumulator so that a new location is addressed in the memory. If the memory contains one period of the sinusoid, then:

$$f_o = K/2^L f_r \quad (2.2)$$

Since most of the components in a direct digital synthesizer are digital, DDS is ideal for single-chip implementation. But since the synthesized frequency is always lower than the reference frequency, it is limited to relatively low frequencies. Even if the reference frequency is at the limit of the fabrication technology, the synthesized output frequency is limited to half of that value [4, 9, 10, 11, 12].

2.2. Indirect synthesis

Indirect frequency synthesizers derive the output frequency from a secondary oscillator locked to the reference frequency (phase-locked loop, Figure 2.4). The output frequency

Figure 2.4 Indirect frequency synthesizer.

of a voltage-controlled oscillator (VCO) is divided by a programmable divider, and then

applied to a phase detector which receives its other input from a reference oscillator (f_r). The dc component at the output of the phase detector (loop error) is passed to the VCO through a low-pass filter. This error signal adjusts the frequency of the VCO until the divider output and reference signals have the same phase and frequency. In this lock condition, the VCO output frequency f_o relates to the reference frequency f_r by $f_o = N f_r$. The phase-locked loop (PLL) configuration shown in Figure 2.4 is the conventional single-loop synthesizer (for details and more references refer to [8]). The output frequency is varied (programmed) by changing the division ratio N . The output frequency step is equal to the reference frequency.

2.3. High-resolution PLL frequency synthesizers

The frequency resolution of the synthesizer of Figure 2.4 can be increased (smaller frequency steps) by reducing the reference frequency. However, a low f_r will require a narrow loop bandwidth which increases the settling time [6, p. 36]. Further, since a PLL is a low-pass filter with respect to the reference signal noise, and a high-pass filter with respect to the VCO noise [13], a wider loop bandwidth is desirable so that more of the VCO noise will be eliminated. These characteristics of the PLL force us to raise the reference frequency to the maximum possible value since a fast acquisition time and short-term stability are required. As a result, there is a trade-off between high resolution and short settling time in the synthesizer of Figure 2.4.

Two possible techniques for increasing the resolution of an indirect frequency synthesizer without decreasing its reference frequency are presented in the following sections.

2.3.1. Multiloop synthesizer

A multiloop synthesizer is shown in Figure 2.5 [14]. Mixers are used to combine two PLLs. Each mixer and the filter which follows it is shown as one block to simplify the

Figure 2.5 Multiloop frequency synthesizer.

diagram. Standard frequencies f_{r1} , f_{r2} and f_{r3} can all have a common origin. The output frequency can be calculated from:

$$f_o = f_{r3} + N_1 f_{r1} - N_2 f_{r2} \quad (2.3)$$

If $f_{r1} = 9.9$ kHz, $f_{r2} = 10$ kHz and $f_{r3} = 99$ MHz, then: $f_o = 99\text{MHz} + N_1 9.9$ kHz $- N_2 10$ kHz.

N_1 and N_2 can be changed by programming the dividers. In other words, the frequency step is equal to 100 Hz while the lowest reference frequency in the circuit is 9.9 kHz. A multiloop synthesizer offers higher resolution as compared to a single-loop synthesizer; however, it includes mixers and filters which complicate its monolithic implementation.

2.3.2. Fractional-division loop

Once again we look at the conventional synthesizer of Figure 2.4. If it were possible to increment N in fractional steps, such as setting $N=10.5$ or 10.000001 , the step frequency of f_o could be made arbitrarily small. A digital counter (divider) cannot perform a true fractional division; however, a method will be discussed which enables a digital divider to provide a fractional relationship between f_o and f_r . The programmable divider of the conventional synthesizer is replaced with a dual-modulus frequency divider, as shown in Figure 2.6. This divider divides by N or $N+1$ when the modulus control signal is at logic

Figure 2.6 Fractional-division loop.

0 or logic 1 respectively. By changing the division ratio between N and $N+1$ alternatively, the average division ratio will be somewhere between N and $N+1$.

It is possible to control the division ratio of the divider using a digital accumulator¹ [8, p. 308], as shown in Figure 2.7. An L -bit accumulator is clocked by the output of the frequency divider. Every time the accumulator overflows (modulus control is at logic 1), the divider divides by $N+1$, otherwise it divides by N . The input to the accumulator, K ,

1. A digital accumulator used for this application is sometimes referred to as a "phase accumulator".

Figure 2.7 Fractional-division loop using an accumulator as the modulus controller.

determines the fractional part of the average division ratio. For example, assume that the divider can divide by 10/11, and L equals 3 (three-bit accumulator). The sequence of a complete cycle for $K=5$ is listed in Table 2.2.

Table 2.2 Accumulator contents and division ratios ($k=5$)

Cycle #	Accumulator content	Carry	Division Ratio
1	0	1	11
2	5	0	10
3	2	1	11
4	7	0	10
5	4	1	11
6	1	1	11
7	6	0	10
8	3	1	11
Repeat from cycle #1			

The average division ratio is: $(11+10+11+10+11+11+10+11)/8 = 10.625$, therefore:

$$f_o = 10.625f_r.$$

The fractional part of the average division ratio is equal to the average number of ones in the carry output, which is given by

$$F = K/2^L \quad (2.4)$$

All the possible values of K for a 3-bit accumulator and the corresponding average division ratios are listed in Table 2.3.

Table 2.3 Accumulator inputs and resultant division ratios

K:	0	1	2	3	4	5	6	7
F:	0	1/8	1/4	3/8	1/2	5/8	3/4	7/8
f_o/f_r:	10	10.125	10.25	10.375	10.5	10.625	10.75	10.875

The frequency step is equal to $f_r/2^L$. Higher resolution can be achieved by increasing the accumulator length, L . For example, using a 20-bit accumulator with a 10-MHz f_r results in a 1-Hz frequency step.

The accomplished fractional division technique, causes phase jitter to appear at the output of the frequency divider. Each division by N or $N+1$ phase leads or phase lags the output of the frequency divider with respect to the pure reference signal. These phase fluctuations are detected by the phase detector and appear at its output. Since the order of the division ratios, selected by the phase accumulator, has a repetition cycle (8 in the example of Table 2.2), the phase jitter at the output of the frequency divider is periodic too. These components, in turn, modulate the VCO and create spurious components around the carrier (for a detailed explanation refer to [8, pp. 305–311]). Since the frequency of the components at the output of the phase detector can be as low as the minimum step (for prime ratios of K and 2^L), a relatively narrow loop bandwidth is required to eliminate them. However,

reducing the loop bandwidth results in a longer settling time [6]. Several techniques have been proposed in the literature for compensating for the phase-noise caused by the fractional division [15]. Among them, digiphase is a well-established method [8].

2.3.2.1. Digiphase

It can be shown that the information needed to compensate for the unwanted components at the output of the phase detector, in Figure 2.7, is available in the phase accumulator [8, pp. 305–311]. That information can be used to generate a canceling waveform, which may be subtracted from the phase detector output before it is applied to the loop filter to eliminate the VCO phase modulation [16]. Figure 2.8 shows the block diagram of the complete

Figure 2.8 Digiphase fractional-N PLL.

synthesizer employing digiphase for phase noise compensation. A digital-to-analog converter is used to provide the analog representation of the phase accumulator content, which is required for the compensation. A disadvantage of this technique is that the time available

to the digital-to-analog converter for each conversion is equal to the period of the reference signal. For some applications, it might be difficult to implement a DAC capable of operation at the frequency range of interest.

The maximum output frequency of a fractional-division loop is equal to the maximum operating frequency of the divider, which is much higher than what is achievable using DDS. The resolution is a function of the phase accumulator length, while the switching speed is controlled by the loop bandwidth. Since these two parameters are independent, both high resolution and short acquisition time can be obtained.

2.4. Summary

The frequency synthesizer properties are summarized in Table 2.4.

Table 2.4 Frequency synthesis technique comparisons

	Direct Analog	Direct digital	Integer-division loop	Multiloop	Fractional-division loop
Monolithic implementation	difficult	✓	✓	difficult	✓
Maximum frequency	✓	low	✓	✓	✓
Resolution	✓	✓	Trade off	✓	✓
Settling time	✓	✓		✓	✓

It should be mentioned here that the choice of the fractional-division phase-locked loop over the other techniques has been made due to the specific requirements of the application. Although neither fractional and integer-division loops are considered difficult for monolithic implementation, integer-division loop has a simpler construction and might be preferred

for an application which does not require both high resolution and fast switching speed. Also, direct digital and fractional-division loop synthesizers are both considered to have high enough switching speeds for the mobile radio, but direct digital synthesis is much faster and might be preferred for an application which does not require a very high output frequency. In conclusion, the fractional-division PLL has been selected as the best technique among the other popular frequency synthesizers because it can most closely satisfy all the requirements of the mobile radio. If designed carefully, the spurious outputs can be eliminated and a high-resolution, agile, high-frequency synthesizer achieved.

The next chapter provides an introduction to the frequency division in the fractional-division PLL context.

Chapter 3

Frequency Dividers

In Chapter 2 it was established that the fractional-division PLL is the most suitable technique for the mobile radio frequency synthesizer. This was based on the requirements for such a synthesizer with regard to resolution, noise level, switching speed and frequency range. One of the PLL components which directly affects these factors is the dual-modulus frequency divider. This chapter is concerned with the system-level design constraints and limitations of dual-modulus frequency dividers for the fractional-division PLL synthesizer.

The frequency divider with its interconnections to the rest of the synthesizer is shown in Figure 3.1. The frequency divider provides the phase detector with a signal, in phase with the VCO, whose frequency is a divisor of the VCO frequency. The phase detector compares this input with the reference and generates the necessary correction signal for the VCO. The division ratio of the divider is selectable between N and $N+1$ by applying the appropriate value to its modulus control input (MC in Figure 3.1). A logic 0 on MC makes the divider

Figure 3.1 Dual-modulus frequency divider inside the loop.

divide by N and a logic 1 makes it divide by $N+1$. MC is fed by the modulus controller which is clocked by the output of the frequency divider. The input of the divider is the output of the synthesizer (f_o in Figure 3.1). Throughout the text, when the frequency divider is considered alone, its input and output frequencies are called f_{in} and f_{out} .

3.1. Dual-modulus frequency divider function

A frequency divider for the mobile radio fractional-division PLL synthesizer should satisfy several conditions including: high operating frequency, reasonable power consumption, low noise and ease of implementation. However, the functionality of such a synthesizer depends on the satisfaction of the following requirements by the divider:

- Having two division ratios, with a difference of one, selectable by the user.
- Phase coherency of the output signal.
- Allowing the user to select the division ratio for every output cycle.
- Having a high operating frequency.

3.1.1. Division ratios

Assuming that the frequency divider divides by N and $N+M$,

$$f_o = (N + MF) f_r \quad (3.1)$$

where F is the average number of ones in a cycle of the MC signal, applied by the modulus controller to the divider. In that case the step frequency at the output of the synthesizer is

$$\Delta f_o = M f_r \Delta F \quad (3.2)$$

It is obvious that, keeping the other parameters constant, $M=1$ gives the highest possible resolution (smallest step frequency). As a result, to have high resolution, a difference of one is desirable between the two division ratios of the divider.

3.1.2. Phase coherency of the output signal

The output of the divider, as shown in Figure 3.1, is applied to a phase detector. The divider must feed back not just the VCO frequency, but its phase as well. In order to have valid phase information fed back to the phase detector, the frequency change at the output of the divider, which results from the division ratio switching, must be phase coherent.

3.1.3. Division ratio selectability

As shown in Figure 3.1, the output of the divider is used to clock the modulus controller. As a result, the modulus controller generates a new MC after each output cycle. If the new value is different from the previous one, the divider must change its division ratio accordingly. In other words, the divider must update its division ratio once every output cycle.

3.1.4. Operating frequency

The highest frequency present in a PLL synthesizer is the VCO output frequency. The only other loop component which has to work with this high frequency is the frequency

divider (Figure 3.1). This limits the output frequency of the synthesizer to the maximum operating frequency of the divider. Even if the VCO is capable of generating higher frequencies, the loop will not operate at frequencies higher than the maximum operating frequency of the divider. Therefore, in order to synthesize a frequency in the GHz range, a GHz-range frequency divider is required.

3.2. Frequency division techniques

There are two general types of frequency dividers. One is based on regenerative frequency division and the other on digital frequency division.

3.2.1. Regenerative frequency dividers

Figure 3.2 shows the block diagram of a regenerative frequency divider [17]. In the

Figure 3.2 General concept of regenerative frequency division.

steady-state condition, the frequency at the input of the amplifier is the same as its output frequency. Therefore

$$f_{in} - f_{out} = f_{out} \Rightarrow f_{out} = f_{in}/2 \quad (3.3)$$

In the fractional division scheme, the dual-modulus frequency divider is expected to update its division ratio once every output cycle. A regenerative frequency divider is incapable of doing that since it is a single-modulus frequency divider. Although regenerative frequency

dividers have very high operating frequencies [18], their construction is unsuitable for the fractional-division loop frequency divider.

3.2.2. Digital frequency dividers

A digital frequency divider is a synchronous sequential circuit¹ which is clocked by the input signal and a combination of its output variables used as the frequency divider output. A block diagram of a synchronous sequential circuit is shown in Figure 3.3 [19, p. 134].

Figure 3.3 A sequential system.

Flip-flops² are the memory devices of a sequential circuit. Since an asynchronous circuit has no clock pulse to control its operation [19, p. 220], it is incapable of operating as a frequency divider. In the remainder of this chapter, "synchronous sequential circuits" are referred to as "sequential circuits".

Counters are a class of sequential circuits that generally require no external input (primary input variables). In that case, the next state of the sequential circuit is only a function

1. The output of a sequential circuit at any instant is determined by the values of its inputs at that instant, as well as the previous values of the inputs.
2. In this thesis, a "flip-flop" is considered to be an edge-triggered device.

of its present state. The state diagram of such a sequential circuit is shown in Figure 3.4.

Figure 3.4 State diagram of a divide-by-4 counter and its corresponding waveforms.

Transition from one state to the next is initiated by the low to high transition of the clock.

If the clock is considered to be the input and Q1 is used as the output, $f_{out} = f_{in}/4$.

Digital frequency dividers are preferred because of their simplicity.

A dual-modulus frequency divider, however, requires a one-bit external input (modulus control or MC) which controls the division ratio. The state diagram of a dual-modulus counter is shown in Figure 3.5. If MC = 1, the divider divides by 4. If MC = 0, the counter

Figure 3.5 State diagram of a dual-modulus counter and its corresponding waveforms.

skips one of its states which results in a division by 3. As mentioned in the original

requirements for the frequency divider, it is possible to switch the modulus (division ratio) of the counter for every output cycle and the division ratio switching is phase coherent.

To successfully select the division ratio of the counter as shown in Figure 3.5, MC must be valid during state S3. This should be carefully verified when the division ratio of a counter is dynamically selected by other components in a circuit. Considering the delays present in a physical circuit, it is necessary to provide the counter with a valid MC from some time before the end of S3 to some time after the starting point of the following state. The timing window in each output cycle during which a valid MC is expected by the counter is one of the important parameters of that counter.

Flip-flops and gates can be arranged in various ways to implement a counter. Section 3.3 examines some of the simple counter styles which are suitable for high-speed frequency division.

3.3. Speed considerations

The maximum clock rate for a synchronous sequential system is determined by the sum of the following time intervals [20, 21]:

τ_1 = Setup time of a flip-flop.

τ_2 = Delay time of a flip-flop from clock to output.

τ_3 = Propagation delay time of any combinational circuit between the flip-flops.

In order to increase the maximum operating frequency, $(\tau_1 + \tau_2 + \tau_3)$ must be minimized.

3.3.1. Johnson counter

A Johnson counter (twisted ring counter [19] or shift counter [22]) is usually used in high-speed frequency dividers since there is no combinational circuit between the flip-flops in this counter ($\tau_3 = 0$). Figure 3.6 shows a Johnson counter used as a frequency divider.

Figure 3.6 Johnson counter.

If all the flip-flops in Figure 3.6 are reset before starting the operation,

$$f_{out}/f_{in} = 2n \quad (3.4)$$

Figure 3.7 shows a dual-modulus (3 or 4) Johnson counter.

$$\begin{aligned} MC=0 &\Rightarrow f_{out}/f_{in} = 3 \\ MC=1 &\Rightarrow f_{out}/f_{in} = 4 \end{aligned}$$

Figure 3.7 Dual-modulus counter.

A dual-modulus Johnson counter, however, needs combinational circuitry for the division ratio control. A Johnson counter is a good candidate for high-speed frequency division because the combinational circuitry needed between the flip-flops in this counter is minimal (none if it is single modulus) compared to other structures. This reduces the τ_3 delay and, by lowering the load of flip-flops, helps reduce the flip-flop delay τ_2 .

A single flip-flop can be used to assemble a twisted ring counter as shown in Figure 3.8.

Figure 3.8 Toggle flip-flop.

This divide-by-two counter (toggle flip-flop) is the fastest counter that can be constructed with a given flip-flop since all the physical connections to the flip-flop are bounded in a small area around it, minimizing the interconnect capacitances. Secondly, the clock signal is distributed in a small area to clock only one flip-flop. As a result, the clock load is minimized and the clocking circuit will have better (shorter) rise and fall times.

3.3.2. Ripple counter

One can use the output of a toggle flip-flop as the clock signal for another toggle flip-flop as shown in Figure 3.9.

Figure 3.9 Ripple counter.

This configuration is a “ripple counter”. The modulus of this counter is

$$f_{\text{out}}/f_{\text{in}} = 2^n \quad (3.5)$$

A ripple counter is in fact a serial combination of sequential circuits wherein the output of

each sequential circuit is used as the clock for the next sequential circuit. In general, if the clock of a flip-flop in a counter is supplied by the output of another flip-flop, the counter is referred to as an "asynchronous counter".

For an application requiring the settled values of the outputs simultaneously, the maximum operating frequency of a ripple counter is relatively low. However, for the application of frequency division with a modulus of 2^n which does not require a feedback in the system, only the settling time of the first flip-flop determines the minimum clock period. In that case, the operating frequency of the ripple counter is as high as that of a synchronous counter and it actually has some advantages. These include:

- The highest possible modulus (2^n where n is the number of flip-flops) with the least amount of circuitry (only n D flip-flops and no combinational circuits) is provided.
- High frequency is limited to a small portion of the circuitry which reduces the high-frequency noise induced on power supply lines and simplifies the layout.

Thus, an asynchronous counter is the best choice when a high-speed single-modulus frequency divider is needed [17, 23, 24, 25].

3.3.3. Higher division ratios

Dual-modulus frequency dividers with higher division ratios can be assembled by incrementing the number of flip-flops in the configuration of Figure 3.7. This, however, increases the number of inputs to the combinational circuit which results in an undesired longer delay (τ_3). To avoid this, the frequency division is usually performed using an asynchronous-counter style (see the previous sub section), as shown in Figure 3.10 [26, 27, 28, 29, 30, 31]. The first stage is a high-speed dual-modulus counter similar to the one shown in Figure 3.7 which can divide by P or $P+1$. The output of this stage is used to clock the second stage, a counter with a modulus of M . The output of the second stage is the output of the

Figure 3.10 A two-stage dual-modulus frequency divider.

divider. Since the construction of the first stage is not affected by this configuration, the maximum operating frequency of the combined divider is the same as that of the first stage. To keep the difference of one between the two final division ratios, feedback is needed from the second to the first stage. A simple combinational circuit detects one of the states of the second stage and during that state, determines the division ratio of the first stage according to the $N/N+1$ signal. During the other states, the first stage has a modulus of $P+1$ regardless of the $N/N+1$ value. The two division ratios of the two-stage frequency divider are thus $N+1=M(P+1)$ and $N=M(P+1)-1$. For this structure to be functional, the total delay of the second stage and the detector must be low enough so that the valid $P/P+1$ signal can reach the first stage on time (see Section 3.2.2). The maximum acceptable value for this delay is a function of the highest operating frequency and construction of the first stage. Since the clock frequency of the second stage is at least P times lower than the main input frequency, the second stage counter can have an operating frequency lower than that of the first stage. This simplifies the design and layout of the second stage and enables the designer to optimize the second stage for lower power consumption.

By using a programmable counter as the second stage, the division ratios of the divider

can be set to different pairs (e.g. 10/11, 20/21 and 40/41). This gives flexibility to the synthesizer so that it can be used with different reference frequencies.

3.4. Flip-flops

Flip-flops are used as memory devices of sequential circuits. An integrated D flip-flop circuit has the simplest construction in comparison to all the other types of flip-flops: this is due to its simple function, which can be summarized as follows. A D flip-flop propagates the logic value of the input D to the output Q at the time of a 0-to-1 clock transition (1-to-0 for a negative-edge-triggered flip-flop) and retains the value at Q until the next clock pulse triggers.

In this section, the transistor-level structures of some D flip-flops are presented and discussed.

One special type of D flip-flop responds to both transitions of the clock pulse [32]. A counter constructed with such a flip-flop counts the number of clock transitions and not the clock cycles. The division ratio of such a counter is half the division ratio of the same counter built with single-edge-triggered flip-flops. This characteristic of the double-edge-triggered flip-flop makes it inefficient for frequency division and it is not given further consideration in this thesis.

The schematic diagrams of the two most widely used CMOS dynamic flip-flops, conventional and clocked CMOS, are shown in Figures 3.11 and 3.12 respectively. High-speed counters are often built with dynamic flip-flops which have shorter setup and delay times relative to those of static flip-flops. Since such a counter cannot be clocked with very low frequencies, it has a minimum operating frequency. Each flip-flop is constructed from two

Figure 3.11 Conventional D flip-flop.

Figure 3.12 Clocked CMOS D flip-flop.

identical level-triggered D latches³, clocked with complimentary signals. As a result, the D flip-flop is edge-triggered. Complementary clocks are extracted from the main clock input to the flip-flop. There is another type of clocked CMOS D flip-flop (Figure 3.13) which has a reduced output voltage swing due to the charge sharing phenomenon [33, pp. 186–188], but may require less chip area [34]. The need for two non-overlapping clock signals in all these flip-flops makes them unattractive at high frequencies. The effect of skew on behavior

3. In this thesis, a “latch” is considered to be a level-triggered device.

Figure 3.13 Clocked CMOS D flip-flop with charge sharing.

of conventional and clocked-CMOS flip-flops is presented in [35].

A true single-phase-clock flip-flop [36, 37] is shown in Figure 3.14. Since this flip-

Figure 3.14 Single-phase-clock flip-flop.

flop operates with a single clock signal, it does not have skew problems.

In differential logic [38], the structure of Figure 3.15 is used as a flip-flop [26].

Figure 3.15 Differential-logic flip-flop.

3.5. Summary

It has been demonstrated how digital counters can be used for dual-modulus frequency division satisfying the requirements regarding division ratio values, phase coherence of the output and division ratio selectability. Speed was also considered and selected digital frequency dividers were compared. The frequency divider will be analyzed in more detail in the next chapter, with a detailed examination of the speed factor and its limitations. A novel design will be introduced which is believed to be faster than circuits reviewed in this chapter.

Chapter 4

The Divider Design

Frequency synthesizers for mobile radio systems consist of both low and high-frequency components which are usually fabricated with CMOS and GaAs or CMOS and bipolar technologies. Reported characteristics of selected high-speed multi-modulus frequency dividers are summarized in Table 4.1, confirming the high-speed capabilities of bipolar and GaAs technologies.

Table 4.1 High-speed multi-modulus frequency dividers

Technology	Division Ratios	Gate Length (μm)	Speed (GHz)	Consumed Power (mW)
HBT [39]	128–255	–	9.72	650
HBT [40]	4/5	–	15.5	1500
Si Bipolar [31]	128/129	–	1.6	63
GaAs [41]	10/11	0.7	2.4	15
GaAs [28]	128/129	0.5	2.5	90
GaAs [42]	252/256	1	3.7	180
CMOS [26]	128/129	0.5	2.06	45
CMOS [26]	128/129	0.4	4.2	95

If CMOS technology could be used to fabricate the high-frequency parts of the frequency synthesizer as well as its low-frequency parts, system integration on a single silicon substrate would be possible, and power dissipation, cost and development time could be significantly reduced.

To pursue high speed for CMOS integrated circuits, shorter-gate-length CMOS architectures are developed, offering higher integration density, lower power consumption and higher operating frequency. However, it is also possible to improve speed by using designs which can efficiently use a relatively conservative process to achieve higher speeds. A success in the latter, the main focus of the research presented here, enables us to fabricate ICs with higher operating frequencies at lower prices (less expensive processes). The challenge has been to explore novel circuit techniques which can fully exploit the capabilities of a given process.

This chapter focuses on the knowledge required to design a high-speed dual-modulus frequency divider. The key design goal is to increase the maximum operating frequency of the divider without compromising its stable operation so that it can satisfy the requirements defined in Chapters 2 and 3. A novel memory device is introduced to be used instead of the D flip-flops employed in conventional CMOS dividers. It will be shown that such a memory device, when used in a counter, results in higher operating speed. A complete divider design is presented along with its simulation results.

Appendix B summarizes the parameters of the two processes (CMOS3 DLM and CMOS4S) used for implementation of the frequency divider. The layouts generated for this design as well as the transistor sizes are shown in Appendix C.

4.1. Clock frequency limits

In order to successfully design a high-speed frequency divider, it is necessary to understand the factors limiting the maximum operating frequency (clock frequency) of a sequential circuit.

The functional block diagram of a cell in a sequential circuit with n flip-flops can be generalized as demonstrated in Figure 4.1. The input to a flip-flop is a combination of the

Figure 4.1 General form of a flip-flop and its interactions in a sequential circuit.

outputs from all the flip-flops and the primary inputs (Chapter 3). For a positive-edge-triggered flip-flop the clock signal activates Latch1 when it is at logic 0 and Latch2 when it switches to logic 1. To arrange that order, the clock signal of some flip-flops (clocked-CMOS or transmission-gate flip-flops) is connected to Latch2 and its complement to Latch1, where Latch1 and Latch2 are exactly the same. Alternatively, in some other flip-flops (true-single-phase-clock or differential-logic flip-flops) the construction of the two latches differs such that one of them is turned on when the clock is at logic 1 and the other when it is at logic 0 (Section 3.4). To keep our block diagram general and not limited to any specific type of flip-flop, the clock signal connections to the latches have not been shown

in the diagram.

As explained in the previous chapter, a D flip-flop has two phases of operation corresponding to each clock cycle. First, the value on the input D is stored in a memory device (latch). This function is performed when the clock is at its initial level. As a result of a clock transition, the second phase is initiated in which the value stored in the first memory device is loaded into the second memory device. The output of the second memory device is output Q of the flip-flop. As a result, in a D flip-flop, output Q shows the value which has been on input D at the time of the clock transition. Delays corresponding to these two periods are usually referred to as setup time (τ_1) and propagation delay (τ_2). After the new value has been transferred to the second memory device, the clock may go back to its initial value. After the flip-flop propagates the new value of Q to its output, an additional time interval (τ_3) is necessary before the next clock transition can take place. The period τ_3 is the time delay that combinational circuits take to evaluate their outputs, which in turn are the inputs of the flip-flops. Figure 4.2 shows the mentioned delays and their positions with respect to

Figure 4.2 Clock waveform at a relatively low frequency.

the clock waveform at a relatively low frequency. The delays, at the maximum operating frequency of the sequential circuit, are positioned as shown in Figure 4.3. It has been

Figure 4.3 The order of the delays at the highest operating clock frequency.

assumed that the clock-to-Q and D-to-Q delays of the first latch are both equal to τ_1 (for a detailed treatment of clocking schemes refer to [43]). Any further increase in the clock frequency will cause an overlap between τ_3 and τ_1 . In other words, the input to the flip-flop, which is delayed by $\tau_2 + \tau_3$ with respect to the rising edge of the clock, will not have been present at the input for a long enough time (τ_1) when the next triggering clock transition occurs. Thus, the proper operation of the sequential circuit can no longer be guaranteed. According to Figure 4.3, $T_{\min}$, the clock period corresponding to the maximum operating frequency, is given by

$$T_{\min} = (\tau_1 + \tau_2 + \tau_3)_{\max} \quad (4.1)$$

or

$$f_{\max} = \frac{1}{(\tau_1 + \tau_2 + \tau_3)_{\max}} \quad (4.2)$$

where τ_1 , τ_2 and τ_3 represent the delays occurred consecutively in the first latch, the second latch and the combinational circuit. In a circuit, different types of flip-flops might be used, each with different delays. The input to a flip-flop might come directly from the output of another flip-flop ($\tau_3 = 0$) while the input to another flip-flop in the same circuit might be

fed by a 4-input NOR gate ($\tau_3 > 0$). In any case, the longest possible sum of the three consecutive τ_1 , τ_2 and τ_3 , time intervals (worst case) has to be considered in Eq. (4.2).

4.1.1. Delays in a flip-flop

Let us analyze a flip-flop in detail and find the factors contributing to the time intervals τ_1 and τ_2 . In a clocked-CMOS flip-flop, each memory device is a clocked-CMOS latch.

Figure 4.4 Clocked-CMOS with charge sharing.

Currents passing through the transistors in a clocked-CMOS flip-flop and the corresponding timing diagrams are shown in Figure 4.4. Assuming there is a logic 0 at the input D, τ_1 will be the time that it takes for the series combination of the two p-channel transistors to charge node A (the dashed capacitors represent the gate and parasitic capacitances present on each node). During that period, current i_1 flows from V_{dd} to node A. Time interval τ_2 corresponds to the discharge of node Q through the two n-channel transistors (current i_2). In a circuit optimized for speed, an n-channel transistor has a higher transconductance than a p-channel transistor and the difference is intensified when series combinations are involved [33, pp. 38–39] [36, p. 66]. Therefore, delay τ_2 is shorter than delay τ_1 . Next,

consider the same flip-flop with a logic 1 at its input D. This time, delay τ_1 corresponds to the discharge time through a series combination of n-channels (i3), while τ_2 is the charging time through two p-channels (i4). For the same reason, this time τ_1 is shorter than τ_2 . This means that in general, a flip-flop has two sets of τ_1 and τ_2 timing values (setup and propagation delays), one corresponding to a logic 1 and the other one to a logic 0.

4.1.1.1. Differential-logic flip-flop

Figure 4.5 shows a simplified version of the differential-logic flip-flop introduced in

Figure 4.5 Differential logic flip-flop.

[26]. Since the structure of the flip-flop is symmetrical and the complimentary values of each signal exist in the circuit, any combinational logic function can be implemented using only n-channel transistors. The schematic diagram of a differential-logic flip-flop with a 2-input NAND at its input, along with its equivalent block diagram, is shown in Figure 4.6. The four n-channel transistors located at the lower part of Figure 4.6 perform the NAND function.

Figure 4.6 Differential-logic flip-flop with a NAND gate at its input.

Absence of slow p-channel transistors in the combinational circuit allows it to operate faster than a standard static gate. By comparing Figure 4.5 and Figure 4.6 it can be seen that the delay of the combinational circuit is not added as an overhead to the flip-flop delay, but rather merged with it. In other words, the τ_1 and τ_3 time intervals are pipelined, which considerably improves the maximum operating frequency. It should be mentioned that this merging is possible in a clocked-CMOS flip-flop too, but with p-channel transistors in the combinational circuit the outcome is not promising. For a detailed comparison between differential and conventional logic circuits refer to [38].

In summary, the differential-logic flip-flop is preferred over clocked-CMOS or transmission-gate flip-flops for the following reasons:

- The absence of series p-channel transistors in the differential-logic flip-flop.
- The merging of the combinational-circuit delay τ_3 with the setup time τ_1 in this logic block.
- The single-phase-clock operation of the differential-logic flip-flop, which eliminates skew problems at high frequencies [36].

The only disadvantage of the differential flip-flop is its higher power consumption. When the clock is at logic 0, there is a flow of current from V_{dd} to the ground through one of the p-channel pull-up transistors and the n-channel branch in series with it. According to the logic values on D and $\bar{D}$, this current flows either through the left or the right branch (Figure 4.5). Further, when the clock transits to logic 1, if the logic value stored in the cross-coupled inverters is different from the input, it is changed by a surge of current from the cross-coupled configuration to the ground. These currents, which specifically flow in differential logic circuits, elevate the power dissipation [38].

In the next section, the possibility of further speed improvement for the differential logic will be investigated.

4.2. Replacing flip-flops with latches.

Consider replacing the flip-flops in a sequential circuit with latches. A block diagram of a cell in such a circuit is shown in Figure 4.7. Each cell has only one latch which is acti-

Figure 4.7 General form of a latch and its interactions in a sequential circuit.

vated at the rising edge of the clock. After τ_2 , the latch delay, the clock can transit back to

logic 0. After an additional delay of τ_3 , the combinational circuit delay, the logic value at the output of the combinational circuit becomes valid and the next clock cycle can begin. Figure 4.8 shows the clock waveform and the mentioned time delays. As expected, the mini-

Figure 4.8 Clock waveform at the maximum operating frequency.

mum clock period has been reduced from $\tau_1 + \tau_2 + \tau_3$ for a flip-flop-operated sequential circuit, to

$$T_{\min} = (\tau_2 + \tau_3)_{\max} \quad (4.3)$$

for a latch-operated sequential circuit. The maximum operating frequency is therefore

$$f_{\max} = \frac{1}{(\tau_2 + \tau_3)_{\max}} \quad (4.4)$$

If it is so easy to eliminate the setup time of flip-flops in a sequential circuit, one may ask why this is not the universal practise. The answer is as follows: If the clock stays high (the latches are kept on) for a time period longer than the latch and combinational circuit delay, the new value loaded into the latch can propagate to the next latch in the same clock cycle, as demonstrated in Figure 4.9. This is an unwanted additional state transition which occurs in a sequential circuit employing latches instead of flip-flops. This unwanted situation can only be avoided by bounding the clock period to an appropriate maximum. The

Figure 4.9 Clock waveform at a low frequency.

proper operation of the sequential circuit is then constrained as follows [44]:

$$(\tau_2 + \tau_3)_{\max} \leq T < 2 \times (\tau_2 + \tau_3)_{\min} \quad (4.5)$$

As long as the clock period satisfies Eq. (4.5), the sequential circuit operates properly. The left-hand side of Eq. (4.5) ensures that there is enough time for latches to transit from a current state to the following one. The right-hand side ensures that the latches are disabled before the data can propagate through more than one logic block (it has been assumed that latches are on for half the clock period). The right-hand side actually introduces a minimum operating frequency for the sequential circuit. The operating frequency range is

$$\frac{1}{2 \times (\tau_2 + \tau_3)_{\min}} < f \leq \frac{1}{(\tau_2 + \tau_3)_{\max}} \quad (4.6)$$

Having such a minimum operating frequency might not be a desired feature for general-purpose frequency dividers since it complicates the clock timing constraints.

However, assuming that $(\tau_2 + \tau_3)_{\min}$ and $(\tau_2 + \tau_3)_{\max}$ are not very different¹, the operating frequency range of the circuit, as expressed by Eq. (4.6), is more than adequate for our

1. This is a reasonable assumption for most of the architectures discussed in Chapter 3.

application (see Table 2.1).

In a sequential circuit, a transition from one state to the next one is expected to occur as a result of a clock transition. In the discussed configuration, state transitions can occur with no clock trigger if the clock is held high (at logic 1) for a time interval longer than $\tau_2 + \tau_3$. Actually, if the clock is held high constantly, the circuit will keep changing its states. This makes the circuit act as an oscillator. Having considered this, the operation of the sequential circuit can be explained in another way. The clock signal keeps enabling and disabling a ring oscillator. Each time the oscillator is enabled, it is only allowed to go through one state transition, which is a fraction of an output cycle, and then disabled again. Therefore, we have an oscillator which is synchronized with its input, the clock signal.

4.2.1. A new D latch structure

A latch design is introduced here which is based on a modified six-transistor SRAM structure [33, pp. 349–351]. Figure 4.10 shows the construction of the latch and the combi-

Figure 4.10 The proposed D latch.

national circuitry which follows it. The latch is very similar to the devices used in the differential logic [26] [38].

The output is taken from one side of the latch so that the combinational circuits can more simply be incorporated (Section 4.3.1). The inverters shown act as output buffers. Transistors used in the inverters are stronger (larger W/L ratio) than the p-channel transistors so that the outputs of the inverters can be used as inputs to another latch of the same kind. The combinational circuit will be merged with the first inverter (Section 4.3.1) in such a way that no additional delay is introduced.

The two p-channel transistors act as the two cross-coupled inverters of the differential logic or the SRAM. By eliminating the n-channel transistors from the inverters, the switching speed is increased at the expense of losing the latch functionality at very low frequencies.

In the differential logic, the switching is done by pulling down one side of the cross-coupled construction (see Figure 4.5). In the new structure, however, one side of the cross-coupled construction is pulled down while the other side is pushed up. This further improves the switching.

In a sequential circuit employing the proposed latch as the state storage element, the only charge transfers occur at the rising edge of the clock since the clock is connected to n-channel transistor gates only. Therefore, the minimum voltage of the clock signal does not necessarily have to be as low as 0 volts. This is another advantage of the proposed technique over a sequential circuit which employs flip-flops. In the latter, the clock signal, which is connected to n-channel and p-channel-transistor gates, has to go to the extremes so that each transistor in flip-flops is completely turned on at the proper time. Shifting up the clock signal will speed up the n-channel transistors but slow down the p-channel transistors. Shifting down the signal will increase the speed of the p-channel transistors while decreasing the speed of the n-channel ones. Thus, changing the dc value of the clock signal will not increase the speed of the flip-flop-operated circuits. However, in a latch-operated circuit, the speed can be improved by offsetting the clock signal. Figure 4.11 shows a rail-to-rail clock signal A as well as a shifted-up signal B, both at the same frequency. Since B holds

Figure 4.11 A rail-to-rail and a shifted-up clock.

the high voltage on the gates of the n-channel transistors for a longer period of time, currents passing through those transistors are larger [33]. As a result, the latch delay τ_2 is shorter when B is used as the clock and, as expressed by Eq. (4.6), the frequency of clock B can be further increased than that of clock A.

4.3. Frequency divider design (the first implementation)

Figure 4.12 shows the block diagram of the dual-modulus frequency divider as it was implemented in CMOS3 DLM, which contains a divide-by $3/4$ synchronous counter as the first stage (dashed box) followed by the second stage, a divide-by-4 asynchronous counter. The standard cells have been shaded, and the differential paths and the buffers in the first stage have not been shown. The divide-by- $15/16$ function is selected through a modulus-selection input (MC). With this input at logic 1, the synchronous counter divides by 4 only, and the divider divides by 16. For the divide-by-15, the synchronous counter divides by 4 until all the flip-flops in the asynchronous counter are set to 1. Then, the complemented outputs from these flip-flops, together with the modulus-selection input at logic 0, generate

Figure 4.12 Functional block diagram of the dual-modulus frequency divider.

a pulse enabling the synchronous counter to divide by 3 only once in a 15-clock cycle. The divider includes three sequential circuits. The first one is the synchronous counter which is clocked by the input signal. The second one is the first toggle flip-flop which is clocked with the output of the synchronous counter. Finally, the third one is the second toggle flip-flop which is clocked with the output of the first toggle flip-flop and provides the output of the divider. Figure 4.13 shows a divide-by-16 cycle followed by a divide-by-15 cycle. State transitions have been marked with horizontal lines. If a state transition is used as a clock for the next sequential circuit, it is specified by an arrow. Both the rising edge and the falling edge of the output signal can be used to clock the external circuits.

Figure 4.13 State flow of the frequency divider.

4.3.1. First stage of the divider

The high-speed D latch introduced in the previous section (Figure 4.10) has been used to construct the first stage of the divider. A schematic diagram of the first stage, whose functional block diagram is enclosed by the dashed box in Figure 4.12, is shown in Figure 4.14.

Figure 4.14 First stage.

When there is a logic 1 on MC1, the five transistors at the bottom of Figure 4.14, which perform the function symbolized by the 2-input OR and 2-input AND in Figure 4.12, have no effect on the operation of the counter. In that case, the counter goes through a four-state sequence and divides by 4. When there is a logic 0 on MC1, those five transistors pull node S down to 0 during the state 1 1. As a result, although there is a 1 stored in Q1, a 0 is passed to D2 during that state. Therefore, with the next clock, the counter goes to the state 00. Now the counter divides by three. The state diagram of the first stage is shown in Figure 4.15.

Figure 4.15 State diagram of the first stage.

4.3.1.1. Layout considerations for the first stage

As mentioned in the previous chapter, the divider speed is limited by the speed of the first stage. Therefore, special attention should be paid to the layout of the first stage.

Every effort has been made to compact the layout in order to keep the parasitic capacitances and resistances as small as possible. The high resistance of the polysilicon (poly) layer and high capacitance between poly and field (Appendix B) necessitate minimizing poly area by replacing it with metal1 or metal2 wherever possible. All the interconnections are done using metal1 or metal2 and the use of poly has been limited to gates. Laying out p and n diffusions close together is another way of reducing the poly sizes in inverters. Where possible, 45° metal lines have been used for long interconnections to shorten them in order to minimize their capacitance and resistance.

To bypass the high sheet-resistance of the diffusion layer (Appendix B) which slows down the transistors, several contacts have been used to connect metal1 to diffusion. This way the carriers can travel through the metal1 layer which has a much lower sheet resistance.

Spikes of current flowing through narrow power lines can cause ac harmonics to appear on the power lines which can be harmful to the operation of the on-chip components

including the divider. To avoid that, wide metal power lines have been laid out to reduce the amount of voltage drop on them. To further smooth out the possible voltage fluctuations on the power lines, capacitors have been placed between V_{dd} and ground lines on the unused areas of the chip.

Device sizing has an important role in increasing the operating frequency of a circuit. Increasing the size of a transistor gives it a higher transconductance but at the same time increases its parasitic capacitances as a result of larger diffusion and gate areas. To find the best size for every transistor in the circuit optimization is necessary. Simulation (HSPICE) and layout modification (CADENCE) have been performed alternatively to size the transistors (for more details see Appendix A). The transistor sizes can be found in Appendix C.

Simulation results show that the operating frequency range of the first stage is from 100 MHz to 165 MHz.

4.3.2. Second stage of the divider

Second stage construction is shown in Figure 4.12. Since the clock frequency of the second stage is at least three times lower than that of the first stage, it does not have to be as fast as the first stage. However, that frequency is still too high for a standard-cell flip-flop. A true single-phase-clock flip-flop [36] is a good choice for the second stage flip-flop (Figure 4.16) because it is fast enough and its power consumption is less than that of a differential-logic flip-flop [38]. By connecting the flip-flop output $\bar{Q}$ to its input D a toggle flip-flop has been formed which toggles on the rising edge of the clock pulse. It is a fully custom-designed cell whose transistors have been sized using the procedure explained in Appendix A. The operating frequency range of the flip-flop has been found by simulation to be from 10 MHz to 100 MHz.

Figure 4.16 The second stage toggle flip-flop.

The second stage is constructed from two toggle flip-flops, forming an asynchronous counter with a division ratio of 4.

4.3.3. The complete frequency divider

The divider includes one first stage cell, two toggle flip-flops, a 3-input OR, an inverter, an output buffer and decoupling capacitors between the power rails. Standard cells were used for the 3-input OR (a 3-input NOR followed by an inverter) and buffer.

Considering the resistance and inductance of the paths connecting the voltage source to each component on the chip, the voltage on the supply rails will be affected by the currents flowing to the frequency divider. The on-chip decoupling capacitors help maintain the consistency of supply voltage on the rails.

The layouts of the first stage, second-stage flip-flop and frequency divider are shown in Appendix C. The frequency divider has an active area of $274\ \mu\text{m} \times 214\ \mu\text{m}$. The capacitor occupies $232\ \mu\text{m} \times 281\ \mu\text{m}$ with a capacity of 45 pF.

An additional frequency divider has been laid out on the same chip allowing its various blocks to be activated separately. The second divider can be useful in case of the main divider

malfunction. In that event, it can be used to find the part of the divider which is responsible for the malfunction.

4.3.4. Simulation results

At GHz frequencies it is almost impossible to have a square-wave clock waveform. Applying such a high-frequency waveform to a chip attenuates most of the frequency harmonics present in the square wave as a result of unwanted low-pass filtering effect caused by the signal path parasitics. Even the fundamental frequency component is considerably attenuated and special techniques have to be employed to ensure the arrival of the uncorrupted signal to the active die area. Although it was not expected to achieve a GHz operating frequency for the 3- μm design, the divider has been designed for operation with a sine-wave clock so that the results can be used for shorter gate-length implementations. Thus, a sine-wave signal has been used as the first stage clock for all the simulations. The sine wave has a minimum voltage of 0 volts and a maximum of 5 volts.

Figure 4.17(top) shows $Q2$, $\overline{Q2}$ and the clock waveforms of the first stage as it divides a 160-MHz clock by 4. The two inputs of the OR gate, $\overline{Q2}$ and MC1 (see Figure 4.12 on Page 45), are shown at the bottom of Figure 4.17 at $f_{in} = 160$ MHz. It can be seen that the second stage and the detecting circuitry are fast enough so that MC1 becomes valid on time (about 12 ns before the $\overline{Q2}$ transition time). Figure 4.18 shows the second stage waveforms for a divide-by-15 cycle.

The timing window, during which a valid MC is required by the divider, was found by simulation to have the following characteristics: $\tau_{\text{setup}} = 21$ ns, $\tau_{\text{hold}} = 7$ ns (Figure 4.19). It is safer to use the rising edge of the output signal ($\overline{Q4}$) to trigger the modulus controller (see Figure 3.1). This way the modulus controller has more time (half the output cycle more) to provide the new MC signal value to the divider.

Figure 4.17 Simulated waveforms, $f_{in} = 160$ MHz.

Figure 4.18 The second stage waveforms, $f_{in} = 150$ MHz.

Figure 4.19 Modulus control timing diagram.

The frequency divider circuit has been simulated to determine its sensitivity to temperature and power supply voltage variations. The results are given in Figure 4.20. The power consumption of the divider circuitry has also been measured using HSPICE simulation

Figure 4.20 Maximum operating frequency as a function of supply voltage and temperature.

Figure 4.21 Power consumption as a function of input frequency.

(Figure 4.21). Since the divider dissipates more power when it divides by 15, all the power measurements have been performed for that division ratio.

4.4. Second implementation

With the help of the first frequency divider test results presented in the next chapter, the divider (with some modifications) was laid out this time in CMOS4S, a 1.2 μ m CMOS technology. Those parts of the frequency divider which were modified are reported in this section.

The functional block diagram is shown in Figure 4.22. No standard cells have been used

Figure 4.22 Functional block diagram of the dual-modulus frequency divider .

and all components have been fully custom designed.

4.4.1. First stage of the divider

Figure 4.23 shows the schematic diagram of the first stage. As compared to the first implementation, the gate of M1 is charged through only one p-channel transistor, resulting in faster operation of the combinational circuit. The other change is the involvement of both latches in deactivating M1. The transistors have been carefully sized to achieve the highest possible operating frequency. Simulation shows an operating frequency range of 0.7–1.41 GHz for the first stage.

Figure 4.23 First stage (second implementation).

4.4.2. Second stage of the divider

The construction of the second stage flip-flop has not been changed since the first implementation. The $1.2\mu\text{m}$ cell has gone through the device sizing procedure (Appendix A) and has an operating frequency range of 10 MHz to 1 GHz.

4.4.3. Input buffer

To enable the divider to operate with weak input signals, an inverter has been placed at the input of the first stage. Biasing the inverter in the high-gain region of its transfer function makes it act as a voltage amplifier.

4.4.4. Input pads

The static protection circuitry of the input pads had to be bypassed in order to let the weak high-frequency input signal pass without too much attenuation. The 500-ohm series resistor of the standard-cell input pad was shorted. Two inverters were also bypassed at the

output stage of the input pad. The input pad formed in this way has been used only for the two input lines carrying the high-frequency signal into the chip. The rest of the inputs use standard input pads with complete static protection and inverter circuitries.

Since the two input pads do not have static protection, there has been a high possibility of losing the parts of the chip connected to those pins as a result of electro-static discharge. To limit the extent of possible destruction, a separate V_{dd} has been used to supply the input buffer. In this way the fraction of the chip which is in direct contact with the unprotected input pads (i.e. the input buffer) has been completely isolated from the rest of the chip. As a result, if the supply line of the input buffer were shorted to the ground as a result of a static discharge, the rest of the chip would be unharmed and still operational using the main V_{dd} lines supplied through the other V_{dd} pad.

4.4.5. Output pad

Information available about the performance of the CMOS4S standard cells when this work was undertaken has been insufficient. As a result there has been the possibility of the output pads being incapable of functioning at the output frequency of the divider. To ensure that the possible output-pad failure would not affect the proper evaluation of the divider circuitry, a second output pad has been connected to the circuit. The output of the divider has been given to the second output pad through an additional divide-by-2 stage, incorporating a D flip-flop and an inverter. In this manner, the second output pad operates at half the frequency of the first. If the output pad were not fast enough to provide the testing equipment with the divider output, the second output pad could be used to check on the divider output.

4.4.6. Power supply pads

An extra set of V_{dd} and ground pads have been used to supply the I/O pads separately. In this way the sensitive circuits at the core of the chip will not be affected by supply voltage fluctuations resulting from the high current spikes drawn by the output pads.

4.4.7. Complete divider

The layouts of the first stage, second stage flip-flop, inverters and modified standard cells (output buffer and 3-input NOR), used to construct the frequency divider, are presented in Appendix C. The divider occupies an area of $130\text{ }\mu\text{m} \times 120\text{ }\mu\text{m}$. The approximate total capacitance of the decoupling capacitors is 50 pF.

In addition to the main frequency divider, three others have been laid out on the same chip, enabling us to test different parts of the divider circuitry separately. This could be helpful if the main divider did not operate properly.

4.4.8. Simulation results

Figure 4.24 (top) shows the simulated waveforms of the first stage at $f_{in} = 1.4\text{ GHz}$. A cycle swallow occurs at $t \approx 26\text{ ns}$. MC1, $\overline{Q2}$ and $\overline{Q3}$ are shown at the bottom of the same figure. MC1, fed back to the first stage, transits from 1 to 0 about 1 ns earlier than the 1-to-0 transition of $\overline{Q2}$. This shows that the second stage and the detecting circuitry are fast enough to switch the division ratio of the first stage on time. Figure 4.25 shows the second stage waveforms for a divide-by-15 cycle.

The timing window for a valid MC was found by simulation to have the following characteristics: $\tau_{setup} = 2.5\text{ ns}$, $\tau_{hold} = 1.2\text{ ns}$ (see Figure 4.19).

The frequency divider has been simulated to find the effects of power-supply and temperature variations on its maximum operating frequency (Figure 4.26). The power consumed by the divider, at various input frequencies, has been measured using HSPICE

Figure 4.24 Simulated waveforms, $f_{in} = 1.4$ GHz.

Figure 4.25 The second stage waveforms, $f_{in} = 1.4$ GHz.

Figure 4.26 Maximum operating frequency as a function of supply voltage and temperature.

simulation (Figure 4.27). The power dissipated in the output buffer and the additional divide-by-two stage are also included in the values of Figure 4.27.

Figure 4.27 Power consumption as a function of input frequency.

4.5. Future improvements

Power consumption has not been a key factor in the design of the frequency divider. Nevertheless, it is an important parameter which should be considered for evaluation of a high-speed circuit. The first stage of the $1.2\mu\text{m}$ divider consumes 6.5 mW in the divide-by-3 mode and 5.85 mW in the divide-by-4 mode, both at 1.3 GHz. Considerable portions of the indicated powers are consumed in the modulus control combinational circuitry due to the missing p-channel transistors which have been eliminated to speed up the circuit. The absence of p-channel transistors causes short-circuit currents flowing directly from V_{dd} to V_{ss} for short time intervals. When the first stage without the combinational circuit was simulated at the same frequency, the amount of power consumption dropped from 5.85 mW to 3.9 mW. This shows that more than 30% of the first stage power is dissipated in its modulus control combinational circuitry.

To reduce the amount of power consumption in the frequency divider, it is possible to optimize the transistor sizes not just for speed but for speed and power.

4.6. Summary and conclusion

In this chapter, factors determining the speed of a general synchronous sequential circuit were introduced. It was demonstrated how latches instead of flip-flops can be used in a counter to increase the maximum operating frequency at the expense of losing the low frequency range. Design of a dual-modulus frequency divider using this scheme was reported. The divider was laid out in CMOS3 DLM (3 μm) and CMOS4S (1.2 μm).

When increasing the speed is the most important concern and operation at low frequencies is not essential (PLL frequency synthesis for the mobile radio), the proposed technique appears to be the answer.

To verify the functionality of the proposed design and show its measure of improvement, the fabricated chips were tested. The test results are presented in the next chapter.

Chapter 5

Performance Evaluation

The layout of the 3 μ m (CMOS3 DLM) frequency divider was submitted to Northern Telecom Electronics through Canadian Microelectronics Corporation for fabrication, and several tests were performed on the fabricated chip CU053. The design of the divider was then improved with the help of the information and experience achieved from the tests performed on CU053. The new design was then laid out in CMOS4S, a 1.2 μ m CMOS technology. The 1.2 μ m divider, CU056, went through the same test procedures to evaluate its functionality and performance. All test procedures and results for both chips are reported in this chapter.

The tests and measurements performed on the frequency dividers included:

- Maximum operating frequency as a function of supply voltage.
- Power consumption at different frequencies.
- Power consumption as a function of supply voltage.
- Minimum input amplitude necessary for the proper operation of the divider at different frequencies.
- Investigation of the proper operation of the divider while performing a fractional division.

5.1. 3 μ m-gate-length dual-modulus frequency divider

This section reports the tests performed on the first design, CU053, which was fabricated using CMOS3 DLM technology.

5.1.1. Test bed

A test bed was built for CU053 to provide it with the power supply and input and output connections. The presence of high-frequency signals on the test board necessitated having a ground plane, careful wiring using coaxial cables and the use of high-frequency capacitors and resistors to avoid unwanted intermodulation effects.

The schematic diagram of the test bed is shown in Figure 5.1. A 40-pin socket soldered to the board holds the chip. An 8-volt dc voltage is needed to supply the test board. An adjustable voltage regulator, LM317, provides the input bias voltage and another one supplies V_{dd} . A 50- Ω high-frequency resistor, soldered as close as possible to the socket holding the chip, applies the dc bias voltage to the input. In addition to the usual capacitors placed at the output of a voltage regulator, a 0.1 μ F high-frequency capacitor has been placed right beside the 50- Ω resistor between the regulator output and the ground to bypass the impedance of the wire connecting the regulator output to the 50- Ω resistor. Also, a 0.1 μ F capacitor placed between pin 1 and the ground bypasses the resistance and inductance of the wire connecting the V_{dd} regulator output to pin 1.

The input signal is fed to the board through a BNC cable, one side of which is soldered to the board, while the other side has a BNC connector for connection to the input source.

Figure 5.1 CU053 test bed.

5.1.2. Operating frequency

To measure the maximum operating frequency, the configuration shown in Figure 5.2 was used. First, the bias voltage was adjusted to 2.5 volts and the input amplitude to 2.5 volts. The spectrum analyzer showed the output fundamental frequency, which should be equal to $f_{in}/15$ when there is a logic 0 on MC and $f_{in}/16$ when there is a logic 1. The input frequency

Figure 5.2 Operating frequency measurement.

was gradually increased until any further increase would cause the frequency divider to fail either for divide by 15 or divide by 16, which occurred at 276 MHz. The same procedure was followed this time, decreasing the input frequency to find the minimum operating frequency. The minimum operating frequency was measured at 136 MHz.

By increasing the bias voltage and decreasing the input amplitude accordingly to keep the maximum voltage equal to 5 V, the maximum operating frequency can be increased at the expense of narrowing the operating-frequency band. At $V_b = 4.35$ V, the frequency range is from 285 MHz to 330 MHz. Input and output waveforms are shown at $f_{in} = 330$ MHz in Figure 5.3. A delay of about 18 ns exists between the clock and the output transitions.

5.1.2.1. Sensitivity to supply voltage variations

By connecting a dc voltage that is higher than the threshold of the n-channel transistors to the input, the divider oscillates. The oscillation frequency is a function of the input voltage. The maximum operating frequency of the divider can be approximated by increasing the input voltage to V_{dd} and multiplying the oscillation frequency by the divider division

Figure 5.3 Oscilloscope traces for the input and output signals at $f_{in} = 330$ MHz.

ratio. This approach was used to measure the supply voltage variation effects on the maximum operating frequency of the divider.

In this case, the input was connected to the supply voltage and the MC pin to the ground

(divide-by-15 configuration). The frequency at the output of the divider was measured by the spectrum analyzer. Results are shown in Figure 5.4. The maximum operating frequency

Figure 5.4 Frequency of oscillation as a function of supply voltage.

of the divider at any supply voltage can be approximated by $15f_{out}$, where f_{out} is the frequency of oscillation (Figure 5.4). The approximated maximum operating frequencies appear on the right-hand side of the diagram.

5.1.3. Power consumption

It is desirable to have high speed and low power consumption at the same time, but there is always a trade-off between these two. In a CMOS circuit where short-circuit dissipation can be neglected, power consumption can be related to the supply voltage and frequency with [33]:

$$P = C_L V_{dd}^2 f \quad (5.1)$$

where C_L is the total capacitance being charged and discharged with the frequency of f . Short circuit dissipation refers to the currents flowing directly from V_{dd} to V_{ss} through the transistors. This kind of current becomes unavoidable in high-speed circuits [26]. In such cases, Eq. (5.1) can no longer represent the total power consumption for the circuit.

This section reports the tests performed on the frequency divider to investigate how its power consumption varies with respect to the changes in the power-supply voltage and input frequency.

The power consumed by the frequency divider was measured indirectly by measuring the current drawn from the power supply (Figure 5.5).

Figure 5.5 Power consumption measurement.

Figure 5.6 shows the power consumed in the unloaded frequency divider at different input frequencies. The consumed power is a linear function of frequency in agreement with Eq. (5.1).

Figure 5.7 shows the power consumption of the unloaded divider as a function of supply voltage. The bias voltage and input amplitude were adjusted to bound the input signal voltage within the zero-to- V_{dd} range. This adjustment was repeated for every new value of V_{dd} .

As the supply voltage increases, the power consumption grows at a rate faster than $(V_{dd})^2$.

Figure 5.6 Power consumption (including the output pad power) as a function of input frequency.

Figure 5.7 Power consumption as a function of supply voltage ($f_{in} = 130$ MHz).

5.1.4. Fractional division and phase noise

When a dual-modulus frequency divider is used as a fractional divider, its division ratio is switched alternatively between the two fixed division ratios. The switching should be possible once every output cycle. To evaluate this capability of the fabricated divider, the following test was performed.

A D flip-flop, wired to perform a divide-by-two function, was clocked by the frequency divider. The flip-flop output was connected to MC control input (see Figure 5.8). This

Figure 5.8 Fractional division test.

configuration applies $\{101010\cdots\}$ to MC and therefore changes the divider division ratio once every output cycle. A divider functioning properly with this modulus control bit stream also guarantees operation with any arbitrary fractional division ratio.

The HP 3585A spectrum analyzer was used to check the proper operation of the frequency divider. The HP 8663 synthesized signal generator clocked the divider at 330 MHz. With an equal number of ones and zeros in the bit stream, the average division ratio is 15.5. Therefore, the output frequency should be at $330 \text{ MHz} / 15.5 = 21.2903225 \text{ MHz}$. The frequency spectrum of the divider output is shown in Figure 5.9. The fundamental frequency is at

Figure 5.9 Spectrum of the output around the fundamental frequency.

a: 0-to-25 MHz frequency range. The marker is on the fundamental frequency, but due to the resolution limitations of the spectrum analyzer, the marked frequency is not accurate.

b: Span of 200 Hz around the fundamental frequency.

21.2903225 MHz. The additional peak corresponds to the jitter resulting from fractional division [Chapter 2].

The diagram at the bottom of Figure 5.9 shows the fundamental frequency with the lowest resolution bandwidth of the spectrum analyzer. The clarity of the peak shows that the phase noise level of the divider is below the noise floor of the measurement equipment.

5.1.5. CU053 performance summary

The fabricated chip was found to be successfully operational as a dual-modulus frequency divider. Its maximum operating frequency is about 50% higher than the simulated value.

For a continuous divide-by-15 operation, the divider occasionally locks into a condition in which no output is generated. A possible explanation is that the complex combinational circuitry (see Figure 4.14 on Page 47) is not capable of detecting and resetting ($Q2=0$ and $Q1=1$), if M1 is on and MC1=0. M1 is never on when $Q2=0$ and $Q1=1$ during a normal operation. But if for some reason M1 turns on in that state while the divider is in a divide-by-15 cycle, the first stage locks in that state and the divider will no longer produce an output. When the divider locks in this state, its operation can be resumed by connecting a 1 to MC (divide by 16) and consequently turning the transistor M1 off.

5.2. 1.2 μ m-gate-length dual-modulus frequency divider

This section reports the tests performed on the second design, CU056, which has been fabricated using CMOS4S technology.

5.2.1. Test Bed

The schematic diagram of the test bed built for CU056 is shown in Figure 5.10. The problem of having high-frequency signals on the test board was more serious this time since GHz-range frequencies clock the divider.

There are two voltage regulators on the board, one for V_{dd} and the other for the input bias voltage. Both regulators are adjustable to facilitate observing the frequency-divider characteristics at different supply and bias voltages.

The power supply is connected to the chip through three pins. The first supplies the pad circuitries, the second is used by the input buffer and the third supplies the frequency divider circuitry at the core of the IC (Appendix C). Such an arrangement allows the power consumed at the divider circuitry to be measured separately from the power consumed in the pads. This is considered important because the power consumed in the pads does not provide any information about the quality of the frequency divider design. To decouple the three supply pins from each other, three separate wires have been used to connect the voltage-regulator output to the pins and a 0.1- μ F capacitor has been placed between each supply pin and the ground plane.

The input signal is applied to the chip through a 1-nF capacitor. To keep the input signal path symmetrical, a 1-nF capacitor has been put in the return path between pin 30, on-chip ground of high-frequency input signal (Appendix C), and the ground plane. The bias voltage is applied to the input pin by a 50-ohm high-frequency resistor, while a 0.1- μ F capacitor has been put between the voltage regulator output and the ground. The capacitor and resistor,

Figure 5.10 CU056 test bed.

placed on board in close proximity to the input pin, help bypass the impedance of the wires so that the input impedance seen by the incoming signal at high frequency is 50 ohms.

5.2.2. Operating frequency

The maximum and minimum operating frequencies of CU056 were measured using the configuration shown in Figure 5.11. The input bias voltage (V_b) was set to 2.5 volts and a

Figure 5.11 Operating frequency measurement.

sinewave input with an amplitude of $0.9 V_{ms}$ was applied to the divider. A maximum operating frequency of 1.3 GHz and a minimum of 700 MHz were measured. The bias voltage was decreased to 2.1 volts resulting in an operating frequency of 1.4 GHz. Figure 5.12 shows the input and output waveforms at $f_{in} = 1.4$ GHz as shown by the oscilloscope. There is a delay of about 8 ns between the clock and the output transitions.

5.2.2.1. Sensitivity to supply voltage variations

To observe the effect of supply voltage variations on the maximum operating frequency, the bias voltage was decreased to 0 to make the divider oscillate without an input signal connected to the input. The frequency at the output of the divider (/15) measured by the spectrum analyzer was recorded at different supply voltages. The results are shown in Figure 5.13.

Figure 5.12 Oscilloscope traces for the input and output signals at $f_m = 1.4$ GHz.

The input frequencies corresponding to such output frequencies (see Section 5.1.2.1) are reported on the right hand side of the same diagram confirming the simulation results (Page 60).

Figure 5.13 Frequency of oscillation as a function of supply voltage.

5.2.3. Minimum input amplitude

Since there is an input buffer on CU056, the divider is expected to operate with low input amplitudes as well. To verify this, the minimum input signal voltage needed by the circuit was measured at different frequencies. The results for two values of V_b are shown in Figure 5.14. Less than 0.6 V is required for the proper operation of the circuit.

5.2.4. Power consumption

The current meter was connected to the test board in such a way that it measured the current flowing to the divider circuitry in the core of the chip and the input buffer only (Figure 5.10). The frequency divider was clocked with a range of input frequencies and the

Figure 5.14 Minimum input signal voltage (rms) required as a function of frequency.

amount of current at each frequency was recorded. The three other frequency dividers on the chip (see Appendix C) were disabled by connecting their high-frequency inputs to the appropriate voltage on the test board (Figure 5.10). Although the other three dividers are disabled, they still dissipate power. To measure the amount of that power, the main frequency divider was disabled as well by setting its input bias voltage to 5 V. The meter measured a 1.8 mA current flowing to the chip core. Therefore, a $1.8/4 = 0.45$ mA current flows to each disabled divider. The measured value has been used to correct the power (current) measurements for the main divider. A subtraction of $3 \times 0.45 \text{ mA} = 1.35 \text{ mA}$ from the measured currents approximates the currents flowing to the main frequency divider.

Figure 5.15 shows the power consumed in the main frequency divider at the correspond-

Figure 5.15 Power consumption as a function of input frequency.

ing input frequencies, and the fact that the power–frequency relation is linear.

The divider was then clocked with a 650 MHz clock and the supply voltage was varied. The power consumed in the chip as a function of the supply voltage was recorded. The current supplied to the three disabled frequency dividers at each supply voltage was found by disabling all the dividers, measuring the current flowing to the chip and multiplying it by three quarters. The final results, after subtraction of the disabled divider powers, are shown in Figure 5.16. Again, the voltage–power relation does not agree with Eq. (5.1) due to the short-circuit currents of the first stage (see Section 5.1.3).

Figure 5.16 Power consumption as a function of supply voltage ($f_{in}=0.65$ GHz).

5.2.5. Fractional division and phase noise

The maximum operating frequency of CU056 has been determined to be 1.4 GHz. For that input frequency, the divider output frequency is about 90 MHz. Since 90 MHz is too high a frequency to route on the test board and clock an off-chip device, a different approach was used to test the fractional division capability of the divider.

There is a divide-by-two stage following the output of the divider on CU056. The additional frequency division stage was implemented to reduce the output frequency so that the output pads would bring the lower frequency out of chip in case they were not fast enough for the main output signal. Fortunately the output pads were fast enough and the main output ($f_{in}/15$ or $f_{in}/16$) was strong (Figure 5.12). Therefore, the on-chip extra frequency division

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stage was free and could be used to control the division ratio of the divider as shown in Figure 5.17. This was the same arrangement used to test CU053 except that here the D flip-

Figure 5.17 Fractional division test..

flop was on-chip.

The divider was clocked with a 1.4 GHz sine wave generated by the HP 8663A synthesized signal generator. The HP 4195A network/spectrum analyzer showed the frequency band around the output fundamental frequency, $f_m / 15.5$ (Figure 5.18).

The graph at the bottom of Figure 5.18 shows the fundamental frequency with the lowest resolution bandwidth of the spectrum analyzer. It can be seen that the frequency divider phase noise is lower than the noise floor of the measurement equipment.

Figure 5.18 Spectrum of the output, around the fundamental frequency.
a: 0-to-98 MHz frequency range. The marker is on the fundamental frequency, but due to the resolution limitations of the spectrum analyzer, the marked frequency is not accurate.
b: Span of 200 Hz around the fundamental frequency.

5.2.6. CU056 performance summary

The fabricated dual-modulus frequency divider was found to be fully operational and can be used to perform fractional division in its operating frequency range. The measurement results match the simulated values. The problem of locking into an unwanted state (first implementation) was successfully solved.

5.3. Summary

The two frequency dividers were tested to find their maximum operating frequency, power consumption, response to power supply voltage variations and their functionality in an environment for which they have been designed (Figure 3.1). Important parameters of the two frequency dividers, along with those of the fastest reported CMOS dual-modulus frequency divider, are summarized in Table 5.1.

Table 5.1 Dual-modulus frequency divider comparisons

	This work		The fastest reported CMOS dual-modulus frequency divider [26]
Gate length (μm)	3	1.2	0.4
Gate oxide thickness	500 Å	250 Å	100 Å
Threshold voltage (V)	0.75	0.8	0.3
Division ratios	15/16	15/16	128/129
Max. operating freq.	330 MHz	1.4 GHz	4.2 GHz
Power (mW) at f_{max}	12.2 *	12.7	95
Required V_{in} (V) (rms)	0.46	0.6	0.53
Propagation delay (ns)	18	8	**

* Including the power consumed in the output pad

** Not reported

The fabricated frequency dividers are functional and can be used to perform fractional frequency division at the limits of their fabrication technology.

Chapter 6

Conclusion

CMOS circuits have always been reported to be too slow for RF applications. In this thesis the problem of designing a high-speed CMOS frequency divider has been approached by an extensive literature research followed by simulations and comparisons of various structures. A new dual-modulus frequency divider design has been proposed and verified through simulation and post-fabrication testing. This frequency divider, integrated in 1.2 μ m CMOS, is believed to be the first GHz-range CMOS dual-modulus frequency divider fabricated with a non-sub-micron technology. The low power consumption of the device makes it feasible for today's low-power radio applications.

The major innovation in this thesis is the use of latches instead of flip-flops in a sequential circuit, something that has always been reported in the literature as a hazardous configuration. This work proves that the proposed technique is functional and improves the speed without impairing the operation of the circuit.

The results of this research show that the dual-modulus frequency divider with a GHz-range operating frequency and reasonable power consumption can be implemented using CMOS technology. The operating frequency can be further increased by integrating the divider in a shorter-gate-length CMOS process.

The next step towards implementation of the mobile radio frequency synthesizer could be the design of a CMOS VCO for the fractional-division PLL. The VCO is another loop component whose design needs special attention. The maximum frequency and the purity of the output signal are the two factors of the CMOS VCO which require improvement. Since the proposed divider requires a low-amplitude input signal, a bipolar VCO can clock the divider with no need for an interface. This can be helpful if a BiCMOS technology is considered for implementation of the single-chip frequency synthesizer. The other possibility is to integrate all the loop components except the VCO on a CMOS chip and use an off-chip bipolar VCO.

Appendix A

Device Sizing

Device sizing plays an important role in the design of a high-speed circuit [36]. The speed of a circuit is a function of its transistor sizes, while the size of each transistor affects its transconductance as well as its gate, drain and source capacitances. Automatic speed optimization is possible by HSPICE for combinational circuits. However, for a sequential circuit, more than just one time delay must be minimized. Each state transition has to be considered separately. This makes the automatic optimization of a sequential circuit more complex than that of a gate or a full adder. Therefore, manual optimization has been used for the device sizing of the divider.

The device sizing procedure is demonstrated in a flow chart in Figure A.1. Layout modification and circuit simulation are performed alternatively using CADENCE and HSPICE in order to increase the maximum operating frequency of the circuit. The HSPICE simulations (level 3 model for MOS transistors) were performed for 25° C and power supply

Figure A.1 Device sizing.

voltage of 5 volts. A sine wave with a minimum of 0 volts and a maximum of 5 volts was used as the clock. Simulation netlists included the parasitic capacitances extracted by CADENCE.

The speed capability was improved by going through the main loop until there was no further improvement in the speed. The smaller loop found the maximum operating frequency after each layout alteration. In the case of a dual-modulus counter (first stage), the small loop consisted of two simulations, one for each division ratio, and the question in the decision block was: "Is the circuit functional in both cases?".

To fabricate the divider with another CMOS process, the transistor sizes in the new technology would have to be optimized once again to ensure the achievement of the highest possible operating frequency.

Appendix B

Process parameters

B.1. CMOS3 DLM

This section is derived from "Guide to the Integrated Circuit Implementation Services" of the Canadian Microelectronics Corporation, version 4:0, March 1989.

CMOS3 DLM is a 3-micron P-well CMOS process with single-level polysilicon and double-level metal. Designs submitted to CMC must be defined using the 5-micron scale (design scale microns or DSM). The designs are scaled down at Northern Telecom to 60% of the specified dimensions prior to the creation of the pattern generator (PG) tapes.

Table B.1 CMOS3 DLM layers

Layer	Mask Level	CIF Name	Description
P-well	010	CPW	– defines P-well
N-well (exclusion)	020	CNG	– implant for enhancement of N-substrate outside of P-well
Device Well	030	CF	– interior defines active regions – exterior regions covered with field oxide (Field) – also referred to as diffusion or thinox
P-Guard	040	CPG	– implant for enhancement of P-well surface doping to prevent inversion under field oxide
Capacitor P-doping (optional)	055	CCP	– defines area of P+ doping in a device well to form bottom plate of capacitor
Polysilicon	060	CP	– defines polysilicon lines and transistor gates
N+ Doping (exclusion)	070	CNP	– defines regions excluded from N+ doping
P+ Doping	080	CPP	– defines regions of P+ doping – substrate doping will occur only in device well regions
Contact	090	CC	– defines contacts from metal to polysilicon or diffusion
Metal1	100	CM	– defines the first metal lines
Via	110	CV	– defines the vias or contacts between metal1 and metal2
Metal2	120	CM2	– defines the second metal2 lines
Passivation Window	130	CG	– defines openings in passivation layer for bonding or probe pads

Table B.2 Parameters used in the HSPICE simulations

Parameter	NMOS	PMOS	Units
vto	0.7	- 0.8	V
kp	4.e-05	1.2 e-05	A/V ²
gamma	1.1	.6	V ^{0.5}
phi	.6	.6	V
lambda	.01	.03	1/V
RD	40	100	ohms
RS	40	100	ohms
pb	.7	.6	V
cgso	3.e-10	2.5e-10	F/m
cgdo	3.e-10	2.5e-10	F/m
cgbo	5.e-10	5.e-10	F/m
rsh	25	80	ohms/sq.
cj	.00044	.00015	F/m ²
mj	.5	.6	-
cjsw	4.e-10	4.e-10	F/m
mjsw	.3	.6	-
js	1.e-05	1.e-05	A/m ²
tox	5.e-08	5.e-08	m
nsub	1.7e+16	5.e+15	1/cm ³
nss	0	0	1/cm ²
nfs	0	0	1/cm ²
tpg	1	1	-
xj	6.e-07	5.e-07	m
ld	3.5e-07	2.5e-07	m
uo	775	250	cm ² /Vs
vmax	1.e+05	7000	m/s
theta	.13	.13	1/V
eta	.05	.3	-
kappa	1	1	-

Table B.3 Other electrical parameters

Capacitance	pF/ μm^2	pF/ μm
Gate (Cox)	6.9E-4	0.5E-4
Metal1 - Field	2.7E-5	0.4E-4
Metal1 - Poly	5.0E-5	
Metal1 - Diffusion	5.0E-5	
Poly - Field	6.0E-5	0.2E-4
Metal2 - Field	1.4E-5	2.0E-5
Metal2 - Diffusion	1.6E-5	
Metal2 - Poly	2.0E-5	
Metal2 - Metal1	2.5E-5	
Capacitor P+ - Poly (0.1%/V linearity)	6.9E-4	0.5E-4

Resistance	ohms/sq.
N+ Diffusion	25
P+ Diffusion	80
N+ Poly	18
Capacitor P+	300
P-well	4k
Metal1	0.035
Metal2	0.030
3 x 3 Metal1 - P+ Diffusion Contact	121
3 x 3 Metal1 - N+ Diffusion Contact	44
3 x 3 Metal1 - N+ Poly Contact	25

B.2. CMC CMOS4S Edge Support Version 1.0 (Beta)

This section contains electrical and simulation parameters for Northern Telecom Electronics CMOS4S, a 1.2-micron, double-polysilicon, double-metal N-well process. All information in this section has been provided by Canadian Microelectronics Corporation (Report IC90-01, February 8, 1990, David Brown and Andrew Scott).

Designs submitted to CMC are fabricated at 80% of their specified dimensions. For example, a design feature with a dimension of 1.5 DSM (Design Scale Microns) is reduced to 1.2 microns in the manufactured version of the design.

B.2.1. CMOS4S mask layers**Table B.4 CMOS4S mask layers**

Mask Level	Name (Function)	CIF Layers	GDS II Layer Number	Functional Description
05	N-Well	CNW	1	Defines n-wells.
10	Device Well	CF	2	Defines active device regions. All other regions will be covered by field oxide.
15	P-Guard Exclusion	CPG	3	Implant mask to increase p-substrate surface doping under field oxide. Exclusion mask to be drawn around n-wells.
20	Polysilicon	CP	6	Defines polysilicon lines and transistor gates.
27	Capacitor polysilicon	CCP	5	Defines top poly plates to form poly-to-poly capacitors (optional).
30	N+ Doping Exclusion	CNP	7	Defines areas not to be doped n+. Substrate doping will occur only in device wells.
35	P+ Doping	CPP	8	Defines areas to be doped p+. Substrate doping will occur only in device wells.
40	Contact Window	CC	9	Defines contact areas from metal 1 to polysilicon or diffusion.
50	Metal 1	CM	10	Defines first level metal lines.
60	Via 1	CV	11	Defines contact areas from metal 2 to metal 1.
70	Metal 2	CM2	12	Defines second level metal lines.
95	Passivation Windows	CG	13	Defines openings in passivation layer for bonding pads.

B.2.2. SPICE and electrical parameters

Physical dimensions, not design scale dimensions, are applicable to the parameters and their use.

Table B.5 SPICE Level 3 parameters

Parameter	NMOS	PMOS	Units
LEVEL	3	3	–
UO	566.3	200.8	cm ² /Vs
VTO	0.7572	–0.8307	V
NFS	5.764E+11	5.864E+11	1/cm ²
TPG	1.000	1.000	–
TOX	2.502E–08	2.502E–08	m
NSUB	1.400E+16	2.011E+16	1/cm ³
VMAX	1.651E+05	2.823E+05	m/s
RS	26.77	58.90	ohm
RD	26.77	58.90	ohm
XJ	1.165E–07	1.742E–07	m
LD	1.157E–07	1.364E–07	m
DELTA	0.3551	0.4598	–
THETA	6.574E–02	0.1376	1/V
ETA	9.814E–02	6.729E–02	–
KAPPA	2.000E–17	7.487	–
PB	0.800	0.800	V
IS	1.000E–16	1.000E–16	A
JS	1.000E–04	1.000E–04	A/m ²
CJ	2.900E–04	4.100E–04	F/m ²
MJ	0.486	0.540	–
CJSW	3.300E–10	3.400E–10	F/m
MJSW	0.330	0.300	–
CGSO	1.973E–10	3.284E–10	F/m
CGDO	1.973E–10	3.284E–10	F/m
FC	0.500	0.500	–

– Nominal conditions.

– All resistances (RS and RD) are for 20–micron–wide devices.

Table B.6 Other Electrical Parameters

Resistance	ohms/sq.
N+ Diffusion	45
P+ Diffusion	100
N+ Poly	30
P+ Poly	45
N-well	1.8K (geometry and voltage dependent)
Metal1	0.050
Metal2	0.025
Metal1 – Diffusion Contacts	20 ohms (1.2 x 1.2 microns) *
Metal1 – Poly Contacts	10 ohms (1.2 x 1.2 microns) *
Metal1–Metal2 Vias	0.120 ohms (1.6 x 1.6 microns) *

Capacitance	Area Component (pF/um ²) *	Edge Component (pF/um) *
Metal1 – Field	2.9E–5	5.00E–5
Metal1 – Poly	6.0E–5	
Metal1 – Diffusion	5.5E–5	
Poly – Field	6.4E–5	2.20E–5
Metal2 – Field	1.6E–5	4.63E–5
Metal2 – Poly	2.5E–5	
Metal2 – Diffusion	2.0E–5	
Metal2 – Metal1	5.2E–5	
Capacitor Poly to Poly	7.76E–4	1.06E–4

* physical dimensions, not design scale dimensions

Appendix C

Physical Design: layouts, transistor sizes and chip configurations

The layouts created for this work are presented here, while the transistor widths (actual sizes in μm) are presented in a diagram following each layout.

C.1. CMOS3 DLM

The first stage and the second stage D flip-flop are the two cells that have been created for the $3\mu\text{m}$ design. The output of the first stage is given to the second stage through an inverter as shown in Figure C.5 and Figure C.7. The inverter is constructed from a $6/3$ n-channel and a $15/3$ p-channel transistor.

All the transistors have a gate length of $3\mu\text{m}$.

The cells and their interconnections as well as the chip pin numbers are shown in Figure C.7 (the standard cells are shaded).

Figure C.1 CMOS3 DLM layer legend.

Figure C.2 First stage, CMOS3 DLM.

Figure C.3 First stage transistor sizes, CMOS3 DLM.

Figure C.4 Second stage D flip-flop, CMOS3 DLM.

Figure C.5 Dual-modulus frequency divider, CMOS3 DLM.

Figure C.6 CU053, outlined Metal1 and Metal2, CMOS3 DLM.

Figure C.7 Configuration of cells on CU053.

C.2. CMOS4S

The custom-designed cells for the 1.2 μ m design are: the first stage cell, the second-stage D flip-flop and two inverter cells used in different locations. The modified standard cells, 3-input NOR, output buffer and input pad are also presented here.

All the transistors have a gate length of 1.2 μ m.

The cells and their interconnections as well as the chip pin numbers are shown in Figure C.18 (the standard cells are shaded).

Figure C.8 CMOS4S layer legend.

Figure C.9 First stage, CMOS4S.

Figure C.10 First stage transistor sizes, CMOS4S.

Figure C.11 Second stage D flip-flop, CMOS4S.

Figure C.12 Inv2 and Inv3, CMOS4S.
Left: Inv2, Right: Inv3.

Figure C.13 The modified NOR3, CMOS4S.

Figure C.14 The modified buffer (Buf1), CMOS4S.

Figure C.15 The modified input pad (Inpad1), CMOS4S.

Figure C.16 Dual-modulus frequency divider, CMOS4S.

Figure C.17 CU056, outlined Metal1 and Metal2, CMOS4S.

Figure C.18 Configuration of cells on CU056.

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