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Dynamic Range and Bandwidth Limitations in Sampled-Data and Clocked Continuous-Time BiCMOS Sigma-Delta Modulators

by

Bill Bereza

This thesis is submitted to the Faculty of Graduate Studies and
Research in partial fulfillment of the requirements for the degree of
Doctorate of Philosophy

Ottawa-Carleton Institute for Electrical Engineering

Department of Electronics
Faculty of Engineering
Carleton University
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"Dynamic Range and Bandwidth Limitations in Sampled-Data and Clocked Continuous-Time BiCMOS Sigma-Delta Modulators"

submitted by Bill Bereza in partial fulfillment of the requirements for the degree of Doctorate of Philosophy.

Prof. M. A. Copeland
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Chairman,
Department of Electronics

April 1996

Prof. David G. Naim
External Examiner

Abstract

$\Sigma\Delta$ modulation has recently proved to be of great importance as an architectural alternative in the implementation of analog to digital converters. The achievable resolution of these converters often depends on various mechanisms that limit the dynamic range. Furthermore, the bandwidth that is achievable depends on the capabilities of the silicon technology and the circuit approaches used.

Following an introductory review of mechanisms that limit dynamic range in analog circuits, this thesis concentrates primarily on circuit noise and nonlinearity and how these and other mechanisms limit the dynamic range in $\Sigma\Delta$ modulators. The first part of this thesis covers a conventional sampled-data, double-integration $\Sigma\Delta$ modulator design. The use of BiCMOS adds to the potential speed capability of these modulators and is analyzed in some detail. Since amplifier gain is often sacrificed for bandwidth, the study of linearity in opamp-based, high-speed oversampled analog to digital converters is of particular importance.

The second part of the thesis focuses on clocked continuous time $\Sigma\Delta$ modulators. Operational transconductance amplifiers are incorporated into a near video bandwidth continuous-time $\Sigma\Delta$ architecture. In this circuit, the amplifier realizes integration onto the compensation (pole splitting) capacitor, and current steering methods are employed to eliminate the use of reference voltages typically required for feedback. The linearity is considerably degraded from the sampled data case. Once again, BiCMOS is exploited to achieve greater bandwidths. A rigorous noise analysis is provided which provides insight into the limitations of the circuits.

In summary, the performance of oversampled analog-to-digital converters is explored with emphasis on noise and nonlinearity. Through the use of relatively new process technology (BiCMOS), potentially lower noise and greater bandwidth may be achieved. Finally, circuit innovation was used to explore the above theme ..

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It is with great honor that I acknowledge the opportunity afforded me by Professor Miles Copeland to pursue this degree under his guidance. His intuitive insights and help throughout the years that I have known him has served me well.

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List of Symbols

$\alpha_1, \alpha_2, \alpha_3, \alpha_4$	Gain coefficients used in the design of the DISDM. They represent capacitor ratios.
α_1, α_4	Gain of the outer differential pairs of the OTA (Chapter 5).
α_n	Integrator gain, including gain error terms.
α_1, α_2	Voltage coefficient of capacitance.
a_0, a_1, a_2, a_3	} Nonlinearity coefficients.
b_0, b_1, b_2, b_3	
$A_1(j\omega), A_2(j\omega), A_3(j\omega)$	
A, A_{OL}	Open-loop gain of the amplifier.
β	Feedback factor and Beta of bipolar transistors.
B_n	Equivalent noise bandwidth.
CTSDM	Continuous-time $\Sigma\Delta$ modulator. (First-order in this thesis)
ΔV_{FB}	The integrated voltage from feedback current.
$D(s)$	Denominator of a biquad transfer function.
dB	Decibels, relative to $1V_{PK}$ ($0dB = 1V_{PK}$)
dBV	Decibels, relative to $1V_{RMS}$ ($-3dBV = 0.707V_{RMS} = 1V_{PK}$ assuming a sinewave).
dBm	Decibels relative to 1mW, assuming a 50Ω load ($0dBm = 0.224V_{RMS} = 13dBV$).
DISDM	Double-Integration, $\Sigma\Delta$ modulator. (Second-order)
e_o	Quantization noise in RMS volts ($e_o^2 = \sigma^2/12$ is the noise variance).
ϵ_s	Permittivity of silicon.

$\epsilon (td)$	Error in amplitude when sampled.
ϕ_1, ϕ_2	Clock phases
ϕ_p	Fermi potential
f_o	Baseband bandwidth.
f_c	Cutoff frequency.
f_s	Sampling or clock frequency.
γ	Body effect gamma factor and also a weighting factor used to modify noise spectral density in sampled-data circuits.
g_m'	An equivalent transconductance $g_m' = I_o / \Delta V_{FB}$.
HD(n)	n^{th} harmonic relative to the fundamental
IMD(f_1, f_2)	Second-order intermodulation distortion product.
IMD($2f_2 - f_1$)	Third-order intermodulation distortion product.
K	Indeterminate gain of the quantizer
$L(s)$	Loop gain.
$n_{mo}(f_o)$	Net quantization noise (RMS Volts).
$N(s)$	Numerator term of the biquad transfer function.
NRZ	Non-return to Zero.
NTF	Noise Transfer Function.
σ	Quantizer span.
RZ	Return to Zero
$\Sigma\Delta M$	Sigma-delta modulator.
$S_o(f), S_n(f)$	Power spectral density of noise in $V^2/(Hz)$
$S_{cn}(f)$	Power current spectral density in $A^2/(Hz)$
SC	Switched-capacitor
SDR	Signal-to-distortion ratio.
SNR	Signal-to-noise ratio.
SN+DR	Signal-to-noise plus distortion ratio.
SR	Slew rate.
STF	Signal Transfer Function.
τ	Timing jitter and time constant
T	Clock period.
T_s	Slewing time.
t_{CGBW}	Time constant $1/\omega_{TCBW}$.

UGBW	Unity-gain bandwidth.
V_{Tn}, V_{Tp}	Threshold voltages of n-channel and p-channel devices.
V_T	General threshold voltage of a MOSFET, or thermal voltage in bipolar transistors ($V_T = KT/q$)
$v_{node}^{source}, i_{node}^{source}$	Voltage and current spectral densities where the source of noise is referred to the node.
ω_{UGBW}	UGBW in radians/sec.
z, Z	Sampled-data representation of delays. ($z = e^{j\omega T}$).

Useful Quantities and Constants

$4kT = 1.66 \times 10^{-20} \text{ [V} \cdot \text{C]}$ at room temperature, where k is Boltzmann's constant.

$q = 1.6 \times 10^{-19} \text{ [C]}$

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1.1 *Introduction*

In this thesis, an exploration into the mechanisms that limit dynamic range and bandwidth in $\Sigma\Delta$ modulator-based analog-to-digital (A/D) converters is undertaken. One of the motivations for this effort is related to the foreseeable signal-to-noise ratio (SNR) requirements of analog circuits at present and in the near future. Mixed analog-digital VLSI circuits with larger bandwidth and higher speed will be required along with the potential lower supply rail voltages. Dynamic range limiting mechanisms, both internal and external to the A/D converter, are of both academic and practical importance.

Before the advent of $\Sigma\Delta$ technology, it has been a challenging task to implement a high precision analog-to-digital converter. Such a converter was often large and rarely achieved more than 14 bits of resolution due to process variations and component mismatches [Ber88]. Furthermore, as these analog-to-digital converters often have sampling rates at the Nyquist frequency, stringent anti-aliasing requirements complicate their implementation [BW88].

Over the last decade or so, oversampled A/Ds, based on $\Sigma\Delta$ modulation have gained tremendous popularity. These modulators can achieve high resolution, but their processing bandwidth is at present, for the most part, moderate (typically less than a few hundred kilohertz). The double-integration $\Sigma\Delta$ modulator (DISDM) as proposed by Candy [Can85], shown in Figure 1.1, has the greatest popularity due to the resolution offered by the circuit as well as good immunity to instability and process variations. This structure is typically realized through the use of a biquad loop filter, comparator and 1-bit digital-to-analog converter (DAC) to trim the feedback to precision levels, as will be shown later. Oversampled analog-to-digital converters are generally smaller compared to conventional A/Ds and are unique in that they have less problems associated with the implementation of precision analog components. Such precision is often absent in processes that are optimized for digital VLSI. However, noise, nonlinearity and other mechanisms can limit the dynamic range. Preliminary

Figure 1.1 Double-integration $\Sigma\Delta$ modulator (DISDM)

research in this thesis had shown several relatively unknown and unexplored mechanisms. These included harmonic and intermodulation distortion from the input signals and intermodulation distortion from high-frequency noise spectra. It is possible for aliased components arising from nonlinear circuit elements to dictate the achievable resolution of $\Sigma\Delta$ modulators. A further motivation for this thesis is to exploit BiCMOS technology and the use of high transconductance bipolar transistors. Such a new capability can allow the present barriers imposed by CMOS technology on oversampled A/D performance to be overcome. In addition to the BiCMOS aspect of this endeavor, a venture into the design of continuous-time $\Sigma\Delta$ modulators is of increasing interest to the analog design community.

1.2 Introduction to the Fundamentals of Second-Order Sigma-Delta Modulation

$\Sigma\Delta$ modulators operate by the sampling of input signals at frequencies far greater than the Nyquist rate. The input signal is modulated to the output of the coder in the form of a pulse density modulated (PDM) digital bit stream, e.g. at the output shown as v_n in Figure 1.1. The DISDM uses only two levels of quantization for producing the PDM output of digital "1"s and "0"s. As there are only two discrete levels being fed back in this structure, it is easy to see why single bit quantizer architectures have inherently linear DACs. It is this DISDM structure that is the architecture under study, particularly in the first part of this thesis. The single-order $\Sigma\Delta$ modulator is simply a digression of the DISDM in that there is only one integrator and one feedback loop.

By immersing the quantizer inside the feedback loop, the quantization noise experiences frequency-dependent attenuation. This is important at in-band frequencies where the noise from the quantizer determines the theoretical resolution of the modulator. The integrators in the DISDM are also instrumental in providing the noise-shaping properties of the modulator. This is somewhat analogous to the manner in which a low-pass biquad filter experiences high-pass filter action from the input of the second integrator to the output of the filter. Due to the high loop gain offered by the circuit, only the noise and nonlinearity of the first integrator (referred to the input) will be significant in reducing the available dynamic range with respect to an ideal modulator. This makes the DISDM an ideal circuit to explore dynamic range limiting mechanisms since the input to the modulator acts as a wide dynamic range probe while producing a digital representation of that input to off-chip destinations in monolithic implementations.

Conventional A/Ds obtain precision through discrete levels of quantization. In $\Sigma\Delta$ modulation, quantization levels are reduced in size through the use of feedback and limit-cycle oscillations producing noise shaping [Can74]. To investigate how quantization noise is shaped, consider the z-domain representation of Figure 1.1, seen in Figure 1.2. The quantizer is replaced by a gain stage, K (which is nominally set to unity for a linear representation) and an additive noise source representative of the quantization noise, e_n . The linearizing assumption for the quantizer shown has limitations but the model will serve for initial discussion. The quantization noise is assumed to be white and uniformly distributed. To find the noise variance, the expectation value of a uniformly distributed process between the intervals of $-\sigma/2$

Figure 1.2 Z-domain representation of Figure 1.1

and $\sigma/2$ with a zero mean, as seen in the probability density function (PDF) of Figure 1.3, is $e_o^2 = \sigma^2/12$ where σ is the quantization step size [Pap84] [Nor90].

Under the linearizing assumption, the z-domain transfer function is found from Figure 1.2 to be

$$V_o(z) = V_i(z) + (1 - z^{-1})^2 e_o \quad \text{Eqn 1.1}$$

Eqn 1.1 shows that the quantized signals at the output of the modulator represent the input signal in addition to an additive quantization noise component that is high-pass filtered or noise shaped. Now considering the magnitude squared of a first-order noise transfer function,

Figure 1.3 Quantization noise probability density function (PDF)

$$|H(z)|^2_{z=e^{j\omega}} = |1 - z^{-1}|^2 = (1 - z^{-1})(1 - z^1) = 4\sin^2(\pi f/f_s) \quad \text{Eqn 1.2}$$

A plot of the quantization noise transfer function (magnitude) as a function of normalized frequency f_o/f_s , may be seen in Figure 1.4, where f_s is the sampling frequency. To generalize, the quantization noise of an n -order $\Sigma\Delta$ modulator goes through to the output as $V_o/e_o = (1 - z^{-1})^n$. Hence, the quantization noise at in-band frequencies may be reduced by either increasing the oversampling ratio (of sampling frequency to the Nyquist rate) or by increasing the order of the converter.

Figure 1.4 Magnitude of the quantization noise transfer function

To make the oversampled A/D viable in most applications, the unwanted high-frequency quantization noise seen at the output must be low-pass filtered and the PDM bit stream converted to the more conventional multi-bit pulse code modulated (PCM) digital representation, decimated to the Nyquist rate [Can85], [UCL90]. This low-pass filter is realized in its simplest form as an FIR filter. Low-pass filtering the bit stream is necessary to keep the baseband of in-

terest as denoted in Figure 1.4. Not only does low-pass filtering keep the integrated RMS quantization noise to a minimum, but performing the filtering at the decimation filter stage satisfies anti-aliasing requirements. Furthermore, the act of decimation reduces kT/C noise as dictated by the oversampling ratio, which is defined as the ratio of the clock to the Nyquist frequency [HB86].

Noise propagates through an n^{th} -order system yielding the mean squared voltage as defined by

$$v_{on}^2(f) = \int_0^{f_o} S_o(f) |H(z)|^{2n} df \quad \text{Eqn 1.3}$$

Here, $|H(z)|^2 = |(1 - z^{-1})|^2 = 4 \sin^2(\pi(f/f_s))$. The single-sided noise spectral density from the variance $e_o^2 = \sigma^2/12$ based on previous assumptions is modified by the act of sampling so that

$$S_o(f) = e_o^2 \frac{2}{f_s} \quad \text{Eqn 1.4}$$

This is because the total noise power is confined between DC and $f_s/2$ to the value of $\sigma^2/12$, which is consistent with the uniform assumption of the uniform quantization noise between the interval $-\sigma/2$ and $\sigma/2$. Once again, the advantages of oversampling are clearly demonstrated. Sampling with a frequency greater than the Nyquist causes a reduction in the quantization noise even before it gets filtered. Hence for the second-order system under consideration,

$$v_{on}^2(f) = \int_0^{f_o} \frac{2}{f_s} e_o^2 \left[4 \sin^2\left(\pi \frac{f}{f_s}\right) \right]^2 df \quad \text{Eqn 1.5}$$

which yields the classical result [Can85]

$$v_{on}(f_o) = \frac{e_o \pi^2}{\sqrt{5}} \left(\frac{2f_o}{f_s} \right)^{5/2} \quad \text{Eqn 1.6}$$

The above result of Eqn 1.6 describes the net integrated RMS quantization noise in the base-band, f_o , for a second-order $\Sigma\Delta$ modulator.

The discussion on the fundamentals of $\Sigma\Delta$ modulation has been centered upon the DISDM structure used in this thesis. It should be noted that other architectures exist which are varia-

tions of the $\Sigma\Delta$ modulation process. Some of these, such as the multi-stage or cascode structures, attempt to reduce the sampling rate by increasing the order of noise-shaping and maximizing dynamic range. Other structures reduce the modulation rate by using multi-level quantization [Can74]. These structures can lose some of the fundamental advantages such as simplicity and immunity from process flaws and nonidealities in the elements. However, recent advances through noise shaping the element mismatch [LBZ⁺96] has made multi-bit DAC architectures more approachable. A detailed comparison of these fundamental structures and their limitations has already been published [Rib91] and is not repeated here.

In the context of the DISDM, more general information may be found in Candy's papers [Can74], [CB81], [Can85] as well as a host of other papers on oversampled A/Ds [Dar90] [Hau91]. Specific design issues will be covered in upcoming chapters.

1.3 *Sampled-Data and Continuous-Time Modulator Design in BiCMOS*

The bandwidth of $\Sigma\Delta$ modulators may potentially be extended with BiCMOS processes that exploit high transconductance bipolar transistors. These transistors have superior high frequency and noise characteristics as compared to their CMOS counterparts. A particular advantage, in terms of maximizing the dynamic range, is the reduction of $1/f$ and thermal noise from the use of bipolar transistors.

Baseband frequencies in sampled-data DISDMs may be extended by designing the opamps to have greater bandwidth which in turn gives license to raise the clock frequency. Lower noise characteristics and greater bandwidths depend primarily on increasing the transconductance of the differential pair at the input of the opamps.

An important way to reduce aliasing in the context of oversampled A/Ds is to move away from the usual method of implementing $\Sigma\Delta$ modulators as switched-capacitor circuits, (Figure 1.5a), and instead implement them as continuous-time alternatives [KHE⁺86] as shown in Figure 1.5b). This has other benefits in that greater bandwidths come automatically with continuous-time as opposed to sampled-data circuits. A comparison of continuous-time to sampled-data circuits follows.

Figure 1.5 a) Typical switched-capacitor DISDM

Figure 1.5 b) A novel g_mC -based oversampled A/D using multiple differential input pairs.

Sampled-data circuits typically require small area and are extremely temperature insensitive if switched capacitors are used. Correlated double sampling or chopper stabilization may be used to reduce $1/f$ noise, in opamps that use CMOS differential input pairs. Finite gain compensation schemes may also be used to reduce the effects of finite opamp gain. In serial structures, this is not a big concern with good design. However, as multi-stage structures rely on the cancellation of quantization noise, any error from opamp finite gain causes the quantization noise spectra to degrade due to the pole associated with leaky integrators [UHK⁺88],

[UCL90]. Furthermore, charge injection and other well known effects may degrade the performance of the sampled-data circuit. In the proper design of sampled-data circuits, appropriate settling of the opamps must take place and clock jitter must be kept low so as not to introduce any unwanted noise.

Perhaps one of the biggest problems associated with sampled-data circuits is the problem of aliased noise. In continuous-time circuits, the problems of aliasing are reduced. There is no thermal switch noise, nor is there any charge injection. Note however that in continuous-time circuits finite gain compensation techniques are no longer available to reduce the effects of $1/f$ noise or opamp finite gain. A continuous-time, multi-stage $\Sigma\Delta$ modulator might be limited in performance because of this. Another problem in continuous-time implementations may be expected if high levels of external clock jitter are present which can cause a decrease in the dynamic range.

The opamp-based integrator used in the sampled-data DISDM may be replaced with an operational transconductance amplifier (OTA-based) integrator for the use in continuous-time modulators (as in the example in Figure 1.5b). As the OTA is always run locally in open-loop (integrator configuration), there are no virtual ground restrictions. Through the use of the OTA (which is nothing more than a voltage-to-current converter) and current steering, a continuous-time $\Sigma\Delta$ modulator has been designed in this thesis to operate in the low megahertz range, a considerable increase in bandwidths typical in $\Sigma\Delta$ modulators.

It will be shown that the design of continuous-time $\Sigma\Delta$ modulators may draw upon sampled-data design concepts and practices already in existence. For example, there is a simple transformation that may be used between the continuous-time and sampled-data domains that allows the design of a continuous-time $\Sigma\Delta$ modulator from a sampled-data modulator, making the design process easier through equivalence.

1.4 Noise and Nonlinearity

A central theme in this thesis is the study of how circuit noise and nonlinearity manifests itself through to the output of the modulator. Ideally, the spectrally-shaped quantization noise would dictate the resolution of the $\Sigma\Delta$ modulator. In reality however, thermal and $1/f$ noises often reduce the available SNR. With the recent availability of bipolar transistors in BiCMOS pro-

cesses, these sources of noise may be decreased with judicious design. Switched-capacitor resistor (or kT/C) noise and amplifier noise must be determined as part of the design process.

Noise in the OTA-based circuits is less trivial to calculate since multiple differential input pairs are used for summing signals, as shown in Figure 1.5b). A methodology is required to determine the noise at the output of the continuous-time modulator. This type of circuit has the potential for low noise high-bandwidth applications. This however comes at the expense of linearity, as will be shown.

Circuit nonlinearity, in the most fundamental sense, causes harmonic distortion (signal components at multiples of the input frequency) to be seen at the output of the $\Sigma\Delta$ modulator. Nonlinearity of $\Sigma\Delta$ modulators is not discussed in any detail in the literature, particularly from the theoretical point of view. It has however been recognized, primarily through simulation, as a mechanism that limits dynamic range [RBG⁺91].

In order to proceed with the analysis of harmonic distortion, a more involved approach in determining the signal transfer function (STF) is required. This entails characterizing the behavior of the loop through studying the quantizer's gain K . Establishing the validity of K allows a more straightforward framework to deal with nonlinearity issues.

Even though many sources of circuit nonlinearity exist, the dominant sources are considered to come from amplifiers. Furthermore, since quantization noise in reality is not white but somewhat correlated with the input signal, it is possible for nonlinear effects to take place on high-frequency quantization noise spurs or tones that arise from limit-cycle behavior of the $\Sigma\Delta$ modulator. This may result in baseband contamination from intermodulation of these spurs. This has been reported as seen from measurement [KHE+86], but the mechanism has not been explained, simulated or quantitatively dealt with. This thesis attempts to explore this mechanism in detail.

Since it is desirable to increase the usable bandwidth of these A/Ds, it is imperative to understand how nonlinearity can affect the available dynamic range of the system. This is because opamp-based circuits trade off open-loop gain for bandwidth. Since nonlinearity increases as open-loop gain decreases, the nonlinearity issues become much more important in higher bandwidth circuits.

1.5 Summary of Goals

It is the intention of this thesis to address the dynamic range limiting mechanisms described above that occur in both sampled-data and continuous-time oversampled A/Ds. This thesis presents both a moderate-speed sampled-data DISDM and a novel high-bandwidth transconductor-based oversampled A/D designed and fabricated in a 0.8 micron BiCMOS process. Pertinent studies on these structures are conducted as described below.

This thesis looks at extending a known method of distortion analysis from nonlinear opamps to include frequency dependence in the sampled-data DISDM. Of particular interest, with regards to this circuit nonlinearity, is an investigation into how high-frequency spurs can intermodulate down to baseband frequencies causing diminished dynamic range. Through an investigation into the gain of the quantizer, it is the intention of this document to enhance the accuracy and understanding of the oversampled A/D's signal transfer function. This in turn provides accuracy in the prediction of distortion product magnitudes. Furthermore, understanding the gain of the quantizer and how it affects the noise transfer function also allows refined estimates of the quantization noise spectrum from the effects of finite amplifier gain.

The design and evaluation of a novel transconductor-based wideband oversampled A/Ds is also presented. Its bandwidth is at an order of magnitude greater than what was commonplace at the time the circuit went to fabrication. Although the emphasis is primarily on low-frequency, the noise and nonlinearity of these devices, as well as their constituent loop filters, are also studied.

1.6 Thesis Organization

In this chapter, motivations for the exploration of relatively unknown dynamic range limiting mechanisms have been provided, and the topic of sampled-data and continuous-time $\Sigma\Delta$ modulators has been introduced. A general introduction into oversampling theory has been given, with emphasis on the second-order modulator which is used extensively in this thesis.

The second chapter acts as background and describes performance aspects of the sampled-data DISDM. The chapter starts with a basic system-level simulation and the concept of how dynamic range is evaluated in oversampled A/Ds. By then considering coefficient selection,

slew rate and settling limitations in addition to other dynamic range limiting mechanisms, a basis for the design of the sampled-data DISDM is formed. It should be noted that the principles that describe the sampled-data system also are, for the most part, applicable to the continuous-time system.

In the serial oversampled A/D structures used in this thesis, the simulations in Chapter 2 are extended to explore lesser known mechanisms such as circuit nonlinearity. In particular, the way in which opamp nonlinearity can limit the achievable dynamic range of a system is shown. A deeper look at DISDMs is taken with emphasis on aspects of the quantizer gain, in an attempt to extend the usability of the linearized model of the DISDM so that it can deal with dynamic range issues better.

With the knowledge gained from the preceding performance evaluations, the design of the sampled-data DISDM may begin in Chapter 3. The opamp used, being perhaps the most important circuit component in the oversampled A/D, is theoretically analyzed for thermal and $1/f$ noise. The manner in which all noise sources go through to the output of the modulator is analyzed and discussed. Furthermore, the design of the switches, capacitors and the comparator is presented. Finally, the fabricated opamp is characterized, with particular attention to the linearity of the device.

Chapter 4 concentrates on theoretical analysis of the DISDM, in order to explain and estimate harmonic distortion levels due to circuit nonlinearity. However, in order to more accurately do so, a better comprehension must be obtained of how the behavior of the quantizer affects the DISDM characteristics. Thus, a great deal of effort is expended in revisiting the typical linearized view of the DISDM's signal and noise transfer functions with particular attention to the gain of the quantizer. Once this has been accomplished, the theoretical intermodulation distortion products from circuit nonlinearity may be attained. Furthermore, the distortion products that come about from high-amplitude, highly-correlated quantization noise spurs may be estimated. These theoretical levels of distortion are then compared to measurement. The effects of finite opamp gain on the DISDM are covered with greater accuracy than before.

Chapter 5 draws on much of what was built upon already in the previous chapters. In an attempt to increase usable bandwidths, experimental OTA-based circuits are designed and fabricated. Once again, amplifier noise and nonlinearity must be considered. After a simple

analogy is drawn between sampled-data and continuous-time oversampled A/Ds, the design of continuous-time oversampled A/Ds is presented. The OTAs utilize current steering techniques, with integration performed internal to the amplifier.

Due to the nature of the Gilbert gain cell based OTA used in this design, noise analysis and verification is essential. Unlike conventional opamps, the OTAs have multiple differential input pairs for the summation of signals. The noise analysis is verified by measurement of a loop filter version without the quantizer. The differences between the expected result from the filter and the oversampled A/D are discussed.

Finally, in Chapter 6 a summary of the thesis is presented with considerations for future work.

Background and the Performance of Sigma- Delta Modulators

2.1 Introduction

This chapter acts as background for upcoming chapters and reviews several topics that pertain to the performance and understanding of $\Sigma\Delta$ modulators. The review is a precursor to the underlying key topics of noise and circuit nonlinearity that are a major focus in this thesis in addition to the experimental circuit designs presented here.

The first portion of this chapter is dedicated to a study expedited through the use of system level simulations for the most part. It is meant to provide the reader with a basic familiarity of oversampled A/Ds while enhanced simulations provide insight into subtleties that cause limitations in performance.

There have been, in the past, several publications that discuss some of the design and performance limitations in $\Sigma\Delta$ modulators [Can85], [BW88], [HB86]. Included in the simulation study presented in this chapter are the effects of settling time, slew rate limitations and coefficient selection to a lesser extent. These evaluations are useful in that they validate and ensure stability of the design of the DISDM seen in the next chapter.

The all-too-familiar linearized model discussed in the Introduction (Chapter 1) is not accurate enough to obtain reasonable estimates of intermodulation distortion in the baseband when inputs or large tones exist at frequencies beyond the baseband. The reason for this will be divulged and the rationale for this focus is as follows.

It has been briefly mentioned previously [KHE+86] that circuit nonlinearity may cause highly correlated (i.e. non-random) high-frequency spectra to intermodulate down to baseband frequencies. In fact, nonlinearity is rarely discussed in the literature with any amount of detail. Thus an attempt to demonstrate the effect of nonlinear integrators in the DISDM is made in which corruption of the baseband may take place. Through simulation, it will be shown that circuit nonlinearity indeed produces these effects, which can occur in both sampled-data and continuous-time modulators. Consequently, as background for upcoming chapters, a mathematical review of nonlinearity is provided.

In upcoming chapters, it will be shown that the accuracy of the STF and NTF is crucial to good estimates of distortion and other effects. The quantizer gain is instrumental to this accuracy (as well as to stability). This topic, and how the gain is measured, will be discussed later.

2.2 Ideal Double Integration Sigma-Delta Modulator

An elaboration of the linearized Candy DISDM of Figure 1.1 is shown in Figure 2.1. The z -transform for this idealized structure leads to

$$V_e = \frac{K\alpha_1\alpha_2 V_i + (1 - z^{-1})^2 e_o}{K\alpha_2\alpha_4 z^{-1} + [1 - (1 - K\alpha_3)z^{-1}][1 - z^{-1}]} \quad \text{Eqn 2.1}$$

Where the quantizer has been replaced by a gain element and an additive noise source such that $V_o = KV_o2 + e_o$. This may be separated into the signal and noise transfer functions (STF and NTF) respectively

$$STF = \frac{V_o(z)}{V_i(z)} = \frac{K\alpha_1\alpha_2}{K\alpha_2\alpha_4 z^{-1} + [1 - (1 - K\alpha_3)z^{-1}][1 - z^{-1}]} \quad \text{Eqn 2.1a}$$

$$NTF = \frac{V_o(z)}{e_o(z)} = \frac{[1 - z^{-1}]^2}{K\alpha_2\alpha_4 z^{-1} + [1 - (1 - K\alpha_3)z^{-1}][1 - z^{-1}]} \quad \text{Eqn 2.1b}$$

where K is commonly defaulted to unity for a linear representation of the system [Can85]. In fact, the gain K is rarely unity and the effect of this gain element plays a more important role than is often realized. K is defined as the gain of the quantizer and may be explained with a practical example. If a signal with a certain frequency is applied to the input of the modulator, then there exists a component of that signal at the output of the second integrator at the same frequency which experiences gain (K) to the output of the modulator. Suffice it to say that the gain K changes under different conditions, e.g. when the input to the modulator approaches high input amplitudes [AP87]. This subject is treated in much greater detail later, but for now the gain may be assumed and remain as unity for simplicity. In addition, note that here the indeterminate gain of the quantizer K is considered to act on both the signal and noise paths. This is the classic manner in which K is handled [Sti88] but it can also be treated separately for both paths [AP87].

Figure 2.1 Ideal DISDM

These following simulations are intended to bring out some important points as a background for the later design and theoretical issues (see Appendix A for program listing). An arbitrary sampling frequency of 10.24 MHz is chosen with a 10 kHz fundamental tone. The baseband is assumed to extend to 40 kHz.

The first simulation is not unusual as it is the result of the simple difference equation indicated by Eqn 2.1 with the addition of a simple quantizer action, for the ideal and degenerate case (all

Figure 2.2a

8 Kpoint FFT of the output bit-stream yielding the quantization noise spectrum for the ideal modulator. Note the existence of harmonics from bit-stream saturation at multiples of the input frequency when input amplitude is high.

Figure 2.2b

FFT (-3 dB Input Amplitude)

Figure 2.2c FFT (-6 dB Input)

Figure 2.2d FFT. (-12 dB Input) Note the 40 dB/dec slope indicative of second-order noise shaping

gain coefficients are unity with no integrator clipping). The results are shown in Figure 2.2a) and Figure 2.2b). Here, an 8 Kpoint FFT is performed with sinusoidal waveforms of varying amplitudes applied to the input. Generally, the amplitude of the spectral components may be expressed in dBV/Hz, dBm/Hz or dB/Hz. dB/Hz is a relative spectral density in dB with respect to the resolution bandwidth of the bin. For example, the $dB/(1250Hz)$ on the y-axis of these plots denotes the resolution bandwidth of the bin for the 8 Kpoint FFT used in this instance normalized with respect to a $\Delta = \pm 1V$ full-scale. dBV/(Hz) is just the RMS version of this. The signal-to-noise ratio (SNR in decibels) shown on the Figures compares the signal amplitude at the modulator's output to the net noise integrated from DC to the desired bandwidth (40 kHz here).

Figure 2.2a) shows the modulator's output spectrum for a 0 dB input. It may be seen that large harmonics are generated at multiples of the input signal frequency (10 kHz) and that the frequency spectra does not reflect second-order noise shaping (i.e. does not have a clear 40 dB/dec rolloff). This comes about because the modulator operates in the "overload" region which occurs when a large input, whose amplitude is comparable to the quantizer level, drives the integrators to accumulate levels far in excess of the quantizer's span. The result is a bit-stream output that resembles a clipped sinewave (approaching a squarewave) and is called "bit-stream saturation" here. It is thus of interest to avoid operating in this region since harmonics from this effect do not come from circuit nonlinearity, a key topic in this thesis that will be explored later. It should be noted that by circuit nonlinearity, mechanisms other than those associated with the quantizer are meant.

As regards Figure 2.2b) through to Figure 2.2d), it may be seen that a decreasing amplitude causes the modulator to operate in the linear region rather than the overload region as in Figure 2.2a). This is depicted by the expected second-order noise shaped spectra and the absence of harmonics.

Up to now, the linearized transfer functions have served to introduce the basic operation of the DISDM. Figure 2.3) shows the expected NTF for K equal to unity with the quantizer linearized as in Eqn 2.1. However, upon closer examination with the simulation of Figure 2.2d), it is clear that the high-frequency quantization noise behavior does not follow a constant upward trend with frequency as expected. It appears that the resonant peak in simulation has decreased in frequency by comparison to what might be expected from the familiar linearized

Figure 2.3 Noise Transfer Functions of the DISDM with the assumed $K = 1$ and more realistic $K = 0.5$.

model seen in Figure 2.1. Thus a discrepancy exists between the transfer function of Eqn 2.1, derived from simple difference equations with $K = 1$, and simulation (i.e. Figure 2.2d).

Upon examination of Eqn 2.1, it may be seen that the noise transfer function experiences a pole from the $[1 - (1 - K\alpha_3)z^{-1}]$ term. Since all the α 's are unity, the K term simply cannot be unity, but rather a definitive value as yet unknown. Rather, the simulation bears a striking resemblance to Figure 2.3), where $K = 0.5$ as an example. Further analysis and discussion later in the thesis will illustrate that the loop in fact sets a value for the gain K . Thus, a deeper look into this issue is necessary because it potentially allows a more simplified view of quantization noise and nonlinearity issues. The exploration into this model will be discussed further.

2.3 Further Dynamic Range Limiting Mechanisms and System-Level Issues

The classic Candy equation (Eqn 1.6) yields the ideal dynamic range from quantization noise alone. Demonstrated in the last section was a simple example where the dynamic range of the

oversampled A/D departed from this ideal due to quantizer overload conditions. Following are issues pertaining to other dynamic range limiting mechanisms whose effects can be easily simulated.

2.3.1 DISDM Operation Including the Effects of Integrator Clipping

It can be shown through simulation that integrator clipping causes a further loss of dynamic range through the generation of harmonics seen at the output of the DISDM. Particularly, for the purposes of studying distortion from circuit (i.e. opamp and capacitor) nonlinearity, it must be shown that the harmonics generated from clipping is far less than the harmonics generated from circuit nonlinearity.

Simulations were run with the imposition of finite rail voltages (see Appendix A, Section A.2) in an attempt to determine how performance is affected in general. A comparison was made between the unclipped modulator against the clipped modulator. The main difference shows up as a shift in the maximum peak SNR resulting in a reduction in the dynamic range by several dB in the clipped integrator case. At lower input levels, integrator clipping no longer occurs and the dynamic range plots merge at around the -10 dB level for the degenerate case. Linearity issues that arise below input levels that cause clipping are a major focus of this thesis. However, it is important to point out that harmonics generated from clipping are relatively low in amplitude and are not expected to compete with those generated from circuit nonlinearity in regions where the SNDR is degraded from clipping alone.

2.3.2 Coefficient Selection

Given any dynamic range limiting mechanism, the manner in which the effect manifests itself at the output of the modulator most often depends upon coefficient selection. There are several factors that must be considered when attempting to set values for the gain coefficients. These include the fundamental operation of the modulator (i.e. setting the STF and NTF), electronic noise, the way in which such noise gets through to the output of the modulator, and stability. These topics will be covered separately. Detailed simulation and discussion on gain coefficients may be seen in Appendix A, Section A.3. The following table summarizes the key

points regarding dynamic range as a function of coefficient selection as mostly supported by simulations from the Appendix.

Coefficient Changed	Results
Decrease α_1	<ol style="list-style-type: none"> 1) STF lowered in magnitude 2) Input-referred opamp noise decreases, but not as fast as STF decreases; hence a loss of dynamic range from this source^d. 3) NTF unaffected 4) Integrator clipping decreases; hence an increase in dynamic range from this source.
Decrease α_2 and α_3 ^b	<ol style="list-style-type: none"> 1) STF unaffected^c 2) NTF unaffected^d 3) Integrator clipping decreases; hence improved dynamic range from this source. Beware that the quantizer must be able to resolve the smaller signals.
Decrease α_1 alone	<ol style="list-style-type: none"> 1) NTF is affected, bringing poles towards baseband frequencies. 2) Causes slight increase in quantization noise at inband frequencies; hence slight loss of dynamic range. 3) Decrease in integrator clipping; results in an increase in dynamic range typically more so than the loss from increased quantization noise stated above.
Decrease α_1 and α_3 equally	<ol style="list-style-type: none"> 1) STF unaffected 2) NTF increases in magnitude; hence a loss in dynamic range. 3) Integrator clipping decreases; thus an increase of dynamic range occurs^c.
Decrease α_3 alone	<ol style="list-style-type: none"> 1) STF increases in magnitude 2) NTF increases equally with STF; hence no change in dynamic range. 3) Input-referred opamp noise is suppressed more; thus an increase in dynamic range.

Table 3.1: Summary of dynamic range consequences as a function of coefficient selection.

- a. There is a dynamic range trade-off between point 2) and 4).
- b. Also mostly true when α_2 is changed alone.
- c. Gain of the quantizer K plays a role in compensating both the STF and NTF as will be discussed later. This is particularly true when changes in α_2 equal changes in α_3 .
- d. See c. above.
- e. There is a dynamic range trade-off between point 2) and 3).

It should be noted that, ultimately, the noise transfer function is set by these coefficients and often, the coefficients are adjusted in tandem so as to typically reduce integrator clipping while preserving the desired NTF and simultaneously attempting to avoid a loss of SNR from other sources (i.e. as in the case of decreasing α_2 and α_1).

2.3.3 Sampled-Data Integrator Considerations

The choice of coefficients also affects the speed of the modulator through the changed capacitive loading implied by changed coefficient values. The integrator's step-by-step transient response in sampled-data circuits is approximately equal to [TA85]

$$\tau = \frac{t_{UGBW}}{\beta} = \frac{1 + C_{in}/C_I}{\omega_{UGBW}} \quad \text{Eqn 2.2}$$

where β is the feedback factor in the control systems context ω_{UGBW} and t_{UGBW} are the integrator's UGBW and associated time constant, C_{in} is the input capacitor and C_I is the integration capacitor. This equation is valid only for single time-constant opamps, however; it provides a guideline in predicting the amount of time required for the output of two-stage opamps to settle.

2.3.4 Slew Rate and Settling Requirements in Sampled-Data Modulators

Ideally, it would be desirable for the outputs internal to the $\Sigma\Delta$ modulator to settle linearly, to produce a fixed (i.e. expressed as a percentage) settling error. As a result, a lack of settling would appear like a capacitor ratio error, which is well known not to adversely affect the operation of the modulator. Furthermore, it has been reported that $\Sigma\Delta$ modulators are tolerant to insufficient settling [BW88], [HB86]. This might be considered surprising since feedback is relatively large and considerable slewing takes place which robs available settling time. Considering the proposed architecture of having all the gain coefficients set to unity, it is prudent to simulate the effects of insufficient settling and compare it other researcher's findings whose gain coefficients were different.

A simulation study (Appendix A, Section A.4) was conducted into the loss of dynamic range as a function of slew rate and settling of signals at the output of opamps. Simulations were performed that allowed the output of the opamp to experience slew rate limiting followed by a

linear settling process analogous to single-time constant (single-stage) opamps. This is just an estimate since settling typically takes longer due to the use of a two-stage opamp in the design.

A desired dynamic range (or number of bits resolution) may be translated into an equivalent settling error. From this, and given a desired clock speed, the integrator time constant may be found which in turn dictates the UGBW of the opamp. Typically, the desired clock frequency will have already been determined according to the desired resolution and baseband frequency from Candy's equation (Eqn 1.6). Using the above settling error as a maximum, the necessary unity-gain bandwidth (UGBW) of the opamp may now be found from Eqn 2.2 and Eqn 2.3 below regarding the settling error, $Error_{settling}$.

$$Error_{settling} = e^{-(t_{settle})/\tau} \quad \text{Eqn 2.3}$$

The results from simulation showed that as much as 80% of the allowable integration time ($T/2$) time could be occupied by slewing before any degradation in performance was noticed. This was manifested as a shift in the peak signal-to-distortion + noise ratio (SNDR) seen first at high input levels from increased harmonic distortion.

Clearly, the settling times are insufficient at this point and worsening them makes no appreciable difference which seems to support other researcher's findings [BW88], [CNI⁺90] that the integrator time constants can be quite large, almost a secondary requirement next to slew rate.

For the architecture used in this thesis, the maximum output swing may be estimated from 1V at the input added to 1V from feedback for a total of 2V. This 2V may be added to a 1V from feedback at the output of the second integrator for the degenerate case for a maximum of a 3V excursion. From simulations just presented and knowing that the tolerance to slewing can be as high as 80%, a maximum bound may be calculated to which the minimum slew rate can be calculated. The maximum time allowed for slewing is thus

$$T_{MAX} = \frac{T}{2} (0.80) \quad \text{Eqn 2.4}$$

and the maximum voltage is 3V or, in general terms, $3 \times \Delta/2$ where Δ is the quantizer span and is equal to 2V here, then the minimum slew rate that can be tolerated for the second integrator is

$$SR = \frac{\Delta V}{\Delta T} = \frac{3(\Delta/2)}{\frac{T}{2}(0.80)} = 3.75 \frac{\Delta}{T} \quad \text{Eqn 2.5}$$

This yields a slew rate of 76.8V/ μ S, which is close to 70 V/ μ S used in simulation (shown in the Appendix), showing the border line of safe operation. For slew rates less than this, harmonics appear in the baseband causing a reduction in the dynamic range due to a loss of SNDR at high input amplitudes to the modulator as a result of insufficient slewing ability. The harmonics that are generated from this mechanism should not be confused with harmonics that come about from the voltage dependent gain of the opamp or voltage dependence of capacitors within the integrator. When faced with the generation of harmonics as a result of insufficient slew-rate or settling, a reduction in the clock frequency is required.

Boser and Wooley [BW88] came to an empirical formula based on simulation that suggests the same inherent characteristics. To reiterate their formula

$$SR > 1.1 \frac{\Delta}{T} \quad \text{Eqn 2.6}$$

This was valid for an architecture that contained gains (the α coefficients) of 1/2 at each integrator and are comparable to Eqn 2.5 after the voltages at the output of the second integrator are scaled to match.

It is also prudent to consider the effects of uneven slew rates often found in opamps, particularly when the rates are marginal as regards optimal dynamic range. From simulation it was shown that a weak positive or negative slew rate yielded the same performance degradation as if both slew rates had been equally weakened. Thus, the worst case slew rate must be taken into account.

2.3.5 System-Level Simulations with Nonlinear Integrators.

In keeping with the theme of this chapter, this section introduces some of the manifestations of circuit nonlinearity in DISDMs through the use of a simulation for illustration only. This topic is explored in detail in the next chapter, with additional simulations and theory as they relate to the fabricated modulator. As was briefly discussed, integrator nonlinearity comes about from nonlinear capacitors and opamps. The dominant contributor however is opamp

nonlinearity since in modern processes, the capacitors are of the poly-poly configuration which are highly linear [Ber88].

It has already been reported that the consequence of integrator nonlinearity is harmonic distortion which limits the maximum SNR possible at high input amplitudes. This conclusion was reached by simulating the DISDM using a nonlinear integrator model as described by Boser and Wooley [BW88] which was reinforced by highly simplified theoretical calculations that were valid at low frequency only. By using a Taylor series expansion representative of the nonlinear integrator [BW88], [UCL⁺90], [LM85], [Ber88], [RBC⁺91], it is a simple matter to replace the linear model with the nonlinear one so that a system-level or macromodel simulation may be performed. Simply, the nonlinear integrator replaces the linear one by using a set of equations. The opamp nonlinearity implicit to the integrator may be written as a power series expansion to the third order as a function of the difference-mode voltage, v_d .

$$v_o = a_1 v_d + a_2 v_d^2 + a_3 v_d^3 \quad \text{Eqn 2.7}$$

where the coefficients a_n represent the open-loop linearity coefficients of the opamp. Taking finite gain into account, the integrator shown in Figure 2.4 has a charge balance equation (this

Figure 2.4 Integrator including finite gain

analysis will be seen in its entirety in the Chapter 4)

$$\alpha_1 (v_i - v_d) + \alpha_2 (v_i - v_d) = (v_o - v_d) + (v_{o,n-1} - v_{d,n-1}) \quad \text{Eqn 2.8}$$

where $\alpha_1 = C_1/C_f$ and $\alpha_2 = C_2/C_f$. By substituting Eqn 2.7 into Eqn 2.8, a polynomial as a function of v_d may then be found. After determining the difference-mode voltage, the output v_o is then easily found according to Eqn 2.7.

There are several ways to determine v_d . Given v_i , v_o , $v_{d,n-1}$ and $v_{o,n-1}$, then v_d may be solved for either mathematically as in a system-level simulator (difficult for high-order polynomials) or iteratively, as in commercial software (i.e. HSPICE or ELDO) through the use of macro-modelling. Here, a voltage-controlled voltage source that uses the polynomial option that describes the opamp nonlinearity may be used. Of course, a full circuit level time-domain simulation would show the effects of nonlinearity, e.g. from the opamp, but this would computationally be difficult and prohibitive. In the next chapter, this difference-mode voltage in essence is approximated through analysis, the accuracy of which may be confirmed through either macromodel or postlayout simulation.

As mentioned earlier, there is limited understanding as to how circuit nonlinearity propagates in the DISDM. It has been previously known that voltage dependent gain of the integrators leads to harmonic distortion seen at the output of the modulator as found through simulation [UCL⁺90] [RBG⁺91]. It was also reported, as found in measurement only, that high-frequency spurs (i.e. tones that appear to rise up out of the quantization noise), may alias to baseband [KHE+86]. This phenomenon will be simulated here and later analyzed in Chapter 4. As a preliminary first step in the study of nonlinearity in $\Sigma\Delta$ modulators, simulations were conducted which included nonlinear integrators in the loop.

At high input amplitudes, harmonics at multiples of the input frequency are generated which degrade the available dynamic range as expected. However, it was discovered that after these harmonics disappeared below the quantization noise floor by decreasing the input level, other harmonics appeared in the baseband, at different, unexpected frequencies. An example of such a simulation is shown in Figure 2.5a), where the baseband frequency response is found for a 10 kHz low-amplitude input sinewave to the modulator. The integrators contain relatively nonlinear 50 dB DC gain opamps for illustration here only. As may be seen, there are strong frequency components that exist at approximately 2.3 kHz, 12.3 kHz, and 22.3 kHz and so on for this particular simulation run. This is due to the intermodulation of high-frequency, highly correlated tones or spurs that exist near half the 10.24 MHz clock frequency, some of which are seen in Figure 2.5b). This is a further effect of circuit nonlinearity impinging upon the per-

Figure 2.5a

Baseband frequencies of a simulation FFT with -40 dB input amplitude to the modulator. Opamp used is low gain and nonlinear (Blackman-Harris Window used prior to performing the FFT)

Figure 2.5b

Frequency spectrum of the quantization noise near half the clock frequency ($f/2 = 5.12\text{MHz}$)

formance of the DISDM. High amplitude spurs spaced at frequencies equal to the input frequency, as well as other frequencies (i.e. approximately 2.3 kHz here), exist and are a consequence of the limit-cycle behavior of the oversampled A/D. This effect will be discussed at greater length later. It is worth noting that there is a SNDR advantage by introducing dither [Sne96],[Risbo] that reduces the magnitude of these high-frequency spurs at the expense of increased baseband noise. Although this solution may be viable in many applications, it is of prime importance to understand how these spurs intermodulate and exactly how these intermodulation products might be suppressed by high opamp gain as another solution that avoids the trade-off mentioned earlier.

It should also be noted that it is possible for single tones to appear in the baseband with DC inputs [BWW91], [LI93]. This should not be confused with the multiple tones related to the intermodulation of the high frequency spurs as described and seen from simulation. The amplitude of the tones here are much larger than predicted from a tone generated from a DC input for this oversampling ratio. Also, these tones do not increase in amplitude with increasing frequency according to the shape of the quantization noise spectra as do tones generated from DC inputs do. The mechanism of intermodulation distortion and how these tones alias back down to baseband is covered extensively in Chapter 4.

2.4 A Deeper Look at DISDMs and the Gain of the Quantizer

Up to now, the operation of the DISDM was observed through the use of system-level simulation assisted with a fundamental and familiar linearized model of the DISDM. This was sufficient to provide a basic understanding of some of the issues regarding the design of the DISDM as well as providing a useful tool to validate any given design, as will be demonstrated in the next chapter. However, it was established early on that the gain of the quantizer can not be ignored (i.e. same as setting the gain to an arbitrary value of unity) as is most often done in the literature. Such an assumption may lead to inaccurate STF and NTFs as already demonstrated. It is prudent and necessary to characterize the gain of the quantizer and validate its use as its properties must be known for upcoming analysis to be accurate.

2.4.1 Modelling the Behavior of the Quantizer

The DISDM is in essence a sampled-data biquad filter with a nonlinear quantizer (and 1-bit DAC) embedded in the loop as shown in Figure 2.6a). The time consumed by the quantizer in effect causes a delay in the feedback path. By ignoring the gain of the quantizer, the z-transform for this Figure would lead to a flat STF for the degenerate DISDM used here. This is in fact highly improbable, as will be shown shortly. To help understand why this is so, consider the operation of the quantizer.

It must be realized that a signum function, contained implicitly within the comparator, causes the quantizer to absorb a signal of any magnitude (barring opamp saturation) that may be applied to it so as to produce the proper bit-stream output, leading to a discrepancy between the real circuit and the simple, linearized loop described above. As alluded to already, it is possible to reconcile these differences by properly assigning a non-unity value to the gain K .

To illustrate this point, consider the placement of an extra gain stage G before the quantizer as seen in Figure 2.7a). This would apparently alter the STF and NTF (Eqn 2.1a and Eqn 2.1b). In actuality, the operation of the circuit does not change because the signum function inherent to the comparator (Figure 2.7b) simply absorbs this difference. It is this disparity which makes it difficult to accurately linearize the loop [AFG⁺91].

In this thesis, the solution to this problem is to allow the loop to be linearly approximated by first characterizing the time-averaged value of the gain of the quantizer K . By "characterizing" here, it is meant that a determination of a value for the gain K is made either experimentally or through simulation for a given loop configuration, and at low input levels. It makes sense to linearize the DISDM in this manner because the loop's behavior is naturally invariant (as discussed below) since the time-averaged value of K , in most circumstances, remains fairly constant for any given modulator architecture. Exceptions to this will be discussed in greater detail later.

One way to illustrate the invariant behavior of the loop is through scaling. Consider changing the gain coefficients α_2 and α_3 by an equal amount in Figure 2.6b), say from 1 to 0.5 each. For the same signal to the input of both modulators, it is intuitive that within the modified modulator, the internal signals at the output of the second integrator are now scaled by one-half. However the quantizer still makes a decision on the polarity of that signal and thus the output bit-

Figure 2.6a DISDM is a linear biquad filter with a quantizer and 1-bit DAC

Figure 2.6b DISDM of Figure 2.1, modelled as a linear system with K indeterminate rather than unity

Figure 2.7a

Commonly modelled DISDM, but with an extra gain stage G . The STF and NTF is affected, a detriment to the simplified, linear model.

Figure 2.7b

In the real circuit, the STF and NTF is not affected because the comparator absorbs this gain

stream is identical to the unmodified, degenerate DISDM (all gain coefficients are equal to 1.0). A system-level simulation of the two different modulators will result in identical bit-stream outputs, which in return will yield the same STF and NTFs for both architectures, consistent with the depiction of Figure 2.7b) as expected.

Bringing in the idea of the characterized time-averaged gain K into the above discussion allows the loop to be properly described. Assume, in an example as Figure 2.7c), that the gain of the quantizer has been characterized through simulation for the degenerate DISDM and found to be $K = -4dB$. How this number is arrived at will be discussed shortly. Assume that the gain coefficients α_2 and α_1 from Figure 2.6b) are replaced with $\alpha_2/\Delta G$ and $\alpha_1/\Delta G$ respectively in Figure 2.7c) so that an imaginary ΔG must then be brought out in front of the quantizer by block diagram manipulation. To duplicate the assumed change of α_2 and α_1 in the previous paragraphs from 1 to 0.5, the value of ΔG would be equal to 2.0. This ΔG , which is not physically implemented, will then combine with the gain of the quantizer as shown in Figure 2.7d) so that the new gain of the quantizer is $K = (-4 + 6) = 2dB$.

Working out the STF and NTF for each modulator from Eqn 2.1a) and Eqn 2.1b) respectively now results in identical answers for the two modulators as expected, making the loop's behavior invariant. Of course this is an example where the gain of the quantizer combines easily with other gains within the loop. This exercise has shown how some scaling operations can produce the same output. More importantly, this effectively demonstrates that characterizing of the gain of the quantizer, as opposed to ignoring or oversimplifying it, is key to accurately taking a linearizing view of oversampled A/Ds. This is also necessary in order to help deal with stability with more precision as well as to understand and estimate distortion that might be found at the output of the DISDM.

2.4.2 Characterizing the Gain of the Quantizer

This section discusses an alternative narrowband method used to determine the gain of the quantizer and is the basis for all quantizer measurements in this thesis. This method came about from discussions with Kwasniewski [Kwa90] and its use later extended to explore quantizer characteristics to be discussed in upcoming chapters. Previously, the gain of the quantizer was deduced as a result of an investigation into modelling the quantizer through a DC measurement technique using average-responding DC voltmeters at the output of the sec-

Figure 2.7c DISDM with characteristic K and scaling operation performed on α_2 and α_3

Figure 2.7d The resulting DISDM, demonstrating invariant behavior with respect of Figure 2.7c) through linear analysis.

ond integrator and the output of the DISDM [AFG⁺91]. Ardalan and Paulos [AP87] have also mathematically described this gain. Assuming the modulator does not operate in the overload region and the input signal is low in frequency relative to the clock, then the PDF remains relatively constant. Examination shows, either through simulation or measurement, that at the output of the second integrator exists an amplified (or attenuated) component of the input signal plus superimposed noise. This of course, when quantized, yields the expected bit-stream output. For example, it is possible to create a scaled histogram (similar to a PDF) by plotting samples of the output of the second integrator. By using the input signal to trigger the plotting sequence (in the same manner in which an oscilloscope displays triggered waveforms), the long-term behavior of V_{o2} may be seen. A typical measured result of such a procedure is seen in Figure 2.8, where the output of the second integrator is sampled 25,000 times and plotted

Figure 2.8

Output of the second integrator. A running-normalized histogram from 25000 plotted samples of V_{o2} is created. The dashed lines denotes the envelope of the integrator's output and the frequency of this signal, associated with the dashed line, equals the frequency of the input signal.

for the fabricated DISDM to be discussed in the next chapter. In the frequency domain, this translates to a spectral component equal in frequency to that of the input signal, plus quantization noise. This component of the input signal must then experience gain in order to get the correct spectral amplitude in the output bit-stream. Thus, by virtue of the fact that a coherent, correlated signal representative of the input exists at the output of the second integrator, an alternate method which utilizes frequency domain techniques may be used to determine the gain of the quantizer.

Then, by applying a sinusoidal input to the modulator, the gain of the quantizer may be found by physically measuring the gain of the quantizer at the fundamental (input) frequency f_i through a spectral measurement (i.e. spectrum analyzer). Alternatively, it may be found experimentally through simulation. For instance, by performing a system-level simulation of the DISDM, an FFT may be carried out on the output bit-stream and the output of the second integrator. The difference in these two magnitudes (in decibels) at the fundamental frequency yields the characteristic, time-averaged gain of the quantizer.

$$K = V_o/V_{o2} = V_o \text{ (dB)} - V_{o2} \text{ (dB)} \quad \text{Eqn 2.9}$$

This has been the approach used in this thesis to determine K . For the degenerate DISDM designed and fabricated in this thesis, the time-domain behavior may be simulated and the spectral response estimated for both the output of the DISDM and the output of the second integrator as shown in Figure 2.9a) and Figure 2.9b) respectively. As an example, a 10 kHz, -15 dBV sinusoidal input (same as -12 dB with respect to the quantizer levels less 3dB from peak to RMS conversion) was applied to the modulator. This value of amplitude was chosen so as to ensure good operation away from the overload region. The resulting unwindowed FFT of Figure 2.9a) shows the fundamental at -15 dBV as expected and is consistent with what one would acquire from a spectrum analyzer. The spectral response of the output of the second integrator of Figure 2.9b) at the fundamental frequency is -11 dBV. This yields a gain of $K = -4\text{dB}$. This gain varies little from simulation run to simulation run, over a relatively wide range of amplitudes and throughout the baseband range of frequencies as will be discussed in greater detail next. It should be noted that single-tone inputs were used to determine the value of K here for simplicity. The value of K would not change if multiple tones had been used, unless integrator saturation affects it as will be discussed next.

Figure 2.9a Low-frequency, 64Kpoint FFT of the output bit-stream for a -15 dBV input to the modulator.

Figure 2.9b Same simulation as above, however the FFT is of the output of the second integrator. The spectral component at 10 kHz is -11 dBV, hence the gain of the quantizer is $K = -4\text{dB}$.

To explore the effects of integrator saturation (i.e. operation in the overload region), a 10 kHz sinusoidal input ranging from a full-scale input down to nearly a -40dB level was simulated, and 16Kpoint FFTs generated and plotted in Figure 2.10 along with the measured values from

Figure 2.10 Simulated and measured gain of the quantizer (at baseband frequencies) as a function of input level to the modulator. The frequency of the input signal is 10 kHz.

the fabricated DISDM. As shown, the simulated and measured gains agree quite well. The gain of the quantizer remains fairly constant, averaged around -4dB for both the simulated and measured gains, for input values up to approximately -8dB. The deviations from the average are due to changes that occur internally to the DISDM. When this happens, the PDF to the input of the quantizer changes causing the gain to differ slightly. An example of this may be artificially created by applying a significant DC offset to the input of the modulator. It was

observed that this in turn pushes the average value of V_{o2} towards a voltage supply rail which causes a loss in gain.

It is difficult to determine the gain for input levels less than that shown in Figure 2.10 as the noise level at the output of the second integrator is comparable to the signal level. It is possible to increase this range by performing larger FFTs in order to reduce the resolution bandwidth, however this is at the expense of computation time. However, it is known that K will tend to zero under idle channel conditions [Sne96].

It is noted that at high input levels (larger than -8 dB in this case), the gain of the quantizer decreases rapidly and is a consequence of operating in the overload region, since the input is comparable in amplitude to the span of the quantizer given the values of α used here. The reason for this is due to the PDF of V_{o2} having expanded to the rail voltages, generally decreasing the gain K . It is particularly interesting to note what effect this has on the NTF. A decrease in K causes a shift in the shape of the quantization noise spectrum, as may be seen in Figure 2.3 as an example from $K = 1$ to $K = 0.5$ say. This decrease in gain has been previously theorized [AP87], in which an increase in the baseband quantization noise was observed through simulation and analysis. The same result is easily shown by observing the theoretical NTF for low values of K , where K is now found from simple simulation or measurement. It will be shown that this gain element can have a profound effect on the signal and noise transfer functions and it will be shown that if the value of K is obtainable, the STF and NTF, for the most part, will be accurate and conform to measurement. As mentioned earlier, previous work on the topic of the gain of the quantizer [AP87] showed that it was possible to model the quantizer with separate gains for the signal and noise paths. Up to now in this work, both gains have been considered as just one, as is commonly done. This was sufficient to estimate the gain of the quantizer in the noise path for purposes here where the NTF is concerned and where better accuracy might be procured regarding upcoming analysis on the effects of finite gain in opamps. However, strictly speaking it is the gain of the quantizer in the signal path that is being found in this thesis as that is what is important.

More advanced characterization of the gain of the quantizer is necessary for a deeper understanding of the STF and will be covered in Chapter 4.

2.4.3 Check of DISDM Stability

Generally, the noise transfer function (NTF) for the most part is defined by the gain coefficients. Assuming that the inband attenuation of quantization noise is sufficient, stability of the system must be ascertained. A check of stability may prove to be unfavorable if the gain of the quantizer is assumed to be unity. Such a procedure would have to be followed up with a multitude of simulations to ensure stability [SY92], [Sch93]. In effect, the noise transfer function must be chosen such that the internal signals do not grow uncontrollably.

Stability of $\Sigma\Delta$ modulators in general may be treated in a variety of ways. This topic is not well understood and several attempts to resolve it have been made [AP87], [AS83] with no easy solution in sight. In the past, the question of stability has been resolved through basic safety guidelines [Can85] and simulation to verify the operation of the modulator for different signal classes and amplitudes. Having to simulate for stability as a function of input signal suggests that the topic of stability is a nonlinear problem best dealt with by appropriate nonlinear analysis techniques. The most robust analysis is often stochastically complicated [SY92], [HZ92], [Sch93] and incomplete while the easier, linearized loops may assume too much. It is known however, that the first-order modulator is unconditionally stable and very recently, the second-order modulator may now also (for all intents and purposes) be considered highly stable for all but certain types of "cooked up" inputs where it is possible (with the right sequence) to make the DISDM go unstable [Sne96], [Lop94].

The topic of stability in this thesis is touched upon, certainly not in the most robust manner possible as that would be too complex and is not the focus of this thesis. However, the technique employed here, along with a margin of error, should confidently yield a stable modulator while simultaneously allowing the use of linear techniques to understand the issues at play.

Many approaches have been attempted and are quite complex, with uncertain practicality. The stability analysis of Ardaian and Paulos [AP87] used a linear analysis approach that included the gain of the quantizer as a linear gain element. This original work presented an oversimplified DISDM with only two gain coefficients instead of four, and there were insufficient delays in the loop, compromising the validity of their analysis. A more robust attempt is made here at understanding stability of the DISDM used in this thesis and is presented below without such assumptions.

It must be remembered that an important characteristic of the quantizer's (time-averaged) gain is that it is nonlinear as it varies from sample period to sample period. Thus, variations of K must be accommodated in the analysis of stability. Furthermore, the gain K of the quantizer may wander out of the predicted range due to comparator overload, start-up transients or even certain inputs where the behavior of the feedback loop causes an unexpected value of K to appear, possibly resulting in instability. Although the approach used here is therefore somewhat limited, the following analysis nonetheless provides insight into the stability of the modulator and is intuitively appealing. For if the stability is found for all values of K , then the modulator must be stable [KKT90].

As already seen, the gain of the quantizer decreases from a nominal -4 dB to -8 dB when the input amplitude to the modulator is high. If the gain of the quantizer drops below some crucial threshold, it is possible for the DISDM to lose stability. Since the loop is stable over a limited range of loop gains, the DISDM is said to be conditionally stable. It is therefore necessary to check the stability under all possible conditions. Thus as a safety factor, -12 dB gain is assumed the lowest gain possible while -3 dB is the largest, as a reasonable bracket of gains that could be encountered.

Consider the DISDM of Figure 2.6a). Neglecting the quantization noise, the loop gain of the system may be found from the denominator of the STF or NTF of either Eqn 2.1a) or Eqn 2.1b) respectively. The denominator is

$$Den(z) = K\alpha_2\alpha_4z^{-1} + [1 - (1 - K\alpha_3)z^{-1}][1 - z^{-1}] \quad \text{Eqn 2.10}$$

Rearranging the denominator and setting it to 0, the loop gain, $L(z)$ may be identified as

$$1 + z^2 + z[K(\alpha_2\alpha_4 + \alpha_3) - 2] - K\alpha_3 = 1 + L(z) = 0 \quad \text{Eqn 2.11}$$

where the denominator had to first be multiplied through by z^2 . In order for stability in a sampled-data system to occur, the poles of the system must reside, by definition, inside the unit circle.

The resulting roots from the above characteristic equation are

$$z_1, z_2 = \frac{[K(\alpha_2\alpha_4 + \alpha_3) - 2] \pm \sqrt{[K(\alpha_2\alpha_4 + \alpha_3) - 2]^2 - 4(1 - K\alpha_3)}}{2} \quad \text{Eqn 2.12}$$

Armed with the gains determined from the previous section, it is possible to sweep the location of these poles with the safety factor in mind so as to ensure the poles reside within the unit circle. This is demonstrated in Figure 2.11a). As may be seen, all the pole locations are in fact within the unit circle.

Alternatively, a formalized approach for testing stability is the Nyquist plot. It shows the relative stability by indicating how close to instability the system may become. By simply plotting the magnitude of the loop gain $L(z)$ against the phase of the loop gain, a polar plot may be created as a function of increasing frequency. As a test, the system will be stable if the contour does not encircle the point $(-1,0)$.

Several Nyquist plots are created as seen in Figure 2.11b), where contours representing $K = -12$ dB through to $K = -3$ dB are plotted for the DISDM. There is no encirclement of the $(-1,0)$ point, thus denoting stability under stringent gain cases.

As the gain of the quantizer is not expected to decrease lower than -8 dB, stability should be ensured. This was verified by testing the DISDM in experiments, where no problems were found with regards to stability.

2.5 *Review of Nonlinearity*

This section serves as a general introduction to the manner in which a supposed linear signal propagates through a nonlinear system. From this, the foundation for further analysis with respect to other circuits and in particular, $\Sigma\Delta$ modulators are made.

When two signals of different frequency are mixed through a nonlinear non-frequency dependent element as shown in Figure 2.12, the results are intermodulation distortion components that occur at sum and difference frequencies, as described below. The intermodulation of signals is used as the example here as it contains the fundamental signal harmonic components as well.

The output of a nonlinear circuit element or system may be described by the power series expansion

Figure 2.11a Stability check on the unit circle. Poles reside inside denoting stability.

Figure 2.11b Nyquist plot for various gains of K . Stability is denoted by the absence of the encirclement of the $(-1, 0)$ point.

$$v_o = A_0 + A_1 v_i + A_2 v_i^2 + A_3 v_i^3 + \dots + A_n v_i^n \quad \text{Eqn 2.13}$$

where v_i is the input signal and, A_n are the coefficients that describe the circuit nonlinearity. Two signals of different frequency are applied to the input such that

$$v_i = V_1 \sin \omega_1 t + V_2 \sin \omega_2 t \quad \text{Eqn 2.14}$$

where $\omega_1 > \omega_2$. Substitution of Eqn 2.14 into Eqn 2.13, expanded up to the third power yields

$$\begin{aligned} v_o = & A_0 + A_1 V_1 \sin \omega_1 t + A_2 V_1^2 \sin^2 \omega_1 t + A_3 V_1^3 \sin^3 \omega_1 t + A_1 V_2 \sin \omega_2 t + A_2 V_2^2 \sin^2 \omega_2 t + A_3 V_2^3 \sin^3 \omega_2 t \\ & + 2A_2 V_1 V_2 \sin \omega_1 t \sin \omega_2 t + 3A_3 V_1^2 V_2 \sin^2 \omega_1 t \sin \omega_2 t + 3A_3 V_1 V_2^2 \sin \omega_1 t \sin^2 \omega_2 t \end{aligned} \quad \text{Eqn 2.15}$$

Through the use of the trigonometric identities

$$\sin^2(\tau) = \frac{1}{2} (1 + \cos(2\tau)) \quad \text{Eqn 2.16}$$

$$\sin^3(\tau) = \frac{3}{4} \sin(\tau) - \frac{1}{4} \sin(3\tau) \quad \text{Eqn 2.17}$$

$$\sin(a) \sin(b) = \frac{1}{2} [(\sin(a+b)) + \sin(a-b)] \quad \text{Eqn 2.18}$$

the above equation may be written (ignoring phase shifts)

Figure 2.12 Linear signals through a nonlinear element

$$\begin{aligned}
 v_o = & \left(A_0 + \frac{A_2 V_1^2}{2} + \frac{A_2 V_2^2}{2} \right) + \left[A_1 V_1 + \frac{3}{4} A_3 V_1^3 + \frac{3}{2} A_3 V_1 V_2^2 \right] \sin \omega_1 t - \frac{A_2}{2} V_1^2 \sin 2\omega_1 t - \frac{A_3}{4} V_1^3 \sin 3\omega_1 t \\
 & + \left[A_1 V_2 + \frac{3}{4} A_3 V_2^3 + \frac{3}{2} A_3 V_1^2 V_2 \right] \sin \omega_2 t - \frac{A_2}{2} V_2^2 \sin 2\omega_2 t - \frac{A_3}{4} V_2^3 \sin 3\omega_2 t \\
 & + A_2 V_1 V_2 \sin (\omega_1 + \omega_2) t + A_2 V_1 V_2 \sin (\omega_1 - \omega_2) t \\
 & - \frac{3}{4} A_3 V_1^2 V_2 \sin (2\omega_1 + \omega_2) t - \frac{3}{4} A_3 V_1^2 V_2 \sin (2\omega_1 - \omega_2) t \\
 & - \frac{3}{4} A_3 V_1 V_2^2 \sin (2\omega_2 + \omega_1) t - \frac{3}{4} A_3 V_1 V_2^2 \sin (2\omega_2 - \omega_1) t
 \end{aligned}$$

Eqn 2.19

The above equations show distortion at harmonic frequencies of the two fundamentals in addition to intermodulation distortion as expected.

Often, it is desirable to quote harmonic distortion with respect to the fundamental component. For example, the second and third *relative* harmonic is defined as

$$\begin{aligned}
 HD(2) &= \frac{\text{coefficient of } \sin(2\omega t)}{\text{coefficient of } \sin(\omega t)} \\
 HD(3) &= \frac{\text{coefficient of } \sin(3\omega t)}{\text{coefficient of } \sin(\omega t)}
 \end{aligned}$$

i.e. the second and third harmonic with respect to ω_1 is

$$HD^{\omega_1}(2) = \frac{A_2 V_1^2 / 2}{A_1 V_1} = \frac{A_2}{2A_1} V_1$$

Eqn 2.20

$$HD^{\omega_1}(3) = \frac{A_3 V_1^3 / 4}{A_1 V_1} = \frac{A_3 V_1^2}{4A_1}$$

Eqn 2.21

The fundamental component is

$$\left[A_1 V_1 + \frac{3}{4} A_3 V_1^3 + \frac{3}{2} A_3 V_1 V_2^2 \right] \sin(\omega_1 t) \equiv A_1 V_1 \sin \omega_1 t$$

Eqn 2.22

i.e., the higher order terms typically do not contribute significantly to the fundamental component in systems that are not grossly nonlinear. This will be true whenever $A_1 \gg A_2$ and $A_1 \gg A_3$ so the by-products of A_2 and A_3 which result in DC and fundamental terms (Eqn 2.19) may be neglected. This "almost lin-

ear" approximation is used throughout this thesis when considering relative harmonic distortion. The fundamental component is thus simplified to

$$A_1 V_1 \sin(\omega_1 t) \quad \text{Eqn 2.23}$$

which yields the simplified results of Eqn 2.20 and Eqn 2.21.

Unless otherwise stated, where there is no normalization with respect to the fundamental component, *absolute* harmonic distortion is assumed. Typically absolute intermodulation distortion is quoted in this thesis. For example, the second- and third-order absolute IMD products are

$$imd(\omega_1 - \omega_2) = A_2 V_1 V_2 \quad \text{Eqn 2.24}$$

$$imd(2\omega_2 - \omega_1) = \frac{3}{4} A_3 V_1 V_2^2 \quad \text{Eqn 2.25}$$

2.6 Conclusions

Through the use of system-level simulation, the fundamental operation of the DISDM has been demonstrated. By considering the issues brought forth such as signal-to-noise ratio, stability and integrator clipping, a judicious choice of coefficients may be made which often leads to a compromise between these effects. A now common architecture employed uses gain coefficients equal to 1/2 [BW88] with an emphasis on maximizing the dynamic range with integrator saturation in mind. However, this thesis focuses in part on exploring dynamic range limiting mechanisms that don't necessarily occur exclusively at high input levels. An initial choice as a way to accomplish this for comparison purposes was to allow all the coefficients to be set to a fixed value of unity. This maximizes the SNR at opamp outputs for low amplitudes, at what can be a considerable expense in loss of SNR from clipping, and is often referred to in this thesis as the degenerate case. This allows input-referred noise and distortion to go through to the output of the modulator with simple gain factors for simplicity. Simulations have shown the operation of the modulator to be stable for the degenerate case as expected [Can85]. An analysis of stability reinforces this choice. From these simulations, a foundation can be laid which allows the design of the DISDM to proceed.

A common linearized view of the $\Sigma\Delta$ modulator ignores the gain of the quantizer. As a result, the theoretical noise transfer function did not coincide with that indicated by simulation. By

taking into account a pragmatic, time-averaged value for the gain of the quantizer, this discrepancy can be eliminated, as will be better shown in Chapter 4. This has accuracy implications where stability and spectral leakage are concerned.

An introduction into the effects of circuit nonlinearity was presented through macromodel simulation by including nonlinear integrators in the loop. Primarily, it is the voltage dependence of opamps that dominates the integrator's nonlinear characteristics. As a consequence, harmonic distortion is generated and encoded into the bit-stream output of the DISDM. Later it will be shown that, as expected, harmonics related to the input frequency decrease with input amplitude until these harmonics become buried under the quantization noise. Through simulation, it was found that a certain input amplitude range exists such that it was possible for high-frequency spurs to intermodulate through circuit nonlinearity, causing distortion products to appear in the baseband. These intermodulation distortion products cause a further loss in the available dynamic range of the system and will be analyzed in detail. As a result, a general mathematical review of nonlinearity was included as background for future reference.

Design of the Double Integration Sigma- Delta Modulator

3.1 Introduction

This chapter is devoted to the detailed design of the sampled-data DISDM. Information found from the preceding simulations coupled with the theoretical foundation leads to a finalized design, which has been fabricated. The components that make up the DISDM are discussed with a particular emphasis on the opamp. The opamp is analyzed with appropriate thermal and $1/f$ noise calculations in addition to the broadband thermal noise arising from switched capacitors. Finally, the opamp is characterized through experimental measurement with emphasis on characterizing its linearity for use in the next chapter.

3.2 Design of the Sampled-Data DISDM

The following single-ended DISDM structure was fabricated on a pilot 0.8μ BiCMOS process at Northern Telecom. The process was not stabilized at the time of fabrication, which resulted in incomplete success of the circuit design. Process problems made measurements difficult;

nevertheless, sufficient experimentation was attainable to validate the technique and explore several dynamic range limitations.

Due to the greater transconductance offered by bipolar transistors, it is possible to design opamps to have open-loop gains in excess of 100 dB and UGBWs in excess of 250 MHz. NPN transistors are inherently less noisy than MOS transistors in many respects. Thus an opamp that utilizes a bipolar input differential pair would benefit greatly in terms of both $1/f$ and thermal noise. Faster opamps allow the switched-capacitors to be clocked at a greater rate. This in turn reduces the thermal switch noise. In switched-capacitor applications however, low input impedance at the base of the bipolar transistor can inhibit their use in the design of the input differential pair. The manner in which provision is made for this is discussed.

In order to explore dynamic range limiting mechanisms, these circuits have been designed to maximize dynamic range at the low end. This is achieved by designing the modulator with the degenerate gain coefficients discussed earlier (all gain coefficients are unity).

The higher opamp gains achievable in BiCMOS would have reduced the effects of nonlinearity and input-referred thermal noise from those seen here. However, as already stated, process problems made biasing difficult, leading to an opamp with less open-loop gain along with a degraded unity-gain bandwidth. This turns out to be an advantage from the point of view of measurement because it made the nonlinear effects easily measurable. It is expected that the conclusions will carry over to more optimal designs.

3.2.1 Detailed Design Procedure

The system level DISDM of Figure 1.1 when classically implemented is as shown in Figure 3.1a). The actual fabricated DISDM used in this thesis is shown in Figure 3.1b) and is slightly different in implementation, however it is for all intents and purposes functionally identical to that in Figure 3.1a). Figure 3.1c) contains a photomicrograph of the fabricated design. (Not shown in this Figure are the test structures that contained the comparator, opamp, switches and capacitors).

This sampled-data single-ended circuit designed is novel for two reasons. This structure as seen in Figure 3.1b), utilizes a single-ended reset-stabilized integrator, which serves to remove

Figure 3.1a Classical switched-capacitor implementation of the DISDM with the loop filter, quantizer and DAC

Figure 3.1b Fabricated circuit, functionally the same as Figure 3.1a)

a portion of the $1/f$ noise component from PMOS source followers that buffer the input differential pair. This circuit also attempts to employ the least number of switches possible to realize switched-capacitor resistor action in an oversampled A/D to minimize several adverse effects such as charge dumping and clock feedthroughs without resorting to differential circuitry.

The opamp was designed to maximize DC gain and bandwidth [Bla90]. The opamp is of the folded-cascode variety and contains a pole-splitting output stage necessary to achieve high DC gain. The schematic of this opamp may be seen in Figure 3.2. The opamps used incorporate high-impedance PMOS source-followers cascaded into a conventional bipolar differential input pair to achieve better transconductance while isolating the relatively low impedance of the bipolar transistor input pair. The folded-cascode opamp has no complementary PNP devices as they were not available. The parasitic pole associated with the PMOS current source in the cascode ultimately limited the UGBW of this opamp to approximately 200 MHz in the original design. Ultimately, the rate at which the DISDM operates will depend on the speed and slew rate of the opamp. A detailed design description now follows.

As discussed in the last chapter, the ability of the opamp to settle to a required number of bits of precision may be slightly relaxed while keeping the desired resolution of the modulator from decreasing. From the procedure laid out in the last chapter, the slew rate available from the opamp usually dictates the maximum clock rate. The slew rate in the opamp used in this structure is nominally 250 V/ μ S. Then, the maximum clock frequency may then be found as a starting point.

$$T = \frac{3.75\Delta}{SR} = \frac{3.75(2)}{250 \times 10^6}$$

$$= 30.0nS \quad \text{Eqn 3.1}$$

$$f_s = 33.3MHz \quad \text{Eqn 3.2}$$

To confirm proper operation, ideal simulations at clock rates equal to 20.48 MHz and 40.96 MHz (as bounds for settling times) were compared to simulations that included the effects of the opamp's slew rate for 250V/ μ S and half that for comparison. At 40.96 MHz, the degradation in SNR at large input amplitudes just becomes noticeable. Should this clock frequency be too fast for proper settling, in-band harmonics will appear as a symptom of the in-

Figure 3.1c Photomicrograph of the sampled-data DISDM, fabricated in $0.8\mu m$ BiCMOS technology

sufficient settling time. Note, as a reminder, that at very low input amplitudes, the effect of settling is mostly constant and hence no degradation in SNR will occur at such levels as discussed previously.

Having established the clock speed capability of the modulator, it is now worth focusing on the theoretical resolution capabilities of the DISDM. Two major noise mechanisms that limit the resolution are quantization noise and thermal noise. The theoretical resolution of the mod

Figure 3.2 MOS-Bipolar opamp used in the DISDM. (Parameter names and values found in simplified schematic to follow)

ulator as dictated by the spectral shaping of the quantization noise is found by considering the net in-band noise as stated already in Eqn 1.6, repeated below:

$$N_{mo}(f_o) = \frac{e_o \pi^2}{\sqrt{3}} \left(\frac{2f_o}{f_s} \right)^2 V_{RMS} \quad \text{Eqn 3.3}$$

where $e_o = \sigma / (\sqrt{12})$ and $\sigma = 2V$. Thus, for any given clock frequency, the baseband width f_o must be decreased for additional resolution, unless the resolution is limited by thermal noise. Two sources of thermal noise that must be considered are switched-capacitor resistor (SCR) broadband thermal noise and input-referred thermal noise of the opamp. These are considered separately. As an estimate, the SCR broadband thermal noise from C_{R1} and C_{R4} in the DISDM may be approximated as contributing to the output as uncorrelated sources of noise. The noise equivalent model of the DISDM is shown in Figure 3.3), where these capacitors are replaced

Figure 3.3 Continuous-time equivalent of DISDM as regards SCR noise generation

by switched-capacitor equivalents R_{CR1} and R_{CR4} . The other SCR's contribution to noise is insignificant as it is suppressed by the high loop gain offered by the circuit. The PSD arising at the output from R_{CR1} is

$$N_{no}^{R_{CR1}} = 4KTR_{CR1} \left(\frac{R_{CR4}}{R_{CR1}} \right) \quad \frac{V}{Hz} \quad \text{Eqn 3.4}$$

The contribution of PSD to the output from R_{CR4} is

$$S_{no}^{R_{CR4}} = 4KT R_{CR4} \frac{V^2}{Hz} \quad \text{Eqn 3.5}$$

As these sources are considered to be uncorrelated, the PSD at the output of the modulator is

$$S_{no} = 4KT R_{CR4} \left(1 + \frac{R_{CR4}}{R_{CR1}} \right) \frac{V^2}{Hz} \quad \text{Eqn 3.6}$$

where $R_{CR4} = \frac{1}{f_s C_{R4}}$ and $R_{CR1} = \frac{1}{f_s C_{R1}}$.

Using the clock frequency as determined earlier and knowing that $R_{CR1} = R_{CR4}$, then the equivalent SC thermal broadband noise at the output is

$$S_{no} = \frac{(1.66 \times 10^{-20}) (2)}{(33.3 \times 10^6) C_{R4}} \frac{V^2}{Hz} \quad \text{Eqn 3.7}$$

The RMS net thermal noise voltage is then

$$V_{AOTM} = \sqrt{\frac{(1.66 \times 10^{-20}) (2)}{(33.3 \times 10^6) C_{R4}} \int f_o} = V_{RMS} \quad \text{Eqn 3.8}$$

for a baseband width of f_o . The net (integrated) quantization noise from Eqn 3.3 is, for comparison,

$$V_{QN} = \frac{\sqrt{12} \pi^2}{\sqrt{5}} \left(\frac{2}{33.3 \times 10^6} \right)^{1/2} f_o^{1/2} = V_{RMS} \quad \text{Eqn 3.9}$$

Up to now, it has been seen that these two sources of noise both depend on f_s . In the interest of making the most efficient use of the bandwidth, (i.e. where the resolution of the coder depends on the quantization noise as opposed to being limited by the thermal noise from the SCRs) the SCR thermal noise may be equated to the theoretical quantization noise. Note that the input-referred thermal and 1/f noise of the opamp will be treated separately later.

Equating Eqn 3.8 and Eqn 3.9 yields in general form

$$\sqrt{\frac{4KT}{f_s C_{R4}} \left(1 + \frac{C_{R1}}{C_{R4}} \right) \int f_o} = \frac{c_o \pi^2}{\sqrt{5}} \left(\frac{2f_o}{f_s} \right)^{1/2} \quad \text{Eqn 3.10}$$

Squaring both sides and rearranging yields

$$\left[\frac{C_p^2 \pi^4}{5} \left(\frac{2}{f_k} \right)^2 \right] f_o^2 - \left[\frac{4KT}{f_k C_{R4}} \left(1 + \frac{C_{R4}}{C_{R4}} \right) \right] f_o = 0 \quad \text{Eqn 3.11}$$

Solving for f_o , the crossover point at which the resolution of the modulator equals the SC thermal broadband noise is then

$$f_o = \sqrt{\frac{4KT}{f_k C_{R4}} \left(1 + \frac{C_{R4}}{C_{R4}} \right)} \quad \text{Eqn 3.12}$$

Putting in values, this becomes

$$f_o = \sqrt{\frac{(1.66 \times 10^{-17}) (1 + 1)}{(33.3 \times 10^{-6}) C_{R4}}} \quad \text{Eqn 3.13}$$

The only variable that is left is C_{R4} .

To ensure stability of the opamp under closed-loop conditions, the SC values were confined to a lower limit of 0.5 pF. This constraint effectively sets the thermal noise. At lower bandwidths where high resolution is desired, the net thermal noise dominates the net quantization noise. The crossover point at which the quantization noise dominates thermal SC noise at higher bandwidths is found from Eqn 3.12 and is plotted in Figure 3.4) for $C_{R4} = 0.5$ pF. Solving Eqn 3.13, f_o is found to be 120 kHz. At this crossover frequency, the net noise which ideally determines the resolution of the modulator may be seen from Figure 3.4) or calculated simply by

$$V_n = \sqrt{\frac{4KT(2)f_o}{f_k C_{R4}}} \quad \text{Eqn 3.14}$$

$$= \sqrt{\frac{(1.66 \times 10^{-17}) (2) (120 \times 10^3)}{(33.3 \times 10^{-6}) (0.5 \times 10^{-12})}}$$

$$= 15.4 \mu\text{V}_{RMS}$$

Figure 3.4 SC thermal noise is dominant at low frequencies. Note the crossover frequency is 120 kHz.

This translates to 16 bits of resolution. In general, for N bits, rearranging Eqn 3.14 yields the required bandwidth f_o from thermal noise alone

$$f_o = \frac{\left(\frac{1}{2^N}\right)^2}{\frac{4KT}{f_s C_{R4}} \left(1 + \frac{C_{R1}}{C_{R4}}\right)} \quad \text{Eqn 3.15}$$

It must be remembered that the quantization noise model assumes white noise. There will, in fact, be an increase in the net quantization noise due to correlated spectra. The theoretical dynamic range in dB is

$$DR = 20 \log \left[\frac{e_o \pi^2}{\sqrt{5}} \left(\frac{2 [120 \times 10^3]}{33.3 \times 10^6} \right)^2 \right] + 20 \log (V_n) = 96.3 \text{ dB} \quad \text{Eqn 3.16}$$

Simulations shows 90 to 93 dB. Hence a 4 dB to 7 dB difference due to correlated quantization noise spectra should also be taken into account. In reality, the dynamic range is further limited by bit-stream saturation effects at high input amplitudes as well as circuit nonlinearity and the effects of finite gain from opamps.

3.2.2 Input-Referred Thermal Opamp Noise

The other source of noise that contributes to the output of the modulator comes from the opamp. This section reviews and summarizes the extensive treatment given in Appendix B to familiarize the reader with how noise may be calculated in BiCMOS amplifiers and the methodology used to input-refer it. The appendix details the noise seen from various sources including thermal noise, collector-current shot noise, base-current shot noise and $1/f$ noise in both MOS and bipolar transistors. In Chapter 5, noise is calculated in the (OTA) amplifier with less explanation since there will be an assumed familiarity with noise at that point.

A simplified schematic of the opamp may be shown in Figure 3.5), without the pole splitting and load capacitors. In order to proceed with a noise analysis, the nominal DC gains from stage to stage are required. Both simplified and detailed analysis is found in Appendix B. In summary, these gains are $V_A/V_{in} = 1$, $V_B/V_A = 1.75$, $V_C/V_B = 1.37$, $V_D/V_C = 1$, $V_o/V_D = 808$. Consideration must also be made to include the current mirror at the bottom of the cascodes. Not only does it provide differential-to-single ended conversion but also adds 6 dB to the overall DC (open-loop) gain of the opamp.

The strategy used here to calculate some of the input-referred opamp noise is to find many of the noise contributions seen at output node V_o seen in Figure 3.5). This quantity will then be divided by the gain from V_{in} to V_o .

The essential formulas used to help design and analyze noise in the opamp are shown below [GM84]. The input-referred PSD from thermal noise in a BJT is

$$\frac{v_n^2}{\Delta f} = 4KT r_{bb} \left[\frac{V_o^2}{H_o^2} \right] \quad \text{Eqn 3.17}$$

where r_{bb} is the intrinsic base resistance.

All BJTs have a collector-current shot noise component whose noise spectral density is

$$\frac{i_{c,n}^2}{\Delta f} = 2qI_c \left[\frac{V_o^2}{H_o^2} \right] \quad \text{Eqn 3.18}$$

Similarly, they also have a base-current shot noise component

Figure 3.5 Simplified schematic of the MOS-bipolar differential input BiCMOS opamp (without capacitors).

$$\frac{i_{bs}^2}{\Delta f} = 2qI_B \left[\frac{A^2}{Hz} \right] \quad \text{Eqn 3.19}$$

A convenient formula that is often used in BJT-based differential input pairs which combines collector-current shot and thermal noise is [Erd81]

$$\frac{v_n^2}{\Delta f} = 4KT \left(\frac{1}{2g_m} + r_{bb} + R_{LL} \right) 2 \left[\frac{V^2}{Hz} \right] \quad \text{Eqn 3.20}$$

where R_{LL} is the emitter degeneration resistance.

The gate-referred thermal noise from MOS transistors may be found from

$$\frac{v_n^2}{\Delta f} = 4KT \left(\frac{2}{3g_m} \right) \left[\frac{V^2}{Hz} \right] \quad \text{Eqn 3.21}$$

The significant contributions to the overall noise of the opamp may be input referred according to the individual gains within the opamp as stated earlier. All the individual input-referred contributions calculated in Appendix B are displayed in tabular form in Table 3.1 below.

VSD_i	$nV/\sqrt{Hz}$	Association and Noise Type
VSD_1	4.0	Inner differential pair (Q2+Q3+R _{ee}), Thermal and $i_{n1}^2/\Delta f$
VSD_2	2.66	Inner differential pair (Q2+Q3+R _{ee}), $i_{n2}^2/\Delta f$
VSD_3	1.97	Cascode current source (M1+M2), Thermal
VSD_4	1.34	Cascode common-gate (M3+M4), Thermal
VSD_5	10.9	Active cascode load (Q14-17), Thermal, $i_{n3}^2/\Delta f$ and $i_{n4}^2/\Delta f$
VSD_6	5.93	Source-follower (M7+M8), Thermal
VSD_7	4.98	Source-follower (M5+M9), Thermal

Table 3.1: Tabulated Voltage Spectral Densities.

The total input-referred thermal opamp noise is then found by summing all spectral densities such that

$$VSD_{th} = \sqrt{\sum_i VSD_i^2} \quad \text{Eqn 3.22}$$

Tabulating all the voltage spectral densities yields the final, input-referred voltage spectral density

$$VSD_{th} = 14.4 \frac{nV}{\sqrt{Hz}} \quad \text{Eqn 3.23}$$

The manner in which this noise goes through to the output of the DISDM will be covered shortly followed with discussion.

3.2.3 Input-Referred Opamp 1/f Noise

Aside from thermal and shot noise, 1/f noise plays a role in degrading dynamic range in BiCMOS analog circuits. The 1/f noise contribution from bipolar transistors is generally much less than MOS transistor contributions. The 1/f noise PSD for bipolar transistors is

$$S_{n(1/f)}(f) = \frac{KI_B^A}{f} \left[\frac{A^2}{Hz} \right] \quad \text{Eqn 3.24}$$

where I_B is the quiescent base current of the bipolar transistor, K and AF are parameters which depend on the process. Usually, $1/f$ noise is quoted at 1 kHz. This noise spectral density (in A^2/Hz) flows into the same resistance that base-current shot noise does, allowing the determination of noise in terms of voltage spectral density. Thus it should be noted that the resulting $1/f$ noise depends greatly upon the source resistance and the intrinsic base resistance, which should be kept in check to keep this source of noise low. This contrasts the $1/f$ noise that is generated from MOS devices, whose magnitude depends only on the width and length of the device. Typically, $1/f$ noise from MOS devices dominates over bipolar $1/f$ noise and that was the case here. For a MOS transistor, the input-referred (i.e. gate-referred) noise is

$$S_{n(1/f)}(f) = \frac{KF}{C_{ox}WLf^A} \left[\frac{V^2}{Hz} \right] \quad \text{Eqn 3.25}$$

where KF and AF are also process parameters. From Appendix B, it was found that two main sources of $1/f$ noise came from the source follower surrounding the bipolar differential input pair (the primary source) and to a lesser extent, from the cascodes.

From Appendix B, the input-referred $1/f$ noise associated with the source follower that encompasses the bipolar differential input pair is calculated out to

$$VSD_{(1/f) \text{ follower}}(1\text{kHz}) = 85.3 \frac{nV}{\sqrt{Hz}} \quad \text{Eqn 3.26}$$

The $1/f$ noise contribution from the cascode devices at 1 kHz when input referred is

$$VSD_{(1/f) \text{ cascodes}}(1\text{kHz}) = 28.3 \frac{nV}{\sqrt{Hz}} \quad \text{Eqn 3.27}$$

Had the gain of the differential pairs in folded-cascode opamps been much lower, a potentially detrimental increase in the amount of noise that may have been referred back to the input may have taken place. This is true not only where $1/f$ noise is concerned, but also where thermal and shot noise may become significant.

Hence, the total $1/f$ noise at 1 kHz (input-referred) is

$$VSD_{(1\text{ kHz})total} = \sqrt{[VSD_{(1\text{ kHz})follower}]^2 + [VSD_{(1\text{ kHz})cascode}]^2}$$

$$= 89.9 \frac{nV}{\sqrt{Hz}}$$

Eqn 3.28

A simulation of this opamp (in closed-loop) of Figure 3.6) reveals a total input-referred thermal noise of $14.8 \text{ nV}/\sqrt{Hz}$ which compares quite well with the theoretical, expected result of $14.4 \text{ nV}/\sqrt{Hz}$. Also the simulation yields a total input-referred $1/f$ noise of $90 \text{ nV}/\sqrt{Hz}$ at 1 kHz which compares extremely well with the predicted theoretical $1/f$ noise (at 1 kHz) of $89.9 \text{ nV}/\sqrt{Hz}$, calculated above. It should be noted that with this reset-stabilized integrator, this $1/f$ noise magnitude will be reduced somewhat. In experiment, the opamp may be put into a voltage follower configuration so that the input-referred noise of the opamp may be seen at the output. Furthermore, this configuration has good drive capability. The input referred noise was found experimentally to be $183 \text{ nV}/\sqrt{Hz}$ at 1 kHz and the thermal noise was found to be $42 \text{ nV}/\sqrt{Hz}$ as found in Figure 3.7a) and Figure 3.7b). The primary reason for the discrepancy

Figure 3.6

Noise simulation of the MOS-Bipolar differential input opamp. Voltage follower configuration is used to observe the input-referred noise at the output

Figure 3.7a Measured 1/f noise of the opamp.

Figure 3.7b Measured thermal noise of the opamp

between theory and measurement relates to the noise models used for calculation and simulation. They were far less than what was seen from fabricated devices. Another reason for this sizable increase as compared to theory is that the gain of the fabricated opamp is far less than expected. Consequently, it is expected that the noise beyond the differential input pair is not suppressed as well. This will be discussed in greater detail later.

3.2.4 Output-Referred DISDM Noise

Finally, the manner in which input-referred noise propagates through to the output of the modulator may be seen by considering Figure 3.3. For example, considering thermal, collector current and base-current shot noise only, the input-referred, total PSD found goes through to the output at low-frequency as

$$S_{no} = S_n \left(1 + \frac{R_{CR4}}{R_{CR1}} \right)^2 \quad \text{Eqn 3.29}$$

where R_{CR1} and R_{CR4} are the switched-capacitor equivalent resistors of the DISDM. The total voltage spectral density as seen at the output from theory is then just

$$\begin{aligned} VSD_o &= \sqrt{S_n \left(1 + \frac{1}{1} \right)^2} = \sqrt{(14.8 \frac{nV}{\sqrt{Hz}})^2 (2)} \\ &= 29.6 \frac{nV}{\sqrt{Hz}} \end{aligned} \quad \text{Eqn 3.30}$$

Over a 120 kHz bandwidth, the net integrated noise from the above is $10.2 \mu V$ which is under the net noise from quantization and SC thermal noise sources (Figure 3.4) leaving broadband SC thermal noise to dominate over the opamp thermal noise.

3.2.5 Summary and Conclusions from Noise Calculations

Emitter degeneration is used intentionally to reduce the bandwidth of the opamp for good phase margin in this particular case. The introduction of emitter degeneration also increases linearity and input impedance. It however has the unfortunate side-effect of increasing the

mal noise. Also significant is the intrinsic base resistance, r_{bb} . At these relatively high quiescent current levels, the thermal noise component associated with collector-current shot noise is small compared to the thermal noise from r_{bb} . The contribution of thermal noise from the differential pair as well as the PMOS source follower's driver and active load are not as dominant as one might think. There is a significant contribution from the cascode transistors as well as from the current mirror load. The reason for this is attributable to the low gain of the differential pair as a consequence of emitter degeneration. Also, with hindsight, the current mirror load could have been degenerated for better noise performance when input-referred.

This opamp uses a PMOS source follower cascaded into the bipolar differential pair so as to isolate the low impedance of the bipolar transistors from the switched-capacitors. The disadvantage of the PMOS source followers is the considerable $1/f$ noise. However, there are no base-current shot noise manifestations at the input to be considered. For example, the use of bipolar Darlington's or an emitter follower in place of the MOS source follower needed for high input impedance would pose serious concerns as regards the effects of base-current shot noise. This is because now the high input impedance of the opamp, which is in parallel with the high-impedance of the switched-capacitors, makes available a high effective resistance into which this base-current shot noise flows. Should this type of all-bipolar input stage be considered, this would give extra incentive to increase the clock frequency so as to reduce the value of the SCR's R_{CR1} and R_{CR4} (with reference to Figure 3.3). This would also mean a reduction in the broadband SCR thermal noise while at the same time mitigating base-current shot noise.

As mentioned earlier, part of the reason the fabricated opamp demonstrated higher noise related to differences between the noise models used in simulation and their larger values in fabricated devices. However, part of the reason also relates to the highly degraded DC gain of the opamp seen in measurement. It is expected that due to a reduction in gain of the cascode gain stages within the opamp, sources of noise such as those associated with the current mirror load do not get attenuated enough and thus start to dominate when input referred. Although this increase in noise results in a decrease in the available resolution of the coder somewhat, it will be seen that thermal noise will not rise above the in-band quantization noise in reality. This is due to other effects related to the operation of the DISDM, notably the effects of finite gain in the opamps causing spectral leakage. In concluding, the increased opamp input-referred noise

seen in measurement will not limit the ability to explore other dynamic range limitations of interest.

3.2.6 Switches, Capacitors and the Comparator

In contrast to the fairly extensive treatment given to the opamp, this section briefly discusses the switches, capacitors and the comparator. Since reference voltages come from off-chip, no DAC is required. Not much design forethought is required for these elements since it is generally known that imperfections in these elements do not significantly affect the operation or performance of the DISDM [BW88].

The design of the switched-capacitors was already covered earlier. In essence, by attempting to maximize opamp bandwidth (with a particular emphasis on maximizing slew rate), the compensation capacitor was kept to a minimum. So as to minimize the capacitive loading on the opamp for stability concerns, the switched capacitors were also kept small. The price paid for this is more SCR broadband thermal noise. However, this is offset by the use of a faster clock frequency.

It is thus possible to design the DISDM for greater speed by using high slew rate, large bandwidth opamps in tandem with a high clock frequency. However, as the clock rate increases, switches must be made large enough to ensure good settling of the signals that pass through the switched capacitors. Judicious design of the switches incorporated complementary n- and p-channel transistors, both having a W/L ratio of 12/0.8. The large size of the transistors, according to simulation, allows settling to better than 16 bits of accuracy for the 30 MHz clock expected to be used. By making the transistors the same size, clock feedthrough and charge dumping (stored charges under the channel) cancel to a first order. The remaining feedthrough component that does not cancel out produces an offset voltage which manifests itself to the output of the integrator. It has been reported that these offset errors, assuming they are not overly large, do not significantly upset the SNR of the modulator [BPS⁺90]. Thus it is important not to oversize the switches to keep the above statement valid. Furthermore, the sizes of the transistors should be kept to a minimum to avoid charge dump induced harmonic distortion. Of particular interest is the switch connected to the input. Since the amount of charge that is dumped is slightly signal dependent, [Lon88] [BPS⁺90] this particular switch may gen

erate distortion from the uncanceled residual charge. By assuring that this charge exits to low impedance nodes, this source of nonlinearity may be kept to a minimum.

The DISDM designed and fabricated in this thesis is configured such that when any switch around the first integrator turns off (this is where harmonic distortion is important), a low impedance node is present on one end of the switch. This routes the residual charge from dumping away from the virtual ground to avoid integration.

A further concern is that the switch's on-resistance is voltage dependent and thus may be a source of nonlinearity. With the size switch used, transistor-level simulations revealed harmonics in excess of 100 dB below the fundamental at full-scale inputs. Thus, this source of nonlinearity may be neglected.

The capacitors used are of the polysilicon-polysilicon variety for good inherent linearity. This comes at the expense of matching performance indicative of more conventional polysilicon-substrate capacitors. However, capacitor mismatch translates to gain variations in the coefficients. The coefficients α_1 and α_2 set the DC gain of the modulator while the other coefficients are less important due to the quantizer's ability to absorb and modify the gain of the quantizer as will be discussed at great length later. Considering that the relative mismatch of capacitors is typically far less than 1%, this effect is insignificant on the performance of the DISDM's SNR since the change in the noise shaped spectrum and signal transfer function are insignificant.

The comparator also does not require stringent design specifications. The main objective here is that the speed of the comparator is adequate given the clock rate of the DISDM. Input-referred noise and offset are suppressed by the high loop gain of the circuit and thus are of no consequence. Even the resolution of the comparator has been reported not to be particularly stringent [BW88].

The comparator used in this thesis was developed from an existing high-speed flip-flop cell [Lon90]. By master and slaving two D flip-flops, adding ECL-to-CMOS conversion and other level conversions, a latching comparator was designed as shown in Figure 3.8), without the ECL-to-CMOS conversion stage. It is a classical high speed architecture that uses two phases based on the system clock. When the leading edge of the clock is delivered, the output of the comparator latches the decision at the input.

Figure 3.8 Sample-Time Comparator

This comparator may be thought of as having four stages. The first and third stages are differential amplifiers while the second and fourth stages are latches. During the tracking phase, when the clock is low, a differential input voltage is developed in the first stage (Figure 3.8). Simultaneously, the slaved D flip-flop is holding the previous state. When the leading edge of the clock comes, the first latch (second stage) amplifies through positive feedback the output of the differential input pair of stage one through current steering from stage one to stage two. At this point, the third stage is amplifying the latched output right through to the output of the comparator. Thus, when the leading edge of the clock comes, the output is a valid binary comparison representative of the input. When the clock goes low again, the fourth stage amplifies this same output, holding it until the next leading edge comes along, while at the same time developing a new differential input voltage at the input to the comparator.

These simple cells, for the most part, worked quite well when the individual components were tested. Although there were process problems that limited the yield, none of these cells gave particular difficulties. The comparator, without ECL-to CMOS conversion, was tested at speeds in excess of 450 MHz and was able to resolve down to 2 mV. It had output transition times of 0.8 nS which is a little slower than the 0.6 nS time simulated.

3.2.7 Opamp Testing and Characterization

This section deals primarily with the linearity characterization of the opamp as this information will be necessary to analyze the linearity of the DISDM in the next chapter. Furthermore, simple measurements of the DC gain and the unity-gain bandwidth are made.

Disappointingly, there was a very limited run of this test chip which severely limited the number of good working devices. In fact of 12 devices of the oversampled A/D that were available, only three DISDMs worked. Of these working devices, the biases were out of specification owing to gate oxide problems in the large cascode MOS transistors. The opamps were nevertheless coaxed to work with a fair degree of loss in DC gain and unity-gain bandwidth. The loss of DC gain simply means that nonlinear effects will proliferate more strongly, however, the use of a lower clock frequency must be accepted. Although the original plan was to use a high resolution coder to measure harmonics that exist with low magnitudes, the ex-

perimental validation of this study into nonlinearity may still be accomplished with a lower resolution coder with larger harmonics.

Briefly, the opamp was characterized as having a unity-gain bandwidth of only 7 MHz to 9 MHz at most with a DC gain just under 40 dB. As discussed earlier, as long as the slew rate is high, the time constant of the integrator can start to approach the clock period. This means that the integrator time constant $\tau = t_{\text{CLK}}/BW$, from the last chapter, yields a maximum clock frequency of 3.5 MHz to 4.5 MHz. When the DISDM is run at these speeds, harmonics appeared denoting insufficient settling. By reducing the clock to 2.5 MHz, the harmonics from this source of distortion disappeared. This makes sense because the opamp used is a two-stage opamp and the integrator time constant τ above was just an estimate. As a safety factor, the DISDM was run primarily at 2 MHz to ensure good settling.

With the opamps working, albeit compromised from the original specifications, characterization of the linearity of the opamp may proceed. With the opamp in open loop, a DC sweep may be performed about the high-gain region of the opamp. The results are plotted in Figure 3.9a). By performing a regression fit of the data, a polynomial equation may be found which describes the output voltage as a function of the difference-mode voltage of the opamp, as may be seen in Figure 3.9b). The regression fit is performed over a limited signal swing so as to achieve a good fit. By including a larger output swing, the polynomial regression does not fit well with the measured data. Furthermore, by increasing the order of the fit, oscillatory behavior of the fourth- and fifth-order terms cause the fit to be worse, degrading the DC gain term.

3.3 Summary and Conclusions

This chapter was devoted to the design of the sampled-data DISDM. With the knowledge gained from simulations in the last chapter, final specifications and the design of the DISDM were completed. It was the intention to use an opamp that demonstrated gain and bandwidth whose limits were related to the ability of the BiCMOS process. In this way, it would have been possible to explore the dynamic range limitations with a lower quantization and thermal noise floor due to the greater possible clock speed. Unfortunately, process problems limited the open-loop gain and the unity-gain bandwidth of the opamp. Although the original specification was not met, it was still possible to operate the DISDM at lower clock frequencies and

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PM-1 3½" x 4" PHOTOGRAPHIC MICROCOPY TARGET
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Figure 3.9a Measured open-loop gain characteristics of the opamp

Figure 3.9b Regression fit of the above measurement yields $V_{out} = 79.1V_d + 9.86e^{-3}V_d + 2.41e^{-6}V_d$

achieve a principle mandate of this thesis, namely the study into the effects of circuit nonlinearity in oversampled A/Ds which is discussed in following chapters.

A further limitation in dynamic range stems from thermal noise from the switched capacitors as well as from the opamp. Noise from the opamp is treated extensively. This is essential to ensure noise control as well as to provide the reader with an analysis that covers the many noise mechanisms present in bipolar transistors in addition to MOS noise manifestations more commonly known to ASIC designers. Simulations resulted in noise spectral densities that agreed well with the theoretical levels. In switched-capacitor circuits, the low impedance of the bipolar transistor must be isolated from the capacitors to conserve charge. As already discussed, this was accomplished through the use of PMOS source followers cascaded into the differential input pair and is a feature of the opamp used. This presents a great deal of $1/f$ noise however. Reset-stabilization was used in the integrator and removes a portion of this noise. Alternative structures might utilize high-impedance bipolar stages. As was discussed, caution must be exercised to keep the base-current shot noise low in such a case.

Keeping to the opamp at hand, it was found that the predominant sources of noise come from the current mirror load, source follower and differential input pair. The noise from the current mirror load is high, when input-referred, due to the low gain of the differential pair. This is a consequence of emitter degeneration used to keep the opamp stable. The thermal noise in the differential input pair is mostly due to emitter degeneration and the intrinsic base resistance. If it were desirable to minimize this source further, larger transistors could have been used to lower the value of r_{bb} . However, this is done at the expense of increased parasitic presence.

The measured $1/f$ and thermal input-referred noise was higher than expected for reasons already discussed. As the noise from the current mirror is quite significant, any loss of gain from the cascode gain stages is detrimental as this noise source, when input referred, becomes quite large. Although the exact places where gain is lost within the opamp are difficult to determine, it is known that the primary problem relates to dysfunctional PMOS transistors, a problem that was inherent to this fabrication run. The output-referred noise of the DISDM was covered as a fundamental calculation necessary to ensure good SNR and is an integral part of the design process. The process difficulties with the experimental circuits covered in this chapter will not hamper efforts to measure and explore other dynamic range limitations to be discussed at

length in the next chapter. A dominating effect at low frequencies is zeros introduced in the quantization noise transfer function and is covered extensively in the next chapter.

Finally, a brief discussion on the design of the switches, capacitors and comparator was given. The opamp was characterized through measurement, particularly for the linearity of the device as needed for the next chapter on the topic of opamp nonlinearity. Good theoretical prediction of distortion is sensitive to the coefficients gathered here that describe the open loop opamp linearity. Thus good measurement accuracy was crucial.

The next chapter concentrates on the theoretical aspects of the DISDM by delving into a more detailed analysis through modelling, particularly as regards circuit nonlinearity. The effects of circuit nonlinearity may, in high resolution oversampled A/Ds, limit the achievable dynamic range in these modulators. Furthermore, high-bandwidth circuits that trade gain for bandwidth typically exhibit more distortion. Since there is a lack of understanding of how nonlinearity proliferates in DISDMs this study is a key topic in this thesis. It will be shown that with good design practice, it is possible to avoid the degradation of the SNR due to the effects of nonlinearity.

Analysis of Double Integration Sigma- Delta Modulators Including Nonlinearity

4.1 Introduction

Double-integration sigma-delta ($\Sigma\Delta$) modulators have enjoyed a reputation as being attractive for VLSI implementation due to their tolerance to circuit nonidealities. However, as process technology and the available speeds improve, and as the demands for resolution increase, circuit nonlinearities can impinge upon the performance of the modulator. This chapter analyzes the manner in which circuit nonlinearities are manifested in the sampled-data DISDM, a key topic in this thesis.

As seen from simulation in Chapter 2, circuit nonlinearity can be responsible for the generation of in-band tones from the intermodulation of high-frequency spectra. However, theoretical analysis is required in order to explore the modulator in greater depth so as to provide behavioral explanations and give quantitative understanding.

This chapter will cover an analysis of the DISDM, looking again at the signal transfer function (STF) with refinement this time. It is shown that, by further characterizing and modelling the

gain of the quantizer, the signal transfer function for the DISDM will be sufficiently accurate enough to allow characterizing of nonlinearity mechanisms.

Signal interactions at the input through circuit nonlinearity might be thought of intuitively to be approachable from the linearized model for the $\Sigma\Delta$ modulator. Armed with a well modelled and understood loop, and after determining the distortion found from z domain analysis of the DISDM, a continuous-time biquad is to be used for linearity analysis as an equivalent to the sampled-data DISDM. This is because the signal transfer function will be shown to resemble something that is closer to a continuous-time biquad rather than a sampled data transfer function, with regards to the higher-frequency portion of the spectrum. In this way, the complexities associated with having to mathematically describe this disparity in the z domain are alleviated. The distortion seen at the output of the DISDM can then be determined with relative ease by ascertaining the closed-loop linearity coefficients as a function of frequency.

As already shown through an initial simulation, circuit nonlinearity can manifest itself through the intermodulation of high-frequency spurs. The way in which these high frequency spurs are first formed is first qualitatively discussed. An estimate of the magnitude of the intermodulation distortion (IMD) products from these high-frequency spurs can be made, which will help validate this mechanism and the approach taken to ascertain them.

Finite gain in amplifiers is known to cause an increase in the quantization noise at low frequencies. The specifics of this mechanism are already detailed for the single order $\Sigma\Delta$ modulator in the literature. The analysis is logically extended for the DISDM here. Both modulators are analyzed for the effects of finite gain in opamps, which now includes the gain of the quantizer, allowing the augmentation of quantization noise in the baseband to be predicted with more accuracy than what is available in the literature.

4.2 Double Integration Sigma-Delta Modulator Analysis

4.2.1 Introduction

To review, an early and still common approach to modeling $\Sigma\Delta$ modulators has been to linearize the loop with an additive noise source and completely ignore the gain of the quantizer (i.e.

same as setting the gain to unity). As seen from Chapter 2, a discrepancy existed between simulation and the theoretical NTF. A previous attempt to rectify this inconsistency resulted in a closer solution, but contained a fundamentally incorrect assumption in that the gain of the quantizer was replaced with a questionable estimate [RKT91] which also resulted in an error between their STF and simulations.

It was seen in Chapter 2 that the gain of the quantizer, for any given architecture, may be characterized. The gain K may be considered as a time-averaged quantity which has the favorable quality of being more or less constant, which to some degree validates the nearly-linear model used. The gain of the quantizer, by one definition, is the convolution of the probability-density function (PDF) of the idling noise seen at V_{oi} with the transfer characteristic of the quantizer [AFG⁺91]. The PDF changes on a per cycle basis, and so the gain of the quantizer fluctuates slightly. This instantaneous gain, as defined from sample period to sample period, depends on the previous integrator outputs [RKT91] and also the value of the gain coefficients of the DIS-DM and the input signal level. Given characterized values, it will be shown quite definitively that the gain K defines the shape of the NTF and STF repeated below, with reference to Figure 4.1.

$$\frac{V_o(z)}{V_i(z)} = \frac{K\alpha_1\alpha_2}{K\alpha_1\alpha_2z^{-1} + (1 - \alpha_1 - K\alpha_2z^{-1})(1 - z^{-1})} \quad \text{Eqn 4.1}$$

Figure 4.1 LiSDM of Figure 2.1, modelled as a linear system with K indeterminate rather than unity

$$\frac{V_{out}(z)}{V_{in}(z)} = K \alpha \left(\frac{1+z^{-1}}{2} \right)^2 \left(\frac{1+z^{-1}}{1-z^{-1}} \right)^2 \quad |H| = 1 \quad \text{Eqn. 4.2}$$

4.2.2 Measured and Simulated Transfer Functions

From Chapter 2, the nominal value for the gain of the quantizer was $K = -4 \text{ dB}$. The theoretical signal and noise transfer functions (STF and NTF) are plotted in Figure 4.2 and Figure 4.3 for a sampling frequency of 2 MHz, the same clock frequency used in measurement. Furthermore, the STF was experimentally confirmed through system-level simulations and measurements from the fabricated device. The results of measured and simulated data are also plotted in Figure 4.2. (Note that the measured data has $(\cos(\omega/2))^{-2}$ applied to the data to compensate for the spectrum analyzer measurements from the bit-stream output.) As regards the STF, it should be noted that the discrepancies between the theoretical and measured (and simulated) magnitudes at high frequency exist due to a departure from the assumption that the gain K is constant. This is a short-coming in the theoretical STF. It will be shown in the next section that acquired STF data depends on the gain K , which appears to decrease in value at high frequencies, which affects the STF. (Note that it is possible that additive noise and correlated tones may interfere with the measurement. However, such a situation was rarely encountered.) The topic of the STF is engaged with greater detail in the next section. To a first order, the nominal gain of $K = -4 \text{ dB}$ sufficiently validates the theoretical STF against simulations and measurement.

The spectrum of the measured (and simulated) NTF is also quite close to the theoretical NTF shown in Figure 4.3 for the $K = -4 \text{ dB}$ case. This may be seen by comparing the shape of the quantization noise spectrums from the simulated modulator of Figure 4.4a) and the measured spectrum of Figure 4.4b) with the shape of the theoretical NTF of Figure 4.3. The quantization noise is essentially flat in all three cases beyond about 400 kHz, consistent with a K of -4 dB .

4.2.3 Frequency Dependence of the Gain of the Quantizer

To explain the discrepancy that exists in the high-frequency portion of the simulated and measured STFs against theory, it is prudent to explore previously unknown characteristics and behavior of the gain of the quantizer at these higher frequencies. It will be shown that the result of this study is key in reconciling these differences regarding the STF.

Figure 4.2 Signal transfer functions for $K = 40\text{ dB}$ with an input of -12 dBV for theoretical, simulated and measured data

Figure 4.3 Theoretical noise transfer function for $K = 0\text{ dB}$ and $K = 40\text{ dB}$

Figure 4.4a

Unwindowed FFT of a system-level simulation. The quantization noise spectrum is essentially flat beyond 400 kHz (Small spectral peak at 400 kHz)

Figure 4.4b

Measured spectrum of the DISDM. Note that the quantization noise has a spectral peak at around 400 kHz. Note that $\sin(x)/x$ filtering at 1 MHz causes 4 dB attenuation, thus the measurement except for the $\sin(x)/x$ effect is essentially flat beyond 400 kHz, making it comparable with the simulation result above.

It is possible to perform system-level simulations to acquire the gain of the quantizer as a function of frequency. Simple simulations of a linear coder are used which include the effects of integrator clipping. (Simulation code may be seen in Appendix A). This was in fact done earlier in Chapter 2 when the gain of the quantizer was investigated as a function of input amplitude for the degenerate modulator used here. A difficulty that may be encountered in simulation is erroneous spectral responses at the output nodes V_{o2} and V_{o1} . An indication of this is excessive tonal behavior. To secure proper results and eliminate tones that might upset the validity of simulation results or measurement, a small DC offset can be applied to the input. Furthermore, the theoretical spectral response at V_{o2} with respect to the quantization noise may be found and used as a useful check against the spectrum of V_{o1} in simulation and measurement. The gain may be found from Figure 4.1 and is

$$\frac{V_{o2}(z)}{C_o(z)} = \frac{z^{-1}[\alpha_2\alpha_4 + \alpha_1(1 - z^{-1})]}{K\alpha_2\alpha_4z^{-1} + 1 - (1 - K\alpha_2)z^{-1}(1 - z^{-1})} \quad \text{Eqn 4.3}$$

In order to acquire the gain of the quantizer as a function of frequency, several sweeps across the spectrum from DC to frequencies near $f_c/2$ may be conducted. Once again, as an example, a nominal -12 dB sinusoidal input with respect to the quantizer levels was applied to the modulator to ensure that the modulator operates away from the overload region. If these lower levels are not used, the resulting gains may become a function of input level. An example of such simulation may be seen in Figure 4.5a) where a -12 dB input at 800 kHz and a DC offset have been applied to the input. This is a particularly clean example in that it is nearly absent of all tones and contains the correct spectral response at V_{o1} as seen when compared to the accompanying theoretical curve in Figure 4.5b). The theoretical curve has been artificially augmented by 10dB so as to clearly demonstrate the shape of the V_{o1} spectrum.

The resulting quantizer gains are plotted in Figure 4.6 as a function of frequency and are accompanied with measured results from the fabricated DISDM. Two characteristics may immediately be noticed. First, as may be seen, the variance of the gain K increases at high frequencies. Secondly, the gain averages to -4 dB at low frequencies and decreases at higher frequencies. That is to say that the gain of the quantizer decreased at very high frequencies in both simulation and measurement nearly merging at the very high frequency range for the example given here. The reason for this is unclear. However, these sweeps in both simulation and measurement were repeated a number of times which lead to the same trends.

Figure 4.5a FFT of a 64 kpoint FFT of a system-level simulation with an input of -12 dB at 800 kHz

Figure 4.5b FFT of the node V_{int1} of the same simulation above. Here, the quantizer gain is -5.8 dB. Also, the theoretical spectrum of V_{int1} is augmented by 10 dB so that the shape of it may be compared with the result of simulation, denoting proper coder operation

Figure 4.6 The simulated (multiple runs i.e. -11.8 dB, -12 dB, -12.2 dB and -12.4 dB) and measured gain of the quantizer as a function of frequency. The input amplitude to the modulator is -12 dB for the measured case.

Generally speaking, any given gain measurement was found to be quite stable from cycle to cycle given any input amplitude, offset and input frequency. Small changes in amplitude were observed to produce (more often than not) small random changes in gain. Small changes in frequency also appeared to have random effects on the gain. At low input frequencies, the variance in the quantizer gain rarely exceeded 0.5 dB. At the higher frequencies, the largest variance was found to be about 1.5 dB in measured data and less than 1 dB in simulation. Also, slightly more tonal behavior was noticed in measurement than in simulation. However, as mentioned earlier, this was mitigated through the use of DC offsets to move any offending tones away from the frequency of interest, where the gain was being measured. Finally, at the higher frequency ranges, where the gain had decreased (i.e. near half the clock frequency), an attempt to find correlation with input levels was made. By reducing the input amplitude to the

coder, no significant increase or decrease in gain took place. Thus, no level dependence was detected unless the input was increased to the levels where clipping takes place (greater than -8dB). In hindsight it could be argued that, near the resonant peak, the measured data may have been influenced by the onset of clipping due to the increased gain from the STF at these frequencies. This may be reinforced by the fact that the simulation data did not reflect this momentary decrease in gain. Beyond the resonant peak (around 200-300 kHz) the decreasing gain as a function of frequency precludes clipping as a possible reason for its behavior.

A criticism of this exercise is that at these higher frequencies, the gain of the quantizer as a time averaged quantity is not as valid since proportionally, the input frequency approaches the sampling frequency [AFG⁺91]. This is because the PDF created from a low frequency signal was assumed to be white. When input signals are higher in frequency, the PDF is made up from a signal that does not act as pseudo-DC anymore, perhaps leaving the PDF of V more correlated with the input. Nevertheless, it is the gain of the quantizer in the signal path that is being measured and should remain valid if the signal component at the input and the output of the quantizer are well defined and above noise. As mentioned earlier, a possible problem is that at high frequencies additive noise and correlated tones may interfere with the measurement. However these mechanisms were not seen in simulation or measurement as causing errors when the proper precautions (i.e. adding a DC offset) are observed.

Given the empirical trend as supported by simulation and measurement, it must now be recognized that these effects will change the shape of and limit the accuracy with which one may predict the theoretical STF (i.e. Eqn 4.1) at high frequencies, as a repercussion of varying and decreasing gain. To be exact, the variance of K on the STF is really only important at higher frequencies, well beyond the baseband. The reason for this is that the STF at high frequencies is more sensitive to changes in K . Conversely, the magnitude of the STF at low frequencies is highly insensitive to the value of K . This is not true of the NTF however. This explains why the STF, when measured or simulated, is not smooth at higher frequencies or at the very least appears ill-defined.

By simply plotting the STF of Eqn 4.1 with K as a random variable between -3.8 dB and -5 dB, fluctuations in the STF at high frequency become evident as seen in Figure 4-7. Furthermore, at low frequencies, the transfer function is smooth and unhindered by variations in the gain K . It should be noted that an even more accurate depiction of the STF might have been

Figure 4.7

STF plotted with a random value of K from -3.8 dB to -5 dB. A reference STF where $K = -4$ dB is plotted for comparison.

portrayed if the average of K had been decreased with increasing frequency. These characteristics correspond to what is seen in measurement.

In concluding, a stable average value of K exists at low frequencies, which decreases at higher frequency accompanied with greater variance in the gain. This pertains to the gain in the signal path by rights, as discussed in Chapter 2. This results in these characteristics discussed in that fluctuations and general behavior of the gain K causes the STF to deviate at high frequency and explains why a frequency sweep across the spectrum results in a transition from a smooth transfer function to a rough one, as typically witnessed in measurement. Also the NTF, with the exception of large input amplitudes, remains constant, also characteristic of a stable K at -4 dB.

This effort has provided a comprehensive understanding of the STF and NTF through a better characterization of the validity of the linearized loop. Moreover, it forms a foundation from which DISDM distortion may be understood. It will be shown later that an accurate representation of the STF is necessary to properly predict the theoretical harmonics from circuit non-linearity in the DISDM. Furthermore, by including the gain K in other related theoretical analysis, results with greater accuracy may be obtained than in the past, an example of which pertains to the topic discussed next, namely the effects of finite opamp gain on quantization noise.

4.3 Finite Gain in Amplifiers

The existence of a difference-mode voltage between the input terminals of an opamp is a direct result of finite open-loop gain. Not only does finite-gain produce a gain error in the system but it also results in a mechanism that can limit the SNR at all amplitudes, thus diminishing the performance of the oversampled A/D. It is the existence of this difference-mode voltage which allows a comprehensive analysis into the topic of nonlinearity to take place later.

The effect of finite gain in the opamps produces a leaky integrator, which in turn causes a zero at frequencies other than DC in the noise transfer function. Thus, not unlike thermal noise in opamps, the spectral response of the DISDM yields a flat spectrum at low frequencies, due now to leaky integration. A nasty manifestation of this effect is a phenomenon known as "deadbanding", the dynamics of which cause a loss of information presented to the input of the modulator. This phenomenon is well documented [FC91] and is not the focus of this thesis. However, the spectral response is of interest as a potential dynamic range limitation.

The treatment of finite gain in opamps in this section pertains to switched-capacitor integrators that make up the sampled-data oversampled A/D. It should be noted however that the results are also applicable for continuous-time integrators and oversampled A/Ds.

The analysis performed here is more accurate than treatments in the past due to the inclusion of the gain of the quantizer. It can easily be shown that for a quantizer gain of -4 dB, an under-

estimate of approximately 5dB would be incurred from conventional treatments where the gain of the quantizer has been ignored, given the gain coefficients used in the DISDM here.

First, consider a typical switched-capacitor integrator that might be found in a DISDM as seen in Figure 4.8a). Taking finite gain into account, the charge-balance equations may be written

Figure 4.8

a) SC Integrator

b) SC Integrator with feedback

(See Appendix C for the complete analysis) which lead to the final z-transform for the leaky integrator, ignoring higher terms

$$\frac{v_o(z)}{v_i(z)} = \frac{-\alpha_1 / \left[1 + \frac{1}{A} (1 + \alpha_1) \right]}{1 - \left(1 - \frac{\alpha_1}{A} \right) z^{-1}}$$

$$\approx \frac{-\alpha_1}{1 - \left(1 - \frac{\alpha_1}{A} \right) z^{-1}}$$

Eqn 4.4

However, either single- or double-integration $\Sigma\Delta$ modulators requires the use of an integrator that sums feedback from the quantizer as seen in Figure 4.8b). The same charge-balance method seen in the appendix leads to the z-transform, approximated as

$$v_o(z) \approx \frac{[-\alpha_1 v_i(z) + \alpha_2 v_o(z)]}{1 - (1 - \frac{\alpha_1 + \alpha_2}{A})z^{-1}} \quad \text{Eqn 4.5}$$

Now, the NTF for a first-order $\Sigma\Delta$ modulator, which includes the effects of finite opamp gain, may be found. Consider the block diagram of Figure 4.9 of a first-order loop. The ideal inte-

Figure 4.9 First-order $\Sigma\Delta$ modulator, modelled to include the effects of finite opamp gain

grator, whose z-transform was

$$T_I(z) = \frac{1}{1 - z^{-1}} \quad \text{Eqn 4.6}$$

is now replaced with the nonideal integrator

$$T_{NI}(z) = \frac{1}{1 - (1 - P)z^{-1}} \quad \text{Eqn 4.7}$$

where the gain error term has been ignored and P represents the correction term due to finite gain of the opamp. The resulting NTF is

$$\frac{v_o(z)}{e_o(z)} = \frac{1 - (1 - \alpha_2/A)z^{-1}}{1 - (1 - \alpha_2/A - K\alpha_2)z^{-1}} \quad \text{Eqn 4.8}$$

where $P = \alpha_2/A$ in this case. If K equals unity, this result agrees in form with [RVR⁺90].

As may be seen, there is a zero in the noise-shaped spectrum and the pole expression in the denominator includes an α_2/A term. As stated earlier, the gain K now having been characterized,

plays a significant role in increasing the accuracy with which the theoretical quantization noise at low frequencies may be found, a point that has not been made in all treatments of this topic by other authors.

It is now possible to extend the consequences of finite gain to the second-order $\Sigma\Delta$ modulator case. Referring to Figure 4.10, the NTF of the DISDM may be found which includes the effects of leaky integration. This results in

$$\frac{v_o(z)}{e_o(z)} = \frac{[1 - (1 - P_1)z^{-1}][1 - (1 - P_2)z^{-1}]}{K\alpha_2\alpha_4z^{-1} + [1 - (1 - P_2 - K\alpha_3)z^{-1}][1 - (1 - P_1)z^{-1}]} \quad \text{Eqn 4.9}$$

where $P_1 = \alpha_4/A$ and $P_2 = (\alpha_2 + \alpha_3)/A$. Again, the noise-shaped spectrum experiences two zeros, one from each integrator, while the pole expressions include finite gain in the same way as discussed in the single-order loop case.

For the 38 dB DC gain opamp that was used in the fabricated DISDMs, a plot of the expected quantization noise spectra may be created, where K is -4 dB from previous characterization. As seen in Figure 4.11, the quantization noise zero is quite apparent and the high-frequency pole has shifted slightly as compared to the case where the opamps have infinite gain.

The theoretical plot of Figure 4.11 may be compared to the simulation of Figure 4.12a) and Figure 4.12b), where the same DC gain opamp is used to get the results. As may be seen, the low-frequency quantization noise flattens out at frequencies below 10 kHz and to an amplitude that is relatively close to theoretical expectations as plotted in Figure 4.11. Also, it may be noted that the high-frequency pole has moved in slightly from 400 kHz to approximately 350 kHz as predicted in theory and is subtly noticeable in simulation as confirmed by comparing Figure 4.12a) to Figure 4.4a). Furthermore, the measured spectrum of Figure 4.13 also compares favorably with theory and simulation.

It must be remembered that the theoretical estimate assumes Gaussian (uncorrelated) white noise. In fact, the quantization noise spectra is usually several dB above the theoretical, which helps explain the difference between theory and simulation or measurement, as was discussed in Chapter 3.

As stated before, the finite gain effect serves to reduce the SNR at all amplitudes. A good rule of thumb has been to allow the DC gain of the opamps to be comparable to or greater than the

Figure 4.10

Second-order $\Sigma\Delta$ modulator, modelled to include the effects of finite opamp gain

Figure 4.11

Theoretical quantization noise spectra for $K = -4$ dB with 38 dB opamp DC gain and infinite DC gain

Figure 4.12a

Full spectral response for the DISDM with 38 dB DC gain. A -50 dBm (into 50 ohms) input was applied to the modulator.

Figure 4.12b

Baseband frequencies of the above simulation.

Figure 4.13 Measured spectrum from DC to 40 kHz for the same input amplitude as in Figure 4.12a) and b)

oversampling ratio for the DISDM [UCL90]. In this way, a minimal, almost insignificant penalty in performance is paid. Such a rule of thumb may be insufficient in order to suppress the effects of nonlinearity however. For the fabricated modulator, as the opamp gain was fairly low, the SNR is severely limited due to this effect as well as the manifestation of circuit non-linearity, the topic that will be discussed next.

It is a simple matter to extend the above analysis to calculate new STFs which include the gain error. The final result of the DISDM with gain error may easily be estimated by including the value of α_n as defined in Appendix C in the analysis where the n subscript refers to the gain coefficient.

4.4 Nonlinearity in Oversampled A/Ds

4.4.1 Introduction

If noise levels are reduced far enough, it is possible that nonlinearity effects may dominate and ultimately limit the dynamic range and hence the resolution of the modulator. Note that finite gain was shown to cause an augmentation in the noise floor due to quantization noise. Additionally, however, finite gain can cause circuit nonlinearity from opamp inputs to be seen. This effect is more likely in high bandwidth circuits, where amplifier gain is sacrificed for speed.

It will be shown that nonlinearity, predominantly from opamps, reduces the SNDR during two distinct ranges of amplitude, thus reducing the dynamic range of the modulator.

Nonlinearity in its simplest form is understood to cause harmonic distortion that appears at the output of the modulator at multiples of the input signal frequency. Alternatively, the intermodulation distortion from two or more input signals is a different manifestation of the same nonlinearity mechanism. This first, basic mechanism is responsible for degrading the dynamic range at high input amplitudes, where harmonic distortion is typically significant and present in the baseband. However, it is not the only manifestation of nonlinearity which occurs, as alluded to in Chapter 2. Due to the breakdown of the assumption that the quantizer produces white uncorrelated quantization noise, strongly correlated spectra appear. These spectra are related to the limit-cycle behavior of the modulator and they interact with circuit nonlinearities. These strongly correlated (i.e. non-random) spectra intermodulate with one another, producing intermodulation distortion difference products that appear at baseband frequencies. This second distortion mechanism typically occurs at lower input amplitudes when the tonal spurs become significant in amplitude. This secondary phenomenon degrades the SNR throughout a second range of input amplitudes.

An attempt to analytically determine the harmonic distortion at the output of the modulator may be made, which then makes it possible to estimate the amount of distortion that will be

intermodulated back to baseband frequencies from high-frequency spurs, reducing the dynamic range beyond what is expected from signal harmonics.

Sources of circuit nonlinearity in serial oversampled A/Ds that use two-level quantizers (and 1-bit DACs) can also come from nonlinear capacitors. The quantizer plays no direct role in randomizing or modifying the power associated with harmonics that are normally a consequence of circuit nonlinearity. As seen, the consequence of circuit nonlinearity is in fact harmonic distortion, as witnessed from simulation in Chapter 2, and not a modification of quantization noise spectra. Harmonic distortion in all opamp-based circuits may be referred to the input [Ber88] [LM85], resulting in a coherent, dependent signal source. Unlike noise however, this input-referred nonlinearity is regulated by the magnitude of the input signal that produces it. Thus, it is unnecessary to invoke any greater role for the quantizer other than having to modify the STF of the circuit, as already discussed, by including K .

The reason for this is because the accuracy with which harmonic distortion is predicted depends upon the transfer function that governs the distortion. As a result, the gain of the quantizer K must be utilized to obtain the proper linearized STF that forms the basis with which theoretical distortion is founded upon. Furthermore, the nature of gain K to decrease with increasing frequency will be invoked to further increase prediction accuracy later on.

4.4.2 Harmonic Distortion from Opamp Nonlinearity

4.4.2.1 Theoretical Analysis

The approach taken to calculate the distortion products at the output of the DISDM is summarized below, describing the mathematical steps used.

The following analysis is based on the well-known work of Lee & Meyer [LM85] and has been extended to include frequency dependence in the STF of the DISDM. The analysis is approximate, however it is sufficiently accurate for purposes of this study. Specifically, it is accurate in the passband where there is no frequency dependence. Also, beyond the natural frequency of the STF, the second- and third-order distortion terms have nominal -24dB/octave and -36dB/octave rolloffs respectively as seen in continuous-time systems (i.e. proportional to the STF squared and cubed respectively).

Since the STF is highly sensitive to the variance of the quantizer gain at high frequencies, the prediction of distortion in this frequency range cannot be absolutely precise. Given this, it is nevertheless relatively easy to validate the manner in which intermodulation of high frequency spurs take place and to estimate their amplitudes with relative accuracy.

With reference to opamp-based circuits, the first step is to write out the transfer function of the circuit. Assume that the nonlinear integrators that make up the circuit are a consequence of nonlinearity in the opamps only. As the opamp has finite gain, the transfer function will include a gain error term which in turn contains the input difference-mode voltage v_d of the opamp, or simply v_o/a_1 where a_1 is the open-loop gain of the opamp.

Such simplicity is afforded by the opamp's characteristic in demonstrating only static nonlinearity in this case, since signals settle by nature of the sampled-data system. Thus all processes proceed to completion. The next logical step is to invoke nonlinearity by expressing the output voltage v_o by a nonlinear representation or power series expansion of the difference-mode voltage so that

$$v_o = a_1 v_d + a_2 v_d^2 + a_3 v_d^3 \quad \text{Eqn 4.10}$$

Note that only the first three terms in the expansion are considered significant. Finally, the difference-mode voltage v_d must be found as a function of the input voltage, v_i . This step can become quite involved, depending on the complexity of the circuit. The result is an expression for v_o in terms of a power series in v_i ,

$$v_o = b_0 + b_1 v_i + b_2 v_i^2 + b_3 v_i^3 \quad \text{Eqn 4.11}$$

At this point, it is a simple matter to find the harmonics. This analysis will continue with more attention paid to the designed structure in order to calculate the effects of opamp nonlinearity later.

It is now timely to rework the transfer function to include nonlinearity described through a power series expansion in some form within the z-domain. The following approach is by no means highly precise. It is accurate enough for the purpose of validating the mechanisms at work here, particularly with reference to the second-order intermodulation distortion product of interest - namely that of high-frequency spurs intermodulated down to the baseband. More complex analysis, such as Volterra theory, is beyond the intended scope of this thesis. "Here

approximations are made, they are stated and the conditions for their use included with appropriate text.

4.4.3 Z-Domain Analysis of the DISDM (Including Opamp Nonlinearity)

In order to determine the effects of opamp nonlinearity upon the DISDM, it is timely to derive the nonlinear transfer function for it. Referring to Figure 4.1, it is useful to write out the transfer function for individual integrator stages. These are, for the second stage,

$$v_o(z) = \frac{K\alpha_2}{[1 - (1 - K\alpha_1)z^{-1}]} v_{o1}(z) \quad \text{Eqn 4.12}$$

and for the first stage,

$$v_{o1}(z) = \frac{1}{1 - z^{-1}} (\alpha_1 v_i(z) + \alpha_2 z^{-1} v_o(z)) \quad \text{Eqn 4.13}$$

This assumes infinite opamp gain.

To reveal the effects of opamp nonlinearity, it is necessary to consider a more detailed picture. By utilizing charge balance, finite gain effects may be included. However, this need only be done for the first integrator. This is because the high loop gain present in the system, as for noise, allows nonlinearity to be ignored beyond the first integrator. This greatly simplifies the transfer function. We re-examine the front end of the structure through charge balance and including the difference-mode input voltage. With reference to Figure 4.8b), the charge balance for this integrator is:

On ϕ_1 :

$$C_{H1}[(v_{o1,n-1,2} - v_{d,n-1,2}) - (v_{o,n-1,1} - v_{d,n-1,1})] = 0 \quad \text{Eqn 4.14}$$

On ϕ_2 :

$$C_{H1}[(v_{o1,n} - v_{d,n}) - (v_{o1,n-1,2} - v_{d,n-1,2})] + C_1(v_{i,n} - v_{d,n}) + C_1(v_{o,n} - v_{d,n}) = 0 \quad \text{Eqn 4.15}$$

Dividing by C_{H1} and re-arranging, yields

$$v_{o1}(z) = \frac{\alpha_1 v_i(z) + \alpha_2 z^{-1} v_o(z) + v_d(z)(1 + \alpha_1 + \alpha_2)}{1 - z^{-1}} \quad \text{Eqn 4.16}$$

where $\alpha = C_1/C_L$ and $\alpha_1 = C_1/C_L$.

Substituting Eqn 4.16 into Eqn 4.12 yields (after re-arranging) the transfer function including the effects of finite gain in the first integrator only.

$$\frac{K\alpha\alpha_1 v_d(z)}{v_o(z)} = K\alpha_1 \frac{v_o(z)}{a} (1 + \alpha_1 + \alpha_1 z^{-1})$$

$$1 + [K(\alpha_1 + \alpha_1\alpha_1) - 2]z^{-1} + (1 - K\alpha_1)z^{-2}$$
Eqn 4.17

where $\alpha = C_1/C_L$ and $\alpha_1 = C_1/C_L$.

To find the nonlinear transfer function, it is necessary to re-write v_o in terms of v_d . From

$$T(z) = \frac{v_o(z) - v_d(z)}{v_d(z) - v_o(z)}$$
Eqn 4.18

it is not hard to equate

$$v_o(z) = T(z) + \frac{v_d(z)}{v_o(z)} = a v_d(z)$$
Eqn 4.19

where $v_d(z)$ is the input difference mode voltage of the first opamp, where (linear) $T(z)$ is Eqn 4.1 and $v_o(z) - v_d(z)$ is Eqn 4.12. Hence

$$v_d(z) = \frac{1 - T(z)}{a_1 v_o(z) / v_d(z)} v_o(z)$$

$$= \frac{1 - \alpha_1 [1 - z^{-1} - K\alpha_1 z^{-1}]}{a_1 [D(z) - 1]} v_o(z)$$
Eqn 4.20

where $D(z) = 1 + [K(\alpha_1 + \alpha_1\alpha_1) - 2]z^{-1} + (1 - K\alpha_1)z^{-2}$. Thus the existence of a difference-mode voltage has been established due to feedback which may be used to drive the nonlinearity as described next. The nonlinearity of the first opamp may be described by the power series expansion

$$v_{o1}(z) = a v_d(z) + a_1 v_d^2(z) + a_2 v_d^3(z)$$
Eqn 4.21

These, when substituted into Eqn 4.17 yield

$$v_o(z) = \frac{K\alpha_1\alpha_2 v_i(z)}{D(z)} - \frac{K\alpha_2(1+\alpha_1+\alpha_4-z^{-1})}{D(z)} \left[V_{in}(z) + \frac{a_2}{a_1} V_{in}(z) + \frac{a_3}{a_1} V_{in}(z) \right] \quad \text{Eqn 4.22}$$

It should be noted that the term $K\alpha_2(1+\alpha_1+\alpha_4-z^{-1})/D(z)$ represents the noninverting transfer function of the DISDM from the noninverting input of the first opamp through to the output of the DISDM. More on this point later.

Finally, substitution of Eqn 4.20 into Eqn 4.22 yields

$$\begin{aligned} v_o(z) = & \frac{K\alpha_1\alpha_2}{D(z)} \left[1 + \frac{(1+\alpha_1+\alpha_4-z^{-1})[1-(1-K\alpha_1)z^{-1}]}{a_1 D(z)} \right] V_i(z) \\ & - \frac{a_2 K\alpha_2\alpha_1^2(1+\alpha_1+\alpha_4-z^{-1})[1-(1-K\alpha_1)z^{-1}]}{a_1^3 [D(z)]^3} V_i(z) \\ & + \frac{a_3 K\alpha_2\alpha_1^3(1+\alpha_1+\alpha_4-z^{-1})[1-(1-K\alpha_1)z^{-1}]}{a_1^4 [D(z)]^4} V_i(z) \end{aligned} \quad \text{Eqn 4.23}$$

Applying to the input two signals of amplitude V_{in} and V_{in} with frequencies ω_1 and ω_2 as per the review in Chapter 2, leads to the second-order IMD products

$$imd(\omega_1 - \omega_2) = \frac{a_2 K\alpha_2\alpha_1^2(1+\alpha_1+\alpha_4-e^{-j\omega_1 T})[1-(1-K\alpha_1)e^{-j\omega_1 T}]}{a_1^3 [1 + [K(\alpha_1+\alpha_2\alpha_4)-2]e^{-j\omega_1 T} + (1-K\alpha_1)e^{-j2\omega_1 T}]} V_{in} V_{in} \quad \text{Eqn 4.24}$$

assuming that $\omega = \omega_1 \approx \omega_2$ and that $\omega_1 - \omega_2$ lies in the flat, baseband region. It is this second order IMD product that is of prime importance in this thesis. For completeness, an estimate of (or the pre-filtered) third-order IMD products is

$$imd(2\omega_2 - \omega_1) \approx \frac{3a_3 K\alpha_2\alpha_1^3(1+\alpha_1+\alpha_4-e^{-j\omega_1 T})[1-(1-K\alpha_1)e^{-j\omega_1 T}]}{4a_1^4 [1 + [K(\alpha_1+\alpha_2\alpha_4)-2]e^{-j\omega_1 T} + (1-K\alpha_1)e^{-j2\omega_1 T}]} V_{in} V_{in} \quad \text{Eqn 4.25}$$

These equations are approximate and will be plotted and discussed in the next section. More importantly, as proven by simulation and measurement, the gain of the quantizer tends to decrease particularly at frequencies near half the clock frequency. As a result, the above equa

tions tend to be inaccurate particularly at the higher frequencies. As a thrust in this study is to reconcile the intermodulation of high-frequency spurs, a better method must be employed to gain accuracy.

4.4.4 Continuous-Time Equivalent Modelling

4.4.4.1 Rationale for this Approach

The determination of harmonic distortion due to circuit nonlinearity within the oversampled A/D may be accomplished by now modelling the switched-capacitor DISDM in Figure 4.14a) as a continuous-time biquad filter shown in Figure 4.14b). This is the preferred approach taken to determine harmonic distortion in this thesis because the s-domain may be used to approximate the high-frequency behavior of the STF. Note that here, the resistors do not equal the switched-capacitor resistor equivalents $R = 1/f_s C$ directly. This is because two fundamental differences exist between the biquad and DISDM. Firstly, the delay in the feedback path does not allow a direct mapping between the transfer function of the DISDM and the biquad. Secondly, the gain K of the quantizer plays an role as already discussed.

In effect, the approach taken here is to fit a biquadratic polynomial, synonymous with the biquad filter, to the sampled-data DISDM transfer function to produce a continuous-time equivalent transfer function. From this, the determination of the nonlinear transfer function may then proceed in the same way as was for the z-domain nonlinear STF. This approach is attractive because of the ease with which one may mathematically tune the continuous-time filter to fit the STF of the z-domain DISDM. For instance, orthogonal tuning may be used to set ω_0 and Q of the biquad filter to match that of the DISDM.

It should be noted that there will be a good correlation between the two transfer functions at low to moderate frequencies. Near half the sampling frequency the magnitude of the continuous-time STF is representative of the real sampled-data transfer function that tries to incorporate the effects of the gain K of the quantizer. As a result, precise calculation is not possible at these very high frequencies, although calculations do lead to good estimates and validate the mechanisms under study.

It is now a simple matter to include amplifier finite gain, and extend the continuous-time filter analysis to include the effects of opamp nonlinearity, the dominant source of harmonic distortion.

Figure 4.14a Sampled-data version of the DISDM. (Simplified)

Figure 4.14b Continuous-time version of the DISDM, modelled as a biquad filter. (Simplified)

tion in this particular case. The reader is reminded that generally, noise and nonlinearity mechanisms are only significant at the input of the first opamp of the DISDM. The contribution of such mechanisms due to the second opamp is insignificant due to the high loop gain offered by the circuit in addition to the high-pass filtering action of the second integrator.

4.4.4.2 Equivalent Circuit Distortion

As already stated, a continuous-time biquad equivalent circuit of Figure 4.14b) is used to model the effects of nonlinearity by finding appropriate values of the components (usually ratios of components is sufficient) given the ω_o and Q of the DISDM's transfer function. This method is possible because nonlinearity may be input-referred as will be demonstrated later. Thus distortion in the form of harmonics and intermodulation distortion products goes through to the output according to the closed-loop behavior as dictated by the transfer function. As long as the equivalent circuit has a transfer function that is for all intents and purposes the same as the DISDM, this method will be valid. The equivalent biquad transfer function could be kept in terms of general parameters (i.e. ω_o , Q) but is better in terms of components. Keeping to the latter allows the facilitation of finite gain which would then lead to a closed-form nonlinear transfer function with resistors as switched-capacitor resistor equivalents ($R = 1/f_s C$, where it must be stressed that the capacitors are not those seen in Figure 4.14a) so that ratios of components rather than absolute values may be found.

With reference to Figure 4.14b), the transfer function of this equivalent circuit may be found in accordance to the mathematical road map laid out earlier. Ignoring the quantization noise and including the difference-mode voltage v_d of the first opamp only, the transfer function may be found by summing currents into the virtual grounds of each opamp.

$$\frac{v_i - v_d}{R_1} + \frac{v_o - v_d}{R_4} + (v_{o1} - v_d)sC_1 = 0 \quad \text{Eqn 4.26}$$

$$\frac{-v_{o1}}{R_2} + \frac{v_o}{R_3} + sC_2 v_o = 0 \quad \text{Eqn 4.27}$$

Through the linear approximation that $v_d = v_{o1}/a_1$, the voltage at the output of the equivalent biquad circuit which includes the effects of finite gain is

$$v_o(s) = - \frac{R_4/R_1}{1 + sC_1 \frac{R_2 R_4}{R_3} + s^2 C_1 C_2 R_2 R_4} v_i(s) + \frac{R_4/R_1 (1 + \frac{1}{R_4 R_1} + sC_1 R_1)}{1 + sC_1 \frac{R_2 R_4}{R_3} + s^2 C_1 C_2 R_2 R_4} \frac{v_{o1}(s)}{a_1} \quad \text{Eqn 4.28}$$

For simplicity, the components of the above equation are identified and may be written as

$$v_o(s) = - \frac{G_{DC}}{D(s)} v_i(s) + \frac{G_{DC} (1 + 1/G_{DC} + sC_1 R_1)}{D(s)} \frac{v_{o1}(s)}{a_1} \quad \text{Eqn 4.29}$$

where the DC gain is $G_{DC} = R_4/R_1$, the polynomial in the denominator is represented by $D(s) = 1 + sC_1 (R_2 R_4/R_3) + s^2 C_1 C_2 R_2 R_4$.

The static nonlinearity of the first opamp may be modeled by a power series expansion

$$v_{o1} = a_1 v_d + a_2 v_d^2 + a_3 v_d^3 + \dots + a_n v_d^n \quad \text{Eqn 4.30}$$

where a_n are the open-loop coefficients that describe the nonlinearity of the opamp. Recall that these coefficients were found in Chapter 2, from characterizing the linearity of the fabricated opamp. Only static (frequency-independent) nonlinearity is required here as well since in sampled-data circuits the signals settle at the output of opamps. Had this been a continuous time implementation, dynamic nonlinearity may have been accounted for by replacing $a_1 \rightarrow a_{10}/(1 + s\tau_d)$ where τ_d is the time constant associated with the dominant pole of the opamp. Substitution of Eqn 4.30 into Eqn 4.29, neglecting higher order power series coefficients, yields

$$v_o(s) = - \frac{G_{DC}}{D(s)} v_i(s) + \frac{G_{DC}}{D(s)} N(s) \left[\frac{a_1 v_d + a_2 v_d^2 + a_3 v_d^3}{a_1} \right] \quad \text{Eqn 4.31}$$

where $N(s) = (1 + 1/G_{DC} + sC_1 R_1)$. It should be noted that the term $[G_{DC}/D(s)] N(s)$ is the fundamental noninverting transfer function of the biquad from the noninverting terminal of the first opamp through to the output. The above equation (as well as the z-domain counterpart of Eqn 4.22) gives key insight to the fact that opamp distortion seen at the output (of the opamp) may be considered as input-referred (from the division of a_1), which then gets multiplied by the closed-loop (noninverting transfer function) gain of the biquad circuit. Note now the ideal gain of the second integrator alone is

$$G_{INT2}(s) = \frac{v_o(s)}{v_{o1}(s)} = \frac{R_3}{R_2(1 + sC_2R_3)} \quad \text{Eqn 4.32}$$

The ideal transfer function of the biquad $v_o(s)/v_i(s)$ may be found by letting the open-loop gain of the opamp approach infinity in Eqn 4.28. In other words, the difference-mode voltage v_d is set to zero so Eqn 4.28 becomes the ideal filter transfer function

$$v_o(s) = \frac{R_4/R_1}{1 + sC_1 \frac{R_2R_4}{R_3} + s^2C_1C_2R_2R_4} v_i(s) \quad \text{Eqn 4.33}$$

and the distortion terms in Eqn 4.31 are gone.

Dividing Eqn 4.33 by the gain of the second integrator yields the transfer function of $v_{o1}(s)/v_i(s)$ so the output of the first integrator is a function of the input signal.

$$v_{o1}(s) = \frac{-\frac{R_4R_2}{R_1R_3}(1 + sC_2R_3)}{1 + sC_1 \frac{R_2R_4}{R_3} + s^2C_1C_2R_2R_4} v_i(s) \quad \text{Eqn 4.34}$$

knowing that $v_d = v_{o1}/a_1$, the difference-mode voltage at the input of the first opamp may be written as a function of v_i ,

$$\begin{aligned} v_d(s) &= \frac{-\frac{R_4R_2}{R_1R_3}(1 + sC_2R_3)}{1 + sC_1 \frac{R_2R_4}{R_3} + s^2C_1C_2R_2R_4} \frac{v_i(s)}{a_1} \\ &= -\frac{G_{DC}/(G_{INT1}(s))}{D(s)} \frac{v_i(s)}{a_1} \end{aligned} \quad \text{Eqn 4.35}$$

Note that at this point a small perturbation from the ideal linear solution caused by finite opamp gain, a_1 , has been established. Consider the effect of this linear voltage component of v_d on the higher-order nonlinear coefficients. Substitution of Eqn 4.35 into Eqn 4.31 and ignoring the DC offset component yields

$$\begin{aligned}
 v_o(s) = & \left(-\frac{G_{DC}}{D(s)} - \frac{G_{DC}/(G_{INT2}(s))}{D(s)} - \frac{1}{a_1} N(s) \frac{G_{DC}}{D(s)} \right) v_i(s) \\
 & + \frac{a_2}{a_1^2} \left(\frac{G_{DC}/(G_{INT2}(s))}{D(s)} \right)^2 N(s) \frac{G_{DC}}{D(s)} [v_i(s)]^2 \\
 & - \frac{a_3}{a_1^3} \left(\frac{G_{DC}/(G_{INT2}(s))}{D(s)} \right)^3 N(s) \frac{G_{DC}}{D(s)} [v_i(s)]^3
 \end{aligned}$$

Eqn 4.36

which may be written in a more appealing form

$$v_o(s) = A_1(s) v_i(s) + A_2(s) [v_i(s)]^2 + A_3(s) [v_i(s)]^3 \quad \text{Eqn 4.37}$$

Here, the closed-loop, equivalent circuit linearity coefficients $A_n(s)$ are frequency dependent all due to the frequency dependence of the STF. Of particular interest are the second- and third-order intermodulation distortion products. The fundamental, second and third linearity coefficients are

$$\begin{aligned}
 A_1(s) &= -\frac{G_{DC}}{D(s)} - \frac{1}{a_1} \left(\frac{G_{DC}}{D(s)} \frac{1}{G_{INT2}(s)} \right) \frac{G_{DC}}{D(s)} N(s) \\
 &\approx -\frac{G_{DC}}{D(s)}
 \end{aligned} \quad \text{Eqn 4.38}$$

$$A_2(s) = \frac{a_2}{a_1^2} \left(\frac{G_{DC}}{D(s)} \frac{1}{G_{INT2}(s)} \right)^2 \frac{G_{DC}}{D(s)} N(s) \quad \text{Eqn 4.39}$$

$$A_3(s) = \frac{a_3}{a_1^3} \left(\frac{G_{DC}}{D(s)} \frac{1}{G_{INT2}(s)} \right)^3 \frac{G_{DC}}{D(s)} N(s) \quad \text{Eqn 4.40}$$

It is now an easy task to determine intermodulation distortion for the DISDM given the linearity of the open-loop opamp. The resulting second-order IMD products are

$$imd(\omega_1 + \omega_2) = \frac{a_2}{a_1^2} \left(\frac{G_{DC}}{D(s)} \frac{1}{G_{INT2}(s)} \right)^2 \frac{G_{DC}}{D(s)} N(s) V_{\omega_1} V_{\omega_2} \quad \text{Eqn 4.41}$$

where it is assumed that $\omega_1 - \omega_2 \approx \omega_1$ and that the IMD product at frequency $\omega_1 - \omega_2$ lies in the flat baseband region.

The third-order IMD product may be estimated as (or conversely the pre-filtered third-order IMD products equal)

$$imd(2\omega_2 - \omega_1) \approx \frac{3}{4} \frac{a_3}{a_1^3} \left(\frac{G_{DC}}{D(s)} \frac{1}{G_{INT2}(s)} \right)^3 \frac{G_{DC}}{D(s)} N(s) V_{i1} V_{i2}^2 \quad \text{Eqn 4.42}$$

These equations that describe the IMD products may be broken down in a manner useful for modelling, giving the reader insight into the way in which nonlinearity propagates through to the output of the DISDM.

The second-order IMD product may be described as

$$imd(\omega_1 - \omega_2) = \frac{a_2}{a_1} \left(\frac{\text{voltage at } V_{o1}}{a_1} \right)^2 (\text{noninverting Transfer Function}) \quad \text{Eqn 4.43}$$

Similarly,

$$imd(2\omega_2 - \omega_1) \approx \frac{3}{4} \frac{a_3}{a_1} \left(\frac{\text{voltage at } V_{o1}}{a_1} \right)^3 (\text{noninverting Transfer Function}) \quad \text{Eqn 4.44}$$

where the noninverting transfer function refers to the closed-loop gain from the noninverting terminal of the first opamp on through to the output of the DISDM. This may be graphically seen in Figure 4.14b).

This agrees in form with [LM85] as previously discussed, and although approximate, contains nominal -24dB/octave and -36dB/octave rolloffs in $A_2(j\omega)$ and $A_3(j\omega)$ respectively as expected through the range of frequencies from beyond the resonant peak up to half the clock frequency for the structure used here.

4.4.4.3 Comparison Between Theory and Measurement

Given the DISDM's signal transfer function in the z-domain, $T(z)$, it is an easy task to match the equivalent biquad circuit's transfer function, $A_1(s)$, to it. The Tow-Thomas biquad filter shown in Figure 4.14b) is very flexible in that the Q of the filter is orthogonal to ω_o and G_{DC}

$$\omega_0 = \sqrt{\frac{1}{C_1 C_2 R_2 R_4}} \quad [\text{rads}^{-1}] \quad \text{Eqn 4.45}$$

$$Q = R_3 \sqrt{\frac{C_2}{C_1 R_2 R_4}} \quad \text{Eqn 4.46}$$

$$G_{DC} = \frac{R_4}{R_1} \quad \text{Eqn 4.47}$$

Given the DC gain, natural frequency and Q from $T(z)$, the ability to selectively adjust a parameter to independently adjust Q , ω_0 and G_{DC} for the continuous-time filter allows a good match throughout most of the frequency spectrum, as may be seen in Figure 4.15. This was accomplished by letting $R = 1/f_s C_R$ in the equivalent biquad circuit where $f_s = 2$ MHz, the clock frequency used in measurement. When the switched-capacitor resistor equivalent is

Figure 4.15 Biquadratic polynomial fit of the sampled-data STF.

used, all the equations and parameters that describe the biquad become a function of capacitor ratios and f_s . Thus Eqn 4.45 through to Eqn 4.47 become

$$\omega_o = f_s \sqrt{\frac{C_{R2}C_{R4}}{C_1C_2}} \quad [\text{rads/s}] \quad \text{Eqn 4.48}$$

$$Q = \frac{1}{C_{R3}} \sqrt{\frac{C_2}{C_1} C_{R2}C_{R4}} \quad \text{Eqn 4.49}$$

$$G_{DC} = -\frac{C_{R1}}{C_{R4}} \quad \text{Eqn 4.50}$$

It is now a trivial matter to fulfil ω_o , Q and G_{DC} independently. For the case at hand, the degenerate DISDM with a nominal quantizer gain of $K = -4$ dB, the natural frequency and Q were found at approximately $f_o = 350$ kHz and $Q = 1.1$. The equivalent biquad transfer function matches well to $T(z)$, when with the help of the above equations, $C_1 = C_2 = 90\%$ and $C_{R1} = 91\%$ of the other capacitors.

The new STF now mimics the sampled-data STF that includes the decreasing gain of the quantizer as empirically seen. In fact, measurements and simulation show this to be true as seen in Figure 4.16, where a comparison is made between the equivalent biquad STF and the measured STF. Note that the measured data, denoted by the "+" signs in the figure, have been $[\sin(x)/x]^{-1}$ compensated to account for the spectrum analyzer, as was done for Figure 4.2.

Now that $A_1(s) \approx -G_{DC}/D(s)$ has been found, the remaining linearity coefficients $A_2(s)$ and $A_3(s)$ are automatically defined from Eqn 4.39 and Eqn 4.40. In this case, the coefficients reduce to

$$A_1(j2\pi f) = -\frac{C_{R1}/C_{R4}}{\left[1 - \left(\frac{2\pi f}{f_s}\right)^2 \left(\frac{C_1C_2}{C_{R2}C_{R4}}\right)\right] + j\left(\frac{2\pi f}{f_s}\right) \left(\frac{C_1C_{R3}}{C_{R2}C_{R4}}\right)} \quad \text{Eqn 4.51}$$

$$A_2(j2\pi f) = \frac{a_2}{a_1} \left[\frac{C_{R1}/C_{R4}}{\left[1 - \left(\frac{2\pi f}{f_s}\right)^2 \left(\frac{C_1C_2}{C_{R2}C_{R4}}\right)\right] + j\left(\frac{2\pi f}{f_s}\right) \left(\frac{C_1C_{R3}}{C_{R2}C_{R4}}\right)} \right]^2 \left[\frac{C_{R3}}{C_{R2}} \left(1 + \frac{j2\pi f C_2}{f_s C_{R3}}\right) \right]^2 \left(1 + \frac{C_{R4}}{C_{R1}} + \frac{j2\pi f C_1}{f_s C_{R1}}\right) \quad \text{Eqn 4.52}$$

Figure 4.16 Theoretical STF of the equivalent biquad versus the measured and simulated STF

$$A_3(j2\pi f) = \frac{a_3}{a_1^4} \left[\frac{C_{R1}/C_{R4}}{\left[1 - \left(\frac{2\pi f}{f_s} \right)^2 \left(\frac{C_1 C_2}{C_{R2} C_{R4}} \right) \right] + j \left(\frac{2\pi f}{f_s} \right) \left(\frac{C_1 C_{R1}}{C_{R2} C_{R4}} \right)} \right]^4 \left[\frac{C_{R3}}{C_{R2}} \left(1 + \frac{j2\pi f C_2}{f_s C_{R3}} \right) \right]^4 \left(1 + \frac{C_{R4}}{C_{R1}} + \frac{j2\pi f C_1}{f_s C_{R1}} \right)$$

Eqn 4.53

where substitution of selected capacitor ratios yields an equation in f and f_s only plus constants.

Now, the closed-loop linearity coefficients $A_1(j2\pi f)$, $A_2(j2\pi f)$ and $A_3(j2\pi f)$ may be evaluated at any frequency, assuming the open-loop opamp linearity coefficients a_1 , a_2 and a_3 are known.

The absolute second-order intermodulation distortion product, denoted by $imd(f_1, f_2)$ for inputs V_{i1} and V_{i2} at frequencies f_1 and f_2 , is

$$imd(f_1 - f_2) = A_2(j2\pi f) V_{i1} V_{i2} \quad \text{Eqn 4.54}$$

where it is assumed that $f = f_1 = f_2$ and that the IMD product at frequency $f_1 - f_2$ lies in the flat baseband region.

The third-order IMD product may be estimated as (or the pre-filtered IMD product equals)

$$imd(2f_2 - f_1) = \frac{3}{4} A_3(j2\pi f) V_{i1} V_{i2}^2 \quad \text{Eqn 4.55}$$

It is not difficult to see that the magnitude of the image intermodulation distortion (IMD) products (those that exist above f_1 and f_2) are equal to the low-frequency IMD products below the fundamental input signals when, and only when, f_1 and f_2 lie well within the flat baseband region. Thus, the only distortion products that need be of interest are $imd(f_1 - f_2)$ and $imd(2f_2 - f_1)$ in this case. This is not true when IMD products exist where filtration of distortion products may occur. Assuming that the two signals are combined or mixed linearly, the intermodulation test method is superior to the single signal harmonic test method. This is because the second- and third-order IMD products are unaffected by the harmonic distortion of the signal source. This is to say that signal harmonics from the source do not occur at the intermodulation frequencies, where nonlinearity from the DISDM produces distortion.

It should be pointed out that the f in $s = j2\pi f$ within the closed-loop linearity coefficients $A_1(s)$, $A_2(s)$ and $A_3(s)$ refers to the fundamental signal frequency and not the harmonic frequencies. In the case here of intermodulation distortion, it must be assumed that the two fundamental signals at f_1 and f_2 are nearly the same frequency for $A_2(s)$ and $A_3(s)$ to be valid.

Given the nonlinearity of the opamp, as characterized in Chapter 3, the second- and third-order IMD products for both the sampled-data and equivalent continuous-time domains are plotted from DC to $f_s/2$ in Figure 4.17 and Figure 4.18 respectively. The magnitudes of the IMD products have been normalized for 0 dBm inputs (V_{i1} and V_{i2}) which are closely spaced in frequency such that $f = f_1 = f_2$. As may be seen, there is very good correlation between the theoretical sampled-data and the equivalent continuous-time biquad products at all frequencies except near half the clock frequency. It follows that because the transfer function of the real device has what is considered a relatively constant roll-off rate, the distortion will also have these same high-frequency characteristics. It is these graphs that are of interest for comparison with measurement.

Figure 4.17

Comparison between the theoretical s- and z-domain second-order IMD products normalized for 0dBm inputs as a function of input signal frequency. (Both inputs are considered to have nearly the same frequency).

Figure 4.18

Comparison between approximate (theoretical) s- and z-domain third order IMD products normalized for 0dBm inputs as a function of input signal frequency. (Both inputs are considered to have nearly the same frequency).

Figure 4.19 Theoretical versus measured IMD (normalized) $imd(f_1 - f_2)$ products

Consider Figure 4.19, a plot of the second-order IMD products as before. For clarity, an interpretation of this graph follows. If two input signals closely spaced in frequency at 10 kHz and 14 kHz, both at 0 dBm in amplitude, are applied to the input of the modulator, a -42 dBm harmonic would theoretically exist at 4 kHz. In fact, this is exactly what is done in experiment. Both input signals V_{i1} and V_{i2} have been set at 0 dBm for simplicity of measurement. As may be seen in a spectrum analyzer plot of the bit-stream output, Figure 4.20 shows how V_{i1} and V_{i2} are placed 4 kHz apart at 10 kHz and 14 kHz respectively. The resulting IMD product at 4 kHz ($imd(f_1 - f_2)$) may be read off the plot directly.

This distance was chosen so that the intermodulation distortion frequencies are unique and this distance also fills the criterion for $A_2(j2\pi f)$ and $A_1(j2\pi f)$ to be valid, as discussed above. As may be seen in Figure 4.20, a typical spectrum analyzer plot of the DISDM bit-stream

Figure 4.20 Spectrum analyzer plot of bit-stream output of the DSDV with two input tones at 0.0 MHz and 1.4 MHz. The plot shows the spectrum and resulting VC products from non-linearity.

shows a 4 kHz second-order intermodulation distortion (IMD) product and a third-order 6 kHz IMD product. Note that also a higher-order fifth-order IMD product at 2 kHz exists, but the higher-order harmonics are beyond the scope of this thesis due to the difficulty in establishing a reliable quantitative value for a_4 and a_5 at the time of determining the open-loop linearity coefficients of the opamp.

By moving the input signals up in frequency, while keeping them separated by 4 kHz, a comparison between the theoretical and measured $imd(f_1 - f_2)$ may be made, shown in Figure 4.19. It was observed that the IMD products can vary in amplitude from moment to moment, particularly when the input signals are at high frequency. This is understandable since the gain of the quantizer affects the STF at high frequencies. It then follows that $A_2(s)$ and $A_1(s)$ would also be influenced by the gain K .

The error bars here represent the variance of the IMD products that was observed in measurement. At low frequencies, less than ± 2 dB variance was seen of these IMD products (including measurement error) while at higher frequencies, the observed variance was larger. The largest error at ± 5 dB occurred at frequencies near $f_s/2$. The fact that the IMD products follow the theoretical curve reinforces the argument for a decreasing K with frequency.

In much the same way, the third-order IMD products may be studied. As already seen in Figure 4.20, a third-order IMD product exists at 6 kHz. A plot of the theoretical $imd(2f_2 - f_1)$ of the equivalent biquad circuit from DC to $f_s/2$ may be found in Figure 4.21. Whereas before, the $imd(f_1 - f_2)$ harmonic always remained at 4 kHz, the $imd(2f_2 - f_1)$ products always trails the lowest driving signal in frequency by 4 kHz. As stated earlier, as the frequency dependence of the transfer function begins to take effect beyond the flat, baseband frequencies the theoretical third-order IMD products are just approximate. The match is as good as it is due to the limited frequency sweep plus a transfer function that does not deviate too much in the region under study. Hence, by sweeping the input signals from DC to 500 kHz, a comparison between the theoretical and measured $imd(2f_2 - f_1)$ may be made as seen in Figure 4.21. It should be noted that $[\sin(x)/x]^{-1}$ compensation was applied to the data and that at frequencies not much higher than 600 kHz or so, the IMD product would become buried in increased quantization noise with frequency. Even at frequencies below this, the inputs V_{i1} and V_{i2} had to be increased from 0 dBm to as high as 6 dBm just to be able to measure the harmonic above

Figure 4.21 Theoretical versus measured IMD (normalized) $imd(2f_2 - f_1)$ products

the quantization noise floor. Care was taken not to exceed this limit in an attempt not to cause the gain of the quantizer to decrease due to overload as discussed earlier.

The error bars in the figure are representative of the observed variance in the IMD products. At very high frequencies, a ± 6 dB variance is not uncommon where at low frequencies, well below the resonant peak, the variance decreases to ± 2 dB.

As may be seen, measurement falls within the bounds dictated by theory with average measurements being high. This is testimony to the fact that the harmonics experience band augmentation at frequencies near the resonant peak. Care must be exercised to ensure that these measurements are not upset by the existence of tonal behavior at higher frequencies that coin-

cides with the driving signals or IMD product. It is an easy task to shift the input signals slightly in frequency to assure a good measurement. This had to be done at least once.

Up to now, the spectral response of the IMD products has been investigated. It must be remembered that a decimation filter will attenuate high-frequency harmonics that are out of band and as a result, the frequency dependence of these transfer functions is not particularly important for driving signals that might exist out of band for $\Sigma\Delta$ modulators. It is for this reason no further steps were taken to investigate the bandlimiting of harmonics using this method and approach. Volterra series analysis, for example, provides a further multiplicative component that filters harmonics. Of particular relevance, with such an approach, are the third-order IMD products when f_1 and f_2 are near or beyond the resonant peak, where the IMD product experiences gain or attenuation. This is also true in second-order IMD products when $f_1 - f_2$ lies near or beyond the resonant peak.

Up to now, the IMD products that remain inband (i.e. mostly second-order IMD products) have centered around driven tones at the input to the $\Sigma\Delta$ modulator. In fact, the preceding study was a necessary precursor to the estimation of IMD products that are generated from the existence of high-frequency spurs. They appear inband during certain conditions, namely when the spurs are significant enough in amplitude and when the distance between spurs is less than the baseband frequency. As a result, the theoretical second-order IMD products determined from the approach used here is valid, again assuming that the spurs are close in frequency such that $f_1 - f_2$ is below the resonant peak frequency. The conditions under which the dynamic range is compromised may now be observed.

Consider now a single-tone applied to the input of the DISDM and the measured spectra that follow. For full-scale input signals, the measured spectrum of Figure 4.22a) shows no discernible, high-frequency tonal behavior. However, as the input is decreased in amplitude, a multitude of small spurs start to appear as seen in Figure 4.22b). These spurs are separated for the most part by a distance equal to f_i . However, they are often separated by a combination of frequencies including f_i and smaller frequencies. By now decreasing the input to -10 dBm, the spurs become fewer in number, but larger in amplitude as seen in Figure 4.22c), and even more so at an input of -20 dBm, as shown in Figure 4.22d). By continuing this downward trend, the input amplitude is reduced to -30 dBm. Only a few high-frequency spurs exist, spaced by f_i in this case as seen in Figure 4.22e). Note that noise-shaped "images" are found at

Figure 4.22a Measured spectrum of the DISDM for a full-scale input (+10 dBm)

Figure 4.22b The start of the formation of high-frequency spurs (0 dBm input)

Figure 4.22c Spurs are becoming fewer in number, but larger in amplitude (-10 dBm input).

Figure 4.22d Few tones left (-20 dBm input).

Figure 4.22e Formation of images near 100 kHz (-30 dBm input)

Figure 4.22f Nearly a single high-frequency spur exists near $f_s/2$ with large amplitude (-40 dBm input)

low frequency that exist at exactly twice the distance from DC compared to the distance from $f_s/2$ the high-frequency spurs exist at. Finally, at -40 dBm, nearly a solitary high-frequency spur exists at high amplitude, seen in Figure 4.22f). By decreasing the amplitude of the input signal, the side spurs may be observed to decrease in amplitude until they disappear entirely, below the quantization noise level.

It is these high-frequency effects that are worth investigating. This was one of the key reasons why the frequency dependence of the linearity coefficient $A_2(s)$ was investigated as opposed to the conventional non-frequency dependent analysis. Calculations of the inband products from these spurs will follow later. Before that, a brief explanation of how these tones arise is provided below.

The 1-bit DISDM, or any 1-bit, n^{th} -order oversampled A/D produces a PDM output of only ones and zeros whose average value at the output equals the input. If the input is zero (i.e. midway between the quantizer levels), then the output will oscillate with an equal number of ones and zeros, naturally.

Upon analyzing the manner in which DC signals modify the bit-stream, a digital "1" must appear every R number of clock cycles in order to keep the average amplitude of the bit-stream equal to the average value seen at the input of the modulator. Simply, $1/R$ is the DC offset expressed as a fraction of the total quantizer span.

$$R = 1 / \frac{\Delta/2 + |DC|}{\Delta} \quad \text{cycles} \quad \text{Eqn 4.56}$$

where $-\Delta/2 \leq DC \leq \Delta/2$, DC is with respect to 0 volts (i.e. mid-rail) and Δ is the span of the quantizer. The resulting bit-stream pattern has extra digital "1"s spaced R clock cycles apart thus having repetition. The periodicity T_R of this repetition is at multiples of the sampling period T_s which obeys

$$T_R = RT_s \quad \text{Eqn 4.57}$$

which may be translated to a frequency component

$$f_R = f_s/R \quad \text{and} \quad f_R = f_s \left(1 - \frac{1}{R}\right) \quad \text{Eqn 4.58}$$

which appears as a high-frequency spur shift equal to

$$\Delta f = \frac{f_s}{2} \left(\frac{2}{R} - 1 \right) \quad \text{Eqn 4.59}$$

from the case where some or no offset previously existed, usually near half the clock frequency since the DC offsets are typically not severe. For small magnitude AC sinusoidal signals applied to the input of the modulator, the spur decreases in magnitude slightly and begins to move about in frequency. This makes sense since the AC input, when oversampled, appears as a pseudo-DC signal.

Recently, an explanation of high-frequency spurs, albeit more qualitative than quantitative, was published with greater detail as regards the above effects [L193]. This reference discusses the existence of an "image" spur at low frequencies which embellishes upon the work of the Brandt et al [BWW91] as regards tones generated in baseband frequencies from DC inputs. Suffice it to say that as AC input amplitudes increase, the spurs decrease in amplitude while spreading even more in frequency due to more randomization in the bit-stream, which explains the high-frequency tonal behavior of figures Figure 4.22a)-Figure 4.22f).

Having witnessed the characteristic, high-frequency tonal behavior of the DISDM as a function of input signal amplitude, it is now timely to concentrate on the low-frequency IMD products that are produced in the baseband as a result of opamp nonlinearity. Under the right conditions, when the system is significantly nonlinear and when the amplitude of the high-frequency spurs become significant enough, a degradation of the dynamic range of the A/D may occur as a result of this mechanism.

Earlier, as seen in Figure 4.20, 10 kHz and 14 kHz driving signals were applied to the input of the modulator leading to the IMD products at 4 kHz and 6 kHz for fixed input amplitudes of 0 dBm. Instead of investigating the frequency response of the IMD products by sweeping the frequency of the driving signals, it is now opportune to simply explore the low-frequency distortion products that vary with the input signals' amplitude at fixed frequencies within the baseband. It will be seen, that for a range of input amplitudes, IMD products develop in the baseband due to the existence of the high-frequency spurs previously mentioned. This is because the spurs are large enough throughout some region of input amplitudes and are of such a formation as to be conducive to causing baseband products to appear. Once again, for convenience of measurement, the two driving signals are set to equal input amplitude.

Near DC (i.e. by letting $f=0$), the closed-loop linearity coefficients $A_2(j2\pi f=0)$ and $A_3(j2\pi f=0)$ may be determined. The normalized theoretical IMD products may be found as a function of input signal amplitude. The second- and third-order IMD products are plotted as shown in Figure 4.23 and Figure 4.24 respectively and are compared to the measured results.

Figure 4.23 Low-frequency IMD products $\text{imd}(f_1 - f_2)$ as a function of input amplitude. (Both driving signals are at the same amplitude)

As may be seen, the measured data matches quite well with theoretical expectations particularly at higher input amplitudes. There are a few exceptions however where the measured data departs from the theoretical.

At very high input amplitudes, the theoretical IMD products underestimate the measured products. This occurs as a result of an incomplete characterization of the opamp at the larger

Figure 4.24

Low-frequency IMD products $imd(2f_2 - f_1)$ as a function of input amplitude (Both driving signals are at the same amplitude).

signal magnitudes. This is a barrier which is imposed due to the limited usefulness of the polynomial approximation method which estimates the nonlinearity. Herein lies a drawback of using polynomial expansions for nonlinear analysis in that this method assumes that the system is still fairly linear. As a result, the method is usually only valid for limited signal magnitudes. In this case, an accurate polynomial fit was generated for the open-loop opamp for output signals up to roughly 0 dBm of signal swing. Attempts to extend the fit beyond this level through the use of higher-order terms resulted in a poor polynomial fit, particularly with poor estimates of the DC gain. It thus comes as no surprise that the measured IMD products are larger

than what theory predicts when the input to the modulator is in excess of approximately 3 dBm, as witnessed in Figure 4.23.

At reasonable input levels (less than 3 dBm), the linearity of the system is well characterized. As the input level decreases, the measured IMD products decrease either as the square or as the cube of the input amplitudes for the $imd(f_1 - f_2)$ and $imd(2f_2 - f_1)$ products respectively, as expected. However between roughly -10 dBm and -20 dBm, there is a region whereby the measured IMD products are greater than the theoretical predictions. This occurs in abundance due to the second-order intermodulation of the spurs. This is because, due to the lower input amplitudes, there are high-frequency spurs that are now of respectable amplitude which intermodulate down to baseband. These IMD products exist at the same 4 kHz and 6 kHz frequencies for the most part since the high frequency spurs that exist are spaced predominantly by 10 kHz and 14 kHz. Thus the 4 kHz $imd(f_1 - f_2)$ and 6 kHz $imd(f_1 - f_2)$ products (where f_1 and f_2 relate to high-frequency spurs) contaminate the baseband, degrading the dynamic range that much more. The manner in which this occurs may be studied either through simulation or by measurement.

Consider a specific example, where the driving signals in measurement are at -18 dBm as seen in Figure 4.25a). As may be seen, a strong 4 kHz component exists which cannot be generated from the conventional intermodulation of the driving signals. Consider the spectrum of the high-frequency spurs seen in Figure 4.25b) that was captured directly after the low-frequency spectrum of Figure 4.25a) was generated. These high-frequency spurs are directly responsible for the 4 kHz tone seen in Figure 4.25a). The IMD products that come about from the intermodulation of the low-frequency 10 kHz and 14 kHz driving signals are very stable in amplitude from clock cycle to clock cycle and thus from spectrum analyzer sweep to the next sweep. Note however that the IMD products from the high-frequency spurs change in magnitude from sweep to sweep. This is a result of the high-frequency spurs changing constantly from one clock cycle to the next coupled with the gain of the quantizer changing with time as discussed earlier.

To validate this entire supposition, a formal method of calculating the IMD products from the strongest spurs follows. The procedure in which this is accomplished is to unilaterally input-refer the high-frequency spurs as if they were a driving signal themselves and then use the closed-loop linearity coefficient, $A_2(s)$, to determine the resulting IMD products in the base-

Figure 4.25a

A spectrum of the bit-stream output of the DISDM. Inputs are -18dBm. IMD product at 4 kHz is a result of the intermodulation of high-frequency spurs near half the clock frequency.

Figure 4.25b

The high-frequency portion of the spectrum, near half the clock frequency. The inputs are the same as in a).

band. Two criticisms of this method come to mind. First, there is no way to ascertain the true spectrum of the spurs that are responsible for the 4 kHz IMD product. This method is at best an estimate since the spur's magnitude changes slightly from clock cycle to clock cycle. Secondly, to compound this, the effects of the gain of the quantizer on the transfer functions is indeterminate thus making this procedure an estimate. Nevertheless, an estimate of the upper and lower bounds may be made to help overcome this latter deficiency and also serves to validate the mechanisms at work here.

With reference to Figure 4.25b), the two strongest spurs are denoted by markers in the plot and are separated by 4 kHz. The strongest spur denotes the centerline of the range of spurs in frequency. This centerline spur, as discussed earlier, grows in amplitude as may be seen in Figure 4.25c) when the driving signals' amplitude is decreased. There are other smaller, albeit

Figure 4.25c A high-frequency portion of the spectrum, near half the clock frequency, typical of lower amplitude driving signals.

relatively strong spurs which are separated by 10 kHz and 14 kHz which when they intermodulate, generate products coincident upon the driving signals and thus is of no concern. Other

spurs are small enough so that they do not contribute significantly to the baseband when intermodulated, although there are small tones at 6 kHz, 8 kHz and 12 kHz barely above the quantization noise floor. It would be a difficult task to validate such marginal IMD products as the original spur's amplitudes are not well known since the high-frequency spurs are constantly changing. However, the 4 kHz tone may be estimated as it is quite significant in amplitude.

With reference to Figure 4.25b), the strongest spur has a magnitude equal to -9 dBm while the other spur is at -10 dBm. At these frequencies, taking $| \sin(\pi f) |^{-1}$ into account, these spurs in the sampled-data domain are approximately 3 dB higher. Hence, these spurs in reality exist at approximately 900 kHz with magnitudes equal to -6 dBm and -7 dBm respectively. These spurs may now be input-referred with the help of Figure 4.15. It must be remembered that the real sampled-data transfer function does not take the decreasing gain of the quantizer into account. On the other hand, the STF of the biquad equivalent is closer to what is measured and simulated and reflects the changing gain of the quantizer somewhat as may be seen in Figure 4.16. In reality, the true STF is rough and jagged in this part of the spectrum. It is thus prudent to input-refer the spurs with a tolerance which will lead to a bracket of possible IMD distortion product magnitudes.

The spurs may be input-referred according to the sampled-data STF and the equivalent biquad STF as a bracket of values. Thus the -6 dBm and -7 dBm spurs gain between extremes an extra 10.5 dB and an extra 15 dB respectively, from Figure 4.15. For the first case (+10.5 dBm gain), the -6 dBm and -7 dBm spurs when input referred to the input of the DISDM are 4.5 dBm and 3.5 dBm respectively at approximately 900 kHz, separated by 4 kHz. With reference to Figure 4.19, these spurs would intermodulate to produce a 4 kHz IMD product equal in magnitude to

$$\begin{aligned} \text{imd}(f_1, f_2) &= 67 + V_{f_1} + V_{f_2} \\ &= 67 + 4.5 + 3.5 \\ &= 59 \text{ dBm} \end{aligned} \quad \text{Eqn 4.66}$$

For the second case (+15 dBm gain), the -6 dBm and -7 dBm spurs have an equivalent 9 dBm and 8 dBm input signals at 900 kHz spaced by 4 kHz. The resulting IMD product at 4 kHz will equal

$$\begin{aligned}
 imd(f_1 - f_2) &= -67 + V_{i1} + V_{i2} \\
 &= -67 + 9 + 8 \\
 &= -50 \text{ dBm}
 \end{aligned}
 \tag{Eqn 4.61}$$

Thus a bound has been established within which the theoretical IMD product should fall. In this case, as there is a strong spur, the other smaller spurs at 4 kHz apart do not significantly contribute to the above estimate. This is because for every 1 dBm difference in both the spurs magnitudes means 2 dBm difference in the IMD product. Since all the other spurs are several dB less than the primary spurs used in the above calculation, their contributions are negligible. Also spurs that may be higher in frequency, which acquire more gain when input-referred, also see double that amount (in dB) in attenuation when the IMD products are calculated, and thus the same $imd(f_1 - f_2)$ levels result regardless of the frequency at which the spurs exist. This is because $A_1(s)$ has a rolloff rate of -12dB/octave while $A_2(s)$ has a nominal rolloff rate of -24 dB/octave at the frequencies of interest. The spurs at lower frequency for the most part are lower in amplitude and have spur spreads leading to IMD products of 10 kHz or 14 kHz primarily which are also of no interest in this example.

Comparing the theoretical bounds determined to the spectrum of Figure 4.25a), it may be seen that the measured IMD product seen at 4 kHz is nearly in the middle of the two bounds. Measured at -55.4 dBm, the theoretical estimates of Eqn 4.60 and Eqn 4.61 are quite close. This validates the mechanisms at work yielding fairly good estimates.

With reference to Figure 4.24, several occurrences of 6 kHz IMD products appeared above the quantization noise level. Inspection of the high-frequency spectra suggested that quite often this was a result of two strong tones spaced apart by 6 kHz. For example, if tones spaced 10 kHz, 14 kHz and 20 kHz (multiple of 10 kHz) apart exist, then the second-order IMD products will include a 4 kHz and 6 kHz product.

It should be noted that at input signals lower than the -20 dBm level, the spurs decrease in numbers but accompany an increase in amplitude in what appears to be the main spur. The location of this main spur, in frequency, represents the DC offset or quiescent point from which the AC signal moves about. The combination of the linearity of the system coupled with the spur's amplitudes typically result in no further degradation in the signal-to-distortion ratio (SDR). This is because the spurs intermodulate down to frequencies either coincident with the driving signals, or at other frequencies with insufficient power in the IMD product to rise

above the quantization noise floor. For example, consider Figure 4.25c), where the input driving signals have smaller amplitudes. As seen, there is a main central spur which grows in amplitude which may intermodulate with other spurs 10 kHz and 14 kHz apart from the main spur. Since the spur 4 kHz away from the main spur is so low in amplitude, the resulting IMD product would not appear above the quantization noise. This consequently causes no further degradation in the SDR of the system.

Furthermore, by performing a macromodel simulation, this mechanism may be further verified. Nonlinear opamps are used which incorporate the linearity coefficients found for the opamp in Chapter 3. The FFTs performed on the simulated bit-stream has not been windowed so that there is no spectral leakage and the quantization noise level is at the correct level, eliminating the need for scaling. Several simulation attempts is sometimes necessary to get a successful FFT that does not require window pre-processing. This difficulty is compounded by trying to get a good high-frequency spur pattern conducive to producing IMD products. Furthermore, coherent sampling is essential for unwindowed FFTs which is more difficult (i.e. time consuming) to do with two tones. Hence only a single tone to the input of the modulator is used in simulation. Consider the successful simulation of Figure 4.26a). Here the input is a single tone at -22 dBm which causes the high-frequency spurs to form as seen in Figure 4.26b) where there are only tones spaced by 10 kHz here and so 20 kHz and 30 kHz IMD products result. Once again, an estimate of the IMD products from these spurs may be made.

As may be seen, what might be considered a main spur near $f_s/2$ at -1 dBm intermodulates with a -12 dBm and -15 dBm spur 20 kHz and 30 kHz away, as seen in Figure 4.26b). Here, the nominal gain (from the continuous-time biquad method) were used to input refer the spurs. Thus from Figure 4.15 at nearly half the clock frequency results in the spurs acquiring approximately an extra 16 dB so that the spurs when input referred are now equivalently 15 dBm, 4 dBm and 1 dBm. The resulting theoretical IMD products are for the 20 kHz and 30 kHz product are then Figure 4.18

$$\begin{aligned}
 imd(f_1 - f_2) &= 70 + V_{c1} + V_{c2} \\
 &= 70 + 15 + 4 \\
 imd(20kHz) &= 51dBm
 \end{aligned}
 \tag{Eqn 4.62}$$

and

$$\text{imd}(f_1 - f_2) = -70 + 15 + 1$$

$$\text{imd}(30\text{kHz}) = -54\text{dBm}$$

Eqn 4.63

Comparing the theoretical result to Figure 4.26a), the simulated results are -51 dBm at 20 kHz and -55 dBm at 30 kHz respectively. There is good agreement between theory and simulation. Here, the low- and high-frequency spectrums are captured at the same time. However, in measurement, the low- and high-frequency spectrums cannot be acquired at precisely the same instant. Furthermore, the precise STF from measurement is not known due to variations and the decreasing nature of the gain of the quantizer.

4.4.4.4 Conclusions Regarding DISDM Nonlinearity from Opamps

This section of the chapter has dealt with the supposition that opamp nonlinearity manifests itself primarily in two ways. First, conventional intermodulation distortion of the driving signals was theorized and verified by measurement of the fabricated DISDM. In essence, the linearity of the first opamp may be input referred, which then goes through to the output of the DISDM according to the closed-loop gain or transfer function of the DISDM. To accommodate the nature of the quantizer gain, a continuous-time equivalent biquad circuit was used in place of the DISDM sampled-data STF which allowed the IMD products to be found with relative ease.

Secondly, an estimate of the IMD products that result from the intermodulation of high-frequency spurs was provided. The term estimate is best used here since at very high frequencies, where the spurs occur, the equivalent biquad STF is just an estimate of the sampled-data DISDM that reflects the apparent decrease in the quantizer gain at higher frequencies.

The example used here is sufficiently nonlinear and unusual in that the DC gain is quite low. Typically, higher DC gain opamps are required to ensure that the effects of leaky integration do not limit the available SNR. As the trend towards high-speed circuits is on the rise, an understanding of harmonic distortion propagation is essential since DC gain is typically traded-off for bandwidth. As DC gain suppresses the effects of nonlinearity, the consequences of such a trade-off may now be ascertained.

Figure 4.26a

FFT of simulation of the DISDM incorporating the fabricated nonlinear opamp. (Low-frequencies) The baseband products are a result of the intermodulation of high-frequency spurs shown below

Figure 4.26b

High-frequency portion of the FFT at frequencies near half the clock frequency

For completeness, the measured signal-to-distortion ratio SDR of this modulator may be found as a function of input amplitude, using the second- and third-order IMD products data from Figure 4.23 and Figure 4.24 respectively. Such a plot may be found in Figure 4.27. As

Figure 4.27 Signal-to-distortion plot of the fabricated DISDM.

may be seen, there are several distinctive regions. At very high input amplitude, near the full-scale level of 10 dBm, bit-stream saturation occurs and is not included here. Between the 0 dBm and 7.5 dBm approximately, the SDR decreases at a rate of just over the expected 2 dB per dB increase in input signal amplitude, characteristic of the relative third-order IMD products, or harmonics. From -7.5 dBm to 0 dBm approximately, the decrease in SDR occurs at a rate of 1 dB per dB increase in input signal amplitude, indicative of the relative second-order IMD products or harmonics as expected. From the -20 dBm to -7.5 dBm zone of inputs, the

SDR is as shown in Figure 4.27 due to the intermodulation of high-frequency spurs. Not until the input decreases to levels below -20 dBm does the measured signal-to-noise+distortion ratio (SNDR) depend solely on the quantization noise, which is augmented due to integrator leak in this case.

From a resolution design point of view, inasmuch as what harmonic levels are tolerable, it is an easy task to now determine what DC gain and linearity requirements are necessary from the opamp. From the $A_2(s)$ and $A_1(s)$ linearity coefficients, it is possible to predict the distortion levels that arise from signal harmonics or intermodulation distortion. Furthermore, by understanding the high-frequency nature of the quantization noise, and what range of input signals causes potentially offensive spurs to occur (found from simulation), it is possible to ensure that the intermodulation of said spurs does not degrade the dynamic range of the system.

4.4.5 Capacitor Nonlinearity

4.4.5.1 Introduction

Due to modern processing technology, the use of polysilicon-polysilicon capacitors makes this source of nonlinearity quite negligible compared to opamp nonlinearity. It is nevertheless prudent to theorize the effects of capacitor nonlinearity for if less linear capacitors (i.e. poly-substrate for better matching characteristics) and very high DC gain opamps are used then capacitor nonlinearity may then be the dominant source of distortion. Examination of the DISDM structure reveals that two mechanisms contribute to harmonic distortion from capacitors as will now be discussed.

First, there is the switched-capacitor R_1 (see Figure 4.14b) which contribute to the total amount of distortion at the output. R_4 and R_5 do not contribute since their inputs are binary in nature. Secondly, since the high loop gain of the system suppresses noise and sources of nonlinearity at or near the second integrator, the only capacitor of interest internal to the loop might be the integrating capacitor belonging to the first opamp.

The continuous-time model of the sampled-data DISDM is helpful here again in determining approximately how much harmonic distortion contributes to the output of the modulator from such nonlinearities.

4.4.5.2 Harmonic Distortion from the Switched Capacitor R_1 .

Built upon the foundation of a previous, simpler analysis [Ber88], the harmonic distortion from the capacitor C_{R1} (Figure 4.14a) may be evaluated as follows. This capacitor is singled out apart from the others since it is directly at the input while C_{R2} is well inside the loop. Disregarding the quantization noise, the transfer function of the DISDM may be written in differential form as

$$\Delta v_o = -\frac{1}{D(s)} \frac{C_{R1}}{C_{R4}} \Delta v_i \quad \text{Eqn 4.64}$$

where the denominator $D(s) = 1 + (sC_1R_2R_3)/R_1 + s^2C_1C_2R_2R_4$ is linearized (no voltage dependence). Assuming all components as ideal, the nonlinear capacitor generalized as $C_R(v)$ may be expressed as

$$C_R(v) = C_{R0}(1 + \alpha_1 v + \alpha_2 v^2) \quad \text{Eqn 4.65}$$

Where C_{R0} is the initial small-signal capacitance at a bias point and v is the voltage across the capacitor. Also α_1 and α_2 are the coefficients of capacitance that describe their nonlinearity. Substituting Eqn 4.65 into Eqn 4.64 yields

$$\Delta v_o = -\frac{1}{D(s)} \frac{C_{R1}}{C_{R4}} (1 + \alpha_1 v_i + \alpha_2 v_i^2) \Delta v_i \quad \text{Eqn 4.66}$$

Integrating

$$\int_0^{v_o} dv = -\frac{1}{D(s)} \frac{C_{R1}}{C_{R4}} \int_0^{v_i} \{1 + \alpha_1 V + \alpha_2 V^2\} dV \quad \text{Eqn 4.67}$$

results in

$$v_o = -\frac{1}{D(s)} \frac{C_{R1}}{C_{R4}} \left\{ v_i + \alpha_1 \frac{v_i^2}{2} + \alpha_2 \frac{v_i^3}{3} \right\} \quad \text{Eqn 4.68}$$

The nature of the nonlinear terms through expansion can be seen more clearly when considering two sinusoidal inputs. Letting $v_i(s) = V_{i1} \sin \omega_1 t + V_{i2} \sin \omega_2 t$ and substituting trigonometric identities for $\sin^2 \omega t$ and $\sin^3 \omega t$ yields the second- and third-order IMD products

$$imd(\omega_1 - \omega_2) = \frac{\alpha_1}{2} \left| \frac{C_{R1}/C_{R4}}{D(j\omega)} \right| V_{i1} V_{i2}, \quad \text{Eqn 4.69}$$

where it is assumed that $\omega = \omega_1 \approx \omega_2$ and that $\omega_1 - \omega_2$ lies in the flat, baseband frequencies. An estimate of (or the third-order) IMD products before filtration are

$$imd(2\omega_2 - \omega_1) \approx \frac{3}{4} \frac{\alpha_2}{3} \left| \frac{C_{R1}/C_{R4}}{D(j\omega)} \right| V_{i1} V_{i2}^2, \quad \text{Eqn 4.70}$$

once again where it is assumed that $\omega = \omega_1 \approx \omega_2$.

Due to proprietary constraints, the values of α_1 and α_2 cannot be disclosed. An arbitrary value of 30 ppm/V for α_1 and 30 ppm/V² for α_2 will be used. These reflect typical values common-place in good processes in the past. A plot of the second- and third-order IMD products may be seen in Figure 4.26a) and Figure 4.28b) respectively for normalized input levels. It is not hard to see from these figures that opamp nonlinearity predominates. With better, more modern processes where the values of α_1 and α_2 are less than those quoted here, the effects of capacitor nonlinearity from this source will decrease.

4.4.5.3 Harmonic Distortion from the Integrating Capacitor, C_1

As already stated, the high loop gain of the circuit suppresses noise and sources of nonlinearity beyond the first opamp. However, as loop gain drops with increasing frequency, the contribution to harmonic distortion from the integrating capacitor, C_1 (Figure 4.14a) is not necessarily all that negligible.

Here, analysis is once again simplified by using the continuous-time representation of the sampled-data DISDM of Figure 4.14b). Neglecting the quantization noise, the input goes through to the output according to Eqn 4.33 repeated below.

$$v_o(s) = \frac{R_4/R_1}{1 + sC_1 \frac{R_2 R_4}{R_1} + s^2 C_1 C_2 R_2 R_4} v_i(s) \quad \text{Eqn 4.71}$$

The nonlinear integrating capacitor C_1 may be expressed as

$$C_1 \approx C_{10} (1 + \alpha_1 v_{o1}(s) + \alpha_2 v_{o1}^2(s)) \quad \text{Eqn 4.72}$$

where

Figure 4.28a SCR capacitor nonlinearity. Second-order IMD product levels as a function of frequency (normalized for 0 dBm input levels) for a voltage coefficient of capacitance of $\alpha_1 = 30 \text{ ppm/v}$.

Figure 4.28b SCR capacitor nonlinearity. Third-order IMD product levels as a function of frequency (normalized for 0 dBm input levels) for a voltage coefficient of capacitance of $\alpha_2 = 30 \text{ ppm/v}^2$.

$$v_{o1}(s) = \frac{v_i(s) - v_o(s)}{sC_1R_1 - sC_1R_4} \quad \text{Eqn 4.73}$$

The equation that will ultimately lead to finding the distortion terms of interest is through the transfer function of Eqn 4.71 with Eqn 4.72 substituted into it.

This leads to

$$v_o(s) = \frac{-R_4/R_1}{1 + sC_{1o}\frac{R_2R_4}{R_1}(1 + \alpha_1v_{o1}(s) + \alpha_2v_{o1}^2(s)) + s^2C_{1o}C_2R_2R_4(1 + \alpha_1v_{o1}(s) + \alpha_2v_{o1}^2(s))} v_i(s) \quad \text{Eqn 4.74}$$

The result above contains the quantity v_{o1} . Substitution of Eqn 4.71 into Eqn 4.73 and allowing C_1 to now be approximated by a linear capacitor C_{1o} yields

$$v_{o1}(s) = \frac{v_i(s)}{sC_{1o}R_1} \left(\frac{1}{1 + sC_{1o}\frac{R_2R_4}{R_1} + s^2C_{1o}C_2R_2R_4} - 1 \right) \quad \text{Eqn 4.75}$$

The linearization of C_1 is necessary at this point so as to avoid recursive substitution. (This necessity has negligible consequences on the outcome.) All that remains is the substitution of Eqn 4.75 into Eqn 4.74. The result is the transfer function that contains the nonlinear capacitor C_1 . The result is omitted here due to its length, but the Mathematica listing may be seen in Appendix D. It contains the quantity $v_o(s)$ fully expanded (equation D.1). Furthermore, as $v_i(s)$ terms reside in the denominator of this equation, a series expansion is performed on D.1 yielding D.2 so that now $v_i(s)$ is in the numerator of the greater nonlinear equation. From previous sections it is once again easy to write out the second- and third-order IMD products. They are

$$\text{imd}(f_1 - f_2) = C_{o2}(j2\pi f)V_{i1}V_{i2} \quad \text{Eqn 4.76}$$

Where once again $f = f_1 \approx f_2$ and $f_1 - f_2$ is small enough to be valid. The pre-bandlimited, third-order IMD products are

$$\text{imd}(2f_2 - f_1) = \frac{3}{4}C_{o3}(j2\pi f)V_{i1}V_{i2}^2 \quad \text{Eqn 4.77}$$

where $f = f_1 + f_2$.

The values of C_{a2} and C_{a4} which make up the IMD products may be seen in Appendix D. These coefficients are given in D.4 and D.5 respectively.

Plots of $\text{imd}(f_1 - f_2)$ and $\text{imd}(2f_1 - f_2)$ may be seen in Figure 4.29a) and Figure 4.29b) respectively as a function of both input amplitude and frequency. It may be seen that this source of nonlinearity is far less at low frequencies than other sources of nonlinearity discussed so far. However at higher frequency particularly near the resonant peak, the effects of nonlinearity become a little more significant. This is an important point where the high-frequencies spurs that can be generated is concerned, for the second-order IMD products that are produced at the higher frequencies. It should be noted however that the harmonic levels are still very low and once again, when considering a more modern process, the coefficients of capacitance are far less leading to even less distortion. Conversely, if capacitors are excessively nonlinear, their effects may now be accounted for.

In concluding, it has been seen that opamp nonlinearity dominates over all other sources of nonlinearity. This statement remains true even when the opamp has considerably better linearity. However, if opamps that have high DC gain are used, then it is possible for the secondary sources of nonlinearity, from the switched-capacitors R_1 and R_2 as well as the integration capacitor C_1 , to play a more significant role in possibly limiting the dynamic range of the DISDM.

4.4.6 Additional Manifestations of Circuit Nonlinearity

4.4.6.1 Introduction

For completeness, it is constructive to consider secondary manifestations of nonlinearity within the DISDM on a simple qualitative level only. It was seen earlier that the position of high-frequency spurs depended upon the quiescent bias of the AC input signal coupled with any DC offset in the opamp. As these spurs typically exist near half the clock frequency, it is then conceivable that a second harmonic of this spur can be generated near the clock frequency. If this harmonic is close enough, then it will alias back down to baseband. It is also possible, however with less likelihood, that a spur near one-third the clock frequency may exist. Should it exist, it is possible that a third-order harmonic of it may be produced near f_c , which would

Nonlinearity in Oversampled A/Ds

Figure 4.28a

Second-order IMD levels seen at the output of the DISDM as a function of input amplitude and frequency due to nonlinear capacitor, C_1 , ($\alpha_1 = 30 \text{ ppm/V}$).

Figure 4.28b

Third-order IMD levels seen at the output of the DISDM as a function of input amplitudes and frequency due to nonlinear capacitor, C_1 , ($\alpha_1 = 30 \text{ ppm/V}$).

be available to then alias down to baseband. This discussion however will be confined to the possibility of spurs existing near $f_s/2$ as they are readily found at this location with significant amplitude.

Consider the simulation of the experimental, nonlinear modulator that produced the FFTs seen in Figures 2.5a) and b). These FFTs were pre-windowed resulting in highly underestimated amplitudes of the spectral components. Qualitatively, an analysis of these plots reveals that due to intermodulation of the high-frequency spurs shown in Figure 2.5b), the strongest IMD products should exist at 2.3 kHz, 12.3 kHz and 22.3 kHz all with nearly the same amplitude. This should be followed by products with less amplitude at 7.7 kHz, 27.7 kHz, 32.3 kHz and so on. Although negligible here, the 7.7 kHz component may be augmented due to the contribution of the spur closest to half the clock frequency, 3.85 kHz away from $f_s/2$. It is expected that this spur produces a second harmonic twice this distance away from $f_s/2$ at $f_s - 7.7$ kHz. This harmonic then aliases down to baseband, modifying the power as regards the spectral component at 7.7 kHz. This mechanism also modifies the power associated with spectral components at 12.3 kHz, 27.7 kHz, 32.3 kHz and so on. The relative contribution of these aliased harmonics to existing IMD products is unknown as the phase and correlation between these contributors is in question. Such a study is beyond the scope of this thesis. Where individual distortion contributions are concerned, the quantitative method described earlier may be used to evaluate such second-order harmonics using the $A_2(\omega)$ coefficient (based on Figure 4.17), including any necessary bandlimiting filtration, after input-referring the spurs.

Although the above mechanism demonstrates how aliased harmonics may degrade the SNR at baseband frequencies, it must be realized that in order for these spurs to exist immediately adjacent to $f_s/2$, the first opamp (in particular) must have no DC offset and the quiescent point about which the input signal swings must also be zero. Alternatively, the quiescent point may cancel the effect of other DC offsets so that the spurs are no further than half a baseband away from $f_s/2$, as discussed previously. Such a condition rarely occurs, as witnessed in measurement, except in the ideal environment offered by simulations.

For completeness, it is worth noting that quantization noise throughout the spectrum may intermodulate with itself to cause an increase in the quantization noise within the baseband. Naturally, the high-frequency portion of the quantization noise would contribute perhaps a portion of what might be seen in the baseband. An added dimension of this argument is that

this quantization noise spectrum when input-referred also has a second- and third-harmonic spectrum. If the harmonics of noise are significant near multiples of the clock frequency, it too is available to be aliased which contributes to the overall baseband noise floor. However, since low DC gain typically accompanies the more nonlinear opamps, the effect of curtailing the noise-shaped spectrum near DC from the effects of integrator leakage dominates this source of quantization noise enhancement from nonlinearity. Where such an effect may become significant is in the use of integrators that have finite gain correction schemes, causing a significant improvement in the quantization noise spectra from integrator leakage.

4.5 Summary and Conclusions

The focus of this chapter has been on identifying and analyzing nonlinearity in $\Sigma\Delta$ modulators. It has been shown through simulation and measurement that in-band tones may be produced from the intermodulation of high-frequency spectra. The manner in which these spurs are produced was shown to relate to the limit-cycle behavior of $\Sigma\Delta$ modulators in general. It was the intention of this chapter to show that these tones could be predicted, given any high-frequency spur pattern.

In order to obtain a solid foundation with which nonlinearity analysis could proceed, it was necessary to expand the present knowledge of the STF with emphasis at high frequencies. Greater understanding and better accuracy in the STF was procured by investigating the gain of the quantizer, particularly at higher frequencies. By studying the nature of the gain κ , the STF throughout the entire spectrum was approximated. Since κ is just a time-averaged quantity, it varies slightly from cycle to cycle. At low frequencies, the STF remains smooth regardless of fluctuations in the gain κ . At high frequencies, the STF's immunity to changes in κ decreases. Furthermore, at higher frequency, the gain of the quantizer visibly increases in variance and its average value decreases. This was the necessary link which explained the high-frequency roll-off seen in the STF in both simulation and measurement.

By considering finite gain in opamps that make up the integrators in sampled-data oversampled A/Ds, an increase in the quantization noise at low frequencies may be theorized and compared to measurement. Limited treatments have been theorized in the past. However, in this thesis, the estimate is further refined by virtue of having included a characterized value for the

gain K in the calculation. The theoretical and measured values for the in-band quantization noise due to this effect are in fairly good agreement.

Having established a foundation and expanded the understanding of the STF of the DISDM, nonlinear analysis proceeded. Due to the difficulty in which nonlinearity would have to be handled in the z -domain as a result of the varying and decreasing average value of K at high frequency, it was prudent to model the DISDM as a continuous-time, equivalent biquad filter as a more practical alternative. As mentioned earlier, this is because the constant roll-off of the equivalent biquad matches the roll-off found in the simulated and measured STF. The manner in which the STF was mapped is as follows.

Pragmatically, the DISDM has a delay in the loop as well as a gain element associated with the quantizer. Hence, the equivalent biquad filter does not map directly by using switched-capacitor resistor equivalents, $R = 1/f_s C$. Rather, the equivalent biquad filter allows the z -transform to be biquadratically fitted through the use of a simple tuning strategy, easily employed by determining the natural frequency, DC gain and Q from the z -domain STF. From that, the effect of opamp and capacitor nonlinearity at all frequencies throughout the spectrum was theorized. The frequency dependence of the gain K was taken into account by modelling the DISDM as an equivalent biquad filter. From this, the closed-loop linearity coefficients as a function of frequency are found.

A large effort was channeled into considering the effects of opamp nonlinearity, as it is typically the dominant source over all other sources of nonlinearity. In order to validate the theoretical effects of nonlinearity in DISDMs (and oversampled A/Ds in general) intermodulation distortion tests were performed having applied multiple tones to the input of the coder across a broad range of frequencies. As expected, there is good agreement between theory and measurement. In fact, this exercise validated the following method which allowed a prediction of the intermodulation distortion product magnitudes that take place from high-frequency spurs.

By input referring the high-frequency spurs, an estimate of the distortion products as a result of these high-frequency "signals" may be made. Validation of this mechanism was indicated by a good agreement between the estimated and measured distortion products and was further supported by simulation.

On a previous point, the nature of sigma-delta modulators is such as to produce short- and long-term periodicities that lead to highly correlated (non-random) spectra or spurs at high frequency, typically near half the clock frequency, as a result of the limit-cycle behavior implicit to the operation of the single-bit quantizer class of oversampled A/Ds. These spurs are usually equally spaced by distances equal to the input signals' frequency as well sometimes at other frequency components. It was seen that these spurs are conducive to the intermodulation process under a limited range of input amplitudes where the spurs become significant enough in magnitude.

Aliased harmonics due to even-order nonlinearity terms may also, under certain conditions, contaminate the baseband. Such is the case when the high-frequency spurs are close to half the clock frequency as set by the AC signal's DC bias from signal DC offset. When baseband tones appear as a result of aliased harmonics, a simple solution is to simply apply a DC bias to the input signal. This will effectively place the aliased tones out of the baseband, filtered out by subsequent decimation.

In concluding, it is now possible to assess what degradation in SNR may be expected from nonlinear elements within the DISDM. The dominant source of nonlinearity typically implicit in switched-capacitor, opamp-based filters comes from opamps, which may now be characterized and the DISDM harmonic levels predicted. Conversely, the harmonic levels in a DISDM may be kept low by designing the opamp with a set of specifications in terms of the ratios of opamp linearity coefficients a_2/a_1^3 and a_3/a_1^4 . As a result, the best solution is to keep the DC gain of the opamp high so as to suppress the nonlinearity. Thus, in high-speed circuits where an inevitable trade off takes place between bandwidth and DC gain, judicious design is essential.

This work has been useful in understanding how circuit nonlinearity manifests itself in oversampled A/Ds through the conventional intermodulation of multiple input tones and of high-frequency spurs. It also provides a basis from which to work in approaching nonlinearity in a novel, OTA-based high-frequency continuous-time $\Sigma\Delta$ modulator in the next chapter.

The Design of Wideband, Continuous-Time Oversampled A/Ds Including Noise and Nonlinearity

5.1 Introduction

In the past, the use of oversampled A/Ds has been confined from low to moderate conversion bandwidths primarily due to the limited bandwidth of opamps in monolithic CMOS implementations. With BiCMOS as a viable technology, the bandwidth of opamps has risen markedly allowing for a greater clock speed and bandwidth through which quantization noise in oversampled A/Ds may be distributed. However, oversampled A/D designs for high-speed applications have been for the most part nonexistent, and as yet relatively unexploited. High-speed A/D conversion has classically been performed using “flash” A/Ds which require large area and considerable power to operate. The significantly smaller area requirements and power consumption that an oversampled A/D would have to offer makes such a device attractive for high-speed monolithic implementations.

In general, switched-capacitor circuits and filters have led to accurate realizations due to the high-precision capacitor ratios available in modern processes, with relatively small area consumption. In the past, continuous-time circuits needed substantial areas to accommodate

large, low-resistivity diffusion resistors. In more modern processes, the availability of polysilicon resistors is of limited usefulness due to their relatively large tolerances and their high temperature coefficient of resistance. As an alternative when precision resistors are required, operational transconductance amplifiers (OTAs) may be employed since they are capable of being tuned [Ple86]. A capacitor placed at the output of a conventional OTA forms a continuous-time integrator. The transconductance of the amplifier replaces the resistor that would normally have been used in the opamp-based integrator.

Sampled-data circuits have drawbacks that include the effects of aliasing, clock-feedthrough noise as well as a need for switches and two- to four-phase clocks to drive them. Furthermore, sampled-data circuits must have opamps and switches that settle within a clock cycle. Moreover, sampled-data integrators require their bandwidth to be a fraction of the opamp's UGBW for settling considerations.

Continuous-time circuits have an inherent advantage over sampled-data circuits as anti-aliasing filters are not required. The potential for higher operational speed may be exploited as there is no longer any concern about signals having to settle within a clock period. The use of opamps in continuous-time circuits (i.e. filters) has drawbacks however. Distortion worsens as frequencies go beyond the dominant pole of the opamp since loop gain is reduced at these higher frequencies. The OTA does not suffer from this effect, although the OTA by nature is already quite nonlinear. Furthermore, the bandwidth of an OTA-based integrator is intrinsically the same as the UGBW of the OTA immediately presenting itself for wideband applications. However, the advantage of high speed gained from the use of OTAs comes at a loss of linearity—a concern that will be addressed later on.

This chapter is devoted to the design of a novel continuous-time modulator which veers away from conventional opamp-based circuits and focuses on transconductor-based circuits. The transconductor or OTA used in these continuous-time circuits addresses this linearity issue through the use of a Gilbert gain cell, at the expense of increased noise as will be discovered. The integrator used was novel at the time of design in that the act of integration is performed internal to the OTA through the use of a pole-splitting output stage. In this way, the impedance of subsequent circuit elements will not cause charge to leak off the integration capacitor. High DC gain in the OTA is easily achieved and parasitics are less of a concern through this technique. The use of this output stage is of particular interest for transconductor-based filters in

that a flat phase response can be maintained for a relatively wide range of frequencies. The OTA has a second differential input pair for summing in feedback, making noise analysis more difficult than conventional, well understood opamp-based circuits.

To date, there have been continuous-time and mixed continuous-time/sampled-data implementations of $\Sigma\Delta$ modulators reported within the last few years [DKS+90], [CST91], [LLF+91], [DPM92], [KHE⁺86]. All of these boast no or no large speed improvements over conventional sampled-data modulators and all but two ([CST91] & [KHE⁺86]) used opamp-based integrators. The closest $\Sigma\Delta$ modulator (of the low-pass loop filter type) that approaches the potential conversion rates comparable with the architectures that will be discussed here, boasts a 1 MHz baseband, clocks at 50 MHz, and was a third-order type [BW91]. A novel first-order continuous-time $\Sigma\Delta$ that clocks in excess of three times that was fabricated, tested successfully and is described in this chapter.

The motivation for this work stems from the desire to fabricate a novel $g_m - C$ based, wide bandwidth oversampled A/D that boasts conversion speeds an order of magnitude greater than what was present the time these circuits went to fabrication. The potential applications of such a wideband device could encompass video signal processing as well as high-speed telephony applications such as Video-on-Demand and Interactive Multimedia applications.

The approach taken here is to integrate feedback current internal to the amplifier, at the second stage of the OTA and through the use of BJTs allow operation at greater bandwidth making it superior to [CST91]. Through the use of an OTA-based integrator scheme, a prototype continuous-time modulator is designed to operate at frequencies an order of magnitude greater than what is typically common-place. To accommodate, the comparator described in Chapter 3 is stripped to the bare ECL-component structure, allowing for the greater speed requirement.

This chapter will start by considering an analogy between the sampled-data and continuous-time (clocked) $\Sigma\Delta$ modulators. Commensurate to that will be the design of the continuous-time modulator at the system level. Also presented are the first- and second-order $g_m - C$ low-pass filters. The OTA that makes up the filters and oversampled A/Ds is presented along with a description of the Gilbert gain cell.

In keeping with a major theme of this thesis, noise analysis of the OTA is performed. This is extended to the filters and the oversampled A/Ds. Measured results are compared with theory.

It will be found however, that quantization noise and the effects of leaky integration dominates electronic noise in the first-order oversampled A/D tested and these effects are quantified separately.

Another focus of this thesis has been the study of distortion in oversampled A/Ds. A look at how nonlinearity proliferates in $g_m - C$ filters and the oversampled A/Ds presented here is considerably different than those of the opamp-based structures. A simple theory is presented that avoids the mathematical complexities from highly complicated and obscure treatments. The amount of error from this approach is not particularly excessive which validates this treatment.

It should be noted that since there is equivalence between the sampled-data and continuous-time circuit, the stability analysis discussed in Chapter 4 is assumed valid for these structures as well and is not repeated. This is because the continuous-time oversampled A/Ds are clocked.

Among the circuits designed and fabricated were a stand-alone OTA integrator, a low-pass filter and a prototype first-order continuous-time $\Sigma\Delta$ modulator. A photomicrograph of these circuits are shown in Fig 5.1. Measurements were most often taken single-ended. A biquad circuit was also designed and tested, however, the second-order continuous-time DISDM that followed had fabrication problems and could not be tested or trouble-shot within the time frame allotted.

5.2 *Analogy between Sampled-Data and Continuous-Time Sigma-Delta Modulators*

5.2.1 *Fundamental Comparison in Operation*

It is now timely to consider the continuous-time equivalent of the sampled data $\Sigma\Delta$ modulator. The difference between the two lies in the use of continuous-time rather than sampled data integrators. Without having to repeat the entire process of simulating the continuous time mod

Figure 5.1 Photomicrograph of continuous-time circuits fabricated in 0.8 micron BiCMOS

ulator, it may be shown that there exists an analogy between the two which shows equivalence in operation.

The operation of the sampled-data integrator consists of rapidly accumulating charge increments derived from the input voltage such that the output is equal to that of a continuous-time integrator at the end of each clock cycle as pictorially described in Figure 5.2a)-Figure 5.2c). The operation of the integrators are governed by the equations below. The sampled-data integrator exhibits a time-domain behavior according to

Figure 5.2

a) Sampled-data integrator operation. b) Continuous time integrator operation. c) Output from both integrators are equivalent at multiples of n in time

$$V_{O,n} - V_{O,p} = \alpha V_{I,n} \quad \text{Eqn 5.1}$$

where $\alpha = C_R/C_I$ in Figure 5.2a) and the subscripts n (now) and p (previous) relate to the clock phase. It may also be seen that the continuous-time integrator also accumulates according to

$$V_{O,n} = \frac{1}{RC_I} \int V_{I,n} dt + V_{O,p} \quad \text{Eqn 5.2}$$

The above two equations are, for all intents and purposes, equivalent. By using a continuous time integrator, there are many advantages [UCI.90] over the sampled-data equivalent, such as the elimination of clock feedthrough, charge injection and aliasing. Furthermore, the ability to drastically increase the speed of the modulator exists by changing from opamp based to operational transconductance amplifier (OTA-based) integrators, as discussed in the introduction.

In conventional opamp-based integrators, the UGBW of the opamp must exceed that of the integrator, since high loop gain is required to keep the virtual ground operation intact. In the OTA-based integrator, the OTA and the integrator have the same UGBW. This translates to faster circuit operation for any given technology. As the output of the $\Sigma\Delta$ modulator must be synchronous, the modulator must be clocked at the quantizer. Now, a first-order $\Sigma\Delta$ clocked continuous-time circuit may be modeled as shown Figure 5.3b), which may be compared to the original sampled-data equivalent of Figure 5.3a). Note that the τ^{-1} describing the delay of

Figure 5.3a System-level description of the sampled-data modulator.

Figure 5.3b System-level description of the continuous-time modulator.

Figure 5.3c System-level description of the second-order continuous-time modulator.

the quantizer in the sampled-data version is replaced by the transfer function of a zero-order sample-and-hold in the continuous-time version. This is necessary in order to accurately model the delay of the quantizer producing a pulse of T seconds in duration. A second-order continuous-time modulator may be modelled as shown in Figure 5.3c) for completeness.

Since the time-domain behavior of the two are for all practical purposes identical, system level simulations for continuous-time oversampled A/Ds may be carried out using the discrete time simulator already developed for the sampled-data modulator.

There is one distinguishing advantage from using a continuous-time $\Sigma\Delta$ modulator. Since the quantizer is clocked, it may be considered a sampler. As such, the aliasing mechanism is in place. However, since the integrator is continuous-time in nature, the loop filter within the modulator acts as an anti-aliasing filter. This will become clear later.

5.3 The Design of the Continuous-Time Circuits

5.3.1 Design of the First-Order, Continuous-Time Sigma-Delta Modulator and Circuit Equivalence

This section presents a simple equivalence transformation used to help design the continuous time modulators from known z -domain transfer functions. Modelling the first-order $\Sigma\Delta$ modulator in the same fashion as in previous chapters, a z -transform may be found from Figure 5.3a) which leads to a signal and noise transfer function (STF and NTF).

$$STF = \frac{K\alpha_1}{1 - (1 - K\alpha_2)z^{-1}} \quad \text{Eqn 5.3}$$

$$NTF = \frac{(1 - z^{-1})}{1 - (1 - K\alpha_2)z^{-1}} \quad \text{Eqn 5.4}$$

A continuation of the analogy between the sampled-data and continuous-time integrators will lead to the general design of the modulator. The integrators have been generalized here at the system level, and will be discussed in greater detail later.

In order to proceed, consider a sampled-data integrator having a transfer function (z-transform)

$$H(z) = \frac{V_o(z)}{V_i(z)} = \frac{\alpha}{1 - z^{-1}} \quad \text{Eqn 5.5}$$

whose magnitude is

$$|H(z)| = \frac{\alpha}{2 \sin(\frac{\pi f}{f_s})} \quad \text{Eqn 5.6}$$

This gives a UGBW of

$$f_{UGBW} = \frac{f_s}{\pi} \sin^{-1}\left(\frac{\alpha}{2}\right) \quad \text{Eqn 5.7}$$

The integrator's time-domain behavior is given by

$$V_{o,n} - V_{o,p} = \alpha V_{i,n} \quad \text{Eqn 5.8}$$

in a single clock cycle.

Now, consider the transfer function of the continuous-time, OTA-based integrator (s-domain)

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{g_m}{sC} \quad \text{Eqn 5.9}$$

which has a UGBW of

$$f_{UGBW} = \frac{g_m}{2\pi C} \quad \text{Eqn 5.10}$$

Looking back to Eqn 5.5 for a moment it may easily be shown that the sampled-data integrator's transfer function from DC to $f_s/2$ is mirrored from $f_s/2$ to f_s , which, of course, replicates about multiples of the clock frequency. The transfer function of the OTA integrator contains a straight $1/s$ term implying that clocked continuous-time circuits have excellent, built-in anti-aliasing properties.

The time-domain behavior of the continuous-time integrator is

$$V_{i,n}(t) = \frac{g_m}{C} \int_0^{\Delta t} V_i(t) dt + V_{i,n}(t - \Delta t) \quad \text{Eqn 5.11}$$

Compare Eqn 5.8 and Eqn 5.11. When Δt is the period of the clock used in the context of the $\Sigma\Delta$ modulator, the two equations are equal and valid at the end of Δt . The difference in operation may be seen pictorially in Figure 5.2c). In continuous-time, the integrator ramps to some final value as opposed to pseudo-squarewave integrations to completion in the sampled data domain. The final value at the end of the clock phase are identical. Equating Eqn 5.8 and Eqn 5.11 and simplifying, yields

$$\alpha V_{i,n} = \frac{g_m}{C} \int_0^{\Delta t} V_i(t) dt \quad \text{Eqn 5.12}$$

Since the inputs at $V_i(t)$ are equal to $V_{i,n}$ at any discrete instant in time, then

$$\alpha V_{i,n} = \frac{g_m}{C} V_{i,n} \Delta t \quad \text{Eqn 5.13}$$

Solving for α ,

$$\alpha = \frac{g_m}{C} \Delta t \quad \text{Eqn 5.14}$$

If $\Delta t = T$ (the clock period) then

$$\alpha = \frac{g_m}{C} T \quad \text{Eqn 5.15}$$

which is the sampled-data to continuous-time coefficient transformation. By putting this into a more general form and rearranging, $\alpha = \omega_u T$ where ω_u represents the integrators bandwidth. Eqn 5.15 agrees with [CST91]. This is a publication on a low frequency, continuous time modulator that came out subsequent to the design and original fabrication submission of the following design. (It should be noted that recent work by Shoaer [Sho95] has shown a better mapping method that utilizes pulse-invariant transformations between sampled data continuous-time $\Sigma\Delta$ modulators.)

In the sampled-data modulator, the time-domain representation at the output of the integrator is

$$V_{out,n} = V_{out,p} - \alpha_1 V_{in,n} - \alpha_2 V_{REF,p} \quad \text{Eqn 5.16}$$

where V_{REF} refers to the reference voltage that typically comes from a DAC. By making use of the sampled-data to continuous-time coefficient transformation, this time-domain equation may be approximated, when $T_s \ll T_c$, as

$$V_{out}(t) = V_{out}(t - T) + \frac{g_{m1}}{C} T V_{in}(t) - \frac{g_{m2}}{C} T V_{REF}(t - T) \quad \text{Eqn 5.17}$$

Intervening for a moment, a more rigorous description of the integrator's output may be found at this point to demonstrate the inherent anti-aliasing properties of the modulator mentioned earlier.

$$V_{out}(t) = V_{out}(t - T) + \frac{g_{m1}}{C} \int_{t-T}^t V_{in}(t) dt - \frac{g_{m2}}{C} T V_{REF}(t - T) \quad \text{Eqn 5.18}$$

The integral in the above equation implies $1/s$ frequency characteristics. Thus, anti-aliasing takes place inherently in this continuous-time modulator, the amount of which depends on the ratio of clock frequency to the unity gain bandwidth of the integrator (i.e. α).

A hypothetical single-ended circuit that uses doubly-differential input pairs in the OTA for the summing operation may be seen in Figure 5.4. If $g_{m1} = g_{m2}$ and the reference voltages V_{REF+} and V_{REF-} are set to 1 volt and -1 volt respectively, then the architecture is degenerate and similar (in a first-order sense) to what was used in the previous chapter if $\alpha_1 = \alpha_2 = 1$.

$$\alpha = 1 - \frac{g_m T}{C} \quad \text{Eqn 5.19}$$

As will be discussed, the OTA integrators used here are designed to have a UGBW of 72.4 MHz (i.e. 36.2 MHz taken at the output single-ended). By rearranging the above equation and solving for $1/T$, the required clock frequency may be found

$$f_{CLK} = \frac{1}{T} = \frac{g_m}{C} = \frac{2\pi 36.2 \times 10^6}{227 \text{MHz}} \quad \text{Eqn 5.20}$$

Figure 5.4 Hypothetical single-ended continuous-time modulator implementation

Immediately, it may be seen that aliasing is reduced due to the high clock rate coupled with the bandlimiting nature of the integrator which precedes the quantizer.

The hypothetical circuit of Figure 5.4 requires the use of a switch and reference voltages. The problems associated with switches such as clock feedthrough and charge dumping needs to be contended with. Not only is the switch-free advantages typical of continuous-time circuits gone, but it would be a difficult task to produce a switch capable of switching at 227 MHz with sufficient settling.

In the interest of eliminating the switch operated by the quantizer, the reference voltages must be eliminated. This is easily accomplished by allowing the high or low output of the quantizer to directly drive the feedback differential pairs embedded in the OTA. The quantizer's output acts to switch slew rate limited current either positively or negatively into the integration capacitor. As the slew rates are constant from cycle to cycle and one of the transistors in the long-tailed pair is always turned on hard, immunity from noise is greatly enhanced. For example, a 1V excursion in time T requires a slew rate

$$SR = \frac{\Delta V}{\Delta t} = \frac{1}{1 + (2\pi \cdot 36.2 \times 10^3)} = 2\pi f_{c,na} = 1.27 \mu S \quad \text{Eqn 5.13}$$

Figure 5.5 Fabricated, fully-differential implementation of the first-order modulator. (Note the integration capacitor is internal to the OTA and g_{m1} is in brackets to remind the reader that this differential pair is used for current steering and has no small-signal properties).

The current that must flow from a branch in a differential pair into a 2pF capacitor (the size used in implementation) to provide feedback is then

$$\begin{aligned} I &= SR \times C \\ &= (227 \times 10^6) (2 \times 10^{-12}) \\ &= 454 \mu A \end{aligned} \quad \text{Eqn 5.22}$$

A fully-differential implementation of this modulator may be shown in Figure 5.5. As will be discussed, the UGBW of the OTA is set by the use of emitter degeneration in one of two differential input pairs for the feedforward signal. The remaining differential pair is kept undegenerated for ease of current steering in the feedback path. The use of the Gilbert gain cell configuration allows the effective transconductance to be tuned by changing bias currents off chip, if deemed necessary or simply to adjust current levels to satisfy any change in slew-rate requirements.

5.3.2 Resolution of Continuous-Time Sigma-Delta Modulators

According to Candy [Can85], the theoretical resolution of a conventional sampled-data modulator depends on the clock speed and the signal bandwidth. In reality, bandwidth expectations

must often be reduced due to thermal noise so as to meet a required resolution. In sampled-data modulators, the clock is often dictated by the slew rate of the opamp and its settling behavior. In the clocked continuous-time modulator presented here, the limitations on the clock rate are no longer valid as there is no settling error or slew rate limitation with which to contend. Now, the resolution depends upon the signal bandwidth and the unity-gain bandwidth of the OTA. However, other nonideal circuit effects may dictate what the final bandwidth of the modulator will be and its resolution. According to [Can85], the resolution of the first order modulator may be theoretically found from the net integrated quantization noise within the baseband, f_o

$$N_{mo}(f_o) = \frac{e_o \pi}{\sqrt{3}} \left(\frac{2f_o}{f_s} \right)^{3/2} \\ = \frac{e_o \pi}{\sqrt{3}} \left(\frac{f_o}{\pi f_{UGBW}} \right)^{3/2} \quad \text{Eqn 5.23}$$

since $f_s = 2\pi f_{UGBW}$ for $\alpha = 1$. Similarly, for a second-order modulator

$$N_{mo}(f_o) = \frac{e_o \pi}{\sqrt{5}} \left(\frac{2f_o}{f_s} \right)^{5/2} \\ = \frac{0.58\pi}{\sqrt{5}} \left(\frac{f_o}{\pi f_{UGBW}} \right)^{5/2} \quad \text{Eqn 5.24}$$

since $f_s = 2\pi f_{UGBW}$ again. Thermal noise, nonlinearity and the effects of leaky integration however ultimately dictate the resolution of the coder.

5.3.3 First-Order Low-Pass Filter

In general, embedded within oversampled A/Ds is the quantizer and a loop filter of the low pass type, in this case. This first-order low-pass $g_m - C$ filter, seen in Figure 5.6a) is analogous to the active RC filter seen in Figure 5.6b) where the resistors are equal to the inverse of the differential pair's transconductance. The loop filter is fabricated separately and is useful for experimentation as regards noise and nonlinearity since, for the most part, it relates to the modulator. This exercise is necessary to validate a methodology for determining noise and

Figure 5.6 a) The first-order low-pass filter, operated in single-ended mode (internal capacitor) b) Active RC equivalent filter.

nonlinearity in the more complex, doubly-differential OTA-based circuits. Since the quantizer is removed, both differential pairs may be degenerated to keep the closed-loop transfer function the same as the modulator's. For example, the transfer function of this filter is

$$\frac{v_o(s)}{v_i(s)} = \frac{g_{m1}/g_{m2}}{1 + sC/g_{m2}} \quad \text{Eqn 5.25}$$

which may be approximated to $\frac{v_o}{v_i} \approx -g_{m1}/g_{m2}$ at frequencies below the UGBW of the integrator (or OTA). Analysis will prove fruitful, the effects of degeneration compensated for and applied to the modulator leading to a comprehensive method for determining the noise and nonlinearity through to the output of the modulator.

This course of action should come as no surprise since it was seen in the last chapter, that noise and nonlinearity goes through to the output according to the closed-loop gain of the loop filter and that the only effect of the quantizer was to introduce a delay, which caused a slight change in the transfer function (noticeable only at high frequencies) and an added gain element. Since the transfer functions of the loop filter and the $\Sigma\Delta$ modulator are the same at low frequencies, certain parts of this study will be confined to the baseband.

5.3.4 The Design of the Second-Order, Continuous-Time DISDM

Although not tested, due to fabrication problems, the design of the continuous-time DISDM is a logical extension of the first-order case. In the sampled-data DISDM, the time-domain representation at the output of the integrators is

$$V_{o1,n} - V_{o1,p} = \alpha_1 V_{i,n} + \alpha_4 V_{K11,p} \quad \text{Eqn 5.26}$$

$$V_{o2,n} - V_{o2,p} = \alpha_2 V_{o1,n} - \alpha_3 V_{K11,p} \quad \text{Eqn 5.27}$$

The use of the sampled-data to continuous-time coefficient transformation allows these time domain equations to be approximated (assuming $f_s \gg f_s$) as was done in the first order case. For the degenerate case modulator all the coefficients are set such that

$$\frac{g_m}{C} T = \alpha = 1 \quad \text{Eqn 5.28}$$

Once again, in the interest of eliminating the switch operated by the quantizer, the reference voltages must be eliminated. This is easily accomplished by allowing the high or low output of the quantizer to directly drive the feedback differential pairs embedded in the OTA in the same manner as described for the first-order case.

A fully-differential continuous-time DISDM is shown in Figure 5.7. The UGBW of the OTA is primarily set by the emitter degeneration in the feedforward differential pairs, as discussed before with the first-order case while the feedback differential pairs remain undegenerated.

5.3.5 The Biquad Filter (Second-Order Low-Pass Filter)

As was done for the first-order continuous-time $\Sigma\Delta$ modulator, the loop filter was fabricated as a separate circuit. The motivation for doing this is the same as was for the first order modula

Figure 5.7

Fully-differential continuous time DISDM (Once again the capacitors are internal to the OTAs, and g_{m1} and g_{m4} are in brackets to identify the differential pair, but large signal current steering occurs here)

tor case. Once again, all of the differential input pairs are emitter degenerated to keep the low-frequency gain the same as the continuous-time DISDM. This may be seen from the transfer function of the biquad, derived from Figure 5.8a).

Figure 5.8 The fabricated biquad shown as operating in both the a) single- and b) double-ended mode. (Capacitors are internal to the OTA).

$$\frac{v_o(s)}{v_i(s)} = \frac{g_{m1} g_{m2} g_{m4}}{s^2 + s \frac{g_{m3}}{C_2} + \frac{g_{m2} g_{m4}}{C_1 C_2}} \quad \text{Eqn 5.29}$$

Once again, the low-frequency gain is $\frac{v_o}{v_i} = g_{m1}/g_{m4}$ which is the same as the first-order low-pass filter (and $\Sigma\Delta$ modulator). The high loop gain offered by these circuits suppresses noise and nonlinearity from the transconductors g_{m2} and g_{m3} when referred to the input of the biquad. Hence the noise analysis for the first and second-order filters (and $\Sigma\Delta$ modulator) should be the same at low-frequency. It will be shown that minimal differences exist between the analysis of the filter and the oversampled A/D as regards noise and nonlinearity.

5.4 The Operational Transconductance Amplifier (OTA)

5.4.1 Introduction

The use of an OTA is central to the design of the continuous-time modulator as it allows a maximization of available bandwidth for any given technology. This is accomplished by the intrinsic advantage OTAs have over conventional amplifiers, namely current rather than volt-

age amplification. As a current amplifier, the bandwidth is potentially limited only by the f_t of the transistor [Gre84].

As already touched upon, the OTA used here [Bea90] is of a fully, doubly-differential configuration and makes use of several techniques to help overcome many of the deficiencies inherent in conventional OTAs. The doubly-differential input pairs, seen in Figure 5.9, is used for summing both feedforward and feedback signals allowing the OTA to remain in open loop. This causes linearity to be sacrificed for bandwidth as there is no longer a virtual ground. One technique that combats this loss of linearity is the use of the well-known Gilbert gain cell [Gil68], [Gre84]. The main advantage of the Gilbert Gain Cell is its tunability. This is to overcome the use of emitter degeneration which typically fixes the transconductance. It should be noted that the linearity of the OTA is still in part due to the V-I conversion stage to be discussed next.

The OTA (also known as a V-I transconductor) should have high-input impedance and high output impedance so as to avoid leakage off the integration capacitor. The folded-cascode amplifier is the perfect candidate as it can have these attributes. A technique that has been employed here, that has come to be known as Miller integration, utilizes a pole-splitting output stage which improves the design of the OTA in several ways. For instance, the pole-splitting capacitor is now the integration capacitor which isolates the capacitor's node from the impedances external to the OTA. Furthermore, the output swing is enhanced from simple folded-cascode architectures and the DC gain of the amplifier, which is greatly improved, minimizes phase lead at the UGBW. The linearization that comes from Gilbert gain cells is necessary here due to the exponential nonlinearity of bipolar transistors used in the differential input pairs which themselves are needed to achieve wide bandwidths. This, in addition to the use of a pole-splitting output stage, are the main features that differentiate this design from the low speed, simple CMOS OTA-based design [CST91], the publication that came out subsequent to the fabricated design presented here.

To elaborate, the Gilbert gain cell is a well-known circuit technique that allows linear amplification at the input stage through the use of a v_{BE} predistortion circuit. The large signal characteristic of current in a differential pair is a tanh function of the difference mode voltage. By predistortion of this difference-mode voltage through another differential pair (inverse tanh), linear current amplification may take place as seen in Figure 5.10a). The driving current into

Figure 5.9 Full schematic of the OTA

Figure 5.10a Compression (predistortion) stage (Q_1, Q_2) of Gilbert Gain Cell into the inner differential pair (Q_3, Q_4).

Figure 5.10b The entire Gilbert gain cell used in the context of the OTA, including the V-I conversion stage

the compression stage is accomplished by linear V-I conversion through a highly degenerated differential pair as shown in Figure 5.10b). The voltage gain of the entire cell has been found to be

$$A_v = \frac{R_O}{R_{EE}} \frac{I_T}{I_{IB}} \quad \text{Eqn. 5.9}$$

where the maximum input range is $I_{IB}R_{EE}$ [KAT+93]. The above expression has no assumptions and is valid for large-signal operation which is necessary here since the small-signal approximation ($v_{be} \ll V_T$) is violated as the OTA runs in open-loop. It should be noted that it is the intention to operate the transconductor with equal currents for if I_I and I_{IB} are not equal, then third-order distortion terms appear due to this mismatch alone [MGv93]. In reality, these currents can never equal due to component and V_{BE} mismatches. Furthermore, the linearity of the emitter degeneration resistor can give rise to second- and third-order distortion products.

Naturally, there will be second-order distortion components that arise from the OTA as well. Other secondary parameters that can affect the linearity are quite well documented [MGv93] and are mismatches in V_T (due to local differences in temperature), R_{EE} , β as well as differences in the bulk resistances r_i and r_{be} . It should be noted that the causes of nonlinearity in the OTA, primarily from the Gilbert gain cell are well documented and are not part of this study. It suffices to say that the OTA is characterizable, in the same manner as the opamp in Chapter 3 was, and the way in which nonlinearity goes through to the output of these circuits is of importance here. This will be discussed with respect to each of the circuits later.

To help minimize many of the problems that cause nonlinearity, common-centroid layout of the transistors is exercised as denoted by the parallel combination of BJTs in Figure 5.9. For good input range and relatively good linearity, the initial V-I stage or differential pair (see Figure 5.10b) is highly degenerated. The UGBW of the OTA taken differentially, with a pole-splitting output stage is

$$\omega_{UGBW} = \frac{g_{mout}}{C_c} \quad [\text{rads/s}] \quad \text{Eqn 5.31}$$

where $g_{mout} = 1/R_{EE}$ when $I_I = I_{IB}$ and C_c is the compensation capacitor. Primarily due to stability, relating to the existence of parasitic poles, the UGBW was set to 36.2 MHz (72.4 MHz differentially).

5.4.2 OTA and Filter Noise

5.4.2.1 Introduction

As has been a main theme throughout the course of this thesis, an important consideration in the design of continuous time oversampled A/Ds and filters is the noise from the OTA and

how it propagates to the output of the circuit. As there are multiple differential pairs required to perform the summing operation at the input, a strategy is needed that will allow a comprehensive method of determining the effects of this noise while in closed-loop. It is possible to identify a common node internal to the amplifier where all sources of noise may be referred to, and then finally referred to the input of one of the Gilbert gain cells. This procedure is not unlike conventional noise analysis where it would be possible to sum all noise contributions to the output of an amplifier, allowing it to then be input-referred.

In conventional opamp-based, external-component filter implementations, input-referred amplifier noise and the external resistor (conventional or switched capacitor) $4kTR$ thermal noise all contribute to the total noise at the output, as seen in the previous chapter. For OTA-based circuits, there are typically no external components leaving only input-referred noise seen at the various inputs to the Gilbert gain cells. Because there is no virtual ground, noise does not get referred to the positive input like conventional opamps.

It was theorized initially and proven through simulation that noise in doubly-differential (as well as conventional) OTAs propagates through to the output of the first- and second-order low-pass filters as shown in Figure 5.11 and Figure 5.12 respectively. The actual noise that is concentrated into the two sources shown in the figures comes from several origins, all related to active noise. It does not come from noise associated with the equivalent resistance the transconductors replace as is sometimes thought. The noise seen at the output of the first-order low-pass filter is

$$VSD_{O1}(\omega) = \sqrt{VSD_{h1}^2 \left[\frac{g_{m1} \cdot g_{m2}}{1 + j\omega C_1 \cdot g_{m1}} \right]^2 + VSD_{u1}^2 \left[\frac{1}{1 + j\omega C_1 \cdot g_{m1}} \right]^2} \cdot \left| \frac{V}{j\omega} \right| \quad \text{Eqn 5.32}$$

Similarly, the noise at the output of the second-order filter is

$$VSD_{O2}(\omega) = \sqrt{VSD_{h1}^2 \left[\frac{g_{m1} \cdot g_{m2}}{1 + \frac{j\omega C_1 g_{m1} + (j\omega)^2 C_1 C_2}{g_{m1} g_{m2}}} \right]^2 + VSD_{u1}^2 \left[\frac{1}{1 + \frac{j\omega C_1 g_{m1} + (j\omega)^2 C_1 C_2}{g_{m1} g_{m2}}} \right]^2} \cdot \left| \frac{V}{j\omega} \right|$$

Eqn 5.33

Figure 5.11 Single-ended representation of the first-order low-pass $g_m - C$ filter with noise sources.

Figure 5.12 Single-ended representation of the second-order low-pass $g_m - C$ filter with noise sources

The fact that noise manifests in this manner, for multiple differential input pairs, makes this type of circuit topology quite advantageous, at least conceptually, over conventional opamp-based, external component implementations assuming that the input-referred noise to each of the differential pairs can be kept low.

The ultimate goal here is to ascertain the relevant noise sources in continuous-time $g_m - C$ oversampled A/Ds. The following section deals with the determination of noise in the loop filters contained within the oversampled A/Ds. The methodology presented may then be extended and compared to the oversampled A/Ds themselves where possible. To that end, it is necessary to examine noise seen at low-frequencies (i.e. frequencies in the baseband, well before the resonant peak in the biquad), as noise beyond the baseband is filtered out by decimation.

5.4.2.2 Low-Frequency, Closed-Loop (Filter) Noise Propagation

Determination of the noise sources seen in Figure 5.11 and Figure 5.12 may be made by considering individual gains throughout the OTA, referring noise to the inputs of the two differential pairs. The manner with which noise goes through to the output of the filters at low frequency is determined quite readily.

First, consider Figure 5.13 - a simplified schematic of the OTA, ignoring the common mode feedback circuit (CMFB) for now. The main sources of noise are attributed to the Gilbert gain cells. Other noise sources deep within the OTA may be referred to node V_1 (and V_2) as will be shown for their overall contribution to the output of the filters and modulators can be significant by virtue of the low gain of the Gilbert gain cells.

Single-ended noise calculations are used here which may subsequently be multiplied by $\sqrt{2}$ for the differential output noise. As the differential signal is twice the single ended output, a 3 dB SNR advantage can be obtained due to the use of differential circuitry.

A complete single-ended path of the OTA of Figure 5.13 may now be drawn as a block diagram shown in Figure 5.14a) which contains the major noise sources and gain sections within the amplifier. This may further be broken up into a more detailed diagram separating out the different stages of the Gilbert gain cells and the constituent noise sources as shown in Figure 5.14b). The values of these noise sources will be found later.

First, a preliminary determination of the gain of individual stages within the OTA is necessary for the purpose of referring noise to the inputs and for determining relative noise contributions to various parts of the circuit.

With reference to Figure 5.15 and using small-signal analysis for simplicity, the voltage gains of the outer differential pairs with emitter degeneration (A_{ODPa}) and without emitter degeneration (A_{ODPn}) are

$$A_{ODPa} = \frac{V_R}{V_{in}} = \frac{1}{2} \frac{g_m}{g_m + R_{EE}} \approx \frac{1}{2} \frac{1}{R_{EE}} \quad (1)$$

0.028

Eq. 5.6

Figure 5.13 Simplified OTA schematic

The Operational Transconductance Amplifier (OTA)

Figure 5.14a Single-ended path of the OTA with voltage gains of both Gilbert gain cells A_{n1} and A_{n2} and A_p along with their respective input-referred voltage spectra that defines VSD_{n1} and VSD_{n2} and $VSD_p = V_o/V_c$.

Figure 5.14b Gilbert gain cells are separated into their respective constituent Gilbert cells with their respective voltage gains, A_{n1diff} and A_{n2diff} with their respective input spectra.

Figure 5.15 (a) Differential pair with emitter degeneration with voltage gain A_{diff0} .

3

PM-1 3 1/2" x 4" PHOTOGRAPHIC MICROCOPY TARGET
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where a transconductance of $g_{m1} = g_{m2} = g_{m3} = g_{m4} = 15.4 \text{ mmho}$ and $R_{F1} = 1100 \Omega$.

For completeness, as a comparison, the single-ended DC gain of the undegenerated differential pair in Figure 5.15b) is

$$A_{ODPa} = \frac{V_{B4}}{V_{Ia}} = \frac{1 \cdot g_{m3}}{2 \cdot g_{m4}} = 0.50 \quad \text{Eqn 5.35}$$

The gain in the above equation is particularly relevant to the oversampled A/Ds. However, in the filters both Gilbert gain cells are equally degenerated, thus A_{ODPa} equals A_{ODPb} here.

The gain of the inner differential pair, A_{IDP} , as well as other gain calculations are derived in Appendix E (Section E.1). For accuracy however, the individual gains found from simulation are used since comparisons between theoretical and simulated noise will be made. Figure 5.16 shows an open-loop AC postlayout simulation of the OTA from the input to node V_B , V_C , V_D , V_O .

Figure 5.16 Gains from the input of the OTA to various nodes from postlayout simulation, taken single-ended at the output

and the output v_o (See Figure 5.13 for node locations). Thus deducing the individual gain leads to $A_{ODPB} = 0.025$ and $A_{IDP} = 16$, the gains that are of immediate importance. The remaining gain from node v_i to the output summates to

$$A = 70\text{dB} \quad \text{Eqn 5.36}$$

and compares favorably with theory. With reference to Figure 5.17 and ignoring the noise sources for now, the loop around the OTA may be closed. This, in effect, represents the low-frequency behavior of the first- and second-order filters and $\Sigma\Delta$ modulators. Relevant at low-frequencies only, it is not difficult to show that

$$\frac{V_o}{V_{th}} = -\frac{A_{ODPB}A_{IDP}A}{1 + A_{ODPB}A_{IDP}A} = -\frac{A_{i1}A}{1 + A_{i2}A} \quad \text{Eqn 5.37}$$

where $A_{i1} = A_{ODPB}A_{IDP}$ and $A_{i2} = A_{ODPB}A_{IDP}$ as was shown in Figure 5.14a) and Figure 5.14b).

If the loop gain is large ($A_{i2}A \gg 1$), then

$$\frac{V_o}{V_{th}} \approx -\frac{A_{i1}}{A_{i2}} \quad \text{Eqn 5.38}$$

as might be expected.

Having determined the low-frequency gain, it is now timely to concentrate on the noise within the amplifier. Foremost, consider the noise associated with the Gilbert gain cells. Referring to Figure 5.14a) and Figure 5.14b), it is easy to see that the Gilbert gain cells have input-referred VSD

Figure 5.17 System-level representation of the OTA in closed-loop

$$VSD_b = \sqrt{S_b} = \sqrt{S_{b1} + \frac{S_{b2}}{A_{OTPB}^2}} \quad \text{Eqn 5.39}$$

$$VSD_a = \sqrt{S_a} = \sqrt{S_{a1} + \frac{S_{a2}}{A_{OTPA}^2}} \quad \text{Eqn 5.40}$$

These equations show a major disadvantage of the Gilbert gain cell. Noise subsequent to the V-I stage (the outer differential pair) can become large when input-referred.

Now, the total noise seen at the output of the open-loop OTA may be found from the individual contributions VSD_a , VSD_b and VSD_c . One method to handle the noise from the second Gilbert gain-cell in addition to all other these sources of noise was to refer them all to the input of just one Gilbert gain cell as shown in Figure 5.18. Including the noise at node V_i , the total in

Figure 5.18 All noise considered significant within the amplifier is input-referred to V_{ib} (single-ended).

put-referred noise is then simply

$$VSD_I = \sqrt{VSD_b^2 + VSD_a^2 \left(\frac{A_{v2}}{A_{v1}} \right)^2 + \frac{VSD_c^2}{A_{v1}^2}} \quad \text{Eqn 5.41}$$

In open-loop (Figure 5.18), this noise goes through to the output of the OTA such that the output-referred VSD is

$$VSD_O = (A_{v1}A) VSD_I \quad \text{Eqn 5.42}$$

where the product $A_{v1}A$ is simply the open-loop gain of the OTA.

In closed-loop (i.e. in the context of the low-pass filters) as seen in Figure 5.19, the various noise sources goes through to the output according to

$$VSD_o = \sqrt{VSD_b^2 \left(\frac{A_{v1}}{A_{v2}} \right)^2 + VSD_a^2 + \left(\frac{VSD_c}{A_{v2}} \right)^2} \quad \text{Eqn 5.43}$$

which at low frequencies equals the closed-loop gain A_{v1}/A_{v2} multiplied by total input-referred noise spectral density VSD_i described above. The next few sections predict thermal and 1/f noise through calculations and are substantiated through HSPICE simulations and measurements. A table may be found at the end that summarizes and compares theoretical predicted, simulated and measured noise in the context of the OTA and filters.

5.4.2.3 Thermal Noise

It is now prudent to calculate the individual noise contributions which input-refer to the quantities VSD_b , VSD_a (associated with the Gilbert gain cells) and VSD_c (mostly due to the cascodes). Once this is done, the noise at the output of the open-loop OTA or the output of either closed-loop filter may be found for comparison with simulation and measurement. This is necessary to validate the methodology taken here in determining how noise propagates in these $g_m - C$ circuits. Recall, in the context of the filters, both Gilbert gain cells have outer differential pairs that are emitter degenerated so that $A_{ODPb} = A_{ODPa} = 0.025$. This is to keep the low-frequency gain of the filters equal to unity, the same as the oversampled A/Ds. A slight modification is made to the following analysis for the A/D case which will be covered later. With reference to Figure 5.20, the individual noise contributors that make up S_{b1} and S_{b2} (which are

Figure 5.19 Closed-loop configuration with the simplified Gilbert cell input-referred noise sources.

Figure 5.20 a) Outer and inner differential pair with noise sources b) Block diagram representation of a).

now the same as S_{a1} and S_{a2}) are as follows. With reference to the figure of the Gilbert gain cell (Figure 5.20), it is clear that S_{b1} is simply equal to S_{n1} . Thus the noise of the outer differential pair comes from transistor Q1 and has a VSD of

$$\begin{aligned} VSD_{b1} &= \sqrt{S_{n1}} = \sqrt{4KT \left(\frac{1}{2g_{m1}} + r_{bb1} + R_{IE} \right)} \\ &= 4.67 \frac{nV}{\sqrt{Hz}} \end{aligned}$$

Eqn 5.44

where values of these components such as transconductance, etc. may be found in Appendix E. Furthermore $S_{b2} = S_{n2} + S_{n5}$. Thus, the resulting VSD associated with the inner differential pairs is

$$\begin{aligned} VSD_{b2} &= \sqrt{S_{n2} + S_{n5}} = \sqrt{4KT \left(\frac{1}{2g_{m2}} + r_{bb2} \right) + 4KT \left(\frac{1}{2g_{m5}} + r_{bb5} \right)} \\ &= 2.36 \frac{nV}{\sqrt{Hz}} \end{aligned}$$

Eqn 5.45

It should be noted that the base-current shot noise from these transistors contribute insignificantly to the above values found. This may easily be seen by considering the relatively low resistance seen from the base-current shot noise sources in Figure 5.21, a detailed schematic of this section.

Figure 5.21 Base current shot noise and 1/f noise considerations as regards the emitter degenerated differential pair. (Note that the resistance seen by each of the noise sources is relatively low)

As stated earlier, both Gilbert gain cells are degenerated and so by using Eqn 5.39 and Eqn 5.40, the noise associated with each of the Gilbert gain cells may be referred to the input of each cell such that

$$\begin{aligned}
 VSD_b = VSD_a &= \sqrt{(4.67 \times 10^{-9})^2 + \left(\frac{2.36 \times 10^{-9}}{0.025}\right)^2} \\
 &= 94.5 \frac{nV}{\sqrt{Hz}}
 \end{aligned}$$

Eqn 5.46

Immediately, it may be noted that the use of a Gilbert gain cell trades off linear input range for better noise since the gain of the outer differential pairs A_{ODPb} (and A_{ODPa}) depends on the size of the emitter degeneration resistor.

Now the remaining noise spectral densities that significantly make up VSD_c may be considered by referring them to node V_c . The dominant sources of noise are attributable to the cascode current sources M1 and M2 as shown in Figure 5.22. It should be noted that normally the cascode load transistor Q9 would be a formidable contributor of thermal noise. However, by virtue of the several parallel combinations of transistors used to make up Q9 (6x transistor) r_{bb} is reduced to be small enough so as not to contribute significantly to VSD_c (when referred to node V_c).

Figure 5.22 Simplified schematic of the OTA with noise sources

Relying on the same methodology presented in Chapter 3 to calculate the relative contributions, these gate-referred thermal noise sources seen at node V_i is found such that VSD_i may be approximated to

$$VSD_i = \sqrt{\left(VSD_{M1} \frac{g_{mM1}}{g_{mM2}} \right)^2 + (VSD_{M2})^2}$$

$$= 6.15 \frac{nV}{\sqrt{Hz}}$$

Eqn 5.47

where the gate-referred thermal noise of M1 is

$$VSD_{M1} = \sqrt{S_{nM1}} = \sqrt{4KT \left(\frac{2}{3} \frac{1}{g_{mM1}} \right)}$$

$$= 1.42 \frac{nV}{\sqrt{Hz}}$$

Eqn 5.48

and similarly the thermal noise from M2 is, $VSD_{M2} = 2.78 nV / \sqrt{Hz}$. (See Appendix E, Section E.1 for all necessary information required for these calculations.)

As a check, all sources of noise may be referred to the input of one of the Gilbert gain cells. The total VSD at the input as seen in Figure 5.18 is from Eqn 5.41 reiterated below

$$VSD_i = \sqrt{VSD_b^2 + VSD_a^2 \left(\frac{A_{v2}}{A_{v1}} \right)^2 + \left(\frac{VSD_i}{A_{v1}} \right)^2}$$

$$= 135 \frac{nV}{\sqrt{Hz}}$$

Eqn 5.49

where $A_{v1} = A_{v2} = 0.45$ from simulation. As predicted, the noise associated with the inner differential pairs, when input referred, causes this type of cell to be quite noisy. For an accurate comparison, the simulated open-loop gain of the OTA was found, from Figure 5.17 to be 63 dB single-ended. Thus, the theoretical output-referred thermal noise is

$$VSD_o = (135 \times 10^{-9}) (1413)$$

$$= 191 \frac{\mu V}{\sqrt{Hz}}$$

Eqn 5.50

This compares favorably with the $200\mu\text{V}/\sqrt{\text{Hz}}$ found in the simulation of Figure E.1a), found in Appendix E, Section E.2. The measured OTA open-loop gain (single-ended) was found to be 48 dB. With this open-loop gain, the expected VSD at the output should be

$$\begin{aligned} \text{VSD}_o &= (135 \times 10^{-9}) (251) \\ &= 34 \frac{\mu\text{V}}{\sqrt{\text{Hz}}} \end{aligned} \quad \text{Eqn 5.51}$$

The measured VSD at the output of the open-loop OTA was $34.8\mu\text{V}/\sqrt{\text{Hz}}$ as shown in Figure E.1b) which compares quite nicely to theory.

When the OTA is in closed-loop (i.e. configured as a first-order, low-pass filter), the low-frequency noise according to Eqn 5.43 is

$$\begin{aligned} \text{VSD}_o &= \sqrt{\text{VSD}_b^2 \left(\frac{A_{v1}}{A_{v2}} \right)^2 + \text{VSD}_a^2 + \left(\frac{\text{VSD}_1}{A_{v1}} \right)^2} \\ &= 135 \frac{\text{nV}}{\sqrt{\text{Hz}}} \end{aligned} \quad \text{Eqn 5.52}$$

since the gain coefficients A_{v1} equals A_{v2} as discussed earlier. The theoretical VSD found above compares closely with the closed-loop gain and noise simulation of Figure E.2a) with $147\text{nV}/\sqrt{\text{Hz}}$ as the resulting VSD seen at the single-ended output of the filter. The measured thermal noise compares very closely at $152\text{nV}/\sqrt{\text{Hz}}$ as shown in Figure E.2b) which validates the methodology used here in determining the noise in these OTA-based circuits.

5.4.2.4 1/f Noise

The 1/f noise contributions from both Gilbert gain cells (for example, transistors Q1, Q2 and Q5) may be considered. With reference to Figure 5.21, these noise spectral densities are

$$S_{n(f)1} + S_{n(f)2} + S_{n(f)3} = \frac{KI_n^{Af}}{f} \left[\frac{A^2}{Hz} \right]$$

$$S_{n(f)1}(1kHz) = \frac{K(4 \times 10^{-6})^{Af}}{1000} \\ = 20.9 \times 10^{-24} \frac{A^2}{Hz}$$

Eqn 5.53

However, as seen in Figure 5.21, this current noise flows into relatively low resistances making this source of noise insignificant compared to the greater quantity of 1/f noise that comes from the MOS current source cascode devices, M1 and M2 (the same is true for M3 and M4 also). Once again, it may be shown that the VSD at node v_c from 1/f noise now is

$$VSD_{(1/f)c} = \sqrt{\left(VSD_{(1/f)M1} \frac{g_{mM1}}{g_{mM2}} \right)^2 + VSD_{(1/f)M2}^2} \\ VSD_{(1/f)c}(1kHz) = 118 \frac{nV}{\sqrt{Hz}}$$

Eqn 5.54

where it may be shown that the gate-referred VSD at 1 kHz, $VSD_{(1/f)M1}(1kHz) = 28.9nV/\sqrt{Hz}$ and $VSD_{(1/f)M2}(1kHz) = 37.8nV/\sqrt{Hz}$. The contribution from the cascode load transistor Q9 does not add significantly to the VSD seen at node v_c and is therefore ignored here. $VSD_{(1/f)c}$ may now be input-referred to one of the Gilbert gain cells as was done in the thermal noise case such that

$$VSD_{(1/f)I}(1kHz) = \frac{VSD_{(1/f)c}(1kHz)}{A_{v1}} \\ = 295 \frac{nV}{\sqrt{Hz}}$$

Eqn 5.55

In open-loop, this 1-f noise would be (using the simulated gain of 63 dB)

$$VSD_{(1/f)O}(1kHz) = (295 \times 10^{-9})(1413) \\ = 417 \frac{\mu V}{\sqrt{Hz}}$$

Eqn 5.56

The simulated 1/f noise seen at the output is $447 \mu\text{V}/\sqrt{\text{Hz}}$ as seen in Figure E.3a). Since the measured open-loop gain is 48 dB here, the expected 1/f noise would be

$$\begin{aligned} VSD_{\text{closed-loop}}(1\text{kHz}) &= (295 \times 10^{-9}) (251) \\ &= 74 \frac{\mu\text{V}}{\sqrt{\text{Hz}}} \end{aligned} \quad \text{Eqn 5.57}$$

which compares well with the measured VSD of $68.8 \mu\text{V}/\sqrt{\text{Hz}}$ seen in Figure E.3b). Furthermore, in the same closed-loop configuration discussed earlier, the expected theoretical 1/f noise at the output is, from Eqn 5.43

$$\begin{aligned} VSD_{\text{closed-loop}}(1\text{kHz}) &= \frac{A_{v1}}{A_{v2}} VSD_{\text{open-loop}}(1\text{kHz}) \\ &= 295 \text{ nV}/\sqrt{\text{Hz}} \end{aligned} \quad \text{Eqn 5.58}$$

when $A_{v1} = A_{v2}$. This compares favorably with both the simulation of Figure E.4a) having a VSD of $316 \text{ nV}/\sqrt{\text{Hz}}$ and the measured VSD of $310 \text{ nV}/\sqrt{\text{Hz}}$ seen in Figure E.4b).

5.4.2.5 Thermal and 1/f Noise in the Biquad Filter

As already stated, the noise results found for the first-order low-pass filter, at low frequencies, should be the same for the biquad filter. As expected, the thermal noise was found to be $147 \text{ nV}/\sqrt{\text{Hz}}$ from simulation (Figure E.5a) which agrees well with the theoretical calculation of $135 \text{ nV}/\sqrt{\text{Hz}}$. The measured thermal noise was $150 \text{ nV}/\sqrt{\text{Hz}}$ from Figure E.5b). The noise at the resonant peak from simulation was $223 \text{ nV}/\sqrt{\text{Hz}}$ while the measured VSD at this peak was found to be $316 \text{ nV}/\sqrt{\text{Hz}}$ (Figure E.5c) which may be explained by a slightly higher Q in measurement. Note that the natural frequency of the measured biquad filter was 36 MHz as may be crudely seen in Figure E.5c). Also, the simulated 1/f noise was, as expected, $316 \text{ nV}/\sqrt{\text{Hz}}$ as seen in Figure E.6a). The measured 1/f noise was $326 \text{ nV}/\sqrt{\text{Hz}}$ as seen in Figure E.6b) which agrees well with both theoretical and simulated voltage spectral densities.

5.4.2.6 Common-mode Feedback Circuit Noise

The common mode feedback circuit (CMFB) within the OTA, shown in Figure 5.13, may be redrawn in a block diagram representation in Figure 5.23. As may be seen, the noise contribu-

Figure 5.23 Block diagram representation of the common-mode feedback circuit

tion seen at the output is simply the input-referred noise of the common-mode circuit and is

$$VSD_{cm} = \sqrt{4KT \left(\frac{1}{2g_{m24}} + 5000 \right)} \\ \approx 9 \frac{nV}{\sqrt{Hz}} \quad \text{Eqn 5.59}$$

which is much less than the difference-mode circuit noise calculated previously. It was therefore not necessary to include this contribution in the overall calculation of output-referred thermal noise, when taken single-ended.

The table below summarizes the results of the last few sections through comparing the theoretical, simulated and measured noise from thermal and 1/f noise sources seen at the output of the OTA open loop, the first- and second-order low-pass filters.

Circuit and Noise Type	Theoretical	Simulation	Measured	Theoretical Measured
Open loop OTA, Thermal	191 $\mu V / \sqrt{Hz}$	200 $\mu V / \sqrt{Hz}$	34.8 $\mu V / \sqrt{Hz}$	34 $\mu V / \sqrt{Hz}$ ^a
Open loop OTA, 1/f ^b	417 $\mu V / \sqrt{Hz}$	447 $\mu V / \sqrt{Hz}$	68.8 $\mu V / \sqrt{Hz}$	74 $\mu V / \sqrt{Hz}$ ^c

Table 5.1: Single-ended Noise Measurements (at low frequency unless specified)

Circuit and Noise Type	Theoretical	Simulation	Measured	Theoretical Measured
1st-order filter, Thermal	135 nV/√Hz	147 nV/√Hz	152 nV/√Hz	N/A
1st-order filter, 1/f	295 nV/√Hz	316 nV/√Hz	310 nV/√Hz	N/A
2nd-order filter, Thermal	135 nV/√Hz	147 nV/√Hz	150 nV/√Hz	N/A
2nd-order filter, Thermal at the resonant peak ^d	205 nV/√Hz	223 nV/√Hz	316 nV/√Hz	291 nV/√Hz ^e
2nd-order filter, 1/f	295 nV/√Hz	316 nV/√Hz	320 nV/√Hz	N/A

Table 5.1: Single-ended Noise Measurements (at low frequency unless specified)

- a. Theoretical measured noise is less than simulation due to the lower measured OTA open loop gain (+48 dB).
- b. All 1/f noise taken at 1 KHz.
- c. Theoretical measured noise is less than simulation due to the lower measured OTA open loop gain (+48 dB).
- d. The resonant peak frequency is at 26 MHz.
- e. The measured magnitude of the resonant peak was 6.5 dB, and is slightly different than theory and simulation from slight Q peaking or mismatch in capacitors or transconductance.

5.4.3 Oversampled A/D Thermal and 1/f Noise

Up until now, the main focus of noise has been confined to the loop filters that exist within the oversampled A/Ds. As was discussed in the previous chapters, the quantizer may be modelled as a simple additive noise source preceded by a gain element—the existence of which does not affect the manner in which noise propagates through to the output of the filters at low frequencies.

Since the oversampled A/Ds use current steering as a means of providing feedback, one of the two Gilbert gain cells must be kept undegenerated for fast switching, an important consideration since slow switching translates to delayed feedback. Delayed feedback and slow switching can cause problems under idle channel conditions and might enhance nonlinearity, as will be discussed later. As slew-rate limited current charges the integration capacitor from this differential pair, it can be shown that there is far less noise associated with it. With reference to

Figure 5.13, the input signal enters via V_{ib} while the signal from the quantizer switches the differential input pair associated with V_{ia} .

This alters the theoretical VSD that would be seen at the output of the oversampled A/D (both first- and second-order) at low frequency since now VSD_a does not exist, but rather a collector-current shot noise component from the current source Q26 from Figure 5.13 and is denoted as VSD_c , found at node V_c , where

$$\begin{aligned} VSD_{CS} &= \sqrt{2qI_{C26}(1/g_{mM2})^2} \\ &= 10.7 \frac{nV}{\sqrt{Hz}} \end{aligned} \quad \text{Eqn 5.60}$$

where this source of noise is only important in the differential pairs that replaced transconductors denoted as g_{m4} in the first- and second-order $\Sigma\Delta$ modulators. Hence the expected VSD at the output of the A/Ds are

$$\begin{aligned} VSD_o &= \sqrt{VSD_b^2 \left(\frac{A_{v1}}{A_{v2}}\right)^2 + \left(\frac{VSD_c}{A_{v2}}\right)^2 + \left(\frac{VSD_{CS}}{A_{v2}}\right)^2} \\ &= 98.4 \frac{nV}{\sqrt{Hz}} \end{aligned} \quad \text{Eqn 5.61}$$

where A_{v1} equals A_{v2} since the closed-loop gain equals 1. This is a substantial reduction over the filter, attributable solely to the use of current-steering feedback.

The $1/f$ noise in the oversampled A/Ds would be the same as in the filters since the dominant source of $1/f$ noise comes from the cascode devices here as well.

This completes the noise analysis of the $g_m - C$ based circuits presented in this thesis. The final result of the above equation is valid for both first- and second-order continuous-time $\Sigma\Delta$ modulators. It sets a fundamental limit on the achievable resolution for any given bandwidth. This will be brought up again at the end of the chapter on the discussion of applications.

5.5 Harmonic Distortion in Transconductor-Based Filters and Oversampled A/Ds

5.5.1 Harmonic Distortion in the First- and Second-Order Low-Pass Filters

5.5.1.1 Introduction

It was proven in the last chapter that the linearity of the loop filter is the same as the linearity of the oversampled A/D at low frequencies. The effect of the gain element K and the delay of the quantizer causes differences only in the high-frequency response between the loop filter and the oversampled A/D. This difference was nearly eliminated by modelling the sampled-data DISDM as a continuous-time biquad filter, allowing the determination of the high-frequency harmonic behavior with relatively good understanding. The study of distortion in these oversampled A/Ds is confined to low frequencies only, and so the necessity of having to characterize the loop by determining the gain of the quantizer is alleviated.

As might be expected, there is a similarity between the manner nonlinearity propagates through to the output of $g_m - C$ $\Sigma\Delta$ modulators and filters. It is interesting to analyze the filters by approximating the distortion characteristics at all frequencies. The results may then be compared to the distortion seen at baseband frequencies in the $\Sigma\Delta$ modulator. It is first necessary, however, to determine the linearity of the OTA in order to proceed with filter and $\Sigma\Delta$ modulator distortion.

This study proceeds with the theoretical distortion seen at the output of an open-loop OTA integrator. The linearity of the OTA, after it has been ascertained, may be used to determine the linearity of the filters and oversampled A/Ds. Comparisons are made between the theoretical, simulated and measured circuits.

5.5.1.2 OTA Distortion

In order to proceed with the distortion analysis of the $g_m - C$ circuits listed above, it is worth taking a moment to clearly describe the manner in which the OTA linearity coefficients are

found. This detailed procedure is found in Appendix E, Section E.3, while the theory follows below along with a tabulated summary of results from the Appendix.

In the previous chapter, the opamp nonlinearity was found through simple static measurements of output voltage as a function of difference-mode input voltage. Here, as there is a pole-splitting output stage attached to the transconductor head stage, measuring current as a function of voltage directly is not possible. Thus, it is necessary to turn to frequency selective techniques in order to determine the OTA linearity coefficients. This will be necessary for both the simulated and measured OTAs since there are differences in UGBW and distortion between the two from circuit imperfections and comparisons are warranted. The distortion seen at the output of the OTA is now theorized.

With reference to Figure 5.24, consider the current that exits this transconductor, described as

Figure 5.24 Open-loop transconductor (OTA)

a power-series expansion such that

$$i_1 = -g_{11}v_i + g_{12}v_i^2 + g_{13}v_i^3 \quad \text{Eqn 5.62}$$

where g_{11} is simply the transconductance g_{m1} while g_{12} and g_{13} are defined as the second- and third-order linearity coefficients of this transconductor (denoted in the figure simply by g_{m1}). It would be possible to express the resulting nonlinearity in the form of a differential equation where $i_1 = Cdv_o/dt$. By using the Laplace transform (i.e. $s \equiv j\omega \equiv d/dt$), a simpler method of determining the harmonics may be employed. This point will be touched upon later. The resulting voltage that is generated at the output of the OTA is simply $v_o(j\omega) = i_1/j\omega C$ leading to

$$v_o(j\omega) = -\frac{g_{11}}{j\omega C}v_i(j\omega) + \frac{g_{12}}{j\omega C}v_i^2(j\omega) + \frac{g_{13}}{j\omega C}v_i^3(j\omega) \quad \text{Eqn 5.63}$$

where $C = 2pF$. The resulting pre-bandlimited absolute signal harmonics, with help from Chapter 2, are

$$\begin{aligned} hd(f) &= \frac{g_{11}/C}{2\pi f} V_i \\ hd(2f) &= \frac{1}{2} \frac{g_{12}/C}{2\pi f} V_i^2 \\ hd(3f) &= \frac{1}{4} \frac{g_{13}/C}{2\pi f} V_i^3 \end{aligned} \quad \text{Eqn 5.64}$$

where V_i is the peak input amplitude applied to the transconductor. Pre-bandlimited here is in reference to the harmonics that exist before filtration by the integrator (i.e. the integrator causes the second- and third-order harmonics to be attenuated by 6 dB and 9.5 dB respectively).

The above equations may now be used to determine the linearity coefficients of the OTA given any set of harmonic levels and the input level V_i . The harmonics of the OTA may first be determined through postlayout simulation and later through measurements.

The measured single-ended UGBW of the transconductor was found to be 31 MHz which corresponds closely with the simulated (postlayout) UGBW as shown in Figure 5.16. It is not 36.2 MHz as originally designed due to differences between the laid-out and extracted parameter values particularly the polysilicon resistors and the polysilicon-polysilicon capacitors.

Applying a sinusoidal voltage of $V_i = 0.42V_{pk}$ at a frequency of 13 MHz to the fabricated OTA results in a $1 V_{pk}$ (-3 dBV) voltage measured at the output—a useful reference against which simulations may be compared.

Referring to Appendix E, Section E.3, a summary of results is tabulated leading to the simulated and “characterized” (i.e. measured) OTA linearity coefficients of the fabricated device.

From	Bandlimited Harmonics (dBV)	1/s Attenuation (dB)	Pre-bandlimited Harmonics (dBV)	Linearity Coefficients
Measured $hd(f)$	-3	0	-3	$g_{11} = 390 \mu A/V$
Measured $hd(2f)$	-55.6	6	-49.6	$g_{12} = 8.67 \mu A/V^2$
Measured $hd(3f)$	-55	9.5	-45.5	$g_{13} = 66.2 \mu A/V^3$
Postlayout Sim'n $hd(f)$	-5	0	-5	$g_{11} = 310 \mu A/V$
Postlayout Sim'n $hd(2f)$	-69.5	6	-63.5	$g_{12} = 1.75 \mu A/V^2$
Postlayout Sim'n $hd(3f)$	-78.2	9.5	-68.7	$g_{13} = 4.58 \mu A/V^3$

Table 5.2: Open-Loop OTA Harmonics from Postlayout Simulation and Measurement

The table above shows that the measured harmonics are larger than those found from simulation due to mismatches in V_{BE} , V_T and differences in tail current between the inner and outer differential pairs of the Gilbert gain cell attributable to β and BJT ratio size errors in the current mirrors.

These results may now be employed to validate the following theory of nonlinearity in $g_m - C$ filters. Since it is clear that distortion is greater in the fabricated OTA, the focus of the study into $g_m - C$ filter and $\Sigma\Delta$ modulator distortion will center on the characterized nonlinearity from the fabricated OTAs for the most part. Further postlayout simulations of the filters will be found in the Appendix. Theory will be developed that considers the nonlinearity from the fabricated OTAs. The distortion (IMDs to be exact) will be predicted and compared to measurement. Further comparisons by way of simulation are relied upon by means of transferring the characterized linearity coefficients into a nonlinear voltage-controlled current source macromodel. The ease and accuracy with which macromodelling is seen to be effective can be proven (as was seen in Appendix) allowing validation of the theories about to be presented.

The intermodulation distortion that arises from two signals (spaced closely together) applied to the input of the filters may now be plotted as a function of input frequency. These input signals will be swept up to the cutoff frequency of each filter and the second- and third-order

IMD products are found and subsequently compared to approximate theoretical levels about to be presented in upcoming theory.

5.5.1.3 First-order Low-pass Filter Distortion

Consider the first-order low-pass filter that was fabricated shown in Figure 5.25a). For ease of explanation, this doubly-differential configuration may be split up into the identical circuit of Figure 5.25b). Presented first is the case where only the feedforward transconductor g_{m1} is

Figure 5.25

a) First-order low-pass filter

b) Simplified representation of a) where transconductors are split up for ease of explanation and g_{m1} is nonlinear.

considered nonlinear. This simple case is important since it relates directly to the first-order oversampled A/D since the feedback is thought to be linear.

The current that exits this transconductor, i_1 , may be written as

$$i_1 = -g_{11}V_i + g_{12}V_i^2 + g_{13}V_i^3 \quad \text{Eqn 5.65}$$

Similarly, with reference to Figure 5.25b), g_{m4} remains linear such that

$$i_4 = -g_{m4}V_o \quad \text{Eqn 5.66}$$

These currents sum together such that $i_{14} = i_1 + i_4$. Thus,

$$i_{14} = -g_{11}V_i + g_{12}V_i^2 + g_{13}V_i^3 - g_{m4}V_o \quad \text{Eqn 5.67}$$

It is tempting to say that the voltage generated at the output is $v_o(j\omega) = i_{14}/j\omega C$. This is, in fact, the approach used to solve the harmonics. However it should be noted that generally better accuracy may be achieved by using differential equations to describe the filter in this case. For example,

$$i_{14} = C \frac{dv_o}{dt} = -g_{11}v_i + g_{12}v_i^2 + g_{13}v_i^3 - g_{m2}v_o \quad \text{Eqn 5.68}$$

Re-arranging leads to

$$\frac{dv_o}{dt} + \frac{g_{m2}}{C}v_o = -\frac{g_{11}}{C}v_i + \frac{g_{12}}{C}v_i^2 + \frac{g_{13}}{C}v_i^3 \quad \text{Eqn 5.69}$$

By letting $v_i = V_i \sin(\omega t)$, the above differential equation may be laboriously solved. One popular approach is through the infamous Volterra series. This is beyond the intended scope of this thesis. By making use of the differentiating theorem, $d/dt \equiv j\omega$ Eqn 5.69 after re-arranging (or simply letting $v_o(j\omega) = i_{14}/j\omega C$) yields the final result

$$v_o(j\omega) = \frac{-g_{11}/g_{m4}}{1 + j\omega C/g_{m4}}v_i(j\omega) + \frac{g_{12}/g_{m4}}{1 + j\omega C/g_{m4}}[v_i(j\omega)]^2 + \frac{g_{13}/g_{m4}}{1 + j\omega C/g_{m4}}[v_i(j\omega)]^3 \quad \text{Eqn 5.70}$$

At frequencies well below the filter's cutoff frequency, the above equation reduces to simply

$$v_o(j\omega) = \frac{-g_{11}}{g_{m4}}v_i(j\omega) + \frac{g_{12}}{g_{m4}}[v_i(j\omega)]^2 + \frac{g_{13}}{g_{m4}}[v_i(j\omega)]^3 \quad \text{Eqn 5.71}$$

Letting $v_i(j\omega) = V_i \sin(\omega t)$ and with help from the previous chapter, the fundamental, second and third absolute harmonics and IMD products are

$$\begin{aligned} hd(f) &\approx \frac{g_{11}}{g_{m4}}V_i \\ hd(2f) &= \frac{1}{2} \frac{g_{12}}{g_{m4}}V_i^2 & imd(f_1 - f_2) &= \frac{g_{12}}{g_{m4}}V_{i1}V_{i2} \\ hd(3f) &= \frac{1}{4} \frac{g_{13}}{g_{m4}}V_i^3 & imd(2f_2 - f_1) &= \frac{3}{4} \frac{g_{13}}{g_{m4}}V_{i1}V_{i2}^2 \end{aligned} \quad \text{Eqn 5.72}$$

where the "Almost Linear" approximation, discussed in Chapter 4, has been invoked.

(i.e. $g_{11}/g_{m4}V_i \gg g_{12}/g_{m4}V_i^2$ and $g_{11}/g_{m4}V_i \gg g_{13}/g_{m4}V_i^3$.) This is so that the by-products of the g_{12} and g_{13} terms resulting in a DC and a fundamental component may be neglected. The linearity

of the first-order oversampled A/D is a logical extension of this where the only source of non-linearity is considered to emanate from the feedforward transconductor since feedback is provided by current steering which is assumed to have no nonlinear traits. This is however, not entirely true of the filter. (The case of the oversampled A/D will be studied in detail later.) In fact, nonlinearity from the feedback transconductor g_{m4} may also contribute to the overall nonlinearity of the filter, as shown next.

Although the focus here is the distortion in the oversampled A/Ds at low frequencies only, it is not hard to extend this analysis to the filters as an approximation only. Consider the case where the feedback transconductor once denoted as g_{m4} is now indeed nonlinear so that

$$i_4 = -g_{41}v_o + g_{42}v_o^2 + g_{43}v_o^3 \quad \text{Eqn 5.73}$$

Summing currents into the capacitor C leads to

$$i_{14} = -g_{11}v_i + g_{12}v_i^2 + g_{13}v_i^3 - g_{41}v_o + g_{42}v_o^2 + g_{43}v_o^3 \quad \text{Eqn 5.74}$$

An approximation is now made. As v_o^2 and v_o^3 must be eliminated in order to get a closed-form solution, albeit simplistic, the overall gain of the filter may be used in conjunction with the above equation.

Recall the linear transfer function of this filter

$$v_o(j\omega) = \frac{-g_{11}/g_{41}}{1 + j\omega C/g_{41}} v_i(j\omega) \quad \text{Eqn 5.75}$$

Now, the higher order terms v_o^2 and v_o^3 may be eliminated by substitution of Eqn 5.75 into Eqn 5.74. The substitution of a linear solution into the nonlinear equation is quite legitimate and has been used extensively throughout this thesis, assuming the "Almost Linear" approximation is valid. Unfortunately, this is a case whereby bringing the v_o^2 and v_o^3 terms to the left-hand side of Eqn 5.76 (before putting it into it's final solved form) and driving it with the linear solution of Eqn 5.75 causes the error (an underestimation) associated with this method to become more substantial at higher frequencies where the frequency dependence becomes significant. Thus, this method used on $g_m - C$ filters in this way becomes more of an approximation at high frequencies. The magnitude of this error is not particularly or surprisingly large, as may be judged in upcoming simulations, since the transfer function itself is relatively well behaved and does not vary greatly with frequency.

Given that $v_o(j\omega) = i_{14}/j\omega C$, the resulting substitution yields an approximate solution

$$v_o(j\omega) = \frac{-g_{11}}{j\omega C} v_i(j\omega) + \frac{g_{12}}{j\omega C} [v_i(j\omega)]^2 + \frac{g_{13}}{j\omega C} [v_i(j\omega)]^3 - \frac{g_{41}}{j\omega C} v_o(j\omega) + g_{42} \left(\frac{g_{11}/g_{41}}{1 + j\omega C/g_{41}} \right)^2 [v_i(j\omega)]^2 - g_{43} \left(\frac{g_{11}/g_{41}}{1 + j\omega C/g_{41}} \right)^3 [v_i(j\omega)]^3 \quad \text{Eqn 5.76}$$

Re-arranging this into its final form yields

$$v_o(j\omega) = \frac{g_{11}/g_{41}}{1 + j\omega C/g_{41}} v_i(j\omega) + \frac{\left[g_{12} + g_{42} \left(\frac{g_{11}/g_{41}}{1 + j\omega C/g_{41}} \right)^2 \right] / g_{41}}{1 + j\omega C/g_{41}} [v_i(j\omega)]^2 + \frac{\left[g_{13} - g_{43} \left(\frac{g_{11}/g_{41}}{1 + j\omega C/g_{41}} \right)^3 \right] / g_{41}}{1 + j\omega C/g_{41}} [v_i(j\omega)]^3 \quad \text{Eqn 5.77}$$

Since some of the resulting harmonic distortion terms at multiples of the input frequency can be very low in amplitude, it may be confused with harmonics from the signal source. Furthermore, it is of interest to look at distortion products that lie in the passband and not the filter stopband where harmonics get filtered which is not accounted for in these equations. Thus the preferred intermodulation distortion terms of interest result in

$$hd(\omega) = \left| \frac{g_{11}/g_{41}}{1 + j\omega C/g_{41}} \right| V_I$$

$$imd(\omega_1 - \omega_2) = \left| \frac{\left[g_{12} + g_{42} \left(\frac{g_{11}/g_{41}}{1 + j\omega C/g_{41}} \right)^2 \right] / g_{41}}{1 + j\omega C/g_{41}} \right| V_I^2$$

$$imd(2\omega_2 - \omega_1) = \frac{3}{4} \left| \frac{\left[g_{13} - g_{43} \left(\frac{g_{11}/g_{41}}{1 + j\omega C/g_{41}} \right)^3 \right] / g_{41}}{1 + j\omega C/g_{41}} \right| V_I^3 \quad \text{Eqn 5.78}$$

where the inputs are both equal such that $V_{I1} = V_{I2} = V_I$ and both inputs are nearly at the same frequency, ω . This must be true for this equation to be a true approximation.

Clearly, the nonlinear contribution from the feedback transconductor is modified according to the gain of the filter. To best see this, consider the IMD products at low frequencies only.

$$\begin{aligned}hd(f) &= \frac{g_{11}}{g_{41}} V_I \\imd(f_1 - f_2) &= \frac{g_{12} + g_{42} (g_{11}/g_{41})^2}{g_{41}} V_I^2 \\imd(2f_2 - f_1) &= \frac{3g_{13} + g_{43} (g_{11}/g_{41})^3}{g_{41}} V_I^3\end{aligned}\tag{Eqn 5.79}$$

The second-order harmonic (i.e. IMD products also) whose nonlinear contributors are additive in nature contrasts with that of the third-order harmonic whose contributions to the overall nonlinearity of the filter are subtractive. In fact if the gain of the filter is unity (as is the case here regarding the fabricated filter) then at low frequency the third harmonic should nearly cancel out completely. Coupled with differential circuitry, it is then possible to cancel out both even- and odd-order nonlinearity, making $g_m - C$ filters more approachable to satisfy high-bandwidth, high-resolution filtering.

The low-frequency distortion characteristics of the low-pass filter were simulated (postlayout), compare extremely well with theory, and may be found in Appendix E, Section E.4. Also a greater appreciation through numerical example between the single and dual nonlinear transconductor theories may be found there.

5.5.1.4 Predicted Distortion from the Fabricated First-Order, Low-Pass Filter

Up to now, part of the thrust has been to explore and validate the theoretical approach taken by examining the low-frequency harmonic behavior of this filter. The original analysis however contained frequency dependence. As the focus of this study makes a transition from postlayout simulation to measured expectations and results, it is of interest to predict measured distortion levels at all frequencies. In this section, the predicted distortion is presented which is compared to the results from macromodel simulations and then finally compared to measurement.

Concentrating on the first-order low-pass filter, the theoretical distortion that should result in measurement at frequencies near DC may be found for a -23 dBV sinusoidal signal applied to

the input. Using Eqn 5.79 dictates that the expected IMD levels from the characterized OTA should be at frequencies well below the pole frequency

$$\begin{aligned}hd(f) &= -23\text{dBV} \\imd(f_1 - f_2) &= -70\text{dBV} \\imd(2f_2 - f_1) &= -7\text{dBV}\end{aligned}\tag{Eqn 5.80}$$

To confirm this, a macromodel simulation of this low-pass filter reveals the IMD levels

$$\begin{aligned}hd(f) &= -23\text{dBV} \\imd(f_1 - f_2) &= -70\text{dBV} \\imd(2f_2 - f_1) &= -132\text{dBV} \quad (\text{close to numerical floor})\end{aligned}\tag{Eqn 5.81}$$

as seen in Figure 5.26. As predicted by theory, the third-order IMD products (and harmonics)

Figure 5.26 FFT from macromodel simulation of the first-order low-pass filter utilizing measured OTA linearity coefficients.

nearly cancels out ideally while the second-order IMD products and harmonics is increased 6 dB here as expected due to the additive nature of both transconductor's nonlinearity.

The theoretical IMD levels, now as a function of frequency for -23 dBV inputs to the filter, are plotted up to the pole frequency as shown in Figure 5.27a) and Figure 5.27b) for second- and third-order IMD products respectively. It is compared with macromodel simulations of the filter. As may be seen in Figure 5.27a), there is excellent correlation between the second-order IMD product levels at low frequency. As frequency increases the nonlinear contribution from transconductor g_{m4} to the total second-order component starts to decrease as expected. The correlation between theory and simulation however departs slightly at higher frequencies. The cancellation of the third-order IMD products is generally nullified as expected and witnessed from Figure 5.27b) by the increase in the size of the IMD product with frequency. The cancellation of the theoretical third-order IMD products in the low megahertz range in this figure seems somewhat excessive when compared to the results of the macromodel simulation. It should be noted that firstly, the theoretical curve assumes perfect equality between the two transconductors. The results from the transient macromodel simulation has finite precision and accuracy which when factored in can cause the theoretical curve to increase markedly at frequencies where a great deal of nonlinear cancellation takes place. This is a gentle reminder of the importance in taking care of achieving proper accuracy by ensuring that enough sample transient points are discarded and that simulator accuracy options are in place. Secondly, the remaining discrepancy or error in approximation is a result of the lack of contributing terms as a result of not having solved the differential equation governing these transfer functions explicitly.

In reality, measured results would never achieve distortion levels this low due to circuit imbalances causing transconductance mismatch between g_{m1} and g_{m4} . This quickly becomes evident when attempting to tune the filter off-chip for 0 dB low-frequency gain. Through this process, it may be observed that the third-order IMD products varies considerably.

Taking the best case transconductance mismatch between differential pairs of 5% results in the theoretical plot of Figure 5.28a) and Figure 5.28b) for $imd(f_1 - f_2)$ and $imd(2f_1 - f_2)$ levels. This 5% figure was obtained through measurement by setting the currents (external to the chip) into the Gilbert gain cells as equal as possible and measuring the low frequency transfer function at relatively low input levels. Ideally, there would be no mismatch. However, considering the sources of error in the Gilbert gain cell discussed earlier, 5% is not unreasonable. The theoretical plots are compared with macromodel simulations including a 5% mismatch. Furthermore, the measured results are summarized on the same plots. As may be seen, the

Figure 5.27a Second-order IMD products. Theoretical vs. macromodel simulations for 0% transconductor mismatch

Figure 5.27b Third-order IMD products. Theoretical vs. macromodel simulations for 0% transconductor mismatch

Figure 5.28a

Second-order IMD products. Theoretical vs. macromodel simulations for 5% transconductor mismatch. This is compared to measured results

Figure 5.28b

Third-order IMD products. Theoretical vs. macromodel simulations for 5% transconductor mismatch. This is compared to measured results

measured results correspond quite well with the 5% mismatch theory and simulations. It should be noted that, not much beyond the pole frequency, the measured harmonics become enlarged due to the nonlinearity of the pole-splitting output stage becoming significant as well as erratic responses due to cable limitations and is therefore not shown. It should also be noted that it was a challenging task to try and find samples that demonstrate a 5% or less transconductor mismatch as this represents an extremely small yield of the total working die. This coupled with the task of tuning the chip for near equivalent current into the Gilbert gain cells made the overall process excessively time consuming.

In summary, the additive nature of the second-order IMD product from theory is corroborated by both simulation and measurement. The high third-order IMD product is due to incomplete cancellation due to mismatches in current levels, V_{BE} and resistor mismatch as well as secondary effects discussed earlier in the section on the Gilbert gain cell. As frequency increases, the cancellation of the third-order IMD product decreases as expected from the filtration of the nonlinearity in the feedback transconductor.

5.5.1.5 Biquad Filter Distortion

This method of determining the harmonics may now be extended to the biquad filter. Consider the simplified schematic of the biquad filter seen in Figure 5.29. The currents out of each transconductor may initially be considered as

Figure 5.29 Simplified representation of the biquad filter in terms of conventional OTAs and capacitors.

$$\begin{aligned}
 i_1 &= -g_{11}v_i + g_{12}v_i^2 + g_{13}v_i^3 \\
 i_2 &= -g_{m2}v_{o1} \\
 i_3 &= -g_{m3}v_o \\
 i_4 &= -g_{m4}v_i = g_{m4}v_o
 \end{aligned}
 \tag{Eqn 5.82}$$

Once again, a differential equation could be used to describe this nonlinear system. However, as discussed before, this complexity is avoided through approximation by using the differentiating theorem. Now,

$$\begin{aligned}
 v_{o1}(j\omega) &= \frac{i_{14}}{j\omega C_1} = \frac{i_1 + i_4}{j\omega C_1} \\
 &= \frac{-g_{11}}{j\omega C_1} v_i(j\omega) + \frac{g_{12}}{j\omega C_1} [v_i(j\omega)]^2 + \frac{g_{13}}{j\omega C_1} [v_i(j\omega)]^3 + \frac{g_{m4}}{j\omega C_1} v_o(j\omega)
 \end{aligned}
 \tag{Eqn 5.83}$$

and

$$v_o(j\omega) = \frac{i_{23}}{j\omega C_2} = \frac{i_2 + i_3}{j\omega C_2} = \frac{-g_{m2}}{j\omega C_2} v_{o1}(j\omega) - \frac{g_{m3}}{j\omega C_2} v_o(j\omega)
 \tag{Eqn 5.84}$$

Re-arranging the above equation yields

$$v_o(j\omega) = \frac{-g_{m2}/g_{m3}}{1 + j\omega C_2/g_{m3}} v_{o1}(j\omega)
 \tag{Eqn 5.85}$$

Solving this for $v_{o1}(j\omega)$ and substituting this into Eqn 5.83 leads to the final result. After re-arranging

$$v_o(j\omega) = \frac{\frac{g_{11}/g_{m4}}{1 + \frac{j\omega C_1 g_{m3}}{g_{m2} g_{m4}} + \frac{j\omega^2 C_1 C_2}{g_{m2} g_{m4}}} v_i(j\omega) - \frac{\frac{g_{12}/g_{m4}}{1 + \frac{j\omega C_1 g_{m3}}{g_{m2} g_{m4}} + \frac{(j\omega)^2 C_1 C_2}{g_{m2} g_{m4}}} [v_i(j\omega)]^2 - \frac{\frac{g_{13}/g_{m4}}{1 + \frac{j\omega C_1 g_{m3}}{g_{m2} g_{m4}} + \frac{(j\omega)^2 C_1 C_2}{g_{m2} g_{m4}}} [v_i(j\omega)]^3}
 \tag{Eqn 5.86}$$

At frequencies well below the resonant peak, the above equation is identical to Eqn 5.71 with the exception of the change in sign. Thus the harmonics are the same as in Eqn 5.72 which is relevant to a second-order continuous-time $\Sigma\Delta$ modulator.

As was done for the first-order low-pass filter, a deeper look into the nonlinearity of the biquad is necessary. It reveals that the transconductors g_{m2} and g_{m3} may be ignored. Their contributions to the overall nonlinearity of the filter is insignificant since the high loop gain suppresses nonlinearity beyond node v_{o1} . Once again, the insignificance of the effect of nonlinearity from g_{m2} and g_{m3} may easily be demonstrated through a macromodel simulation.

However, as was the case with the first-order low-pass filter, the transconductor g_{m4} can contribute significantly to the overall nonlinearity of the biquad. An extension of the above analysis through approximation may now be made. The current i_4 is now replaced by the power-series expansion

$$i_4 = -g_{41}v_x + g_{42}v_x^2 + g_{43}v_x^3 = g_{41}v_o + g_{42}v_o^2 - g_{43}v_o^3 \quad \text{Eqn 5.87}$$

since $v_x = -v_o$. Now

$$\begin{aligned} v_{o1}(j\omega) &= \frac{i_{14}}{j\omega C_1} = \frac{i_1 + i_4}{j\omega C_1} \\ &= \frac{-g_{11}}{j\omega C_1} v_i(j\omega) + \frac{g_{12}}{j\omega C_1} [v_i(j\omega)]^2 + \frac{g_{13}}{j\omega C_1} [v_i(j\omega)]^3 + \frac{g_{41}}{j\omega C_1} v_o(j\omega) + \frac{g_{42}}{j\omega C_1} [v_o(j\omega)]^2 - \frac{g_{43}}{j\omega C_1} [v_o(j\omega)]^3 \end{aligned} \quad \text{Eqn 5.88}$$

Once again, an approximation is now made as was done in the first-order low-pass filter case. In the interest of eliminating $[v_o(j\omega)]^2$ and $[v_o(j\omega)]^3$, the overall gain of the biquad filter may be used together with Eqn 5.88. Recall the linear transfer function of the biquad such that

$$v_o(j\omega) = \frac{g_{11}/g_{41}}{1 + \frac{j\omega C_1 g_{m3}}{g_{m2} g_{41}} + \frac{(j\omega)^2 C_1 C_2}{g_{m2} g_{41}}} v_i(j\omega) \quad \text{Eqn 5.89}$$

Eliminating the higher order terms $[v_o(j\omega)]^2$ and $[v_o(j\omega)]^3$ in Eqn 5.88 through the substitution of the above equation into it yields the intermediate form

$$\begin{aligned}
 v_{o1}(j\omega) = & \frac{-g_{11}}{j\omega C_1} v_i(j\omega) + \frac{g_{12}}{j\omega C_1} [v_i(j\omega)]^2 + \frac{g_{13}}{j\omega C_1} [v_i(j\omega)]^3 + \frac{g_{41}}{j\omega C_1} v_o(j\omega) \\
 & + \frac{g_{42}}{j\omega C_1} \left[\frac{\frac{g_{11}/g_{41}}{1 + \frac{j\omega C_1 g_{m3}}{g_{m2}g_{41}} + \frac{(j\omega)^2 C_1 C_2}{g_{m2}g_{41}}} }{1 + \frac{j\omega C_1 g_{m3}}{g_{m2}g_{41}} + \frac{(j\omega)^2 C_1 C_2}{g_{m2}g_{41}}} \right]^2 [v_i(j\omega)]^2 - \frac{g_{43}}{j\omega C_1} \left[\frac{\frac{g_{11}/g_{41}}{1 + \frac{j\omega C_1 g_{m3}}{g_{m2}g_{41}} + \frac{(j\omega)^2 C_1 C_2}{g_{m2}g_{41}}} }{1 + \frac{j\omega C_1 g_{m3}}{g_{m2}g_{41}} + \frac{(j\omega)^2 C_1 C_2}{g_{m2}g_{41}}} \right] [v_i(j\omega)]^3
 \end{aligned}$$

Eqn 5.90

Solving Eqn 5.85 for $v_{o1}(j\omega)$ and substituting this into the above equation yields, after re-arranging

$$\begin{aligned}
 v_o(j\omega) = & \frac{g_{11}/g_{41}}{1 + \frac{j\omega C_1 g_{m3}}{g_{m2}g_{41}} + \frac{(j\omega)^2 C_1 C_2}{g_{m2}g_{41}}} v_i(j\omega) - \frac{[g_{12} + g_{42}(T(j\omega))^2]/g_{41}}{1 + \frac{j\omega C_1 g_{m3}}{g_{m2}g_{41}} + \frac{(j\omega)^2 C_1 C_2}{g_{m2}g_{41}}} [v_i(j\omega)]^2 \\
 & - \frac{[g_{13} - g_{43}(T(j\omega))^3]/g_{41}}{1 + \frac{j\omega C_1 g_{m3}}{g_{m2}g_{41}} + \frac{(j\omega)^2 C_1 C_2}{g_{m2}g_{41}}} [v_i(j\omega)]^3
 \end{aligned}$$

Eqn 5.91

where $T(j\omega) = (g_{11}/g_{41}) / \left[1 + \frac{j\omega C_1 g_{m3}}{g_{m2}g_{41}} + \frac{(j\omega)^2 C_1 C_2}{g_{m2}g_{41}} \right]$. The resulting harmonics are

$$\begin{aligned}
 hd(\omega) &= \left| \frac{g_{11}/g_{41}}{1 + \frac{j\omega C_1 g_{m3}}{g_{m2} g_{41}} + \frac{(j\omega)^2 C_1 C_2}{g_{m2} g_{41}}} \right| V_I \\
 imd(\omega_1 - \omega_2) &= \left| \frac{\{g_{12} + g_{42}(T(j\omega))^2\}/g_{41}}{1 + \frac{j\omega C_1 g_{m3}}{g_{m2} g_{41}} + \frac{(j\omega)^2 C_1 C_2}{g_{m2} g_{41}}} \right| V_I^2 \\
 imd(2\omega_2 - \omega_1) &= \frac{3}{4} \left| \frac{\{g_{13} - g_{43}(T(j\omega))^3\}/g_{41}}{1 + \frac{j\omega C_1 g_{m3}}{g_{m2} g_{41}} + \frac{(j\omega)^2 C_1 C_2}{g_{m2} g_{41}}} \right| V_I^3
 \end{aligned}
 \tag{Eqn 5.92}$$

which, well below the resonant peak frequency, is identical to the first-order low-pass filter harmonics (below its cutoff frequency) as seen in Eqn 5.79. Like the first-order low-pass filter, the biquad was also simulated to ensure that Eqn 5.79 holds true at low frequencies near DC, as seen in Appendix E, Section E.5.

5.5.1.6 Predicted Distortion in the Fabricated Biquad Filter

Once again, the characterized OTA linearity coefficients found earlier may be used to calculate the theoretical distortion levels from the biquad filter that should result in measurement. As was done in the case of the first-order low-pass filter, the results of the biquad filter macromodel simulations are plotted against the theoretical intermodulation distortion products as a function of frequency using the standard -23 dBV input levels as before. Pragmatically, like the first-order case, a mismatch between the transconductors causes the IMD levels to depart from ideally 0% mismatch. Once again, a best case 5% mismatch between transconductors g_{m1} and g_{m4} may be used and the theoretical IMD products plotted. Figure 5.30a) and Figure 5.30b) show this along with macromodel simulations (that include the 5% mismatch) and the measured results.

Like the first-order low-pass filter case, the second-order IMD characteristics as a function of frequency loosely mimic the transfer function of the filter while the third-order characteristics grow by virtue of less distortion cancellation with frequency. Considering that the simple theory is an approximation, fairly good agreement exists between it and macromodel simulations

Figure 5.30a

Biquad second-order IMD products. Theoretical vs. macromodel simulations for 5% transconductor mismatch between g_{m1} and g_{m4} . This is compared to measured results.

Figure 5.30b

Biquad third-order IMD products. Theoretical vs. macromodel simulations for 5% transconductor mismatch between g_{m1} and g_{m4} . This is compared to measured results.

of the biquad. The second-order IMD products match well, while the third-order IMD products tend to vary more near the natural frequency of the filter. This is not surprising since any error is squared for the second-order case while the error is cubed for the third-order case. This error is expected and is a result of not having explicitly solved the differential equation that governs these harmonics.

With respect to the plots, it should be immediately noticeable that a difference exists between the theoretical/macromodel simulations and the resulting curves from measurements of both the second- and third-order IMD products. This is because the natural frequency of the biquad filter was measured at 36 MHz, not 31 MHz as predicted. Since this difference is not significant, it does not diminish the comparison.

5.6 The First-Order Continuous-Time Oversampled A/D

5.6.1 Introduction

The focus of discussion now shifts onto the distortion characteristics of the $g_m - C \Sigma\Delta$ modulators. Since feedback is relied upon through ideal, linear current steering (not nonlinear transconductance), the simpler "single nonlinear transconductor" theory may be used to describe nonlinearity and predict distortion in the first- and second-order oversampled A/Ds here. This means that the second-order distortion products should be less compared to the filters, however the third-order components cannot cancel out.

This circuit was run in single-ended mode so as to allow a study of both the even- and odd-order harmonics since when run differentially, the even-order harmonics, would nearly cancel out.

5.6.2 Quantizer Clock Rate

The first-order continuous-time $\Sigma\Delta$ modulator (CTSDM) was tested at a clock frequency of 160 MHz, slightly less than the originally designed clock frequency. The reduction in speed,

as required in both simulation and measurement was necessary due to two factors. First, since the measured UGBW of the integrator was less than designed, a reduction in the clock from $2\pi 36.2 \text{ MHz}$ (227 MHz) to $2\pi 31 \text{ MHz}$ (195 MHz) was necessary to keep the gain coefficient α_1 equal to unity. This would also mean that the switched current levels (in each branch of the differential pair) would have to be reduced to

$$\begin{aligned}
 I_O &= \frac{\Delta V_{fb} C}{T} \\
 &= \frac{(1 \text{ V}) (2 \times 10^{-12})}{1 / (195 \times 10^6)} \\
 &= 390 \mu\text{A}
 \end{aligned}
 \tag{Eqn 5.93}$$

The ΔV_{fb} in the above equation should be recognized as being equivalent to the $\alpha_4 V_{ref}$ term in the sampled-data oversampled A/D. ΔV_{fb} , as discussed before, should ideally be set to 1 V for good headroom during integration. As the desired V_{ref} here is 1 V, then $\alpha_4 = 1$ and as such, the low-frequency gain of the A/D would be $\alpha_1 / \alpha_4 = 1$ by virtue of the given, measured transconductance that set α_1 . As long as this ratio remains equal to unity, there is a basis for direct comparison between the filters (single nonlinear transconductor theory) and the oversampled A/Ds (i.e. the distortion products should equal under these terms).

However, a second reduction in quantizer speed was necessitated due to the delay inherent in the quantizer. Even at the lower speed of 195 MHz, it was found at the time of measurement that poor noise shaping and generally incorrect amplitude responses resulted at input signal levels near idle channel. These problems were completely avoided by further reducing the quantizer clock frequency a little further to 160 MHz and applying a DC offset at the input. This means that the reference voltage, which generally defines the maximum input voltage to the A/D, has effectively increased from $\Delta V_{fb} = 1 \text{ V}$ to

$$\begin{aligned}
 \Delta V_{fb} &= \frac{I_O T}{C} \\
 &= \frac{390 \times 10^{-6}}{2 \times 10^{-12}} \frac{1}{160 \times 10^6} \\
 &= 1.2 \text{ V}
 \end{aligned}
 \tag{Eqn 5.94}$$

One could further reduce the current I_o in the current-steered differential pair to bring V_{ref} back down to 1 V, however $\alpha_1 = g_{m1}T/C = 1.2$ now and would upset the α_1/α_4 desired ratio unity. Thus, it is advantageous to leave the current level set as is. The reduction in quantizer speed also allows a comparison in harmonics with the filters to be more approachable since the effective reference voltage V_{ref} has increased slightly. This is because bit-stream saturation and the effects of integrator clipping also causes harmonics as discussed in Chapter 2.

Figure 5.31 shows the entire spectrum for the measured first-order coder with a low amplitude input. As long as the extended integration range on the capacitor C does not upset the operation of the modulator, (i.e. from the premature saturation of transistors in the output stage of the OTA) then an adjustment must be made is to raise the measured spectrum in its entirety by 1.5 dB (1.2x). This is so a 0 dB input signal to the A/D relative to $1V_{pk}$ corresponds to a 0 dB output signal. Keeping this in mind, Figure 5.31 corresponds to the expected theoretical spectrum after also considering the gain of the ECL buffer that unloads signals off-chip. (More on these specifics later).

5.6.3 The Effects of OTA Finite Gain in the CTSDM

Before proceeding with the theoretical distortion that should be found in the $\Sigma\Delta$ modulators, it is prudent to consider how finite gain effects from the OTA manifests itself in continuous-time oversampled A/Ds. In general, leaky integration occurs in continuous-time $\Sigma\Delta$ modulators and as such produces a zero in the noise-shaped spectrum as discussed in Chapter 4.

The continuous-time oversampled A/D can, in essence, be reduced down to a type of sampled-data system since it is clocked. As discussed earlier, the only operational difference between a continuous-time and sampled-data implementation lies in the integration process. Simply put, the outputs of the integrators are equal, at the end of each clock cycle, regardless of the implementation so long as equivalent architectures are used. Thus, by virtue of their equivalence, the analysis provided in Chapter 4 on this topic is valid here and need not be re-derived [Sho95].

In amplifier-based structures, the finite gain of the opamp is responsible for leaky integration. In conventional $g_m - C$ based structures, any resistance (such as amplifier output resistance) around the integration capacitor is responsible for this effect. The implementation here utilizes

Figure 5.31 Measured spectral response of the first-order continuous-time $\Sigma\Delta$ modulator. (-50 dBV input signal, $f_i = 157\text{ MHz}$)

Figure 5.32 Simplified diagram of the OTA showing the folded-cascode amplifier feeding current into the Miller integration output stage.

what has come to be termed a “Miller Integration” output stage, as shown in Figure 5.32. Here, there is ideally no resistance around the capacitor, however, the finite gain of the output stage is wholly responsible for the leaky integration that takes place.

A 256 kPoint FFT of a postlayout simulation of the first-order continuous-time $\Sigma\Delta$ modulator (CTSDM) is shown in Figure 5.33 and is further zoomed into the baseband region for clarity. Clearly, the zero in the spectrum of the quantization noise may be seen. Superimposed upon the FFT is the theoretical noise-shaped spectrum. This theoretical spectrum was arrived at by using the mathematical derivation in Chapter 4, modified for the dBm scale, increased reference voltage and ECL output driver span just as the plotted FFT was. Furthermore, it is assumed that the gain of the quantizer is unity — a quantity that markedly changes the magnitude of the quantization noise floor.

The gain of the OTA’s output stage from postlayout simulation was 45 dB (see Figure 5.17) and this is the value used in the calculation. As may be seen in Figure 5.33, the flattened quantization noise spectra near DC is comparable to the theoretical value expected.

Figure 5.33

256Kpoint FFT of CTSDM postlayout simulation results (baseband only). Superimposed upon it is the theoretical quantization noise spectrum including finite gain effects. The gain of the output stage is 45 dB.

5.6.4 Measured Spectrum and Finite Gain Effects

The fabricated, first-order $\Sigma\Delta$ modulator was tested single-ended at a nominal clock frequency of 160 MHz with the current source of the feedback differential pair set at 390 μA off-chip. The successful operation of the CTSDM is shown by observing the characteristic first-order, noise-shaped spectrum seen in Figure 5.31 with a small, -50 dBV input at 2 MHz applied to the input of the coder. A low-valued input is used here to demonstrate that proper noise-shaping and good operation is taking place—a difficulty that was discussed earlier. For this plot only, the clock frequency was decreased a few percent so that the peak near half the clock frequency may be observed, indicative of low inputs and proper operation. Any tonal behavior indicative of first-order coders that may be observed in either simulation or measurement may be mostly eradicated by the use of a small DC offset applied to the input.

A -50 dBV input is expected to yield a -47 dBm spectral tone at 2 MHz after all the conversions, discussed later, are applied. This is in fact what is seen in Figure 5.31. The theoretical spectrum, using the measured gain of the output stage at 34 dB so as to include finite gain effects, may be seen in Figure 5.34a). Here, the gain of the quantizer K , as found from simulation, was -3 dB. The gain K from experiment was not measured since the load on the output of the integrator would upset the operation of the coder, assuming that the output of the integrator would have even been available to a pin off-chip. As may be seen, the measured (from Figure 5.31) and theoretical spectra match closely. (A higher resolution theoretical plot for the baseband only is shown in Figure 5.34b), to be used for future reference in an upcoming section showing with greater detail how well the measured quantization noise corresponds to theory.)

5.7 Distortion in the Continuous-Time Oversampled A/D

5.7.1 Theoretical Distortion and Comparison with Postlayout Simulation

As was discussed earlier, this topic has been confined to low frequencies only (i.e. baseband). This was done to avoid the difficulty in making high-frequency measurements of the quantizer gain K . A logical extension to high frequencies however may have been done as seen in Chapter 4. The main focus here is the distortion that arises from applied signals to the input of the A/D and not the intermodulation of high-frequency spectra as was the case in the previous chapter.

The harmonic levels that come about from signals applied to the input of the A/D are theoretically the same as those that result from the single nonlinear transconductor first-order, low-pass filter. The signal harmonics, ignoring frequency effects, are

Figure 5.34a

Theoretical spectrum expected from the modulator with 34 dB of gain from the output stage (Note that $\sin x/x$ effects are not accounted for in this plot)

Figure 5.34b

Baseband region only (of above plot).

$$\begin{aligned}
 hd(f) &\approx \frac{g_{11}}{g_{m4}} V_I \\
 hd(2f) &= \frac{1}{2} \frac{g_{12}}{g_{m4}} V_I^2 & imd(f_1 - f_2) &= \frac{g_{12}}{g_{m4}} V_{I1} V_{I2} \\
 hd(3f) &= \frac{1}{4} \frac{g_{13}}{g_{m4}} V_I^3 & imd(2f_2 - f_1) &= \frac{3}{4} \frac{g_{13}}{g_{m4}} V_{I1} V_{I2}^2
 \end{aligned}$$

Eqn 5.95

where g'_{m4} is an equivalent transconductance to the quantity $g'_{m4} \equiv I_o / \Delta V_{fb}$ in the oversampled A/D where I_o and ΔV_{fb} are equal to the quantities discussed earlier.

A postlayout simulation of the first-order coder was run. Two signals, separated by 1 MHz, was applied to the input of the coder. A 256 kPoint FFT was performed, the results of which are seen in Figure 5.35a).

Referring to the figure, the noise-shaped spectrum conforms well to theory. The inputs applied to the A/D are both -8 dBV in amplitude which correctly yields -5 dBm fundamentals in the FFT. This amplitude is as expected due to the dBV-to-dBm conversion coupled with the fact that the digital output from the quantizer's ECL buffer/pad driver has a span of $\pm 0.375V$. Also, the entire spectrum is low by 1.5 dB due to the heightened reference voltage ΔV_{fb} as a consequence of the aforementioned clock rate reduction. As a result and a convenient coincidence, the input in dB (relative to full scale, $1V_{pk}$) is nearly identical to the output in the spectrum in dBm.

It is now timely to consider simulated and measured results. Using the linearity coefficients found for the simulated OTA, the theoretical harmonic levels from a postlayout simulation of the first-order coder for large -5 dB (-8 dBV or $0.55 V_{pk}$) inputs would be

$$\begin{aligned}
 imd(f_1 - f_2) &= \frac{g_{12}}{g'_{m2}} V_{I1} V_{I2} = \frac{1.75 \times 10^{-6}}{310 \times 10^{-6}} (0.55)^2 = -58.4 dBV \text{ (at 1 MHz)} \\
 &= (-55.4 dBm \text{ expected on FFT}) \\
 imd(2f_2 - f_1) &= \frac{3}{4} \frac{g_{13}}{g'_{m2}} V_{I1} V_{I2}^2 = \left(\frac{3}{4}\right) \frac{4.58 \times 10^{-6}}{310 \times 10^{-6}} (0.55)^3 = -57.7 dBV \text{ (at 3 MHz)} \\
 &= (-54.7 dBm \text{ expected on FFT})
 \end{aligned}$$

Eqn 5.96

Figure 5.35a

256Kpoint FFT of the first-order coder postlayout simulation results superimposed upon by the theoretical quantization noise levels. The input signal levels are -8 dBV.

Figure 5.35b

Baseband region only. Harmonics and distortion products are just above the quantization noise levels. (Quantization noise leakage due to finite gain effects in the OTA.) Superimposed upon it is the theoretical quantization noise spectrum including finite gain effects. The gain of the output stage is 45 dB

The answers in parenthesis are the converted, expected intermodulation distortion levels that should be found on the FFT in the above figure. Note that -8 dBV is the amplitude of choice. Input amplitudes not much greater than this cause quantizer overload to affect the spectrum. Naturally, lower input amplitudes would cause harmonics to be buried in the quantization noise due to the relatively good linearity of the simulated OTA.

Comparing the theoretical to the simulated results, it is clear that the third-order, $imd(2f_2 - f_1)$ harmonic is buried in or comparable to the quantization noise as witnessed in the baseband region seen in Figure 5.35b). The second-order $imd(f_1 - f_2)$ harmonic appears to have a magnitude of -52 dBm, which is very close to the theoretical value calculated. Admittedly, the $imd(f_1 - f_2)$ harmonic level is too close to the quantization noise floor to say for sure that it is not simply a correlated tone that happens to reside at 1 MHz. However repeated simulations show the 1 MHz component at much the same level with neighboring tones changing frequency. Unfortunately, it is difficult to clearly demonstrate the effects of circuit nonlinearity at the postlayout simulation level. The size of the FFT cannot be increased very much without reaching memory limits. The minimal reduction in resolution bandwidth from a 512 kPoint FFT would not sufficiently clarify this ambiguity and it is estimated that four weeks would be required to run such a postlayout simulation given the computing capabilities available at the time. This simulation however does demonstrate one phenomenon quite definitively. It shows the effects of finite gain upon the noise-shaped spectrum quite well as discussed earlier. Proof of how circuit nonlinearity manifests itself in OTA-based oversampled A/Ds is nonetheless better demonstrated with measurements of the fabricated device, whose OTA nonlinearity is greater than the nonlinearity of the simulated OTA.

5.7.2 Measured Harmonic Distortion in the Fabricated First-Order Coder

Using the characteristic nonlinearity of the measured OTA it is possible to predict what harmonic levels should be present in the fabricated modulator. Using Eqn 5.95, the second- and third-order intermodulation distortion products expected from the first-order $\Sigma\Delta$ modulator (as well as the second-order modulator) may be calculated and plotted. Since the characteristic (measured) nonlinearity of the coder is considerably higher than the simulated one, the harmonics seen at the output of the coder may easily be seen.

Figure 5.36 Spectrum analyzer plot showing the baseband intermodulation products. The clock frequency is 160 MHz.

A sample of the measured intermodulation distortion is shown in Figure 5.36 for an input amplitude significant enough so that the resulting harmonics are above the noise floor. Before making a comparison between the expected and measured IMD products, it is judicious to comment on this spectral plot first.

First, the expected thermal noise levels are considerably lower than the quantization noise levels due prominently to finite gain effects. Secondly, it may be seen that the quantization noise level at low frequencies corresponds well with the expected quantization noise levels seen in Figure 5.34b), validating the calculation technique for the effects of finite gain. The obtrusive bump near DC in these plots is a residue of this type of spectrum analyzer and could not be suppressed or avoided and should not be mistaken for $1/f$ noise.

The expected IMD results may be plotted against the measured second- and third-order IMD products (compensating for all conversions discussed already) as may be seen in Figure 5.37a) and Figure 5.37b). (See Appendix F for more samples of spectrum analyzer plots demonstrating distortion at various inputs.)

Figure 5.37a Theoretical versus measured second-order IMD products from the first-order continuous-time $\Sigma\Delta$ modulator.

Figure 5.37b Theoretical versus measured third-order IMD products from the first-order continuous-time $\Sigma\Delta$ modulator.

Like simulations, the inputs here were kept below the -8dBV level to avoid the spectral contamination from quantizer overload effects. With reference to the figures, it is immediately noticeable that the measured second-order IMD products are larger than expected. Although the reason for this is unclear, there are several reasons why this may have occurred. One obvious answer is that the OTA fabricated on the $\Sigma\Delta$ modulator die had a larger second-order linearity coefficient than that of the stand-alone OTA. Secondly, upon reflection, the fact that a DC offset was applied to the input caused a shift in the OTA's operating point. Depending upon the size of the offset, this can significantly affect the linearity coefficient g_{12} , and most likely did. When square wave outputs have unequal slew rates, second-order distortion components result [Ris94]. In hindsight, if the ECL pad driver used to drive the bit-stream output off chip suffered from unequal slew rates, then it is possible that the second-order distortion components may have been augmented as a result.

Other possible reasons of why distortion may be larger than expected relate to the so-called ideal current-steered differential pairs used to provide feedback in the modulator. As this is a slew-rate limited current source, any imbalance or unevenness between the positive and negative slew rates simply produces a DC offset at the output of the coder. However, that is only true in the ideal case. In reality, successive integrations in one direction will not always produce a change in voltage equal to the desired ΔV_{FB} . Circuit nonidealities such as limited integration range due to finite rail voltages cause these limitations. The above effect alone occurs symmetrically and therefore produces odd-order distortion. If the slew rates are unequal, then the error associated with ΔV_{FB} will produce a DC offset that is signal dependent. The result is even-order nonlinearities.

Recall that a DC offset was applied to the input of the coder in order to overcome an observed phenomenon under idle channel conditions. Specifically, the spectral shape of the quantization noise became distorted and the magnitude of the signal at the output would be in error. Upon inspection, the bitstream output for the first-order modulator resembled that of a second-order coder under idle channel (i.e. 11001100). The reason for this relates to the use of non-return-to-zero (NRZ) feedback.

NRZ produces what amounts to a delay and an induced offset during integration that is nulled when the quantizer flips polarity as seen a from the simulation shown in Figure 5.38a). Assuming that the rise and fall times associated with the feedback control signal from the quan-

Figure 5.38a Matlab simulation of idle channel condition, showing the effect of delayed feedback. Here, the quantizer is resolving signals outside the band equal to $V_{band} - 4 \cdot SR \cdot delay_{quantizer}$.

Figure 5.38b Simulation where the initial voltage was just under 0V (within V_{band}).

tizer output are equal, a run of successive pulses of the same polarity (i.e. 111000 from large input amplitudes) cause subsequent integration to not accumulate error as is sometimes thought. If error did accumulate, this type of feedback architecture would exhibit odd-order nonlinearity. Simulations of ideal coders by Risbo [Ris94] in fact showed no difference between NRZ and RZ architectures where nonlinear distortion from this type of feedback is concerned. Rather the error that exists is a constant magnitude which depends upon the propagation delay of the quantizer. Given any sequence of pulses, this error is nulled out as stated above. Note that unequal rise and fall times causes even-order nonlinearities as it is akin to signal-dependent DC offsets.

However, if the output of the integrator straddles the quantizer threshold voltage (as it does in the case of idle channel - See Figure 5.38b), the initial delay causes a shortfall in the integrated charge which in turn results in a second successive pulse from the quantizer of the same polarity. The idle channel condition is a special case because it is possible to get caught in this 11001100 sequence, without breaking out of it. This is somewhat synonymous with deadbanding in that sufficient voltage at the input is unavailable to be properly encoded.

From above discussion, it is thus necessary to minimize this delay. This was the main reason the quantizer in experiment was clocked slower than designed, in order to keep the integration time-to-quantizer delay ratio high. Coupled with a DC offset, used to push the integrated voltage near the quantizer threshold away, allowed proper operation and good noise shaping at low input levels and under idle channel conditions.

It should be noted that there were instances during measurement when the coder was biased "just right" so as to cause the output bitstream to produce excessive third-order distortion. Although this was not too common, and more often than not was a consequence of operating the coder at too high a clock frequency, it is worth noting.

5.8 Summary and Conclusions

This chapter has covered the design of wideband $g_m - C$ filters and $\Sigma\Delta$ modulators. These designs draw upon a collection of circuit techniques integrated into a doubly-differential OTA, the use of which is novel in the above applications. The use of the Gilbert gain cell subdues

the large signal, nonlinear characteristics of the input differential pairs due to the nonexistence of virtual ground. The use of a pole-splitting output stage produces large DC amplifier gain necessary for the reduction of excess phase lead in the OTA. This reduces Q degradation in the biquad filter while at the same time high gain reduces quantization noise leakage in the $\Sigma\Delta$ modulators.

Complementary to these novel designs has been the study of noise and nonlinearity in the OTA and how these mechanisms propagate through to the output of the filters and modulators. This was necessary so that the achievable limits on dynamic range may be understood.

The original intention of the $g_m - C$ $\Sigma\Delta$ modulator designs was to demonstrate that oversampled A/Ds could be fabricated which exceed the low- to moderate-bandwidths they are typically accustomed to. The target here was to get the conversion speeds in the low MHz region which is greater than an order of magnitude over what was seen the time this circuit originally went to fabrication. Now that noise and nonlinearity is understood as a result of this study, it is worth looking at potential applications.

Wideband A/D conversion has classically been performed using large, flash A/Ds. They are often tasked with conversion rates between 5 MHz and 50 Mhz for applications such as video bandwidth compression, digital video transmission, reception, recording, digital image enhancement and radar signal analysis just to name a few [Gre84]. On the lower end of the applications scale is digital NTSC TV with a signal bandwidth as low as 3 MHz and Interactive Multimedia with required signal bandwidths as low as 1-2 MHz.

The noise that would exist in the baseband of either the first- or second-order continuous-time $\Sigma\Delta$ modulator at the output was earlier calculated to be $98.4 \text{ nV}/\sqrt{\text{Hz}}$. This means that a fundamental limit of 12 bits resolution could be maintained for signal bandwidths up to 6 MHz from noise alone. (A known application [BNR93] requires 6 MHz baseband with 6 bits of resolution.) As regards the first-order coder tested, (160 MHz clock) the signal-to-noise ratio from quantization noise can be shown to limit the resolution to just under 6 bits for such a wide bandwidth and may not be appropriate for the larger wideband applications. If the bandwidth of the first-order coder is limited to 2 MHz, as required for Video-On-Demand/Multimedia applications, a full 8 bits of resolution would result. Unfortunately, the existence of harmonic distortion reduces the dynamic range somewhat. In this case, input signals above

-12 dB (relative to full scale) cause a loss of dynamic range from nonlinearity. Hence over 6 bits of resolution is possible with 2 MHz signal bandwidths. Similarly, just over 7 bits of resolution is possible, when taking distortion and integrated quantization noise into account, when the signal bandwidth is limited to 1 MHz. Note that the resolution here depends upon the measured second-order distortion terms as the limiting mechanism. If the second-order distortion terms were closer to theory, which is possible through better design, then the resolution would be better than that quoted. Even though this is a simple, first-order modulator, it nevertheless ranks as a functional A/D for some applications. This clearly demonstrates the viability of these designs in general for high-speed, wideband applications. It goes without saying that a vast improvement (albeit the same distortion) would be possible with the second-order $\Sigma\Delta$ modulator.

A relatively simple strategy was developed in this chapter which allowed noise to be accounted for in closed-loop configurations of $g_m - C$ filters. An excellent correlation was found to exist between measured and theoretical noise in the filters as a result. From analysis, it was shown that there is a trade-off between the linear input range and the noise from the inner differential pairs referred to the input of the OTA, due to the gain as set by emitter degeneration. Base-current shot noise is kept small by the low impedances necessary to keep the Gilbert gain cells wide in bandwidth. However, other sources of noise may contribute from beyond the input stage such as the PMOS cascodes. The cascodes are in fact the major contributors of $1/f$ noise.

The oversampled A/Ds versions have less noise associated with them as a result of one of the Gilbert gain cells acting as a switch. Thus, only the current source providing the steered feedback current will contribute a collector-current shot noise component to the overall noise seen at the output of the modulators. This component replaced the other noise sources associated with the feedback transconductor, causing a reduction in overall noise as compared to the filters. Note however that the effects of finite gain in the pole-splitting output stage dominate noise at low frequencies, to be summarized later.

The linearity of the ideal OTA was found to be quite high as proven from postlayout simulations. In reality, the V_{BE} mismatch amongst transistors as well as a host of other effects are responsible for the higher nonlinearity present in the fabricated OTA. For example, differences exist causing excessive nonlinearity to appear due to parameter value errors (i.e. relative mis-

match) such as β and BJT ratio size errors that exist between the inner and outer differential pairs that make up the Gilbert gain cell. It is because of this that macromodel simulations had to be performed so as to allow a behavioral study of what the expected distortion would be in measurement. Fortunately, the variance in these errors in measurement was found to be not excessive. This allowed for the characterized OTA to be indicative of what would be found in the filters and $\Sigma\Delta$ modulators.

Regarding the filters, a single nonlinear transconductor theory was developed that led to the expected distortion at the output of the $\Sigma\Delta$ modulators. This also provided the starting point for theorizing distortion in the filters. Since the modulators are considered to have ideal, linear current feedback, only the first or feedforward transconductor need be considered nonlinear. This is however not true of the filters. In essence, because the nonlinearity from the feedback transconductor must be included as well, the amount of which depends on the transfer function, it too must be included when theorizing the overall nonlinearity of the filters. The results of this study showed the following.

For both the first- and second-order ideal low-pass filters, it was established through theory, postlayout and macromodel simulations that at low frequencies the third-order IMD levels cancel out completely. As the input frequency increases, the ability to cancel out the third-order distortion components decreases due to the frequency dependent transfer function of the filter affecting the feedback transconductor. The second-order IMD product levels are in contrast additive in nature, the amount of which also depends on frequency, as might be expected.

However, upon measurement, the third-order nonlinearities curtail or flatten at low frequencies rather than cancelling out completely. This is because the fabricated filters contains circuit nonidealities which lead to transconductor mismatches, as discussed earlier in the section on Gilbert gain cells. Measuring the low-frequency gain of the filter at low input amplitudes allowed the determination of a 5% mismatch between the feedforward and feedback gain-setting transconductor in both filters. This 5% was then integrated into theory which allowed an explanation as to the characteristic, third-order IMD levels seen as a function of frequency. The frequency dependence of the harmonic levels in the filters was verified with macromodel simulations of both filters which then compared well with measurement.

As a general comment, it is worth noting that the theoretical IMD product levels relate closely to both simulated and measured results at low frequencies. They start to depart slightly at higher frequencies. This is a consequence of not explicitly solving the differential equation that describes the nonlinear filters. The procedure used to eliminate the higher-order terms v_o^2 and v_o^3 in the derivation of the nonlinear transfer functions becomes less valid at higher frequencies. This clearly shows up as a discrepancy at these higher frequencies between the theoretical and measured (or simulated) results and is a limitation of this method, even though this may not necessarily be obvious from inspection of the results. In spite of this it is clear that a virtue of this theory is its ability to estimate what the IMD levels would be at low frequency with good accuracy. This is particularly true of the third-order IMD products. For example, by considering the pragmatic picture and including transconductor mismatch between the Gilbert gain cells, it was seen that the low-frequency third-order IMD products remains relatively constant. Without this theory, it would have been rather mysterious as to why the harmonics didn't cancel and why they would have existed as high in magnitude as they did.

An immediate suggestion to reduce the amount of distortion as a result of component mismatch in the OTAs would be to use common-centroid layout for the diodes in the pre-compression stage of the Gilbert Gain cell. This was not done in the designs shown here, a contributing factor that led to a higher degree of mismatch and characteristic distortion in the transconductor. Furthermore, it is possible that the emitter degeneration resistor is highly nonlinear in the V-I, outer differential input pair used in the Gilbert gain cell. This source of nonlinearity is not accounted for in postlayout simulations. In hindsight, a test structure to measure this source would have been prudent.

Varying degrees of difficulty were encountered during testing of these circuits—the reasons for these are predominantly process related. Although certain manufacturability issues may not have been addressed, most of the problems relate to the immaturity of the BiCMOS process used throughout this thesis. As regards the continuous-time circuits, all test circuits, filters and oversampled A/Ds functioned properly but one. It was disappointing that the second-order continuous-time $\Sigma\Delta$ was not operational. All samples tested suffered from common-mode feedback signal problems. Specifically, the common-mode voltage that is sensed at the output of the OTA in the second-order coder was erratic, which resulting in a mis-biased OTA. Several attempts with microsurgery to remedy the problem or even to manually set this voltage off-chip proved fruitless, mostly due to a lack of accessibility to specific nodes on-chip.

Although this problem was characteristic of some of the other circuits, at least enough working samples were obtained to meet the demands to successfully undergo testing in these other circuits. Unfortunately, a lack of time and samples precluded any further effort on the second-order coder. Nevertheless, the first-order $\Sigma\Delta$ modulator sufficiently demonstrated the design techniques and operational speed of these devices.

A comparison of how distortion proliferates between the sampled-data and continuous-time $\Sigma\Delta$ modulators may be made with reference to their constituent loop filters. As previously discussed, the harmonic distortion seen from the loop filter should be identical to the distortion seen in the oversampled A/D at low-frequencies. This has been proven through simulation and measurement previously [BW88] and was reiterated again in this thesis in the previous chapter for the opamp-based, sampled-data modulators. This statement is also true, in principle, of the continuous-time $\Sigma\Delta$ modulators. The distortion seen at the output of the coders presented here is only slightly different by virtue of the linear current sources which provide feedback. Naturally, the gain and delay associated with the quantizer causes a departure from the loop filter's transfer function at higher frequencies as demonstrated in the previous chapter.

Finite gain effects in the $C_m - C$ $\Sigma\Delta$ modulators were also demonstrated for the first-order coder. The theoretical calculations performed for finite gain effects here were drawn upon the spectral noise leakage calculations carried out in the last chapter regarding these effects in sampled-data modulators. This procedure was valid for two reasons. First, the mechanism responsible for leaky integration can predominantly be attributed to finite gain in the Miller integration, pole-splitting output stage. The effects from finite gain in voltage-mode amplifiers was covered in the last chapter and this analysis is perfectly valid here. Secondly, because the output of the continuous-time integrator is the same as the sampled-data integrator at the end of a clock cycle, there is an equivalence in operation for all practical purposes.

In conclusion, the design and many of the dynamic range limiting mechanisms present in $C_m - C$ filters and $\Sigma\Delta$ modulators were addressed. In the next and final chapter, possible directions for future work will be brought to the readers attention.

Summary and Conclusions with Suggestions for Future Work

6.1 Summary and Conclusions

The purpose of this thesis was two-fold. First, the mechanisms of noise and nonlinearity in oversampled A/Ds (and to a lesser extent filters) were studied. Second, the use of BiCMOS as a relatively new technology was exploited in an attempt to improve bandwidths and dynamic range in oversampled A/Ds, particularly with the aid of transconductance circuit techniques. In doing so, this thesis has advanced the understanding of noise and nonlinearity and has offered an innovative operational transconductance amplifier based continuous-time $\Sigma\Delta$ modulator.

The thesis starts by describing the motivation for such a study. A general introduction on oversampled A/Ds was provided and a comparison between sampled-data and continuous time modulators was presented. Generally, sampled-data modulators are valuable in many respects. They are small and temperature insensitive, and techniques exist to reduce $1/f$ noise and the effects of finite gain. However, they are limited by the sampling speeds with which signals settle in opamps and switches. Continuous-time circuits, on the other hand, offer improved

speed and the potential for better noise since aliasing does not occur, and in the case where sampling does take place, inherent filtering is in place to reduce this effect.

Through the course of the research, insufficient information on the design of $\Sigma\Delta$ modulators prompted a system-level simulation study to evaluate many of the mechanisms that limit the dynamic range in oversampled A/Ds in general. Simulations included the effects of integrator clipping, finite slew rate and settling time in opamps. This helped to ascertain the potential loss of dynamic range from intrinsically generated harmonics. The results showed that harmonics from circuit nonlinearity are the dominant ones for most of the input range.

Other basic simulations coupled well with theory, particularly on the topic of coefficient selection. This allowed a greater understanding on how to minimize certain dynamic range limitations such as integrator clipping and noise. One important theme that is re-iterated throughout the thesis is the many aspects of the gain of the quantizer. Typically, the gain of the quantizer is set to unity in the linearized model of oversampled A/Ds, a view which is limiting. Prompted by a discrepancy between simulation and this well known linearized model of the DISDM, investigation into this gain element was afforded.

Discussions on the question of circuit nonlinearity in oversampled A/Ds are nearly nonexistent in the literature, making this topic a focus of this thesis. In previous publications, simplistic equations have been published that are valid for low-frequencies only. This thesis expands the analysis (particularly of interest is the second-order intermodulation distortion product) throughout the entire spectrum. Simulations were performed on a nonlinear coder which showed a link between spurious tonal behavior and the intermodulation of high-frequency spectra (i.e. spurs). It is of interest to understand the mechanism and predict contamination in the baseband from the intermodulation of these spurs through nonlinearity. The spectra appear as a result of limit-cycle action associated with the nature of the oversampled A/D, and their frequency can be understood and described by simple math analysis.

The input-referred noise of $\Sigma\Delta$ modulators often quoted in the literature is kT/C based and typically only takes the first sampling capacitor into consideration, ignoring the transfer function of the coder. In this thesis, greater accuracy is obtained by accounting for noise from the feedback switched capacitor and the overall gain of the modulator. Furthermore, the input-referred noise of the opamp is determined through noise analysis, allowing a more complete es-

estimate of the total noise seen at the output of the modulator. $1/f$ and thermal noise of the opamp were simulated and compared to measurement.

The experimental modulator noise at low frequencies was found to be dominated by opamp finite gain effects. The effects of opamp finite gain cause an augmentation in the quantization noise floor by the existence of induced zeros. Some literature is available that discusses this effect, mostly qualitatively. An analysis was presented in this thesis that determines the effects of opamp finite gain on the transfer functions for the first- and second-order modulators, enhancing its accuracy along the way by including the gain of the quantizer.

To allow attaining more accurate signal and noise transfer functions, the gain of the quantizer was studied. Of particular interest was the high-frequency portion of the signal transfer function, where the gain of the quantizer is in question. As discussed, this gain is most often arbitrarily assigned to unity for simplicity. However it is relatively well known that high input amplitudes cause the gain to decrease. In this thesis the gain of the quantizer was also found to be frequency dependent. Furthermore, as the gain of the quantizer is a time-averaged quantity, the gain at any given instant may deviate from the norm in real time. Combining this wandering gain with a signal transfer function whose response is more sensitive at higher frequencies explains the ill-defined nature of the signal transfer function at those frequencies.

As a consequence of the frequency dependence of the quantizer gain, the high-frequency portion of the signal transfer function flattens out, resembling the action of a continuous-time filter rather than a sampled-data one. The modification in the behavior of the signal and distortion transfer functions is fundamental in achieving greater accuracy in the prediction of intermodulation distortion products found in the baseband from conventionally driven tones and high-frequency spurs. Using the characterized linearity coefficients of the opamp, theoretical distortion calculations compared well against measured results as tones at the input of the modulator were swept in frequency up to nearly half the clock frequency. The second-order intermodulation distortion products, as sourced from high-frequency spurs, also fared well against theoretically predicted values. Owing to the ill-defined nature of the signal and distortion transfer functions at these high frequencies, a bracket of predicted values validates the mechanism and the theoretical approach used to determine the intermodulation distortion products that contaminate the baseband.

As DC gain in the opamp suppresses the effects of nonlinearity at the output of the modulator, it is clear that in cases where DC gain has been traded-off for larger bandwidth, the dynamic range may be reduced as a result of spurs by means of this intermodulation mechanism.

Capacitor nonlinearity in sampled-data and continuous-time circuits has been a concern for many years. Analysis, in this thesis, has shown that with modern process technology, the contribution to the overall distortion at the output of the $\Sigma\Delta$ modulator is negligible compared to opamp nonlinearity.

The use of BiCMOS technology can heighten the bandwidth in which these circuits can operate. This technology coupled with the use of OTAs can allow even greater bandwidths to be achieved. In this spirit, a first-order transconductor-based oversampled A/D was fabricated and tested, in addition to first- and second-order low-pass $g_m - C$ filters. The design approach used a pole-splitting output stage in the OTA, which allows low output impedance devices such as BJTs to connect to them (i.e. the input to the comparator) and allows 90 degrees of phase shift across a wide band, making the filters less susceptible to Q degradation.

Little literature exists on the topic of noise propagation in doubly-differential closed-loop OTA configurations such as the $g_m - C$ filters used here. Similarly, electronic noise sources that are seen at the output of the continuous-time oversampled A/D need to be determined as well. Work was done to show how noise propagates in these circuits. One conclusion drawn from this exercise was that linear input range can be traded-off for better noise performance, since much of the noise seen at the input to these Gilbert gain cells is greatly increased from input-referring through the low-gain, V-I conversion stage.

Noise measurements and simulations validated the theoretical strategy and resulting predictions in the OTA and filters. The oversampled A/D demonstrated finite gain effects that caused the quantization noise to dominate over the electronic noise sources discussed above. This too was easily predicted by logical extension from the earlier analysis presented for sampled-data oversampled A/Ds. This is because the integration capacitor is in feedback as part of the pole-splitting output stage.

The high-frequency capability of these continuous-time circuits was demonstrated. Single-ended measurements exhibited cutoff frequencies of 31 MHz for the first-order low-pass filter and 36 MHz for the biquad, which are relatively close to the designed cutoffs. However, lin-

earity in transconductance-based circuits is a major concern due to the lack of local feedback around the amplifier necessary to suppress distortion at the output.

Inadequate literature and a lack of understanding exist on how nonlinearity in OTA-based filters propagates to the output. Although OTAs typically exhibit poor linearity, an advantage that has not been fully recognized is their constant distortion characteristics across much of the band. This thesis has made apparent that a major advantage of transconductance-based filters and oversampled A/Ds is the relatively constant distortion characteristics (i.e. depending only on the transfer function) that exist all throughout the passband, in contrast to the situation in opamp-based continuous-time filters and oversampled A/Ds. In general, this is because $g_m - C$ circuits operate on current rather than voltage. To confirm this and validate theoretical estimates, transient simulations and FFTs were performed on filters that contained macromodelled nonlinear OTAs. Fairly close measurements reinforced theoretical predictions. For the filters, it was found that even-order nonlinearities are additive while odd-order nonlinearities cancel out with proper design. In reality, transconductor mismatch prevents total cancellation, as was explored in theory and validated experimentally. A general conclusion can be made that wider dynamic range and wider bandwidth filters can be fabricated by using a more linear V-I conversion stage coupled with differential circuitry.

A technique was developed which allowed the determination of the linearity coefficients for the OTA. Unlike the straightforward process for the opamp, it was not possible to statically measure the current that exited the transconductor headstage as a function of voltage. Rather, the bandlimited harmonics that are generated for an input sinusoidal voltage, applied to the input of the OTA (in open-loop), allowed this determination.

The nonlinear behavior of continuous-time oversampled A/Ds was studied concurrently with the $g_m - C$ filters. Due to the use of current-steered feedback, the linearity of the modulator depends only on the linearity of the first feedforward transconductor.

The first-order modulator was operated at a clock frequency of 160 MHz, with signals typically applied at 2MHz. Throughout the course of testing, at the original designed speed of 227MHz, it was noticed that at low input or idle channel amplitudes, incorrect noise shaping and faulty output amplitudes resulted. It was shown that this depended upon the quantizer delay and the timed response from feedback. Reducing the clock to 160 MHz and allowing a DC

offset to be applied at the input eliminated this problem. The second-order intermodulation products were higher than theory predicted, most likely due to a change in the second-order linearity coefficient. This change would have taken place as a result of a shift in the OTA's operating point due to the DC offset. The third-order intermodulation components compared extremely well to the theory presented.

In terms of improving circuit performance, more linear V-I conversion techniques can be investigated to increase the linearity of the OTA. The linearity of the OTA depends on the outer differential pair along with mismatch amongst the active devices that make up the Gilbert gain cells. There are servo feedback techniques that force linearized voltage differences around the emitter degeneration resistor in the outer differential pair, in response to changing difference-mode voltages at the input. There are several variations of this classical instrumentation technique that have risen lately, giving viable alternatives [WMG93] which could be considered.

6.2 *Suggestions for Further Work*

Throughout the course of this thesis, the transfer functions and stability of the oversampled A/Ds were afforded greater accuracy by characterizing the gain of the quantizer. A range of values for such gain was empirically determined through simulation and measurement. It might be recommended that further work on modelling the quantizer, particularly the gain, could be undertaken. However, given the empirical data it would be useful to mathematically obtain a formula that describes this nonlinearity to the overall system. One such technique that may be employed makes use of describing-functions. Describing-functions [Oga70] could be used for the behavior of the quantizer gain as both a function of input amplitude and frequency, thus assisting in signal transfer function and intermodulation distortion calculations. For example, it was found that the average gain of the quantizer decreased with increasing frequency. The result, as witnessed in the signal transfer function of the DISDM, was a rather constant roll-off at frequencies beyond the resonant peak and right up to half the clock frequency. Even though this was a sampled-data system, a continuous-time biquad fit the profile better than the sampled-data one. By including a mathematical description of the quantizer nonlinearity, the sampled-data transfer function could have been kept by including a describing-function for the quantizer.

A second application of describing-functions regards the stability of the oversampled A/Ds. Once again, since the range of values for the gain of the quantizer was found, a multitude of Nyquist plots were generated that guaranteed stability. With describing-functions, a better method may be employed to determine stability. By separately plotting Nyquist graphs of both the transfer function of the loop filter and the describing-function of the nonlinear quantizer, information regarding the stability of the system may be ascertained. If the Nyquist plot of the loop filter transfer function encloses any portion of the plotted portion of the inverse describing-function, the enclosed area denotes regions of instability. From this, the conditions for instability may be graphically determined.

The method used to determine distortion in both the sampled-data and continuous-time oversampled A/Ds assumed that no filtering of the harmonics took place. For example, in order to simplify analysis, the two driving tones used in the analysis of intermodulation distortion were assumed to reside at frequencies such that one tone had the same filtering as the other tone. The second-order intermodulation components did not experience any filtering, as they fell into the baseband. However, had the tones been separated further, this assumption may not necessarily hold. Furthermore, when two tones are high enough in frequency and experiencing filtering, the third-order intermodulation distortion products also experience a further filtering component that is not accounted for in this simple analysis. Multiplying the distortion components by the filtering transfer function would allow for a simple estimate that would correct this deficiency.

For higher accuracy, with none of the limitations listed above, the use of Volterra series [Min80] to estimate harmonic distortion would be prudent. The analysis technique is mathematically complex and is somewhat less intuitive. The Volterra series method is limited to weakly nonlinear systems since if the solution requires numerical iterations, it may be divergent if the system is too nonlinear.

Finally, one dynamic range limitation that was not studied was the effect of jitter on continuous-time $\Sigma\Delta$ modulators. The clock source used in experimentation had low jitter characteristics and so jitter effects would not have been seen, particularly in this case where high quantization noise exists from finite gain effects at low frequencies. In higher order modulators, where thermal noise would dominate, it is important to consider the effects of jitter since

it directly affects feedback and the amount of integrated voltage that appears at the output of the integrators.

Appendix A

- A.1) C Program Listing of the Oversampled A/D Simulator
- A.2) DISDM Operation Including the Effects of Integrator Clipping
- A.3) Coefficient Selection Regarding Fundamental Operation
- A.4) Slew Rate and Settling Requirements in Sampled-Data Modulators

A.1 *Program Listing of the Oversampled A/D Simulator*

```
/* Bill Bereza May/90.
Simulation of second order delta-sigma modulator
Opamps have Slew Rate limiting and Finite Settling Effects added . */
/* computes the spectrum of the bit stream */

#include <stdio.h>
#include <math.h>
#include "complex.h"

#define npoints 16*1024
#define countoff 279395
#define fs 40.96e6
#define fo 10.0e3
#define BW 160.0e3
#define Vref 1.0
#define A1 1.0
#define A2 1.0
#define A3 1.0
#define A4 1.0
#define fft 1

float Viny[npoints+countoff],Vo1,V02,V01p,V02p,Vq,pi,mag[npoints+2],ampl;
float *Vin;
float noise,V01max,V02max,maxmag,ratio,snr,snrsum,vd;
float a0,a1,a2,a3,win;
complex bit_stream[npoints];
int i,k,fun,nbw;
extern float slew_settle();
```



```

main ()

{ Vin=&Viny[countoff];
    pi = 4.0*atan(1.0);
    aol=oa1;
/*    ampl = 0.0625;*/
    puts("Enter Amplitude in dB ");
    scanf("%f",&ampl);
    mag[npoints]=ampl;
    ampl=pow(10.0,(ampl/20.0));
    Vq = Vref;
    ratio=20*log10(ampl/Vref);
    fun = fo/fs*npoints;
    nbw = BW/fs*npoints;
    printf ("fo = %d BW= %d\n",fun,nbw);
    printf ("simulating candy's 2nd. order sigma-delta modulator\n");
    Vo1 = Vo2 = Vo1max = Vo2max = Vo1p=Vo2p= 0.0;
    for (i=-countoff;i<npoints;i++) {
        /* Quantizer */
        Vo1p=Vo1;Vo2p=Vo2;
        if (Vo2 >= 0.0) {
            Vq = Vref;
            if (i>=0){bit_stream [i] = Complex (1.0,0.0);}}
        else {
            Vq = -Vref;
            if (i>=0) {bit_stream [i] = Complex (0.0,0.0);}}
/* if (i>=0) {bit_stream[i]=Complex(Vo2,0.0);}*/
        Vin[i] = ampl*cos(2.0*pi*fo*i/fs);
        Vo1 = Vo1 - A1*Vin[i] + A4*Vq;
/* CLIPPING INTEGRATOR 1
        if (Vo1>2.5) Vo1=2.5;
        if (Vo1<-2.5) Vo1=-2.5;*/
        Vo1=slew_settle(Vo1,Vo1p);
/* CLIPPING INTEGRATOR 2
        if (Vo2>2.5) Vo2=2.5;
        if (Vo2<-2.5) Vo2=-2.5;*/
        Vo2=slew_settle(Vo2,Vo2p);

/*printf("Vo2= %f vd= %f a1= %f\n",Vo1,vd,a1);
        if ((i>0)&&(i<10)) printf("Vo1= %f del1= %f Vo2= %f del2= %f\n",Vo1,Vo1-Vo1p,Vo2,Vo2-Vo2p);*/
    }
/* printf ("Windowing the data 4term BH \n");*/
/* windowing data with 4-sample blackman-harris window obtained from
    harris's paper eqn (33) */
/* for (i=0;i<npoints;i++) {
    win = 0.3635819 - 0.4891775*cos(2.0*pi*((float)i/(float)npoints))+0.1365995*cos(4.0*pi*((float)i/(float)npoints))-

```

```

0.0106411*cos(6.0*pi*((float)i/(float)npoints));
bit_stream[i] = RCmul(win,bit_stream[i]);
}*/

printf("taking fft of bit stream\n");
four1 (&bit_stream[0],npoints,fft);
for (i=0;i<npoints;i++) mag[i] = Cabs (bit_stream[i]);
for (i=0;i<npoints;i++) {
    mag[i]=mag[i]/((float)npoints)*4.0;
if (mag[i]!=0.0)
    mag[i]=20*log10(mag[i]);
    else mag[i]=mag[i-1];
}

ampl=mag[fun];
mag[npoints]=ampl;
snrsum=0.0;
for (i=1;i<fun-2;i++) snrsum=snrsum+pow(10.0,(mag[i]/10.0));
for (i=fun+2;i<nbw;i++) snrsum=snrsum+pow(10.0,(mag[i]/10.0));
snr=mag[fun]-(10*log10(snrsum));
puts("*****");
puts(" ");
puts(" *** SNR = ***");
printf(" *** %8.4f ***\n",snr);
puts(" ");
puts(" ");
puts("*****");
puts(" AMPLITUDE = :");
printf(" %8.4f\n",ampl);
mag[npoints+1]=snr;
write_array ("mag.dat",mag,npoints+2);
/*system ("rsh spock matlab < splot.m >& crapout");*/
}

```

```

float slow_settle(v,vp)
#define tf 1e-12
#define fgbw 100e6
#define SRp 250e6
#define SRn -250e6

double v,vp;
{
double SRpos,SRneg,newv,tau,delv,Vs,Ts,Tx,T,Vsr,Vexp;
SRpos=SRp;SRneg=SRn;
T=1/fs;
tau=1.0/(2.0*pi*fgbw);
delv=v-vp;

```

```

if (delv>=0){
  Vsr=SRpos*tf;
  Vexp=delv*(1-exp(-tf/tau));
  if (Vsr>=Vexp)
    {
      delv=delv*(1-exp(-T/2/tau));
      newv=vp+delv;
/*printf("The Exponential NewV= %f and the old value was %f\n",newv,v);*/
      return newv;
    }
  else {
    Vs=delv-tau*SRpos;
    if (Vs<0) puts(".....Vs is Negative...");
    Ts=Vs/SRpos;
    Tx=Ts+tau*log(tau*SRpos/delv);
    if (Tx<0) puts("...Negative time exists ->Tx");
    if (T/2>Tx) delv=delv*(1-exp(-(T/2-Tx)/tau));
    else delv=SRpos*T/2;
    newv=vp+delv;
/*printf(" The SRpos + Settled NewV= %f and the old value was %f\n",newv,v);*/
    return newv;
  }
}
else {
  Vsr=SRneg*tf;
  Vexp=delv*(1-exp(-tf/tau));
  if (Vsr<=Vexp)
    {
      delv=delv*(1-exp(-T/2/tau));
      newv=vp+delv;
/*printf("The Exponential NewV= %f and the old value was %f\n",newv,v);*/
      return newv;
    }
  else {
    Vs=delv-tau*SRneg;
    Ts=Vs/SRneg;
    Ts=fabs(Ts);
    Tx=Ts+tau*log(tau*fabs(SRneg)/fabs(delv));
    if (Tx<0) puts("...Negative time exists ->Tx");
    if (T/2>Tx) delv=delv*(1-exp(-(T/2-Tx)/tau));
    else delv=SRneg*T/2;
    newv=vp+delv;
/*printf(" The SRneg + Settled NewV= %f and the old value was %f\n",newv,v);*/
    return newv;
  }
}
}
}
}

```

A.2 DISDM Operation Including the Effects of Integrator Clipping

For completeness, it is necessary to consider the effect of integrator clipping. Due to the finite rail voltages, the integrator output voltages in the DISDM are limited. Simulations were run with the imposition of such limits, at $\pm 2.5V$, in an attempt to determine how performance is affected. The results of such an exercise reveal that harmonics persist at lower input levels as a consequence of clipping, which thus degrade the SNR. An example is shown in Figure A.1)

Figure A.1 16 Kpoint FFT of the output bit-stream. (-3 dB Input). Integrator clipping is included

for the -3 dB input case which may be compared to the ideal modulator simulation of the same input amplitude in Figure 3.2b). A comparison is made between the unclipped modulator versus the clipped modulator in a dynamic range plot (SNR vs. Input) as shown in Figure A.2a) and Figure A.2b). The main difference may be seen as a shift in the maximum peak SNR when comparing these two plots. This results in a reduction in the dynamic range by several dB in the clipped integrator case. At even lower input levels, integrator clipping no longer occurs and the dynamic range plots merge at around the -10 dB level for the degenerate case. It

Figure A.2a

Dynamic range plot (SNR vs. Input) for the ideal modulator.

Figure A.2b

Dynamic range plot for the modulator that include the effects of integrator clipping.

should be noted that the variance in the SNR determined at each input level may be reduced by increasing the size of the FFT. This however is computationally expensive.

A.3 *Coefficient Selection*

There are several factors that must be considered when attempting to set values for the gain coefficients. These include the fundamental operation of the modulator, electronic noise, the way in which such noise gets through to the output of the modulator, and stability. Ultimately, the choice determines the quantization noise transfer function. The following simulations use -18 dB as the input amplitude to avoid integrator clipping and keep the modulator well into in the linear region. Figure A.3) depicts a simulation of the modulator at this level for reference.

A.3.1 *Fundamental Modulator Operation*

A.3.1.1 *Coefficient α_1*

The gain coefficient α_1 (in Figure 3.1) effectively scales the input signal before it reaches the loop. Considering that input-referred noise occurs at the input of the first integrator, decreasing α_1 causes an automatic loss of dynamic range. Furthermore, the quantization noise transfer function is also immune to any change in α_1 while the input experiences attenuation. This also may be seen directly from Eqn 3.1.

In practice, α_1 is often scaled down in tandem with α_4 to avoid excessive integrator saturation. As seen from Section A.2 and Figure A.2b), the loss of dynamic range due to clipping must be ascertained so as not to attenuate α_1 excessively.

A.3.1.2 *Coefficient α_2*

Intuitively, the gain of the quantizer may be thought of as being able to compensate for variations in α_2 and α_3 . A robust explanation will be given later when probing deeper into the behavior of the gain of the quantizer and how it affects the signal and noise transfer functions since K and coefficient values are inter-related. Taking this for granted, it would seem that reducing the value of α_2 is advantageous in that the second integrator experiences a reduction in integrator saturation due to lower accumulated voltage. Figure A.4a) shows the noise-shape

Figure A.3 16 Kpoint FFT that will be used as a reference for comparison with other simulations.

Figure A.4a FFT with coefficients α_2 is reduced to 0.5.

Figure A.4b FFT with $\alpha_2 = 0.5$ and $\alpha_3 = 0.5$

spectrum for a -18 dB input signal for the case where $\alpha_2 = 0.5$ (while the other gain coefficients remain at unity). Comparison with Figure A.3) shows, for all intents and purposes, no difference in SNR, since at an input of -18 dB the modulator does not experience internal clipping. Similarly, Figure A.4b) depicts the output spectrum where both α_2 and α_3 are reduced. Once again, there is no significant difference in SNR at the -18 dB input level as expected. However, as the input increases to the point where clipping starts to become significant, an increase in SNR can be achieved through the reduction of the α_2 and α_3 coefficients. The simulations presented here were kept low in input amplitude on purpose to demonstrate that the gain of the quantizer absorbs differences in the gains α_2 and α_3 on a qualitative level.

A.3.1.3 Coefficient α_3

As can be seen from the transfer function of Eqn 3.1, changes in α_3 cause a pole to shift. This is evident at high frequencies only. Figure A.5 shows a system simulation with $\alpha_3 = 0.5$ and input amplitude at -18 dB. There is no significant change in SNR. This is expected since both the signal and the quantization noise at moderately low frequencies are attenuated by the same amount as seen from Eqn 3.1. However, close inspection reveals that the quantization noise peak has shifted from approximately 3 MHz in Figure A.3) to 1.5 MHz in Figure A.5). This result is equivalent to what a reduction in K would produce. (Discussed in Chapter 3.)

A.3.1.4 Coefficient α_4

Consider the low-frequency gain of the structure as shown in Eqn A.1 where K is assumed to be unity,

$$V_o = \frac{\alpha_1 V_i}{\alpha_4} + \frac{(1 - z^{-1})^2 e_o}{\alpha_2 \alpha_4} \quad \text{Eqn A.1}$$

As may be seen, the gain of the modulator is α_1/α_4 . Since the input signal and spectrally shaped quantization noise are both divided by α_4 , no significant difference in SNR is expected when α_4 is either increased or decreased. Simulation verifies this to be true.

Figure A.5 FFT with varied coefficients. Note the high-frequency noise is pushed towards the baseband.

A.4 Slew Rate and Settling Requirements in Sampled-Data Modulators - A Simulation Study

Simulations were performed that allowed the output of the opamp to experience slew rate limiting followed by a linear settling process analogous to single-time constant (single-stage) opamps. It is understood that unless the opamp has critically damped characteristics, the results are only an estimate when two-stage opamps are used.

This topic is best explained through the use of an example. Figure A.6 depicts the SNR versus input (dynamic range) plot of an ideal modulator. The input signal is -88 dB when 0 dB SNR is reached, which may loosely approximated as the dynamic range. As a starting point, this corresponds to 14.6 bits of resolution, translating to an allowed 0.00398% settling error (i.e. 99.996% settling at the output of the integrators). Allowing this to be the largest error as a guide [RVR⁺90], then for any given clock frequency, typically set for quantization noise considerations, the necessary UGBW of the opamp may be found, partially from

$$\tau = \frac{I_{UGBW}}{\beta} = \frac{1 + C_{in}/C_I}{\omega_{UGBW}} \quad \text{Eqn A.2}$$

For the following calculation the clock is kept at 10.24 MHz so comparisons may be made with the ideal modulator simulation. In this example, the maximum amount of slewing time T_s is arbitrarily assumed to take 30% of the integration time $T/2$. The UGBW that the opamp must have to settle according to [RVR⁺90], is then calculated as follows:

A 10.24 MHz clock has integration time $T/2 = 48.8nS$. Also $T_s = 0.3 (T/2) = 14.6nS$.

For 2 V excursions, this translates to a required slew rate of 137 V/ μ S. To settle to 0.00398% in the remainder of the integration time, the time constant of the integrator is found from the settling error, $Error_{settling}$,

$$Error_{settling} = e^{-(V_{settle})/\tau} \quad \text{Eqn A.3}$$

so that

$$e^{-(T/2 - T_s)/\tau} = 39.8 \times 10^{-6} \quad \text{Eqn A.4}$$

Figure A.6 Dynamic range plot of the ideal coder.

Solving for τ yields 3.37 nS or $1/(2\pi\tau) = 47\text{MHz}$. Note that the UGBW of the opamp must be twice that (i.e. 94 MHz) in consideration of Eqn A.2, assuming that the ratio of feedforward to integration capacitance is equal to 1.

Simulations were performed incorporating the slew rate and settling limitations as above. As expected, there is no difference between the ideal dynamic range plot (solid line) and the nonideal modulator with the above limitations, as shown in Figure A.7a). In fact, allowing the slew rate to be halved (Figure A.7b) has an insignificant effect. Through simulation, the slew rate may take up as much as 80% of the integration time (Figure A.7c) before a noticeable difference is seen at the high input amplitudes. Any further degradation in the slew rate causes devastating results in the dynamic range as seen in Figure A.7d) and Figure A.7e). Here, the settling times are insufficient and worsening them makes no appreciable difference which seems to support other researcher's findings [BW88], [CNL⁺90] that the integrator time constants can be quite large, almost a secondary requirement next to slew rate. This is intuitively understood when considering the time-domain behavior at the outputs of the integrators. At low input levels, the amount of slewing followed by settling is quite similar and thus there is a certain amount of linear settling that takes place. Hence, there is an apparent immunity to the effects of insufficient settling time at low input levels. At higher levels, considerably more slewing takes place and the settling process from one cycle to the next may be in jeopardy if sufficient settling is not available.

For the architecture used in this thesis, the maximum output swing may be estimated from 1V at the input added to 1V from feedback for a total of 2V. This 2V may be added to a 1V from feedback at the output of the second integrator for the degenerate case for a maximum of a 3V excursion. From simulations just presented and knowing that the tolerance to slewing can be as high as 80%, a maximum bound may be calculated to which the minimum slew rate can be calculated. The maximum time allowed for slewing is thus

$$T_{MAX} = \frac{T}{2} (0.80) \quad \text{Eqn A.5}$$

and the maximum voltage is 3V or, in general terms, $3 \times \Delta/2$ where Δ is the quantizer span and is equal to 2V here, then the minimum slew rate that can be tolerated for the second integrator is

Figure A.7a

Dynamic range plots that compare the ideal (solid line) modulator and the modulator with unsettled integrators from finite slew rate and finite unity gain bandwidth opamps. Slew rate (SR) and closed-loop time constants are varied.

Figure A.7b

Dynamic range plots comparing ideal and nonideal operation of the modulator

Figure A.7c Dynamic range plots comparing the ideal and a suffering nonideal modulator.

Figure A.7d

Dynamic range plots. The finite slew rate of the opamps are too low for the clock rate of 10.24 MHz

Figure A.7e

Dynamic range plots. No appreciable difference occurs when the closed-loop time constant is decreased

$$SR = \frac{\Delta V}{\Delta T} = \frac{3(\Delta/2)}{T(0.80)} = 3.75 \frac{\Delta}{T} \quad \text{Eqn A.6}$$

This yields a slew rate of 76.8V/ μ S, which is close to the 70 V/ μ S simulation of Figure A.7b), showing the border line of safe operation. For slew rates not much less than this, harmonics appear in the baseband causing a reduction in the dynamic range due to a loss of signal-to-distortion + noise ratio at high input amplitudes to the modulator as a result of insufficient slewing ability.

When the modulator operates at critical slew rates, the designer must be aware of the effects of uneven slew rates that are inherent to opamps. Figure A.8 shows this to be quite similar to Figure A.7d) and Figure A.7e). The designer must ensure that the worst case slew rate be taken into account.

Figure A.8 Dynamic Range DRC of a modulator whose integrators have uneven slew rates

Appendix B

B.1) Detailed Noise Analysis of the MOS-Bipolar Transistor Differential Input Stage Folded-Cascode Opamp.

B.2) Detailed DC Gain Analysis of the MOS-Bipolar Transistor Differential Input Stage Folded-Cascode Opamp.

B.1 Detailed Noise Analysis

B.1.1 Input-Referred Thermal Opamp Noise

This section details the noise seen from various sources including thermal noise (and collector-current shot noise), base-current shot noise and $1/f$ noise in both the NPN and MOS transistors. An extensive treatment is given here to familiarize the reader with how noise may be calculated in BiCMOS amplifiers and the methodology used to input-refer it. In Chapter 5, noise is calculated in the (OTA) amplifier with less explanation since there will be an assumed familiarity with noise at that point. Certain calculations will not be shown as their insignificance may be proved by referring back to this section.

A simplified schematic of the opamp may be shown in Figure B.1), without the pole splitting and load capacitors. In order to proceed with a noise analysis, the nominal DC gains from stage to stage are required. Both simplified and detailed analysis is found later in this Appendix. In summary, these gains are $V_A/V_{in} = 1$, $V_B/V_A = 1.75$, $V/V_B = 137$, $V/V = 1$, and $V_o/V_i = 808$. Consideration must also be made to include the current mirror at the bottom of the cascodes. Not only does it provide differential-to-single ended conversion but also adds 6 dB to the overall DC (open-loop) gain of the opamp.

The strategy used here to calculate some of the input-referred opamp noise is to find many of the noise contributions at output node V_o seen in Figure B.1). This quantity will then be divided by the gain from V_{in} to V_o including the 6 dB advantage from the cascode's current mirror load.

Figure B.1 Simplified schematic of the MOS-bipolar differential input BiCMOS opamp (without capacitors).

Consider the inner differential pair first, ignoring the source follower cascaded into the differential pair for now. With reference to the Figure, the differential pair has input-referred thermal noise according to [GM84], [Erd81]

$$\frac{v_n^2}{\Delta f} = 4KT \left(\frac{1}{2g_{m2}} + r_{bb2} + R_{EE} \right) 2 \quad \frac{V^2}{Hz} \quad \text{Eqn B.1}$$

where the intrinsic base resistance r_{bb} is approximated at 245Ω and R_{EE} is the emitter degeneration resistance. Furthermore,

$$g_{m2} = \frac{I_{C2}}{V_T} = \frac{300\mu A}{0.026V} = 11.5mmho \quad \text{Eqn B.2}$$

The resulting voltage spectral density (VSD) is then

$$\begin{aligned} VSD_1 &= \sqrt{\frac{v_n^2}{\Delta f}} = \sqrt{1.66 \times 10^{-20} \left(\frac{1}{2(11.5 \times 10^{-3})} + 245 + 200 \right) \times 2} \\ &= 4.0 \frac{nV}{\sqrt{Hz}} \end{aligned} \quad \text{Eqn B.3}$$

The contribution from base-current shot noise from the inner differential input pair (assume $\beta_2 = 100$) is

$$\frac{i_{bs2}^2}{\Delta f} = 2qI_{B2} = 2(1.6 \times 10^{-19}) \left(\frac{300 \mu A}{100} \right) = 960 \times 10^{-27} \frac{A^2}{Hz} \quad \text{Eqn B.4}$$

The resistance R_A seen into node V_A by the current source $i_{bs2}^2/\Delta f$ may be seen in the example of Figure B.2) and is

Figure B.2 i) Base-current shot noise flows into equivalent resistance, R_A . ii) Small-signal model.

$$\begin{aligned} R_A &= \left[r_{bb2} + \left(\frac{1}{g_{mM7}} \parallel \frac{1}{g_{oM5}} \right) \right] \parallel \left[2[r_{\pi 2} + (1 + \beta_2)R_{EE}] + r_{bb3} + \left(\frac{1}{g_{mM8}} \parallel \frac{1}{g_{oM9}} \right) \right] \\ &\cong \left[r_{bb2} + \frac{1}{g_{mM7}} \right] \parallel 2 \left[\frac{\beta_2}{g_{m2}} + \beta_2 R_{EE} \right] \\ &\cong 1920 \Omega \end{aligned}$$

Eqn B.5

where

$$\begin{aligned}
 g_{mM1} &= \sqrt{2Kp \frac{W}{L} I_{DS}} \\
 &= \sqrt{2 (30 \times 10^{-6}) \left(\frac{80.2}{1.6} \right) (132 \mu A)} \\
 &= 0.63 \text{ mmhos}
 \end{aligned}
 \tag{Eqn B.6}$$

The PSD from the inner differential pair's base-current shot noise is then (using the result of Eqn B.4)

$$\begin{aligned}
 \frac{v_{bs2}^2}{\Delta f} &= \frac{i_{bs2}^2}{\Delta f} R_A^2 \\
 &= (960 \times 10^{-27}) (1920)^2 \\
 &= 3.53 \times 10^{-18} \frac{V^2}{Hz}
 \end{aligned}
 \tag{Eqn B.7}$$

This PSD may be multiplied by two to account for the other symmetrical half of this circuit (i.e. $i_{bs1}^2/\Delta f$ adds difference-mode noise across the two inputs (bases of Q2 and Q3)). From this, the voltage spectral density may then be found from

$$\begin{aligned}
 VSD_2 &= \sqrt{2 \times 3.53 \times 10^{-18}} \\
 &= 2.66 \frac{nV}{\sqrt{Hz}}
 \end{aligned}
 \tag{Eqn B.8}$$

As the voltage follower cascaded into the differential pair has a voltage gain of unity, the noise that has been calculated thus far may be referred back to the input of the follower with a gain of one. Now, the thermal noise from the cascode transistors may be found.

The gate-referred thermal noise from the current source M1 (or M2) is

$$\frac{v_{nM1}^2}{\Delta f} = 4KT \left(\frac{2}{3g_{mM1}} \right)
 \tag{Eqn B.9}$$

where

$$\begin{aligned}
 g_{mM1} &= \sqrt{2Kp \frac{W}{L} I_{DS}} = \sqrt{2 (30 \times 10^{-6}) \left(\frac{182}{1.6} \right) (600 \times 10^{-6})} \\
 &= 2.02 \text{ mmhos}
 \end{aligned}
 \tag{Eqn B.10}$$

This yields a VSD (gate-referred) of

$$v_{thM1} = 2.34 \frac{nV}{\sqrt{Hz}} \quad \text{Eqn B.11}$$

According to the simple analysis provided in Section B.2 of this appendix, this quantity experiences a gain to node V_z in Figure B.1), giving a VSD of

$$\begin{aligned} v_z^{thM1} &= g_{mM1} R_z v_{thM1} \\ &= 667 \frac{nV}{\sqrt{Hz}} \end{aligned} \quad \text{Eqn B.12}$$

Since $R_z = 137k\Omega$. Similarly, as may be seen in Section B.2,

$$v_z^{thM2} = v_z^{thM1} = 667 \frac{nV}{\sqrt{Hz}} \quad \text{Eqn B.13}$$

The total noise from M1 and M2 seen at node V_z is

$$\begin{aligned} v_z^{th(M1+M2)} &= \sqrt{(v_z^{thM1})^2 + (v_z^{thM2})^2} \\ &= 943 \frac{nV}{\sqrt{Hz}} \end{aligned} \quad \text{Eqn B.14}$$

This quantity may now be referred to the input by dividing the result of the above equation by $V_z/V_i = g_{meff}R_z = 480$ (Section B.2). The resulting input-referred noise is

$$\begin{aligned} VSD_3 &= \frac{943 \frac{nV}{\sqrt{Hz}}}{771} \\ &= 1.97 \frac{nV}{\sqrt{Hz}} \end{aligned} \quad \text{Eqn B.15}$$

Consideration must now be made to include the thermal noise arising from M3 and M4. The gate-referred thermal noise from M3 is

$$\begin{aligned} v_{thM3} &= \sqrt{4KT \left(\frac{2}{3g_{mM3}} \right)} \\ &= 3.30 \frac{nV}{\sqrt{Hz}} \end{aligned} \quad \text{Eqn B.16}$$

With reference to Section B.2, this voltage spectral density experiences gain to node v_z according to

$$\begin{aligned} v_z^{thM3} &= g_{mM3} R_z v_{thM3} \\ &= 457 \frac{nV}{\sqrt{Hz}} \end{aligned} \quad \text{Eqn B.17}$$

since

$$\begin{aligned} g_{mM3} &= \sqrt{2K_p \frac{W}{L} I_{DS}} \\ &= \sqrt{2(30 \times 10^{-6}) \frac{91.2}{1.6} (300 \times 10^{-6})} \\ &= 1.01 \text{ mmho} \end{aligned} \quad \text{Eqn B.18}$$

Similarly, $v_z^{thM4} = v_z^{thM5} = 457 \frac{nV}{\sqrt{Hz}}$. The total thermal noise contribution to node v_z from transistors M3 and M4 is

$$\begin{aligned} v_z^{th(M3 + M4)} &= \sqrt{(v_z^{thM3})^2 + (v_z^{thM4})^2} \\ &= 644 \frac{nV}{\sqrt{Hz}} \end{aligned} \quad \text{Eqn B.19}$$

To input refer this quantity, the above result is divided by v_z/v_i once again. The resulting input-referred noise is

$$\begin{aligned} VSD_4 &= \frac{644 \frac{nV}{\sqrt{Hz}}}{480} \\ &= 1.34 \frac{nV}{\sqrt{Hz}} \end{aligned} \quad \text{Eqn B.20}$$

A large source of thermal noise comes from the active load comprising of transistors Q14, Q15, Q16 and Q17 as seen in Figure B.3). The contribution of noise from each transistor will be found at node v_z and then referred back to the input.

The base-referred thermal noise of Q15 and Q17 is

Figure B.3 i) Noise in the cascode load. ii) Small-signal analysis of Q15 showing that $v_{\pi 15} = v_{th15}$

$$v_{th15} = v_{th17} = \sqrt{4KT \left(\frac{1}{2g_{m15}} + r_{bb15} \right)}$$

$$= 2.2 \frac{nV}{\sqrt{Hz}}$$

Eqn B.21

where $g_{m14-17} = \frac{300\mu A}{0.026V} = 11.5mmhos$ and $r_{bb15} = r_{bb17} = 245\Omega$. Noise is generated at the collectors of Q15 and Q17 according to

$$i_{c15} = g_{m15} v_{\pi 15} = \beta_{15} i_{b15}$$

Eqn B.22

where $v_{\pi 15} \approx \frac{r_{\pi 15}}{r_{bb15} + r_{\pi 15}} v_{th15} \approx v_{th15}$. Hence i_{b15} flows primarily from the voltage $v_{\pi 15}$ across $r_{\pi 15}$.

Hence

$$i_{c15} = g_{m15} v_{th15}$$

$$= (11.5 \times 10^{-3}) (2.2 \frac{nV}{\sqrt{Hz}})$$

$$= 25.3 \frac{pA}{\sqrt{Hz}}$$

Eqn B.23

This current spectral density goes through Q14 and thus mirrored to the collector of Q16 unattenuated where it then modulates into R_z producing a VSD of

$$\begin{aligned}
 V_z^{th15} &= i_{cs15} R_z \\
 &= (25.3 \times 10^{-12}) (137 \times 10^3) \\
 &= 3.47 \frac{\mu V}{\sqrt{Hz}}
 \end{aligned}
 \tag{Eqn B.24}$$

Similarly, i_{cs17} is approximately the same as i_{cs15} . The current spectral density i_{cs17} goes through Q16 unattenuated which then modulates into R_z . The resulting VSD is

$$\begin{aligned}
 V_z^{th17} &\approx i_{cs17} V_{th17} \\
 &\approx V_z^{th15} \\
 &\approx 3.47 \frac{\mu V}{\sqrt{Hz}}
 \end{aligned}
 \tag{Eqn B.25}$$

The collector-current shot noise of Q14 is

$$\begin{aligned}
 \frac{i_{cs14}^2}{\Delta f} &= 2qI_{c14} \\
 &= 2 (1.6 \times 10^{-19}) (300 \times 10^{-6}) \\
 &= 96 \times 10^{-24} \frac{A^2}{Hz}
 \end{aligned}
 \tag{Eqn B.26}$$

This current power spectral density mirrors over to the collector of Q16 where it is added to the collector-current shot noise of Q16

$$\begin{aligned}
 \frac{i_{cs16}^2}{\Delta f} &= 2qI_{c16} \\
 &= 96 \times 10^{-24} \frac{A^2}{Hz}
 \end{aligned}
 \tag{Eqn B.27}$$

The total collector-current shot noise from Q16 and Q14 is

$$\frac{i_{cs(14+16)}^2}{\Delta f} = 192 \times 10^{-24} \frac{A^2}{Hz}
 \tag{Eqn B.28}$$

Which modulates into R_z . The VSD that results is

$$v_{i_c}^{(14+16)} = \sqrt{\frac{I_{c14+16}}{\Delta f} R_{i_c}^2} = 1.9 \frac{\mu V}{\sqrt{Hz}} \quad \text{Eqn B.29}$$

Note that collector-current shot noise and not base-referred thermal noise contributions were calculated for Q14 and Q16. This is because Q14 and Q16 have emitter degeneration (Q15 and Q17) which causes an insignificant amount of base-referred thermal noise to appear across r_{π} . Hence $v_{\pi} \ll v_{th}$ and thus the resulting noise current that flows ($g_m v_{\pi}$) is insignificant. The total VSD seen at node v_{i_c} is then

$$v_{i_c} = \sqrt{(v_{i_c}^{(15)})^2 + (v_{i_c}^{(17)})^2 + (v_{i_c}^{(14+16)})^2} = 5.26 \frac{\mu V}{\sqrt{Hz}} \quad \text{Eqn B.30}$$

This may now be input referred by dividing the above result by v_{i_c}/v_i . Hence

$$VSD_{i_c} = \frac{v_{i_c}}{480} = 10.9 \frac{nV}{\sqrt{Hz}} \quad \text{Eqn B.31}$$

The other base-current and collector-current shot noise contributions beyond node v_{i_c} are insignificant compared to the spectral densities seen so far.

Now, the thermal noise of the source follower's driver (transistor M7 in Figure B.1) may be addressed. Taking both inputs into account,

$$VSD_{M7} = \sqrt{2 \times 4KT \left(\frac{2}{3g_{mM7}} \right)} = 5.93 \frac{nV}{\sqrt{Hz}} \quad \text{Eqn B.32}$$

where the transconductance of the driver is known from a previous calculation. The thermal noise calculation of the load device M5 as follows. The transconductance of M5 is

$$g_{mM5} = \sqrt{2 (30 \times 10^{-6}) \left(\frac{40}{1.6} \right) (132 \mu A)}$$

$$445 \mu mhos$$

Eqn B.33

This yields a gate-referred thermal noise

$$V_{thM5} = \sqrt{4KT \left(\frac{2}{3g_{mM5}} \right)}$$

$$4.99 \frac{nV}{\sqrt{Hz}}$$

Eqn B.34

The resulting current that flows is $g_{mM5}V_{thM5}$ into the resistance R_A seen at node A is

$$R_A = \left(\frac{1}{g_{mM7}} \parallel \frac{1}{g_{OM5}} \right) \parallel (r_{bb2} + R_f)$$

$$\approx \frac{1}{g_{mM7}}$$

$$\approx 1590 \Omega$$

Eqn B.35

The VSD at node A (V_A) is

$$\begin{aligned} V_A^{thM1} &= g_{mM5} V_{thM5} R_A \\ &= (445 \times 10^{-6}) (4.99 \times 10^{-9}) (1590) \\ &= 3.52 \frac{nV}{\sqrt{Hz}} \end{aligned}$$

Eqn B.36

Taking into account the source follower attached to the other half of the differential pair,

$$VSD_T = \sqrt{2 \times (3.52 \times 10^{-9})^2} = 4.98 \frac{nV}{\sqrt{Hz}}$$

Eqn B.37

which is referred to the input unattenuated.

The total input-referred thermal opamp noise is then found by summing all spectral densities such that

$$VSD_{th} = \sqrt{\sum_i VSD_i^2} \quad \text{Eqn B.38}$$

Tabulating all the voltage spectral densities yields the final, input-referred voltage spectral density

$$VSD_{th} = 14.4 \frac{nV}{\sqrt{Hz}} \quad \text{Eqn B.39}$$

The manner in which this noise goes through to the output of the DISDM is covered in Chapter 3. It is now prudent to cover the $1/f$ noise in the opamp.

B.1.2 Input-Referred Opamp $1/f$ Noise

The $1/f$ noise PSD for bipolar transistors is

$$S_{n(i/b)}(f) = \frac{KI_b^M}{f} = \frac{A^2}{Hz} \quad \text{Eqn B.40}$$

where I_b is the quiescent base current of the bipolar transistor, K and MF are parameters which depend on the process. Here, as is often done, $1/f$ noise is quoted at 1 kHz. This noise spectral density (in A^2/Hz) flows into the same resistance that base-current shot noise does, allowing the determination of noise in terms of voltage spectral density. For a MOS transistor, the input-referred (i.e., gate-referred) noise is

$$S_{n(g/d)}(f) = \frac{KF}{C_{ox}WLf^M} = \frac{V^2}{Hz} \quad \text{Eqn B.41}$$

where KF and MF are also process parameters. Although not disclosed, representative values for KF and MF are near $KF = 250 \times 10^{-27}$ and $MF = 0.95$ for PMOS transistors while K and MF for bipolar transistors are near $K = 5 \times 10^{-11}$ and $MF = 1.7$. With reference to Figure B.2), the gate-referred voltage spectral density from flicker noise at 1 kHz from the source follower's driver M7 is

$$VSD_{(1-f)M7}(1KHz) = \sqrt{\frac{KF}{C_{ox}(80.2)(1.6)(1000)^3}} \\ = 42.6 \frac{nV}{\sqrt{Hz}} \quad \text{Eqn B.42}$$

Furthermore, the follower's load M5 also displays gate-referred 1/f noise at 1 kHz

$$VSD_{(1-f)M5}(1KHz) = \sqrt{\frac{KF}{C_{ox}(40.1)(1.6)(1000)^3}} \\ = 60.4 \frac{nV}{\sqrt{Hz}} \quad \text{Eqn B.43}$$

The above gate-referred VSD causes a noise current to flow according to $g_{mM5}VSD_{(1-f)M5}$ which modulates into the resistance at node V_A . This resistance is approximately $1/g_{mM7}$. Hence the resulting VSD at node V_A is

$$VSD_A^{(1-f)M5}(1KHz) = \frac{g_{mM5}}{g_{mM7}} VSD_{(1-f)M5}(1KHz) = 42.7 \frac{nV}{\sqrt{Hz}} \quad \text{Eqn B.44}$$

where $g_{mM5} = 445\mu mhos$ and $g_{mM7} = 0.63mmhos$ as defined previously. This is referred back to the input of the source follower unattenuated. The resulting VSD is the RMS sum of $VSD_{(1-f)M7}$ and $VSD_A^{(1-f)M5}$ which is multiplied by $\sqrt{2}$ to account for the other half of the differential pair.

$$VSD_{(1-f)follower}(1KHz) = \sqrt{[(VSD_{(1-f)M7})^2 + (VSD_A^{(1-f)M5})^2]} \times 2 \\ = 85.3 \frac{nV}{\sqrt{Hz}} \quad \text{Eqn B.45}$$

This quantity is as low as it is by using very large gate area and utilizing PMOS rather than NMOS devices.

It is now prudent to consider the noise contribution from the cascode devices. As was done in the calculation of thermal noise, the gate-referred 1/f noise of the MOS cascode transistors ex-

periences gain (Section B.2) to node V_x where the total contribution from all sources may then be referred to the input of the opamp. Transistor M1 (and M2) has 1/f noise PSD

$$S_{n(f),M1}(1\text{kHz}) = \frac{KF}{C_{ox}(182.4)(1.6)(1,000)^2} \\ = 800 \times 10^{-18} \frac{\text{V}^2}{\text{Hz}} \quad \text{Eqn B-46}$$

which yields a gate-referred VSD at 1 kHz of

$$VSD_{(f),M1}(1\text{kHz}) = VSD_{(f),M1}(1\text{kHz}) = 28.3 \frac{\text{nV}}{\sqrt{\text{Hz}}} \quad \text{Eqn B-47}$$

This gets to node V_x according to $v_x/(VSD_{(f),M1}) = g_{mM1}R$ as seen in Section B.2. Thus

$$VSD_{(f),M1}(1\text{kHz}) = g_{mM1}R VSD_{(f),M1}(1\text{kHz}) \\ = 7.83 \frac{\mu\text{V}}{\sqrt{\text{Hz}}} \quad \text{Eqn B-48}$$

Similarly,

$$VSD_{(f),M2}(1\text{kHz}) = g_{mM2}R VSD_{(f),M2}(1\text{kHz}) \\ = 7.83 \frac{\mu\text{V}}{\sqrt{\text{Hz}}} \quad \text{Eqn B-49}$$

Transistor M3 (and M4) has 1/f noise PSD

$$S_{n(f),M3}(1\text{kHz}) = \frac{KF}{C_{ox}(91.2)(1.6)(100)^2} \\ = 1.6 \times 10^{-17} \frac{\text{V}^2}{\text{Hz}} \quad \text{Eqn B-50}$$

which results in a gate-referred VSD at 1 kHz of

$$VSD_{(1/f)M3}(1\text{KHz}) = VSD_{(1/f)M4}(1\text{KHz}) = 40.0 \frac{\text{nV}}{\sqrt{\text{Hz}}} \quad \text{Eqn B.51}$$

This experiences gain to node V_2 according to $v_2/(VSD_{(1/f)M3}) = g_{mM3}R_z$ as seen in Section B.2. Hence

$$\begin{aligned} VSD_2^{(1/f)M3}(1\text{KHz}) &= g_{mM3}R_z[VSD_{(1/f)M3}(1\text{KHz})] \\ &= 5.54 \frac{\mu\text{V}}{\sqrt{\text{Hz}}} \end{aligned} \quad \text{Eqn B.52}$$

Similarly,

$$\begin{aligned} VSD_2^{(1/f)M4}(1\text{KHz}) &= g_{mM4}R_z[VSD_{(1/f)M4}(1\text{KHz})] \\ &= 5.54 \frac{\mu\text{V}}{\sqrt{\text{Hz}}} \end{aligned} \quad \text{Eqn B.53}$$

The total VSD 1/f noise contribution from the cascode devices, at node V_2 at 1 kHz is

$$\begin{aligned} VSD_2^{(1/f)(M1-M4)}(1\text{KHz}) &= \sqrt{[VSD_2^{(1/f)M1}]^2 + [VSD_2^{(1/f)M2}]^2 + [VSD_2^{(1/f)M3}]^2 + [VSD_2^{(1/f)M4}]^2} \\ &= 13.56 \frac{\mu\text{V}}{\sqrt{\text{Hz}}} \end{aligned} \quad \text{Eqn B.54}$$

This quantity is now input-referred

$$\begin{aligned} VSD_{(1/f)\text{cascode}}(1\text{KHz}) &= \frac{VSD_2^{(1/f)(M1-M4)}(1\text{KHz})}{V_2/V_i} \\ &= (13.56 \frac{\mu\text{V}}{\sqrt{\text{Hz}}}) / 480 \\ &= 28.3 \frac{\text{nV}}{\sqrt{\text{Hz}}} \end{aligned} \quad \text{Eqn B.55}$$

It is clear that the low gain of the differential pairs in folded-cascode opamps is detrimental in increasing the amount of noise that can be referred back to the input not only where 1/f noise is concerned but also thermal and shot noise.

Hence, the total 1/f noise at 1 kHz (input-referred) is

$$\begin{aligned} VSD_{1/f, total}(1\text{kHz}) &= \sqrt{[VSD_{1/f, Dto, lower}(1\text{kHz})]^2 + [VSD_{1/f, Dto, codes}(1\text{kHz})]^2} \\ &= 89.9 \frac{\text{nV}}{\sqrt{\text{Hz}}} \end{aligned}$$

Eqn B.86

Simulations concur very well with theory, as shown and discussed in Chapter 3.

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B.2 Detailed DC Gain Analysis

Refer to Figure B.1), the simplified schematic.

Assume the Early voltage of the PMOS device to be $V_A=46$ V and $V_A=38$ V for the NPN device. (Do not confuse V_A , the Early voltage with the node voltage, v_A).

- 1) The gain of the emitter follower, v_A/v_{in} is approximated to 1.
- 2) The gain of the differential stage from v_A to v_B is found as follows, where

Figure B.4 Inner differential pair to the cascode

$g_{m2} = 11.5 \text{ mmhos}$ and $R_{EE} = 200 \Omega$ and also where

$$\begin{aligned}
 g_{mM4} &= \sqrt{2K_P \frac{W}{L} I_{DS}} \\
 &= \sqrt{2(30 \times 10^{-6}) \frac{91.2}{1.6} 300 \times 10^{-6}} \\
 &= 1.0 \text{ mmho}
 \end{aligned}
 \tag{Eqn B.57}$$

The impedance looking into v_B is dominated by $1/g_{mM4}$. Hence,

$$\frac{v_B}{v_A} \approx -\frac{1}{2} \frac{R_{EE} \parallel 1/g_{m2}}{g_{mM4}} \approx -1.75
 \tag{Eqn B.58}$$

The overall gain of this stage is twice that indicated above as there is a current mirror that exists at the bottom of the cascode stage (10.9 dB total).

3) The gain of the common-gate configuration, v_f/v_B .

Figure B.5 Common-gate section plus ac small-signal schematic of it

The Wilson Current source improves the output resistance of Q16 to $R_{out} \approx \frac{\beta r_{o16}}{2}$ [Gre84]

where $r_{o16} = \frac{V_A}{I_C} = \frac{38}{300 \times 10^{-6}} = 127k\Omega$, $r_{\pi19} = 10.6k\Omega$ since $\beta_{19} \approx 100$, $r_{\pi20} = 1.3K\Omega$

and r_{o18} is very high compared to $r_{\pi20}$. Consequently,

$$\frac{v_f}{v_B} \approx g_{mM4} \left(\frac{\beta r_{o16}}{2} \parallel [r_{\pi19} + (1 + \beta_{19}) r_{\pi20}] \right)$$

$$\approx 137 \quad (42.7dB)$$

Eqn B.59

Note that the high impedance characteristic of cascode stages from M2 and M4 seen at node Z [GM84][Abi88] (i.e. $R_{cascode} = r_{oM2} + r_{oM4} (1 + g_{mM4} r_{oM2})$) is defeated by the existence of r_{o16} in parallel with $R_{cascode}$.

4) The gain of the emitter follower stage, $\frac{v_{Z'}}{v_Z}$ is

$$\frac{v_{Z'}}{v_Z} = \frac{r_{\pi 20}(1 + \beta_{10})}{r_{\pi 10} + r_{\pi 20}(1 + \beta_{10})} \approx 1 \quad \text{Eqn B.60}$$

Hence $v_Z/v_1 = 480$

5) The gain of the output stage $\frac{v_O}{v_{Z'}}$ is

Figure B.6 Output stage

where $r_{o20} = 24.7K\Omega$, $r_{oM6} = 30.5k\Omega$ and $g_{m20} = 59.2\text{mmho}$. Hence the gain of the output stage is

$$\frac{v_O}{v_{Z'}} = g_{m20}(r_{o20} \parallel r_{oM6}) = 808x \quad (58.1\text{dB}) \quad \text{Eqn B.61}$$

The total DC gain is $10.9 + 42.7 + 58.1 = 111.7\text{ dB}$ which is close to the simulation result (109 dB.)

$$g_{meff} = \frac{1}{\frac{1}{g_m} + R_{Et}}$$

$$g_{mM_1} = g_{mM_2} = 2.02 \text{ mhos}$$

$$g_{mM3} = g_{mM4} = 1.01 \text{ mmhos}$$

$$R_f = 137K\Omega$$

$$i_{total} = i_1 + i_1'$$

Basic Folded-Cascode Opamp used here, without the pole-splitting output stage

Gain V_z/V_i

The voltage V_i causes current i to flow as seen at node A. The opposite effect occurs at node A'. The voltage gain from V_i to node A is then

$$v_A = i/g_{mM3} = \frac{g_{meff} v_i}{g_{mM3}} \frac{1}{2} \quad \text{Eqn B.62}$$

This in turn causes the current i_1 to flow according to

$$I_1 = g_{mM3} V_A = g_{meff} \frac{V_i}{2} \quad \text{Eqn B.63}$$

This current is replicated to node Z by the current mirror. Similarly, there is a current i_1' that is equal and opposite to i_1 such that the total current exiting node Z is

$$I_{total} = i_1 + i_1' = g_{meff} V_i \quad \text{Eqn B.64}$$

The voltage at node Z is

$$v_z/v_i = g_{mell}R_f = 480 \quad \text{Eqn B.65}$$

Hence, all noise that contributes to node Z may be input referred by dividing the voltage spectral density at node Z by the gain V_z/V_i shown above.

Individual Gains

$$v_z/v_{thM1}$$

The current that flows from M1 as a result of noise on the gate is pictorially shown as i_a .

$$i_a = g_{mM1}v_{thM1} \quad \text{Eqn B.66}$$

As seen already, the voltage at node A as a result of i_a is

$$v_a = i_a/g_{mM3} = (g_{mM1}v_{thM1})/g_{mM3} \quad \text{Eqn B.67}$$

The resulting current that flows in branch B is, as already seen,

$$i_b = g_{mM3}v_a = g_{mM1}v_{thM1} \quad \text{Eqn B.68}$$

as expected. This current is mirrored to the other side so that the voltage generated at node Z is

$$v_z = g_{mM1}v_{thM1}R_f \quad \text{Eqn B.69}$$

Similarly, $v_z/v_{thM2} = v_z/v_{thM1}$

With little effort, it may also be seen that the gain

$$v_z/v_{thM3} = v_z/v_{thM4} = g_{mM1}R_f \quad \text{Eqn B.70}$$

This is accomplished by considering that the voltage spectral density on the gate of M3 is seen at node A as this is essentially a source follower. Thus a current i_b flows as shown above where

$$v_a = v_{thM3} \text{ causing a voltage } v_z.$$

Appendix C

C.1 Finite Gain in Amplifiers

The existence of a difference-mode voltage between the input terminals of an opamp is a direct result of finite open-loop gain. Not only does finite-gain produce a gain error in the system but it also results in a mechanism that can limit the SNR at all amplitudes, thus diminishing the performance of the oversampled A/D. It is the existence of this difference-mode voltage which allows a comprehensive analysis into the topic of nonlinearity to take place later.

The effect of finite gain in the opamps produces a leaky integrator, which in turn causes a zero at frequencies other than DC in the noise transfer function. Thus, not unlike thermal noise in opamps, the spectral response of the DISDM yields a flat spectrum at low frequencies, due now to leaky integration. A nasty manifestation of this effect is a phenomenon known as “deadbanding”, the dynamics of which cause a loss of information presented to the input of the modulator. This phenomenon is well documented [FC91] and is not the focus of this thesis. However, the spectral response is of interest as a potential dynamic range limitation.

The treatment of finite gain in opamps in this section pertains to switched-capacitor integrators that make up the sampled-data oversampled A/D. It should be noted however that the results are also applicable for continuous-time integrators and oversampled A/Ds. First, consider a typical switched-capacitor integrator that might be found in a DISDM as seen in Figure C.1. Taking finite gain into account, charge balance equations may be written which include the difference-mode voltage, v_d .

During ϕ_2 , charge balance dictates

$$C_1 [(v_{i,n} - v_{d,n}) - (0 - 0)] + C_{F1} [(v_{o,n} - v_{d,n}) - (v_{o,n-1/2} - v_{d,n-1/2})] = 0 \quad \text{Eqn C.1}$$

Similarly, during ϕ_1

$$C_{F1} [(v_{o,n-1/2} - v_{d,n-1/2}) - (v_{o,n-1} - v_{d,n-1})] = 0 \quad \text{Eqn C.2}$$

Adding the above two equations, substituting $v_d = -\frac{v_o}{A}$ and expanding leads to

Figure C.1 Switched-capacitor integrator, with charge balance models for each phase

$$C_1 v_{i,n} + C_1 \frac{v_{o,n}}{A} + C_n v_{o,n} + C_n \frac{v_{o,n}}{A} - C_n v_{o,n-1} - C_n \frac{v_{o,n-1}}{A} = 0 \quad \text{Eqn C.3}$$

where A is the DC gain of the opamp. Rearranging and writing as a z transform,

$$v_o \left[C_n + \frac{C_1 + C_n}{A} \right] - C_n z^{-1} - \frac{C_n}{A} z^{-1} = C_1 v_i \quad \text{Eqn C.4}$$

Dividing by the integration capacitor, C_n , and letting $\alpha_1 = C_1/C_n$, then

$$\frac{v_o(z)}{v_i(z)} = \frac{\alpha_1}{1 + \frac{1}{A}(1 + \alpha_1) - (1 + \frac{1}{A})z^{-1}} \quad \text{Eqn C.5}$$

This may be written as

$$\frac{v_o(z)}{v_i(z)} = \frac{\alpha_1 / \left[1 + \frac{1}{A}(1 + \alpha_1) \right]}{1 - \left[\frac{1 + 1/A}{1 + \frac{1}{A}(1 + \alpha_1)} \right] z^{-1}} \quad \text{Eqn C.6}$$

$$\frac{\alpha_1'}{1 - L_K z^{-1}} \quad \text{Eqn C.7}$$

where the α_1' represents the coefficient α_1 with a gain error term and L_K represents the leakage term. Furthermore, the binomial expansion may be applied to the L_K term so as to simplify the final expression.

$$\begin{aligned} L_K &= \frac{1 + 1/A}{1 + \frac{1}{A}(1 + \alpha_1)} \\ &= (1 + \frac{1}{A}) \left[1 - \frac{1}{A}(1 + \alpha_1) \right] \\ &= 1 - \frac{\alpha_1}{A} \end{aligned} \quad \text{Eqn C.8}$$

when neglecting the higher order terms. Hence, the final z-transform for the leaky integrator is

$$\begin{aligned} \frac{v_o(z)}{v_i(z)} &= \frac{-\alpha_1' \left[1 + \frac{1}{A}(1 + \alpha_1) \right]}{1 - (1 - \frac{\alpha_1}{A})z^{-1}} \\ &= \frac{-\alpha_1'}{1 - (1 - \frac{\alpha_1}{A})z^{-1}} \end{aligned} \quad \text{Eqn C.9}$$

In reality, a single- or double-integration $\Sigma\Delta$ modulator requires the use of an integrator that also sums feedback from the quantizer as seen in Figure C.2. The same charge balance method used for the simple integrator may be used to determine the z-transform for the integrator shown in Figure C.2. The result of such an exercise leads to a z-transform

$$\begin{aligned} \frac{v_o(z)}{v_i(z)} &= \frac{\alpha_1 v_i(z) - \alpha_2 v_o(z)}{1 + \frac{1}{A}(1 + \alpha_1 + \alpha_2) - (1 + \frac{1}{A})z^{-1}} \\ &= \frac{[\alpha_1 v_i(z) - \alpha_2 v_o(z)]}{1 + \frac{1}{A}(1 + \alpha_1 + \alpha_2)} \cdot \frac{1/\left[1 + \frac{1}{A}(1 + \alpha_1 + \alpha_2)\right]}{\left[1 + \frac{1}{A}(1 + \alpha_1 + \alpha_2)\right]z^{-1}} \end{aligned} \quad \text{Eqn C.10}$$

Figure C.2 Switched-capacitor integrator used in oversampled A/Ds with feedback.

which may be approximated as

$$v_o(z) = \frac{[-\alpha_1 v_i(z) - \alpha_2 v_j(z)]}{1 - (1 - \frac{\alpha_1 + \alpha_2}{A})z^{-1}} \quad \text{Eqn. C.11}$$

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> + 4! r2 r4 (-1) + 1
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> (1 - 4 P1^2 c2 c1 f^2 r2 r4 + -----)
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> (-1) + 1 - 4 P1^2 c2 c1 f^2 r2 r4 + -----)
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> r1 + (-1) r2 r4 (-1) +
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> 1 (1 - 4 P1^2 c2 c1 f^2 r2 r4 + -----)
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> (r1 c3), 2) (1 - 4 P1^2 c2 c1 f^2 r2 r4 + -----)
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> 1 - 4 P1^2 c2 c1 f^2 r2 r4 + -----)
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> (-1) + 1 / (1 - 4 P1^2 c2 c1 f^2 r2 r4 + -----)
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> In[82]:=
> In[82]:= Coef=Coefficient[q,v1 v1]

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Appendix E

E.1) Detailed DC Gain Analysis of the OTA.

E.2) Simulation and Measurement Results of OTA, First-Order and Second-Order $g_m - C$ Filters.

E.3) OTA Distortion Study

E.4) Expected Distortion from Postlayout Simulation of the First-Order, Low-Pass Filter

E.5) Expected Distortion from Postlayout Simulation of the Biquad Filter

E.1 Detailed DC Gain Analysis of the OTA

Refer to Figure 5.14, the simplified schematic.

Assume the Early voltage of the PMOS device to be $V_A=46$ V and $V_A=38$ V for the NPN device.

E.1.1 1) The gain of the outer differential pairs.

E.1.1.1 i) v_{B4}/v_{ia} .

$$g_{m3} = g_{m4} = \frac{I_C}{V_T} = 15.4 \text{ mmho}$$

$$A_{OPPa} = \frac{v_{B4}}{v_{ia}} = -\frac{1}{2} \frac{g_{m4}}{g_{m3}} = -0.5 \quad (-6\text{dB})$$

Eqn E.1

$$\text{since } R_{B4} = r_{\pi 4} \parallel \frac{1}{g_{m3}} \parallel \frac{1}{g_{m4}} = \frac{1}{g_{m4}}$$

E.1.1.2 ii) v_B/v_{ib}

$$g_{m1} = g_{m2} = \frac{I_c}{V_T} = 18.4 \text{ mho}$$

$$A_{ODPb} = \frac{v_{B4}}{v_{ia}} \approx \frac{1}{2} \frac{1/g_{m2}}{R_{EE}} \approx 0.028 \quad (-31.1 \text{ dB}) \quad \text{Eqn E-2}$$

since $R_{B1} = r_{\pi s} \parallel \frac{1}{g_{o1}} \parallel \frac{1}{g_{m2}} \approx \frac{1}{g_{m2}}$.

E.1.2 2) Gain of the inner differential pairs.(ie. v_i/v_B)

$$\frac{v_i}{v_B} \approx -\frac{1}{2} \frac{g_{m5}}{g_{mM2}} \approx -10.8 \quad (20.7 \text{ dB}) \quad \text{Eqn E-3}$$

where $g_{m5} = g_{m1}$.

E.1.3 3) Gain of the cascode stage (low-impedance to high-impedance point), v_D/v_i .

where $1/g_{oN} = 38/1200 \times 10^{-6} = 31.7 \text{ k}\Omega$, $r_{\pi12} = \beta_{12}/g_{m1} = 6.5 \text{ k}\Omega$
 , $r_{\pi14} = 3.15 \text{ k}\Omega$, $1/g_{oM2} = 46/1200 \times 10^{-6} = 38.3 \text{ k}\Omega$ and

$$g_{mM1} = \sqrt{2K_p \frac{W}{L} I_{DSM1}}$$

$$= \sqrt{2(30 \times 10^{-6}) \frac{199.6}{1} 2267 \times 10^{-6}}$$

$$= 5.21 \text{ mmho}$$

$$g_{mM2} = \sqrt{2K_p \frac{W}{L} I_{DSM2}}$$

$$= \sqrt{2(30 \times 10^{-6}) \frac{56.6}{2} 1200 \times 10^{-6}}$$

$$= 1.43 \text{ mmho}$$

$$g_{m9} = (1200 \mu\text{A}) / (0.026 \text{ V}) = 46.2 \text{ mmho}$$

$$\frac{v_D}{v_C} = g_{mM2} R_D$$

$$= 24.8 \quad (27.9 \text{ dB})$$

Eqn E.4

where

$$R_D = \frac{1}{g_{o9}} || \left[r_{\pi 12} + (1 + \beta_{12}) \left(\frac{1}{g_{o13}} || r_{\pi 14} \right) \right] || R_{cascode}$$

$$= 17.4 \text{ k}\Omega$$

Eqn E.5

where $k_{cascode} = r_{oM1} + r_{oM2}(1 + g_{mM2}r_{oM1})$ and is very high compared to $\frac{1}{g_{mM2}}$.

E.1.4 4) Gain of the emitter follower, $\frac{v_{D'}}{v_D}$.

$$\frac{v_{D'}}{v_D} = \frac{(1 + \beta_{12})(r_{o13} \parallel r_{\pi14})}{r_{\pi12} + (1 + \beta_{12})(r_{o13} \parallel r_{\pi14})} \approx 1$$

Eqn E.6

E.1.5 5) Gain of the pole-splitting output stage, $\frac{v_O}{v_{D'}}$.

Here, $r_{o14} = 46K\Omega$, $r_{oM5} = 55.8K\Omega$ and $g_{m14} = 31.7mmho$.

$$\frac{v_O}{v_{D'}} = g_{m14}((r_{o14} \parallel r_{oM5}) \parallel 10K\Omega) = 227 \quad (47.1 dB)$$

Eqn E.7

The total DC gain of the OTA from the inner differential pair to the output is

$$A_{TOTAL} = 20.7 + 27.9 + 47.1 = 95.7 dB$$

Eqn E.8

Simulation shows 94.6 dB which is quite close compared to theory.

**E.2 *Simulation and Measurement Results of the OTA,
First-Order and Second- Order $g_m - C$
Filters.***

The following pages contain HSPICE noise simulations and are presented in power spectral densities. These are compared with measurements using an HP3585A spectrum analyzer.

Figure E.1a

Simulated thermal noise power spectral density ($VSD = 200\mu V/\sqrt{Hz}$) at low frequency at the output of the open-loop OTA. (Open-loop gain shown for reference)

Figure E.1b

Measured open-loop OTA thermal noise is less because the gain of the OTA is less. Taking this into account, the noise level is consistent with theoretical.

Figure E.2a

Simulated thermal noise ($147 \text{ nV}/\sqrt{\text{Hz}}$) for the first-order low-pass filter.

Figure E.2b

Measured thermal noise, consistent with the above results.

Figure E.3a Simulated $1/f$ noise ($447 \text{ nV}/\sqrt{\text{Hz}}$ at 1 kHz) for the open-loop OTA.

Figure E.3b Measured $1/f$ noise, consistent with the above when taking the gain of the OTA into consideration.

Figure E.4a Simulated $1/f$ noise ($316\text{nV}/\sqrt{\text{Hz}}$ at 1 kHz) for the first-order low-pass filter.

Figure E.4b Measured $1/f$ noise, consistent with the above results.

Figure E.5a Simulated thermal noise ($147\text{ nV}/\sqrt{\text{Hz}}$) for the biquad filter.

Figure E.5b Measured thermal noise, consistent with the above results.

Figure E.5c

Measured VSD at the resonant peak is $316 \text{ nV} / \sqrt{\text{Hz}}$, higher than expected due to the slightly higher measured Q.

Figure E.6a Simulated $1/f$ noise ($316nV/\sqrt{Hz}$ at 1 kHz) for the biquad filter.

Figure E.6b Measured $1/f$ noise, consistent with the above results.

E.3 OTA Distortion Study

The study in $g_m - C$ circuit distortion must proceed as follows. Having determined the theoretical distortion from the open-loop OTA, a postlayout simulation of the open-loop OTA may be used to determine its linearity coefficients by examining the harmonics. To ensure the correctness of this theory, a macromodel simulation is performed using the linearity coefficients found in an attempt to reproduce the harmonics found from the postlayout simulation. This will validate the theory and the measured OTA harmonics may then be used to determine the linearity coefficients of the fabricated device. This exercise will then lead to a prediction of the harmonic levels in the filters and the oversampled A/Ds.

With reference to Figure E.7, consider the current that exits this transconductor, described as a

Figure E.7 Open-loop transconductor (OTA)

power-series expansion such that

$$I_1 = -g_{11}v_i + g_{12}v_i^2 + g_{13}v_i^3 \quad \text{Eqn E.9}$$

where g_{11} is simply the transconductance g_{m1} while g_{12} and g_{13} are the second- and third-order linearity coefficients of this transconductor. The resulting voltage that is generated at the output of the OTA is simply $v_o(j\omega) = i_1/j\omega C$ leading to

$$v_o(j\omega) = \frac{g_{11}}{j\omega C}v_i(j\omega) + \frac{g_{12}}{j\omega C}v_i^2(j\omega) + \frac{g_{13}}{j\omega C}v_i^3(j\omega) \quad \text{Eqn E.10}$$

where $C = 2pF$. The resulting pre-bandlimited absolute signal harmonics, with help from the previous chapter, are

$$hd(f) = \frac{g_{m1} C}{2\pi f} V_I$$

$$hd(2f) = \frac{1}{2} \frac{g_{m1} C}{2\pi f} V_I^2$$

$$hd(3f) = \frac{1}{4} \frac{g_{m1} C}{2\pi f} V_I^3$$

Eqn E.11

where V_I is the peak input amplitude applied to the transconductor. Pre-bandlimited here is in reference to the harmonics that exist before filtration by the integrator.

The above equations may now be used to determine the linearity coefficients of the OTA given any set of harmonic levels and the input level V_I . The harmonics of the OTA may first be determined through postlayout simulation and later through measurements.

The measured single-ended UGBW of the transconductor was found to be 31 MHz which corresponds closely with the simulated (postlayout) UGBW as shown in Chapter 5. It is not 36.2 MHz as originally designed due to differences between the laid-out and extracted parameter values particularly the polysilicon resistors and the polysilicon-polysilicon capacitors.

The inner and outer differential pairs that make up the Gilbert gain cell is biased equally in both simulation and in measurement for consistency. An arbitrary test frequency must be chosen. The linear signal source used in initial measurements was limited to 13 MHz and the spectrum analyzer used was limited to 40 MHz frequencies, barely capturing the third harmonic. Comparisons between measurement and simulation are done at this frequency. At a nominal frequency of 13 MHz, a sinusoidal peak voltage of $V_I = 0.42V_{pk}$ is applied to the input of the OTA so that a $1V_{pk}$ fundamental (-3 dBV) results at the output of the measured OTA, as a reference.

Consider first an FFT of the postlayout simulation of Figure E.8a). The resulting fundamental (denoted as $hd(f)$) and harmonics are (at multiples of 13 MHz)

$$hd(f) = -5\text{dBV}$$

$$hd(2f) = -69.5\text{dBV}$$

$$hd(3f) = -78.2\text{dBV}$$

Eqn E.12

Figure E.8a Resulting FFT from postlayout simulation of the OTA

Figure E.8b Resulting FFT from macromodel simulation used to replicate harmonics from postlayout simulation

However, the $1/s$ low-pass filtering action of the OTA suppresses these harmonics by 6dB and 9.5dB at twice and three times the fundamental frequency respectively. The pre-bandlimited harmonics are then

$$\begin{aligned}hd(f) &= -5\text{dBV} && (0.794\text{V}_{pk}) \\hd(2f) &= -63.5\text{dBV} && (0.044\text{mV}_{pk}) \\hd(3f) &= -68.7\text{dBV} && (0.019\text{mV}_{pk})\end{aligned}\tag{Eqn E.13}$$

(Note that $hd(f)$ is not -3 dBV since the UGBW of the OTA is slightly less than the 31 MHz found in measurements.) The resulting linearity coefficients which may be found from Eqn E.11 are, when $V_I = 0.42\text{V}_{pk}$ and $C = 2\text{pF}$

$$\begin{aligned}g_{11} &= 310\mu\text{A/V} \\g_{12} &= 1.75\mu\text{A/V} \\g_{13} &= 4.58\mu\text{A/V}^2\end{aligned}\tag{Eqn E.14}$$

As a double check, the above linearity coefficients are used in a macromodel simulation using a standard voltage-to-current polynomial element in HSPICE. A transient simulation leads to the resulting FFT shown in Figure E.8b) which yields the same harmonics as the postlayout simulation of Figure E.8a). This conclusively verifies the theoretical approach taken here.

Ideally, the harmonic levels seen from the postlayout simulation of the open-loop OTA should be very low since the simulation environment is nearly ideal (i.e. no mismatches between transistors, etc., as covered earlier in the discussion on the operation of the Gilbert gain cell.)

Applying the same bias and input amplitude to the OTA in measurement yields the spectrum analyzer snapshot of Figure E.8c). The resulting harmonics are

$$\begin{aligned}hd(f) &= -3\text{dBV} \\hd(2f) &= -55.6\text{dBV} \\hd(3f) &= -55\text{dBV}\end{aligned}\tag{Eqn E.15}$$

Removing the $1/s$ low-pass filtration discussed earlier raises the second and third harmonic levels by 6dB and 9.5dB respectively. The pre-bandlimited harmonics are then

Figure E.8c

Measured open-loop OTA spectrum with x10 probe. Input amplitude is $0.42V_{pk}$ at 13 MHz resulting in a $1V_{pk}$ output amplitude plus harmonics.

$$\begin{aligned}
 hd(f) &= -3dBV & (1V_{pk}) \\
 hd(2f) &= -49.6dBV & (4.68mV_{pk}) \\
 hd(3f) &= -45.5dBV & (7.5mV_{pk})
 \end{aligned}$$

Eqn E.16

As discussed in Chapter 5, the linearity is worse in the measured OTA due to mismatches in V_{BE} , V_T and biasing. Once again, the resulting linearity coefficients are found, now for this characterized OTA.

$$\begin{aligned}
 g_{11} &= 390\mu A/V \\
 g_{12} &= 8.67\mu A/V^2 \\
 g_{13} &= 66.2\mu A/V^3
 \end{aligned}$$

Eqn E.17

As a triple-check, these linearity coefficients were used in a macromodel simulation of the open-loop OTA at 13 MHz. The resulting FFT (not shown) confirmed the correctness of this analysis once again by yielding the expected harmonic levels as seen in Eqn E.15.

E.4 *Expected Distortion from Postlayout Simulation of the First-Order, Low-Pass Filter*

Using $0.1 V_{pk}$ (-23 dBV) input amplitudes as a standard, FFTs from postlayout simulations were used to compare against predicted distortion in the low-pass filter, as theorized in Chapter 5. Furthermore, this section provides an appreciation for the differences between the single- and dual-nonlinear transconductor theories.

The IMD products that would theoretically exist from the simple, single-nonlinear transconductor filter are repeated below and would be, at any frequency well below the pole frequency (i.e. near DC)

$$\begin{aligned}hd(f) &\approx \frac{g_{11}}{g_{m4}} V_I \\imd(f_1 - f_2) &= \frac{g_{12}}{g_{m4}} V_{I1} V_{I2} \\imd(2f_2 - f_1) &= \frac{3}{4} \frac{g_{13}}{g_{m4}} V_{I1} V_{I2}^2\end{aligned}\tag{Eqn E.18}$$

To obtain a numerical feel between the single- and dual-nonlinear transconductor theories, these products evaluate to

$$\begin{aligned}hd(f) &= -23dBV \\imd(f_1 - f_2) &= -88dBV \\imd(2f_2 - f_1) &= -100.5dBV\end{aligned}\tag{Eqn E.19}$$

Note the size of the IMD products. Now, consider the dual-nonlinear transconductor theory. The expected theoretical harmonic levels are, at frequencies well below the pole frequency reduce down to

$$\begin{aligned}
 hd(f) &= \frac{g_{11}}{g_{41}} V_I \\
 imd(f_1 - f_2) &= \frac{g_{12} + g_{42} (g_{11}/g_{41})^2}{g_{41}} V_I^2 \\
 imd(2f_2 - f_1) &= \frac{3g_{13} - g_{43} (g_{11}/g_{41})^3}{4g_{41}} V_I^3
 \end{aligned}
 \tag{Eqn E.20}$$

where $V_I = V_{I1} = V_{I2}$. The resulting IMD levels are

$$\begin{aligned}
 hd(f) &= -23\text{dBV} \\
 imd(f_1 - f_2) &= -82\text{dBV} \\
 imd(2f_2 - f_1) &= -\infty\text{dBV}
 \end{aligned}
 \tag{Eqn E.21}$$

The second-order IMD product increases by 6 dB as expected while the third-order IMD product cancels out. Figure E.9 shows the resulting FFT from a postlayout simulation which

Figure E.9 FFT from postlayout simulation of the first-order low-pass filter.

corroborates this quite well. The harmonics are

$$hd(f) = -23dBV$$

$$imd(f_1 - f_2) = -81.8dBV$$

$$imd(2f_2 - f_1) = -106.8dBV$$

Eqn E.22

As may be seen the second harmonic is very close to the predicted theoretical while the third harmonic exists at a higher level due to differences in current exiting the current mirrors between the two Gilbert gain cells from the postlayout simulation.

The theoretical distortion was also corroborated by macromodel simulation for both the single- and dual-nonlinear transconductor cases.

E.5 Expected Distortion from Postlayout Simulation of the Biquad Filter

It is reasonable to expect, at very low frequencies, that the postlayout simulation of the single-ended biquad filter should be the same as the postlayout simulation of the first-order low-pass filter. The results of such a simulation is shown in Figure E.10. As seen, it is nearly identical to

Figure E.10 FFT from post-layout simulation of the biquad low-pass filter.

the postlayout simulation results of the first-order low-pass filter seen in Figure E.9. This result is not unexpected since the transconductance g_{m1} and g_{m4} set the low frequency gain in both these filters. As was the case in the first-order filter, the third-order distortion levels are as high as they are due to differences in current exiting the inner and outer differential pairs of the Gilbert gain cells in simulation, causing a lack of cancellation.

Appendix F

First-Order $\Sigma\Delta$ Modulator

Some additional plots of the spectrums of the bit-stream output of the continuous-time $\Sigma\Delta$ modulator.

Spectrum analyzer plot with inputs just under 1.5 MHz spaced by 0.1 MHz. Inputs are -10dB F.S.

Spectrum analyzer plot with inputs just under 1.5 MHz spaced by 0.1 MHz. Inputs are -15dB F.S.

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