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**AN ULTRA-PRECISION DIGITIZER
FOR INERTIAL SYSTEMS**

By

THOMAS G. FEJES, B.Eng.

**A Thesis submitted to the
School of Graduate Studies and Research
in partial fulfilment of the requirements
for the degree of
Master of Engineering**

**Ottawa Carleton Institute for Mechanical and Aerospace Engineering
Department of Mechanical and Aerospace Engineering
Carleton University, Canada**

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for Inertial Systems"**

submitted by Thomas G. Fejes in partial fulfilment of the requirements for the degree of Master of Engineering.

Prof. Douglas A. Staley
Thesis supervisor

Prof W Martin Snelgrove
Thesis co-supervisor

Prof Robert Bell
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Department of Mechanical and Aerospace Engineering

ABSTRACT

A new Analog to Digital Conversion (ADC) system has been implemented using the most recent 1 bit digitizer technologies. It incorporates improved offset, offset drift and latency characteristics. The final subsystem will be implemented in an inertial Heading Reference Unit (HRU) with an accuracy goal of 1 part per million (ppm) or at least 20 bits. The digital calculation delay or latency is controlled to better than 10 microseconds.

An important component of this research was the 1 bit ADC used in the subsystem design. The 1 bit Sigma Delta conversion technology is the only presently available which can achieve the resolution required for the high accuracy measurements needed in inertial navigation. However, the delays associated with the digital filtering stage could limit its applicability to high performance control system design without the addition of latency correction. Sigma delta conversion technology is explored to better understand the expected performance of these devices.

In any high performance ADC, noise is a concern. Sources of noise are investigated and minimization of these sources is presented.

Implementation of the final system is presented and results from testing show the viability of this new system to measure high resolution signals (about 0.01 ppm) from the gyroscopes in the HRU.

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List of Symbols

ϵ_0	Permittivity of free space (Farads / metre)
ϵ_r	Relative permittivity (Farads / metre)
λ	Wavelength (metre)
μ_0	Permeability of free space (Henry / metre)
ϕ	phase (radians)
Ψ_E	Electric flux (Coulomb)
Ψ_M	Magnetic flux (Weber)
ω	Radian frequency (radians / second)
ADC	Analog to Digital Converter
B	Magnetic flux density (Weber / metre ²)
BW	Bandwidth (Hertz)
c	Speed of light (metre / second)
C	Capacitance (Farads)
CMOS	Complementary Metal-Oxide-Semiconductor
D	Electric flux density (Coulombs / metre ²)
DAC	Digital to Analog Converter
dB	Decibel
DNL	Differential Non-Linearity
E	Electric Field Intensity (Newton / Coulomb)
F	Force (Newton)
f_0	Baseband edge frequency (Hertz)
FIR	Finite Impulse Response
F_Q	Noise Transfer Function
f_s	Sampling frequency (Hertz)
F_x	Signal Transfer Function
G	Gain (decibels)
GBP	Gain Bandwidth Product
H	Magnetic field intensity (Ampere / metre)
HRU	Heading Reference Unit
HSW	H-Switch
Hz	Hertz
I	Current (Ampere)
IIR	Infinite Impulse Response
INL	Integral Non-Linearity
J	Volume current density (Ampere / metre ²)
l	Length (metre)
L	Inductance (Henry)
LSB	Least Significant Bit
M	Mutual Inductance (Henry ²)
n	Number of bits of resolution
N	Filter Order
OSR	Oversampling Ratio

PCB	Printed Circuit Board
PCM	Pulse Code Modulation
Q	Charge (Coulomb)
R	Resistance (Ohm)
rms	Root Mean Square
S	Surface Area (metre²)
SDR	Signal to Distortion Ratio (decibel)
SHC	Sample and Hold Circuit (decibel)
SNR	Signal to Noise Ratio (decibel)
SQNR	Signal to Quantization Ratio (decibel)
t	time (seconds)
VLSI	Very Large Scale Integration
W	Work (Joule)

Chapter 1 Introduction

1.1 General

Inertial measurement and navigation systems are important in the operation of commercial and military aircraft and spacecraft attitude control. Modern systems are highly accurate and reliable, taking advantage of the availability of small, lightweight digital computers.

One problem with present inertial systems is in the conversion of the analog data supplied by the accelerometers and gyroscopes (gyros) to digital data suitable for computation. The accuracy of present analog to digital converters (ADC's) is nearly two orders of magnitude less than the gyro dynamic range. This problem is under active investigation by several researchers [1, 2]. Another problem with presently available converters is the drift characteristic. A secondary issue is latency (speed of response) due to calculations in the digital system and is of concern in high performance control

systems. This research project is an investigation of these problems and has resulted in the development of a new analog to digital conversion system that has improved stability, resolution, drift and latency characteristics.

Increased resolution in the ADC's raises other problems with noise sources that would normally be overlooked. Standard practices in printed circuit board and interface design are not adequate to achieve the required resolution. These aspects of ADC design are also considered in this project.

1.2 Motivational Background

1.2.1 Inertial Navigation

The precise location and orientation of a vehicle can be found using a navigation system. Early dead-reckoning systems resolved airspeeds using directional gyroscopes (gyros) or a magnetic compass to give directional components of velocity. Analog computers were used to determine the distances travelled. Errors in these systems as high as 10% were principally due to errors in the heading reference system. Gyroscopes tend to drift with time and must be periodically reset. Over large distances, the curvature of the earth must also be included in the navigation calculations.

Advances in gyro technology since World War II have allowed inertial systems to be considered for navigation and spacecraft attitude control applications. The market for inertial navigation systems flourished in both military and civil applications, including aircraft and maritime navigation. There are two fundamentally different types of inertial systems presently in use: gimballed and strap-down.

In a gimballed system, all gyros and accelerometers are mounted on a servo driven, mechanically gimballed "stable platform" that isolates the instruments from the angular velocity of the vehicle. Gyros are used to sense angular rotations and command

the servos to rotate the platform in the opposite direction. In this manner, accelerometer outputs are integrated twice to determine distance travelled. These gimbaled systems have the disadvantages of being costly, prone to mechanical failure, prone to "lock up" modes if incorrectly designed and require long "warm-up" times. They are, however, very accurate.

Technical advances over the past 30 years, including the Apollo lunar module in the late 1960's, have allowed the gyros and accelerometers to be mounted directly (or strapped-down) to the airframe. In a strap-down system, gyros measure the angular rate of rotation of the vehicle and accelerometers measure unresolved accelerations. Digital computers use the rotation rate information to resolve the accelerations into vehicle coordinates and calculate required navigation parameters. Strap-down systems are difficult to align and calibrate, however, they are mechanically simple, smaller and lighter than gimbaled systems, and are therefore inherently more reliable. Another important characteristic of strap-down systems is that they require much more computation than gimbaled systems.

Gyroscopes are a mature technology with few new fundamental developments recently, but many improvements. Most current systems use tuned rotor, ring laser or fibre optic gyros. The most accurate units can measure angular rotations with a resolution of 0.001 parts per million (ppm) which is well beyond the resolution and dynamic range of most analog to digital converters (ADC's).

There are two approaches taken to improve the resolution of the overall inertial system, one based on a pure digital rebalance with pulsed current and the other on ultra-precise ADC's.

1.2.2 Digital Rebalance Loop Heading Reference Unit

The digital rebalance loop Heading Reference Unit (HRU) developed at Defence Research Establishment Ottawa is shown in Figure 1.1. The gyro rotor angle data is collected by the analog electronics and converted into digital format using ADC's. The digital input is used by the processor to generate control signals to rebalance the gyros through the H-Switches and an electronic interface board. The navigation processor uses the gyro control pulse data and accelerometer data to calculate the current position.

The wheel supply provides the necessary power to the spin motors of the tuned rotor gyros. The X-axis and Y-axis ADC's are 12 bit components that measure the gyro data pick-offs and are used for feedback control (rebalance) of the gyro and bandwidth augmentation in the navigation algorithms.

The H-switches are high technology Field Effect Transistor (FET) switching systems that are capable of high speed, high current and high accuracy operation. The electronic interface board is used to translate the outputs from the H-switches into appropriate inputs to the gyros. Due to the high speed and high current, the switches have demonstrated a tendency to deteriorate and fail over a random period of time. The H-switch electronics is currently under evaluation in another research program. Results of that evaluation may show that the H-switch is not a viable technology for inertial systems in the long term. The problems with the H-switches have prompted the design of a new analog rebalance loop HRU which uses analog to digital converters.

Kalman filters help reduce errors caused by the loss of resolution resulting from the process of converting the analog signal into digital form. The Kalman filters model the gyro outputs given servo (known in the field as torquer) inputs and outputs (pick-offs). The Kalman filters provide control signals to the H-switches to stabilize the gyros and aid the navigation software to provide position and heading data.

Figure 1.1 : Digital Rebalance Loop Heading Reference Unit. Note the use of H-Switches (HSW) to Command the Tuned Rotor Gyroscopes in the Digital Feedback Loop.

1.2.3 Analog Rebalance Loop Heading Reference Unit

The proposed analog rebalance loop HRU is shown in Figure 1.2. The gyros are stabilized directly with analog rebalance circuitry without using H-switches. Analog loops are well known and have been proven to work reliably. Fast analog electronics are not needed and most of the components required already exist for the HRU. Here, the digital output from the ADC's is fed directly into the processor that performs the navigation algorithms. The bandwidth of the gyros, which use an analog rebalance loop, is between 20 and 40 Hz.

The accuracy and resolution in the digital signals must be at least comparable to the performance of the analog equivalent. Extremely high resolution converters are available at the expense of additional delays in the system. Although latencies in audio and seismic applications are of no concern, latency in real time control and measurement systems must be kept to a minimum to maintain stability. In the HRU, where real time data is used to stabilize a platform and to measure attitudes for data processing, additional latencies may result in degraded performance of the system. The stable platform includes mechanical resonances in the 10 Hz range and for adequate control and a high degree of accuracy, latencies must be less than a millisecond or better.

The main concern surrounding currently available high resolution ADC's is offset drift. Although offset can be nulled for any converter, the offset drift is difficult to model and varies not only with temperature but also time.

Comparing Figures 1.1 and 1.2, the decreased number of components and the elimination of the troublesome H-switches in the latter illustrates the desire to use the analog rebalance loop HRU. Other advantages of the analog rebalance loop unit are:

- 1) reduced computational requirements and
- 2) simplified control of the gyros.

Figure 1.2 : Analog Rebalance Loop Heading Reference Unit. Note the Analog Loop Placed Directly around the Gyroscopes. The X and Y-Axis ADC's are Used for Bandwidth Augmentation

1.3 Thesis Outline

The development of the final system takes a "bottom-up" rather than a "top-down" approach. The elemental components are described in detail in earlier chapters and their interconnection is discussed in later chapters.

Chapter 2 provides a general introduction to current ADC technologies and their limitations. The topic of sigma delta conversion and the problems usually associated with ADC's are discussed in detail.

Chapter 3 is a discussion of the problems encountered when designing high accuracy ADC systems. Noise sources are identified, and suggestions for their minimization given. Printed circuit board design for high accuracy systems is covered in detail. Selection criteria of the cables for electronic signals, and the interface between the cables and the support electronics, is given.

Chapter 4 is an investigation of the current limitations of the components that will be used in the development of the new ADC system. The expected performance of the new system is also discussed. The design of the electronics and software of the new system and the experimental data acquisition and the test set-up are also presented.

In Chapter 5 the results of the tests demonstrating the performance of the new ADC design are presented and discussed.

Finally, conclusions and recommendations for future work are given in Chapter 6.

1.4 Definitions of Terms

This thesis contains terminology that has been freely used in many references. For example, many authors do not distinguish between accuracy and resolution while others assume the Signal to Noise Ratio (SNR) includes Quantization and Harmonic

distortion as well. For clarity, all terms are defined in Appendix D and conform to the usage presented in most of the references.

1.5 Objectives

The strap-down HRU using two degree of freedom gyroscopes will be controlled by analog rebalance loops. The required dynamic range of the analog to digital converters will be from $0.01^\circ/\text{hour}$ to $400^\circ/\text{hour}$ ($1\mu\text{V}$ to 10V). Existing converters which can provide the resolution for this dynamic range have output rates of only 1Hz. For this application, output rates of up to 200Hz are needed.

The objective of the present program is to explore the use of multiple analog to digital converters to obtain a better offset drift and latency characteristic, and better dynamic range with increased output rates. Current high resolution converter technologies will be explored and their potential implementation into the HRU will be studied. Reduction of latencies in the conversion process will also be studied and solutions to this problem will be presented.

A major objective of the program is to design and implement an analog to digital conversion system that demonstrates improved offset and drift characteristics to presently available units. The final product of the present program will be a subsystem component that will be implemented into an analog rebalance loop inertial heading reference unit.

Chapter 2 Analog to Digital Conversion

2.1 Introduction

For any digital system to interface to an analog system, an analog to digital converter (ADC) is required. An analog to digital converter is a device that accepts an analog input (a continuous voltage or current signal) and quantizes it into a finite number of levels. The number of levels, or resolution, of the converter is determined by the number of output bits of the converter. The output bit stream is a digital representation of the input signal level.

For example, in a high accuracy 16 bit converter, there are $2^{16}=65536$ discrete reference levels. With a 2 volt input dynamic range, each level is $(2V/65536) = 30\mu V$ apart. This level of voltage resolution is beyond the limit of typical ADC's implemented in standard Very Large Scale Integrated circuit (VLSI) technology.

For low cost systems, the analog input, conversion and signal processing circuitry should be integrated onto a single silicon chip. Problems with designing and producing an integrated digital-analog chip are:

- 1) The silicon process is optimized to produce digital circuitry and not analog components.
- 2) The integrated digital circuitry may add unwanted high frequency power supply and substrate noise which can couple onto the input analog signal and degrade the converter performance.

Newer technologies have the resolution required for inertial systems, however, even with "auto-zero" circuitry, offset and drift are limitations on the performance of these devices.

To obtain the high accuracy required for inertial applications, these and other noise sources must be identified and minimised. The "traditional" ADC technologies are not sufficient to achieve the resolution and the accuracy required for gyro control.

This chapter introduces the reader to the topic of ADC and provides an overview of the existing technologies used. The main emphasis in this chapter is sigma delta modulation, a relatively new technology that makes use of oversampling and digital filtering.

The components of the sigma delta modulator are discussed in detail and trade offs are proposed for each component. An advantage of sigma delta is that high resolution converters can be made with simple and robust analog circuits.

2.2 Analog to Digital Converter Architectures

There are two basic types of analog to digital converters. The first type operates near the Nyquist rate, which defined as twice the maximum frequency of interest, and is a basic parameter of all digital system design. Further information on the Nyquist rate

and its relationship to sampling frequencies is available in Oppenheim [3]. The most common converter of this type is the linear pulse code modulator (PCM). The second type of converter architecture is the oversampling converter. The first section of this chapter presents a discussion of the existing architectures for analog to digital conversion. A classification of these converters is shown in Figure 2.1.

2.2.1 Nyquist Rate Analog to Digital Converters

A typical ADC converter is shown in Figure 2.2. In general, an ADC will accept an analog signal (a voltage or a current) as an input. An input is shown in Figure 2.3 (a) as a triangular spectrum with white noise distributed throughout the frequency band. An anti-alias filter removes the out-of-band noise to allow sampling at the Nyquist rate (twice the base band frequency). An anti-alias filter is shown in Figure 2.3 (b) as a low pass function that has its cutoff (half power point) at half the sampling frequency. The output of the filter is shown in Figure 2.3 (c), clearly leaving some noise that will be aliased into the passband after sampling. A sample and hold circuit is used to allow the ADC to quantize the input signal to discrete levels. The discrete levels are transformed into a digital representation of the analog signal. The frequency domain representation of the digital output is shown in Figure 2.4. Excellent explanations of various ADC implementations are given in the references, but a brief introduction to the most common types of ADC's will be given below.

Nyquist rate converters require high accuracy analog components in the anti-alias filter stage to achieve high resolution by removing the noise above the Nyquist rate. For a high accuracy ADC, the SNR should be better than 96 dB. "Brick wall" anti-alias filters are not achievable and even with high accuracy filters, some noise is still aliased into the passband.

Figure 2.1 : Analog to Digital Architecture Technologies

Figure 2.2: A Simplified Analog to Digital Converter

(a) Input Analog Signal with White Noise

(b) Anti-Alias Filter Response

(c) Anti-Alias Filter Output

Figure 2.3 : A Typical Analog to Digital Conversion Process

Figure 2.4 : A Digital Output Sampled at the Nyquist Rate

Another disadvantage of the high resolution anti-alias stage is the addition of non-linear latency to the system near the cutoff frequency. There are many types of filters available for anti-aliasing, such as maximally flat and minimum ripple. Each filter has its own merits, and the reader is directed to the references for detailed discussions on each [3, 4]. The best type of filter depends on the specific application.

Sample and hold circuits (SHC) are used to store an analog voltage accurately over a specified time while a PCM converts the held voltage into a digital word. SHC's are made up of a very fast switch driver to sample the input and a capacitor to hold the signal. Delays in the switching driver result in switching errors, usually caused by Gain Bandwidth Product (GBP) limitations of the FET switch. The charge time of the capacitor or "slew rate" limits the conversion time and is often the limiting factor in an SHC operating speed. The finite amplifier output and switch resistance will cause the held signal to settle exponentially to its ideal output value. Associated problems with timing and amplitude are discussed by Darling and Hawksford [5] and Snelgrove [6].

Quantizer errors are caused by the finite representation of input signals with infinite spectral components. Ideally, the anti-alias filter will have removed all the out-of-band noise and the sampling process will have added no additional noise. Any input signals that go out of the range of a quantizer level are assigned the next quantizer level.

Quantizer errors can be modelled as an additive noise source. Assuming that the quantizer errors and input signal are statistically independent (valid for a sinusoidal input that just saturates the converter) the Signal to Quantization Noise Ratio (SQNR) can be expressed as:

$$SQNR = 6.02 * n + 1.72$$

2.1

where SQNR is in dB and n is the number of bits. Equation 2.1 shows the performance of the converter will improve by 6 dB for each additional bit of resolution. The constant coefficient 1.76 dB will be different for input signals other than a pure sinusoid.

It is important to note that this expression is inaccurate for small input signals that are spectrally simple (for example, when only the Least Significant Bit (LSB) is changing). The quantization non-linearity is approximately constant in amplitude as the input signal gets smaller.

2.2.1.1 Pulse Code Modulation

The most common form of ADC found in commercial pulse code modulation is the successive approximation converter. The basic successive approximation architecture is shown in Figure 2.5. Successive approximation converters use a single comparator, a successive approximation register and a Digital to Analog Converter (DAC) in a feedback fashion to achieve about 12 bits of resolution (a limitation due to the DAC). The successive approximation register finds the digital word which will produce the best approximation to the held input error signal. The digital word is fed back into the comparator to produce the next error signal. Note that even with high performance operational amplifiers (opamps) the GBP of 5 to 70 MHz will generate a 10 μ V broad band rms noise voltage. The peak input signal must be scaled to at least 2.5 V to achieve 16 bits of resolution. This architecture is popular because of its simplicity and low power consumption.

Differential PCM (DPCM) provides a reduction in the output bit rate for a given quality by digitizing the difference between two adjacent samples of the analog input. A differential modulator is shown in Figure 2.6.

Figure 2.5 : Successive Approximation Architecture

Figure 2.6 : Differential Pulse Code Modulation Architecture

The quantizer converts the difference between the current and the previous input sample, such that the relation of the output to the input is:

$$Y_n = X_n - X_{n-1} \quad 2.2$$

where Y_n is the output of the DPCM converter, X_n is the current input sample and X_{n-1} is the previous input sample.

DPCM is useful for inputs with a large dynamic range, especially music, which have a smaller time rate of change. Darling and Hawksford [5] suggests that for such signals, DPCM offers a 6 to 10 dB advantage over PCM operating at the same clock frequency. The SQNR is dependent on the input signal for both PCM and DPCM, so a noise analysis is dependent on the application.

Although PCM has become a standard for converting signals at the 16 bit level, many other "standard" converter technologies have evolved. Examples of other general purpose converters are:

Flash converters:

These converters are typically extremely high speed and low precision and are used in video applications. The input signal is usually connected to a resistor string, and comparators are used to determine a distinct threshold level. The resulting "thermometer" code is converted digitally to a binary output. Since the number of comparators in these converters increases geometrically with resolution, they can quickly consume a large power budget. These converters rarely achieve better than 8 bit resolution.

Two-Stage and Pipeline Converters:

A two-stage converter can be created by cascading a reduced accuracy ADC with a DAC and finding the error signal from the original analog signal. The error signal is converted and the result of the two conversions is a maximum resolution

of about 10 bits. The two-stage converter can be extended to multiple stages. This design consumes less power but runs more slowly than the Flash converter described above. The pipeline converter avoids this reduction in speed by sampling the error signal and allowing the following sections to do a fine conversion on the previous sample. The output from each stage is delayed so that the output sample is aligned for each stage.

Algorithmic converters:

Algorithmic converters calculate the error signal using a single comparator (as in a Two-Stage converter) and cycle it through a loop. This architecture is power efficient although very slow. Rather than having a fixed reference, the reference signal and the input are circulated through the loop.

Integrating and Double Integrating:

These converters use a single comparator with a ramp input as a reference and perform a high speed count. The number of counts is used to determine the digital output. Multiple ramps can be used to achieve higher resolution. The maximum resolution obtainable with these converters is about 16 bits.

2.2.2 Oversampling Analog to Digital Converters

Oversampling PCM

Using a sampling frequency much higher than the Nyquist rate (typically more than 16 times higher) allows the elimination of high performance anti-alias filters in the design. The noise is spread over the spectrum such that baseband noise is reduced. Oversampling alone will decrease the noise power in the baseband by distributing it over a wider spectrum. Digital filters following the conversion stage are used to remove the high frequency noise in the stopband more effectively than analog filters [7].

An implementation of an oversampled input is shown in Figure 2.7. The oversampling ratio (OSR) is:

$$OSR = f_s / (2 * f_c) \quad 2.3$$

where OSR is the oversampling ratio, f_s is the sampling frequency and f_c is the maximum baseband frequency. For Nyquist sampling the OSR would be unity. Note that some references refer to the Oversampling number that is the ratio of the sampling frequency, f_s , to the baseband frequency, f_c .

Increasing the OSR will improve the SQNR. Expressing this in decibels yields a total SQNR of:

$$SQNR = 6.02 * n + 1.72 + 10 \log_{10} OSR \quad 2.4$$

Equivalently, the oversampling ratio could be expressed in octaves such that $OSR = 2^L$ where L is the number of octaves of oversampling. The SQNR can now be expressed as:

$$SQNR = 6.02 (n + 0.5 L) + 1.76 \quad 2.5$$

Equation 2.5 shows that for PCM, a doubling of the OSR decreases the noise by 3 dB and increases the resolution by half a bit. In theory, an infinite OSR would yield infinite SNR. This objective is clearly limited by the settling time of the fastest opamp.

Figure 2.8 illustrates the noise reduction property of oversampled systems. Figure 2.8 (a) highlights the noise power in the band of interest for a system sampled at the Nyquist rate. Figure 2.8 (b) illustrates this power density spread out over a larger spectrum.

The delta modulation system and the sigma delta modulation system are examples of oversampled systems. These are discussed in the following sections.

Figure 2.7: An Illustration of the Oversampling Ratio

(a) Input Signal Sampled at the Nyquist Rate

(b) Input Signal Oversampled

Figure 2.8: An Illustration of the Noise Reduction in Oversampled Systems

Delta Modulation

Delta modulation is a well established method of converting analog signals into a digital pulse train [5, 8, 9]. Figure 2.9 (a) shows the block diagram for the delta modulator. The principle of operation of the delta modulator is to quantize the change in the signal from sample to sample rather than quantize the absolute value of the signal at each sample. The integrator in the feedback path acts as a predictor, attempting to minimize the error at each sample. The error term is used to make the next prediction. Figure 2.9 (b) shows an example of the output for a sinusoid input from the delta modulator. For an increasing input slope, the predictor will output a larger ratio of "high" values and for decreasing input slope, a larger number of "low" outputs. The output of the integrator is shown in Figure 2.9 (c). This signal can be low pass filtered to reconstruct the input analog signal.

Delta modulators may exhibit distortion due to gain non-linearities and the spectral shape of the noise power depends on the step size imbalance and quantizer hysteresis. The primary use of delta modulation is for storage or transmission of analog signals due to its reduced bit rate.

Sigma Delta Modulation

For modulation and demodulation, delta modulation uses two integrators, as shown in Figure 2.10 (a). Since integration is a linear operation, the second integrator can be moved before the modulator without effecting the characteristics of the converter. The two integrators in Figure 2.10 (b) can also be combined into one integrator using the linearity property. The resulting structure in Figure 2.10 (c) is called a sigma delta converter.

(a) Delta Modulator Architecture

(b) Sample Output from a Delta Modulator

(c) Sample Output from a Linear Predictor

Figure 2.9 : Delta Modulation

(a) Delta Modulator and Demodulator

(b) Delta Sigma Modulator and demodulator

(c) Simplified Delta Sigma Modulator and Demodulator

Figure 2.10 : Deriving a Sigma Delta Modulator from a Delta Modulator

The term "sigma delta" modulation is derived from the placement of an integrator (sigma) in front of a delta modulator. The output of the sigma delta modulator has one bit resolution at a frequency much higher than the Nyquist rate. The output of the sigma delta modulator differs from the delta modulator due to the integrator in the feedback loop. For larger inputs, the output will be a larger proportion of "high" outputs, and for smaller inputs, there will be a larger proportion of "low" outputs.

Unlike the delta modulator, the quantization noise characteristic of the sigma delta modulator is frequency dependent, that is, the noise can be "shaped" such that the noise in the band of interest is reduced.

Noise shaping is best described by Figure 2.11. The sigma delta modulator main loop integrates the error between the sampled output and the sampled input signal. A simplified first order sigma delta modulator is shown in Figure 2.11 (a). If the one bit quantizer is represented as an additive noise source, $Q(z)$, the transfer function is:

$$Y(z) = Q(z) + (X(z) - Y(z) z^{-1}) I(z) \quad 2.6$$

where $X(z)$ is the sampled input signal, $Y(z)$ is the output bit stream and $I(z)$ is a discrete integrator. If the integrator is replaced by an ideal representation as shown in Figure 2.11 (b), that is:

$$I(z) = 1 / (1 - z^{-1}) \quad 2.7$$

then we can represent the sigma delta modulator as shown in Figure 2.11 (b). The above transfer function now simplifies to:

$$Y(z) = Q(z) (1 - z^{-1}) + X(z) \quad 2.8$$

The input signal has unity gain. The $(1 - z^{-1})$ term is a differentiator and doubles the power of the quantized noise, however, it has also shifted it to a higher frequency [8].

(a) Simplified First Order Sigma Delta Modulator

(b) Expanded First Order Sigma Delta Modulator

(c) In-Band Noise for Different Converters

Figure 2.11: A First Order Sigma Delta Modulator

The noise transfer function can be calculated [7, 10, 11] for the sigma delta modulator as is shown in Figure 2.11 (c) to be:

$$F_Q(j\omega) = 2 \sin(\omega/2) \quad 2.9$$

where $F_Q(j\omega)$ is the noise transfer function. The figure also compares the noise characteristics for the one-bit Nyquist sampler, the oversampler, the first, second and third order sigma delta modulators.

The z-plane and frequency domain representations of this transfer function are shown in Figure 2.12 (a). Clearly, the effect is high pass filtering of the noise. This demonstrates the frequency dependent "noise shaping" property of the sigma delta modulator.

Note that the poles of the forward filter will be the zeros of the noise transfer function. In practice pole zero placement of the system will be as shown in Figure 2.12 (b). This method reduces the likelihood of instability. The zero is moved inside the unit circle, and the low frequency noise attenuation is degraded as shown

Since a one bit quantizer is used in the sigma delta, the system is inherently linear. Linearity error is limited only by the imperfections in the input SHC

The process of oversampling improves the resolution of the converter by half a bit for each doubling of the sampling frequency. It can be shown that for the first order sigma delta modulator, each doubling of the sampling frequency reduces the noise by 9 dB and increases the resolution by 1.5 bits [7].

The remainder of this chapter will discuss the implementation of sigma delta analog to digital conversion

2.3 Sigma Delta Analog to Digital Conversion

2.3.1 Introduction

Sigma delta modulation was developed in 1962 but only recently had commercial implementation due mostly to recent advances in VLSI technology. The advance required was the use of fine-line Complimentary Metal Oxide Semiconductor (CMOS) VLSI that allowed the implementation of several thousand gates to perform the digital decimation or interpolation filters. Early sigma delta converters were limited to voice band coder and decoders (codecs). Sigma delta converters naturally lend themselves to VLSI technology since only a small amount of simple analog circuitry is required in the design. Also, sigma delta converters do not require component trimming to achieve high resolution in the conversion process. The analog architecture lends itself to switched capacitor implementation [6, 12]

Figure 2.13 illustrates the difference between sigma delta modulation and sigma delta conversion. The process of converting the high speed 1 bit output from the modulator into a lower frequency, standard coded PCM signal is done by digital decimation and filtering

2.3.2 Classification of Sigma Delta Converters

Sigma delta converters can be classified by two structures: classic and cascaded.

Classic Sigma Delta Converters

The classic first order structure is a single modulator followed by a digital low pass decimation filter as shown in Figure 2.14 (a). The noise characteristic of this converter is limited by the digital filter, oversampling ratio and resolution of the feedback loop.

(a) Ideal Noise filtering characteristics

(b) Effect of guaranteed stability

Figure 2.12: Z-Plane and Frequency Response of the First Order Modulator

Figure 2.13 : Sigma Delta Modulation in Analog to Digital Conversion

Increasing the modulator order is also a means of reducing the noise level, however, stability is a concern for modulators of order greater than two or three when using one bit quantizers. Instability may also be due to variations in circuit parameters.

Candy [10] introduced a method of increasing the order of the sigma delta modulator. The second order system principle he suggested is shown in Figure 2.14 (b), highlighting the use of a first order modulator and a second feedback loop. Although he suggested reasons against modulators of order greater than two, several others developed higher order modulators achieving higher resolution [1, 14 - 17]. All designers dealing with modulators of order greater than two discuss in great detail the methods used to stabilize their designs. It was shown previously that doubling the OSR for PCM increased the resolution by half a bit and for first order noise shaping the resolution increased by one and a half bits. Doubling the OSR with second order noise shaping increases the resolution by two and a half bits.

Adams [1, 14] achieved 18 and 20-bit resolution using noise shaped PCM rather than sigma delta because of reduced sensitivity to waveform asymmetry and limitations in the stability of higher order sigma delta modulators.

Welland et al [16] designed a fourth-order sigma delta shown schematically in Figure 2.14 (c). The main difference between this implementation and the normal classic fourth order modulator is the location of the quantizer and the use of feedback to maintain stability. Welland's design team noted the regions of stable operation and provided circuitry to detect excessive integrator levels as an indication of instability. The unstable integrators would be reset at power up and during the excessive levels. There was no effect on the output of the circuit due to resetting the states in the unstable integrators. This design achieved 16 bit, 24 kHz performance.

Norsworthy et al [17] achieved 14 bit 80 kHz performance with a second order modulator similar to Candy's earlier design.

Adams [18] revealed a new approach to simplify the analysis of high-order loops using differential switched capacitor techniques and an unusual loop topology to achieve 18 bit resolution.

Cascaded Sigma Delta Converters

Cascaded structures use multiple low order (usually $N = 1$ for simplicity) modulators to obtain high order noise shaping. The first stage of the structure converts the input analog signal and each subsequent modulator converts the error signal from the previous modulator. This concept is shown schematically in Figure 2.14 (d).

The advantages of cascading first order modulators are clear: stability to any order, no noise degradation with increased input amplitudes and the architecture easily allows itself to be pipelined.

The main disadvantage of the cascaded architecture is the sensitivity to the component accuracy. The main component which limits the accuracy of these components is the switched-capacitor integrator. Manufacturing techniques and analysis of these devices is currently an intense field of research [12]. The integrator components must have an almost ideal transfer function. Otherwise, there will be leakage of the first order shaped and un-shaped noise into the output of the converter.

For the second order modulator, the noise ideally falls by 15 dB and the resolution increases by 2.5 bits. Another way of looking at the cascading effect of sigma delta modulators is to consider the feedback transfer function as improving the noise rejecting characteristics of the modulator. In general, for a modulator of order N the noise decreases by $3 * (2 * N + 1)$ dB and the resolution increases by $(N + .5)$ bits.

(a) First Order Classic Sigma Delta Modulator

(b) Second Order Classic Sigma Delta Modulator

(c) A Schematic Fourth Order Classic Sigma Delta Modulator

(d) A Schematic Third Order Cascaded Sigma Delta Modulator

Figure 2.14: Classic and Cascaded Sigma Delta Converters

An early use of cascaded sigma delta conversion (sometimes called MASH or multi-stage noise shaping) was published by Matsuya et al [19]. The outputs of the individual first order sigma delta modulators were combined using differentiators to achieve 16 bit resolution with a 24 kHz bandwidth.

Using an architecture similar to the one described by Matsuya et al, Rebeschini et al [20] achieved 16 bit performance with a 160 kHz bandwidth. The design made use of a novel auto-zero switched capacitor integrator which reduced the leakage of un-shaped quantization noise for a given opamp gain. The resulting gain in the bandwidth of the opamp allowed an increase in the bandwidth of the converter. Rebeschini also found that the limitation of the cascaded architecture was the dependency on the accuracy of the analog components which cancel the quantization noise of the first modulator.

2.3.3 Digital Decimation and Filtering

The digital decimation and filtering stage following the sigma delta modulator (Figure 2.13) is used to convert the high frequency, low resolution modulator output into a lower frequency, higher resolution standard output code format, such as PCM. The digital decimation and filtering stage must:

- 1) remove quantization noise that could be aliased into the baseband,
- 2) convert the high frequency 1 bit data to lower frequency multiple bit data and
- 3) provide anti-aliasing to remove the out-of-band noise before conversion to the Nyquist rate.

Digital Decimation

The act of digital decimation converts a given signal sample rate to a lower sample rate. A sampling rate reduction of M is achieved by forming a new digital signal by

saving only every M th sample of the filtered output [21]. The sampling frequency must be brought down from the oversampled value to some intermediate value before the anti-aliasing stage.

Digital decimation can also be thought of as a resolution enhancer. This idea arises from the digital arithmetic in the decimator and must have adequate word width to support added resolution. The increased resolution caused by increasing the OSR in PCM and noise shaped systems has been demonstrated earlier in this paper.

Filtering

The quantization noise generated by the sigma delta modulator must be removed from the signal output. The output of the sigma delta modulator is at a high frequency, so simplicity in the low pass filter is important. There are many possibilities for the digital filter stage, and the designer must select the "correct" filter based on the requirements of the system. The following sections briefly introduce the most commonly available filters.

There are two standard types of digital filters, finite impulse response (FIR) and infinite impulse response (IIR). IIR and FIR filters are also known as recursive and non-recursive filters respectively.

Finite Impulse Response Filters (FIR)

FIR filters are desirable in many applications because of their linear phase characteristic and their inherent stability. Decimation can be incorporated directly into the filter to achieve a simpler computational requirement. The main drawback of the FIR filter in this application is the inherent delay associated with them. FIR filters can only implement zeroes, no poles, so their stopband attenuation or roll-off is limited.

The comb filter (moving average filter) is the simplest filter to use for removing the quantization noise, since all its coefficients are unity and do not require multipliers. The frequency response of a single comb filter is a "sinc" function and may not have enough attenuation in the stop bands. Figure 2.15 (a) illustrates the comb filter in the time domain and the frequency domain.

Figure 2.15 (b) shows an analog sinusoid input and its sampled equivalent. The input sinusoid is repeated around the sampling frequency when sampled. Also shown in the figure is the equivalent noise power if the signal were not oversampled. Figure 2.15 (c) shows the effect of filtering the sampled signal. The delay is exaggerated in this figure to illustrate the effect of filtering. The noise in the high frequency range is attenuated, with a smaller amount of attenuation in the passband. To achieve the necessary SNR cascaded comb filters are used to achieve the required result. Figure 2.15 (d) shows the advantage of using cascaded comb filters to achieve better attenuation in the stopband. Figure 2.15 also shows the delay effect in the time domain. Cascaded filters will increase the delay as shown in the time domain. Figure 2.15 (e) shows a decimated signal and the aliasing of the unfiltered noise into the passband.

The tapped delay line filter has much better filter characteristics than the comb filter. Sharper cutoff and higher attenuation are needed to remove the out-of-band noise before the signal is re-sampled at the Nyquist rate. Since the comb filter and first decimator have already decreased the sampling frequency, the transition band is much larger and more accurate filtering can be done at this stage. A simple comb filter first stage and more complex filter following the decimation stage is usually preferred.

Figure 2.16 (a) shows an input sinusoid to a third order sigma delta ADC. Figure 2.16 (b) shows the output of a third order sigma delta modulated signal superimposed on the input signal.

(a) Comb Filter

(b) Sampled Input Signal

(c) Filtered Signal

(d) Effect of Cascaded Filters

(e) Decimated Signal

Figure 2.15: Finite Impulse Response (FIR) Signal Filtering

The noise shaping characteristic can clearly be seen in the frequency domain. Also notice the larger proportion of harmonics produced by the modulator. These harmonics can be made insignificant by proper design of the digital filter stages. Figure 2.16 (c) shows the output of the single stage comb filter in the time domain and the frequency domain. The largest harmonics have been removed along with most of the shaped noise. Here, it can be clearly seen that the attenuation of the single stage is insufficient. In comparison, Figure 2.16 (d) shows the frequency response of four cascaded 16'th order comb filters with a larger attenuation in the stopband.

Common FIR filters are the Comb, Hamming, Hanning, Blackman, and Bartlett and are shown in Figure 2.17. Kaiser developed a method that produced near optimal FIR window results given the required frequency response. Parks McClellan Optimum filters are recursively calculated to achieve the required frequency response.

Infinite Impulse Response Filters (IIR)

Infinite Impulse Response (IIR) filters use past output data to calculate new output signals. There are several advantages to the IIR filter design:

- 1) The ability to use available analog filters and transform them into digital form.
- 2) Reduced mathematical complexity for an improved frequency response characteristic .
- 3) Lower group delay in the passband (The group delay is defined as the negative rate of change of phase with respect to frequency, indicating the degree of non-linearity in the phase).

Improved characteristics are achieved since IIR filters can implement zeroes and poles.

Figure 2.16 . Filtering Sigma Delta Converters

Figure 2.17 : Commonly Used Finite Impulse Response Filters

Note that the window functions have been plotted as continuous functions however, the functions are defined only at integer values of 'n'.

The disadvantages of IIR filters are

- 1) Non-linear phase response that usually results in an increased group delay at the passband edge for decreased transition bands.
- 2) The decimation stage must be done separately and cannot be built into the filter.

Typical analog filters that can be transformed into digital IIR form are Butterworth, Chebyshev, Elliptic, and Bessel filters. Many texts discuss the design of these filters in detail and so they will not be discussed here [3, 4, 21]. The Gaussian filter is not well documented and since it is important in the present project, its characteristics are discussed in Appendix A.

2.4 Error Sources in Sigma Delta Analog to Digital Converters

2.4.1 Introduction

Although the improvements achieved by sigma delta over conventional ADC's were shown in the previous section, this technology is not without its error sources. The limiting error sources are harmonic distortion, clock jitter, limit cycles that overload the quantizer and quantization noise.

Stability of the measurement system may be a concern. When discussing stability, it is necessary to consider both AC and DC stability. Any system using feedback also may be susceptible to instability.

2.4.2 Harmonic Distortion

It was found that AC input signals which were within 10 dB of the dynamic range (where 0 dB is defined as an input whose peak to peak amplitude equals the spacing between the two quantization levels) is a source of odd harmonic distortion. The third harmonic may actually dominate and will limit the Signal to Distortion Ratio (SDR) [17].

2.4.3 Limit Cycles

The quantizer in an oversampler has outputs that vary between levels in a way that keeps the average value equal to the input [10, 22]. When the input is steady, the output of the oversampler is a series of recurrent pulses that are dependent on the input level. The output will be noisy if the repetition rate of the output recurrent pulses is in the band of interest. In this case, the assumption that the quantizer is an additive white noise source becomes invalid. Candy and Benjamin [22] noted the noise is largest when the modulator input is biased near the ends of its range and next largest near the centre.

It has been demonstrated that limit cycle behaviour can be reduced using dither [23 and 24]. Dither forces the ADC input to be "busy" rather than have a low amplitude signal. The dither is usually removed digitally from the signal after conversion. It has been shown that in oversampled systems the dither can be a square wave at integer multiples of the final sampling rate. These locations were ideal since they were coincident with the zeros of the digital filter stage.

Limit cycle behaviour is more severe in first order modulators than in higher order modulators.

2.4.4 Quantization Noise

Quantization noise was discussed earlier in this chapter for standard PCM converters. It was shown that the sigma delta modulator shapes the quantization noise so that the passband noise performance is improved at the expense of the stopband. Many have studied the effects of quantization noise and have published methods of calculating the quantization noise for sigma delta converters of any order [13, 17, 22, 26].

2.4.5 Clock Jitter

Sampling clock jitter causes non-uniform sampling and increases the error power in the quantizer output. The magnitude of the error power is a function of both the statistical properties of the jitter and the ADC. An increased OSR decreases the amount of error permissible due to clock jitter.

Harris [25] showed that oversampled sigma delta analog to digital converters are less sensitive to random white clock jitter than Nyquist rate PCM converters. Also, sigma delta analog to digital converters and Nyquist rate PCM converters are equally susceptible to the effects of sinusoidal clock jitter.

2.4.6 AC Errors

Stray capacitance on inputs of feedback circuits may lead to stability problems. The stray capacitance can represent a potential phase shift at a corner frequency of:

$$f = 1 / (2 \pi R_f C_s) \quad 2.10$$

where f is the corner frequency in Hertz, R_f is the feedback resistance in Ohms and C_s is the stray capacitance in Farads.

The problem increases with increased R_f because the inverse in Equation 2.10 relationship may interfere in the band of interest. The cumulative effect of the phase shifts may cause oscillation. However, reducing R_f may not be possible for gain reasons, so a more common solution will be to use a compensation capacitor, C_f , which creates a frequency compensated divider. The value of C_f is not precisely known and is usually found by experimentation. In practice, 3 pF to 10 pF capacitors are used with feedback resistors of 10 k Ω .

A similar phase shift problem can occur if the stray output capacitance is greater than 100 pF. Addition of a series output resistance isolates the output stray capacitance

from the amplifier. A feedback capacitor C_F is added to reduce the gain of the loop at high frequencies. Typical values for C_F are again 3 pF to 10 pF.

2.4.7 DC Errors

Flicker noise (also known as $1/f$ noise) is a low frequency source that is found in non-equilibrium systems, where a DC current is flowing. Spectral density is inversely proportional to frequency. Sources of flicker noise are related to surface properties of materials and imperfect contact between connectors.

High quality passive components must be used. For example, external gain setting resistors must be high stability, low temperature coefficient types. Converters should be selected which provide internal gain setting resistors

2.4.8 Voltage Offset

Ideally, systems will have zero output voltage for zero input voltage. Practical systems will have an input offset voltage, which is defined as the voltage required to give a zero output voltage. Input offset voltage is usually due to imperfect matching at the input stage of a system, and it will be different from one system to the next. Offset voltages are always referenced to the input, since the output offset voltage is the input offset multiplied by the closed loop gain.

In a high precision sigma delta ADC, the offset voltage will be defined as the input voltage required to have a "digital zero" output. The source of the offset voltage may come from a combination of all the components of the ADC, including the analog input stage, the quantizer, the integrator and the digital filter

2.4.9 Voltage Offset Drift

After the offset voltage has been removed, the remaining offset voltage errors are due to offset voltage drift. Although the offset voltage can be nulled at a given temperature, the thermal coefficients of components will cause the offset voltage to drift from zero. Offset drift may also be the result of component aging. Some precision amplifier manufacturers specify drift with temperature and time. The offset voltage drift cannot be nulled, however, methods exist that will minimize it.

The digital representation of an analog signal from an ADC will be a function of the reference voltage, which may drift with time or temperature. In order for no error to occur in the output data code, the analog input must change at the same rate as the voltage reference.

Converter measurements taken relative to a drifting voltage reference will be inaccurate. A typical voltage reference will have a non-linear compensation feedback network of thermistors and resistors, Figure 2.18.

2.4.10 Removing Voltage Offset and Offset Drift

Offset voltages can be reduced to zero by applying an opposing voltage at one input terminal. A more practical method is to select devices that will provide an offset below the minimum acceptable offset voltage. Offset nulling methods will be discussed.

High precision amplifiers in the input stage of an ADC will typically have an offset voltage of 10 mV. The limitation in highly sensitive CMOS amplifiers is $1/f$ noise. The classical method of reducing $1/f$ noise is to enlarge the gate area of the input devices. This method is costly and inefficient because offset and $1/f$ noise subsists at low frequencies. Further improvements in offset require special circuit techniques such as auto-zero and chopper techniques.

Auto-zero circuits use a capacitor to store input noise during one clock phase and subtract that instantaneous noise from the subsequent input sample. Although this method will remove the $1/f$ noise, offset cancellation is limited by charge injection due to the auto-zero switch. Using fully differential circuits, this charge injection can be reduced.

If the bandwidth of interest is limited to a few tens of Hertz, CMOS chopper stabilized amplifiers can be used to achieve low offset voltages. Chopper stabilized amplifiers repeatedly null the amplifier's actual offset voltage several hundred times a second using charge storage capacitors. When external capacitors are used, the power consumption may be as high as 240 mW. Enz et al [27] used a chopper amplifier with a second order low pass selective (200 Hz) amplifier to achieve offset below 5 μV and a power consumption of only 34 μW .

Amplifiers may also be designed such that the feedback is AC coupled, which gives a DC gain of unity. This makes the input and output offset voltages the same. Time constants may be too long, leading to long turn-on delays.

Another solution is to cascade amplifiers with lower gain stages to obtain more manageable offsets, but this may add additional components and unnecessary cost and also introduce stability problems.

Offsets and drifts can be nulled using microprocessor control as shown in Figure 2.19. Here, the initial circuit offsets are calibrated out of the system by applying a zero input and storing the resultant in memory which is subtracted from subsequent readings. This real time nulling is the equivalent of the chopper stabilized opamp.

Removing voltage offset from an ADC may be done after the system is powered up and calibrated. Calibration is described below.

Figure 2.18 : Offset Nulling with a Microprocessor

Figure 2.19 : Stable Voltage Reference Using Compensation Feedback

When calibration is initiated, two data codes are stored from the ADC, a "zero input" and a "full scale" reading. The calibration microcontroller calculates a slope factor in Least Significant Bit per μV (LSB/ μV) by dividing the span between the two measurements by the resolution of the converter (i.e. for a 16 bit converter $2^{16}=65,536$ segments). This slope factor is used to calculate the offset corrected binary output code for an analog signal.

Calibration may be performed any time, but ideally it should be performed when the converter is at operating temperature. A microcontroller can select the appropriate calibration mode and initiate calibration as shown in Figure 2.20. It is possible to have the micro-controller control multiple data converters. This allows one converter to work while another is calibrating. This configuration requires that the converters be synchronized. Multiple data converter control is shown schematically in Figure 2.21.

The calibration methods described above are for "unipolar mode" (voltages are from zero to an absolute maximum). The calibration can also be performed in "bipolar mode" (voltages are from an absolute minimum to an absolute maximum), where "zero input" reading is taken as analog ground or analog input and a "full scale" reading is taken as the reference voltage or analog input. The slope factor is calculated as above, however, only half the resolution of the converter is used.

2.5 Summary

In this chapter analog to digital conversion was introduced and the problems associated with traditional techniques were discussed. Sigma delta modulation and its application to ADC were also introduced and examined. The components used in sigma delta ADC and their limitations were presented. The problems associated with ADC's were noted with some general solutions proposed.

Figure 2.20 : Offset Nulling with a Microcontroller

Figure 2.21 : Microcontroller for Multiple Data Converters

Chapter 3 Considerations in High Accuracy Systems

3.1 Introduction

For ADC's with less than 12 bits of resolution, the effects of random noise can be eliminated by careful design. For higher resolution converters where the Least Significant Bit (LSB) is below $80\mu\text{V}$, random noise becomes more difficult to eliminate.

Before discussing the circuit board layout for high accuracy ADC circuits, one must consider the noise sources involved. This chapter will discuss the problems associated with undesired noise corrupting the ADC circuits and how to avoid them. Solutions to noise problems are suggested for the circuit board designer.

3.2 Noise Sources

3.2.1 Introduction

There are many external noise sources, and the most common will be discussed in this section. Although external noise sources are important in designing high accuracy systems, designers must also examine internally generated noise. Internal noise sources are usually induced by high speed digital signals that cause crosstalk noise that can effect signals and clocks. Noise in high accuracy systems can be induced through the ground system of a circuit. Another mechanism that can effect the performance of a high accuracy system is degradation of the components with time. Some interference sources are shown in Table 3.1.

Type	Source
Ground Induced	ground loops, ground potentials, reactance coupling and ground bounce.
Internally Induced	crosstalk, leakage current, common impedance coupling and finite impedance of conductors.
Externally Induced	electric and magnetic fields, conductor motion, triboelectric effect and coupling by mutual inductance and capacitance.
Degradation	galvanic action and electrolytic action.

Table 3.1 : Noise Sources

3.2.2 Grounds

A ground is a common zero reference point to which signals in the circuit are referred. The ground pins of each separate functional element must be connected together. If separate elements have more than one path to ground, or signals are sharing a common ground, the non-zero impedance of the common path can cause an extraneous coupling of signals between the different elements. These error signals can be significant in high resolution converters. Coupling between analog and digital sections of a converter can be especially harmful.

The most undesirable situation for circuits that operate at frequencies above 1MHz is the single point common ground system. The single point common ground has all ground potentials assumed to be 0 volts. Unfortunately, because of its simplicity, this is the most common ground system in use. This system is shown in Figure 3.1 (a), which shows the change in potential for different points along the ground path.

More desirable at low frequencies is the separate ground system shown in Figure 3.1 (b). This allows minimum cross-coupling between shared ground currents in different circuits. For circuits that operate at frequencies above 10 MHz and digital circuits, separate grounds must be used.

Multiple point ground systems, shown in Figure 3.1 (c), are also a possible solution for high frequency and digital circuits. Here, all grounds are connected to a common ground plane (a ground grid increases the number of return paths for ground currents and may be as effective as a ground plane). The connections must be as short as possible to reduce common ground impedance (less than a few millimetres). For digital circuits, the ground must be multiple point, however, the supply voltage need not be multiple point since it is usually DC.

Figure 3.1 : Ground Configurations

Note the effective resistances are assumed to be equal for simplicity. The single point ground plane should be avoided since the ground potential for each component is different.

Hybrid grounds, having different characteristics at different frequencies, are also possible. The system shown in Figure 3.1 (d) is used mainly when several chassis must be grounded to a power system ground for safety reasons. The inductors provide low impedance safety at power line voltages and ground isolation at higher frequencies.

Data converters usually have a digital ground, an analog ground and an analog input signal ground. Digital ground is the point where digital currents in the circuit return to the digital power supply. Analog ground is the point where analog currents return to the analog power supply. Analog input signal ground is the zero reference for input analog signals.

3.2.3 Ground Loops

A ground loop is formed when two ground points of a circuit are separated and a potential difference exists between the two grounds (See Figure 3.2(a)). A ground loop is usually formed by a magnetic flux inducing a current to flow between two ground points. The induced current can be found by applying Lenz's law (see Appendix B)

Possible solutions to reducing the induced current are evident from Lenz's law:

1. Remove one ground creating a single point ground.
2. Reduce the area of the effected circuit.
3. Reduce the interfering source.
4. Orient the effected circuit to be normal to the magnetic flux lines.
5. Isolate the interfering source and the effected circuit.

The two circuits could be isolated using a transformer, a common mode choke, optical isolators, frequency selective grounding or balanced circuits [28, 29]. Use of a transformer or a common mode choke may add unnecessary magnetic fields and is not recommended. Optical isolators may have non-linearity problems and could consume a

large proportion of the power budget. Balanced circuits are preferred for high accuracy conversion, since they inherently reject common mode ground noise voltages. The methods of isolation are shown schematically in Figure 3.2.

3.2.4 Current Leakage

Current leakage is an important source of error in high accuracy systems, and is covered extensively in many books. Charge can leak from conductors through humidity in the air, with increased humidity causing more leakage from the conductor. Sealing circuits in containers filled with inert gasses or ions of opposite charge will help maintain a thermal equilibrium and will retard the leakage of charge.

3.2.5 Finite Impedance of Conductors

Unfortunately, any practical conductor has finite impedance. This can lead to a major problem where two voltages in a circuit are taken relative to ground at different points in the circuit. The "ground voltages" may be at different potentials if there is sufficient current flowing in the trace between them causing a potential drop.

The external inductance of a straight, round conductor of diameter d , whose centre is a distance h above a ground plane is:

$$L = (\mu/2\pi) \ln(4h/d) \quad 3.1$$

where L is the inductance per unit length (Henries per metre) and μ is the permeability of free space. Equation 3.1 shows that inductance can be reduced by either decreasing the distance between the conductor and the return path or increasing the size of the conductor. A first order approximation would suggest that to satisfy both conditions at once, a wide flat rectangular conductor (such as a printed circuit board trace) would reduce inductance.

Figure 3.2 : Ground Loops Formed by a Potential Difference Between the Grounds of Two Circuits

The voltage drop in a conductor is a function of the resistance and the maximum rate of change of current. At higher frequencies, the concentration of current near the surface is increased and the effective resistance of the conductor increases. This mechanism is known as the skin effect, and a result of a magnetic field produced by the current concentration near the surface of the conductor. The resistance of the conductor can be reduced by using a flat rectangular cross section since the surface area per cross sectional area is larger than a round cross section. Therefore, flat straps are used as ground conductors

Possible solutions to reduce the effect of finite impedance of conductors are:

1. to silver plate the surface in question,
2. to keep the lengths of the ground leads as short as possible,
3. to use a ground grid rather than a plane in multiple point systems.

When connecting different systems (analog and digital), a single point connection should exist between the two ground planes.

3.2.6 Induced Switching Noise (Ground bounce)

In analog systems, external noise sources are usually the main concern. In digital systems, the internal noise is usually a problem. When a logic gate changes state, either a current pulse is taken from the supply to charge the node stray capacitance or a current pulse is released to the ground. The result of the increased current is a voltage pulse at the ground terminals of other gates due to the inductance in the conductors. The only solution is to reduce the ground circuit impedance by at least an order of magnitude. At the VLSI chip level, Gabara [30] suggests a new method of connecting bonding pads to the silicon substrate, which reduces the resistance and improve the conduction path.

Supply voltage spikes are not much of a problem since "logic high level" noise immunity is good. Supply voltage spikes can be attenuated by proper decoupling. Disturbances on a high impedance ground line can cause spurious switching of unused and susceptible gates. An example of ground and supply voltage spikes is shown in Figure 3.3(a).

In synchronous systems this problem is magnified, since several gates will be switching simultaneously. If this is the case, a low inductance ground system is vital to the correct operation of the circuit.

Methods to reduce the effects of switching noise are discussed in the references [31, 32]. Unused pins on integrated circuits must be tied to ground or the positive supply rail as specified in Section 3.3.1

3.2.7 Crosstalk

Interference caused by unwanted electromagnetic coupling of signal energy from one circuit to another or between cables in a wire bundle is known as crosstalk. Crosstalk is well known in audio where separate speech channels are transmitted together and one breaks through onto the other. It should be possible to design the system to make the level of interference as low as required by the application.

The coupling can be capacitive, inductive, or due to transmission line phenomena (Appendix B and C). Crosstalk can be harmful in digital circuits where mis-clocking may occur. Figure 3.3 (b) shows the effect of crosstalk on digital clocks.

Crosstalk is also a problem with printed circuit board signal traces that can couple by the transmission line phenomena. The coupling can be reduced by routing ground conductors between pairs of signal lines that may be susceptible. (See also Guard Voltages Section 3.3.3)

(a) Voltage Spikes on the Supply and Ground Rail Induced by Switching

(b) Effect of Crosstalk Coupling on Digital Clocks

Figure 3.3: Effects of Ground Noise

Suggestions to reduce the effects of crosstalk are listed below:

1. In digital systems, the circuits chosen must have good immunity to noise.
2. The circuit source and/or load impedances should be lowered. Low impedances require more capacitance for a given amount of coupling.
3. Shorter cables or cables with lower core to core capacitance will reduce the mutual coupling capacitance (Appendix B). Ideally, each circuit should be screened by a grounded shield.
4. Reduce the circuit bandwidth to the minimum required by the specifications. Coupling depends directly on the rise times of the offending signal, a slower rise time means less crosstalk.
5. Use differential data transmission to inject the same level of crosstalk in common mode to an input buffer so that it is rejected. Notice that the crosstalk coupling capacitance is not reduced or eliminated, only rejected in common mode.
6. Clock leads should not run parallel to data buses or signal leads for long distances.

3.2.8 Other Noise Sources

Galvanic action occurs when different materials are brought in close contact and produce a noise voltage when a current is passed through them. Corrosion of the two surfaces will lead to eventual failure or intermittent operation.

Electrolytic action differs from galvanic action in that the two materials may be similar metals and an electrolyte is required.

The triboelectric effect occurs when the effective dielectric constant is changed due to a mechanical motion of a conductor inside its cable. Cables should be tied down to avoid this effect.

Every resistor is a random thermal white noise generator. Carbon resistors are much noisier than metal film and wire wound resistors. In analysis, the noise from a resistor can be represented by an equivalent series voltage source. Each noise source is

first considered separately, then combined. The total noise voltages can be found using the root mean square of the separate voltages.

Noise in transistors can be characterized by an equivalent noise voltage source and an equivalent current source referred to the input of the transistor. For different types of transistors (CMOS, Bipolar and Junction-FET), different noise sources can be distinguished, including: thermal noise, shot noise, channel noise and flicker noise.

Noise in resistors and transistors is an important topic for high accuracy systems. This topic is extensive and beyond the scope of this thesis, however, an excellent treatment of the subject is given in the references [28, 29, 33 - 35].

Exceeding device power supply and current limits may lead to excessive internal power dissipation, which can cause a thermal gradient to exist on chips and printed circuit boards. For example, a carbon film resistor can have a temperature coefficient between -150 and -1000 ppm/°C, and a metal film resistor between +50 and +200 ppm/°C. The main source of thermal drift in circuits is from amplifiers.

Connectors in electro-mechanical systems are also susceptible to thermal effects. Temperature variations will induce noise and unexpected voltages. Other effects of temperature variations in an electro-mechanical interface are dimensional and resistive changes, changing current flows and hence calibration.

3.3 Printed Circuit Board Design

The main problem of interfacing analog and digital signals is the prevention of digital switching noise from interfering with the analog signal. Another problem is to accommodate large analog inputs to the digital circuit. Many problems discussed in the previous section must also be addressed [36].

Digital control signals typically pass between boards that interact with each other. Processed analog signals may also pass between boards that may not be susceptible to ground noise. Often the easiest solution is to allow the ground return current to flow, and allow ground injected noise. However, if,

- 1) the ground return path has a high inductance,
- 2) the ground return path has a long distance,
- 3) the signals are high speed digital or
- 4) the signals are high precision analog signals,

then alternate solutions must be used.

If each interfacing signal is given its own return path, the problem of multiple power supply return currents may occur and more noise may be injected than if nothing at all were done. Careful design will allow the use of separate ground returns for the input stage separate from the rest of the printed circuit board. A high value resistor is then used to separate the input stage ground and the printed circuit board ground.

Another solution is to use differential connections at the interface, so that no ground returns are needed and any ground noise is cancelled by the input buffer. This solution may be more expensive than single ended solutions, since dedicated buffers and interfaces are required.

3.3.1 Grounding Techniques

Ground Planes

A good design of the grounding system in a high accuracy ADC application is vital to the proper operation of the system. A ground plane is often used in circuit boards, but these are not created by simply filling unused sections of a printed circuit board with copper and connecting them to ground. There should be as few interruptions as possible

in a ground plane. Holes generally do not pose a problem, however, long traces that interrupt the ground plane cause current to flow around them and increase the inductance. Multiple layer boards are preferred so an entire layer can be devoted to a ground plane.

Ground planes are useful in high accuracy applications since they have a low impedance for surface currents and result in lower potential drops, hence, a lower induced electrical (E) field. Ground planes approximate an equipotential plane, hence, there is no tangential E field along this surface. A ground plane does not eliminate fields, it only serves to approximate an equipotential plane that limits cross coupling. (Appendix B)

Ground planes are used in printed circuit board applications to provide a signal return path and a power return path. Note that a ground plane and a signal trace form a transmission line, with the field for each signal confined to a small region close to the trace (see Appendix C). Using ground planes in printed circuit boards allows higher clock rates in digital circuits and reduces crosstalk, radiation and coupling to other parts of the circuit.

A power plane is similar to a ground plane except it supplies a power connection. When a power plane is parallel to a ground plane, they act as a low impedance transmission line and can supply immediate energy for logic transmission. This low impedance source is limited and decoupling capacitors are still needed. The signal traces should be as short as possible.

For unused terminations, mounting holes and tooling holes, a minimum of one hole diameter should be left clear around the hole as shown in Figure 3.4 (a) and (b). Two to six connections should be used for terminals connected to the ground plane as shown in Figure 3.4 (c) and (d). This prevents "heat sinking", which may cause inferior solder joints. The ground plane will usually be on the component side to reduce warpage and blistering during flow soldering.

a) Nonfunctional Terminal Mounting Hole (with mounting pad)

b) Nonfunctional terminal Tooling hole (no mounting pad)

c) Two Point Connection Between Ground Plane and Terminal

d) Four Point Connection Between Ground Plane and Terminal

Figure 3.4 : Printed Circuit Board Terminal Connections

Experiments were done by the Crystal Semiconductor Corporation to measure the impact of ground planes on coupling between digital sections and analog sections of a printed circuit board. The experiment set-up is shown in Figure 3.5. The reduction in pick-up by using a ground plane was 15 dB. An additional 21 dB attenuation was achieved by using a trace fill. Using two ground plane layers attenuated noise pick-up by an additional 3 dB.

Guard Voltages

Guard traces are used on printed circuit boards to minimize leakage current flow to a high impedance node through surface resistance. The high impedance node is surrounded with a conductive trace connected to a low impedance point at the same potential. The guard effectively absorbs the leakage currents from other tracks. The guard voltage can also be driven at a fixed potential, such as ground, when the interfering sources are fixed in potential. Figure 3.6 shows a simple example of guarding the inputs of an operational amplifier. Ground fill traces can be used to guard the sensitive analog inputs

There should be a guard trace on both sides of a double sided board, however, the guard traces do not effectively attenuate leakage through the board. Guard width is unimportant, but larger traces do increase the surface resistance.

One can also have guard voltages on the shields of connectors. Double shielded cables are available, so that the outer shield is grounded to protect against electrostatic interference and the inner shield is driven at the voltage of the signal inside the cable.

Reduction
in coupling
at 9MHz

Figure 3.5 : Experimental Results for Ground Planes

Figure 3.6 : An Example of Guarding

Grounding in ADC Printed Circuit Boards

The analog and digital ground planes of a converter must be separate and connected at only one point in the circuit. If more than one ground connection is made, there is a possibility for an analog and digital ground to share the same path and induce coupling errors. The single common tie point should be made as close to the converter as possible, preferably to a large ground plane under the unit.

If a converter is made up of discrete components, under no circumstances should the currents returning to a digital ground share a common return line with analog signal return or an analog power supply return.

Floating inputs are susceptible to noise and should be driven high or low using the supply voltage, the ground rail or through the output of another unused gate held at logic high. Unused Transistor-Transistor Logic (TTL) inputs must be tied to the supply (through a 1 k Ω resistor) or ground rail (which will draw extra DC drain current). Unused CMOS pins must be connected to the supply voltage (protection resistors are unnecessary) or ground. An output driven high due to floating inputs will result in an output drain current that will be excessive. The high gain of the gates may even cause the gates to oscillate.

3.3.2 Cable and Connector Configurations

Groups of cards are often connected to one common mother board or backplane. The backplane serves to provide power and I/O connections. The backplane is often built without a ground plane since there are no logic elements on its surface, so the tight field control gained on the cards is lost on the backplane.

If the backplane has a ground plane, it must provide a connection from the ground plane to each card. The backplane principle is the same as the ground plane principle,

higher currents forced into smaller connections create increased fields. These areas may radiate or be susceptible to radiation or crosstalk. As with ground planes, a backplane can be formed by a grid, or even distributed multiple ground return paths. The grounding principle must be carried onto the conductors that connect to it.

Open conductor pairs

If open conductor pairs are used, it is beneficial to twist them and run them over a ground plane on a circuit board. Shielding the twisted pair will also reduce induced coupling. The shield must be grounded only once where the signal grounds, otherwise a ground loop will be created. For higher frequency interference, multiple grounds may be necessary for the twisted pair. Increased capacitance at higher frequencies limits the applicability of twisted pairs to moderate frequency range circuits.

Coaxial Cabling

The shield of a coaxial cable is used to confine the electric field of the signal within the cable and provide a sink for external disturbing fields. Terminating a coaxial cable with a pigtail will be insufficient, as interference may enter the cable at this point. Some basic rules for terminating coaxial cables are:

1. Shield terminations should not enter the equipment through a connector. Noise current on the shield can radiate into the hardware.
2. The shield connection should be outside a bulkhead and should not be formed into a half turn.
3. The shield should be bonded to the connector at more than one point and cannot be painted, anodized or subject to corrosion.
4. In critical applications the shield should be terminated in a back shell connector. This connector must be properly bonded to the bulkhead on a prepared surface.

Coaxial cables with foil shields are fragile and difficult to terminate. Foil shielded cables often have a drain wire in contact with the inside the shield, which can be easily broken by mechanical motion of the cable. A drain wire on the foil exterior is preferred to an inside drain.

Braided sheathing may be preferred to solid foil shielding because of its flexibility, durability and strength, though its efficiency is between 60% and 98%. Braided sheathing may allow interference at frequencies above 100 kHz, where currents outside the sheath follow the weave and enter the inside surface of the sheath and couple with the field inside the cable. At even higher frequencies, the braided shield becomes even less effective, since the braid holes become larger compared to the wavelength of the signal. This mechanism may be eliminated by using finer braids or double shielding

Guard voltages may also be used in double shielded coaxial cables. The outer shield is grounded to allow a termination for electric field lines. The inner shield is driven at the same potential as the signal carried by the cable to reduce the effect of induced electric fields.

Shields are used to reduce the effect of external interference on the cable. The effectiveness of the shield near the ends of the cable depends on the way the shield is terminated. The worst case is the situation shown in Figure 3.7 (a), where there is no connection at all between the shield and ground. An improvement is to use a pig-tail connection, however, current is concentrated into one side of the shield. Resonance caused by pig-tail inductance can limit noise protection at high frequencies. A pig-tail connection is shown in Figure 3.7 (b).

Maximum protection can be achieved by a connector that has 360° connection with the back plane. Examples of such connectors are BNC, UHF and Type N connectors,

which are illustrated in Figure 3.7 (c). Note that grounding a coaxial line at one end offers no magnetic protection.

Ribbon Cabling

A return path should be provided for each signal path in a ribbon cable. For low speed and low accuracy applications, one return path may be sufficient, Figure 3.8 (a). For high accuracy applications, it is necessary to provide a signal return path adjacent to each signal in the cable, Figure 3.8 (b). These additional grounds prohibit coupling between signals through common grounds and also provide an "extended" ground plane that minimizes electrostatic interference from adjacent signals and external sources. Clock leads should always be adjacent to a ground return conductor.

Cables bonded to a ground plane are available, however, the entire length of the ground plane must be terminated or the benefits of the ground plane will not be realized, Figure 3.8 (c).

Like coaxial cables, ribbon cables must be properly terminated. Although a pig-tail connection is a possible solution, a screened back shell is the ideal method of terminating ribbon cables, Figure 3.7 (d). A screened back shell is in direct contact with the connector shell and is bolted firmly and conductively to the equipment case,

3.3.3 Shielding

Electrostatic Shielding

As discussed in Appendix B, electrostatic flux lines originate at positive charges and terminate at negative charges. So, shielding cables against electrostatic fields is as simple as providing a grounded sheath to protect the enclosed cable.

a) Ungrounded Coaxial Cable

b) Pig-tail termination for Coaxial Cable

c) BNC termination with 360 degree contact

d) Screened Ribbon Cable "D" shield.

Figure 3 7 : Methods of Terminating Cables

a) Single Ground

b) Alternate ground

c) Signal over ground plane

Figure 3.8 . Ground Connections in Ribbon Cables

Most sensitive components are shielded by a metal enclosure. This enclosure provides a terminal for electric field lines and has a mutual capacitance (Appendix B) with all other electric field sources in the circuit. The shield must be grounded to avoid the possibility of coupling of input to output.

Some basic rules for low frequency shielding:

1. A circuit can be guarded from external electric fields by placing it in a metal enclosure.
2. The enclosure should be connected to the circuit reference conductor to avoid feedback paths.
3. If the circuit reference conductor exits the enclosure, the enclosure must include this conductor.
4. The enclosure can only be connected to the reference conductor once at the point where the reference conductor connects to an external circuit or ground.
5. Minimize the length the centre conductor extends beyond the shield.

The effectiveness of a shield is a function of the reflection, absorption and re-reflection of the incident wave. Reflection losses decrease with increasing frequency for E fields and increase for the magnetic (H) fields. Absorption loss is the dominant source for fields at high frequencies. Re-reflection loss is insignificant if the absorption loss is greater than 10 dB. A good treatment of electromagnetic and electrostatic shields is given in Ott [28] and Williams [32].

Electromagnetic Shielding

Shielding against magnetic flux lines is not as straightforward as shielding against electric flux lines. The simplest remedy is to avoid potential sources of magnetic interference such as motors and transformers. Another remedy is to reduce the coupling of magnetic fields to the circuit.

Reducing magnetic fields in areas is possible by redirecting the energy stored in a magnetic field using a magnetic material. For example, a steel plate near a connector can be used to carry the flux away from a connector so that it does not couple to the pin connection area inside the connector.

Conductive surfaces can be used for electromagnetic shielding, and reflection is the primary mechanism for shielding. The shielding can be conductive paint, plating on plastic surfaces or using a conductive filler moulded into the plastic [28]. Shielding can also be through screens, meshes or conductive glass.

Magnetic materials can be used as a shield. Using a magnetic material at low frequencies causes an increase in absorption loss and decreases the reflection loss. One property of magnetic materials is that their shielding effectiveness is frequency dependent. One magnetic material may be superior at one frequency while unacceptable at another frequency. Another magnetic material may be sufficient at all frequencies. A common magnetic metal for shielding is mu-metal, which has a high permeability, even at low flux densities. It is most often used as a shroud for cathode ray tubes to prohibit modulation of the electron beam by external interfering sources.

In general, magnetic materials such as steel or mu-metal are better for low frequency magnetic shielding and conductive materials are more effective at high frequencies. Losses due to holes and apertures must also be considered when analyzing a system with magnetic shielding. Ott [28] provides an excellent analysis of the effectiveness of conductive and magnetic material shields, and experimental results for materials at different thicknesses and frequencies.

Shielding a coaxial cable against magnetic fields requires more than one ground. Consider Figure 3.9 (a), where no shielding is provided. The large loop area shown allows magnetic interference to couple into the loop. If a shield were added and grounded

at one end of the circuit, in Figure 3.9 (b), the loop area remains unchanged since the signal current has no path through the shield. Grounding the shield at both ends as shown in Figure 3.9 (c) reduces the loop area if the current will flow through the shield. This protection may be non-existent at low frequencies. To maintain magnetic protection at all frequencies, the connections shown in Figure 3.9 (d) must be used.

Grounding the shield at both ends has a complication since the shield provides a path for the current produced by the difference in ground potentials between the two circuits (see Figure 3.1). The mutual inductance between the shield and the signal lead now produces a noise voltage in the signal lead. The ideal solution here is to use a shielded twisted pair to cancel the effect of the magnetic field.

Modelling even a simple magnetic field is not easy. However, some research has been done into the modelling and prediction of magnetic fields in certain very simple circuits [37].

3.4 Summary

This chapter introduced some important fundamentals to the design of PCB's for high accuracy ADC's. The recommendations made in this chapter should be followed to reduce the effects of not only external, but also internal noise.

a) Unshielded Cable

b) Coaxial cable shielded on one end

c) Coaxial Cable grounded at both ends

d) Coaxial cable grounded at both ends

Figure 3.9 : Magnetic Shielding

Chapter 4 The Ultra-Precision Digitizer

4.1 Introduction

This chapter describes the design and implementation of a new Analog to Digital Conversion (ADC) system that will yield improved offset drift and latency characteristics over existing technologies. The design of the system and the software implementation is given. The software language used was Borland Turbo C++. The setup of the experimental data acquisition system is also discussed.

4.2 Subsystem Design

A block diagram of the new system is shown in Figure 4.1. The principle of the system is to operate two converters simultaneously on one analog input, where one is periodically calibrated and the other calibrated only at start-up.

Figure 4.1 : The New Analog to Digital Conversion Subsystem Design with Lowered Offset Drift.

Note that the two converters are Crystal Semiconductor 20-bit Analog to Digital Converters. The components of the new system are described in the text.

The components enclosed in the box are implemented in software. The output is an offset drift corrected digital signal.

Converter 2 is operated continuously and allowed to drift. The converter may drift outside the specified range given by the manufacturer. Converter 1 operates on the identical analog input signal, however, it is periodically calibrated using software.

The long term drift of Converter 2 is sensed by the low pass filters (LPF). These filters have cutoff frequencies set at 1 Hz. The drift term is calculated by finding the error signal between Converter 1 and Converter 2.

An all pass filter (APF) may be added to the forward path to equalize the group delay error induced by the on-chip Gaussian filter and the LPF. Recall the group delay is defined as the negative rate of change of phase with respect to frequency, indicating the degree of non-linearity in the phase. This signal is combined with drift correction signal. In this way, the resulting output is corrected for the latency of the entire system.

4.2.1 Hardware Components (Analog to Digital Converters)

The wide availability of low cost, high accuracy converters allowed this thesis to extend from a theoretical discussion to a practical implementation. Although many ADC's are available from many manufacturers, the CS5503 20-bit oversampled sigma delta converter family of chips were chosen from Crystal Semiconductor Corporation [38].

Crystal offered evaluation boards that allowed the printed circuit board (PCB) design and manufacture to be bypassed for this proof of concept model. These evaluation boards do however contain extraneous circuitry that may add unwanted ground noise and are not optimised for any particular task. These issues must be addressed and are suggested as further research and development for implementation into the final inertial platform. The direct software implementation allowed the proof of concept to be made at a minimal cost.

The CDB5503 evaluation board illustrates the implementation of many recommendations for noise reduction outlined in Chapter 3 of this thesis. The analog and digital grounds are isolated and connected only at one point. The ground plane is double layered on the sensitive analog side. Shielded coaxial cables are used to connect the analog signal to the circuit board.

Detailed operation of the boards can be found in the data book that is readily available from Crystal Semiconductor [38]. Below is a brief discussion of the design and layout of the CDB5503 evaluation board. Suggestions for the implementation in an inertial system are given in the Chapter 6.

The evaluation board can be broken into 12 sections as seen in Figure 4.2.

1. Power supply:

Power supplies to the board consist of ± 5 volts and a digital ground. These supplies are located on the digital ground plane.

2 Converter:

The CS5503 chip bridges the analog and digital ground planes. The analog input and voltage reference are located on the analog ground plane.

3. Clock:

The input clock can come from either an on-board crystal oscillator to provide jumper scalable input clock frequencies, or an external input clock. This circuitry is on the digital ground plane far from the analog ground plane.

4. Master Clock Generator:

The clock can be scaled to one of seven different values using jumpers. The counter is used to divide the input clock by 2^n where $n = 0, 1, 2, \dots, 7$.

5. Voltage Reference:

A 2.5 volt precision voltage reference is provided to the converter

6. Analog input:

The analog input is located on the analog ground plane. A low valued resistor is placed in series with the input to provide some protection to the converter from excessive input overrange current. The input of the converter is diode clamped to both supplies, however, excess current may damage the device.

7. MicroPort Interface:

The microport interface is provided to allow access to the output data from the converter. A detailed discussion of the operation of this port is included later in this chapter.

8. Header Control:

Several control pins can be activated using switches or a microcontroller, including the calibration pin, sleep pin and the calibration options pins.

9. Serial Interface:

Not used, provided for lower accuracy converters.

10. Baud Rate Generator:

Not used, provides a baud rate clock for the serial interface.

11. Parallel Interface:

Not used, provided for lower accuracy converters.

12. Decimation Counter:

Not used, provided to allow reduced output word rates. The decimation counter also uses a flip-flop to provide a signal to the remote reading device whenever the data registers are updated. This decimation counter is used directly with the serial interface, and cannot be used to reduce the output rate from the converter when using the microport interface.

Clearly, more than 50 percent of the board is not used in this application and could be removed. Recommendations for the final implementation are presented in Chapter 6.

Figure 4.2 : Crystal Semiconductor Evaluation: Circuit Board Layout

The input stage of the CS5503 uses chopper stabilized techniques to achieve low input drift. Chopper stabilized amplifiers are introduced in Section 2.4.8 and covered extensively by Enz et al [27].

The analog input of the CS5503 can be modeled as shown in Figure 4.3. A 20 pF capacitor is used to dynamically sample the input signal. Every 64 clock cycles, the switch alternates between the output of the buffer and the analog input. When the capacitor is switched from the buffer output to the analog input, a small packet of charge will be required from the input source to settle the voltage on the sample capacitor to its final value. The offset voltage on the buffer may cause a voltage difference of up to 100 mV between the output of the buffer and the analog input. The settling time is defined as:

$$V_{out} = V_{in} (1 - e^{-t/RC}) \quad 4.1$$

where V_{in} is the input voltage, V_{out} is the final settled voltage R is the input source resistance, C is the 20 pF sampling capacitor and t is $64/CLKIN$ ($CLKIN$ is the input clock frequency). Rearranging Equation 4.1 it can be found that for the CS5503 with a 100 mV offset voltage in the buffer and an error voltage of 600 nV (1/4 LSB), the maximum source resistance is 60 k Ω .

Figure 4.3 : Analog Input Model for the CS5503 Analog to Digital Converter

2 of/de 2

PM-1 3½"x4" PHOTOGRAPHIC MICROCOPY TARGET
NBS 1010a ANSI/ISO #2 EQUIVALENT

PRECISIONSM RESOLUTION TARGETS

Calibration

When the power is applied to the converter, operation cannot commence until the device is calibrated. The converter is calibrated so that the output state can be precisely known. Calibration of the ADC can be performed in one of three ways, self-calibration system offset/gain and system calibration [38].

The offset voltages specified by the manufacturer are valid only after calibration, and should be performed at the operating temperature. The dependence on the offset voltage drift with temperature is shown in Figure 4.4. This figure illustrates the good offset stability for temperatures between -40°C to 70°C . Above 75°C , leakage current becomes the main source of offset drift. The solution to this problem is to maintain a constant temperature around the converter or introduce a temperature compensation algorithm to compensate for the offsets.

For calibration, the converter measures the 1's density for a "full scale" input and a "zero scale" input. When calibrating, the microcontroller stores the 1's density from the modulator for each state and calculates a slope factor that represents the gain slope for the input to output transfer function of the converter. This slope factor is used in later calculations of the binary output code for any input analog signal. The full scale and zero scale reference sources are shown in Table 4.1 for the three different modes of calibration.

Table 4.1 also shows the different calibration times for each mode. Note the dependency of the calibration time on the input clock frequency.

For this application, the self-calibration was chosen, since a full scale output from the gyro is difficult to achieve without a precision rotation table. Some gyros do provide a start-up function that will provide a zero scale and a full scale output. The bipolar mode was chosen for the converter since gyro rotations are bi-directional.

Figure 4.4 : Typical Self Calibration Bipolar offset versus temperature after calibration at 25°C

Calibration Type	"Zero Scale"	"Full Scale"	Calibration Time*
Self-Calibration	Analog Ground	Voltage Reference	3,145,655/CLKIN
System Offset & System Gain	Analog Input		1,052,599/CLKIN
		Analog Input	1,068,813/CLKIN
System Offset	Analog Input	Voltage Reference	2,117,389/CLKIN

Table 4.1 : Calibration Modes for the CS5503 Analog to Digital Converter

*Note : The clock frequency (CLKIN) used on the evaluation board is 4.096 MHz.

Converter 2 is calibrated only at start-up using a 5 volt pulse to the calibration pin of the converter. Converter 1 is calibrated at a fixed rate of once per second to up to once per minute. During calibration of ADC1, the outputs of the filters is locked to their previous outputs to stabilize the offset correction during calibration.

4.2.2 Filter Design

The CS5503 uses an on-chip digital filter to reject the high frequency quantization noise. The digital filter implemented on the CS5503 is a 6-pole Gaussian filter. The design of the Gaussian filter is presented in Appendix A. The delay characteristic of this filter is important since it will be compensated for in the latency correction stage.

4.2.3 Low Pass Filter Design

The flexibility of the system allows the constraints on the low pass filter (LPF) to be very relaxed, allowing a low order filter to be generated. The lower order allows the delay due to the LPF to be minimised.

An important specification for this filter is the maximally flat passband response. With this requirement, the filter designs could be either a Butterworth or a Chebyshev Type II filter. Both these filters were designed using MATLAB software.

It was found that for both filters of comparable order, the Chebyshev filter gave much better stop band attenuation and a more rapid roll off. The Chebyshev group delay was higher than the Butterworth group delay, and equalization was not sufficient to remove the delay. Both filter responses are shown in Figure 4.5.

Figure 4.5 (a) shows the specified requirements. The sampling frequency in Figure 4.5 is 250 Hz, and responses up to half the sampling frequency are shown. The passband is up to 1 Hz and the stopband is set at 50 Hz, with an attenuation of 30 dB.

Figure 4.5 (b) shows the Chebyshev Type II implementation of this requirement. The passband is flat with a zero at the cutoff frequency to achieve the required attenuation. Figure 4.5 (c) illustrates the delay characteristic of this filter. Figure 4.5 (d) shows the Butterworth filter response to the desired response. The delay characteristic of the Butterworth, shown in Figure 4.5 (e) illustrates its preferred delay characteristic to the Chebyshev filter. The delay of the Butterworth is approximately half that of the Chebyshev.

The filters were implemented using the algorithms given in Stearns and Hush [39]. The algorithm used was:

$$H(z) = \frac{b_0 + b_1 z^{-1} + \dots + b_{N-1} z^{-(N-1)} + b_N z^{-N}}{1 + a_1 z^{-1} + \dots + a_{N-1} z^{-(N-1)} + a_N z^{-N}} \quad 4.2$$

where b_i are the numerator coefficients and a_i are the denominator coefficients associated with the specific filter. The z^{-n} terms indicate that n 'th delayed sample is used, and N is the filter length.

(a) Magnitude Filter Requirements

(b) Magnitude Response of the Chebyshev Type II implementation of the Specification

(c) Delay Response of the Chebyshev Type II implementation of the Specification

(d) Magnitude Response of the Butterworth implementation of the Specification

(e) Delay Response of the Butterworth implementation of the Specification

Figure 4.5 : Low Pass Filter Design

4.2.4 All Pass Group Delay Equalisation Filter Design

Although a flat passband magnitude response is desirable, a constant group delay in the passband is also required for this system. The delay correction algorithm introduced in the following section assumes that the delays are independent of frequency. As shown in previous sections, the group delays of the Gaussian Filters and the subsystem LPF's are frequency dependant.

Figure 4.6 illustrates an example of delay equalization. In this example, the delay characteristic of a low pass filter will be modified to be approximately constant in the passband. The original un-equalized filter is shown as a solid line in Figure 4.6. The magnitude response shown in Figure 4.6 (a) is a low pass continuous time filter with a cutoff frequency at 1Hz. The non-linearity in phase response near the passband edge can be seen in Figure 4.6 (b). Figure 4.6 (c) illustrates the increased group delay near the passband edge.

The response of the equalization filter is shown as a dotted line in Figure 4.6. The equalization filter does not modify the magnitude response, but the group delay can be designed to any specification. The equalization filter has been designed so that the effect of the peak group delay near the passband edge is reduced.

The combined response of the equalization filter and the original filter is shown as a dashed line in Figure 4.6. The magnitude response has remained unchanged as shown in Figure 4.6 (a). The phase is more linear than the original filter, but the combined group delay is increased. The group delay has been modified to remain within a fixed range of delays.

Delay equalization is achieved using an all-pass filter. Methods have been designed to optimally place the all-pass poles and zeros to equalize with a minimum increase the group delay or maximize the linearity of the phase response [3, 4, 40]. The

"filterX" software package developed by Chris Ouslis at the University of Toronto was used to help design the all-pass equalization filters used in this system. The drawback to the filterX program was its drastic increase in the group delays. Lower group delays and a reasonable tolerance were achieved by placing the pole-zero pairs by trial and error.

Note that if it is assumed that :

- 1) the delay in the two filters and the adders is negligible and
- 2) the offset drift is varying very slowly

the APF may be removed. The effect of removing the APF will be to improve the delay characteristics and decrease the workload for the latency correction algorithm. This option is available only when the purpose of the APF is to delay the signal to coincide with the corrected signal. If the delay is not uniform over the passband, the latency correction algorithm will not work.

(a) Magnitude Response for a Low Pass Filter, an All Pass Filter and the combined response of the two filters.

(b) Phase Response for a Low Pass Filter, an All Pass Filter and the combined response of the two filters. Note the increased linearity in the combined response.

(c) Delay Response for a Low Pass Filter, an All Pass Filter and the combined response of the two filters. Note the overall increase in the delay curve

——— Original Low Pass Filter
 All Pass Filter
 - - - - - Combined Response

Figure 4.6 : Group Delay Equalization Using an All Pass Filter Compensation.

4.2.5 Latency Correction

Delays introduced by the sampling process and the frequency independent calculations in the system can be removed by latency correction algorithms. The latency correction algorithm developed by Staley [41] will be described here. Group delay equalization, described in the previous section, is used to modify the frequency dependant group delay of the frequency to be more constant in the frequency band of interest.

If the frequency independent delay of a system is expressed as L , then the transfer function would be expressed as:

$$G(s) = e^{-sL} \quad 4.3$$

where $s = j2\pi f$ and $G(s)$ is the transfer function of the delayed signal.

If we express the problem more generally in the discrete-time domain, then:

$$G(z) = z^{-L} \quad 4.4$$

where $G(z)$ is the transfer function of the delayed signal and $z = re^{j2\pi fT}$. Note that when $r = 1$, the z -Transform corresponds to the Fourier Transform [3].

The first order algorithm for latency correction can be expressed as:

$$y_n = x_n + (x_n - x_{n-1}) (L/T) \quad 4.5 (a)$$

where x_n is the current input sample, x_{n-1} is the previous input sample, y_n is the output sample, L is the latency to be corrected and T is the sampling period. Here, the approximation to the first derivative is used to predict the expected sample which was delayed by L samples. The prediction decreases in accuracy with increased input frequency.

Applying the z -Transform to Equation 4.5 (a):

$$Y(z) = X(z) + (X(z) - z^{-1} X(z)) (L/T) \quad 4.5 (b)$$

where $X(z)$ and $Y(z)$ are the z -Transforms of the input and output sequences respectively, L is the latency and T is the sampling period.

Equation 4.5 can be expressed as:

$$Y(z) = X(z)(1 + L/T) - z^{-1} X(z) (L/T) \quad 4.6$$

or simplified as:

$$Y(z) = X(z) (a + b z^{-1}) \quad 4.7$$

where $a = (1 + L/T)$, and

$$b = -L/T.$$

The overall transfer function, $H(z)$, represented by Equation 4.6 can be expressed as:

$$H(z) = (a + b z^{-1}) \quad 4.8$$

If the desired overall response is a latency corrected output, then the product of $G(z)$, the transfer function of the delayed system, and $H(z)$, the compensating transfer function will be unity:

$$G(z) H(z) = 1 \quad 4.9 (a)$$

Substituting for $G(z)$ and $H(z)$:

$$z^{-L} (a + b z^{-1}) = 1 \quad 4.9 (b)$$

If Equation 4.9 is expanded in the frequency domain,

$$G(e^{j2\pi fT}) H(e^{j2\pi fT}) = e^{j2\pi fL} (a + b e^{j2\pi fT}) \quad 4.10$$

where f is the input frequency. If the power series approximation is used for the exponential Equation 4.10 can be expressed as:

$$(1 - j2\pi fL + \frac{(j2\pi fL)^2}{2!} - \dots)(a + b[1 - j2\pi fT + \frac{(j2\pi fT)^2}{2!} \dots]) = 1 \quad 4.11$$

The number of terms used in Equation 4.11 can be calculated using the minimum acceptable error allowed in the output.

It is important to note that the calculation of the number of terms allowed in Equation 4.11 is dependent on three terms, the sampling period (T), the latency (L) and the input frequency (f). The sampling period of the constructed ADC system is 4 milliseconds.

The latency, L , will be dependent on the final system implementation and is difficult to predict at this point, however, the sources of latency can be identified as:

- 1) the sampling process at the input stage of the converter (Section 4.2.1),
- 2) the conversion time of the converter,
- 3) the combined delay of the Gaussian filter and the equalizing filter,
- 4) the offset correcting adder and
- 5) delays in the calculation of the latency correction itself

The main source of delay is due to the digital filter and equalization filter combination. Delay from the Gaussian filter alone is 60 milliseconds and is not acceptable. Latency correction is difficult with delays of this duration since the algorithm uses a difference equation to predict future samples. This problem will be addressed in Chapter 5. An acceptable latency expected from this system would be much less than 5 milliseconds.

At this point it is necessary to determine the expected input frequency to the gyroscope. The input frequency is necessary to determine the number of terms required to minimize the error induced by the latency correction algorithm. A larger number of terms will provide an improved prediction of the next sample at the expense of increased calculations. As specified in Chapter 1, the gyro dynamic range in an inertial navigation system, is approximately 30 Hz.

The first order error for this system could be expressed using Equation 4.11:

$$2\pi fT = 2\pi(30 \text{ Hz})(0.004 \text{ seconds}) = 0.75$$

and

$$2\pi fL = 2\pi(30 \text{ Hz})(0.005 \text{ seconds}) = 0.94$$

The third order error for this system could also be expressed using Equation 4.11:

$$(2\pi fT)^3/4! = 0.01$$

and

$$(2\pi fL)^3/4! = 0.03$$

The error terms which have been calculated using Equation 4.11 are residual errors. These errors are used to determine if more terms are required to accurately predict the latency.

4.3 Software Design

4.3.1 Introduction

The software for the data acquisition system was written using Borland Turbo C++ Version 3.0. It is beyond the scope of this thesis to provide a detailed explanation of Object Oriented Programming (OOP) and the reader is referred to Booch [42], Hu [43] or Borland [44] for familiarity on this topic. Some topics in OOP will be introduced below to provide the reader with the necessary elements to understand the software design. The initial package was written for ease of use and to simplify testing.

4.3.2 Object Oriented Programming (OOP)

OOP is a simplified method which allows computer programs to model the real world. There is little benefit achieved from OOP in small programs. The true advantage lies in larger programs, making them more modular, structured, and reduces programming time by defining reusable code.

In this section, italicized words are used to indicate terms that are used specifically by Borland, however, other OOP languages use different terms with similar meaning. Words indicated in bold italics are variable names (identifiers) that are used in the software.

A *class* can be used to describe events, things or systems. A door on a car can be described by a *class*. This *class* could be called ***Door***, for example, and it would contain the door's properties, such as colour and size, and also its actions (or *methods*), such as open or closed. This process of combining data (colour and size) with functions (*actions* or *methods*) is called *encapsulation*.

An instance of a *class* is called an *object*. In the description of a car (which could be another *class*), there would be 4 instances (*objects*) of the *class*, ***Door***. Each instance could be given a different name, for example ***DriverDoor***, ***PassengerDoor*** and so on. Note that these new *objects* do not have to be re-programmed, only declared, much like any data type, such as an integer or a floating point variable.

In defining a new *derived class* (***Door*** for example) which *inherits* previously defined *base classes* (***Hinge*** and ***Window*** for example) the programmer can create a *hierarchy* of classes. This inheritance also allows the programmer to *recycle* code. For example, when defining a ***Hood*** or a ***Trunk***, the ***Hinge*** class, which was used for the ***Door***, could be used as a *base class* without any modification.

Note that the *Door* class actually inherits from *Hinge* and *Window*. This is an example of *multiple inheritance*, where the *derived class* inherits from more than one base class.

The simple example of the *Car* data class is shown in the *inheritance diagram* of Figure 4.7. Note that the accepted practice is to have the arrows point from the *derived class* to the *base class*.

Although the hierarchy shows the car class and how it is made up of sub-components, it does not necessarily define the system that will use it. For example, the system might be a traffic model or a vehicle performance model.

4.3.3 Subsystem Software Design

Several *classes* were defined to represent each data converter accurately. Each *class* was created to describe some property of each item in the system. Similar properties were grouped into *classes* and these are inherited by subclasses. The *class inheritance hierarchy* of the new ADC subsystem is shown in Figure 4.8.

The system could have been modeled many different ways. The signal passing through the system could have been considered an *object* and *methods* operating on it as it passed through each component in the system. A more reasonable description of the system could be made by making each component in the system an *object*. The messages passed between the *objects* would be the data passing through the system.

Each component in this system has at least one input and at least one output. This similarity in the system is used to create the *base class Data*. The *Data class* has input and output data structures and *methods* to retrieve these data structures. All other *classes* inherit from the *Data class*. For classes with multiple inputs or outputs, additional inputs or outputs are generated internally, and are exclusive to that *class*.

Figure 4.7 : Example of an Inheritance diagram.

Here the derived class, **Car**, inherits from its base classes.
By convention, the arrows point from the derived class to the base class.

Figure 4.8 : Class **Data** and its Derived Classes

The system is made up of the reusable subclasses defined as Objects.

Note that the *class inheritance hierarchy* shown in Figure 4.8 does not reflect the operation of the system, only the methods to create the subsystems that operate within it. The *objects* declared using the *classes* are assembled to create the system shown in Figure 4.1.

The *Filter class* is used to create the low pass and all pass filters. When declared with an identifier, the filters are initialized with the specific number of coefficients of the filter and the calculated filter coefficients. The *Delay class* delays a signal by a fixed number of samples. The *Latent class* is the latency correction algorithm. Third order accuracy was used to achieve the required accuracy. The *Adder class* is used to combine signals. Note that the signals that enter this class should be synchronized so that the appropriate signals are added. The *Calib class* is used in conjunction with the *Converter class* as shown in Figure 4.8. This class is modified when a converter is being calibrated. If a converter is calibrating, a delay is activated until it has completed. This class also controls the filters to reduce drift errors during calibration.

The *Converter class* is used to model the ADC's used as sub-components of the system. This class serves mainly as a defining function for information about the converters used. The information stored in this class is:

- 1) the port address of the converter,
- 2) the number of bits of resolution,
- 3) the scale factor,
- 4) the offset error and the
- 5) state of the converter (active or inactive).

All the above classes inherit from the *Data class*.

As shown in the block diagram of Figure 4 1, the re-calibration of Converter 1 must be synchronized with the filter output that corrects Converter 2. During calibration, the outputs from the filters are locked to the previous filter output such that there is nominal error correction during calibration. The duration of the calibration depends on the input clock, and is 0.64 seconds for the maximum input clock on the evaluation board. The effect on the overall performance during this period must be analyzed. The outputs from the filters should be frozen, allowing some nominal error correction to take place during calibration.

Data is collected by polling the converter until it has converted data ready to transmit. When data is not ready at the pre-determined sampling interval, the output sample remains unchanged from the previous sample. This method of data collection is acceptable for the data testing phase, however, it should be replaced by an interrupt driven system. In an interrupt structure, the ADC informs the microcontroller when data is ready, and the microcontroller receives the data when it is idle.

An interrupt request line is available on the parallel port connection used, but the polling system was much simpler to implement for the proof of concept.

The IEEE-488.2 data interface standard is used for most components of the navigation system and should be adopted for this component also. The IEEE-488 is an instrumentation data bus with hardware and programming standards originally adopted in 1975 and revised in 1987.

4.3.4 The Microport Interface

Data retrieval from the Crystal Semiconductor evaluation board is performed by connecting the microport interface to the parallel port of the controlling computer. The microport signal lines are:

1. Data Ready (DRDY) - Used by the converter to indicate when the converter has sample of data ready to output.
2. Send Data (SDATA) - Data is transmitted serially (one bit at a time) through this line.
3. Send Clock (SCLK) - The computer uses this line to retrieve data.
4. Chip Select (CS) - This line is used by the computer to activate a converter.

The standard parallel interface is shown schematically in Figure 4.9, with the naming conventions of the pins illustrated in Table 4.2. Also shown is the interface connection to the Crystal Semiconductor evaluation board. The 25-pin parallel port is segregated into 4 groups. Eight lines are grounded and the remaining 17 lines are divided into data, control and status lines.

The data register has eight data lines that are used to transfer eight bits (one byte) of data at a time.

The control register is used to select and initialize the device connected in parallel. The control lines comprise the four least significant bits of the 8-bit control ports. The other bits are used for parallel port interrupt control.

The status register is used to relay information about the connected device to the computer. One line in the status register can be used for interrupt control requests (IRQ) if it is configured as such by the control register.

Figure 4.9 : Standard Parallel Port Registers.

- Notes :
- Circles indicate inverted inputs.
 - Arrows indicate the direction of data flow.
 - Data is obtained through the Bit Positions of the Port Address.
 - Grounds are not shown for clarity, but at least one connection must be made.

Name	Crystal Designation	Bit Position	Bit Position	Pin No.
Data Register				
data 0	SCI	0	0000 0001	2
data 1	CS	1	0000 0010	3
data 2	SCO	2	0000 0100	4
data 3	SelfCal1	3	0000 1000	5
data 4	SelfCal2	4	0001 0000	6
data 5	BP/UP(bar)	5	0010 0000	7
data 6	SLEEP(bar)	6	0100 0000	8
data 7	CAL	7	1000 0000	9
Status Register				
-busy	-	7	1000 0000	11
-ack (IRQ)	-	6	0100 0000	10
+PE	-	5	0010 0000	12
+SLCT	DRDY	4	0001 0000	13
-error	SDATA	3	0000 1000	15
Control Register				
-SLCT IN	-	3	0000 1000	17
-init	-	2	0000 0100	16
+auto FD XT	-	1	0000 0010	14
+Strobe	Impulse Input	0	0000 0001	1
Ground	-			18 -> 25

Table 4.2 Parallel Port Interface

The Crystal evaluation board use of the parallel ports does not conform to a true parallel connection. Data is retrieved serially (one bit at a time) from the ADC at the switching speed determined by the clock speed set by the controlling computer.

The segment of code shown in Figure 4.10 is used to illustrate the method in which the data is obtained from the ADC evaluation boards. The code in Figure 4.10 is referred to by line number.

In line 1, the variable `ppa` is the parallel port address, at which the data, status and control registers can be accessed. First, the Status Register and the Control Register are initialized for input by writing zeros into the `ppa` address.

Line 2 is the conditional statement that checks to see if data is ready to be read from the ADC. This is accomplished by reading the status register (which is an 8 bit value) and testing to see if the Data Ready Bar (DRDY) pin is active. (refer to Table 4.2 for locations of the pins in the parallel port). Lines 3 and 15 brace this conditional loop.

Line 4 resets the clock for input of data. Table 4.2 shows the locations of the clock line.

In line 5, the Chip Select Bar line is set. The variables, `clocklow` and `clockhi`, are used to temporarily store the information on the data pins. The variable, `clocklow`, is used to store the clock low condition and the other variable, `clockhi`, is used to store the clock high condition. The high condition is achieved by incrementing `clockhi` on line 6.

The loop defined on line 7 is used to read data from the Send Data line. The clock is alternated by alternating the output of variable `clocklow` and `clockhi` while the data bits are read into the contents of the address `data`.

Before the loop is completed, the Chip Select and the Send Clock are set to their idle states in line 13. Line 14 sets a status variable so that the calling program is informed of a successful data transfer.


```

1  outp(ppa+1,0x0);
2  if (!( inp(ppa+1) & 0x10 ))
3  {
4      outp(ppa,inp(ppa) & 0xfe);
5      outp(ppa,clocklow=clockhi=inp(ppa) & 0xfd);
6      clockhi++;
7      for(x=0; x<bits ; x++)
8      {
9          outp(ppa,clocklow);
10         *data= (*data<<1) + ((inp(ppa+1) & 8) ? 1 : 0);
11         outp(ppa,clockhi);
12     }
13     outp(ppa,inp(ppa) | 0x02 & 0xfe);
14     status = 1;
15 }

```

Figure 4.10 : Code Segment Illustrating the Use of the Microport for Data Retrieval from the Analog to Digital Converter

4.4 Experimental Procedure

The test program was carried out on a static free work station to prevent damage to the converters. Each converter was provided its own power supply to help reduce ground switching noise (Section 3.2.6.). The software system highlighted in Figure 4.4 was implemented and tested using an IBM PC-AT 486-33 MHz. Two parallel ports were polled to collect data from the converters. Ribbon cable adapters were constructed to interface the 25-pin parallel connector to the 10-pin header connection on the evaluation boards. Coaxial cables were used to help reduce noise corruption on the input signal.

The following sections will describe the tests used to evaluate the performance of the sub-components and the new data acquisition system.

4.4.1 "Warm-Up" Tests

The "warm-up" tests performed were used to illustrate the requirement for the present program. The two converters were powered, calibrated and operated with the input grounded.

The two types of warm-up tests used to evaluate the system performance were:

- 1) from room temperature to operating temperature
(duration = 1 hour ; sampling period = 1 second)
- 2) from sub-zero temperature to operating temperature
(duration = 1 hour ; sampling period = 1 second)

The initial sub-zero temperature was achieved by protecting the evaluation circuit boards in static resistant bags and placing them outside for one hour. The ambient temperature in the Ottawa area during these tests were regularly below -20°C. The temperature in degrees Celsius reported by the Ottawa weather office was recorded for each test. During these "warm-up" tests, only start-up calibration was performed.

4.4.2 Comparison to Existing High Resolution Converters

High precision multimeters were used to compare the accuracy of the new system with a standard reference. For these tests, the Datron and Keithley multimeters were assumed to be calibrated to an accuracy of 7.5 digits (approximately 0.05ppm, or 24 bits). The most recent calibration information for the multimeters was recorded.

An alkaline cell power supply was used as a reference DC voltage. The stability of the output voltage was not an issue and its drift helped in assessing the outputs from the converters.

4.4.3 Induced Offset Tests

The induced offset tests were performed to illustrate the performance of the system under varying reference voltage conditions. The sampling frequency was much higher than in the "warm-up". The evaluation boards provided voltage references with variable potentiometers for fine calibration.

This test was performed by initially grounding the input to both ADC's and applying an input voltage. The input voltage was induced exposing the grounded end to a magnet. Although the input voltage could not be precisely measured, the input voltage was in the microvolt range and offset characteristics were readily visible.

The format of the induced offset test was:

- 1) Ground the input,
- 2) Start the data collection routine,
- 3) Induce a high frequency (10 Hz) input to the grounded input,
- 4) Induce a low frequency offset drift voltage using the potentiometers on the voltage references.

4.5 Summary

This chapter introduced the design and implementation of a new Analog to Digital Conversion (ADC) system that will yield improved offset drift and latency characteristics over existing technologies. The setup of the experimental data acquisition system was also discussed.

Chapter 5 Results and Discussion

5.1 Introduction

This chapter will present the results from testing the individual components of the system, and demonstrate the improved performance of the overall system. The specified performance of the Crystal Semiconductor ADC sub-components that are used in the test system, and their actual tested values are presented. A description of the system modifications for use in an inertial navigation system will be presented. The results of the test program will be discussed.

5.2 Performance of Crystal Sub-Converters

Initially, the two Crystal Semiconductor CDB5503 20-bit analog to digital converter evaluation boards were tested to analyze their performance. Twenty bit resolution is difficult to measure due to noise with a standard signal generator. The noise

reduction methods described in Chapter 3 were used to achieve the most reasonable performance from the converters. Coaxial cables were terminated with a grounding connection and the performance of the system was recorded. Note that although this method provided some insight into the noise characteristics of the CS5503, this test is only a minimum. A high accuracy source would be needed to measure the dynamic range and the response of the converters.

The analog characteristics of the CS5503 are summarized in Table 5.1. The measurements were made for a grounded input, since no sources were available to offer 20-bits of accuracy. The bipolar offset was observed using a graphical interface designed for a computer as part of the present project.

The offset values are valid only after calibration at the temperature of interest. The effect of temperature variations were discussed in Chapter 4.

Offset drifts were easily simulated using the variable voltage reference. The voltage references of both converters were varied and the results are shown in Figure 5.1. The output of ADC 1 was calibrated each second to maintain the offset voltage within the specification published by the manufacturer. ADC 2 was calibrated only at start-up and allowed to drift. Also shown in Figure 5.1 is the output from the system. The output clearly shows reduced effect from the offset voltages.

5.3 Results from Design

5.3.1 Initial Testing Results

Initial results from the system described in Chapter 4 provided output data much noisier than was expected. The magnitude of the error was approximately 100 LSB's. Offsets were corrected as expected and latencies were removed, however, the output had a high frequency noise component, especially for high frequency signals.

Parameter	Typical Specified by Crystal	Measured
Bipolar Offset	4 LSB* to 16 LSB	5 LSB (see text)
Bipolar Offset Drift	34 LSB	12 LSB (see text)
Resolution	20 bits	20 bits
Noise referred to output	1.6 LSB	2 LSB (approx.)

Table 5.1 : Analog Characteristics of the CS5503

Note the measured characteristics of the Crystal Semiconductor CS5503 are within the specifications of the manufacturer. The measured results were found using a terminated coaxial cable and should be considered as a minimum test of the parameters. A high precision source should be used to determine the operating range of the converter.

*Least Significant Bit.

Figure 5.1 Induced Offsets using variable Voltage References

The source of the noise was found to be in the latency correction algorithm. Latency correction algorithms shown in Chapter 4 were initially designed for a continuous-time systems and application to discrete systems was assumed. When the input is a sampled continuous signal as shown in Figure 5.2 (a), predictions using the derivative are accurate and the overshoot error is the primary source of error.

When continuous-time sampled signals are digitized, they are approximated by fixed binary signals. These finite approximations are good estimates for the slowly varying component of an input signal. The latency correction algorithm, which uses an approximation to the derivative to predict signals, amplifies the changes in the discrete quantities which appears as high frequency noise. This can be seen in Figure 5.2 (b).

The amount of overshoot in the first order latency correction algorithm was calculated for various frequencies and latencies. For an input sampling frequency of 250 Hz the overshoot for various input frequencies is shown in Figure 5.3 (a). The error in the algorithm increases for increasing frequency and is no longer valid near one half of the sampling frequency. Figure 5.3 (b) shows the overshoot for increasing latencies with a similar increase in error for increased latency.

Figure 5.3 illustrates the validity requirement for the equations developed in Section 4.2.5. The input signal must be low frequency and the latencies should be as low as possible. For input signals which are expected to deviate from the low frequency-low latency model, a filter could be designed to compensate the magnitude distortion based on predicted models of the input signal.

5.3.2 Warm-Up Test Results

Initially, the characteristics of the Crystal Semiconductor CDB5503 ADC evaluation boards were assessed. The previous chapter described the warm-up tests.

Figure 5.2 (a) : Correction Overshoot for a Sampled Continuous Signal

Note : The input signal is 1Hz and the latency is 100ms

Figure 5.2 (b) : Correction Overshoot for a Discrete Sampled Signal

Note : The input signal is 1Hz and the latency is 100ms

Figure 5.3 (a) : Correction Overshoot for different Frequencies

Figure 5.3 (b) : Correction Overshoot for different Latencies

The need for the offset correction system is demonstrated by the results shown in Figure 5.4 (a). Both boards were cooled to -21°C , powered, calibrated and allowed to operate for one hour. The initial offsets after calibration were -15 LSB for ADC 1 and -9 LSB for ADC 2. These offsets were removed from the outputs using software. Although the offsets drifts were similar, the magnitude of the offset is unpredictable. Temperature control of the converters to some extent in the HRU may reduce the effect of this error.

The offset voltage drift was measured after the system was powered up and calibrated at room temperature. Each converter was allowed to operate for one hour until it reached operating temperature. Here, the offset voltage drift is not as extreme as in the previous case, however, a high precision navigation system usually does not operate under stable temperature conditions. The initial offsets after calibration were 10 LSB for ADC 1 and -4 LSB for ADC 2.

A demonstration of the stability of the calibrated ADC is shown in Figure 5.4 (c). The evaluation boards were both cooled to -30°C , powered, calibrated and allowed to operate for one hour. The initial offsets after calibration were 18 LSB's in ADC 1 and -25 LSB's in ADC 2. ADC 1 was calibrated once every 2 seconds and ADC 2 was allowed to drift freely. The jump in the output has not been explained and should be studied further to determine if this is a characteristic of the converter or an anomaly.

5.3.3 Induced Offset Test Results

The induced offset drift tests were performed as described in Chapter 4. Normally, offset drift must be measured in a temperature controlled lab to accurately predict drifts. These tests, although demonstrating the effects of temperature on the offset drift, are a better demonstration of the offset drift with time.

Figure 5.4 (a) : Warm-Up test from -21C to Operating Temperature
Note the different offset drift rates for the different converters

Figure 5.4 (b) : Warm-Up test from Room Temperature
Note the different offset drift rates for the different converters.

Figure 5.4 (c) : Warm-Up test from -30C
Note ADC 1 was calibrated every 2 seconds and ADC 2 was allowed to operate continuously.

Figure 5.5 illustrates the offset drift correcting properties of the new converter. The converter input was grounded using a coiled wire. An input voltage was induced manually by moving a magnet near the coil. The result for no input offset voltage is shown in Figure 5.5 (a). The error between the two converters is very low with a maximum error of 5 LSB. The converter output error was slightly higher at 8 LSB.

The advantage of the new converter can be seen for larger offset voltages. After an offset voltage of 18 LSB was applied to both converters, the output of the new system had an improved drift error of 8 LSB compared to the uncorrected converter, ADC 2.

5.3.4 Comparison to High Resolution Analog to Digital Converters

The new system was operated simultaneously with existing high resolution converters which were available at the Defence Research Establishment Ottawa Navigation Laboratory. An alkaline cell power supply was used as a common voltage reference for all the devices. A nominal input of 10mV with the following instruments was used:

- 1) Datron 7.5-digit multimeter, previously warmed-up, used without filtering and calibrated only at start-up.
- 2) Keithley 10-channel, 24-bit converter, warmed-up for 20 minutes, used with filtering, calibrated at startup and operated in "relative measurement mode" [45].
- 3) Racal Dana 6.5 digit (21-bit) multimeter, warmed up for 20 minutes, used without filtering and calibrated only at startup.
- 4) The New ADC system, warmed up for 20 minutes, system calibration only at startup and operated in default mode described in Chapter 4.

As seen in Figure 5.6 (a), the new ADC performed exceptionally well compared with the higher accuracy Keithley and Datron meters. Over the four hour test period, the error of about $\pm 10\mu\text{V}$ is only about $\pm 5\text{ppm}$ for the $\pm 2.5\text{ V}$ maximum input range. This output is a clear improvement of the manufacturer's specifications.

Figure 5.5 (a) : Applied Low-Voltage Input with No Offset

Figure 5.5 (b) : Applied Low-Voltage Input with Induced Offset Error

Note : The offset in ADC 2 has been reduced by ADC 1

The slow drift over the test period can be attributed to the temperature change seen in Figure 5.6 (b) or to the decay of the alkaline cell. The main advantage of the new system is the high output rate compared to the other high accuracy systems. The output rate of the new system is 250 Hz compared to the 60 Hz Keithley and the 2 Hz Datron.

Figure 5.6 (a): New Converter System compared to Existing High Resolution Analog to Digital Converters. Drift is mainly due to temperature variation and battery life decay.

Figure 5.6 (b): Recorded Ambient temperature for Converter Comparison Test. Note that the temperature sensor was approximately 1 metre from the test equipment.

The final offsets of the individual converters were recorded to be $5\mu\text{V}$ for ADC 1 and $87\mu\text{V}$ for ADC 2. The offset of the system was measured to be $5\mu\text{V}$. Although the output of the new ADC system was noisier, the offset performance of ADC 2 was improved.

5.4 Discussion

The current problems with the existing system are:

- 1) Latency correction algorithm limited by the integer arithmetic,
- 2) Reduced resolution in Converter 2,
- 3) Slow Gaussian FIR filter response.

These concerns are addressed below.

5.4.1 Correcting Errors caused by the Latency Correction Algorithm

The implementation of the Latency correction algorithm is not ideally suited for placement after the ADC subsystem. It has been shown that the unscaled integer outputs from the converter are poor inputs to the latency correction algorithm. Its placement should be in the floating point navigation algorithms, after the gyro outputs have been converted from integer values to floating point rotation rates.

5.4.2 Improving the Resolution of the System

Figure 5.6 shows the proposed implementation of the subsystem in an inertial navigation unit. Two different converters are used:

- 1) a 20-bit resolution, 10 Hz bandwidth, 4 kHz output converter is used for offset drift sensing and
- 2) a 24-bit resolution, 100 Hz bandwidth, 250 Hz output converter for gyroscope rotation rate sensing.

The higher resolution converter has a higher bandwidth which is appropriate for rotation rate sensing. The higher resolution converter was much higher in cost than the CS5503 and this prohibited its use in this project. The interfaces of the two converters are different and additional design time will be required to accommodate both converters into one system. Two 20-bit converters were selected for:

- 1) low cost and
- 2) ease of implementation.

The results of this proof of concept will decide the justification for the higher resolution converter. Note that the offset correction capability is limited by the lower resolution correction converter, and the resolution of the entire system is limited by the continuously operating higher resolution converter.

The implementation of two converters with different output rates will require extra processing. For minimum delays in the system, decimation of the high frequency output is preferred to interpolation of the low frequency signal. An alternative would be to implement both converters as high resolution 24-bit converters at a higher cost.

The latency correction algorithm will be implemented with the navigation software for reasons discussed earlier in this chapter.

5.4.3 Improved Filter Response

The 24-bit converter system chosen as a sub-component is made up of two parts, a sigma delta modulator chip and a digital filter. This allows the designer to design the digital filter to have a reduced delay compared to the Gaussian filter. The filter chip offered by Crystal is an FIR filter, so a DSP or a custom chip may need to be designed for an IIR reduced delay filter.

Figure 5.7 : The New Analog to Digital Conversion Subsystem Design with Lowered Offset Drift.

Note the placement of the Latency correction calculation from the drift corrected system to the Navigation software.

Chapter 6 Conclusions and Recommendations

6.1 Conclusions

This thesis has focused on the implementation of an ultra-precision analog to digital converter for use in an analog rebalance loop Heading Reference Unit (HRU). This has not been done before because of technology limitations, especially in the hardware of the sigma delta modulators. Technology has evolved to the point where sigma delta converters are cost competitive with standard PCM and DPCM. The sigma delta converter outperforms most standard PCM conversion techniques. Offset, offset drift and latency were identified as the main limiting factors to the implementation of analog to digital converters in inertial navigation systems.

Currently available high resolution converters can provide the precision, dynamic range and output rates required by navigation systems. The limitations of the analog to digital converters have been found to be:

1. Offsets between 50 μ V and 200 mV.
2. Drift rates from 60 μ V/hour to 0.1 mV/hour.
3. Latency (pure delay) and frequency dependant delay due to the decimation filter.

The results of this thesis show that the offsets and drifts for these high resolution converters can be controlled by using multiple converters. A latency correction algorithm was also introduced with the following restrictions:

1. Inputs must be low in change in amplitude.
2. Inputs must be low in frequency (less than 100 Hz).
3. All calculations must be made using floating point arithmetic.

The advantages from the new structure presented in this thesis are:

1. Lower cost compared to the high precision multimeters currently in use.
2. Lower drift rates due to the analog to digital conversion electronics tolerance requirements and temperature control.
3. Reduced size of the circuit due to lower component count.
4. Simplified maintainability due to the modularity of the hardware and software components.

The software for the new system is an important feature. The object oriented approach reduced design time by allowing individual components to be created and tested. The modularity will allow easy adaptation into the analog rebalance loop Heading Reference Unit.

Use of higher resolution converters with this system will allow the analog rebalance loop HRU to achieve its requirements of:

1. High resolution.
2. Low offset and offset drift.
3. Reduced latency.
4. Low cost.

6.2 Suggestions for Further Research

As discussed in Chapter 4, the two converter systems could be implemented onto the same circuit board in the final system implementation. The benefits of integrating the system onto one circuit board are:

- 1) reduce the analog input area by fifty percent,
- 2) a single clock input for the converters,
- 3) simplified power supply circuitry,
- 4) reduced ground induced noise and
- 5) reduce input noise from tolerance matching in the input protection components

A proposed PCB implementation of the final system is shown in Figure 6.1. The STD circuit board configuration shown is the standard used in the existing system. This suggested layout allows all the required circuitry to be placed on the board without crowding and has some space left for optimizing.

If a multiplexer is used to allow the converters to share the microport, the on-board area and circuitry are reduced even further. This option is not advisable since the multiplexer may degrade the performance of the system and add more ground noise.

The current polling method of data collection should be replaced by an interrupt driven system. The standard interface for most components of the existing system is the IEEE-488/1978 data interface technique and is suggested as the standard for this system. Implementing the IEEE-488 communication protocol onto the STD board will increase the amount of circuitry, however, it will allow the removal of the microport circuitry.

The effects of the overshoot of the latency correction algorithm for changing input frequencies and latencies was shown in Chapter 5. For input signals which are expected to deviate from the "low frequency, low latency" model, a filter could be designed to compensate the magnitude distortion. The output from the conversion system should have

the latency removed in floating point arithmetic for reasons described in Chapter 5. This additional processing can be done on a daughter board (possibly with an 80286 processor) before the data is passed to the main navigation computer.

A decision must also be made regarding the reference voltage source. A single voltage reference seems preferable since:

- 1) fewer components are required,
- 2) the offset in both converters due to reference voltage will be identical,
- 3) both converters will drift at the same rate due to reference voltage variation.

The only apparent drawback to this new system is the calibrating converter's inability to sense offset drifts due to reference voltage variations. Temperature variations may cause the voltage references to drift. The common drift of the references will appear as a common input signal and be passed through the system. Possible solutions to this problem are to:

- 1) use a high precision voltage reference,
- 2) use multiple voltage references,
- 3) or maintain a defined range of stable temperatures for the voltage reference.

Although only one voltage reference is shown in Figure 6.1, there is room for a second reference.

Once implemented into the inertial navigation system there will be two converters operating for each gyro, for a total of 4 new converter systems. A system with three single axis gyros would have 6 new converter systems. Issues such as health monitoring and system failure recovery must be addressed. A more precise voltage reference system for the analog to digital converters may also need to be developed.

Figure 6.1 Suggested Printed Circuit Board Layout

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Appendix A : Gaussian Filters

When designing filters to specifications, usually the magnitude response is the primary concern. To design the group delay response to be equalized over a specific frequency band an all-pass phase correction network can be placed directly in cascade with the filter. This method allows magnitude and phase characteristics to be designed somewhat independently of one another.

Whenever the phase is linear, or the group delay is constant, then for a minimum phase network, the accompanying magnitude characteristic is reasonably close to being Gaussian. Approximations to the ideal Gaussian magnitude characteristic include Bessel, Chebyshev and equiripple filters. These filters are used to approximate a constant group delay, or a linear phase maximally flat magnitude response or maximally flat group delay.

The advantage of the Gaussian filter is that it provides the smallest group delay of all the listed filters.

Design of the Gaussian Filter

Considering the ideal Gaussian magnitude characteristic:

$$|H(j\omega)| = \exp(-\omega^2 / 2) \quad \text{A.1}$$

The aim is to find an all-pole transfer function

$$H(s) = 1 / (G_a(s, \sigma)) \quad \text{A.2}$$

where $G_n(s, \mathbf{a})$ is a real Hurwitz polynomial with a coefficient vector $\mathbf{a}$, whose spectrum approximates $|H(j\omega)|$ best in the Taylor sense at the origin. We begin with:

$$H(s) H(-s) = \exp(s^2) = 1 / (\exp(-s^2)) \quad \text{A.3}$$

and define the error function as:

$$E_n(s, \mathbf{a}) = G_n(s, \mathbf{a}) G_n(-s, \mathbf{a}) - \exp(-s^2) \quad \text{A.4}$$

so that the optimum $G_n(s, \mathbf{a}) G_n(-s, \mathbf{a})$ corresponds to the truncated Maclaurin expansion:

$$G_n(s, \mathbf{a}) G_n(-s, \mathbf{a}) = 1 - s^2 + s^4 / 2! - \dots + (-1)^n s^{2n} / n! \quad \text{A.5}$$

$G_n(s, \mathbf{a})$ is isolated and the remaining expression is factored and the left-hand plane factors are retained. The transfer function is re-normalized such that the 3 dB bandwidth is unity. Humpherys [4] summarizes the solutions to this equation for $n = 2$ up to $n = 10$. For $n = 6$, the pole locations are:

$$-1.4667 \pm 1.8199i$$

$$-1.7559 \pm 1.0008i$$

$$-1.8746 \pm 0.3228i$$

These continuous-time domain poles are plotted in Figure A.1. The unscaled coefficients of the Gaussian filter will give a cutoff frequency of unity. By scaling the locations of the poles the corner frequency of the filter can be adjusted. This characteristic is shown in Figure A.2 (a) for different sampling clocks. At this point, it should be noted that the representation in Figure A.2 (a) is a continuous-time domain representation of the Gaussian Filter, and dependence on a "clock" is strictly illustrative only. The discrete-time domain response is shown in Figure A 4 (a). This response was obtained using the bilinear transform on the continuous-time representation. The properties of the Gaussian filter will be discussed in the continuous-time domain.

Properties of the Gaussian Filter

As shown in Figure A.2, the magnitude response of the filter can be selected by scaling the pole locations. The magnitude characteristics remain the same for each scaled filter, however, the group delay decreases significantly for increasing corner frequency as shown in Figure A.2 (c). The identical magnitude, phase and delay curves are shown in Figure A.3 on a linear frequency scale. It is much clearer in Figure A.3 that the lower cutoff frequency increases the slope of the phase response. From the definition of the group delay (Appendix D) the increased slope in the phase curve yields a higher delay.

For a 4.9152 MHz input clock, and an output update rate of 4800 Hz, the bilinear transform was applied to the continuous-time Gaussian filter to create Figure A.4. Only the low frequency region from 0-100 Hz is plotted for simplicity. The magnitude response shows the cutoff frequency at 10 Hz and a "flat" group delay in the passband.

Figure A.1 : Gaussian Pole-Zero Locations

(a) Magnitude Response for different clock frequencies

(b) Phase Response for different clock frequencies

(c) Delay Response for different clock frequencies.

Figure A.2 : Continuous-time Gaussian Filter Characteristics on Logarithmic Frequency Scale.

(a) Magnitude Response for different clock frequencies

(b) Phase Response for different clock frequencies

(c) Delay Response for different clock frequencies.

Figure A.3 : Continuous-time Gaussian Filter Characteristics on Linear Frequency Scale.

(a) Magnitude Response for 250 Hz output rate.

(b) Phase Response for a 250 Hz output rate

(c) Delay Response for a 250 Hz output rate.

Figure A.4 : Discrete-time Gaussian Filter Characteristics

Appendix B : Interference and Coupling

The following is a generalized discussion on Electrostatic theory, that is, the expressions are given for free space and ideal Gaussian surfaces. The concepts shown here are used in the discussion of noise sources in high accuracy systems.

Electrostatic Interference

An electrostatic field is produced by a static charge distribution, such as found in a cathode ray tube.

Coulomb's law states that the force F between two point charges (Q_1 and Q_2) is along the line joining them, proportional to the product of the charges and inversely proportional to the square of the distance R between them. This can be expressed as:

$$F = kQ_1Q_2/R^2 \quad \text{B.1}$$

or

$$F = kQ_1Q_2/R^2 \mathbf{R}_{12} \quad \text{B.2}$$

where k is a proportionality constant, Q_1 and Q_2 are in Coulombs, R is in metres, $\mathbf{R}_{12}$ is the unit vector in the direction R and F is in Newtons.

The force is a vector, F_{12} , which is the force on Q_2 due to Q_1 . This law can be extended to many charges using the principle of superposition.

The electric field intensity can then be expressed as:

$$E = F / Q \quad \text{B.3}$$

where E is the electric field intensity in the direction of the force and expressed in Newtons/coulomb or volts/metre and Q is the charge in coulombs.

The electric flux density is:

$$D = \epsilon_0 E \quad \text{B.4}$$

where D is the electric flux density (or displacement) measured in Coulombs per square metre and ϵ_0 is the permittivity of free space (Farads/metre).

Electric flux can be now defined in terms of D as:

$$\Psi_E = \int D \cdot dS \quad \text{B.5}$$

where Ψ_E is the electric flux (coulombs) and S is the surface area (square metres) penetrated by the electric flux.

Gauss's law states that the total electric flux, Ψ_E , through any closed surface (a sphere for example) is equal to the total charge enclosed by that surface, thus:

$$\Psi_E = Q_{\text{enclosed}} \quad \text{B.6}$$

This principle is shown in Figure B.1.

Suppose we wanted to move a point charge from point A to point B in an electric field E . Using Coulomb's law, the force on Q is $F = Q E$, so that the work done to displace the charge by dl is:

$$dW = F \cdot dl \quad \text{B.7}$$

The total work done is:

$$W = -Q \int E \cdot dl \quad \text{B.8}$$

The quantity V_{AB} is known as the potential difference and can be expressed

$$V_{AB} = W / Q = - \int E \cdot dl \quad \text{B.9}$$

The above formulation shows that the electrostatic interference can be found by grounding the ground lead of a probe and attaching a short bare wire to the input. (The bandwidth of the meter must be wide enough to see the resulting interference.) From Gauss's law, the total electric flux due to the charge enclosed by an imaginary Gaussian surface (i.e. a sphere) can be found.

Figure B.1 shows this principle. A charge Q is shown enclosed by an imaginary sphere. A potential measured by the meter at the surface of the sphere can be expressed as an electric field. The electric field can be expressed as a flux density, and depending on the Gaussian surface used, the total electric flux can be calculated. This calculation would be for the ideal situation, and in practical terms, minimizing the electric flux is the true goal.

Electromagnetic Interference

Electromagnetic waves are propagated by the coexistence of an electric field and a magnetic field. As electrostatic fields are related by Equation B.4 so are magnetic fields related by:

$$B = \mu_0 H \quad \text{B.10}$$

where H is the magnetic field intensity expressed in Amperes per metre, B is the magnetic flux density (or magnetic induction) in Webers per metre² and μ_0 is a constant known as the permeability of free space in Henry per metre.

Electric flux can be now defined in terms of B :

$$\Psi_E = \int B \cdot dS \quad \text{B.11}$$

where Ψ is the magnetic flux (in webers) and S is the surface area (square metres) penetrated by the magnetic flux.

Gauss's Law

$$\Psi = Q_{\text{enclosed}}$$

$$\Psi = \oint \mathbf{D} \cdot d\mathbf{S}$$

Figure B.1: Gaussian Surface Enclosing a Point Charge

Ampere's Law

$$\oint \mathbf{H} \cdot d\mathbf{l} = I_{\text{enclosed}}$$

Figure B.2 : Ampere's Law Applied to an Infinite Line Current

Recall that an electrostatic field is produced by static charges. If the charges are moving with a constant velocity, a static magnetic field is produced. This movement of charges (i.e. current flow) may be due to permanent magnets or current carrying wires.

Ampere's circuital law states that the line integral of the tangential component of H around a closed path is equal to the current enclosed by the path.

$$\oint H \cdot dl = I_{\text{enclosed}} \quad \text{B.12}$$

This principle is shown in Figure B.2.

The enclosed current could also be expressed as a current density, such that:

$$I_{\text{enclosed}} = \int J \cdot dS \quad \text{B.13}$$

where J is the volume current density in Amperes per square metre and S is the area through which the current passes in square metres.

Lenz's law states that a change in a magnetic field will induce a voltage into any loop of wire that couples to this magnetic flux. Lenz's law can be expressed by:

$$V = d\Psi_M / dt \quad \text{B.14}$$

where V is the induced voltage and $d\Psi_M/dt$ is the rate of change of the magnetic flux.

This property of Lenz's law is used in transformers where N loops are formed and the induced voltage is expressed as:

$$V = N d\Psi_M / dt \quad \text{B.15}$$

Electromagnetic interference is difficult to pinpoint, but large sources can be tested by shorting the leads of a probe and creating a loop in the region of suspicion. Ampere's law shows that an induced current in the leads of the meter by the magnetic flux intensity will be due to a stray current in the circuit.

The similarities between electrostatic and electromagnetic properties have been shown, however, there are major differences that will require different shielding techniques.

Properties of electric flux lines:

1. Lines originate at positive charges and terminate at negative charges.
2. No two flux lines can intersect except at singular or equilibrium points.
3. The electric flux density D is tangential to the flux lines at every point in an electric field.

Properties of magnetic flux lines:

1. There is no equivalent to the electric positive or negative charge. Magnetic poles will always come in N-S pairs.
2. Magnetic flux lines always close upon themselves.
3. The magnetic flux density B is tangential to the flux lines at every point in a magnetic field.

Coupling by Mutual Inductance

Just as capacitance stores electric field energy, an inductance stores magnetic field energy. By definition, the unit Henry stores one unit of magnetic flux per unit of current. From this definition, larger circuits and circuits with larger currents will have a much larger inductance.

The inductance of ground return traces on printed circuit boards are a function of the length rather than the width. Widening a return track does not substantially reduce its inductance. Providing multiple narrow tracks (such as a grid rather than a plane) that are in parallel will reduce the inductance of the line. The total inductance for two conductors will be:

$$L_{TOTAL} = (L_1 L_2 - M^2) / (L_1 + L_2 - 2M) \quad \text{B.16}$$

where L_1 and L_2 are the self inductances of the two conductors and M is the mutual inductance between them in Henries.

Mutual inductance is shown in Figure B.3, where the inductors represent the inductance of the conductors. If the conductors are close together, then the total inductance will approach the inductance of a single conductor. If the conductors are far apart, they will be loosely coupled and the total inductance will be half the inductance of a single conductor. Conductor spacing and mutual inductance were investigated by Mohr (1967) to be:

$$M = 0.107 \ln (1 + (2h)^2 / (D)^2) \quad \text{B.17}$$

where M is the mutual inductance in μH per metre, h is the height above the ground plane in metres and D is the distance between the conductors.

This calculation shows that spacing of D/h of 10 to 20 will yield a result close to the optimum reduction of 50%. For printed circuit board dimensions, this is between 1 mm and 5 mm.

If power supply and ground return traces are made very close to each other (i.e. matched on a double sided printed circuit board) then the total inductance is reduced since the supply and return currents are opposing each other at all points in the circuits. Connectors are a known source of coupling.

An excellent mathematical treatment of mutual inductance is given in Ott [28].

Coupling by Mutual Capacitance

Consider two conductors, A and B shown in Figure B.4. Conductor A is carrying a signal, and is partially shielded by a grounded sheath. Conductor B is grounded to the same ground as the sheath on conductor A. As discussed previously, when the voltage on conductor A changes, so do the electric flux lines, and the charge distribution. The ratio of charge on conductor B to the voltage on conductor A is called the mutual capacitance.

Figure B.3 : An Example of Mutual Inductance

Figure B.4 : An Example of Mutual Capacitance

If the shield completely covered conductor A, then the field would be completely contained and the mutual capacitance would be zero. If the conductors are moved further apart, the mutual capacitance decreases and the noise voltage on Conductor B is reduced.

An excellent mathematical treatment of mutual capacitance is given in Ott [28].

Appendix C : Transmission Lines

Basic circuit theory diverges from Electromagnetic Field Theory as frequency of operation increases. The consequence of this is that ordinary wires and cables become transmission lines. Transmission line effects must be considered when the effects become important to the operation of the circuit. The previous statement is deliberately ambiguous since many different variables effect the operation of a circuit as a transmission line.

One must consider the relation:

$$\lambda = c / f \quad \text{C.1}$$

where λ is the wavelength in metres, c is the speed of light (approximately 3×10^8 metres per second) and f is the frequency of operation of the circuit (in Hertz).

The wavelength will decrease when waves propagate through a medium by:

$$\lambda_d = \lambda / \sqrt{\epsilon_r} \quad \text{C.2}$$

where λ_d is the decreased wavelength in metres and ϵ_r is the relative permittivity of the material.

A rule of thumb is that a cable or wire should be considered a transmission line when the wavelength of the highest frequency in the line is less than ten times its length. For a 33-MHz signal, the longest cable length usable without considering it a

transmission line is less than one metre. This number will of course be less when considered outside free space.

The characteristic impedance is the most important parameter for a transmission line. It is given by:

$$Z_0 = [(R + j\omega L)/(G + j\omega C)]^{0.5} \quad \text{C.3}$$

where R is the series resistance per unit length (Ohm per metre), L is the series inductance (Henries per metre), G is the shunt conductance (Mho per metre) and C is the shunt capacitance (Farads per metre).

Also, L and C are related to the velocity factor by:

$$\text{velocity of propagation} = 1/\sqrt{LC} = 3 \times 10^8 / \sqrt{\epsilon_r} \quad \text{C.4}$$

General circuit theory states that the source impedance should be low while the receiving load should be high. The source and load impedances on a transmission line must match the transmission line if the signal is to pass without distortion due to reflected waves.

Printed circuit boards make excellent microstrip transmission lines, which by definition, consist of an open strip conductor and a ground plane separated by dielectric substrate (see Figure C.1 (a)). The pattern of the electromagnetic field of a microstrip line is shown in Figure C.1 (b). Clearly, the effect of transmission line phenomena is important in the design of high speed circuits.

An excellent introduction on transmission line theory is given by Sadiku [46].

(a) typical microstrip configuration

(b) field lines of a microstrip conductor

Figure C.1 : Transmission line effects

Appendix D : Glossary of Terms

Accuracy:

The precision with which a device converts a signal. Although the resolution of a signal may be n bits, its accuracy may, in fact, be less. For a 16 bit converter, the number of discrete levels is $2^{16} = 65536$. For an input dynamic range of 2 volts, the spacing of the discrete levels is only $30\mu\text{V}$. For this device, the resolution is 16 bits, however, if the spacing between the discrete levels is less than $30\mu\text{V}$, the accuracy specification is less than 16 bits.

Bits:

In a standard analog to digital converter, inputs are sampled and held, then converted to discrete quantization levels, usually a thermometer code. The quantization levels are translated into a binary coded signal. Each element of the binary coded signal is called a bit. With an increased number of bits, the precision of the device is increased.

Dynamic Range:

The ratio of the full-scale (rms) signal to the broadband noise signal. Broadband noise is measured with the input grounded within the bandwidth of interest. Units in decibels (dB).

Full-Scale Error:

The ratio of the difference between the value of the voltage reference and the analog input voltage to the full scale span (2 times the voltage reference value). This ratio is calculated after the effects of offset and the external bias components are removed and the analog input voltage is adjusted. Units in percent (%).

Full Scale Input Overrange:

The absolute maximum negative or positive voltage allowed for either accurate system calibration or accurate conversions. Units in volts.

Gain Bandwidth Product (GBP) :

In setting the closed-loop gain (or bandwidth) of an amplifier, there must be a trade-off, since the Gain Bandwidth Product (GBP) is constant, that is:

$$GBP = G * BW = constant = f_t \quad \text{D.1}$$

where G is an approximation of the closed loop gain, $G+1$, and BW is the bandwidth.

Gain Error:

Deviation of the ideal output code caused by an error in the gain of the converter. The effect of the gain error is shown in Figure D.1 (c). This error can be removed externally by adjusting the reference voltage to the converter.

Group Delay:

The delay through a component of the system. Defined as:

$$\tau_g = - (1/2\pi) * d\phi / df \quad \text{D.2}$$

where τ_g is the group delay, ϕ is the phase of the system and f is the frequency. The deviation of the group delay from a constant indicates the degree of non-linearity in the phase.

Input Span:

The voltages applied to the analog input pin in the calibration mode of the converter. The input span specification indicates the minimum and maximum inputs that the converter can accept and still calibrate gain accurately. The span is defined from the zero-scale to the full scale in unipolar mode or from positive full scale to negative full scale in bipolar mode. Units in volts (V).

Intermodulation Distortion:

The ratio of the rms sum of the two test frequencies that are each 6 dB down from full scale to the rms sum of all intermodulation components within the bandwidth of interest. Units in decibels (dB).

Latency:

Pure delay between the output code and its corresponding input signal. Units in milliseconds (msec).

Least Significant Bit (LSB):

The bit in a binary coded signal that contributes the smallest amount. In a 16 bit word, the difference in 1 LSB is shown in the following example.

$(1010\ 1010\ 0101\ 0101)_{\text{binary}} = (\text{AA55})_{\text{hex}} = (43605)_{\text{decimal}}$

$(1010\ 1010\ 0101\ 0100)_{\text{binary}} = (\text{AA54})_{\text{hex}} = (43604)_{\text{decimal}}$

Linearity Error:

Also known as end-point linearity. The deviation of a code from a straight line connecting the two endpoints of the A/D converter transfer function as shown in Figure D.1 (f). One endpoint is located 1/2 LSB below the first code transition and the other endpoint is located 1/2 LSB beyond the code transition to all ones. Note that some converters are specified by their best fit to a straight line as

shown in Figure D.1 (e). The best fit method does not have a mathematical definition. Unit in percent of full-scale.

Linearity (Differential) :

Also known as Differential Non-Linearity (DNL) This measure is used to describe deviations of a code's width from its ideal width. Units in Least Significant Bits (LSB). See Figure D.1 (d).

Linearity (Integral) :

Also known as Integral Non-Linearity (INL) This measure is used to describe the maximum overall deviation from an end-point line characteristic. Units in Least Significant Bits (LSB). See Figure D.1 (e).

Missing Codes :

If the DNL is larger than one code width, it is possible for an output code to disappear. Many converters that have DNL smaller than one ideal code width will specify "No Missing Codes".

Offset:

The difference between the analog ground and the analog voltage necessary to yield a unipolar output code of zero (00H). Offset may be specified for Unipolar (0 volts to some positive fixed voltage) or Bipolar (a range of inputs from a fixed negative voltage to a fixed positive voltage) inputs. Unipolar Offset is the deviation of the first code transition from the ideal (1/2 LSB above analog ground) when in unipolar mode. Bipolar Offset is the deviation of the mid-scale code transition (011...111 to 100...000) from the ideal (1/2 LSB below analog ground) when in bipolar mode. Units in Least Significant Bits (LSB) or millivolts (mV). See Figure D.1 (b).

Offset Drift:

The change in the offset value with temperature. Units in $\mu\text{V}/^\circ\text{C}$.

Passband Frequency:

The signals passed within the specified frequencies band. The edge of the pass band is specified where the pass band power drops by 50% (or -3 dB).

Quantizer:

A Quantizer is a device that produces one output for a range of input voltages. The difference between the input voltage and the quantized output voltage is the noise added to the loop.

Resolution:

The specified precision of a device. Usually calculated from a ratio, ie, a device with 1:1,048,576 is said to have a resolution of 0.000095% or about 1 ppm. The number of bits can be found from this requirement using 2^n , where n is the number of bits (in this case, $n=20$). Usually expressed in bits, parts per million (ppm), percent of full scale (%). See also Accuracy.

Signal to Distortion Ratio (SDR):

The ratio of the full scale (rms) signal to the rms sum of all harmonics up to the maximum passband frequency. Units in decibels (dB).

Signal to Noise Ratio (SNR):

A common figure of merit for a converter is its Signal to Noise Ratio (SNR). The ratio of the rms value of the signal to the rms sum of all other spectral components below the Nyquist rate (except dc), including the distortion components. The desired SNR can be related to the number of bits of resolution of a converter (shown in many introductory texts on digital communications). An approximation of the relation is:

$$SNR = 6.02 * n + 1.72 \quad D.3$$

where SNR is the signal to noise ratio in dB and n is the number of bits. This relation shows that the SNR improves by 6.02 dB for each bit added to the resolution of the converter. The constant 1.72 is for an ideal sinusoidal input and will change with different input signals.

Signal to Peak Harmonic or Spurious Noise:

The ratio of the rms value of the signal to rms value of the next largest spectral component below the Nyquist rate (except dc). This component is often an aliased harmonic when the signal frequency is close to the sampling rate. Units in decibels (dB).

Signal to Quantization Noise Ratio (SQNR):

Quantizers must express an analog input signal by a discrete value. This quantization error leads to the Signal to Quantization Noise Ratio (SQNR) which can be expressed as:

$$SQNR = 6.02 * n + 1.76 \quad D.4$$

where SQNR is the signal to quantization noise ratio in dB and n is the number of bits. This equation clearly shows that the SQNR improves by 6 dB for each bit of resolution added. The constant 1.72 is for an ideal sinusoidal input and will change with different input signals.

Thermometer Code:

A binary representation of a signal, where larger signals are represented by a larger ratio of high signals.

a) Ideal ADC transfer function

b) ADC Offset Error

c) Gain Error

d) Differential Non-Linearity

e) Linearity measure using Best fit method

f) Linearity measure using End Point method

Figure D.1 : Measurement of Linearity in Analog to Digital Converters

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