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THE DESIGN AND EVALUATION OF A NEW
SLOTLINE-TYPE FREQUENCY DIVIDER

by

© Grigorios Kalivas, Dipl. Eng.

A thesis
submitted to the
Faculty of Graduate Studies and Research
in partial fulfilment of the requirements
for the degree of
Master of Engineering
in
Electrical Engineering

Department of Electronics

Carleton University
Ottawa, Ontario

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The undersigned recommends to the Faculty of Graduate Studies and Research, the acceptance of the thesis,

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submitted by Grigorios Kalivas, Dipl. Eng., in partial fulfilment of the requirements for the degree of Master of Engineering in Electrical Engineering.

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ABSTRACT

A systematic design procedure for a slotline-type frequency divider has been developed. The principle of operation of these devices is based on the design of a subharmonic resonator which is isolated from the input "pump" circuit. The resonator and the input circuit interact only via the nonlinear reactances of two varactor diodes.

A Computed-Aided-Design (CAD) technique is used in this thesis in order to develop a suitable output circuit. The same program (named COMPACT) is used for analysis and optimization of the final divider circuit.

The effectiveness of the design procedure is tested by fabricating two frequency divider circuits designed in the 3.5-8.0 GHz band. A "two-signal" method for measuring "pumped" input and output impedances is then employed. The experimental evaluation of the halver (including both performance and "pumped" impedance measurements) is in good agreement with the theory.

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LIST OF PRINCIPAL SYMBOLS

A	Cross-sectional area of the junction
α_c	Conductor loss
α_d	Dielectric loss
α_r	Radiation loss
α_T	Total microstrip loss
a_i	Incident waves ($i=1,2$)
B	Stray capacitance parameter
β	Phase constant
b_i	Reflected waves ($i=1,2$)
c	Velocity of light
C_j	Diode junction capacitance
C_p	Package capacitance
C_i	A voltage-invariant capacitance between the metal top constant to the semiconductor chip, and n^+ substrate.
C_f	Open circuit end capacitance
$\Gamma_{d.in}$	Input reflection coefficient of the divider
$\Gamma_{d.out}$	Output reflection coefficient of the divider
Γ_M	Measured values of reflection coefficients
Γ_r	True values of reflection coefficients
Γ_{trans}	Reflection coefficient of CPW or microstrip to coax transition
e	Electron charge
ϵ, ϵ_r	Dielectric constant
ϵ_{eff}	Effective dielectric constant of substrate

ϵ_{re}	Coplanar waveguide effective dielectric constant
f_c	Cutoff frequency
F_c	Large-signal cutoff frequency
ϕ	Thermal equilibrium potential barrier at the p-n junction
G_j	Small-signal conductance
h	Substrate thickness
L_p	Package inductance
l_{eo}	Equivalent end-effect length
λ_s	Slotline wavelength
λ_g	Guided wavelength
λ_o	Free space wavelength
m_K	Modulation ratio
N_A	Acceptor concentration on the p-side of an abrupt junction
N_D	Donor concentration on the n-side of an abrupt junction
v	Normalized frequency
P_{in}	Input power
Q	Total charge in either half of depletion layer
Q_F	Small-signal quality factor
Q_V	Overall quality factor
r_s	Series resistance
R_s	Surface resistivity
ρ_c	Sensitivity of the strip conductor
s	Coplanar strip width
S_j	Junction elastance

S_{ij}	Scattering parameters ($i=1,2, j=1,2$)
S_B^A	Sensitivity of A with respect to B
σ	A parameter used as a phase term in the solution of Mathieu D.E.
t	Conductor thickness
$\tan\delta$	Loss tangent
U_p	Pumping voltage
U_s	Output voltage
V_p	Phase velocity
V_T	Total bias point
w	Microstrip width, slotline width
W_{eff}	Effective strip width
X	Pumping amplitude
x	Forcing function
y	Output variable
$Y(w)$	Equivalent admittance
Z_0	Characteristic impedance of microstrip
$Z_{d.in}$	Input impedance of the frequency divider
$Z_{d.out}$	Output impedance of the frequency divider
Z_{ocp}	Coplanar waveguide characteristic impedance
Z_{os}	Characteristic impedance of slotline
Z_L	Load impedance
$Z_{in 2\omega_0}, Z_{in f}, Z_{in}$	"Pumped" input impedance
$Z_{in \omega_0}, Z_{out f}, Z_{out}$	"Pumped" output impedance
Z_V	Varactor small-signal impedance
ω_0	Output frequency

CHAPTER 1

INTRODUCTION

1.1 Introduction

Microwave frequency halvers are used to translate very wide microwave bands to lower frequencies where either analog or digital signal manipulation can be easily accomplished. They generally operate on the principle of converting a pump (input) frequency to an output frequency equal to half the input frequency, using two varactor diodes which compose a subharmonic resonator.

The pump and subharmonic circuits are isolated from each other and they interact only via the nonlinear reactances imposed by the two varactor diodes. Hence, the two diodes constitute a balanced structure where the generated subharmonic signal, which exists as the difference between the varactor voltages, is free of even-order harmonics of f_0 . When the varactor-pair is pumped at the input frequency f_{in} the devices are excited equally both in magnitude and phase. If the input power level is small, then frequency division will occur only over a rather narrow bandwidth in the vicinity of the small-signal subharmonic resonance frequency. However, for input power levels larger than a threshold level the bandwidth will expand considerably mainly towards the lower frequencies of operation.

Some of the many interesting properties and characteristics of the microwave frequency halvers are listed below [1]:

- (a) Ability to function without the need of a local oscillator;
- (b) Accurate frequency-division by two;
- (c) Ability to cover octave bandwidths provided power is above threshold.

Typical applications include [1]:

- (a) Frequency translation of microwave signals;
- (b) High-quality microwave signal generation for communications;
- (c) Increase the effective modulation index of a PLL when direct FM modulation of the VCO is used;
- (d) Indirect amplification.
- (e) Down conversion in frequency counters.

1.2 Approach-Objective

In this thesis 4-8GHz slotline type frequency halvers using MIC circuitry are built and measured. For this purpose, the input and output circuits must be designed in such a way as to get the best possible matching to the impedances presented by the two varactors. Hence the input circuit consists of microstrip stepped transformer sections (tapered transformers can also be used) that are used to match the 50 Ω external world to the parallel-connected pumped varactor impedances. The resonator is of slotline type and is located at the bottom side of the substrate between the two diodes, and is designed to tune out the imaginary part of the small signal impedance of the two varactors which are effectively connected in series at f_0 . After the resonator an output circuit is

designed in order both to match the load to the 50Ω output and to transform it from the balanced output of the slotline resonator to an unbalanced one in order to be connected to a 50Ω load.

As can be seen (Section 2.2) the resonance is not symmetrical with respect to frequency. The larger part of the bandwidth increase with signal level occurs at frequencies below the small-signal resonance f_0 . This means that the resonator should be designed so that the required higher output frequency of the halver occurs at or near the small-signal resonance frequency.

The basic characteristics of a slotline type frequency halver are the following:

- (1) An increase of the bandwidth of operation can be achieved with proper design of input and output circuits using computer-aided design (CAD) methods.
- (2) Experimentally, optimization of the performance can be obtained by varying the bias voltage of the two varactor diodes and/or by varying the lengths or widths of the various elements of input and output circuits including the resonator itself.
- (3) The resonator must be designed to be as short as possible (5° - 20°) in order to achieve wideband operation.

The aims of this thesis are:

- (i) To use a CAD method to optimize the input and output matching circuits.
- (ii) To design and measure various usable output circuits such as to be both suitable matching circuits and to act as balanced-to-

unbalanced transitions.

- (iii) To employ a large-signal impedance measurement method to obtain Z_{in} and Z_{out} of the device while it is actually operating as a frequency halver. In this way one can use the measured large-signal impedances to make a new design that could give a better performance.

1.3 Thesis Organization

The subsequent chapters of this thesis are arranged as follows:

In the second chapter a suitable background theory is given. The basic structure, characteristics and equivalent circuits of the varactor diode are given as well as a brief presentation of the frequency halving theory. Finally, design equations of microstrip and slotline are presented briefly.

In Chapter 3, various kinds of output circuits are considered and their ability to match a frequency-variable load is calculated and measured. As well as providing matching, these circuits have to present good balance-to-unbalance transformation characteristics. In particular, two different kinds of slotline-to-coax transitions are designed using CAD methods and their experimental performance is given.

Chapter 4 deals with the overall frequency divider (FD) design using computer-aided-design methods. Two circuits are designed in this way, using slotline-to-coplanar waveguide (CPW) transitions in the output. Their experimental performance is given as well.

In Chapter 5 a two-signal large signal impedance measurement method is used in order to extract input and output impedance data from the devices tested in Chapter 4.

Finally, in Chapter 6, the conclusions of this thesis are given as well as suggestions for further work.

CHAPTER 2

BACKGROUND THEORY

2.1 Varactors

2.1.1 Introduction

Experience in the last few decades has shown that the varactor diode is one of the most useful of the many kinds of semiconductor diodes.

The potential of microwave devices based on the variable capacitance principle was first described by Uhlir [2], in 1958. Uhlir predicted that these diodes would be useful in the following kinds of microwave devices:

1) Frequency multipliers (Harmonic generators)

Here the varactor is excited at a frequency ω_0 and power is delivered to a load at frequency $2\omega_0$ or $3\omega_0$ or in general $N\omega_0$ for some integer N . Harmonic generators are useful in frequency control and comparison systems, and for generation of moderate amounts of microwave power [3].

2) Parametric mixers (Frequency converters)

This kind of application requires the interaction of three or more frequencies. If a large current at frequency ω_p and a small current at frequency ω_s are simultaneously put through a varactor, sidebands with frequencies of the form $n\omega_p \pm \omega_s$ are generated. At one of these frequencies, power flows to a load [3].

3) Subharmonic generators (divide by 2,3,...,n circuits)

These are similar to the previous case, but here the output frequency is lower than ω_s . The device investigated in this thesis belongs to this category.

4) Switches and limiters

5) Parametric Amplifiers

Here the concept of negative resistance can be used as an amplifying mechanism.

The semiconductors principally used for manufacturing varactors are Si and GaAs; epitaxy is usually used to minimize series resistance.

2.1.2 Varactor Characteristics

Modern practical varactors are made from semiconductor diodes. All p-n junctions exhibit nonlinear barrier capacitance. If this effect "predominates" in some sense, then the junction can be used to advantage as a varactor diode. We have various kinds of diodes depending on the nature of the junction: the abrupt-junction diode, the graded-junction diode and the hyperabrupt-junction diode.

In the abrupt-junction diode the doping changes abruptly (Figure 2.1(a)) from an excess of donors to an excess of acceptors whereas in the graded-junction diode the doping changes gradually from p-type to n-type (Figure 2.1(b)). In practice, many varactors are neither exactly abrupt nor exactly graded. At zero volts and low forward bias voltages, varactors can be better approximated by the abrupt junction model than by the graded one. The theory of the abrupt p-n junction gives the following charge-voltage relationship [4]:

(a)

(b)

Figure 2.1 (a) Charge Density in an Abrupt Junction
(b) Doping Density of a Graded Junction

$$Q(V) = A \sqrt{2e\epsilon \frac{(\phi_0 - V)}{\left(\frac{1}{N_D} + \frac{1}{N_A}\right)}} \quad (2.1)$$

where:

Q = total charge in either half of depletion layer

A = cross-sectional area of the junction

e = electron charge

ϵ = permittivity

ϕ_0 = thermal equilibrium potential barrier at the p-n junction

V = total external voltage across the p-n junction

N_A = acceptor concentration on the p side of an abrupt junction

N_D = donor concentration on the n side of an abrupt junction

This relationship is presented graphically in Figure 2.2(a). A large signal capacitance or an "equivalent large signal" capacitance cannot be well defined because the varactor is fundamentally a device with a nonlinear V-Q characteristic which means that its capacitance can only be defined as a small signal quantity. At a given bias voltage V_0 the junction capacitance can be defined as follows:

$$C_j(V_0) = - \left. \frac{dQ}{dV} \right|_{V_0} \quad (2.2)$$

From (2.2) and (2.1):

$$C_j(V_0) = \frac{A}{2} \sqrt{\frac{2e\epsilon}{\frac{1}{N_D} + \frac{1}{N_A}}} \cdot \frac{1}{\phi_0 - V_0} \quad (2.3)$$

Figure 2.2 (a) Varactor Q-V Characteristic
(b) Varactor C-V Characteristic

The value given usually by the manufacturers is the junction capacitance at zero bias voltage:

$$C_j(0) = \frac{A}{2} \sqrt{\frac{2e\epsilon}{\frac{1}{N_D} + \frac{1}{N_A}} \cdot \frac{1}{\phi_0}} \quad (2.4)$$

Hence (2.3) can be written as follows:

$$C_j(V_0) = \frac{C_j(0)}{\sqrt{1 - \frac{V}{\phi_0}}} \quad (2.5)$$

Equation (2.5) is plotted in Figure 2.2(b).

The small-signal quality factor of $C_j(V)$ in parallel with $G_j(V)$ is given by:

$$Q_F = \frac{\omega C_j(V)}{G_j(V)} = \frac{\text{stored energy}}{\text{dissipated energy/cycle}} \quad (2.6)$$

where $G_j(V)$ is the small signal conductance shown in Figure 2.3(c). For the linearly graded junction the $C_j(V)$ expression corresponding to (2.5) is:

$$C_j(V) = \frac{C_j(0)}{(1 - \frac{V}{\phi_0})^{1/3}} \quad (2.7)$$

Generally, the $C_j(V)$ law may be written:

$$C_j(V) = \frac{C_j(0)}{(1 - \frac{V}{\phi_0})^n} \quad (2.8)$$

Usually the abrupt-junction varactor is the preferred device in most practical applications as mentioned above.

$C_j(V)$ in (2.5), (2.7) and (2.8) is the voltage-dependent capacitance associated with the depletion layer. This is the dominant nonlinearity under reverse bias conditions ($V < 0$). However, the diffusion capacitance dominates under forward bias. Using (2.1) and (2.4) $Q(V)$ can be expressed in terms of $C_j(0)$ and V :

$$Q(V) = 2 C_j(0) \sqrt{\phi_0} \sqrt{\phi_0 - V} \quad (2.9)$$

2.1.3 Varactor equivalent circuit

Various varactor equivalent circuits are shown in Figures 2.3(a), (b), (c), and (d). The simplest useful one is that of Figure 2.3(d).

In each case the voltage-dependent junction capacitance is represented by $C_j(V)$, r_s is the series resistance. L_p is package inductance while C_p is the package capacitance. C_j in Figure 2.3(b) represents a voltage-invariant capacitance between the metal (usually gold) top contact to the semiconductor chip, and the n^+ substrate. $G_j(V)$ is a voltage-dependent conductance used for forward bias conditions (nonlinear junction conductance). In Figure 2.4(a) a typical varactor structure is shown while in Figure 2.4(b) one can see the physical origin of the parasitic circuit elements.

The most important feature of the varactor diode, after the nonlinear junction capacitance, is the series resistance r_s which is physically due to the bulk resistance of the semiconductor and to the resistance of the leads. The series resistance depends on the depletion-layer thickness (because it is a function of the integral of semiconductor bulk resistivity over the region outside the depletion layer). Referring to Figure 2.3(c), the elements associated with the junction itself are:

Figure 2.3 (a), (b), (c) & (d) Various Varactor Equivalent Circuits

(a)

(b)

Figure 2.4 (a) A Typical p^+nn^+ Varactor Structure
 (b) A Typical Packaged Varactor and the Physical Origin of its Parasitic Elements

r_s , $G_j(V)$ or $R_j(V)$ and $C_j(V)$ and the impedance of the varactor diode is:

$$Z_Y = r_s + R_j \parallel \frac{1}{j\omega C_j} = \frac{r_s[1+(\omega C_j R_j)^2] + R_j - j\omega C_j R_j}{1 + (\omega C_j R_j)^2} \quad (2.10)$$

This expression gives an overall quality factor of:

$$Q_Y = \frac{\omega C_j R_j^2}{r_s[1+(\omega C_j R_j)^2] + R_j} \quad (2.11)$$

If $R_j(V) \ll r_s$ (forward bias) then (2.11) gives:

$$Q_F = \omega C_j(V) R_j(V) = \frac{\omega C_j(V)}{G_j(V)} \quad (2.12)$$

If $r_s \ll R_j(V)$ (reverse bias) the quality factor of $C_j(V)$ and r_s in series dominates:

$$Q_R(V) = \frac{1}{\omega r_s C_j(V)} \quad (2.13)$$

Another parameter usually quoted by manufacturers is the varactor "cutoff frequency". It is defined as that frequency at which the capacitance reactance $\omega C_j(V)$ becomes equal to r_s :

$$f_c(V) \triangleq \frac{1}{2\pi r_s C_j(V)} \quad (2.14)$$

Usually it is defined at 0 volts:

$$f_c(0) \triangleq \frac{1}{2\pi r_s C_j(0)} \quad (2.15)$$

But frequently $V = -6$ volts is used as the voltage at which f_c is defined:

$$f_c(-6) \triangleq \frac{1}{2\pi r_s C_j(-6)} \quad (2.16)$$

A generally useful relation is:

$$f_c(V) = f_{Q_R}(V) \quad (2.17)$$

This is particularly useful for measurement purposes. The cutoff frequency $f_c(V)$ as defined above is an indicator of varactor loss under small-signal conditions. The large-signal cutoff frequency F_c defined below is a measure of varactor loss under large-signal conditions [3]:

$$F_c \triangleq \frac{1}{2\pi r_s} (S_j^{\max} - S_j^{\min}) \quad (2.18)$$

where $S_j(V) = \frac{1}{C_j(V)}$ = junction elastance

$$S_j^{\min} = \frac{1}{C_j(0)} \text{ (elastance at 0 volts)}$$

$$S_j^{\max} = \frac{1}{C_j(-V_{BR})} = \frac{1}{C_j(0)} \cdot \sqrt{1 + \frac{V_{BR}}{\phi_0}} \text{ (elastance at reverse breakdown)}$$

Using (2.18) one can get:

$$F_c = f_c(0) \left[\sqrt{1 + \frac{V_{BR}}{\phi_0}} - 1 \right] \quad (2.19)$$

Considering now the simplest equivalent circuit for reverse bias, (package capacitance C_p is neglected) the small-signal impedance of the varactor is:

$$Z_V = j\omega L_p + r_s - \frac{j}{\omega C_j(V)} \quad (2.20)$$

The cutoff frequency is:

$$f_c(V) = \frac{1}{2\pi r_s C_j(V)} \quad (2.21)$$

The diode series resonance will occur at a frequency:

$$f_{SR}(V) = \frac{1}{2\pi\sqrt{L_p C_j(V)}} \quad (2.22)$$

Using (2.21) and (2.22), (2.20) gives:

$$\frac{Z_V}{r_s} = 1 - j \frac{f_c(V)}{f} [1 - (\frac{f}{f_{SR}(V)})^2] \quad (2.23)$$

Equation (2.23) shows that the varactor impedance is capacitive at frequencies below the self-resonant frequency $f_{SR}(V)$, but that it becomes inductive at higher frequencies. It should be noted that the selection $S_j^{\min} = \frac{1}{C_j(0)}$ used for the definition of large signal cutoff frequency F_C is somewhat arbitrary. One might choose

$$S_j^{\min} = \frac{1}{C_j(+0.5V)} \quad \text{for Si} \quad \text{or}$$

$$S_j^{\min} = \frac{1}{C_j(+1V)} \quad \text{for GaAs}$$

depending on the semiconductor material and the application. Penfield and Rafuse [3] explain that the choice of the numerator of F_C as in (2.18) is the best that could be chosen among other possible quantities expressing various numerical combinations of $S^{\max}$ and $S_{\min}$ like:

$$S^{\max} + S^{\min}, \frac{1}{S^{\max}} + \frac{1}{S^{\min}}, \text{ etc.}$$

Another group of quantities used for varactor characterization are the modulation ratios [3]:

$$m_k = \frac{|S_k|}{S_{\max} - S_{\min}} \quad (2.24)$$

where S_k represents the k^{th} Fourier coefficient of the series

$$S(t) = \sum_{k=-\infty}^{\infty} S_k e^{jk\omega_p t} \quad (2.25)$$

$S(t)$ is the pumped elastance supposing that the pumping proceeds at frequency ω_p and its harmonics. The large-signal cutoff frequency F_c is associated with another useful concept characterizing varactor quality under pumped conditions. This is called the pumped figure of merit and is equal to $|S_1| \cdot r_s^{-1}$. The same quantity (F_c) is useful in describing the fundamental limits of large-signal devices, such as harmonic multipliers, harmonic dividers and large signal frequency converters and amplifiers. Another quantity that appears in formulas for pump power and power-handling capabilities of large-signal varactor devices is the normalization power P_{norm} [3]:

$$P_{\text{norm}} = \frac{(V_{B+\phi})^2}{r_s} \quad (2.26)$$

The higher the normalization power (for a given cutoff frequency) the higher the power levels that the varactor is inherently capable of handling but conversely, the higher the power necessary to pump the varactor.

2.2 Frequency Dividers [5]

2.2.1 Introduction

Like other nonlinear reactances, varactors have the peculiar property that they can, when pumped, generate power not only at harmonics of the pumping frequency but also at subharmonics and at rational fractions of the pumping frequency. When generating subharmonics as in the frequency halver which is the device of interest in this thesis, varactors behave like oscillators. A brief presentation of frequency halver principles and equations follows in the remainder of this part of Chapter 2, which comes from the Ph.D. thesis by Harrison [5].

2.2.2 General Presentation and Evolution of Frequency Dividers

Frequency division, or subharmonic generation, can be obtained when a capacitance is a continuous (or discontinuous) function of time. Considering the circuit of Figure 2.5(a), the equation characteristic of it is the following [5]:

$$\frac{d^2 Z'}{d\tau'^2} + Z'[1 - X' \cos 2v\tau] = 0 \quad (2.27)$$

where $Z(\tau) = Z'(\tau) e^{-k\tau/2}$, Z = charge q normalized to an arbitrary constant charge, $v = \omega/\omega_0 = 1/\alpha$, $\tau = \omega t$, $k = \frac{1}{\omega_0 C_0 R}$ = damping term.
 $(\tau' = \sqrt{\alpha'} \tau, \alpha' = 1 - 1/4 k^2, X' = X/\alpha)$.

This equation can have harmonic, fundamental, or 1/2-order subharmonic solutions for v less than 1/2, $v = 1/2$ or $v = 1$ respectively. The exact conditions for oscillation depend on the pumping amplitude X

Figure 2.5 (a), (c) and (d) Circuits Used to Analyze the Initial Forms of Frequency Dividers
(b) Frequency Stability Chart for a Frequency Divider in the $(v-X)$ Plane [5]

as well as the frequency ω . The canonical form of this equation is Mathieu's differential equation (D.E.):

$$\frac{d^2 Z}{dX^2} + (a - 2p \cos 2X) Z = 0 \quad (2.28)$$

$$\text{where } p = \frac{aX}{2}. \quad (2.28a)$$

In general there are two kinds of solution for this D.E., stable and unstable. From the point of view of subharmonic generation, the solution of interest is one of the 2 independent unstable solutions [5]:

$$Z = e^{\mu X} [\sin(x-\sigma) + a_3 \cos(3x-\sigma) + b_3 \sin(3x-\sigma) + a_5 \cos(5x-\sigma) + b_5 \sin(5x-\sigma) + \dots] \quad (2.29)$$

where $\mu > 0$ or :

$$Z(\tau) = e^{\mu \nu \tau} [\sin(\nu \tau - \sigma) + a_3 \cos(3\nu \tau - \sigma) + b_3 \sin(3\nu \tau - \sigma) + a_5 \cos(5\nu \tau - \sigma) + b_5 \sin(5\nu \tau - \sigma) + \dots] \quad (2.30)$$

σ is a parameter taking a value between 0 and $-\pi/2$ and can be calculated in terms of a and p .^{*}

The important point is that the first term of the above series represents a frequency equal to half the forcing function. The frequency stability chart for the parametric frequency divider in the (ν, X) -plane [5] is as in Figure 2.5(b). The region of interest is the unstable shaded region denoted "subharmonic oscillation" where the fundamental component of the solution is at half the input

* C. Hayashi, "Nonlinear Oscillations in Physical Systems", McGraw-Hill, 1964, p.91.

frequency and the amplitude of the oscillation grows without limit as time increases.

In a frequency halver the capacitance variation is achieved by pumping one or more varactor diodes. Practical low frequency (10-20MHz) halvers that have been built and measured [5], showed considerable disagreement between their (v, X) diagrams and the corresponding appropriate solution of the Mathieu equation. It was found that the resemblance is only qualitative. Some points of disagreement are listed below:

- (1) The boundaries of the curve "bend the wrong way".
- (2) The measured results show a region of hysteresis within which the subharmonic oscillations may or may not exist. This hysteresis behaviour is not predicted by any solution of Mathieu's D.E.
- (3) In practice it was found that although the amplitude of the subharmonic output does increase exponentially initially, it soon saturates at a well-defined level. This saturation is not accounted for by the Mathieu D.E. representation. All this means that a different approach, through the formulation and solution of appropriate nonlinear D.E.s, is needed in order to obtain a satisfactory explanation of the observed phenomena.

Figure 2.5(c) shows a topology of a circuit that can be used to analyze parametric up-converters and down-converters employing nonlinear capacitive reactance. It is possible for a divide-by-two

circuit to be constructed using this configuration. The two circuits, simply, have to be tuned to ω and $\omega/2$ as indicated. However, in practical applications of frequency halvers, this kind of tuning is undesirable for the following reasons:

(a) The bandwidth of operation will necessarily be small because high-Q tuned circuits are needed to isolate the input and output frequencies and, as is well known, the bandwidth is inversely proportional to the Q factor ($\Delta\omega \propto 1/Q$)

(b) The high energy storage of such tuned circuits will limit the rate at which the frequency halver can respond to RF pulses.

In order to avoid this kind of problem one can remove the two linear capacitors (as indicated in Figure 2.5(d)) and consider that L_1 and the nonlinear (NL) capacitor are tuned to ω and that L_2 and the NL capacitor are resonant at $\omega/2$.

Although some of the non-essential energy-storing elements have now been removed, their elimination means that a large number of unwanted harmonics will appear because the filtering is now poor. Further reduction of the number of energy-storing elements, results in the circuits of Figure 2.6(a).

Figure 2.6(b) shows the output voltage waveform of the second circuit in Figure 2.6(a) for $V_p(t) = V_p \sin \omega t$. It can be seen that the output contains a lot of undesired frequencies in addition to the desired $1/2$ th subharmonic. The problem of obtaining an output

Figure 2.6 (a) Single Tuned Unbalanced Frequency Halving Circuits
 (b) Output Waveform of the Series Single Tuned Circuits [5]

signal with reduced harmonic content, while at the same time minimizing the energy storage can be solved by "adding together" a pair of circuits of the voltage-driven type shown above.

There are two ways of doing it, one way resulting in a balanced circuit where the varactors are both oriented in the same direction, the other resulting in a circuit where the varactors point in opposite directions. Hence in Figure 2.7 one can see the "evolution" of the two basic types of balanced varactor frequency-halving circuits. In all cases the voltage source represents the input at the pump frequency.

In the series type circuit the pump is applied using a hybrid transformer with a center-tapped secondary. The current i_p (pump frequency current) circulates in the outer loop such that the two diodes are either forward-driven or reverse-driven together. The varactors are excited 180° out of phase at the subharmonic frequency because the corresponding current i_s circulates in opposite directions in the two loops of the circuit. These currents add in the central inductor, across which the subharmonic output voltage is developed. In the parallel type of circuit the pump voltage is applied directly to the center-tap of the inductor, and a transformer is not needed for the circuit to operate. Currents i_p circulate in opposite directions in the two loops, exciting the two varactors in parallel.

The output voltage is developed across the inductor because the subharmonic-frequency current i_s circulates in the outer loop. The

Figure 2.7 "Evolution" of the Two Basic Types of Balanced Varactor Frequency-Halving Circuits [5]

output signal is therefore balanced.

In both these types of frequency-divider the balanced form of the circuits has the effect of suppressing the even-order harmonics of the input frequency, while the output voltage is predominantly sinusoidal. The input frequency band is suppressed at the output because it is the second harmonic of the $1/2$ subharmonic and even-order harmonics are suppressed as has been mentioned above.

Hence these circuits have the important property that the pump and subharmonic circuits are isolated from each other and they interact only via the nonlinear reactances.

2.2.3 Equations and Solutions of Balanced Frequency Halver

(a) First order Quasi-Static theory of Balanced Freq. Halver

Before considering the differential equations of practical frequency halvers, a brief discussion will be given of the quasi-static theory of the series-type balanced frequency halver. The method is based on the expansion of the nonlinear reactance function in a power series about the total bias point $V_T \triangleq V_0 + \phi_0$. Only the first two terms of the series are retained, so that the validity of the analysis is restricted to small voltage excursions about V_T . The quasi-static assumption implies that the rates of change of amplitude and phase of the output voltage $U_s(t)$ developed across L are negligibly small. The equation for the current through the inductor is:

$$i \approx -2 C_0 V_T \frac{d}{dt} [y(nx+1)] \quad (2.31)$$

where:

$$x = \frac{U_p}{V_T} \text{ (forcing function), } y = \frac{U_s}{V_T} \text{ (output variable)}$$

The approximate equivalent admittance (at the subharmonic frequency) appears in parallel with L and written in "linear" notation is:

$$Y(\omega) = j2\omega C_0 - n\omega C_0 \frac{U_p}{V_T} e^{-j2\theta} \quad (2.32)$$

The angle θ represents the phase with which the output signal is generated.

The equivalent circuit at the subharmonic frequency ω , for $\theta=0$ or π is shown in Figure 2.8(a). The tuned circuit in parallel with the negative conductance gives rise to exponentially growing oscillations. For $\theta=\pm\frac{\pi}{2}$ the equivalent circuit is that of Figure 2.8(b) containing a positive conductance that leads to exponentially decaying oscillations.

The admittance of a varactor at the pump frequency is:

$$\frac{1}{2} Y(2\omega) = j2\omega C_0 + \frac{1}{2} n\omega C_0 \frac{U_s^2}{V_T U_p} \quad (2.33)$$

The power supplied by the pump, $P_{2\omega}$, is equal to the power P_ω generated at the subharmonic frequency at the particular phase angles $\theta=0, \pi$, (power balance occurs only at $\theta=0, \pi$). Conservation of energy requires that the small-signal subharmonic phase angle θ must tend to one or other of these values.

(a)

(b)

Figure 2.8 (a) Subharmonic Frequency Equivalent Circuit for $\theta=0, \pi$ (Quasi-Static Approximation)
 (b) Subharmonic Frequency Equivalent Circuit for $\theta=\pm\pi/2$ (Quasi-Static Approximation)

Since the amplitude and phase of the third harmonic (3ω) signal are not known in relation to those of the subharmonic (ω) (because there are no 3ω terms in the equation (2.31)), this approach cannot show the effect of third harmonics on the admittance $Y(\omega)$. To sum up, this quasi-static method shows that the small-signal equivalent circuit of the frequency-halver is, in a sense, a function of the past history of the device. No steady-state solution is predicted, and detuned cases are not covered. The solution does not hold rigorously under transient conditions either.

(b) Voltage Differential Equations and Solutions of Balanced Frequency Halvers

Contrary to the situation in a linear system, the nature of the differential equation of a nonlinear system depends on the way in which it is formulated. Consider first the voltage D.E. of an unbalanced frequency divider such as that in Figure 2.9(a):

$$\frac{d}{d\tau} [(1+y)^{-n} \overset{0}{y}] + k(1+y)^{-n} \overset{0}{y} + y = x(\tau) \quad (2.34)$$

where $x = \frac{U_p}{V_T}$ (pump voltage), $y = \frac{U_s}{V_T}$ (voltage across varactor), $\overset{0}{y} = \frac{dy}{dt}$

$$\tau = \omega_0 t, \quad \omega_0 = \frac{1}{\sqrt{LC_0}}, \quad k = \omega_0 C_0 r_s \quad (2.34(a))$$

Now, the voltage general D.E. for both balanced series-type and parallel-type frequency halvers is the following:

(a)

(b)

(c)

Figure 2.9 (a) Unbalanced Frequency Divider Circuit
 (b) Balanced Series Type Circuit
 (c) Balanced Parallel-Type Circuit [5]

$$\frac{1}{a(1-n)} \frac{d^2}{d\tau^2} [(1+x+\frac{1}{2}ay)^{1-n} - (1+x-\frac{1}{2}ay)^{1-n}] +$$

$$+ k \frac{dy}{d\tau} + y = 0 \quad (2.35)$$

where $a = 2$ for the series type

$a = 1$ for the parallel type

$$y = \frac{U_s}{V_T}, \quad x = \frac{U_p}{V_T}, \quad \tau = \omega_0 t$$

$$\omega_0 = \frac{1}{\sqrt{2LC_0}} \quad \text{for the series-type circuit (two } C_0 \text{'s in parallel)}$$

$$\omega_0 = \sqrt{\frac{2}{LC_0}} \quad \text{for the parallel-type circuit (two } C_0 \text{'s in series)}$$

$$k = \omega_0 LG_L \quad \text{for the series-type circuit}$$

$$k = \omega_0 L/R_L \quad \text{for the parallel-type circuit.}$$

In these circuits the resistance r_s of the varactor has been neglected for simplicity. As far as the generation of subharmonics is concerned the pumping function $x(\tau)$ is coupled to the tuned circuit only via the nonlinear reactances as was mentioned above in this chapter. This can be seen by setting $n=0$ in equation (2.35). This has the effect of linearizing the reactances.

Equations (2.34) and (2.35) show the essential difference between the D.E.'s of balanced and unbalanced frequency halvers: it is in the nonlinear term that contains the output variable y . These terms are unsymmetrical functions of y in the unbalanced halvers but antisymmetrical functions in the balanced ones.

Expanding the nonlinear function in a series about the operating point and truncating at the third power, the generalized 'voltage' D.E. (2.35) can be reduced to the following form [15]:

$$\frac{d^2}{d\tau} \left[nxy + \frac{1}{2}n(n+1)(x^2y) + \frac{1}{12}a^2y^3 \right] + \overset{\infty}{y} + ky + y = 0 \quad (2.36)$$

which is valid under the following constraints:

$$|x| < 1$$

$$\left| \frac{1}{2}ay \right| < 1$$

Approximating the normalized output voltage $\bar{y}$ by:

$$\bar{y} = Y(\tau) \cdot \sin(\nu\tau + \theta(\tau)) \quad (2.37)$$

and using the Harmonic Balance method [5] to solve (2.36) one can get (eliminating θ) for the steady-state solution

$$Y^2 = \frac{8}{a^2} \left\{ \frac{1}{\beta} \left[\left(\frac{1-\nu^2}{\nu^2} \right) \pm \sqrt{(\alpha X)^2 - \left(\frac{k}{\nu} \right)^2} \right] - X^2 \right\} \quad (2.38)$$

$\theta(\tau)$ is the phase being referred to that of the normalized pump voltage

$$X(\tau) = X \sin 2\nu\tau$$

$$\alpha = \frac{1}{2} Bn, \quad \beta = \frac{1}{4} Bn(n+1), \quad B = \frac{2C_0}{2C_0 + C_s} \quad (2.38(a))$$

B is named the "stray capacitance parameter". C_s = varactor package capacitance plus other stray capacitances. Equation (2.38) (the solution of (2.36)) describes how the amplitude Y of the normalized 1/2-subharmonic output voltage depends on the normalized pump-voltage amplitude X and the normalized frequency ν ($\nu=1$ is the resonance condition). The boundary

of the region in which 1/2 subharmonics are possible, on the (v, X) plane is given by setting $Y=0$ in Equation (2.38):

$$X^2 = \frac{1-v^2}{\beta v^2} + \frac{1}{2} \left(\frac{\alpha}{\beta} \right)^2 \pm \left(\frac{\alpha}{\beta} \right) \sqrt{\frac{1-v^2}{\beta v^2} + \frac{1}{4} \left(\frac{\alpha}{\beta} \right)^2 - \left(\frac{k}{\alpha v} \right)^2} \quad (2.39)$$

This represents the frequency characteristic.

Figure 2.10(a) shows the predictions of Equation (2.39) compared with the measurements of Harrison [5] for a series type frequency halver. It is seen that the agreement is satisfactory only when $X < 0.7$, $v > 0.96$. The first inequality is reasonable, taking into account that the reactive nonlinearity has been approximated by a truncated power series, an approximation that begins to fail for $X > 0.8$.

Also shown in Figure 2.10(a) are the measured and calculated "nose-loci" which define the low- X limit of the hysteresis region. Hysteresis phenomena cease when the interior of the root of Equation (2.38) becomes negative. For a fixed frequency v , Equation (2.38) gives a curve on the (X, Y) -plane which is usually called the (X, Y) -profile. In Figure 2.10(b) calculated (X, Y) -profiles are illustrated [5]. One can notice that the profiles are double-valued in Y over a certain range of X for $v < 1$, i.e. there is "amplitude hysteresis".

For example, if $v = 0.98$ hysteresis occurs in a certain range $X_N < X < X_{FC}$. There is no frequency division until $X = X_{FC}$. Then frequency division suddenly begins and the amplitude jumps to $Y = Y_{FC}$. For larger values of X , Y remains on the stable part of the profile (positive root in (2.38)). If X is decreased, the upper part of the (X, Y) -profile is retraced until the "nose" (X_N, Y_N) is reached where Y drops to zero.

Figure 2.10 (a) Measured and Calculated Frequency Characteristic [5]
 (b) Calculated X-Y Profile of a Frequency Halver [5]

An important detail about the design of the resonator will close this section: As can be seen from Figure 2.10(a) the operational band is not symmetrical with respect to the small-signal resonance frequency ω_0 (most of the bandwidth increase occurs below ω_0).

Thus, the subharmonic-frequency resonator must be designed so that the small-signal resonant frequency ω_0 falls near the upper limit of the required band of output frequencies.

2.2.4 Expressions for the input and output "impedances" of pumped frequency halvers

The slotline type of frequency halver that is to be studied in this thesis is a parallel-type balanced device, since the varactors are excited in parallel. This can be easily seen in the next chapter.

Hence, for the input "impedance" to be calculated, the two varactors have to be considered in parallel, as in Figure 2.11(a). R_V is the "effective" pumped resistance in that figure. According to Penfield and Rafuse [3], the drive level-dependent "input impedance" at $2\omega_0$ for a single varactor is:

$$Z_{in}|_{2\omega_0} = r_s + \frac{S_0}{j2\omega_0} + \frac{m_1^2}{2m_2} \cdot \frac{\omega_0}{2\omega_0} r_s e^{-j\theta} \quad (2.40)$$

where:

S_0 = non-time-varying term of the Fourier expansion of the varactor elastance waveform (see Equation (2.25))

(a)

(b)

Figure 2.11 (a) Equivalent Input Impedance of Two Varactors in Parallel
(b) Microstrip Configuration [7]

$$m_1 = \frac{|S_1|}{S^{\max} - S^{\min}} = \text{modulation ratio at output frequency } \omega_0$$

(Equation (2.24))

$$m_2 = \frac{|S_2|}{S^{\max} - S^{\min}} = \text{modulation ratio at input frequency } 2\omega_0$$

(Equation (2.24))

$$\omega_c = \frac{S^{\max} - S^{\min}}{r_s} = 2\pi F_c \text{ (large-signal cutoff frequency)}$$

ω_0 = output frequency.

Note that Z_{in} is not the input impedance of the circuit in the usual sense.

The varactor is a nonlinear device and does not have an input impedance.

The ratio of input voltage to input current is however a well-defined

concept, and its value depends on the drive level. As a first approximation

one can take $1/S_0 \approx C_j(V_0)$. (This is to be interpreted as the average capacitance of the varactor, depending on both bias V_0 and drive level).

One can also consider that the load can be tuned such that $\theta=0$ [3], which

is the condition for highest efficiency. Another assumption that should

be made is that the varactor is driven from the breakdown voltage V_B to the bias where $C_j \rightarrow \infty$ (so that $S^{\min} \rightarrow 0$). This simplifies the expression

for ω_c to:

$$\omega_c = \frac{S^{\max}}{r_s} = \frac{(1 + \frac{V_B}{\phi})n}{r_s C_j(0)} \quad (2.41)$$

The quantity $m_1^2/2m_2$ must now be evaluated. For the maximum efficiency of an abrupt-junction divide-by-2 at low frequencies (compared to ω_c or F_c) we have:

$$m_1 = 0.208, \quad m_2 = 0.08 + \frac{m_1^2}{2m_2} = 0.27 \quad (2.42)$$

For maximum output power P_{out} the corresponding values are:

$$m_1 = 0.192, \quad m_2 = 0.096 \quad \frac{m_1^2}{2m_2} = 0.192 \quad (2.43)$$

Another way of calculating this ratio is to assume that the junction voltage is constrained such that the swing is limited between forward conduction and reverse breakdown [3]. In this case, the constraint is:

$$m_1 + m_2 \leq 1/4 \quad (2.44(a))$$

Another relation is given by the Manley-Rowe equation for a halver:

$$m_1^2 \omega_0 = m_2^2 2\omega_0 \quad (2.44(b))$$

$$\text{Hence } m_1 = \sqrt{2} m_2 \quad (2.45)$$

Assuming maximum pumping, (2.44) can be considered as:

$$m_1 + m_2 = 1/4 \quad (2.46)$$

Using (2.45) and (2.46) one finds:

$$m_1^2 / 2m_2 = 0.207 \quad (2.47)$$

Hence, between (2.42) and (2.43) and (2.47) a reasonable compromise is:

$$\frac{m_1^2}{2m_2} = 0.20 \quad (2.48)$$

Using reasonable assumptions one can take for the approximate* input

-
- * 1. a practical halver may be driven significantly into forward bias.
 2. the drive may not go from S^{max} to S^{min} .

impedance expression, from (2.40) and including L_p :

$$Z_{in}|_{\omega} = r_s + 0.2 \frac{(1 + \frac{V_B}{\phi})^n}{\omega C_j (0)} + \frac{1}{j\omega C_j (V_0)} + j\omega L_p \quad (2.49)$$

where $\omega = 2\omega_0$ (input frequency).

For two varactors in parallel (as in Figure 2.10(c)):

$$Z_{in}|_{\omega} = \frac{1}{2} [r_s + 0.2 \frac{(1 + \frac{V_B}{\phi})^n}{\omega C_j (0)}] - j \frac{1}{2} [\frac{1}{\omega C_j (V_0)} - \omega L_p] \quad (2.50)$$

For the output impedance, the real part under pumped conditions is [3]:

$$R_{out} = r_s (\frac{m_2 \omega_c}{\omega_0} \cos \theta - 1) \quad (2.51)$$

As before, $\theta=0$ and Equation (2.51) gives:

$$R_{out} = r_s (\frac{m_2 \omega_c}{\omega_0} - 1) \quad (2.52)$$

taking into account that $\omega_0 < m_2 \omega_c$.

Also as before:

$$\omega_c = \frac{s_{max}}{r_s} = \frac{(1 + \frac{V_B}{\phi})^n}{r_s C_j (0)} \quad (2.41)$$

For the output of a slotline-type halver the varactors are connected in series (see next chapter). For the output circuit, R_{out} plays the role of R_V in the varactor equivalent circuit.

Hence, regarding the above discussion, the total output impedance for 2 varactors in series at the output frequency ω_0 is approximately

$$Z_{out}|_{\omega_0} \approx 2[0.1 \frac{(1 + \frac{V_B}{\phi})^n}{\omega_0 C_j(0)} - r_s] - j2[\frac{1}{\omega_0 C_j(V_0)} - \omega_0 L_p] \quad (2.53)$$

where we have put $m_2 \approx 0.10$ (from the previous discussion).

2.3 Microstrip Transmission Lines

2.3.1 Introduction

Two decades ago, the strong need for miniaturization of components and the availability of high-quality, low-loss dielectrics made microstrip transmission line the subject of considerable investigation. Today the more important characteristics of microstrip lines are well documented.

Below, some of the advantages of the circuits which are built using microstrip transmission lines are mentioned [6]:

(a) The complete conductor pattern can be deposited and processed on a single dielectric substrate which is supported by a single metal ground plane, avoiding the higher cost of waveguide or coaxial circuit configurations.

(b) Beam-leaded active and passive microwave devices can be bonded directly to metal strips on the dielectric substrate.

(c) Devices and components incorporated into hybrid integrated circuits are accessible for probing and circuit measurements. The following sections of this part of the chapter present briefly the basic mathematical expressions and characteristics for microstrip transmission lines.

2.3.2 Basic Microstrip Equations

Microstrip is a two-conductor transmission line which can be considered to have evolved conceptually from a two-wire line. It consists of a strip conductor and a ground plane separated by a flat dielectric substrate of small thickness, as shown in Figure 2.11(b). The important microstrip parameters are:

w = strip width, h = substrate thickness

ϵ_r = dielectric constant, t = conductor thickness

The inhomogeneous medium consisting of the dielectric substrate and the air above it causes a discontinuity in the electric and magnetic fields, which results in a propagating mode that is not pure TEM but quasi-TEM. The following represent some of the methods used to characterize the performance of the microstrip line [7]:

- 1) The Conformal transformation method
- 2) The Finite Difference Method (relaxation method)
- 3) The Integral equation method (Green's function method)
- 4) The Variational Method in the Fourier Transform Domain (FTD)
- 5) The Hybrid mode analysis.

The first four methods are based on the quasi-TEM approximation. The last one involves extensive computation. For the quasi-TEM mode of propagation, the phase velocity in microstrip is given by [6]:

$$V_p = \frac{c}{\sqrt{\epsilon_{eff}}} \quad (2.54)$$

where c = velocity of light,

ϵ_{eff} = effective dielectric constant of the substrate.

$$\text{Microstrip wavelength } \lambda_g = \frac{v_p}{f} \quad (2.55)$$

Closed form expressions for characteristic impedance Z_0 and ϵ_{eff} have been reported by Schneider [6] and Hammerstad [8], and are given below:

For $w/h \leq 1$,

$$Z_0 = \frac{60}{\sqrt{\epsilon_{\text{eff}}}} \ln (8h/w + 0.25 w/h) \quad (2.56)$$

where

$$\epsilon_{\text{eff}} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \left[\left(1 + 12h/w \right)^{-1/2} + 0.04 \left(1 - \frac{w}{h} \right)^2 \right] \quad (2.57)$$

For $w/h \geq 1$,

$$Z_0 = \frac{120\pi / \sqrt{\epsilon_{\text{eff}}}}{w/h + 1.393 + 0.667 \ln (w/h + 1.444)} \quad (2.58)$$

$$\text{where } \epsilon_{\text{eff}} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} (1 + 12h/w)^{-1/2} \quad (2.59)$$

Simple and accurate formulas for ϵ_{eff} and the effective strip width W_{eff} which take into account the finite strip thickness t are [9]:

$$\text{For } w/h \leq \pi/2 \quad W_{\text{eff}}(o) = w + \frac{t}{\pi} \left(1 + \ln \frac{4\pi w}{t} \right) \quad (2.60)$$

$$\text{For } w/h \geq \pi/2 \quad W_{\text{eff}}(o) = w + \frac{t}{\pi} \left(1 + \ln \frac{2h}{t} \right) \quad (2.61)$$

$$\text{and } \epsilon'_{\text{eff}} = \epsilon_{\text{eff}} - \frac{\epsilon_r - 1}{4.6} \frac{t/h}{\sqrt{w/h}} \quad (2.62)$$

Above a certain frequency f_0 , the phase velocity, Z_0 and ϵ_{eff} begin to change with frequency and the transmission line become dispersive. This frequency f_0 is:

$$f_0 = \frac{6.0}{(\epsilon_r - 1)^{1/4}} \sqrt{\frac{Z_0}{h}} \quad (2.63)$$

where h is in mils and f_0 is in GHz.

The results for $Z_0(f)$, $\epsilon_{\text{eff}}(f)$ and $W_{\text{eff}}(f)$ are given below [10]:

$$Z_0(f) = \frac{120 \pi h}{W_{\text{eff}}(f) \sqrt{\epsilon_{\text{eff}}(f)}} \quad (2.64)$$

$$W_{\text{eff}}(f) = W - \frac{W_{\text{eff}}(0) - W}{1 + (f/f_g)^2} \quad (2.65)$$

where

$$f_g = \frac{c}{2W_{\text{eff}} \sqrt{\epsilon_{\text{eff}}}} \quad (2.66)$$

$$\epsilon_{\text{eff}}(f) = \epsilon_r - \frac{\epsilon_r - \epsilon_{\text{eff}}}{1 + (0.6 + 0.009 Z_0) \left(\frac{f}{f_p}\right)^2} \quad (2.67)$$

where

$$f_p(\text{GHz}) = \frac{15.66 Z_0}{h(\text{mils})} \quad (2.68)$$

$$\text{and } W_{\text{eff}}(0) = \frac{120 h}{Z_0 \sqrt{\epsilon_{\text{eff}}}} \quad (2.69)$$

Losses

There are three types of losses in microstrip lines: Conductor losses, dielectric losses and radiation losses. The total loss per unit length is:

$$\alpha_T = \alpha_d + \alpha_c + \alpha_r \quad (2.70)$$

The two components α_c and α_d are given by [9]:

For $w/h \leq 1$

$$\alpha_c = 1.38 A \frac{R_s}{h Z_0} \cdot \frac{32 - (w_{eff} h)^2}{32 + (w_{eff} h)^2} \text{ dB/unit length} \quad (2.71)$$

for $w/h \geq 1$

$$\alpha_c = 6.1 \times 10^{-5} A \frac{R_s Z_0 \epsilon_{eff}}{h} \left[w_{eff}/h + \frac{0.667 w_{eff}/h}{w_{eff}/h + 1.444} \right] \text{ dB/unit length} \quad (2.72)$$

$$\text{and } \alpha_d = 27.3 \frac{\epsilon_r}{\epsilon_r - 1} \frac{\epsilon_{eff} - 1}{\epsilon_{eff}} \frac{\tan \delta}{\lambda_0} \text{ dB/unit length} \quad (2.73)$$

where λ_0 = free-space wavelength.

$$R_s = \sqrt{\pi f \mu_0 / \rho_c} \text{ } \Omega \text{ } P_c = \text{resistivity of the strip conductor}$$

$$\sigma = \omega \epsilon_0 \epsilon_r \tan \delta = \text{conductivity of the dielectric substrate}$$

$$A = 1 + \frac{h}{w_{eff}} \left\{ 1 + \frac{1.25}{\pi} \ln \frac{2h}{t} \right\} \quad (\text{for } w/h \geq \pi/2) \quad (2.74)$$

$$A = 1 + \frac{h}{w_{eff}} \left\{ 1 + \frac{1.2}{\pi} \ln \frac{4\pi w}{t} \right\} \quad (\text{for } w/h \leq \pi/2) \quad (2.75)$$

The radiation losses are smaller than the conductor and dielectric losses for thin substrates at higher frequencies.

2.3.3 Microstrip end effects

The region near the end of an open-circuited microstrip line stores much more accumulated charge than the remaining part of the strip. There are three main phenomena associated with the "open circuit":

- (a) Fringing fields extending beyond the abrupt end of the metal strip.
- (b) Surface waves launched from the end of the strip.
- (c) Energy radiated from the open end.

Item (a) may be accounted for by assuming some equivalent capacitance to be connected at the open end and this feature almost always dominates the end-effect. Several quasi-static field calculations of the open circuit end capacitance C_f have been documented, the most reliable of which seems to be the work of Silvester and Benedek [11]. The expression is:

$$\frac{C_f}{w} = \exp \left\{ 2.2036 \sum_{i=1}^5 k_{\epsilon} \left(\log \frac{w}{h} \right)^{i-1} \right\} \text{ pF/m} \quad (2.76)$$

where the coefficients k_{ϵ} are functions of ϵ_r and are given in [11] for various values of ϵ_r . An equivalent end-effect length can be calculated to be:

$$l_{eo} \approx \frac{c Z_0 C_f}{\sqrt{\epsilon_{eff}}} \quad (2.77)$$

Alternatively it is directly given by an empirical expression [12]:

$$l_{eo} = 0.412h \left(\frac{\epsilon_{eff} + 0.30}{\epsilon_{eff} - 0.258} \right) \cdot \left(\frac{w/h + 0.262}{w/h + 0.813} \right) \quad (2.78)$$

2.3.4 Impedance step discontinuities

In microstrip circuits involving transmission lines in series, the impedance step discontinuities cause distortion of the electric and magnetic fields, which results in capacitive and inductive effects.

The reactance that is introduced by the impedance step discontinuity can be modelled by several equivalent circuits. The most reliable of these consists of a shunt capacitance C_s in the plane of the junction and a series inductor ΔL_s on either side of it. According to Garg and Bahl [13] these elements are given by:

$$\frac{C_s}{\sqrt{W_1 W_2}} \text{ (pF/m)} = 130 \log \left(\frac{W_2}{W_1} \right) - 44 \quad (2.79)$$

for $\epsilon_r = 9.6$ and $3.5 \leq W_2/W_1 \leq 10$. For ΔL_s the equation is:

$$\frac{\Delta L_s}{h} \text{ (nH/m)} = 40.5 \left(\frac{W_2}{W_1} - 1.0 \right) - 75 \log \frac{W_2}{W_1} + 0.2 \left(\frac{W_2}{W_1} - 1 \right)^2 \quad (2.80)$$

The error in Equation (2.79) is claimed to be less than 0.5%, and better than 5% in (2.80) provided that $W_1/W_2 \leq 5.0$.

W_1 and W_2 represent the widths of the two successive microstrip transmission lines.

2.4 Slotlines

2.4.1 Introduction

Slotline is an alternative transmission structure proposed for use in MICs by Cohn in 1968. The basic slotline configuration is shown in Figure 2.12(a). It consists of a dielectric substrate with a narrow slot etched in the metallization on one of the surfaces of the substrate. The other surface of the substrate has no metallization. The geometry is planar and is well suited for use in microwave integrated circuits.

An advantage of slotlines is that they can be included in microstrip circuits by etching the slotline circuit in the ground plane of the microstrip circuit [7]. Another advantage is that circuit elements which cannot easily be achieved in a microstrip configuration can be incorporated in the slotline part of the circuit such as short circuits, high impedance lines ($Z_0 > 120 \Omega$) or series stubs.

2.4.2 Slotline Design Equations

In a slotline the wave propagates along the slot with the major electric field component oriented across the slot in the plane of metallization on the dielectric substrate.

The mode of propagation is non-TEM and almost transverse electric in nature. However, unlike conventional waveguides, there is no low cut-off frequency because slotline is a two-conductor structure. One can see approximate field distributions for slotline in Figure 2.12(b).

(a)

----- MAGNETIC FIELD LINES
 ———— ELECTRIC FIELD LINES

(b)

Figure 2.12 (a) Slotline Configuration [7],
 (b) Field Distributions in a Slotline [7]

The basic slotline parameters are:

W = slot width

h = substrate thickness

ϵ_r = dielectric constant

The most widely used method of slotline analysis is the one given by Cohn [14] which employs a transverse resonance approach.

Other methods available and various analytical techniques are listed below:

- (a) approximate analysis [14]
- (b) the transverse resonance method [14]
- (c) Galerkin's method in Fourier Transform Domain (FTD) [15-16]
- (d) analysis in elliptical coordinates [17].

None of these methods of analysis lead to closed form expressions for slotline wavelength and impedance. Closed-form expressions have been obtained by curve fitting [18] the results based on Cohn's analysis, where the analysis and impedance evaluation is based on the power-voltage relationship: $Z_{os} = V^2/2P$, V = peak voltage across the slot, P = average power. These expressions have an accuracy of about 2% for the following sets of parameters:

$$9.7 \leq \epsilon_r \leq 20$$

$$0.02 \leq W/h \leq 1.0 \quad \text{and}$$

$0.01 \leq h/\lambda_0 \leq (h/\lambda_0)_c$ where $(h/\lambda_0)_c$ is equal to the cut-off value for the TE_{10} surface-wave mode on the slotline. The expressions obtained are:

1) For $0.02 \leq W/h < 0.2$

$$\lambda_s/\lambda_0 = 0.923 - 0.448 \log \epsilon_r + 0.2 W/h - (0.29 W/h + 0.047) \log (h/\lambda_0 \times 10^2) \quad (2.81)$$

$$\begin{aligned} Z_{0s} = & 72.62 - 35.19 \log \epsilon_r + 50 \frac{(W/h - 0.02)(W/h - 0.1)}{W/h} \\ & + \log (W/h \times 10^2) [44.28 - 19.58 \log \epsilon_r] \\ & - [0.32 \log \epsilon_r - 0.11 + W/h (1.07 \log \epsilon_r + 1.44)] \\ & \cdot (11.4 - 6.07 \log \epsilon_r - h/\lambda_0 \times 10^2)^2 \end{aligned} \quad (2.82)$$

2) For $0.2 \leq W/h \leq 1.0$

$$\lambda_s/\lambda_0 = 0.987 - 0.483 \log \epsilon_r + W/h (0.111 - 0.0022 \epsilon_r) - (0.121 + 0.094 W/h - 0.0032 \epsilon_r) \log (h/\lambda_0 \times 10^2) \quad (2.83)$$

$$\begin{aligned} Z_{0s} = & 113.19 - 53.55 \log \epsilon_r + 1.25 W/h (114.59 - 51.88 \log \epsilon_r) \\ & + 20 (W/h - 0.2) (1 - W/h) \\ & - [0.15 + 0.23 \log \epsilon_r + W/h (-0.79 + 2.07 \log \epsilon_r)] \\ & \cdot [10.25 - 5 \log \epsilon_r + W/h (2.1 - 1.42 \log \epsilon_r) - h/\lambda_0 \times 10^2]^2 \end{aligned} \quad (2.84)$$

The logarithms are to the base 10 in the above expressions.

A FORTRAN program named SLOT.F97HARRG has been written using these expressions in order to calculate the slot wavelength λ_s and the

characteristic impedance Z_{0s} . Using this program one observes that impedances Z_{0s} less than 45Ω are hard to realize because the width of the corresponding slotline should be less than $50\mu\text{m}$. This is a physical limitation.

The disadvantage of the expression (2.81) - (2.84), is that the upper limit on the value of W/h has been restricted to unity since Cohn's analysis of slotline is valid only for $W \leq h$.

However, another FORTRAN program named PAROS has been written for calculations with $W/h \geq 1$. This program is due to Siweris [19] and has been slightly modified here. It makes use of the definition of the characteristic impedance Z_{0s} given by Cohn:

$$Z_{0s} = \frac{\pi^3 W^2}{4 \int_0^\infty \text{int}_z(W, h, f, \epsilon_r, \epsilon_{\text{eff}}, x) dx} \quad (2.85)$$

$$\text{and } \int_0^\infty \text{int}(W, h, f, \epsilon_r, \epsilon_{\text{eff}}, x) dx = 0 \quad (2.86)$$

The integrals int and int_z are transcendental functions. The program consists of a main program and four FUNCTION- subprograms. The program, a brief description of each subprogram and the input and output variables are presented in Appendix I.

Although this method uses Cohn's analysis it can be used for $W/h \geq 1$ because Cohn's method gives accurate results for $W/h \geq 1$ as compared with Galerkin's method in the Fourier Transform Domain (FTD) [15]. One can see this in Figure 5.9, p.212 in [6] for $W/h = 2.0$. Since Galerkin's method has no limitation on W/h , this means that Cohn's method gives

accurate results not only for $W/h \leq 1$ but also for $W/h \geq 1$. This is why one can solve equations (2.85) and (2.86) using the computer and take accurate results for $W/h \geq 1$. Using this second program PAROS one can easily find that values of $Z_{0s} = 200\Omega$ and higher can be obtained. The only limitation is that the slotwidth should be $W \leq \lambda_s/4$.

2.4.3 Slotline Discontinuities

As in the case of microstrip circuits, the characterization of slotline discontinuities is important for the design of slotline circuits. However, only very limited experimental results are available [20].

A short circuit is created by merely ending the slot or equivalently filling the slot with a conducting surface lying in the plane of the slot. In this case a current flows around the end of the slot and there is appreciable energy storage beyond the termination. The net result is a predominance of stored magnetic energy giving rise to a inductive reactance.

CHAPTER 3

FREQUENCY DIVIDER OUTPUT DESIGN CONSIDERATIONS3.1 Computer Aided Output Circuit Design3.1.1 Introduction

It has been made clear in the second chapter that one of the main elements of the output section of a frequency halver is the resonator itself. In this thesis the resonator is of the slotline type. Figure 3.1 shows the output of a slotline type frequency divider (F.D.) and its equivalent circuit representation. The slotline resonator is etched on the back side of a two-sided metal coated substrate. On the upper side of the substrate the microstrip input circuit of the device is etched. Z_v represents the pumped impedance of each varactor at a particular bias level. The purpose of the slotline resonator (θ_1 , Z_1) is to tune out the reactive components at small signal subharmonic resonance frequency f_{SSR} . θ_1 is the phase length at f_{SSR} and Z_1 the characteristic impedance of the resonator.

If the output of the resonator is directly connected to the 50 Ω external world through a standard slotline to microstrip transition [21] there will be reflections due to impedance mismatch. In Table 3.1 one can see the resulting VSWRs if one connects $Z_{out}|_f$ directly to a 50 Ω load. Still, taking into account the reflections due to the transition itself the output VSWR will be much larger than that indicated in Table 3.1. Some other kinds of output circuits which can considerably reduce the output VSWR of the device will be discussed in this chapter.

F (MHz)	RHO (MAGN. < ANGLE)	VSWR	RET L/G (DB)	Z(R+jx) OHM
2000	0.312	1.91	-10.12	59.11 -34.54
2200	0.274	1.75	-11.25	53.63 -29.27
2400	0.242	1.64	-12.31	49.07 -24.72
2600	0.218	1.56	-13.23	45.21 -20.69
2800	0.202	1.51	-13.89	41.90 -17.07
3000	0.196	1.49	-14.17	39.03 -13.79
3200	0.198	1.49	-14.07	36.52 -10.76
3400	0.208	1.52	-13.65	34.31 - 7.96
3600	0.224	1.58	-13.01	32.34 - 5.33
3800	0.243	1.64	-12.27	30.58 - 2.86
4000	0.266	1.73	-11.50	28.99 - 0.52

Table 3.1 Output VSWR for $Z_{out}|f$ Connected Directly to a 50 Ω Load

Figure 3.1 (a) Slotline Resonator
(b) Output Equivalent Circuit

The first has been designed and tested by Schiek [22] and will be referred to from now on, as Schiek's Transition. The second one is a slotline-to-coplanar-waveguide (CPW) transition using a Marchand balun (2nd, 3rd, or 4th order) structure [23-25].

These transitions and how they can be designed in order to minimize the output VSWR of the device will be investigated in detail below.

3.1.2 Design of the resonator

Since the edge of the upper-side microstrip represents a virtually common potential connection between the two varactors, looking at the output circuit side, the two varactors are considered to be connected in series in the output. (This has already been mentioned in the second chapter). Here the formula which has been obtained in the second chapter for the pumped output impedance of the two varactors in series will be used:

$$Z_{out_{AA'}} = Z_{out}|_f \quad (3.1)$$

This impedance is presented at AA' without taking into account the slotline resonator section (θ_1, Z_1) which will give another impedance Z_{res} that should be added to $Z_{out_{AA'}}$ in order to find the total output impedance Z_{out} . In this project type GC-1504 silicon tuning varactors made by Frequency Sources, Inc., GHz Division, are used. These devices are mounted in the style 85 package. Brief information about this specific diode is given in Appendix II. For this diode: $r_s = 0.56\Omega$, $V_B = 30$ volts, $L_p = 0.15nH$, $C_j(o) = 3.5pF$ (manufacturer's data). Low frequency bridge measurements (1MHz Boonton 75D) gave $C_j(o) = 3.2pF$. Using these values one can calculate $Z_{out_{AA'}} = Z_{out}|_f$ applying Equation 2.53. Here it must be made clear that Equation 2.53 does

not necessarily represent the true impedance that would be measured under large signal conditions at the plane of the diodes looking from the output but it is the most reliable closed-form expression which can be used to initiate the design of the halver. Large signal impedance measurements can be made after the halver has been implemented in order to effect in an improvement in the design and performance of the device. As has been stated in the previous chapter the resonator should be calculated at the top-end of the output band, i.e., in this case at 4GHz, in order to achieve the desired bandwidth. For the resonator $Z_{res} = jZ_1 \tan \theta_1$ (short-circuit stub).

Hence the resonance condition is:

$$jZ_1 \tan \theta_1 - j2 \left[\frac{1}{\omega C_j(V)} - \omega L_p \right] = 0 \Big|_{4\text{GHz}} \quad (3.2)$$

Hence:

$$\theta_1 = \arctan \left\{ \frac{2 \left(\frac{1}{\omega C_j(V)} - \omega L_p \right)}{Z_1} \right\} \Big|_{4\text{GHz}} \quad (3.3)$$

In order to achieve maximum bandwidth the electrical length θ_1 should be reasonably small (5° - 15°). Using this criterion Z_1 can be chosen to be 60-100 Ω . The output impedance that should be matched to 50 Ω is:

$$Z_{out|f} = R_e(Z_{out|f}) + j[I_m(Z_{out|f}) + Z_1 \tan \theta_1] \quad (3.4)$$

3.1.3 Schiek's Transition

3.1.3.(a) General Description

In Figure 3.2(a,b) one can see the form of this transition. The dashed line part of the figure represents the slotline circuitry at the back side of the substrate while the solid line part on the upper side is the microstrip input. The transition has been made by Schiek on alumina (Al_2O_3) of thickness $h=0.020$ " with a relative permittivity $\epsilon_r=10$. These specifications are close enough to the Duroid* 6010 substrate material that will be used in this project. Both microstrip and slotline in this transition are 50Ω lines. In Figure 3.2(d) one can see the standard microstrip to slotline transition [21], which is not satisfactory because the VSWR is not particularly low and the usable bandwidth is not as large as one expects it to be. This non-optimum behaviour is due to the fact that, because of mechanical restrictions, the effective plane of the microstrip short circuit is not exactly at the slotline plane where it should be theoretically. Similarly, the slotline open circuit is not exactly beneath the microstrip. In the new design no dimension is extremely critical except the width of the lines that should give characteristic impedance equal to 50Ω at midband frequency. Referring to Figure 3.2(c) there is no direct coupling between ports 1 and 6. This can be explained qualitatively on the basis of field configurations for the microstrip (port 1) and the slotline (port 6) shown in Figure 3.3(a,b), where the E-field of microstrip has even symmetry while that of slotline has odd symmetry. Thus there is no net coupling. A similar situation

* RT/duroid 6010 is a ceramic/PTFE composite made by Rogers Corporation, Chandler, Arizona 85224.

Figure 3.2 (a), (b) & (c) Configuration of a Microstrip-Slotline Transition Using a Six-Port Junction
(d) Standard Microstrip-Slotline Transition [7]

holds for the magnetic field lines. The equivalent circuits as seen from ports 1 and 6 illustrated in Figure 3.3(c,d) [7] from which one can see that the 6-port is matched at port 1 and port 6 if ports 2-5 are terminated by matched loads. This depends on the characteristic impedances of the strip and slotlines all being the same, e.g., 50Ω , and if junction effects can be neglected.

considering now a signal incident at port 1 (Figure 3.2(a), 3.3(d)), it will be equally distributed into ports 2 through 5 (port 6 is decoupled). If these components are totally reflected from identical reactive terminations connected to ports 2 to 5 then the signal will be reflected back into port 1. Similarly, an input signal at port 6 (slot side) will also be equally transmitted into ports 2-5, but in phase opposition to ports 2 and 5 with respect to ports 3 and 4. Again, equal reflection coefficients at ports 2-5 will reflect the signals back into port 6. Therefore a reflection coefficient of $\exp(j\phi)$ at ports 2 and 5 and of $\exp(j\phi+180^\circ)$ at 3 and 4 will cause a perfect transmission of the input signal at port 1 into the output port 6. For the above conditions to hold, the electrical lengths of the microstrip and slot lines from the open or short circuits to the center of the junction should be equal, i.e.,

$$\beta_{\text{mstrip}} \ell_{\text{mstrip}} = \beta_{\text{slot}} \ell_{\text{slot}} = \theta \quad (3.5)$$

where β_{mstrip} and β_{slot} are the phase constants and ℓ_{mstrip} and ℓ_{slot} are line lengths for microstrips and slotlines respectively.

Figure 3.3 (a), (b) Coupling of Electromagnetic Waves From Microstrip to Slotline [7]
 (c), (d) Transmission Line Equivalent Circuits for Figure 3.2(c) When Viewed From Ports 6 and 1 respectively [7]

This transition has been reported to give a VSWR less than 1.22 over the entire 2-8 GHz band. Experimental results, that have been measured in this thesis, for this kind of structure, will be reported at the end of this chapter.

Figure 3.4(a) represents the remainder of the output of the device between the resonator and the output port. Box A represents the slotline-to-microstrip transition and box B is a matching network that can be used to transform the load impedance $Z_{out|f}$ to a 50Ω slotline. Here, a couple of different matching networks will be discussed and optimized results will be given.

3.1.3(b) Slotline stepped impedance transforming matching network

In Figure 3.4(b) one can see how this part of the circuit would generally be represented. In order to calculate the characteristic impedances Z_{01} , Z_{02} , Z_{03} of each section, the Butterworth maximally-flat response formulas can be used. In addition, tables due to Young [26] can be used to estimate the normalized impedances $\bar{Z}_{01}$, $\bar{Z}_{02}$, and $\bar{Z}_{03}$. The output impedance at BB' is 50Ω and the input at AA' can be taken as the mean value of $R_e(Z_{out|f})$. One should keep in mind that these are only "starting" values for an optimization process that will be carried out using a special CAD language for microwave networks called COMPACT [27]. In Appendix III one can see how a data file in COMPACT can be written.

A very brief description of the basic COMPACT functions will also be given. The variables to be optimized are six: Z_{01} , Z_{02} , Z_{03} , θ_{01} , θ_{02} , θ_{03} (characteristic impedances and electrical lengths at the midband output

Figure 3.4 (a) The Part of the Output of the F.D. Between the Resonator and the Output Port
 (b) The Matching Network B of Figure 3.4(a) Used to Transform the Load $Z_{out}|_f$ to a 50Ω Slotline

frequency, which is 3GHz) and are identified to COMPACT by negative signs. Optimization gave the results presented in Figure 3.5(a,b), in terms of VSWR, reflection coefficient and return loss. One can see that the maximum VSWR occurs at the middle of the band and is equal to 1.77. This network presents good matching properties especially at the upper end of the band.

3.1.3(c) Slotline stepped-impedance transformer using one $\lambda/8$ -section matching network

An interesting impedance matching network has been described by Steinbrecher [28]. This will be used to get the starting values of Z_{01} , θ_{01} , Z_{02} , θ_{02} for a matching network consisting of two lines Z_{01} , $\theta_{01} = \lambda/8$ and Z_{02} , $\theta_{02} = \lambda/4$ as shown in Figure 3.6(a). Using this matching circuit any load impedance can be transformed to a real impedance by a $\lambda/8$ transformer section, whose characteristic impedance is equal to the magnitude of the load impedance. Hence first of all $Z_{01} = |Z_L| = |Z_{out}|$ and

$$Z_{aa'} = \frac{R_{out}|f}{1 - \frac{X_{out}|f}{Z_{out}|f}}, \quad Z_{02} = \sqrt{Z_{aa'} Z_0} \quad (3.6)$$

These formulas give the following starting values:

$$\begin{aligned} Z_{01} &= 55\Omega & \theta_{01} &= 45^\circ \text{ at } 3\text{GHz} \\ Z_{02} &= 42.26\Omega & \theta_{02} &= 90^\circ \text{ at } 3\text{GHz} \end{aligned}$$

The optimization, through COMPACT, using these starting values gives the performance shown in Figure 3.6(b) where the maximum VSWRs occur at the first and the last frequency of the 2-4GHz band and are 1.69 and 1.58 respectively. This performance has been obtained for the following set

F (MHZ)	RHO (MAGN., ANGLE)		VSWR	RET L/G (DB)	Z (R+JX) OHM	
2000.000	.275	-62.0	1.76:1	-11.23	56.55	-29.65
2200.000	.195	-124.1	1.48:1	-14.22	38.29	-12.82
2400.000	.184	164.2	1.45:1	-14.72	34.84	3.61
2600.000	.223	105.5	1.57:1	-13.05	40.68	18.36
2800.000	.262	60.1	1.71:1	-11.64	57.69	28.11
3000.000	.280	20.9	1.78:1	-11.04	83.07	18.03
3200.000	.273	-15.9	1.75:1	-11.28	84.19	-13.61
3400.000	.238	-52.8	1.63:1	-12.46	61.38	-24.67
3600.000	.179	-92.7	1.43:1	-14.96	46.17	-17.01
3800.000	.104	-145.1	1.23:1	-19.64	41.84	-5.04
4000.000	.072	113.0	1.16:1	-22.85	46.86	6.25

(b)

Figure 3.5 (a) & (b) - Optimization Results in Terms of VSWR for an Output Circuit of the Form of Figure 3.4(b)

(a)

(b)

Figure 3.6 (a) Impedance-Matching Network Employing A $\lambda/8$ and a $\lambda/4$ Transformer Sections
 (b) Theoretical Performance in Terms of Output VSWR of the Structure in Figure 3.6 (a)

of values:

$$Z_{01} = 53.46\Omega, \theta_{01} = 29.06^\circ, Z_{02} = 40\Omega, \theta_{02} = 177.26^\circ$$

Hence we can see that with only two transformer sections one can get a performance as good as the 3-element matching circuit, although the bandwidth of the first matching circuit seems to be more extendable toward the upper frequency limit as one can easily see in Figure 3.5(a).

3.1.4 Fourth-Order Marchand Balun Structure

3.1.4(a) Introduction

In the kind of F.D. studied here a balanced slotline (resonator output) to unbalanced (50 Ω external world) transformation has to be done as far as the output part of the device is concerned. Hence a balun structure can be employed of 2nd, 3rd or 4th order. If in a balun structure there is only a series open-circuited stub and a parallel short-circuited stub this is a 2nd order balun. With one transformer added either in the input or the output the structure becomes a third order balun. Among the various structures that have been described (mainly third order) the most useful ones are these by Oltman [29] and Laughlin [30].

The Laughlin structure is the most interesting because it is a planar structure (microstrip circuitry). The position of the transformer depends on how large the input (or output) impedance is compared to the output (or input). For example Oltman writes that if there is a large balanced line impedance, it is definitely preferable to provide the impedance transformation in the balanced line.

Figure 3.7 The Fourth-Order Marchand Balun

- (a) Coaxial Structure
 - (b) Transmission Line Equivalent Circuit
 - (c) Equivalent Circuit Using Distributed Element.
- Notation (U.E.=unit element and represents the two transformer sections Z_1 and Z_4)

3.1.4(b) Fourth-Order Marchand Balun Planar Structure

Cloete [23-24] presents the design of 4th order coaxial baluns (transformers on both input and output) using graphs of element values Z_1, Z_2, Z_3, Z_4 . In Figure 3.7(a-c) one can see the form and the equivalent circuits of a 4th order Marchand balun. The advantage of this structure over the third-order balun is that for a given load resistance, a significant reduction in passband reflection coefficient can be obtained, depending on the required bandwidth. Taking into account both Figure 3.7 and the structure considered and measured by Houdart [25], the structure of Figure 3.8 can be considered as the planar form of the Marchand balun which is a Coplanar Waveguide (CPW) - to slotline transition, and can be used as the output of the F.D. The equivalent circuit of Figure 3.7(b) also holds for this planar balun. It consists of:

- (a) a slotline of characteristic impedance Z_4 and length $\lambda/4$ at the centre frequency. This is the section that goes directly after the resonator on the left of AA' denoted by Z_0 in Figure 3.1.
- (b) a slotline short-circuited parallel stub of characteristic impedance Z_3 and length $\lambda/4$ at the centre frequency.
- (c) a coplanar waveguide open-circuit series stub of characteristic impedance Z_2 and length $\lambda/4$ at the centre frequency.
- (d) a coplanar waveguide transmission line section of characteristic impedance Z_1 and length $\lambda/4$ at the centre frequency.
- (e) the output to the unbalanced 50Ω world in the form of a CPW section of characteristic impedance $Z_0=50\Omega$.

In order to obtain proper conditions for excitation of this balun, the two ground planes of the coplanar lines must be connected through low-impedance

Figure 3.8 A New Design for the Output Circuit Representing a 4th Order Marchand Balun in Planar Form

bonding wire on each side of the slotlines.

Before proceeding to the detailed design of the output circuit for a particular F.D., a brief presentation of CPW circuit design and its limitation will be given since CPW is used in the output circuit as an open-circuit series stub and transmission line portion.

3.1.4(c) Coplanar Waveguide Design Equations and Limitations

Coplanar waveguide was proposed by Wen [31]. As shown in Figure 3.9(a), it consists of a centre strip with two ground planes located parallel to and in the plane of the strip, (i.e. on the same surface of the dielectric slab). The electric and magnetic field configurations for a quasi-static approximation are shown in Figure 3.9(b). The quasi-static results for CPW due to Wen may be modified to give for the characteristic impedance Z_{ocp} and the effective dielectric constant ϵ_{re} :

$$Z_{ocp} = \frac{30 \pi}{\sqrt{\epsilon_{re}}} \cdot \frac{K'(k)}{K(k)} \quad (3.7)$$

$$\text{where } k = \frac{S}{S+2W}, \quad k' = \sqrt{1-k^2}$$

Accurate and simple expressions for the ratio K/K' are available in the literature [32]. These are reproduced below:

$$\frac{K(k)}{K'(k)} = \frac{1}{\pi} \cdot \ln \left[2 \left(\frac{1+\sqrt{k}}{1-\sqrt{k}} \right) \right] \quad \text{for } 0.707 \leq k \leq 1 \quad (3.9a)$$

$$\frac{K(k)}{K'(k)} = \frac{\pi}{\ln \left[2 \left(\frac{1+\sqrt{k'}}{1-\sqrt{k'}} \right) \right]} \quad \text{for } 0 \leq k \leq 0.707 \quad (3.9b)$$

Figure 3.9 (a) Coplanar Waveguide (CPW) Geometry [7]
 (b) Electric and Magnetic Field Distributions in CPW [7]

The numerical results of Davis et al [33] have been curve-fitted [7] to obtain the following closed form expression for ϵ_{re} :

$$\epsilon_{re} = \frac{\epsilon_r + 1}{2} [\tan h \{1.785 \log (h/w) + 1.75\} + \frac{kw}{h} \{0.04 - 0.7k + 0.01 (1 - 0.1\epsilon_r) (0.25 + k)\}] \quad (3.10)$$

According to Dupuis and Campbell [34] to attain a $\pm 10\%$ tolerance from the previous closed-form expressions it is necessary to employ a substrate thickness $h \geq 0.05"$ and an aspect ratio $k \geq 0.4$. For $h/w \geq 2$ the characteristic impedance Z_{ocp} will be within 5% of the value predicted by the ideal model (Equation 3.7-3.10). Since the substrate thickness in this project is $h = 0.025"$ a sensitivity analysis will be presented below, to evaluate the deviation of Z_{ocp} [7]:

The maximum change in the values of characteristic impedance may be written as:

$$\begin{aligned} \frac{|\Delta Z_0|_{\max}}{Z_0} &= \left| \frac{\Delta W}{W} S_W^0 \right| + \left| \frac{\Delta S}{S} S_S^0 \right| + \left| \frac{\Delta h}{h} S_h^0 \right| + \\ &+ \left| \frac{\Delta \epsilon_r}{\epsilon_r} S_{\epsilon_r}^0 \right| + \left| \frac{\Delta t}{t} S_t^0 \right| \end{aligned} \quad (3.11)$$

The sensitivity of $Z_0 = Z_{ocp}$ with respect to a parameter y may be evaluated from the sensitivities of Z_0^a and ϵ_{re} from:

$$S_y^0 = S_y^a - \frac{1}{2} S_y^{\epsilon_{re}} \quad (3.12)$$

$$\text{where } Z_0^a = Z_0 \sqrt{\epsilon_{re}} \quad (3.13)$$

is the characteristic impedance a coplanar line with air as dielectric.

Expressions for sensitivities of the characteristics of CPW (Z_{ocp}^{α} and ϵ_{re}) with respect to various parameters (w , s , h , ϵ_r and t) can be calculated using the closed form expressions for Z_{ocp}^{α} and ϵ_{re} given by Equations 3.7-3.10 and the definition of sensitivity. These sensitivities of characteristic impedance are given in Figure 3.10(a) for $\epsilon_r=10.0$, $h=0.025"$, $h/w=3.0$, $h/w=1.0$. Since Duroid 6010 has the same characteristics (except that $\epsilon_r=10.5$, which will have a rather slight effect on the sensitivity values) the curves of Figure 3.10(a) can be used to calculate $\frac{|\Delta Z_o|_{max}}{Z_o}$.

For Duroid 6010 we have:

$$\left. \begin{aligned} \epsilon_r &= 10.5 \pm 0.25 \rightarrow \Delta\epsilon_r = \pm 0.25 \\ h &= 0.025" \pm 0.001" \rightarrow \Delta h = \pm 0.001" \\ \Delta w &= \pm 0.0001", \Delta s = \pm 0.0001" \end{aligned} \right\} \quad (3.14)$$

The worst case $h/w=1.0$ will be considered here. From Figure 3.10(a) one can get for $k=0.4$:

$$|S_{\epsilon_r}^{Z_{ocp}}| = 0.45, |S_w^{Z_{ocp}}| = 0.32, |S_h^{Z_{ocp}}| = 0.13, |S_s^{Z_{ocp}}| = 0.22 \quad (3.15)$$

The effect of strip thickness on the CPW characteristics is very small and therefore will not be included here.

$$\text{Hence } \left| \frac{\Delta t}{t} S_t^{Z_o} \right| \rightarrow 0.$$

From Equations (3.11) (3.12), (3.14) and (3.15):

$$\begin{aligned} \frac{|\Delta Z_o|_{max}}{Z_o} &= \frac{0.0001}{0.025} \times 0.32 + \frac{0.0001}{0.033} \times 0.22 + \\ &+ \frac{0.001}{0.025} \times 0.13 + \frac{0.25}{10.5} \times 0.45 = 0.01786. \end{aligned}$$

(a)

(b)

Figure 3.10 (a) Sensitivities of Characteristic Impedance of CPW With Respect to Various Parameters [7]
 (b) Comparison Between Theoretical and Experimental Values of Impedance for CPW [7]

This corresponds to a 2% deviation. This is in agreement with Figure 3.10(b) which compares theoretical and experimental values of impedance. Then

$$VSWR_{\max} = [1 - 0.01786]^{-1} \approx 1.02$$

Hence one can see that this will have only a very slight effect on the total VSWR at the output (less than 5%). From Figure 3.10(b) one can see as well that in order to have no more than 10% deviation in calculated Z_{ocp} from the experimental value, impedances between 48Ω and 90Ω should be used in CPW designs.

3.1.4(d) Output Circuit Design Using A 4th Order Planar Marchand Balun Structure

Taking into account the equivalent circuit of Figure 3.7(b) for the structure of Figure 3.8, the circuit to be optimized using COMPACT is that of Figure 3.11. Two transformer slotline sections are used before the Marchand balun. The reason for this is as follows: According to Cloete [23] R in Figure 3.7(b) represents the balanced load. In this case it is a mean value of the real part of the two varactors in series which is $R_e(Z_{\text{out}}|_f)$ and it is less than 30Ω . The values of Z_1 , Z_2 , Z_3 , and Z_4 given in Table 3.2 were calculated [24] for various values of R and a bandwidth ratio equal to 10. These element values can be calculated using the exact non-redundant method for the synthesis of commensurate-length distributed networks described by Horton and Wenzel [35], and the model of Figure 3.7(c) for the equivalent circuit of a 4th order Marchand balun using distributed element notation.

Figure 3.11 Topology of the Output Circuit to be Optimized Using COMPACT

Hence it is not possible to match a resistance less than 30Ω to 50Ω with a 4th order Marchand balun directly because according to Table 3.2 one cannot match R less than 54.65Ω . What can be done is to transform $R_e(Z_{out}|f)$ using two transformer sections (Z_5, Z_6 in Figure 3.11) to a value such as to get reasonable values for Z_1, Z_2, Z_3 and Z_4 that comes after the transformer section. Here we have chosen $R=68.21\Omega$, a value that gives more or less reasonable values for Z_1, Z_3 and Z_4 but not for Z_2 ($=11.29\Omega$ from Table 3.2). One should not forget that Z_1 and Z_2 are CPW characteristic impedances and Z_3 and Z_4 are slotline characteristic impedances. The COMPACT file (without the impedance data) is shown in Figure 3.12(a) where the resonator is represented by the following line (see Appendix III for explanation of the notation):

TRL HM SE 90 7.19° 3000.

The optimization process gives the performance of Figure 3.12(b). It can be seen that the maximum VSWR is 1.56 which is much better than the other output circuits presented in this chapter. The element values for this performance are the following:

$$\begin{array}{lll}
 Z_1 = 75.56\Omega & Z_2 = 81.77\Omega & Z_3 = 160.18\Omega \\
 \theta_1 = 93.42^\circ & \theta_2 = 110.40^\circ & \theta_3 = 112.71^\circ \\
 Z_4 = 154.56\Omega & Z_5 = 71.39\Omega & Z_6 = 48\Omega \\
 \theta_4 = 188.28^\circ & \theta_5 = 88.40^\circ & \theta_6 = 135.72^\circ
 \end{array}$$

All these impedance values are feasible to make in the selected transmission-line media.

ELEMENT VALUES FOR FOURTH ORDER MARCHAND BALUN
AS COMPUTED BY THE SYNTHESIS PROGRAM

FOURTH ORDER MARCHAND BALUN WITH IN AND OUTPUT TRANSFORMERS

BANDWIDTH RATIO = 10

RHO(DB)	Z_1	Z_2	Z_1/Z_2	Z_2	R
-35.00	51.58	5.35	255.44	52.97	54.65
50.00	50.00				
-34.00	51.77	5.68	242.96	53.32	55.20
50.00	50.00				
-33.00	51.97	6.03	231.29	53.70	55.82
50.00	50.00				
-32.00	52.21	6.41	220.37	54.12	56.51
50.00	50.00				
-31.00	52.46	6.81	210.17	54.59	57.28
50.00	50.00				
-30.00	52.75	7.25	200.66	55.12	58.15
50.00	50.00				
-29.00	53.00	7.71	191.81	55.71	59.13
50.00	50.00				
-28.00	53.44	8.20	183.58	56.36	60.23
50.00	50.00				
-27.00	53.84	8.73	175.95	57.08	61.47
50.00	50.00				
-26.00	54.29	9.30	168.90	57.89	62.86
50.00	50.00				
-25.00	54.79	9.92	162.40	58.79	64.43
50.00	50.00				
-24.00	55.36	10.58	156.44	59.80	66.20
50.00	50.00				
-23.00	55.99	11.29	151.00	60.92	68.21
50.00	50.00				
-22.00	56.69	12.06	146.06	62.17	70.49
50.00	50.00				
-21.00	57.49	12.90	141.62	63.56	73.08
50.00	50.00				
-20.00	58.38	13.81	137.67	65.13	76.04
50.00	50.00				
-19.00	59.39	14.80	134.20	66.88	79.43
50.00	50.00				
-18.00	60.52	15.88	131.21	68.84	83.33
50.00	50.00				
-17.00	61.80	17.06	128.72	71.05	87.82
50.00	50.00				
-16.00	63.26	18.35	126.72	73.54	93.04
50.00	50.00				
-15.00	64.91	19.79	125.25	76.36	99.12
50.00	50.00				
-14.00	66.80	21.37	124.32	79.55	106.27
50.00	50.00				
-13.00	68.96	23.14	123.98	83.20	114.75
50.00	50.00				
-12.00	71.46	25.12	124.29	87.37	124.88
50.00	50.00				
-11.00	74.37	27.36	125.32	92.19	137.14
50.00	50.00				
-10.00	77.79	29.91	127.18	97.81	152.16
50.00	50.00				

Table 3.2 Element Values For Fourth Order Marchand Balun
As Computed By The Synthesis Program [24]

TRL AA SE 75.56 93.42 3000

L

QST BB SE 81.77 110.40 3000
 SST CC PA 160.18 112.71 3000
 TRL DD SE 154.56 188.28 3000
 TRL EE SE 71.39 88.40 3000
 TRL FF SE 42 135.72 3000
 IMP GG SE
 TRL HH SE 90 7.19 3000
 CAX AA HH
 PRI AA IR 50 0
 PLO AA IR 50 0
 END
 2000 4000 200
 END

VSWR

Figure 3.12 (a) COMPACT File for the Marchand Balun Structure
 (b) Optimized Results in Terms of VSWR for (a)

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3.2 Experimental Results

3.2.1 Schiek's Transition

A circuit with two microstrip-to-slotline transitions was designed in a manner similar to that of Figure 3.2(b). An Al_2O_3 substrate was used with $\epsilon_r=10.0$, $h=0.025$ ". Measurements taken using an Automatic Network Analyser (ANA) system, are presented in Table 3.3(a).

3.2.2 4th Order Marchand Balun

A double slotline-to-CPW transition was made according to Figure 3.8 using the same substrate material (Al_2O_3) with the same specifications. Low-impedance bonding wires connected each side of the slotlines (ground planes of the CPW stubs and lines) in order to get proper conditions for excitation for the two baluns in series.

The measurements taken using the ANA system are listed in Table 3.3(b).

3.2.3 Discussion

Schiek's transition performance was more or less as expected. The high reflection at 2.00GHz is due to the finite diameter of the slot open-circuit area being rather small for this frequency, as Schieck has reported also. The reflection coefficients of the Marchand balun are slightly larger than expected but are reasonable. Although the performance of Schieck's transition is better than that of the Marchand balun, the balun is preferable as an output for the F.D. because it combines both a slotline-to-CPW transition and a successful matching circuit.

$f(\text{MHz})$	$S_{11}(\text{DB})$	ANG. (DEG.)
2000	5.3	-60°
2250	7.8	-81°
2500	11.5	-87°
2750	12.3	-107°
3000	19.7	-147°
3250	21.5	-126°
3500	31.5	181°
3750	22.9	-119°
4000	26.6	-172°
4250	21.3	-161°
4500	19.5	129°
4750	21.1	121°
5000	17.8	83°

(a)

2000	3.4	9°
2200	8.7	-30°
2400	10.7	-40°
2600	13.2	-88°
2800	15.9	-118°
3000	16.5	-169°
3200	16.4	-179°
3400	10.9	133°
3600	15.1	105°
3800	10.1	51°
4000	11.4	-14°
4200	15.5	138°
4400	10.3	147°

(b)

Table 3.3 Experimental Results From (a) Schiek's Transition, (b) 4th Order Marchand Balun

If Schieck's transition is to be used a separate matching circuit is required and should be designed as described previously in this chapter. Of course, this fact does not preclude the use of Schieck's transition as one of the best forms for the output of the F.D. (after Marchand's balun).

CHAPTER 4

FREQUENCY DIVIDER DESIGN AND PERFORMANCE USING A SLOTLINE-TO-CPW TRANSITION IN THE OUTPUT CIRCUIT

4.1 Introduction

In this chapter the design of some devices using COMPACT will be presented and their experimental performance will be given in terms of input power threshold and output power over the entire band of operation. The effect of changing the position of the diodes on the double-sided M.I.C. is also discussed as well as the effect of tuning either the input or the output matching circuits.

4.2 C.A.D. Of Input and Output Matching Circuits

4.2.1 Input Matching Circuits

The purpose of the input circuit in these designs is to use micro-strip circuitry to match the 50Ω external world to the pumped "input impedance" that is presented by the two varactors in parallel in the input circuit. This impedance is given by Equation (2.50) in Chapter 2. It can be easily seen from Figure 3.1(a) why the two varactors are connected in parallel in the input. The input circuits of the devices consist of suitable combinations of transmission line (t.l.) elements (modeled as TRL in COMPACT) and open-circuit parallel stubs (modelled as OST).

Figure 4.1 Input Microstrip Pattern of the First Design

(a) First Design

Figure 4.1 shows the input matching circuit microstrip pattern as optimized by COMPACT for a bias voltage $V_D=0$ volts. It consists of three t.l parts and two open circuited stubs. The second stub is off-axis because we want to avoid perturbing the slotline beneath. The small circles at the end of the pattern identify the position at which the diodes are to be placed. Hence narrow copper shims will be needed to connect the diodes to the microstrip input. It has been experimentally found during small-signal diode impedance measurements that these narrow copper shims connecting the diode to the microstrip have a considerable inductance that can be modelled as a part of a microstrip transmission line whose parameters (ϵ_r, h) are similar to these of the substrate used. Hence if the copper shim is narrow enough (0.016"-0.010") its reactance can be expressed by the following equation:

$$X = Z_0 \tan \beta l_{cs} = \omega L_A \quad (4.1)$$

where Z_0 = characteristic impedance of the lead (depends on its width)

β = phase constant as if the lead was a part of the microstrip circuit with the same ϵ_r, h .

l_{cs} = length of the lead.

The two 150° moon configurations connected by $g/4$ high characteristic impedance sections (120 Ω) comprise the bias circuit. The R.F. power coming into the device "sees" this bias circuit configuration as an open circuit. One of the local minima calculated by COMPACT gives for the input circuit configuration of Figure 4.1 the performance shown in Figure 4.2 in terms of input VSWR versus frequency. This is not the best result obtained using COMPACT because a compromise has been made restricting strip widths to $\lambda g/4$ maximum. Problems that may arise for strip widths

F (MHZ)	RHO (MAGN. - ANGLE)	VSWR	RET L/G (DB)
3600.000	.350 -103.4	2.08:1	-9.11
4000.000	.236 -162.6	1.62:1	-12.53
4400.000	.183 117.9	1.45:1	-14.75
4800.000	.215 43.6	1.55:1	-13.35
5200.000	.255 -13.6	1.69:1	-11.86
5600.000	.266 -65.9	1.73:1	-11.50
6000.000	.247 -121.8	1.66:1	-12.13
6400.000	.224 171.9	1.58:1	-12.99
6800.000	.237 97.5	1.62:1	-12.50
7200.000	.285 28.5	1.80:1	-10.91
7600.000	.312 -35.2	1.91:1	-10.12
8000.000	.255 -111.0	1.68:1	-11.88
8400.000	.283 87.0	1.79:1	-10.95

Figure 4.2 Theoretical Performance in Terms of VSWR
for the First Input Circuit

near $\lambda_g/2$ will be mentioned in section 4.2.1(b) and discussed in Appendix IV.

It must be mentioned here that the COMPACT optimization procedure, which was used to obtain satisfactory values of input matching, always tended to cause a very rapid increase in the width of the microstrip t.l. section close to the diodes. This occurred whatever the starting microstrip pattern and element values were.

(b) Second Design

In Figure 4.3 one can see the input matching microstrip circuit as optimized by COMPACT for the same bias voltage $V_D=0V$. In this case no restrictions to the widths of the TRL (transmission line) sections have been set. The result is to get a much better performance than the previous design (Figure 4.4) in terms of input VSWR. Here $VSWR \leq 1.31$ over the entire input frequency band.

Table 4.1 represents the dimensions of the input circuits of the first and second designs. This table shows that in order to get this improved performance, widths of 0.203", 0.360" and 0.160" should be used. As proposed in Appendix IV very narrow slots ($w \approx 0.002"$) along these wide transmission line sections can be used to avoid transverse resonances. These slots can be seen in Figure 4.3 as well. The same bias configuration is used here as in the first design.

Figure 4.3 Input Microstrip Pattern of the Second Design

(MHZ)	RHD(MAGN.<ANGLE)		VSWR	RET L/D (DB)	Z(R+JX)OHM	
3600.000	.128	-3.4	1.29:1	-17.88	64.59	-1.01
3800.000	.012	-30.1	1.02:1	-38.18	51.07	-.63
4000.000	.069	140.7	1.15:1	-23.17	44.74	3.95
4200.000	.117	121.4	1.26:1	-18.65	43.44	8.7E
4400.000	.135	102.4	1.31:1	-17.40	45.62	12.2E
4600.000	.130	81.5	1.30:1	-17.75	50.25	13.10
4800.000	.107	57.2	1.24:1	-19.38	55.20	10.09
5000.000	.078	24.5	1.17:1	-22.19	57.49	3.72
5200.000	.057	-27.9	1.12:1	-24.85	55.24	-2.97
5400.000	.067	-86.4	1.14:1	-23.47	49.97	-6.72
5600.000	.093	-125.2	1.20:1	-20.65	44.43	-6.80
5800.000	.116	-152.1	1.26:1	-18.75	40.52	-4.44
6000.000	.128	-175.2	1.29:1	-17.88	38.71	-.83
6200.000	.126	163.2	1.29:1	-17.97	39.11	2.90
6400.000	.112	140.5	1.25:1	-19.04	41.67	5.99
6600.000	.086	113.5	1.19:1	-21.30	46.12	7.34
6800.000	.057	75.2	1.12:1	-24.87	51.16	5.67
7000.000	.046	9.5	1.10:1	-26.83	54.70	.82
7200.000	.066	-47.3	1.14:1	-23.61	54.42	-5.30
7400.000	.092	-79.9	1.20:1	-20.76	50.78	-9.24
7600.000	.107	-104.9	1.24:1	-19.38	46.33	-9.73
7800.000	.102	-127.7	1.23:1	-19.84	43.59	-7.10
8000.000	.071	-152.6	1.15:1	-23.02	44.01	-2.87
8200.000	.016	129.2	1.03:1	-35.97	48.99	1.21
8400.000	.095	7.3	1.21:1	-20.45	60.38	1.46

Figure 4.4 Theoretical Performance in Terms of VSWR of the Second Input Circuit

TABLE 4.1

FIRST DESIGN

(1) TRL AA MS:	$w_1 = 19.98$ mils	$\theta_1 = 130.16^\circ$
(2) TRL BB MS:	$w_2 = 38.04$ mils	$\theta_2 = 84.19^\circ$
(3) OST CC PA:	$w_3 = 4.51$ mils	$\theta_3 = 56.54^\circ$
(4) TRL DD MS:	$w_4 = 35.30$ mils	$\theta_4 = 32.49^\circ$
(5) TRL EE MS:	$w_5 = 180$ mils	$\theta_5 = 42.85^\circ$
(6) OST FF PA:	$w_6 = 26.87$ mils	$\theta_6 = 39.49^\circ$

SECOND DESIGN

(1) TRL AA MS:	$w_1 = 47.92$ mils	$\theta_1 = 82.3^\circ$
(2) TRL BB MS:	$w_2 = 131.3$ mils	$\theta_2 = 55.5^\circ$
(3) TRL CC MS:	$w_3 = 202.7$ mils	$\theta_3 = 52.40^\circ$
(4) TRL DD MS:	$w_4 = 360$ mils	$\theta_4 = 166.7^\circ$
(5) OST EE PA:	$w_5 = 26.52$ mils	$\theta_5 = 53.45^\circ$
(6) TRL FF MS:	$w_6 = 160$ mils	$\theta_6 = 12.15^\circ$

Table 4.1 Dimensions of the Input Circuits of the First and Second Designs

4.2.2 Output Matching Circuit

An output matching circuit has been designed for both designs because in the output design there were no problems due to physical or electrical limitations such as those which appeared in the design of the input matching circuits.

A 4th order Marchand Balun output matching network has been chosen because of its good theoretical and experimental performance, as presented in Chapter 3. A procedure similar to that of section 3.1.4(d) is followed in order to design the output circuit. This takes into account the impedance restrictions due to physical limitations where slotline and CPW transmission lines are used. A photomask and a sketch of the output circuit are given in Figure 4.5(a) and (b). As shown, this circuit consists of 7 parts:

- (0) The 50 Ω CPW output section.
- (1) The series CPW t.l. section.
- (2) The CPW open-circuited series stub (OST).
- (3) The slotline short-circuited parallel stub (SST).
- (4) A slot transmission line section.
- (5) Another slotline section of different characteristic impedance.
- (6) The slotline resonator located between the two diodes.

In Table 4.2 the dimensions of the output circuit are given. The theoretical performance of the circuit as calculated by COMPACT in terms of output VSWR is given in Figure 4.6. The band of interest is from 1.70 GHz to 4.3 GHz.

Figure 4.5 Output Circuit Pattern: Two-Dimensional Fourth-Order Marchand Balun:

- (a) Metallization Pattern
- (b) Identification of Network Elements

MHZ	RHO(MAGN.<ANGLE>)	VSWR	RET L/G (DB)	Z(R+JX)OHM
1600.000	.226	1.58:1	-12.92	43.18
1800.000	.201	1.50:1	-13.96	63.57
2000.000	.275	1.76:1	-11.22	35.69
2200.000	.261	1.71:1	-11.68	29.39
2400.000	.225	1.58:1	-12.95	37.68
2600.000	.234	1.61:1	-12.62	65.88
2800.000	.266	1.73:1	-11.49	82.14
3000.000	.276	1.76:1	-11.20	50.49
3200.000	.251	1.67:1	-11.99	34.04
3400.000	.215	1.55:1	-13.34	32.49
3600.000	.202	1.51:1	-13.90	43.85
3800.000	.209	1.53:1	-13.60	69.80
4000.000	.193	1.48:1	-14.27	68.19
4200.000	.127	1.29:1	-17.92	45.12
4400.000	.155	1.37:1	-16.21	42.63
				20.44
				-18.67
				-19.46
				-2.03
				15.84
				22.61
				-14.92
				-28.80
				-14.30
				3.00
				18.29
				15.64
				-14.12
				-11.14
				12.44

Figure 4.6 Theoretical Performance in Terms of VSWR for the Output Circuit

TABLE 4.2

Type of Element	Ch. Impedance (Ω)	Electrical Length (Degr.)	Phase Length (mils)	Phase Width (mils)
50 Ω (CPW) (Z_0)	50.03			$S_d = 19.56$ $d_0 = 36.23$
TRL AA (CPW) (Z_1, θ_1)	60.0	67.83°	318.3	$s_1 = 13.61$ $d_1 = 36.23$
OST BB (CPW) (Z_2, θ_2) (Open circuit stub)	60.05	80.58°	378.1	$s_2 = 13.61$ $d_2 = 36.23$
SST CC (SLOT) (Z_3, θ_3) (short circuit stub)	123.34	99.08°	738.0	$w_3 = 72.00$
TRL DD (SLOT) (Z_4, θ_4)	65.78	56.46°	335.2	$w_4 = 7.5$
TRL EE (SLOT) (Z_5, θ_5)	49.0	215.64°	1168.2	$w_5 = 2.0$
TRL GG (SLOT RESONATOR) (Z_6, θ_6)	90	7.19°	48.6	$w_6 = 25.0$

Table 4.2 Dimensions of the Output Circuit

The maximum VSWR was 1.76 and it can be seen that the useful output bandwidth can be increased further (especially towards the upper edge of the band). This fact demonstrates the potential of this kind of output circuit: it has both good transition and output matching properties. Finally, it should be mentioned that the length of the resonator, as seen in the photomask, was made at least 3 times larger than the calculated value in order to be able to tune the device at the proper bandwidth.

4.3 Experimental Results

After soldering the varactors, the dc blocking capacitor, the low impedance wires (in the output circuit) and the input and output SMA connectors, the device can be tested using a suitable set up such as the arrangement shown in Figure 4.7(a). Two different plug-ins are used to cover a band in excess of 3.4 to 8.0 GHz. A minimum output power of about +16 dBm across the band can be obtained using an amplifier. The list of the instruments used in this set up is given below:

- A: HP 8620C sweep oscillator
- B: Amplica Inc., 719CSL amplifier
- C: Narda Microline 792 FM precision attenuator
- D: Narda Microline 3044B 10-dB precision directional coupler (3.7-8.36 Hz)
- E: HP432A Power Meter
- F: Aertech ASC-4080 circulator (4GHz-8GHz) (or ASC-2040 2.0-4.0 GHz)
- G: Device under test
- H: AIL-707 spectrum analyzer (1MHz-12GHz)
- I: HP5342A Microwave frequency counter-power meter

Figure 4.7 (a) The Test Set Up Used to Measure the Performance of the Devices
 (b) Possible Diode Positions With Respect to the Slotline Resonator

The F.D. is a threshold device, which means that it is sensitive to input power level, P_{in} . This can be measured by a power meter after it has been calibrated accurately. Before taking any measurements the tuning should be done in order to obtain the best performance.

Tuning can be accomplished by:

- (i) Adjustment of the slotline resonator length (on back of the substrate)
- (ii) Addition of copper-shim tuning elements of various widths to the input circuitry (microstrip at front of the substrate)

The length of the resonator can be adjusted by pressing a small piece of copper shim against the resonant slot until a position is found where the high frequency end of the $f_{in}/2$ output band is maximized. After that the short-circuiting shim should be soldered in place. The three possible positions of the diodes with respect to the resonator can be seen in Figure 4.7(b). Next, the input microstrip matching circuit should be tuned by pressing small flat (wide or narrow) pieces of copper shim against it. Although this does not appreciably affect the frequency characteristic the resulting output power could be more than twice the value obtained when the tuning of the input circuit is not tuned.

In Figures 4.8 to 4.17 the performance of the two designs presented in part 4.2 can be seen for $V_D=0V$. There are three kinds of diagrams. The frequency characteristic, which is a "map" on the (f_{in}, P_{in}) plane, shows the region within which frequency division by two takes place. P_{in} represents the threshold power that is needed by the device to operate as a frequency halver. The second kind of diagram represents output power P_{out} versus frequency f_{in} , when a constant power is applied

to the input of the device. The third type of diagram shows $P_{in}-P_{out}$ transfer functions for constant values of input frequency.

In Figures 4.8-4.14 the performance of the first design can be seen while in Figures 4.15-4.17 measurements for the second design have been plotted. In all cases the first kind of tuning mentioned above (adjustment of the length of the resonator) has first been done before taking the measurements.

(a) First Design

Figures 4.8 and 4.9 show the performance of the first design with the diodes in position 3 (See Figure 4.7(b)). The maximum threshold power level P_{th} is about +16.5 dBm while the minimum value is close to +4.8 dBm. The useful bandwidth is from 3.4 GHz up to 7.0 GHz. The reason why no halving has been taken above that frequency is given below: The tuning of the resonator by pressing a copper shim against the slot does not "work" properly above 7.2 GHz because the suitable "effective" resonator length that gives a small signal resonance above that frequency is not easily achievable. This is due to parasitic inductances of the shortening copper shim that makes the length of the resonator to be larger than that desired. According to the calculations this should be about 7.2^0 at 3.00 GHz. Hence, the resonator should be etched such that its length corresponds to the small signal resonance at the higher desired frequency. One can observe that the frequency characteristic has the theoretically expected shape (see section 2.2). There is a dip of the threshold input power near the upper edge of the band and after that a very rapid increase takes place. The output power of this device (Figure 4.1) is not large enough (varying

Figure 4.8 Frequency Characteristic of the First Design: No Tuning Shims in the Input Circuit, Diodes at Position 3

Figure 4.9 Output Power of the First Design: No Tuning Shims in the Input Circuit, Diodes at Position 3, $P_{in} = +17$ dBm

between 3 dBm and -13 dBm) because of shortcomings of the input matching network as will be seen later. After soldering in place a rather narrow tuning copper shim at the input microstrip placed close to the diodes, the output power is as given in Figure 4.10. Here P_{out} is greater than -5 dBm over the entire band of operation. Using wider copper tuning shims soldered in place on the input microstrip adjacent to the varactors, one can obtain an even larger output power.

This can be seen in Figure 4.12 for a shim 450-500 mils wide. In Figure 4.11 the corresponding frequency characteristic is shown. This leads us to think that the agreement between, the tendency of the COMPACT optimization procedure to generate wide input microstrip sections adjacent to the diodes, and the experimental results reported here is profound.

Generally, the output spectrum is quite clear, except in a range between 4.3 GHz and 4.5 GHz where the output splits into two frequencies close to the expected output frequency. It was found that this can be reduced to a frequency range of less than 100 MHz if the d.c. 5.6 pF blocking capacitor is replaced by another one (33 pF). The corresponding frequency characteristic and the output power vs. frequency are shown in Figures 4.13 and 4.14 respectively.

(b) Second Design

In Figures 4.15, 4.16 and 4.17 the frequency characteristic, the output power vs. frequency and the (P_{in}, P_{out}) transfer functions for the second device can be seen. In this case the diodes are placed at position (1) (see Figure 4.7(b)).

Figure 4.10 Output Power vs. Frequency of the First Design: Narrow Shims in the Input Circuit, Diodes at Position 3, $P_{in} = +16.5$ dBm

Figure 4.11 Frequency Characteristic of the First Design: Wide Tuning Shim in the Input Circuit, Diodes at Position 3

Figure 4.12 Output Power vs. Frequency of the First Design: Wide Tuning Shim in the Input Circuit, Diodes at Position 3, $P_{in} = 16\text{dBm}$

Figure 4.13 Frequency Characteristic of the First Design: Wide Tuning Shim in the Input, Diodes at Position 3, dc Blocking Capacitance = 33pF

Figure 4.14 Output Power vs. Frequency of the First Design: Wide Tuning Shim at the Input, Diodes at Position 3, dc Blocking Capacitance = 33pF

Figure 4.15 Frequency Characteristic of the Second Design: No Tuning Shlm, Diodes at Position 1

Figure 4.16 Output Power vs. Frequency for the Second Design: No Tuning Shim, Diodes at Position 1, $P_{in} = 17$ dBm

Figure 4.17 $P_{in} - P_{out}$ Transfer Functions for the Second Design

The output power is quite high without any copper tuning shim in the input microstrip circuit because, according to the calculations of this optimized structure, the input VSWR is less than 1.31 (the best that could be achieved for this type of diode).

Figures 4.18 and 4.19 are photographs of the output signal spectra for four different input frequencies. Figure 4.20 is a photograph of the output spectrum during a sweep frequency measurement from 5.0 to 7.0 GHz using an ALC (Automatic Level Control) loop in the measuring system.

4.4 Discussion

The agreement between the experimental results and the performance calculated by using COMPACT leads us to the conclusion that a good design can be made using theoretical values for Z_{in} , Z_{out} and a suitable COMPACT optimization procedure.

The high output power obtained by suitable tuning of the input circuit demonstrates the ability of the chosen output circuit not only to provide good matching to a frequency-variable load for a bandwidth of more than one octave but also to give good slotline-to-coaxial transition properties. Proper CPW excitation is very important if a clear, spurious-free output signal is to be obtained. This means that the two low-impedance wires connecting the edges of the slotline stub and the CPW output should be as short and as close to the surface of the structure as possible, resulting in a well-grounded CPW output structure. This output circuit gives a quite low feed-through signal which is about 10 dB less than the power of the output signal over almost all the useful band.

2.0 GHz

2.50 GHz

Figure 4.18 Output Signal Spectra for (a) $f_{in} = 4.0$ GHz,
(b) $f_{in} = 5.00$ GHz

Spectrum Analyzer Settings:

Sweep = 1MHz/cm, Sweep Time = 3msec IF.BW.→AUTO

Amplitude Range = 10dB/cm, IF Attenuation = 20dB

RF Attenuation = 0dB

3 GHz

3.5 GHz

Figure 4.19 Output Signal Spectra for (a) $f_{in}=6.0$ GHz
(b) $f_{in}=7.0$ GHz

Spectrum Analyzer Settings:

Sweep = 1MHz/cm, Sweep Time = 3msec, IF BW.→AUTO

Amplitude Range = 10dB/cm, IF Attenuation = 20dB

RF Attenuation = 0dB

Figure 4.20 Output Spectrum for a Sweep Frequency
Measurement Using an ALC Loop (5.0-7.0 GHz)
Horizontal Scale: 200 MHz/cm.
Vertical Scale: 5dB/cm.

Finally, the position of the diodes with respect to the input and output circuits dramatically affects the performance of the device especially as far as the bandwidth of operation is concerned. The diodes should be placed close together so that the subharmonic current path is as short as possible (large lengths in these frequencies usually tend to reduce the broadband behaviour of a device). This has been observed in this thesis when the diodes had been set at position (2) (see Figure 4.7(b)) and the maximum output frequency was about 6.0 GHz.

CHAPTER 5

LARGE SIGNAL INPUT AND OUTPUT
LOAD-PULL IMPEDANCE MEASUREMENTS

5.1 Introduction

In this chapter a method described by Mazunder [37] will be used to measure the large-signal input and output impedances presented at the input and output ports of the halver and also at the plane where the varactor diodes are located.

First Mazunder's method will be presented. Then it will be used to measure impedances versus both frequency and input power for one of the devices designed and discussed in the fourth chapter. Finally, the effectiveness of this method as applied to F.D. measurements will be discussed.

5.2 A Load Pull Method for Measuring Impedances of Non-Linear 2-Ports

Generally an active two-port can be characterized at a specified power level, and frequency by large-signal S-parameters (see Figure 5.1(a)).

$$b_1 = S_{11} a_1 + S_{12} a_2 \quad (5.1)$$

$$b_2 = S_{21} a_1 + S_{22} a_2 \quad (5.2)$$

From these equations one can obtain:

Figure 5.1 (a) Definition of S-matrix for Non-linear Two Port
 (b) Circular Loci in b_i/a_j Plane as a Function of a_2/a_1

$$S_{11} = \left. \frac{b_1}{a_1} \right|_{a_2=0}, \quad S_{12} = \left. \frac{b_1}{a_2} \right|_{a_1=0} \quad (5.3)$$

$$S_{21} = \left. \frac{b_2}{a_1} \right|_{a_2=0}, \quad S_{22} = \left. \frac{b_2}{a_2} \right|_{a_1=0}$$

However, these relations cannot be applied here because the parameters S_{12} and S_{22} of the two combined diodes cannot be measured since according to the definition of S-parameters, the signal has to be applied at the output port, the input port being terminated ($a_1=0$) by the characteristic impedance. If we were to attempt to do this here the input drive power of the frequency halver would be removed and so the voltages and currents flowing in the two diodes would be completely different from those of the device operating as a halver. This happens because, according to theory (see Chapter 2) and measurement (see Chapter 4) the F.D. is a limit device and a suitable threshold input power must be established in order to operate in the halving mode. A similar problem was encountered by Mazumder [37] for a transistor amplifier under class C operating conditions.

Here the two diodes play the role of the nonlinear element instead of the transistor. If the measurements are made by simultaneously applying the two inputs a_1 and a_2 , there is no such problem because a suitable power level can be injected (by adjusting $|a_1|$) in order for the device to operate as a halver. Now (5.1), and (5.2) can be written in the following forms:

$$\frac{b_1}{a_1} = S_{11} + S_{12} \frac{a_2}{a_1} \quad (5.4)$$

$$\frac{b_1}{a_2} = S_{11} \frac{a_1}{a_2} + S_{12} \quad (5.5)$$

$$\frac{b_2}{a_1} = S_{21} + S_{22} \frac{a_2}{a_1} \quad (5.6)$$

$$\frac{b_2}{a_2} = S_{21} \frac{a_1}{a_2} + S_{22} \quad (5.7)$$

Hence if $|a_1|$ and $|a_2|$ are constant, then each of $\frac{b_i}{a_j}$ ($i, j=1, 2$) generates a circle in the corresponding plane as a function of the phase angle between a_2 and a_1 as shown in Figure 5.1(b) [38]. One can also see from Figure 5.1(b) that the center of the circular locus of $\frac{b_i}{a_j}$ corresponds to the S -parameter S_{ij} .

The quantities $\frac{b_i}{a_j}$ can be obtained from reflection or transmission measurements made with a Network Analyzer. This means that the $\frac{b_i}{a_j}$ locus can be taken as a function of the phase angle between a_2 and a_1 , if one can vary the phase at a specified input or output power level $|a_1|^2$ or $|a_2|^2$ respectively.

This can be done using a phase shifter as will be seen below. Hence the desired S -parameters can be determined by locating the centers of the $\frac{b_i}{a_j}$ loci.

5.3 Input and Output F.D. Impedance Measurements Using Mazunder's Technique

To determine S_{11} and S_{22} , we need only to measure $\frac{b_1}{a_1}$ and $\frac{b_2}{a_2}$. Using S_{11} and S_{22} the input and output impedances can then be found. The set-up used to make these measurements in this thesis are shown in Figure 5.2. The instruments used are listed in Appendix V. The two

Figure 5.2 Large Signal s-Parameters Measurement Set-Up Using "Two-Signal" Method

To measure the locus of: (i) b_1/a_1 : connect C to R; D to T;

(ii) b_2/a_2 : connect A to R; B to T.

input signals a_1 and a_2 are derived from the signal source. In order to stimulate the frequency division situation, the signal a_2 injected into the output of the halver should have half the frequency of the signal a_1 . Hence the source gives power at the output frequency band which is transformed to the input band using a frequency doubler before a_1 enters the input of the halver. Hence the frequency of a_1 is double that of a_2 as it should be under halving conditions. The quantities $\frac{b_1}{a_1}$ and $\frac{b_2}{a_2}$ are measured using the HP8410A Network Analyzer. The phase angle between a_1 and a_2 is varied by the phase shifter, and the amplitudes $|a_1|$ and $|a_2|$ can be adjusted using the variable attenuators.

For a good "simulation" of the halving conditions (which will give more accurate results), the injected power at the output $|a_2|^2$ should be about -3dBm which is the mean power coming out of the halver as can be seen from Chapter 4.

Of course the input power $|a_1|^2$ should be about +16.4dBm for the device to operate as a halver over the entire desired input frequency band. The measurement procedure is as follows: For each frequency the following four steps are taken:

(a) Calibration measurements are made using a 50Ω matching load, an open-circuit and a short circuit positioned at the input or output ports of the device. Let us name these measured values Γ_{m50} , Γ_{msh} , Γ_{mop} . Knowing the expected (true) values Γ_{rso} , Γ_{rsh} , Γ_{rop} we can calculate the complex coefficients K, L, and M [39] such as:

$$\Gamma_m = \frac{K\Gamma_r + L}{M\Gamma_r + 1} \quad (5.8)$$

In this way, for each measured value Γ_m (which represents b_1/a_1 or b_2/a_2 in this application), one can calculate its "true" value, Γ_r , by solving (5.8):

$$\Gamma_r = f(\Gamma_m, K, L, M) \quad (5.9)$$

(b) Take three measurements Γ_{m1} , Γ_{m2} , and Γ_{m3} for different phase shifter settings (different $\frac{a_2}{a_1}$) such as to locate three different points on the circles mentioned in section 5.2 (See Figure 5.1(b)). Hence having three points, the centre of the circle can be determined. For b_1/a_1 , and b_2/a_2 measurements, this centre corresponds to S_{11} and S_{22} respectively. Of course, before finding the centre of the circle the true values Γ_{r1} , Γ_{r2} , and Γ_{r3} (corresponding to Γ_{m1} , Γ_{m2} and Γ_{m3}) according to (5.9) must first be extracted. Let the centres of the circles be Γ_{rin} , Γ_{hout} .

(c) For better accuracy the microstrip to coaxial(input) and CPW to coaxial(output) transition discontinuities can be taken into account. One can apply the following equation [40]:

$$\Gamma_{rin(out)} = \Gamma_{trans.} + \frac{\Gamma_{din(out)}(S_{12})^2}{1 - \Gamma_{trans.} \Gamma_{d.in(out)}} \quad (5.10)$$

$$\text{We know that } |S_{12}|^2 = 1 - |\Gamma_{trans.}|^2 \quad (5.11)$$

and that S_{12} is perpendicular to $\Gamma_{trans.}$. Hence, since in (5.10) we have $(S_{12})^2$ we do not need to know the phase. $\Gamma_{trans.}$ can be measured using suitably shaped pieces of absorbing material pressed on to the microstrip input or CPW output lines of the divider.

$\Gamma_{r.in}$ and $\Gamma_{r.out}$ have been calculated in step (b) of this procedure. Hence r can be found using (5.10). These $\Gamma_{d.in}$ and $\Gamma_{d.out}$ represent the true S_{11} and S_{22} of the device under frequency halving conditions. $Z_{d.in}$ and $Z_{d.out}$ are the corresponding impedances.

(d) The reflection coefficients Γ_{zin} , Γ_{zout} at the plane of the diodes can be found using a suitable COMPACT impedance de-embedding file because we know the input and output matching circuit patterns. Hence from these coefficients, the "pumped" input and output impedances Z_{in} , and Z_{out} can be found.

Using this procedure the results listed in Tables 5.1, 5.2, 5.3 and 5.4 have been taken, making measurements on one of the devices discussed in Chapter 4, and using a FORTRAN program named LARSIMEAS (See Appendix VI). Table 5.1(a) presents $Z_{d.in}$ for $P_{in} = +16.4\text{dBm}$ and 8 frequencies from 3.50GHz to 7.00GHz with a step size of 0.5GHz. Table 5.1(b) presents $Z_{d.out}$ for $P_{in} = +16.4\text{dBm}$ and $|a_2|^2 = -3\text{dBm}$ for the corresponding output frequencies (1.75-3.5GHz). Table 5.2 presents $Z_{d.in}$ and $Z_{d.out}$ for the threshold input power level at each frequency.

In Table 5.3 the values of Z_{in} and Z_{out} corresponding to these of Table 5.1 can be seen beside the theoretically expected values. Finally, Table 5.4 shows $Z_{d.out}$ at 3.0GHz versus input power. In Figures 5.3 and 5.4 a comparison of the calculated and measured VSWRs at the input and output is given. Comparing the results of Tables 5.2 and 5.1 one can see that at $P_{in} = P_{\text{threshold}}$ the input and output matching is slightly better. This is in agreement with theory presented by Rafuse [2] because the formulas used to calculate the "pumped" impedances are valid for $P_{\text{threshold}}$.

TABLE 5.1

f_{in} (GHz)	$Z_{d.in}$ (Ω)	VSWR
3.5	30.26 - j23.12	2.159
4.0	47.29 + j3.97	1.105
4.5	18.84 + j8.98	2.85
5.0	35.86 + j30.40	2.169
5.5	49.53 - j3.26	1.068
6.0	54.71 + j3.46	1.120
6.5	42.23 + j4.27	1.215
7.0	42.91 - j3.64	1.192

f_{out} (GHz)	$Z_{d.out}$ (Ω)	VSWR
1.75	59.77 - j5.03	1.222
2.00	49.82 + j7.22	1.156
2.25	41.77 + j7.04	1.265
2.50	50.36 - j7.86	1.170
2.75	47.96 - j4.84	1.115
3.00	38.57 - j10.23	1.415
3.25	43.51 + j8.14	1.250
3.50	47.56 - j10.81	1.255

$$P_{in} = +16.4\text{dBm}$$

Table 5.1 Measured Input and Output Impedances of the Device
 $(Z_{d.in}, Z_{d.out})$ Versus Frequency for $P_{in} = +16.4\text{dBm}$

TABLE 5.2

f_{in} (GHz)	$Z_{d.in}$ (Ω)
3.50	-
4.00	$50.52 + j2.61$
4.50	$56.9 + j4.92$
5.00	$41.71 + j30.00$
5.50	$48.85 - j1.95$
6.00	$55.59 + j4.40$
6.50	$41.66 + j3.30$
7.00	$43.95 - j3.51$
f_{out} (GHz)	$Z_{d.out}$ (Ω)
2.50	$50.68 - j7.84$
2.75	$52.73 - j2.14$
3.00	$40.46 - j9.85$

$P_{in} = P_{threshold}$ (at each frequency)

Table 5.2 Measured Input and Output Impedances of the Device (Z_{din} and Z_{dout}) Versus Frequency. The Input Power Level Equals the Threshold Power at Each Frequency

TABLE 5.3

f_{in} (GHz)	Z_{in} (Ω) (experimental)	Z_{in} (calculated)
3.50	$7.01 + j3.95$	$10.7 + j1.11$
4.00	$8.21 + j7.96$	$9.69 + j2.58$
4.50	$7.58 - j1.41$	$8.84 + j3.95$
5.00	$9.05 + j0.19$	$7.75 + j5.82$
5.50	$10.33 + j9.33$	$7.00 + j7.63$
6.00	$11.17 + j9.47$	$6.55 + j8.77$
6.50	$7.54 + j10.84$	$6.16 + j9.88$
7.00	$8.28 + j8.83$	$5.66 + j11.51$

f_{out} (GHz)	Z_{out} (Ω) (experimental)	Z_{out} (calculated)
1.75	$73.07 - j53.83$	$67.81 - j50.31$
2.00	$55.05 - j19.20$	$59.11 - j41.70$
2.25	$51.28 - j41.05$	$52.63 - j35.66$
2.50	$54.27 - j24.08$	$47.21 - j31.82$
2.75	$52.00 - j23.55$	$41.90 - j27.20$
3.00	$37.55 - j33.85$	$39.03 - j24.66$
3.25	$37.30 - j35.19$	$36.52 - j22.39$
3.50	$56.80 - j39.91$	$33.28 - j19.14$

Table 5.3 Measured "Pumped" Input and Output Impedances
 $(Z_{in}$ and $Z_{out})$ Compared to the Theoretically Expected Ones.

TABLE 5.4

P_{in} (dBm)	Z_d in (Ω)
+12	39.65 - j9.68
+13	39.53 - j9.72
+14	39.40 - j9.82
+15	38.88 - j10.13

Frequency = 3.00 GHz

Table 5.4 Output Measured Impedance Versus Input Power at $f_{out} = 3.00$ GHz

Comparing as well the experimental and calculated Z_{in} and Z_{out} from Table 5.3 one can see that they are in good agreement especially for the output. From Figure 5.3 it is evident that the discrepancy between the measured and calculated input VSWR is considerable. This is due to the fact that the device measured was one with copper tuning shims soldered in the input circuit. This means that there are discrepancies in the determination of the input circuit pattern which affect the calculated VSWR of this structure.

On the other hand, Figure 5.4 demonstrates a good agreement between measured and calculated values of the output VSWR versus frequency. This happens because the output circuit pattern is accurately determined since it has not been altered in any way.

All these results lead us to conclude that Mazunder's method is an effective and accurate method to determine the input and output "pumped" impedances in a frequency halver. An agreement with the calculated pumped impedances should be mentioned as well. The low measured VSWR values for the output circuit confirm the potential of the 4th order Marchand balun form used in this thesis. This has been concluded in Chapter 4 as well from the performance of the measured circuits. Figure 5.5 is a plot of Z_{in} and Z_{out} (Table 5.3) in the Smith Chart.

Figure 5.3 Calculated and Measured Input VSWR Versus Frequency

Figure 5.4 Calculated and Measured Output VSUR Versus Frequency

Figure 5.5 Smith Chart Representation of Z_{in} and Z_{out} From Table 5.3 for the corresponding input and output frequencies

CHAPTER 6

SUMMARY, CONCLUSIONS AND RECOMMENDATIONS6.1 Summary and Conclusions

A 4th order Marchand Balun structure having the properties of good coaxial-to-slotline transition and good frequency-variable load matching for a bandwidth in excess of an octave has been found to be a good choice as an output network for octave bandwidth slotline type frequency dividers. The theoretical background used as a basis for this thesis has been given in Chapter 2. The varactor characteristics were discussed first. Frequency halving theory, equations and characteristics followed and the basic stages of evolution of a frequency divider as presented by Harrison were given briefly, as well as the D.E. used to characterize a frequency halver. Then expressions for the calculated input and output "pumped" impedance presented by the two diodes were given. Finally, microstrip and slotline design equations and characteristics have also been given.

In Chapter 3 various kinds of slotline to coaxial transitions were discussed. First the slotline resonator design was given. Then an improved microstrip-to-slotline transition (Schiek's transition) was designed and tested for this particular application to match a frequency variable load. The 4th order Marchand balun structure was then considered and coplanar waveguide design equations and limitations were also given. Finally, a Schiek's transition and a 4th order Marchand balun has been built and tested, and their experimental performance presented in terms

of return loss. The design method followed in Chapters 3 and 4 was based on a CAD technique, and a special program named COMPACT was used for analysis and optimization of the circuits. In Chapter 4 two complete F.D. designs have been given in detail. Marchand's structure was used as the output circuit. The input matching circuit (consisting of micro-strip stepped impedance transformer and stub sections) as well as the output matching circuit were designed first using COMPACT.

Finally, these designs were fabricated and tested. Their experimental performance has been presented in terms of frequency characteristics output power vs. frequency and (P_{in} , and P_{out}) transfer functions. In Chapter 5 Mazumder's method of large signal impedance measurements was presented briefly and was used in this particular application to extract the "pumped" input and output impedance of one of the devices designed in Chapter 4. The resulting impedances and a comparison of input and output VSWR have also been given.

The conclusions of this thesis work can be summarized as follows:

- (i) A 4th order Marchand Balun structure has the potential of both providing a good matching to a frequency-variable load for a bandwidth in excess of an octave and giving good slotline-to-coaxial transition properties. This gives the best reported form of output circuit for slotline type frequency dividers.
- (ii) Mazumder's large-signal impedance measurement method is a powerful tool for the extraction of "pumped" input and output impedances of a halving circuit. After that, depending on the performance achieved, these measurements can be used to optimize the design of the input and output matching circuits.

- (iii) Mazumder's method as applied here showed that there is a considerable agreement (especially at threshold input power levels) between the theoretically calculated and experimentally measured pumped diode impedances.
- (iv) COMPACT was proved to be an efficient tool to optimize input and output circuit design in terms of input and output VSWRs. The starting element values as well as the form of the circuit to be optimized have a considerable effect on the finally obtained minimum value of the error function.
- (v) Better matching in the input circuit (and therefore better performance) can be obtained by using wide microstrip lines adjacent to the diodes. Transverse resonances can be avoided by etching narrow longitudinal slots in these wide lines.
- (vi) Schiek's transition gave good microstrip-to-slotline transition properties compared with all previous microstrip-to-slotline transitions reported in the literature.
- (vii) It is found that the halver performance is sensitive not only to the design of the input and output networks but also to such details as the proper design of the resonator (i.e. compromising between small electrical lengths and large widths) and the exact position of the varactor diodes with respect to both the resonator and the input microstrip circuit.

6.2 Recommendations for Further Work

This thesis has presented an efficient method for designing slotline-type microwave frequency halvers. It can be easily seen that

the main obstacles to obtaining better performance are problems with the matching networks, particularly the input network. The following points are suggested for further work:

- 1) To improve the input matching, diodes with different junction capacitance characteristics can be used.
- 2) The input matching can be improved by using a tapered input microstrip section rather than stepped impedance transformer sections. Suitable stubs can be included in the input circuit pattern as well.
- 3) The potential of the Marchand form of the output circuit can lead to a design for a bandwidth of 2 octaves. Since the obstacle is again the input matching, a better performance might be achieved using tapered input sections and various kinds of devices to make the design.
- 4) The other kind of output circuit tested in this thesis (Schiek's transition) gave very good transition properties.

Hence a divider can be designed using this type of output circuit and including slotline transmission line sections combined with slotline short circuit stubs to achieve the best output matching.

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APPENDIX I

The computer program PAROS consists of the main program and four FUNCTION-subprograms [19].

The subprogram INT calculates the function values $\text{int}(\dots)$. The subprogram GINTEG is used to perform numerical integration and applies an eight-point Gaussian quadrature formula [35]. Hence the slotline characteristic impedance Z_{os} is computed using GINTEG. The subprogram ZINT calculates the values of the integrand $\text{int}_z(\dots)$.

The last subprogram JZERO is called by INT and ZINT, and computes the Bessel function of first kind and order using polynomial approximations [36].

Input Variables:

EPSR	= dielectric constant ϵ_r of the substrate material
H	= substrate thickness h (cm).
WANF	} first value, difference between successive values (>0), and last value of the slot width w (cm).
DW	
WEND	
FANF	} first value, difference between successive values (>0), and last value of frequency f Hz.
DF	
FEND	

Output Parameters Printed:

W	= "actual" value of slot width w (cm).
F	= "actual" value of frequency f (GHz).

LAMG = slot wavelength λ_g (cm).

LAMG/LAM = relative wavelength ratio λ_g/λ_0

EPSREFF = effective dielectric constant ϵ_{reff} .

Z = characteristic impedance Z_{0s} (Ω).

- The program is listed below together with a group of output parameters.

C THIS PROGRAM CALCULATES GUIDE WAVELENGTH AND CHARACTERISTIC
C IMPEDANCE OF A SLOT LINE AS A FUNCTION OF PHYSICAL DIMENSIONS
C SUBSTRATE PERMITTIVITY AND FREQUENCY.

C INPUT VARIABLES:

C 1) EPSR =DIELECTRIC CONSTANT OF THE SUBSTRATE MATERIAL
C 2) H =SUBSTRATE HEIGHT IN CM
C 3) WANF =FIRST VALUE OF SLOT WIDTH IN CM
C 4) IW =DIFFERENCE BETWEEN SUCCESSIVE VALUES OF
C SLOT WIDTH IN CM (GREATER THAN 0.0)
C 5) WEND =LAST VALUE OF SLOT WIDTH IN CM
C 6) FANF =FIRST VALUE OF FREQUENCY IN GHZ
C 7) IF =DIFFERENCE BETWEEN SUCCESSIVE VALUES OF
C FREQUENCY IN GHZ (GREATER THAN 0.0)
C 8) FEND =LAST VALUE OF FREQUENCY IN GHZ

C MAIN PROGRAM:

```

REAL KO,INT
COMMON KO,PI,EPSR,EPSRE,W,H
EXTERNAL INT,ZINT
READ(5,51)EPSR,H,WANF,IW,WEND,FANF,IF,FEND
51 FORMAT(8F10.7)
OGR=400.
PI=3.14159265358979
WRITE(6,92)EPSR,H
92 FORMAT(36H0SLOT LINE ON A DIELECTRIC SUBSTRATE
F//6H EPSR=,F6.3/7H H[CM]=,F6.4)
WRITE(6,93)
93 FORMAT(1X, 'W[CM] F[GHZ] LAMG[CM] LAMG/LAM0
FEPSREFF Z[OHM]')
NW=IFIX((WEND-WANF)/IW+0.5)+1
NF=IFIX((FEND-FANF)/IF+0.5)+1
DO 30 K=1,NW
W=WANF+FLOAT(K-1)*IW
DO 30 J=1,NF
F=FANF+IF*FLOAT(J-1)
ALAM0=29.9792/F
KO=2.*PI/ALAM0
N=1
X0=2.
X1=0.8*EPSR
EPSRE=X0
Y0=GINTEG(INT,OGR,0.)
10 EPSRE=X1
Y1=GINTEG(INT,OGR,0.)
X2=X1-(X1-X0)*Y1/(Y1-Y0)
IF(ABS(X1-X2).LT,0.0001)GOTO 20
IF(N.GT,10)GOTO 30
N=N+1
X0=X1
X1=X2
Y0=Y1

```



```

      GOTO 10
20  EPSRE=X2
      ALAMG=ALAMO/SQRT(EPSRE)
      ALGO=ALAMG/ALAMO
      XPOL=K0*SQRT(EPSR-EPSRE)
      Z=0.25*PI*PI*PI*W*W/GINTEG(ZINT,OGR,XPOL)
      WRITE(6,91)W,F,ALAMG,ALGO,EPSRE,Z
91  FORMAT(1H ,F7.5,4X,F6.3,4X,F9.7,4X,F9.7,4X,F10.7,4X,F11.7)
30  CONTINUE
      STOP
      END

SUBPROGRAM GINTEG:
      FUNCTION GINTEG(FKT,OGR,XPOL)
      GINTEG=0.
      NMAX=IFIX(SQRT((OGR-XPOL)*10.))+1
      DO 100 N=1,NMAX
      RN=FLOAT(N)
      XL=(RN-1.)*(RN-1.)*0.1+XPOL
      XU=RN*RN*0.1+XPOL
      A=0.5*(XU+XL)
      R=XU-XL
      C=0.48014492824876812*R
      Y=0.0506142681451881130*(FKT(A+C)+FKT(A-C))
      C=0.39833323870681337*R
      Y=Y+0.11119051722668724*(FKT(A+C)+FKT(A-C))
      C=0.26276620495816449*R
      Y=Y+0.15685332293894364*(FKT(A+C)+FKT(A-C))
      C=0.09171732124782490*R
      Y=R*(Y+0.18134189168918099*(FKT(A+C)+FKT(A-C)))
100  GINTEG=GINTEG+Y
      IF(XPOL.EQ.0.)RETURN
      NMAX=IFIX(XPOL*10.))+1
      IX=XPOL/FLOAT(NMAX)
      DO 200 M=1,NMAX
      RM=FLOAT(M)
      XL=(RM-1.)*IX
      XU=RM*IX
      A=0.5*(XU+XL)
      R=XU-XL
      C=0.48014492824876812*R
      Y=0.0506142681451881130*(FKT(A+C)+FKT(A-C))
      C=0.39833323870681337*R
      Y=Y+0.11119051722668724*(FKT(A+C)+FKT(A-C))
      C=0.26276620495816448*R
      Y=Y+0.15685332293894364*(FKT(A+C)+FKT(A-C))
      C=0.09171732124782490*R
      Y=R*(Y+0.18134189168918099*(FKT(A+C)+FKT(A-C)))
200  GINTEG=GINTEG+Y
      RETURN
      END

```

C SUBPROGRAM INT:

```

      REAL FUNCTION INT(KX)
      REAL KO,KX,JZERO
      COMMON KO,PI,EPSR,EPSRE,W,H
      EX=JZERO(W*KX/2.)*W/2.*PI
      GAM1=SQRT(KX*KX+KO*KO*(EPSRE-1.))
      RAD=KX*KX+KO*KO*(EPSRE-EPSR)
      IF(RAD.LT.0.)GOTO 100
      GAM2=SQRT(RAD)
      T=(EXP(GAM2*H)-EXP(-GAM2*H))/(EXP(GAM2*H)+EXP(-GAM2*H))
      V=1.
      GOTO 200
100  GAM2=SQRT(-RAD)
      T=SIN(GAM2*H)/COS(GAM2*H)
      V=-1.
200  DET=(V*GAM2*T+EPSR*GAM1)*(GAM2/T+GAM1)
      DET=DET*(EPSR-EPSRE)/(EPSRE-1.)/EPSR/KO/KO
      INT=GAM2/T+GAM1*(EPSR-EPSRE)/(1.-EPSRE)/EPSR
      INT=INT*(1.-V*T*T)/DET/KO
      INT=(INT-T*KO/GAM2)*(EPSR-EPSRE)
      INT=(INT+(EPSRE-1.)*KO/GAM1)*EX*EX
      RETURN
      END

```

C SUBPROGRAM ZINT:

```

      FUNCTION ZINT(KX)
      REAL KO,KO2,KO3,KX,KX2,INT,JZERO
      COMMON KO,PI,EPSR,EPSRE,W,H
      EX=JZERO(W*KX/2.)*W/2.*PI
      EX2=EX*EX
      KO2=KO*KO
      KO3=KO2*KO
      KX2=KX*KX
      EPS=(EPSR-EPSRE)/(1.-EPSRE)
      GAM12=KX2+KO2*(EPSRE-1.)
      GAM1=SQRT(GAM12)
      GAM22=KX2+KO2*(EPSRE-EPSR)
      IF(GAM22.LT.0.)GOTO 100
      GAM2=SQRT(GAM22)
      S=(EXP(2.*GAM2*H)-EXP(-2.*GAM2*H))/2.
      C=(EXP(GAM2*H)+EXP(-GAM2*H))/2.
      T=(EXP(GAM2*H)-EXP(-GAM2*H))/2./C
      V=1.
      GOTO 200
100  GAM2=SQRT(-GAM22)
      S=SIN(2.*GAM2*H)
      C=COS(GAM2*H)
      T=SIN(GAM2*H)/C
      V=-1.

```

```

200 C2=C*C
DET=KX2*(EPSR-1.)*(EPSR-1.)/(1.-EPSRE)/(1.-EPSRE)/K02
DET=DET*EPSRE/EPSR-GAM22/K02-GAM12*EPS*EPS/K02/EPSR
DET=DET-GAM1*GAM2*EPS/K02*(V*T/EPSR+1./T)
BE=(EPSR-1.)/(1.-EPSRE)*EX/DET
BH=-EX/DET/K0*(GAM2/T+GAM1*EPS/EPSR)
AE=EPS*BE/EPSR/C
AH=EPS*BH/C
ZINT=V*KX2*EPSRE*BE*BE/K02/EPSR/T/T
ZINT=ZINT-BH*BH-BH*EX*S*K0/GAM2+C2*EX2*K02/GAM22
ZINT=ZINT*(GAM22-KX2)*H/K02/C2/C2
ZINT=ZINT-2.*KX2*(1.+EPSRE/EPSR)*BE*BH/K03/C2
HV=V*KX2*BE*BE/K0/GAM2/T+T*BH*BH*K0/GAM2
HV=(HV+S*EX2*K03/2./GAM2/GAM22)*(GAM22+KX2)/K03/C2
ZINT=ZINT+HV+2.*(1.+EPSRE)*KX2*AE*AH/K03
HV=EPSRE*KX2/K02*AE*AE+AH*AH+K02*EX2/GAM12
ZINT=ZINT+HV*(GAM12+KX2)/GAM1/K02
ZINT=ZINT*SQRT(EPSRE)/8./PI/29.9792
RETURN
END
C SUBPROGRAM JZERO:
REAL FUNCTION JZERO(X)
IF(X.GT.3.)GOTO 100
XIDQ=X*X/9.
JZERO=1.+7.((((0.00021*XIDQ-0.0039444)*XIDQ+0.0444479)
F*XIDQ-0.3163866)*XIDQ+1.2656208)*XIDQ-2.249997)*XIDQ
RETURN
100 X3=3./X
TET=X-0.78539816+((((0.00013558*X3-0.00029333)*X3
F-0.00054125)*X3+0.00262573)*X3-0.00003954)*X3-0.04166397)*X3
F=0.000+0.79788456+((((0.00014476*X3-0.00072805)*X3+0.00137237)
F*X3-0.00009512)*X3-0.0055274)*X3-0.00000077)*X3
JZERO=1./SQRT(X)*F*COS(TET)
RETURN
END

```

APPENDIX II

The junction capacitance versus reverse bias is presented above for Silicon Tuning Varactors fabricated by Frequency Sources Inc., GHz Division. A pair of GC1504 varactors was used in this thesis.

APPENDIX IIIComputer Aided Design - COMPACT

COMPACT is an ideal tool to design passive and active microwave circuits. The circuit element library includes a wide variety of lumped and distributed elements as well as active devices described by their two-port scattering or y-parameters.

The program has the following main functions:

- (a) Circuit analysis and stability analysis
- (b) Sensitivity analysis
- (c) Optimization (which can be accomplished using up to 15 variables)

For maximum efficiency the program is based on the "two-port" analysis technique that does not require matrix inversions. Optimization is one of the most important features of this program and is widely used in this thesis to optimize both the input and the output matching networks of the F.D.

Mathematically, optimization is a search process in order to find the optimum (minimum) value of a specified function controlling the variation of parameter values upon which the function depends. This function is formulated such as to give a weighted difference between the calculated circuit response and the specified target response. This difference is a measure of "error" in the final objective of the design, and from that the function is defined as the "error function".

The optimum value of the error function is its minimum value, and there may be more than one minimum value. The optimum values of the error function is the least among the various minima and is called the "global minimum" while all others are called "local minima".

A typical error function, used in COMPACT, is of the following form:

$$EF = \frac{1}{N} \sum_{FI}^{FF} (w_1 |S_{11}|^2 + w_2 |VSWR|^2 + w_3 |RLG_D - RLG_A|^2 + w_5 PAD^2) \quad (III:1)$$

where

S_{11} = input reflection coefficient

RLG_A = actual dB Reflection Gain

RLG_D = desired dB Reflection Gain

FI = first frequency

FF = last frequency

w_1, w_2, w_3, w_5 = weighting factors, specified in the data file

N = number of frequencies

PAD = Phase angle in degrees

w_5 is an optional weighting factor, used only when phase angle minimization of S_{11} is required.

In Figure III-1 one can see a COMPACT data file used for the optimization of the input circuit. In Section 1 the definitions and circuit interconnections are given. The frequency information in terms of first frequency, last frequency and frequency step is given in section 2, while the frequency variable impedance data (derived using Equations (2.50)-(2.53) or measured values) are given in section 3.

Finally, the required optimization data are set in terms of weighting factors (Equation (III.1)) in section 4. In this case since optimization in terms of VSWR is required, the weighting factor w_1 corresponding to the input reflection coefficient is set equal to 10 while all others are 0.

TRL AA MS -25.6 -124.3 6000 10.5 25

L

TRL BB MS -52.4 -98.3 6000 10.5 25

OST CC PA -54.5 -52 6000

TRL DD MS 80 -59.2 6000 10.5 25

TRL EE MS 360 -24.3 6000 10.5 25

OST FF PA -45.73 -32.3 6000

TRL GG MS 12 8.38 6000 10.5 25

IMP HH SE

CAX AA HH

PRI AA IR 50 0

PLD AA IR 50 0

END

3600 8400 200

END

10.74 -4.62

10.19 -4.19

9.69 -3.80

9.24 -3.43

8.84 -3.09

8.46 -2.77

8.12 -2.47

7.81 -2.19

7.52 -1.92

7.25 -1.67

7.00 -1.42

6.77 -1.19

6.55 -0.96

6.35 -0.75

6.16 -0.54

5.98 -0.33

5.82 -0.14

5.66 0.05

5.51 0.24

5.37 0.41

5.23 0.59

5.11 0.76

4.99 0.93

4.87 1.09

4.76 1.25

END

.07

10 0 0 0

END

Section 1

Section 2

Section 3

Section 4

Figure III-1 A Typical COMPACT Data File

APPENDIX IV

EFFECTS OF LARGE MICROSTRIP WIDTHS ($> \frac{\lambda_g}{4}$) IN THE
PERFORMANCE OF THE INPUT CIRCUIT

In the design of the input circuit there are strip widths larger than 0.162" which is approximately equal to $\lambda_g/4$ in the frequency region of interest. This fact could result in two kinds of problems:

(a) Frequency dependency of the scattering matrix

Numerical results of scattering parameters vs. frequency have been reported by Kompa [41]. Typical results for frequency dependent scattering matrix coefficients are shown in Figure IV-1a ([6], p.164). The incident mode considered there is the dominant TEM mode while only even modes with $m=0,2,4$ are assumed to be excited by the discontinuity. Figure IV-1a shows that, at frequencies well below the cut-off frequency of the first higher-order mode ($m=2$), the transmission and reflection coefficients are fairly constant. At the cut-off frequency of the TE_{20} mode (f_{c_1}) the incident TEM mode is rejected and no transmission is possible. In the case of Figure IV-1a $f_{c_1} = 6.1 - 6.3$ GHz. Let us examine the case for the maximum width that is used in the designs of Chapter 4, which is 0.360".

$$f_c = \frac{mc}{2\sqrt{\epsilon_{re}(f)} W_e(f)} \quad (IV.1)$$

Using (IV.1) the cutoff frequency of the TE_{20} mode f_{c_1} is:

$$f_{c_1} = \frac{2c}{2\sqrt{\epsilon_{re}(f)} W_e(f)} \quad (m=2) \quad (IV.2)$$

$$W = 0.360" = 0.9144 \text{ cm}, \epsilon_r = 10.5 \text{ hence } f_g = \frac{c}{2W\sqrt{\epsilon_r}} = 5.062 \text{ GHz}$$

$$\epsilon_{re}(0) = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} F(w/h) = 9.2581 \quad (\text{IV.3})$$

$$\text{where } F(w/h) = (1 + 12h/w)^{-1/2} \quad (\text{IV.4})$$

$$Z_{om} = \frac{\eta}{\sqrt{\epsilon_{re}(0)}} \left\{ \frac{W}{h} + 1.393 + 0.667 \ln \left(\frac{W}{h} + 1.444 \right) \right\}^{-1} \quad (\text{IV.5})$$

$$\text{where } \eta = 120\pi$$

$$Z_{om} = 7.02547\Omega$$

$$\epsilon_{re}(f) = 10.5 - \frac{10.5 - 9.2581}{1 + \left(\frac{f}{f_p}\right)^2} \quad (\text{IV.6})$$

$$G = 0.6 + 0.009 Z_{om} = 0.66323, f_p = \frac{15.66 Z_{om}}{h \text{ (mils)}} = 4.4007 \text{ GHz}$$

$$(\text{IV.6}) \text{ gives: } \epsilon_{re}(f) = 9.6977 \text{ for } f=4\text{GHz and } \epsilon_{re}(f) = 10.111 \text{ for } f=8\text{GHz} \quad (\text{IV.7})$$

$$W_e(0) = 120\pi h / (Z_{om} \sqrt{\epsilon_{re}(0)}) = 1.120 \text{ cm} \quad (\text{IV.8})$$

$$W_e(f) = W + \frac{W_e(0) - W}{1 + (f/f_g)^2}$$

$$\text{This gives } W_e(f) = 1.0291 \text{ for } f=4\text{GHz}$$

$$\text{and } W_e(f) = 0.993832 \text{ for } f=8\text{GHz} \quad (\text{IV.9})$$

Using (IV.2), (IV.7) and (IV.9) one can get:

$$f_{c1} = 9.36 \text{ GHz for } f = 4.0\text{GHz}$$

$$\text{and } f_{c1} = 9.493 \text{ GHz for } f = 8.0\text{GHz}$$

One can see that this cut off frequency is far from the useful input bandwidth (3.50-7.2 GHz).

(b) Transverse resonances

For a sufficiently wide microstrip line ($\geq \frac{\lambda}{4}$) a transverse-resonant mode can exist which can also couple strongly to the quasi-TEM microstrip mode. At the cut-off frequency for this transverse resonant mode the equivalent circuit is a resonant transmission line of "length" $w+2d$ (see Figure IV-1(b)) where d accounts for the microstrip side-fringing capacitance: $d=0.2h$. This situation is illustrated in Figure IV.-1(b). A half-wavelength must be supported by the "length" $w+2d$. Therefore the cut-off half-wavelength is:

$$\frac{\lambda_{CT}}{2} = w+2d \quad (IV.10)$$

For $\epsilon_r=10.5$ and $h=0.025"$ (IV.10) gives that w should be greater than $0.200"$ in order for f_{CT} to be out of the useful input band. Vendelin [42] has indicated that slots, introduced into the metal strip, can suppress the transverse-resonant mode.

(a)

(b)

Figure IV-1(a) Computed Scattering Coefficients for A Step Discontinuity as a Function of Frequency [7]
 (b) Transverse Resonance: Standing Wave $|E_y|$ and Equivalent Transmission Line

APPENDIX V

A list of instruments used for the measurements in Chapter 5 is given below:

1. H.P. 8620C Sweep Oscillator: RF Plug In (1.7-4.3 GHz)
2. H.P. 11667A power splitter
3. 3203B NARDA coaxial directional coupler (1.0-12.4 GHz)
4. H.P. 432A power meter
5. 3753B NARDA coaxial phase shifter
6. 15 792 FM NARDA variable attenuators (2.0-12.4 GHz)
7. ASC-2040 Aertech circulator (2.0-4.0 GHz)
8. 3022 NARDA bi-directional coaxial coupler (1.0-4.0 GHz)
9. Device under test (D.U.T.)
10. HP 8410A Network Analyzer and HP 8411A Harmonic Frequency Converter
- 11., 12. Digital Multimeters (D.V.M.)
13. RX8000 16436 Aertech Frequency Doubler
14. 719CSL Amplica Inc., microwave amplifier (4.0-8.0 GHz)
16. ASC-4080 Aertech circulator (4.0-8.0 GHz)
17. 3024 NARDA bi-directional coaxial coupler (4.0-8.0 GHz)

APPENDIX VI

The variables presented in the FORTRAN program named LARSIMEAS are as follows:

$$R = \begin{bmatrix} R_e(r_{m1}) + j I_m(r_{m1}) \\ R_e(r_{m2}) + j I_m(r_{m2}) \\ R_e(r_{m3}) + j I_m(r_{m3}) \\ R_e(r_{m4}) + j I_m(r_{m4}) \end{bmatrix}$$

r_{m4} = the reflection coefficient due to the transition

$$C = R_e(r_{msh}) , D = I_m(r_{msh}) , E = R_e(r_{mop}) , F = I_m(r_{mop})$$

$$G = R_e(r_{rop}) , J = I_m(r_{rop}) , O = R_e(r_{mso}) , P = I_m(r_{mso})$$

A list of the program follows:

1C LARSIMEAS

```

      INTEGER IA,M,N,KBASIS,IP(4),IER,JA1,M1,N1,KBASIS1,IP1(3),IER1
      REAL A(4,4),B(4),TOL,X(4),H(4),C,D,E,F,G,J,O,P,Q
      REAL A1(3,3),B1(3),TOL1,X1(3),H1(3)
      REAL Y4,Y5,Y7,Y8,Y9,Y10,Y11,Y15,Y16,Y17,Y18,Y19
      COMPLEX R(4),S(4),Y1,Y2,Y3,Y6,Y12,Y13,Y14
      READ(5,8)R
8  FORMAT(8F8,4)
      READ(5,*)IA,M,N,KBASIS,TOL
      READ(5,*)C,D,E,F,G,J,O,P
      PJ=3.141593
      A(1,1)=-C
      A(1,2)=D
      A(1,3)=1.0
      A(1,4)=0.0
      A(2,1)=-D
      A(2,2)=-C
      A(2,3)=0.0
      A(2,4)=1.0
      A(3,1)=(G*F)+(E*J)
      A(3,2)=(E*G)-(F*J)
      A(3,3)=-J
      A(3,4)=-G
      A(4,1)=(E*G)-(F*J)
      A(4,2)=-G*F-(E*J)
      A(4,3)=-G
      A(4,4)=J
      B(1)=C-D
      B(2)=-D+P
      B(3)=P-F
      B(4)=-O+E
      CALL ILSQF(A,IA,M,N,B,TOL,KBASIS,X,H,IP,IER)
      WRITE(6,90)B -
90  FORMAT(4F10,5)
      WRITE(6,40)TOL
40  FORMAT(F8,3)
      WRITE(6,50)X
50  FORMAT(4F15,5)
      Y1=CMPLX(X(1),X(2))
      Y2=CMPLX(X(3),X(4))
      Q=-O
      Y3=CMPLX(Q,P)
      DO 15 I=1,4
      S(I)=(Y3-R(I))/(Y1*R(I)-Y2)
      WRITE(6,60)S(I)
60  FORMAT(2F12,3)
15  CONTINUE

```

```

A1(1,1)=2*(REAL(S(1)))
A1(1,2)=2*(AIMAG(S(1)))
A1(1,3)=1.0
A1(2,1)=2*(REAL(S(2)))
A1(2,2)=2*(AIMAG(S(2)))
A1(2,3)=1.0
A1(3,1)=2*(REAL(S(3)))
A1(3,2)=2*(AIMAG(S(3)))
A1(3,3)=1.0
R1(1)=-((REAL(S(1)))**2)-((AIMAG(S(1)))**2)
R1(2)=-((REAL(S(2)))**2)-((AIMAG(S(2)))**2)
R1(3)=-((REAL(S(3)))**2)-((AIMAG(S(3)))**2)
READ(5,*)IA1,M1,N1,KBASIS1,TOL1
CALL LLSQF(A1,IA1,M1,N1,R1,TOL1,KBASIS1,X1,H1,IP1,IER1)
WRITE(6,75)R1
75 FORMAT(3F10.5)
WRITE(6,25)TOL1
25 FORMAT(F8.3)
WRITE(6,35)X1
35 FORMAT(3F15.5)
Y4=-X1(1)
Y5=-X1(2)
Y6=CMPLX(Y4,Y5)
Y7=AIMAG(S(4))/(REAL(S(4)))
Y8=TAN(PI/2+ATAN(Y7))
Y9=(1-(CABS(S(4)))*(CABS(S(4))))/(1+(Y8)*(Y8))
Y10=SQRT(Y9)
Y11=(Y10)*(Y8)
Y12=CMPLX(Y10,Y11)
Y13=(Y12)*(Y12)
Y14=(Y6-S(4))/(Y13)
Y15=1-REAL(Y14)
Y16=((Y15)**2)/(AIMAG(Y14))
Y17=100/(Y16+AIMAG(Y14))
Y18=(Y17*(1-REAL(Y14)))/(AIMAG(Y14))
Y19=Y18-50
WRITE(6,45)Y6,Y12,Y13,Y14
45 FORMAT(8F10.5)
WRITE(6,6)Y7,Y8,Y9,Y10
6 FORMAT(4F10.5)
WRITE(6,65)Y11,Y15,Y16,Y18
65 FORMAT(4F10.5)
WRITE(6,67)Y19,Y17
67 FORMAT(2F10.5)
STOP
END

```


END

0	6	1	0	9	1	8	4
---	---	---	---	---	---	---	---

FIN