Low Noise CMOS Voltage-Control Oscillator Design Methodology with Emphasis on Non-linear Effect Contributions, 2.4 GHz CMOS Design Example

by

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The information used in this thesis comes in part from the research program of Dr. Tadeusz Kwasniewski and his associates in the VLSI in Communication group. The research results appearing in this thesis represent an integral part of the ongoing research program. All research results in this thesis including tables, graphs and figures but excluding the narrative portions of the thesis are effectively incorporated into the research program and can be used by Dr. Kwasniewski and his associates for educational and research purpose, including publication in open literature with appropriate credits. The matters intellectual property may be pursed cooperatively with Carleton University and Dr. Kwasniewski and where and when appropriate.

Abstract

The Voltage-controlled oscillator (VCO) is one of the most important building blocks in modern communication applications. Although results of many studies have been reported, designing a VCO with low phase noise remains an active research area. Much effort has been devoted to study the generation of phase noise, in order to guide the design and optimization of VCO. However, most of the existing phase noise magnitude expressions are based on linear models. At the same time, practical implementations show attempts to design oscillators operating with fewer harmonics [1].

This thesis demonstrates an attempt to link non-linear (transient) oscillator behavior with phase noise. Phase noise generation is first studied, starting with examining Groszkowski's equation. After studying the mechanism, it is found that phase noise is determined by the transfer function and harmonics and based on which, a VCO design guideline is proposed to aid low phase noise VCO design. Then a novel VCO topology is proposed based on this guideline, aiming to reduce the harmonics and decrease the magnitude and the bandwidth of the transfer function. The circuit was designed and implemented in 0.13um IBM CMOS technology. The simulated performance at 2.4GHz was -133dBc/Hz at 1MHz offset with supply current of 3.07mA at 1V supply.

Acknowledgements

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List of Symbols and Abbreviations

γ	Noise factor of field=effect transistor
θ	Phase
ω	Angular frequency
f	Frequency
F	Noise factor
g_m	Transconductance of transistor
G	Gain of Transfer Function
G_m	Transconductance of differential pair
H	Function of feedback part
j	Imaginary unit ($j^2 = -1$)
k_B	Boltzman constant (1.3807×10^{-23}[J/K])
$\mathcal{L}$	Noise power per Hertz
P	Power
q	Charge of electron
Q	Quality factor
T	Absolute temperature [K]

AC	Alternating Current
CMOS	Complementary Metal Oxide Semiconductor (FET)
DC	Direct Current
FET	Field-Effect Transistor
ISF	Impulse Sensitivity Function
MOS	Metal Oxide Semiconductor
NMOS	N-Channel Metal Oxide Semiconductor (FET)
PLL	Phase-Locked Loop
PMOS	P-Channel Metal Oxide Semiconductor (FET)
RF	Radio Frequency
THD	Total Harmonic Distortion

VCO	Voltage Controlled Oscillator

1 Chapter: Introduction

With the rapid development of the wireless communication industry, more available channels are demanded. As a result, phase noise requirements in the local reference signal in transceiver and receiver systems (Figure 1.1) are becoming more stringent. Usually the reference signal is generated by a frequency synthesizer [2- 4], of which there are three types: direct analog synthesizers, direct digital synthesizer and indirect digital synthesizers. Indirect digital synthesizers, or the so-called phase-locked loop (PLL), are implemented by locking the phase of the voltage-controlled oscillator (VCO) to the reference signal.

In typical PLL architecture, the VCO is the main component for determining the phase noise performance and power consumption of the entire system (see Figure 1.2). In the past, the VCO was fabricated in gallium arsenide (GaAs) technology or bipolar junction transistors (BJT) for higher performance. Nowadays, as the integrated circuits converge into complementary metal-oxide semi-conductors (CMOS), studies and designs around high-performance CMOS VCOs have become very important.

1.1 VCO Metrics

Table 1 lists the specifications and requirements for a VCO. Among them, center frequencies, tuning range, phase noise, and power consumption are the key metrics. Center frequency and tuning range differ from the applications. Usually, center frequency may be influenced by temperature and other conditions, thus a wide tuning range is desirable [5].

Designing a low-phase noise VCO is a major direction in VCO research. Many theory and topologies have emerged with the aim of achieving better phase noise [6- 26]. With greater numbers of portable wireless devices developed, low-power VCO design has become another major research direction. Obviously, to achieve low power, the most direct method is to reduce supply voltage. However, reducing the supply voltage will inevitably increase phase noise. Therefore, it is extremely important to find a

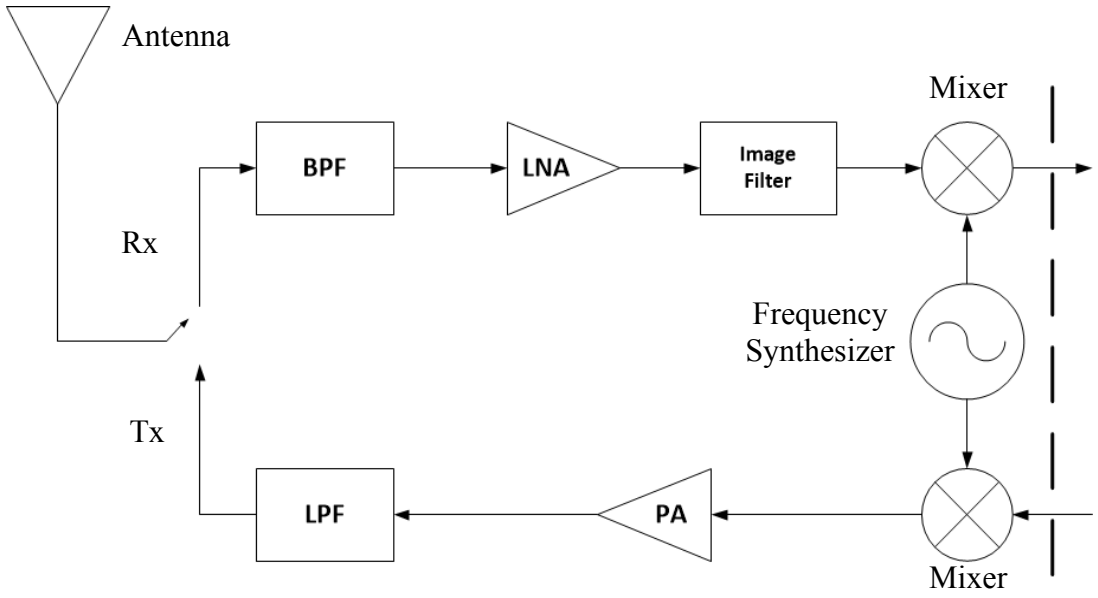


Figure 1.1: Block diagram of RF front end in a typical heterodyne radio transceiver.

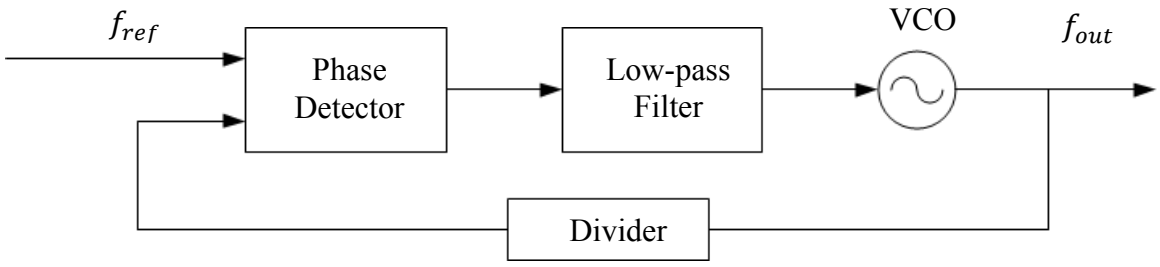


Figure 1.2: Block diagram for a typical PLL system

solution for achieving high-phase noise performance under a limited voltage supply and power budget.

1.2 Motivation

Many efforts have been made to study the generation of phase noise. Various models and approaches have been put forward to predict the phase noise, from Leeson's empirical equation [27] in 1966 to Hajimiri's Impulse Sensitive Function approach [13] in 1999. However, although accurate in predicting the phase noise, these theory are less practical

Table 1: VCO specification list

Specifications	Unit
Center Frequency	GHz
Tuning Range	MHz
Phase Noise	dBc/Hz @ offset (Hz)
Power Consumption	mW
Supply Voltage	V
VCO-Gain	MHz/V
Pulling	MHz/load-spec
Pushing	MHz/V
Area	μm^2

in guiding VCO designs. Therefore it is critical to find a design methodology giving more insight to the actual VCO designing.

Hence, in this work, an attempt to link non-linear behavior to phase noise has been made. From the exploration, non-linear factors that determining the phase noise performance have been found gradually. These factors provide clear insights in VCO designs.

Following the design insights, a VCO topology employs non-linear factors suppression techniques has been proposed. Simulation results showed that the phase noise performance is highly increased in the proposed circuit. For further verification, a 2.4GHz VCO example has been designed and fabricated in IBM 130nm process using the proposed topology.

1.3 Organization of Thesis

This thesis starts with a review in VCO theory and topologies in Chapter 2. The theory includes both linear and non-linear approaches. Topologies cover the review of the circuits from previous literatures.

In Chapter 3, an analysis of phase noise generation is first presented, followed by a proposal of VCO topology aimed at reducing phase noise using non-linear factors

suppression techniques. Simulation results comparison among the proposed topologies and other two references topologies are reported, showing the advantage of the employed techniques.

In Chapter 4, an example circuit using the proposed topology has been designed. Design issues are discussed, including tank, transformer, and overview optimization. Simulation results are shown consequentially.

In Chapter 5, chip design is demonstrated. Measurements setup and failure analysis are included.

In Chapter 6, the thesis is summarized. Contributions are concluded, followed by a discussion of future work.

2 Chapter: Reviews on VCO Theory

2.1 Introduction

This chapter first reviews the previous studies on VCO theory, including both linear and non-linear approaches. Barkhausen Criteria, a linear approach in determining the oscillation startup is first reviewed, followed by another linear approach, negative resistance approach. Then Leeson's empirical equation, which gave a general insight of the factors that influence the phase noise performance, is introduced. Darabi's mixer approach gave more insight in the noise factor of the circuit. Finally Hajimiri's non-linear cyclone stationary approach, which is usually referred as Impulse Sensitive Function (ISF), is presented.

In the second part, several circuit examples in recent literatures have been demonstrated, including ring oscillators and LC-tank based oscillators. In this thesis focus are put on LC-VCOs considering their phase noise performance is generally higher than ring-oscillators. Starting with the conventional LC-VCO, another three circuits have been analyzed. Some other techniques and circuits also have been reviewed roughly.

2.2 Reviews on VCO Theory

2.2.1 Barkhausen Criteria

Barkhausen Criteria [28] is a mathematical formula to determine when a linear electronic circuit will oscillate. The criteria treat the oscillator as a linear positive feedback loop, as shown in Figure 2.1, where the forward gain $G(j\omega)$ represents the voltage transfer function of the amplifier and $H(j\omega)$ is the voltage transfer function of the feedback network. Obviously the transfer function of the complete network is given by

$$\frac{V_{out}}{V_{in}} = \frac{G(j\omega)}{1 - G(j\omega)H(j\omega)}. \quad (1)$$

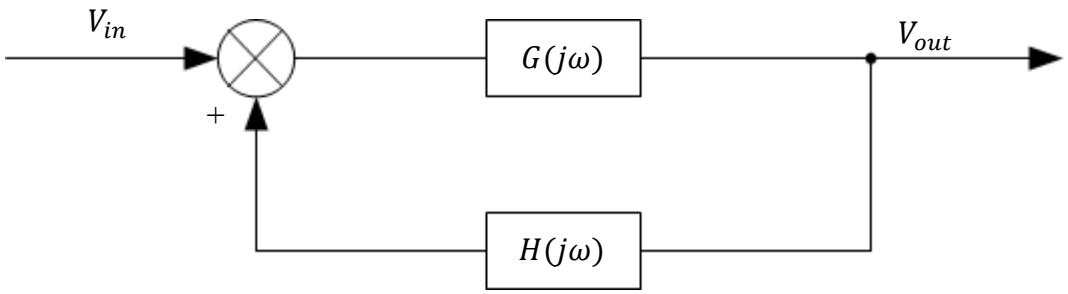


Figure 2.1: Block diagram of feedback oscillator circuit

To make the system unstable, the root of the denominator should be located at the right-hand side of the complex axis, given

$$|G(j\omega)||H(j\omega)| \geq 1. \tag{2}$$

To keep the amplitude constant,

$$|G(j\omega)||H(j\omega)| = 1. \tag{3}$$

For the phase,

$$\emptyset_{G(j\omega)} + \emptyset_{H(j\omega)} = 0 + 2\pi k \qquad k = 1, 2 \ \ldots n. \tag{4}$$

Equations (3) and (4) represent the well-known Barkhausen Criteria, where $\emptyset_{G(j\omega)}$ and $\emptyset_{H(j\omega)}$ is the phase shift of $G(j\omega)$ and $H(j\omega)$. Note that these criteria pose a necessary condition, but are not sufficient. In some circuits, the criteria are fulfilled, but do not oscillate. In reality, to guarantee the start-up, the loop gain $|G(j\omega)||H(j\omega)|$ is usually made larger than 1, leading to increase of the amplitude. Then, the gain will fall back to 1 as a result of the nonlinearity of the circuit.

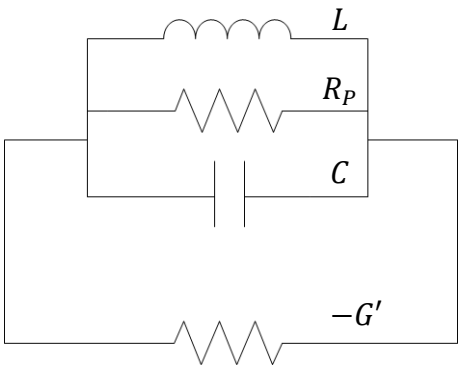


Figure 2.2: Negative resistance model for oscillators

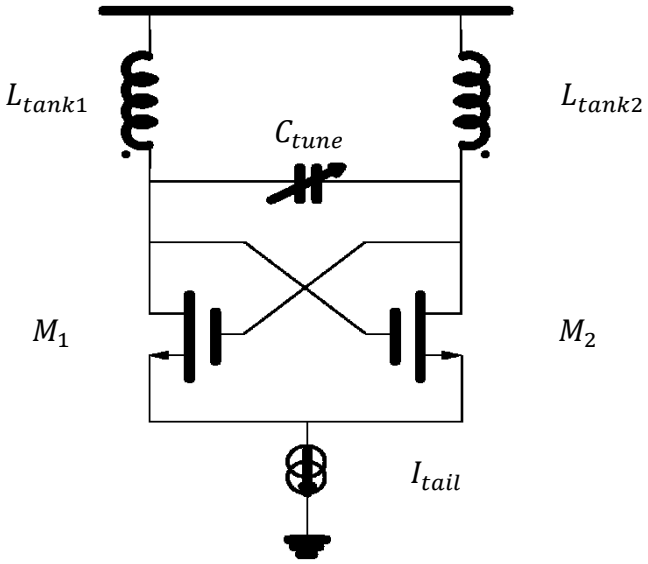


Figure 2.3: Schematic of conventional differential LC-VCO

2.2.2 Negative Resistance Approach

This approach is widely used in LC tank-based oscillators. In actual LC tanks, the oscillations will die out because of parasitic resistance as the resistance consumes power and causes energy loss. Hence, to maintain the oscillation, the active network should generate a negative conductance, $-G'$, to cancel the conductance G from the tank (see Figure 2.2).

As the calculation of $-G'$ depends on the topology, here the conventional LC-VCO is taken as an example (Figure 2.3). Consider the VCO as a circuit consisting of a port (tank) and a negative resistance network shown in Figure 2.4(a). The equivalent

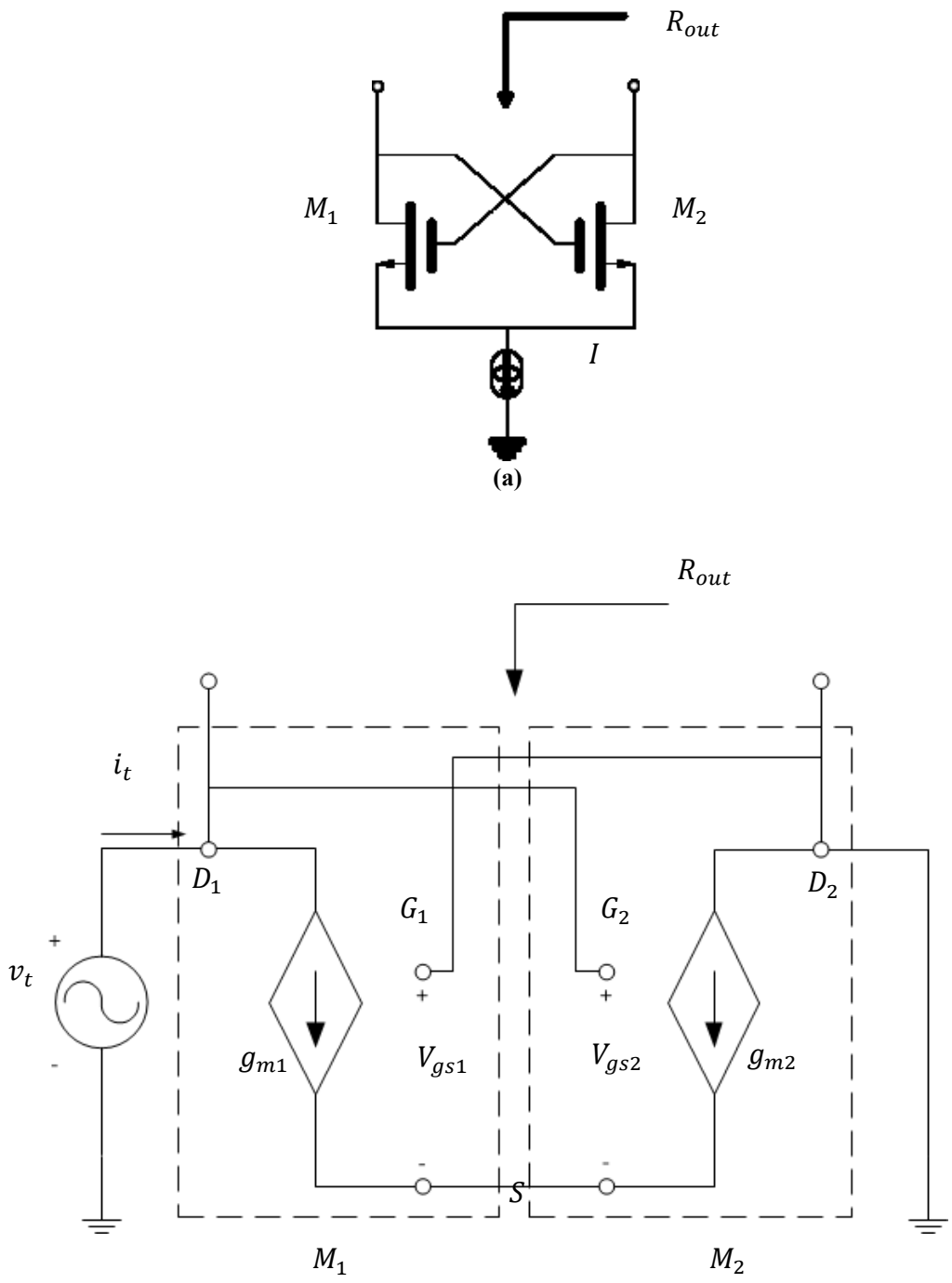


Figure 2.4: (a) One-port model for LC-VCO; (b) Small signal model for LC-VCO.

small signal circuit is shown in Figure 2.4(b). The dependence of the signal quantities on time will be dropped in order to simplify the analysis of this circuit.

Given the voltage across v_t

$$v_t = v_{gs2} - v_{gs1}, \tag{5}$$

and the current flow through the transistors i_t

$$i_t = g_{m1} v_{gs1} = -g_{m2} v_{gs2}, \tag{6}$$

where g_m is the transconductance of the transistors, R_{out} can be given by

$$R_{out} = \frac{v_t}{i_t} = -\frac{1}{g_{m1}} - \frac{1}{g_{m2}}. \tag{7}$$

In typical design $g_{m1} = g_{m2}$, given

$$R_{out} = \frac{v_t}{i_t} = -\frac{2}{g_{m1}}. \tag{8}$$

Equation (9) provides insights in choosing appropriate dimensions of active devices. It should be noted that g_{m1} and g_{m2} are the average transconductance.

2.2.3 Leeson's Empirical Expression

In 1966, Leeson [27] put forward a well-known empirical expression (10) for the single-sideband phase-noise spectrum of oscillators,

$$\mathcal{L}(\Delta f) = 10log\left[\frac{1}{2}\left(\left(\frac{f_0}{2Q_L}\right)^2 + 1\right)\left(\frac{f_c}{\Delta f} + 1\right)\left(\frac{F k_B T}{P_s}\right)\right] \tag{10}$$

where f_0 is the output frequency, Q_L is the loaded quality factor of the tank, f_c is the $1/f$ corner frequency, Δf is the offset from the output frequency, F is the noise factor, k_B is

Boltzman's constant, T is the absolute temperature in Kelvins, and P_s is the output power of the oscillator.

This empirical expression gives two ways of reducing the phase noise, whether increasing Q_L or increasing P_s. To maximize Q_L, one should employ a high Q tank. Because

$$P_s \propto V_{peak}^2. \tag{11}$$

The most efficient way to improve P_s is to increaseV_{peak}, which is the maximal voltage across the tank. Usually V_{peak} is limited by the supply voltage, but also depends on the topologies.

With

$$Q_L \approx \omega L_s/R_s \tag{12}$$

$$\boldsymbol{f_c \gg \Delta f} \tag{13}$$

$$P_s = V_{peak}^2/(2R_s) \tag{14}$$

equation (10) can be simplified to:

$$\mathcal{L}(\Delta f) = 10log\left[\left(\frac{Fk_BT}{P_s}\right)\left(\frac{f_c}{\Delta f}\right)^2\right]. \tag{15}$$

Note that equation (15) only describes the $1/f^2$ portion of the phase noise.

2.2.4 Mixer Model

In 2000, Darabi proposed a simple model [29] for noise in mixers, showing that the model of switching pairs is sufficient to explaining all frequency translations of noise. In

[25], Rael used the model to explain the noise in conventional differential LC-VCOs (see Figure 2.3).

The model treats the transistors as switching pairs. Assume that the sinusoidal output waveform v_o is accompanied by noise v_n. Suppose that the switching pair can be fully turned on with a small amount of voltage around the zero crossing, hence the pulse-width modulated current can be decomposed into the original periodic-square wave and random-width pulses with constant height $2I_{tail}$ (Figure 2.5). These pulses can be viewed as a train of impulses with a double-oscillation frequency sampling the original noise waveform.

The noise source in the circuit forms three parts: tank, differential pair and current source. Hence the phase noise can be given by

$$\mathcal{L}(\Delta f) = 10log\left[F\frac{4k_BTR_p}{V_{peak}^2}\left(\frac{f_0}{2Q\Delta f}\right)^2\right] \tag{16}$$

with a noise factor F, where

$$F = 2 + \frac{8\gamma R_p I_{Tail}}{\pi V_{peak}} + \frac{8}{9}\gamma g_m R_p. \tag{17}$$

Here R_p is the equivalent parallel resistance of the tank, Q is the quality factor of the tank, γ is the noise factor of a single field-effect transistor (FET) (typically $\gamma \approx \frac{2}{3}$), and g_m is the transconductance of the FET. Replacing R_p by

$$R_p = Q^2 R_s, \tag{18}$$

phase noise can be derived into,

$$\mathcal{L}(\Delta f) = 10log\left[\frac{Fk_BTR_s}{V_{peak}^2}\left(\frac{f_0}{\Delta f}\right)^2\right]. \tag{19}$$

It can be seen that equation (19) is in accordance with equation (15), which proves

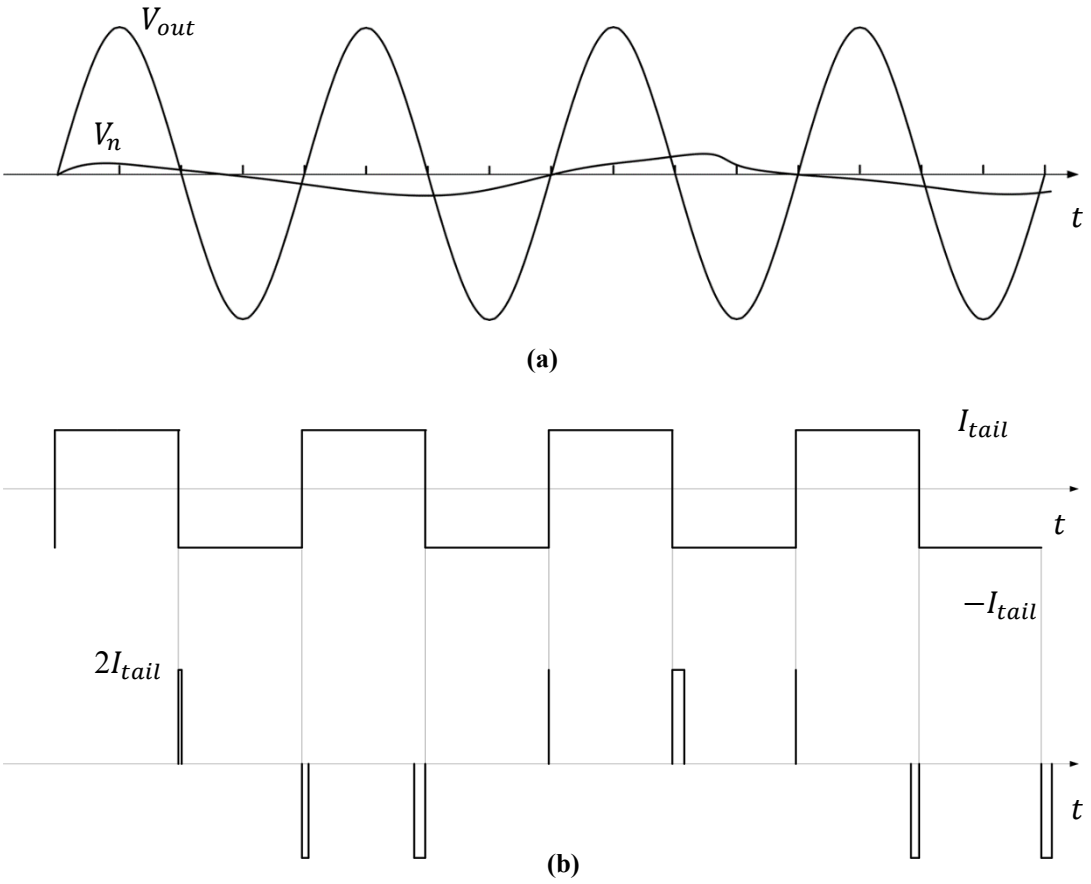


Figure 2.5: (a) Noise at input of differential pair modulates instants of zero crossing. (b) Output current consists of square wave and random noise pulses.

Leeson's hypothesis. However, this approach gives more insight into the relation between the dimensioning of the active part and the noise factor F.

2.2.5 Impulse Sensitivity Function

In 1998, Hajimiri proposed a time-variant phase noise model for electrical oscillators [13] [15]. The theory's main idea is that noise sensitivity is time-variant over a period, as illustrated in Figure 2.6. If a current impulse is injected into the voltage waveform at the peak point, it does not cause phase shift, leaving amplitude shift only. If the impulse is

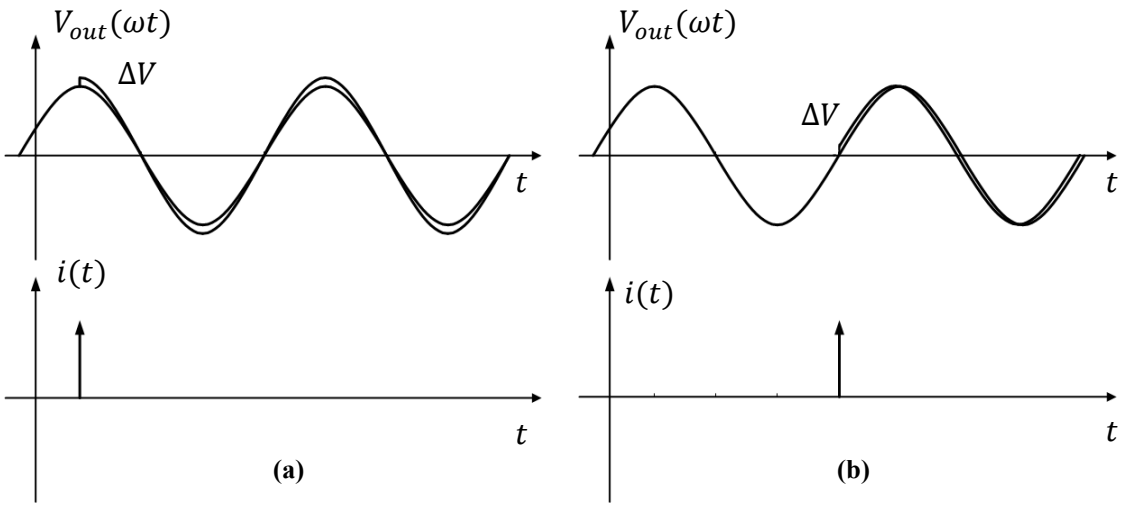


Figure 2.6: (a) Impulse injected at the peak. (b) Impulse injected at the zero crossing.

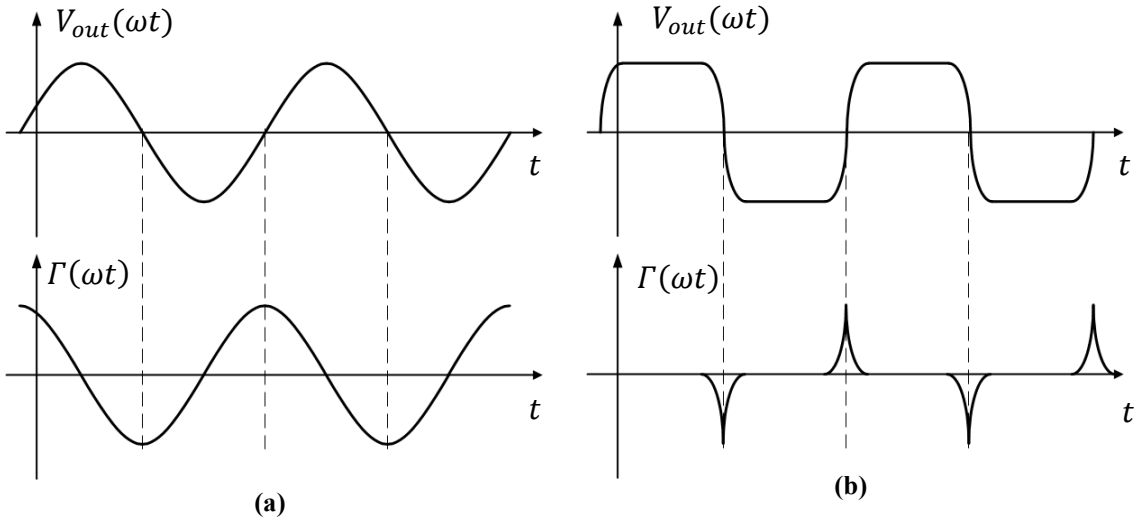


Figure 2.7: Typical ISF for (a) LC-VCOs and (b) ring oscillators.

injected at the zero crossing point, the noise is transferred only into phase shift, producing no amplitude change. At other points, the impulse causes both amplitude and phase shifts. However, only the phase shift will be transformed into phase noise. Therefore, an impulse sensitivity function (ISF), $\Gamma(\omega t)$, is defined as a dimensionless, frequency, and amplitude-independent periodic function to describe the extent to which phase shifts are caused by applying a unit impulse at $t = \tau$.

Figure 2.7 shows the ISF for typical LC-tank VCO and ring oscillators. In practice, $\Gamma(\omega t)$ can be approximated as the first derivative of the voltage waveform.

After derivation, the phase noise spectrum of the $1/f^2$ region is:

$$\mathcal{L}(\Delta\omega) = 10log\left(\frac{\Gamma_{rms}^2}{q_{max}^2}\frac{\overline{i_n^2}/\Delta f}{4\Delta\omega^2}\right) \tag{20}$$

where Γ_{rms} is the rms value of $\Gamma(\omega t)$, $\overline{i_n^2}/\Delta f$ is the power spectral density of each noise source, q_{max} is the maximum charges across the tank, $\Delta\omega$ is the offset frequency. Γ_{rms} can be obtained by

$$\Gamma_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi}|\Gamma(\omega t)|^2 d\omega t}. \tag{21}$$

q_{max} can be obtained by

$$q_{max} = CV_{peak} \tag{22}$$

where C is the capacitance of the tank.

The ISF theory is extremely general and can be applied to all electrical oscillators. The theory accurately predicts the phase noise of a VCO.

2.3 VCO Topology Examples from Literatures

2.3.1 Ring Oscillators

Ring oscillators are built by a chain of inverters. Each stage offers a phase shift with 180°. To create oscillation, the number of stages should be odd. Figure 2.8 shows a three-stage ring oscillator. Ring oscillators are easy to design and integrate, occupying only a small

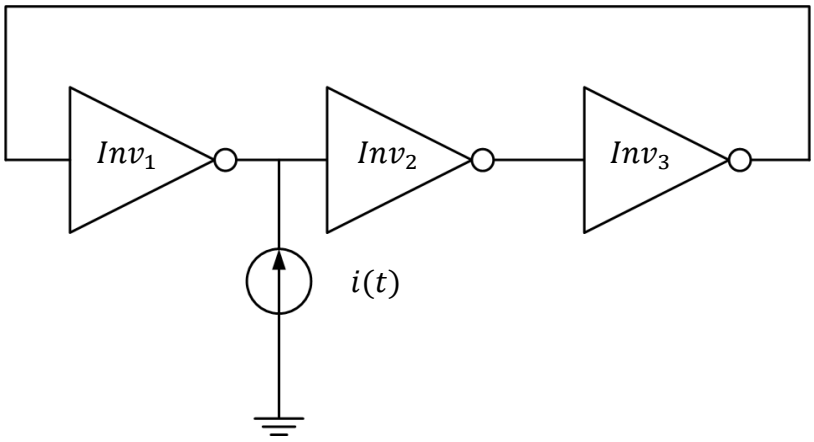


Figure 2.8: 3 stages ring oscillators.

area. Also, they have a very wide tuning range. The main drawback, however, is the high-phase noise they produce. Because the ring oscillators form a closed chain, noise inside accumulates, leading to high overall noise [30 -32].

2.3.2 LC-tank Based VCO

Here, we only discuss N-type metal-oxide semiconductor logic (NMOS) LC tank–based VCO topologies.

2.3.2.1 Conventional LC-VCO

The most widely used VCO topology is shown in Fig. 2.3. It is also referred to as negative-resistance VCO or cross-coupled differential VCO. Analysis based on the negative resistance model has been presented in chapter 2.2.2.

From the mixer approach, the circuit can be interpreted as using a feedback network consisting of a differential switching pair and FET as the current source. The current source not only provides bias current, but also offers high impedance in series [25]. Both would help to reduce the phase noise.

In time domain, the switching transistors M_1 and M_2 are turned on alternatively

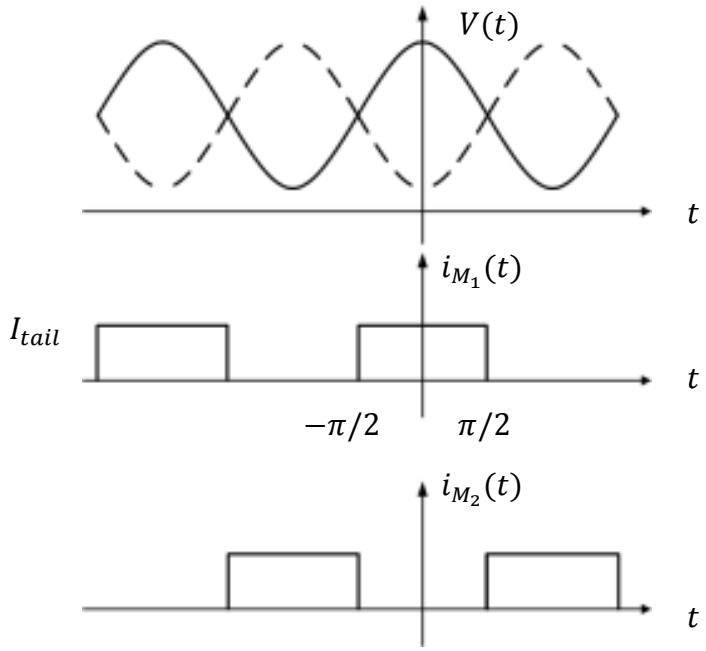


Figure 2.9: Time domain waveforms for conventional LC-VCO.

(see Figure 2.9). The drain currents of M_1 and M_2 can be approximated as square wave, which are,

$$I_{d1} = I_{tail} \cdot \sum_{n=-\infty}^{\infty} \prod\left(\frac{\phi - 2n\pi}{\pi}\right) \quad (\mathbf{23})$$

$$I_{d2} = I_{tail} \cdot \sum_{n=-\infty}^{\infty} \prod\left(\frac{\phi - 2n\pi - \pi}{\pi}\right) \quad (\mathbf{24})$$

where $\prod(x)$ is a single pulse centered at the origin with unity amplitude and duration of 1, namely

$$\prod(x) = \begin{cases} 1, & -0.5 \le x \le 0.5 \\ 0, & \text{otherwise} \end{cases}. \quad (\mathbf{25})$$

After Fourier transformation, it is easy to obtain the DC component I_0 and the magnitude of the first harmonic I_1 at ω_0 respectively, which are

$$I_0 = \frac{1}{2} I_{tail} \tag{26}$$

$$I_1 = \frac{2}{\pi} I_{tail}. \tag{27}$$

where I_{tail} is the average current of the tail current. Since the resonator impedance is low except at frequency around ω_0, the single-ended oscillation amplitude can be calculated as

$$V_{peak} = \frac{2}{\pi} I_{tail} R_p, \tag{28}$$

where R_p is the parallel resistance of the tank.

As it has been mentioned in previous chapter, $\Gamma(\omega t)$ can be approximated as the first derivative of the voltage waveform. Hence for the tank, $\Gamma(\omega t)$ is given by

$$\Gamma_{tank,eff,RMS}^2 = \frac{1}{2\pi} \int_{-\pi}^{\pi} \Gamma_{tank}^2(\phi) \alpha^2(\phi) d\phi = \frac{1}{2\pi} \int_{-\pi}^{\pi} sin^2(\phi) d\phi = \frac{1}{2} \quad (\mathbf{29})$$

where $\alpha(\phi)$ is the noise modulation function (NMF). The power density of the stationary white noise current induced by the equivalent tank resistance is given as

$$\overline{i_{R_p}^2} = 4k_B T \frac{1}{R_p} \cdot \Delta f. \tag{30}$$

However, since the single-ended switching pair only turns on for half period, the effective noise is then changed to

$$\Gamma_{M_1,eff,RMS}^2 = \frac{1}{2}\Gamma_{tank,eff,RMS}^2 = \frac{1}{4}. \tag{31}$$

The power spectral density of the thermal current noise of M_1 can be express as

$$\overline{\iota_{M_1}^2} = 4k_B T\gamma g_{m,M_1}\Delta f. \tag{32}$$

Similarly, for the constant tail current and power spectral density of the tail current thermal noise,

$$\Gamma_{tail,eff,RMS}^2 = \frac{1}{2}\Gamma_{tank,eff,RMS}^2 = \frac{1}{4} \tag{33}$$

$$\overline{\iota_{tail}^2} = 4k_B T\gamma g_{m,tail}\Delta f. \tag{34}$$

Hence the total phase noise can be calculated as,

$$\begin{aligned}\mathcal{L}_{total}(\Delta\omega) &= 10\log\left(\frac{\Gamma_{rms,drain,eff}^2}{q_{max}^2}\cdot\frac{\frac{\overline{\iota_{R_p}^2}}{\Delta f}}{2\Delta\omega^2}\right)\\ &= 10\log\left(\frac{4k_B T(1+\frac{1}{2}\gamma g_{m,M_1}R_p+\frac{1}{2}\gamma g_{m,tail}R_p)}{\pi^2 R_p^3 I_{tail}^2 C^2(\Delta\omega)^2}\right).\end{aligned} \tag{35}$$

2.3.2.2 LC-VCO with Noise Filter

In [1], Hegazi proposed several VCOs with noise filters. According to his study, for current sources, only thermal noise around second harmonics causes phase noise. Hence, the main purpose of adding noise filters is to filter out second harmonics.

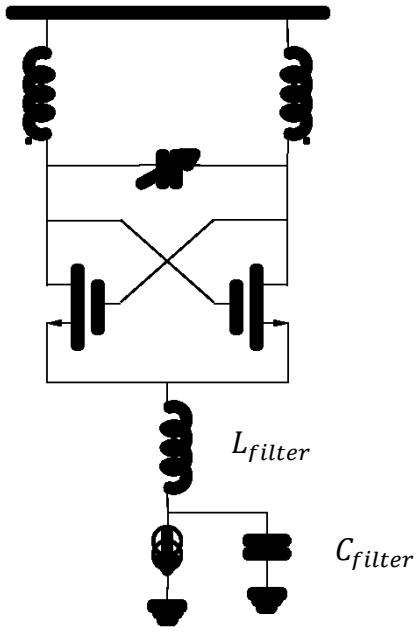


Figure 2.10: LC-VCO with noise filter

no current flowing through the current source. At the same time, even harmonics flow in a common-mode path through the active devices, resonator circuit, and current source.

Because the level of third- and higher-order harmonics in the resonant LC oscillator is negligibly small, the effect of the second harmonic can be taken into account. To prevent the effect of current-source low-noise modulation of the second harmonic, it is critical to provide low impedance for the second harmonic. In other words, it is necessary to create a filter to filter out the second harmonic. Such an approach to phase noise improvement is called a filtering technique. Several filtering techniques have been applied to differential LC-VCOs.

The complete noise filter consists of a tail inductor and a tail capacitor (see Figure 2.10). In a different application, the filter can be implemented with either capacitor only or inductor only.

2.3.2.3 LC-VCO Based on Transformer Feedback

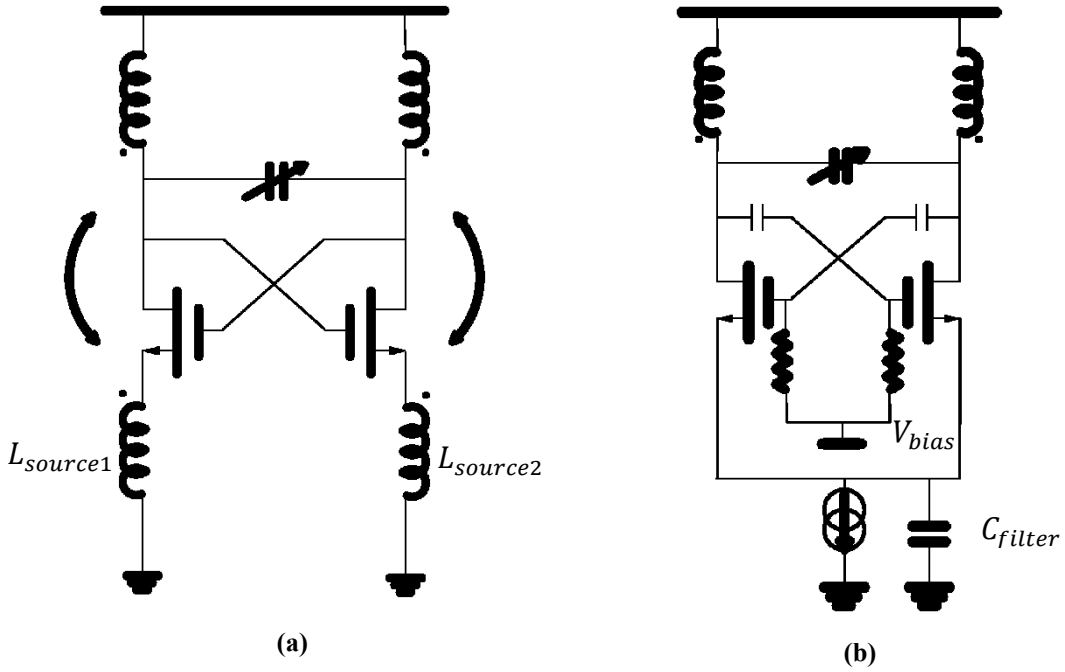


Figure 2.11: (a) LC-VCO based on transformer feedback. (b) Class-C VCO

In [18], the author proposed a VCO topology based on transformer feedback. Using a transformer can enlarge the voltage headroom, which is highly beneficial under low-voltage supply conditions. The output voltage swing may also be enlarged, producing lower phase noise.

The circuit can also work like a Colpitts oscillator, namely the conduction angles of the transistors are decreased, which results in the reduction of effective noise. This also contributes to a better phase noise performance.

2.3.2.4 Class-C VCO

Class-C VCO has become popular recently. Many studies have examined class-C VCO in [6 - 21]. Figure 2.11(b) shows one very widely used class-C topology.

The main idea of class-C VCO is to make the transistors work in the class-C mode, namely shape the injected current into tall, narrow pulses. Class-C operation allows for larger current delivery efficiency. Achieving high efficiency in oscillators is

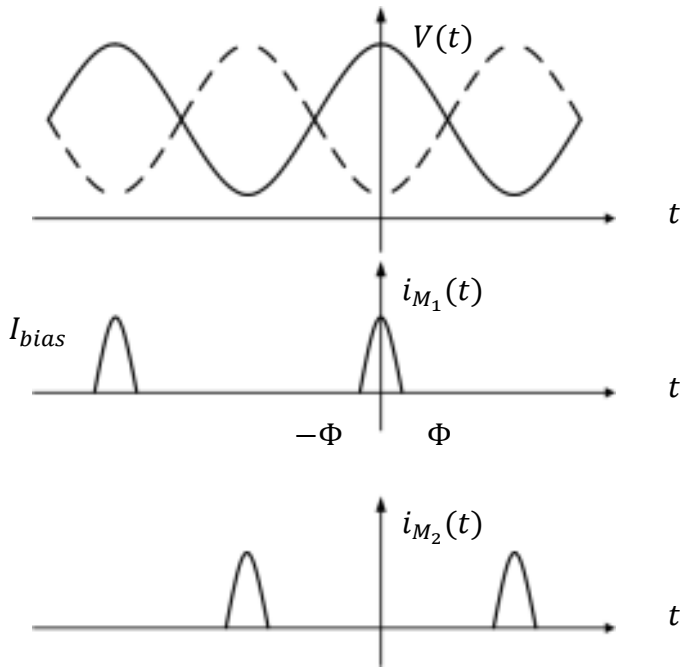


Figure 2.12: Time domain waveforms for class-C VCO.

beneficial for increasing battery life, reducing heat dissipation and enhancing reliability of both measurement equipment and radio transmitters. What's more, it maximizes the oscillation amplitude. At the same level of power consumption, phase noise can be improved by 3.9 dB theoretically. In other words, to achieve the same phase noise level, more than 50% of the current can be saved [6].

The time domain waveforms are shown in Figure 2.12. Assume the conduction angles of transistors are 2Φ ($\Phi < \frac{\pi}{2}$), according to [8], the amplitude can be given as

$$V_{peak} \approx 2I_1R_p \approx 2I_{tail}R_p \tag{36}$$

where $\Gamma(\omega t)$ and noise power density of the tank is identical to (29)(30) respectively. The NMF $\alpha(\phi)$ from the switching pair is

$$\alpha(\phi) = \sqrt{\cos(\phi) - \cos(\Phi)}. \tag{37}$$

Hence ISF for a single end is given by

$$\Gamma_{M_1,eff,rms}^2 = \frac{1}{2\pi}\int_{-\Phi}^{\Phi}\frac{1}{4}sin^2(\phi)(\cos(\phi)-\cos(\Phi))d\phi. \quad (38)$$

Using Taylor expansion,

$$\Gamma_{M_1,\text{eff,rms}}^2 \approx \frac{1}{8\pi}\cdot\frac{2}{15}\Phi^5\left(1-\frac{11}{42}\Phi^2\right)\approx\frac{\Phi^5}{60\pi}. \quad (39)$$

For a single-ended transistor, the instantaneous transconductance of M_1 is,

$$g_m(\phi) = \beta V_{peak}(\cos(\phi)-\cos(\Phi)). \quad (40)$$

therefore

$$I_{tail} = 2\cdot\frac{1}{2\pi}\int_{-\Phi}^{\Phi}\frac{\beta {V_{peak}}^2}{2}(\cos(\phi)-\cos(\Phi))^2 d\phi \approx \frac{\beta {V_{peak}}^2}{15\pi}\Phi^5. \quad (41)$$

After transformation,

$$\Phi = \left(\frac{15\pi}{\beta {V_{peak}}^2}\frac{I_{tail}}{2}\right)^{1/5}. \quad (42)$$

Substitute (42) into (39) , given,

$$\Gamma_{M_1,\text{eff,rms}}^2 = \frac{I_{tail}}{8\beta {V_{peak}}^2}. \quad (43)$$

Hence the total phase noise is,

$$\mathcal{L}_{total}(\Delta\omega) = 10\log\left(\frac{\Gamma_{rms,drain,eff}^2}{q_{max}^2}\cdot\frac{\overline{\frac{i_{R_p}^2}{\Delta f}}}{2\Delta\omega^2}\right)$$

$$= 10\log\left(\frac{2k_BT(1+\gamma g_{m,M_1}\ R_p+\frac{1}{2}\gamma g_{m,tail}R_p)}{R_p^3 I_{tail}^2 C^2(\Delta\omega)^2}\right). \quad (44)$$

2.3.2.5 Other Technique and circuits

In [26], Soltanian proposed a tail current shaping technique. Starting with the mathematical derivation, the author gave a conclusion that narrower tail current pulses lead to less phase noise. Ideally, if the conduction angle of the switching pair approaches 0, the phase noise can be improved by 9.1dB.

Hence, to reduce the conduction angle, a peak detector is added to detect the peaks and control the tail current periodically (see Figure 2.14). In fact, this circuit can be viewed as another version of class-C VCO with square shape current pulses.

The amplitude of the output voltage is given by

$$V_{peak} \approx\ sinc\left(\frac{\Phi}{\pi}\right) I_{tail}R_p. \quad (45)$$

NMF is

$$\alpha(\varphi) = \frac{\phi}{2\Phi}. \quad (46)$$

Hence

$$\Gamma_{M_1,eff,rms}^2 = \frac{1}{2\pi}\left(\Phi - \frac{1}{2}\sin(2\Phi)\right). \quad (47)$$

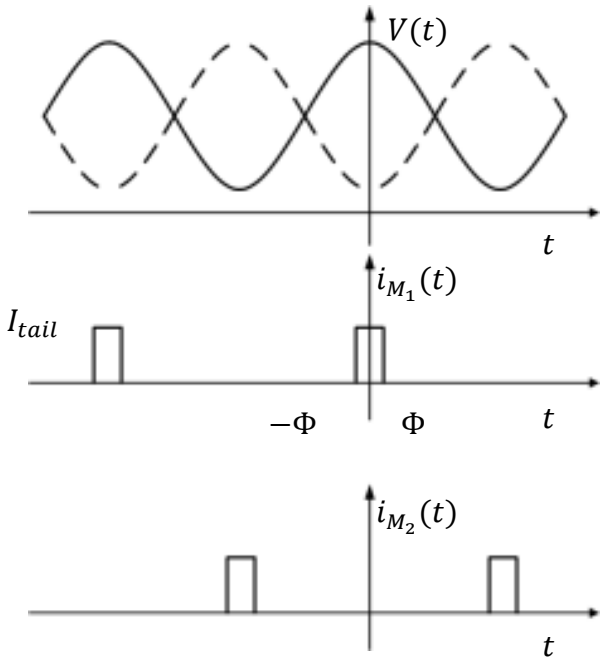


Figure 2.13: Time domain waveforms for VCO using tail current shaping technique.

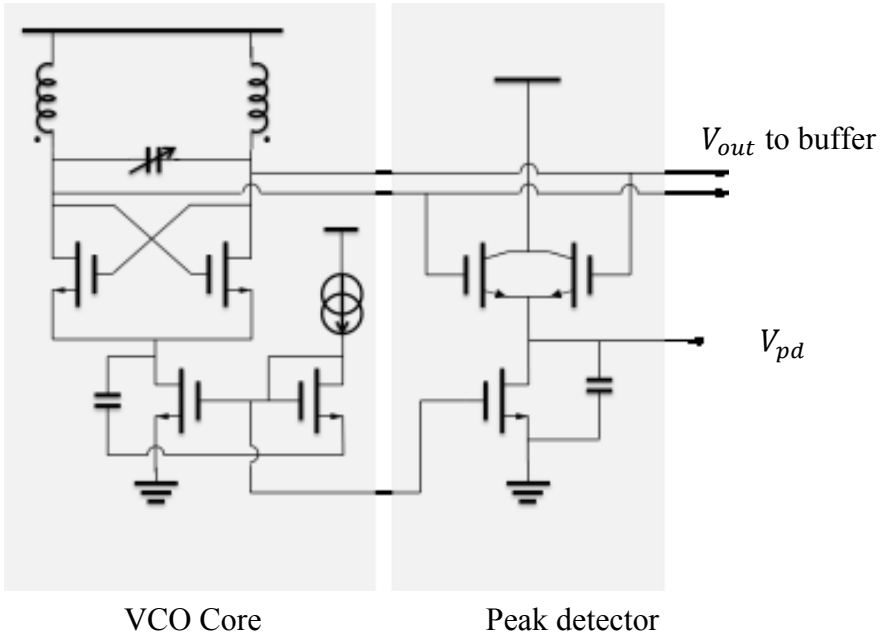


Figure 2.14: Schematic of the fabricated VCO2 core and differential bipolar peak detector.

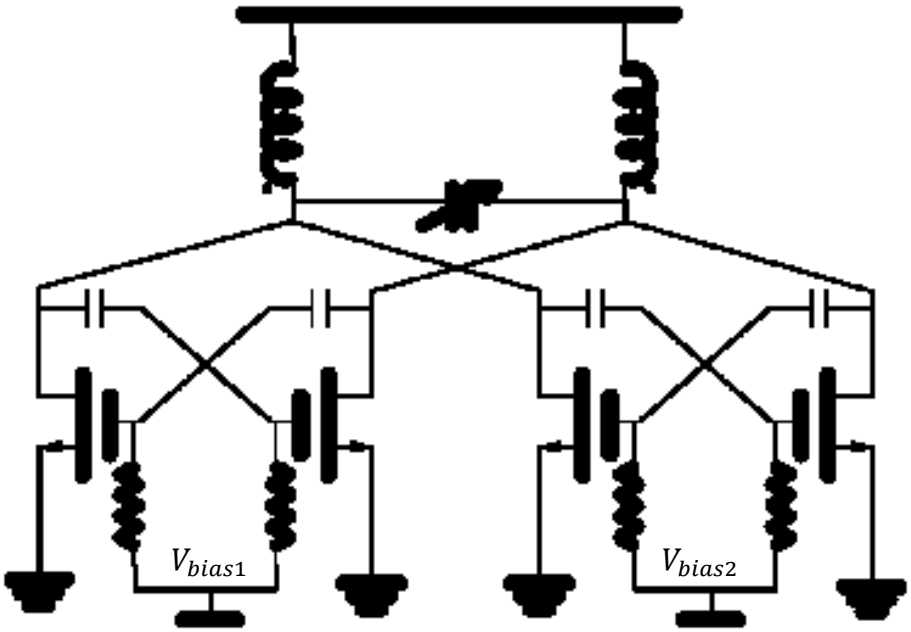


Figure 2.15: Dual-Conduction class-C VCO

Phase noise is therefore given by,

$$\mathcal{L}_{total}(\Delta\omega) = 10\log\left(\frac{\Gamma_{rms,drain,eff}^2}{q_{max}^2}\cdot\frac{\frac{\overline{i_{R_p}^2}}{\Delta f}}{2\Delta\omega^2}\right)$$

$$= 10\log\left(\frac{4k_BT(1+\gamma g_{m,M_1}\frac{\Phi-\frac{1}{2}\sin(2\Phi)}{\sqrt{2\pi\Phi}}+\gamma g_{m,tail}R_p\frac{\Phi-\frac{1}{2}\sin(2\Phi)}{2\Phi})}{\pi^2R_p^3I_{tail}^2C^2(\Delta\omega)^2}\right). \quad (48)$$

Another interesting circuit is proposed by Okada in [23]. The circuit is designed with super low voltage supply of 0.2V. The circuit employed dual class-C operation. One branch is designed with comparatively large conduction angle to ensure robust startup, while the other branch is designed with smaller conduction angle to reduce effective

noise (see Figure 2.15). The circuit achieved ultra-low power consumption; however the trade-off is a less favorable phase noise performance.

2.4 Conclusion

This chapter reviews the VCO theory, including linear and non-linear approaches as well as circuit examples from literatures It turned out although many attempts have been made to predict the phase noise performance and some of them have achieved quite precise prediction, the existing circuits showed weak connections to these theory, namely those theory, are not insightful enough to guide a practical VCO design. Hence, finding insight for low noise VCO designs becomes the first target of this thesis.

3 Chapter: Proposed VCO Topology

3.1 Introduction

This chapter first presents a study on phase noise generation. The study begins by examining the relation between phase noise and harmonics. However, simulation results show that harmonics are not the only factor to determine the phase noise. After studying the mechanism of the generation of phase noise, it is found that the phase noise is determined by the transfer function and harmonic components of the circuit. Hence a VCO design guideline has been concluded to guide VCO design. Based on this research, a novel VCO topology is proposed. Experiments are carried out on the proposed circuit with two other reference topologies to verify the circuit's ability to reduce the transfer function and harmonics, which yields better phase noise performance.

3.2 Study on Relation between Phase Noise and Harmonics

According to the energy definition of the quality factor, in an ideal lossless tank,

$$Q = \omega \frac{E_{stored}}{E_{diss}} \to \infty. \tag{49}$$

given

$$\Delta\omega_{3dB} = \frac{\omega_c}{Q} \to 0. \tag{50}$$

In reality, however, Q of a tank is not infinite. Phase noise and harmonic components are thus unavoidable. Therefore it is reasonable to assume that harmonics cause or partially cause the phase noise.

Researchers have studied the relation between phase noise and harmonics [33–35]. In 1933, Groszkowski mathematically proved that the presence of harmonics in the tank current of a LC-VCO, which induced by the nonlinearity of the circuit, results in a shift of the oscillation frequency from the tank resonance frequency in [35]. This shift is shown in,

$$\frac{\Delta\omega}{\omega_0} = -\frac{1}{2Q^2}\sum_{n=2}^{\infty} a_k n_k^2 \tag{51}$$

where a_k being a coefficient depends on the topology and

$$n_k = \frac{I_k}{I_1} \tag{52}$$

where I_k is the amplitude of the kth harmonic of the tank current. If any noise changes n_k, a spurious frequency modulation will arise and then low frequency noise will be upconverted into phase noise sidebands [36]. Also, in [1], the authors demonstrated that by adding filters on VCOs, second harmonics will be filtered out, and phase noise is consequently decreased. While these researchers all discussed the relation between phase noise and harmonics, no study has reportedly examined the relationship.

Therefore, in this thesis, the research begins with examining the relationship. A VCO with a filter (see Figure 3.1) has been employed to research the relationship. The filter can be adjusted by tuning the inductor, which yields different harmonic components.

After many experiments, it was found that the third harmonic is of most importance. This matches the results demonstrated in [33]. Even order harmonics are absent because of the symmetry of the circuit. Other harmonics that are higher than the third harmonics are relatively small and can be ignored. This is because the filtering

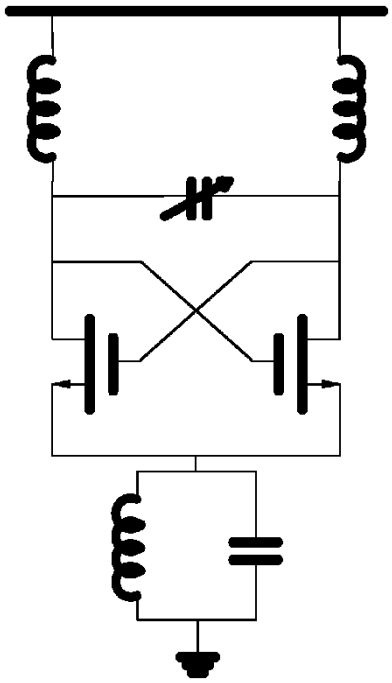


Figure 3.1: VCO with tunable filter.

effect of the tank circuit. Therefore, the Total Harmonic Distortion (THD) can be approximated by,

$$\text{THD} \cong \frac{V_{3rd}}{V_{1st}} \tag{53}$$

where V_{3rd} is the voltage amplitude of third harmonics in the differential output signal, and V_{1st} is the voltage amplitude of the fundamental component. Using $L_{tank} = 2nH, C_{tank} = 2pF,$ Figure 3.2– Figure 3.4 shows the phase noise performance with various inductances of the filters.

From the simulation results, it can be observed that the predicted trend is confirmed, namely higher THD has the tendency to produce more phase noise. However, these results indicate that the phase noise performance may not only depend on harmonics.

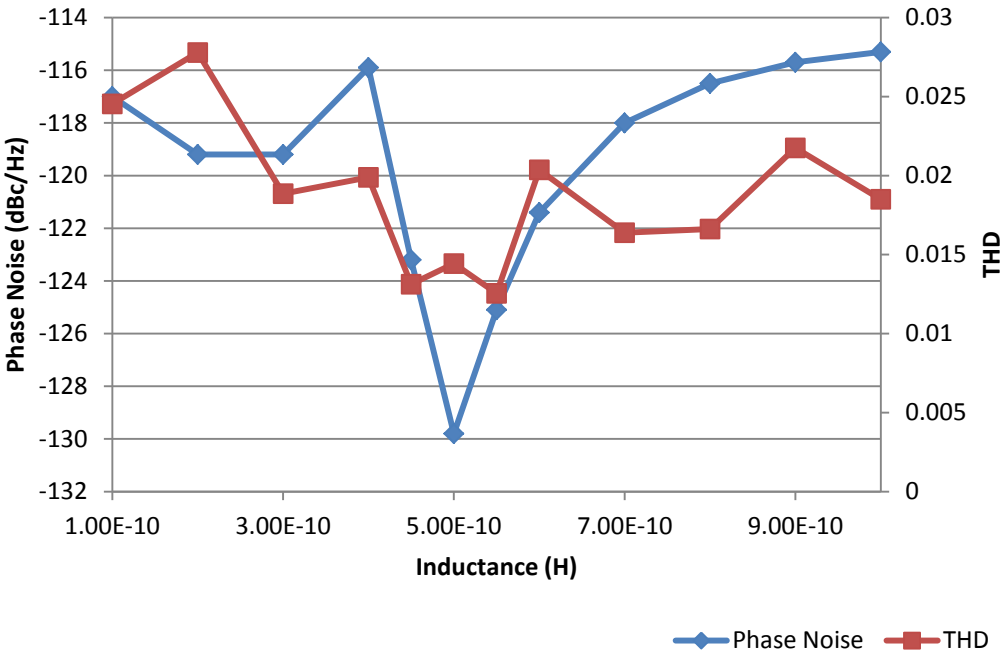


Figure 3.2: Simulation results for the phase noise performance with different harmonics when C=2pF.

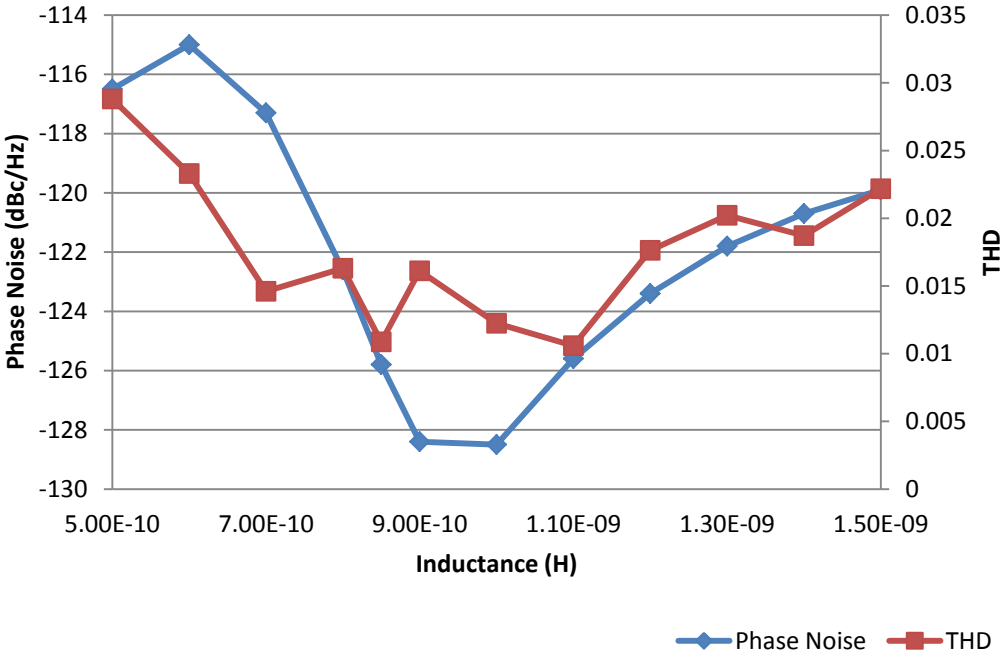


Figure 3.3: Simulation results for the phase noise performance with different harmonics when C=1pF.

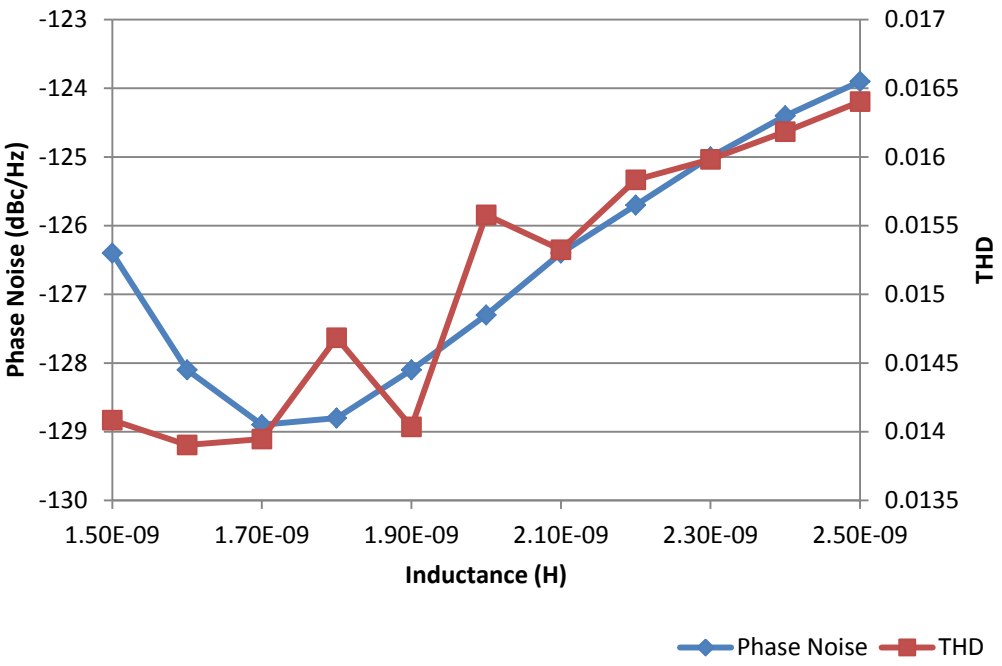


Figure 3.4: Simulation results for the phase noise performance with different harmonics when C=0.5pF

3.3 Generation of Phase Noise

To discover the other factor that determines the phase noise, the mechanism of the generation of phase noise is explored first.

Here only white noise is analyzed. Flicker noise is ignored because low frequency noise will be filtered out by the PLL loop in VCO implementations. Hence, the noise power spectral density of the noise source should be nearly constant throughout the frequency spectrum ideally. According to the Nyquist theorem, the noise spectrum $S_v(\omega)$of the circuit is related to the real part of the impedance. The noise power spectrum is therefore modified by the circuit by

$$S_v(\omega) = 2kT \cdot \mathrm{ReZ}(j\omega). \tag{54}$$

To observe a general case, the circuit can be simplified by connecting an independent current source $n_i(t)$ (noise), a noiseless resistor R and a network containing

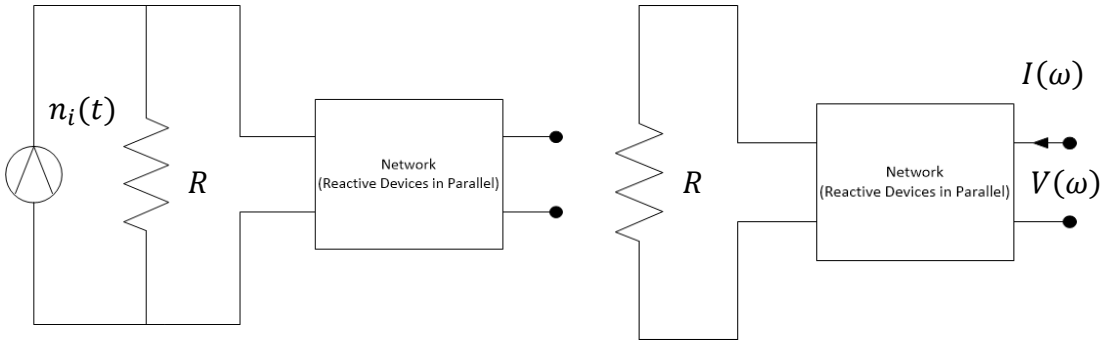


Figure 3.5: Black box model for oscillators [37].

only reactive devices in parallel (see Figure 3.5). Thus, the system transfer function $H(\omega)$ is equal to

$$H(\omega) = \frac{V(\omega)}{I(\omega)} \tag{55}$$

where $V(\omega)$ and $I(\omega)$ represent the amplitude of the voltage across the resistor and $I(\omega)$ represents the amplitude of the input sine wave current. Because the circuit is assumed to be noiseless, the input power is equal to the output power, given

$$|I(\omega)|^2 \cdot \mathrm{ReZ}(j\omega) = \frac{|V(\omega)|^2}{R}. \tag{56}$$

By substituting equation (55) with quation (56), we obtain

$$S_v(\omega) = S_{n_i}(\omega) \cdot |H(\omega)|^2, \tag{57}$$

$$S_{n_i}(\omega) = \frac{2kT}{R}. \tag{58}$$

Note that equations (3.4)–(3.8) are cited from [37].

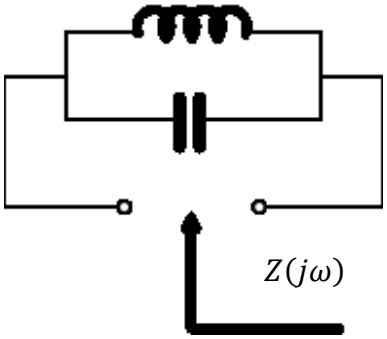


Figure 3.6: LC resonator.

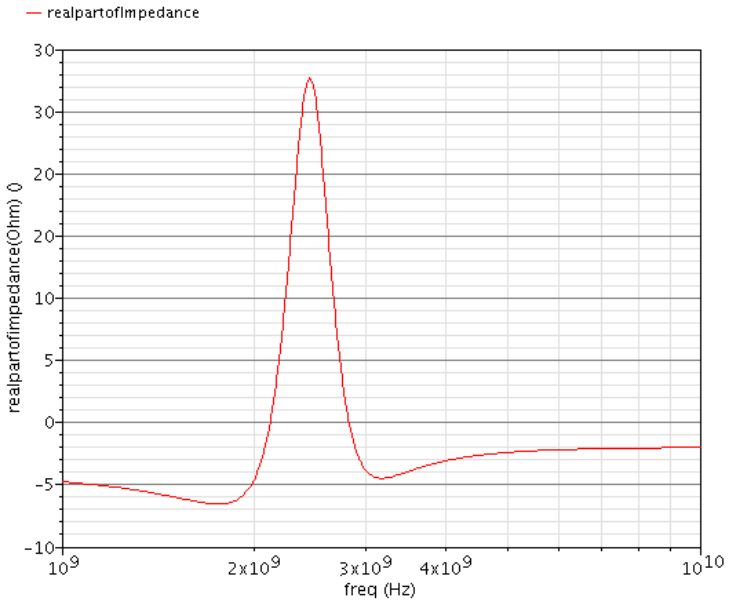


Figure 3.7: Impedance of a LC-VCO (example).

In LC-tank VCOs, the network in Figure 3.5 should be a LC tank (see Figure 3.6). In an ideal LC circuit, at resonant frequency f_c, where

$$f_c = \frac{1}{2\pi\sqrt{LC}}, \tag{59}$$

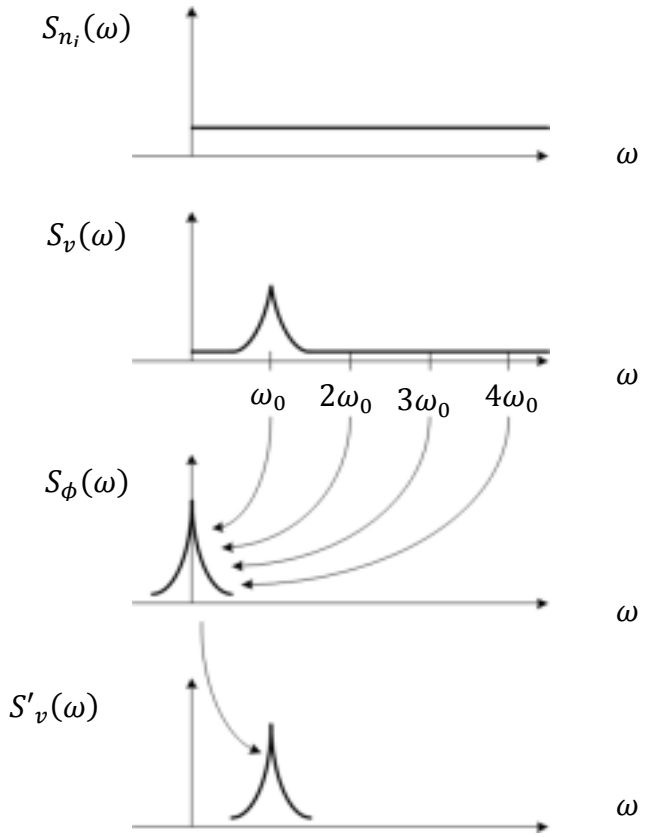


Figure 3.8: Conversion of noise to phase noise

and the real part of the impedance looking into the tank (see Figure 3.6), Re$Z(j\omega)$, approaches infinity since

$$Z(j\omega) = \frac{1}{\frac{1}{Z_c} + \frac{1}{Z_L}} = \frac{1}{\frac{1}{j\omega L} + j\omega C} = \frac{1}{0} \to \infty. \tag{60}$$

In reality, due to the existence of parasitic resistance, the tank cannot be simplified into a LC resonator. The impedance at the resonant frequency is finite, and the shape of the impedance is pulse-like. Figure 3.7 gives an example of the impedance of a LC-VCO. According to the equation (54), the noise power spectral density should share the same shape as that of the impedance.

However, because of the nonlinearity, there are always harmonic components existing in an oscillator. These harmonics will, in turn, mix with the noise. Recall the frequency mixing equations between the two signals $A_1\cos(\omega t)$ and $A_2\cos(vt)$,

$$v_{out} = A_1\cos(\omega t)\cdot A_2\cos(vt) = \frac{A_1A_2}{2}\left[\cos\big((\omega+v)t\big)+\cos\big((\omega-v)t\big)\right]. \quad (61)$$

The sum and difference frequencies will be produced when these two signals are mixed. In this case, noise around the integer multiples of the oscillating frequency is down-converted into low frequency noise sidebands by the harmonics. Namely, the energy around the harmonics is taken down by the harmonics, accumulating around dc. Then noise around DC will then be up-converted by the fundamental frequency, forming the phase noise sidebands around the carrier. Phase noise is then generated. The whole process is illustrated in Figure 3.8.

3.4 LC-VCO Design Guideline

Studies of the generation of phase noise benefit designing low phase noise VCOs. In previous studies, some LC-VCO design guidelines for low phase noise VCOs can be achieved through those VCO models. For example, from Leeson's empirical equation (10), it can be concluded that one should maximize the Q factor and maximize the power of the output signal to minimize phase noise.

From the mixer model mentioned in Chapter 2.2.4 (see equation (19)), it can be concluded that regardless of what topology is used to reduce phase noise, the voltage amplitude of the output signal should be maximized, while the noise factor should be minimized. The noise factor is dependent on the dimension of the active devices. However, the voltage amplitude of the output signal and the noise factor are not always orthogonal. Usually, larger amplitude is achieved by enlarging g_m of the active devices, but enlarging g_m will in turn change the noise factor. Whether it increases the noise factor depends on real case calculations.

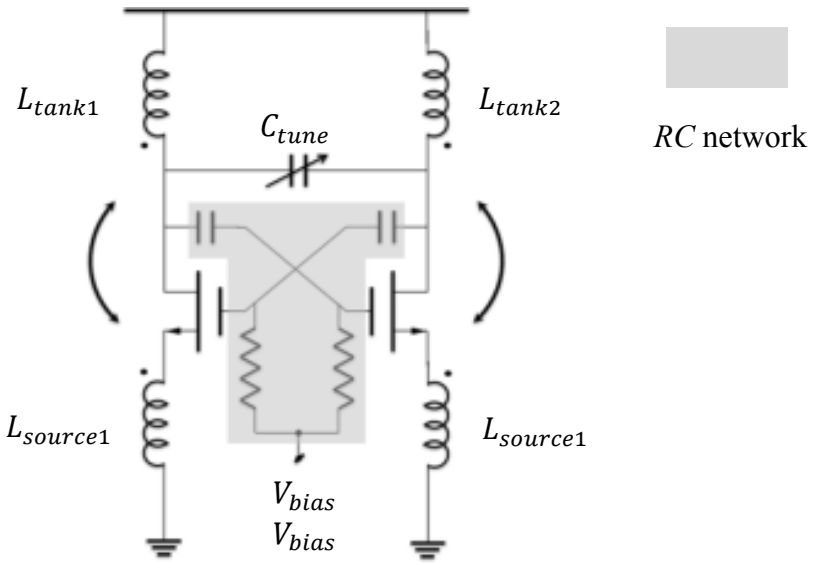


Figure 3.9: Schematic for proposed VCO

From Hajimiri's ISF theory (see equation (21)), it can be observed that one way to reduce the phase noise is to increase the maximal charge across the tank. This method can be achieved by enlarging the voltage amplitude because the charge is proportional to the voltage amplitude. Another away to reduce phase noise is by decreasing the Γ_{rms}^2. However, decreasing Γ_{rms}^2 is not intuitive, which makes the theory less practical in guiding VCO design [6].

In this thesis, the analysis in the previous chapter reveals the link between the phase noise and nonlinearity of the circuit, which is, the phase noise performance of an oscillator is determined by the presence of noise and harmonic components of the circuit. This conclusion serves to guide the design of oscillators with low phase noise.

First, regardless of the harmonics, when the noise source remains the same, the lesser the noise amplitude is, the better the phase noise performance is. According to (57), noise spectral density is proportional to the square of the noise to output transfer function. Therefore, if the magnitude of the transfer function is reduced or narrower bandwidth, the presence of noise of the oscillators can be proven.

Second, regardless of the presence of noise, if one can enlarge the fundamental component and suppress higher harmonics, less noise would be converted around the carrier. The phase noise performance is in turn improved.

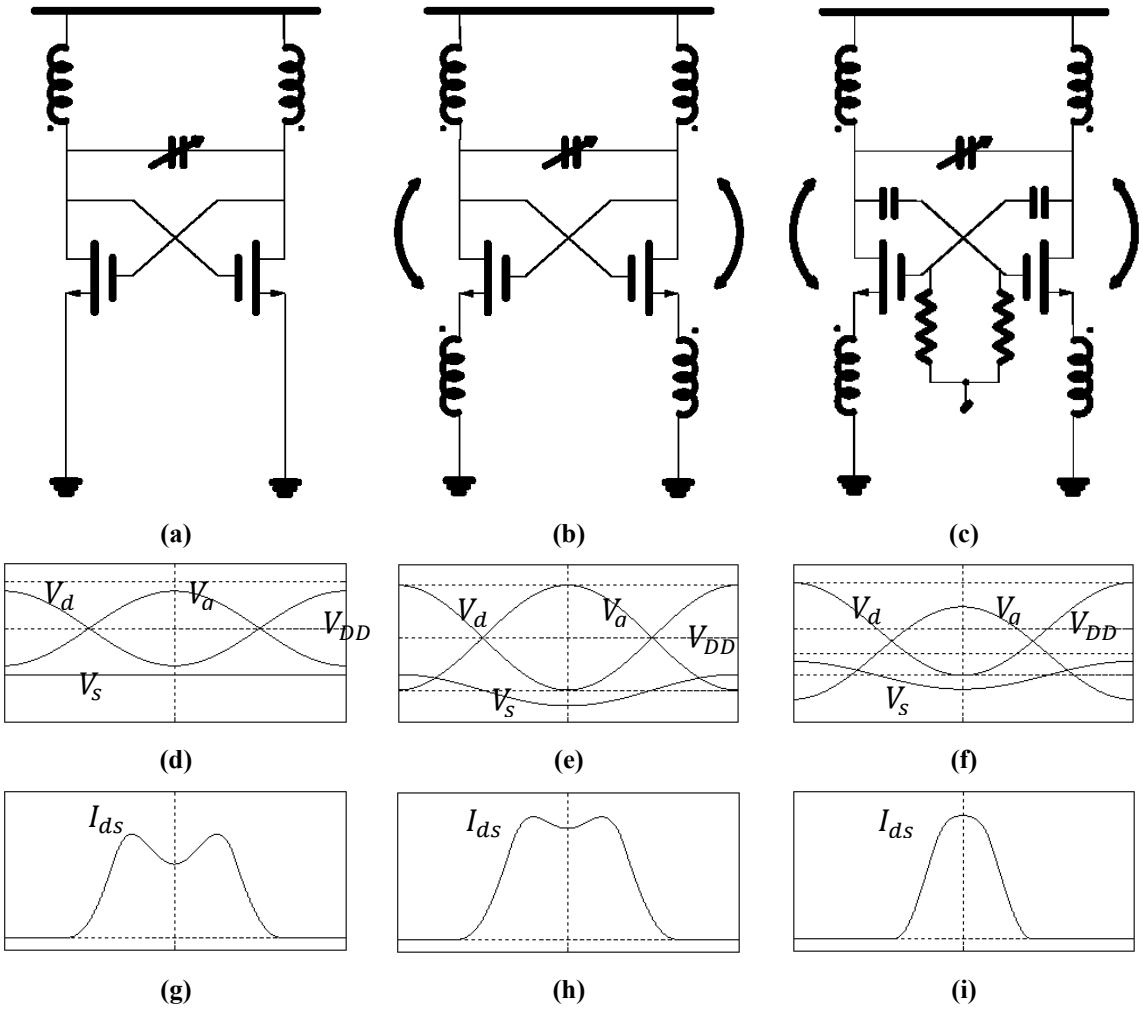


Figure 3.10: Topology for (a) VCO1 (b) VCO2 (c) VCO3 (Proposed). (d)(e)(f) show voltage waveform in time domain for three VCOs. (g)(h)(i) show injected current in time domain.

Overall, better phase noise performance can be achieved by reducing either the presence of noise or the harmonic components, or both. It should be noted that the such design guideline is concluded under the condition that flicker noise is ignored.

3.5 Proposed VCO Topology

Following the conclusion in the previous chapter, it can be easily concluded that an ideal candidate VCO circuit should minimize both transfer function and harmonics. Among the circuits that have been reviewed in Chapter 2, VCOs with noise filter and transformer feedback VCOs made efforts to reduce the harmonics—the former tried to filter out the second harmonics, while the latter provided more voltage headroom, which in turn

reduced the nonlinearity. However, no effort has been made to modify the transfer function directly.

Therefore, a new VCO topology has been proposed to achieve better phase noise performance (see Figure 3.9). The circuit can be interpreted as adding transformers and an RC feedback network onto the simplest LC-tank VCO (see Figure 3.10(a)). The RC network is highlighted in the figure.

As with the transformer feedback VCO, the aim of adding transformers is primarily to reduce the harmonics. By coupling inductors $L_{source1}$ and $L_{source2}$ to tank inductors L_{tank1} and L_{tank2}, respectively, in time domain, voltage at the source node of the transistors V_s becomes variant instead of remaining at 0V in the simplest VCO topology (see Figure 3.10(a)). This provides two advantages. First, it provides more voltage headroom, which enlarges the fundamental component in the output signal. Second, through careful design, the current injected into the tank can be shaped closer to sinusoidal (see Figure 3.10 (i)). Using the negative resistance model (see Figure 2.2), the shape of the voltage across the tank will be closer to sinusoidal, producing fewer harmonics.

The main purpose of adding the *RC* feedback network is to modify the transfer function. This method can be considered as adding *RC* filters in the feedback network. By setting appropriateV_{bias}, the feedback gain can be reduced. The bandwidth of transfer function will become much smaller.

3.6 Simulation

Here, three VCOs are compared. Topologies are shown as above [Figure 3.10 (a)–(c)]. VCO1 is the simplest VCO topology, VCO2 employs transformers only (without the RC feedback network), and VCO3 is the proposed topology. The same tank is employed in three circuits to ensure similar quality factors. Supply voltage is also kept identical. Transformers in VCO2 and VCO3 are the same, which also presents the same coupling factors to the tank inductors.

To explore how much the proposed circuit may benefit the phase noise performance, two experiments were carried out. Experiment I is designed to show how

Table 2: Parameters for Experiment I

	VCO1	VCO2	VCO3
Supply Voltage (V)	0.5	0.5	0.5
$L_{tank1,2}$ (nH)	2	2	2
$C_{tank1,2}$ (pF)	2	2	2
$R_{tank1,2}$ (ohm)	2	2	2
W/L	26um/120nm	26um/120nm	26um/120nm
$L_{source1,2}$ (nH)	0.6	0.6	0.6
$R_{source1,2}$ (ohm)	0.6	0.6	0.6
Coupling Coefficient	-	0.4	0.4
$R_{filter1,2}$ (Mohm)	-	-	100
$C_{filter1,2}$ (pF)	-	-	10

Table 3: Parameters for Experiment II

	VCO1	VCO2	VCO3
Supply Voltage (V)	0.5	0.5	0.5
$L_{tank1,2}$ (nH)	2	2	2
$C_{tank1,2}$ (pF)	2	2	2
$R_{tank1,2}$ (ohm)	2	2	2
W/L	22um/120nm	12um/120nm	26um/120nm
$L_{source1,2}$ (nH)	0.6	0.6	0.6
$R_{source1,2}$ (ohm)	0.6	0.6	0.6
Coupling Coefficient	-	0.4	0.4
$R_{filter1,2}$ (Mohm)	-	-	100
$C_{filter1,2}$ (pF)	-	-	10

this topology would influence the transfer function and harmonics when the noise sources are the same. To keep the noise source the same, identically sized active devices are

employed in the three circuits. However, this would make the output amplitude of the three circuits different from each other. Therefore, another experiment, Experiment II, is designed to show how this topology would influence the transfer function and harmonics when the output amplitude is kept the same for the three circuits. Active devices in the three circuits are adjusted to give the same output amplitude, which is 2.0V for peak-to-peak voltage of the differential voltage output. Parameters for Experiment I and Experiment II are shown in Table 2, respectively.

As aforementioned, the main goal of adding transformers is to reduce the harmonics. Therefore, the harmonics difference in VCO1 and VCO2 are mainly compared, as the transformer is the only difference between the two topologies. A large improvement in suppressing harmonics should be obtained in VCO2 as compared with VCO1 in both experiments. For transfer function, results for VCO2 and VCO3 and mainly focused on how the *RC* feedback network benefits. A transfer function with much narrower bandwidth and lower peak amplitude should be obtained in VCO3 when compared with VCO2.

In both experiments, harmonics are obtained first, using the Fast Fourier Transformation (FFT) analysis. For transfer function, instead of using the traditional method, which breaks the loop and calculates the open loop transfer function directly, the Middlebrook method is used to obtain a more accurate result. It is important to note that before this thesis, no study has reported utilizing the Middlebrook method on differential VCOs. Details about the advantages of this method and its implementation are introduced in Appendix A. Here, only the results are presented.

It should be noted that the Middlebrook method can only simulate white noise spectrum. To exclude the influence from flicker noise, flicker noise is turned off first in the simulator to explore how harmonics and transfer function affect phase noise performance from Chapter 3.6.1 to 3.6.3. In Chapter 3.6.4, flicker noise is turned on again in Spectre to see the phase noise performance in the proposed circuit when flicker noise is taken into account.

3.6.1 Harmonics

Table 4: Simulation results for Harmonics for Experiment I

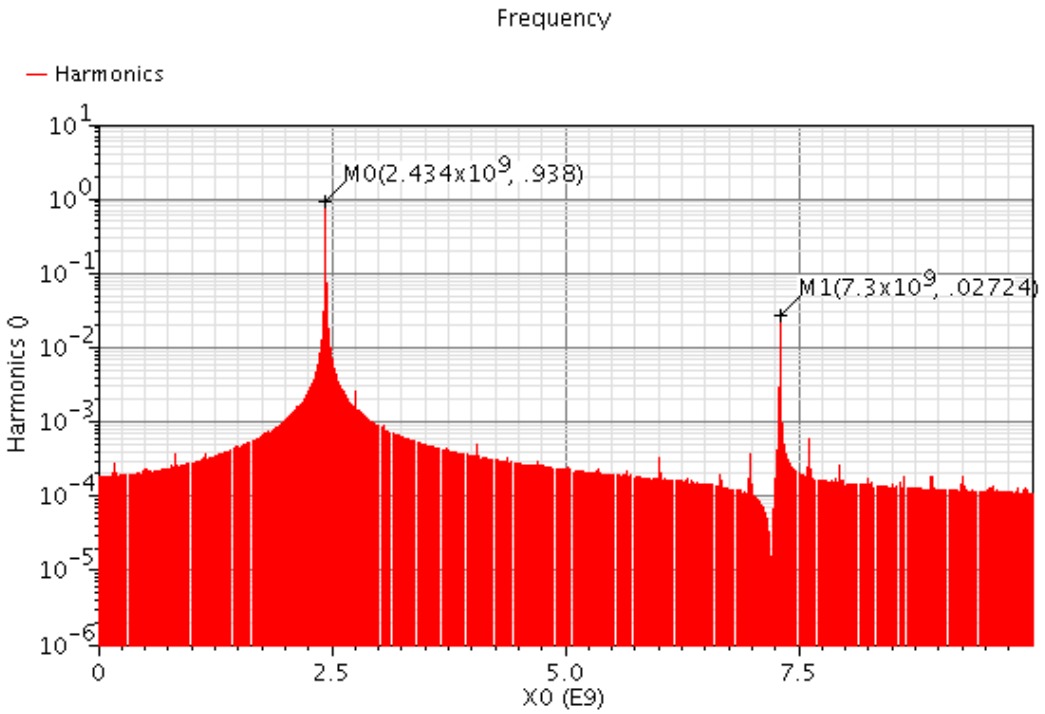
	Fundamental (V)	2nd Harmonics(V)	3rd Harmonics (V)	THD
VCO1	0.938	-	0.02724	0.0290
VCO2	0.847	-	0.01802	0.0213
VCO3	1.054	0.0091	0.00722	0.0110

Table 5: Simulation results for Harmonics for Experiment II

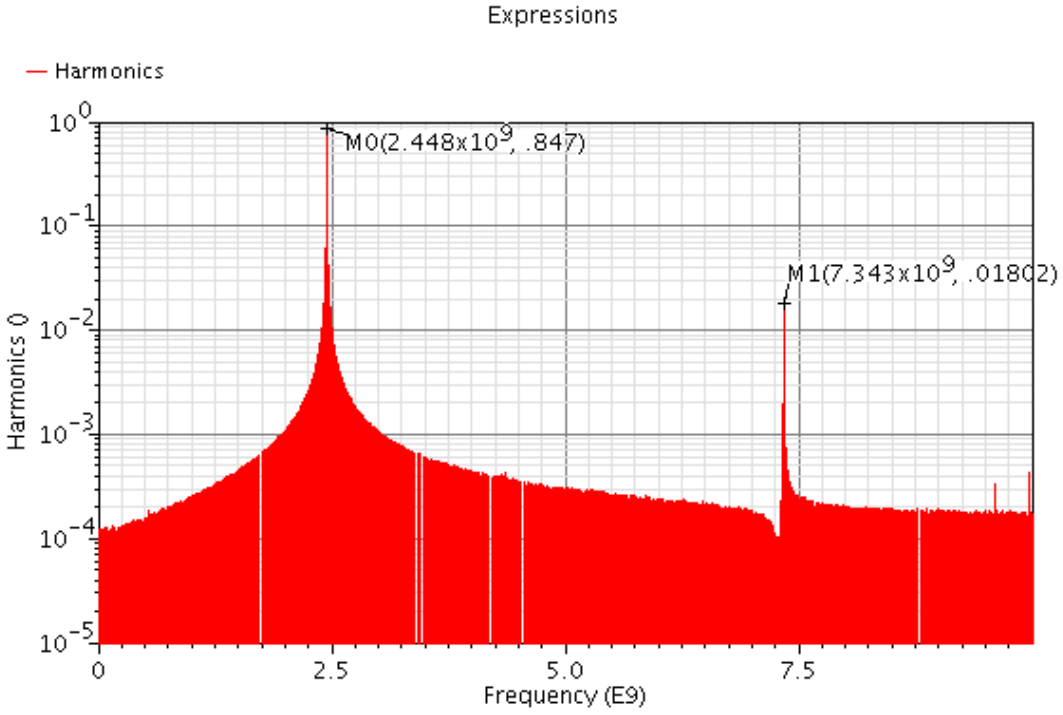
	Fundamental (V)	2nd Harmonics(V)	3rd Harmonics (V)	THD
VCO1	0.8415	-	0.01692	0.0201
VCO2	0.9226	-	0.00583	0.0063
VCO3	1.054	0.0091	0.00722	0.0110

Harmonics from the differential output of the three topologies in Experiment I and Experiment II are shown in Figure 3.11 and Figure 3.12, respectively. The conclusion of the harmonics components are shown in Table 4 and Table 5. Note that the fundamental frequencies of the three circuits change slightly, as VCO2 and VCO3 introduce extra components (e.g. inductors), resulting in shifts in center frequencies. Furthermore, voltage harmonics under 10^{-4}V are ignored. Therefore, harmonics that are higher than fourth harmonics are ignored.

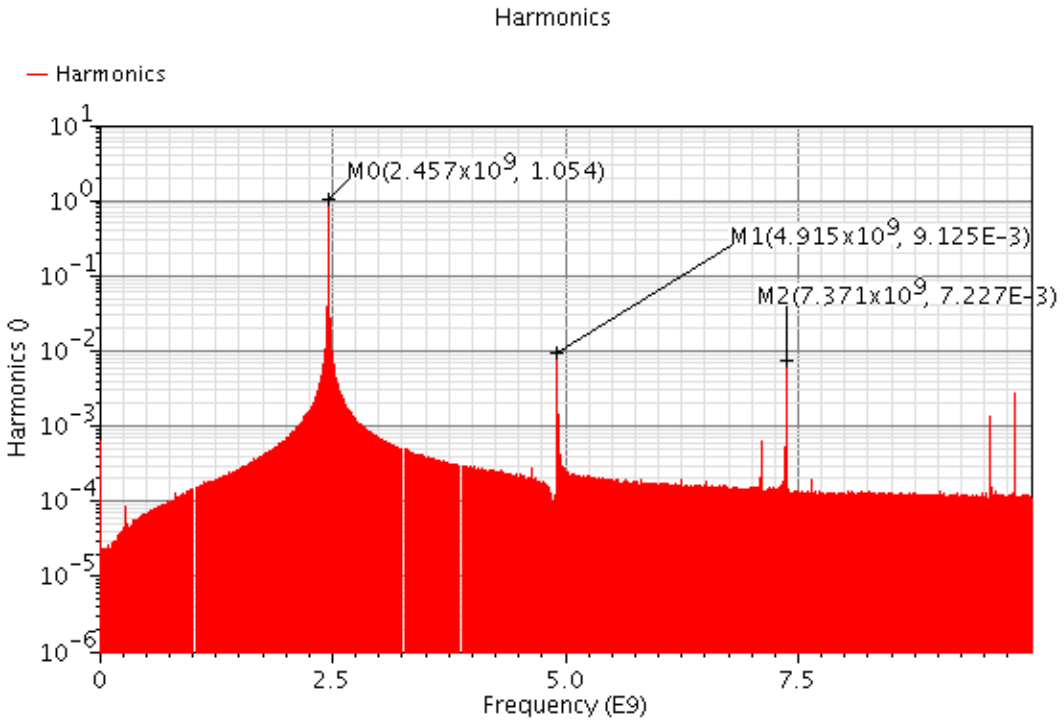
In Experiment I, third harmonics are dominant in VCO1 and VCO2. Although VCO2 did not suppress the absolute value of the third harmonics; it efficiently enlarges the fundamental component. The value of THD is reduced by 26.5%. This shows that the transformer suppresses the harmonics. In VCO3, despite the fact that second harmonics are introduced, it still successfully suppressed the third harmonics and increased the fundamental component at the same time. The THD value is slightly higher than it is in VCO2. Because the only difference between VCO2 and VCO3 is the *RC* feedback network, it can be conjured that the harmonic variation in VCO2 and VCO3 is caused by the *RC* feedback network; however, the variation is very small.


Frequency
Harmonics
M0(2.434x10^9, .938)
M1(7.3x10^9, .02724)
Harmonics 0
X0 (E9)

(a)

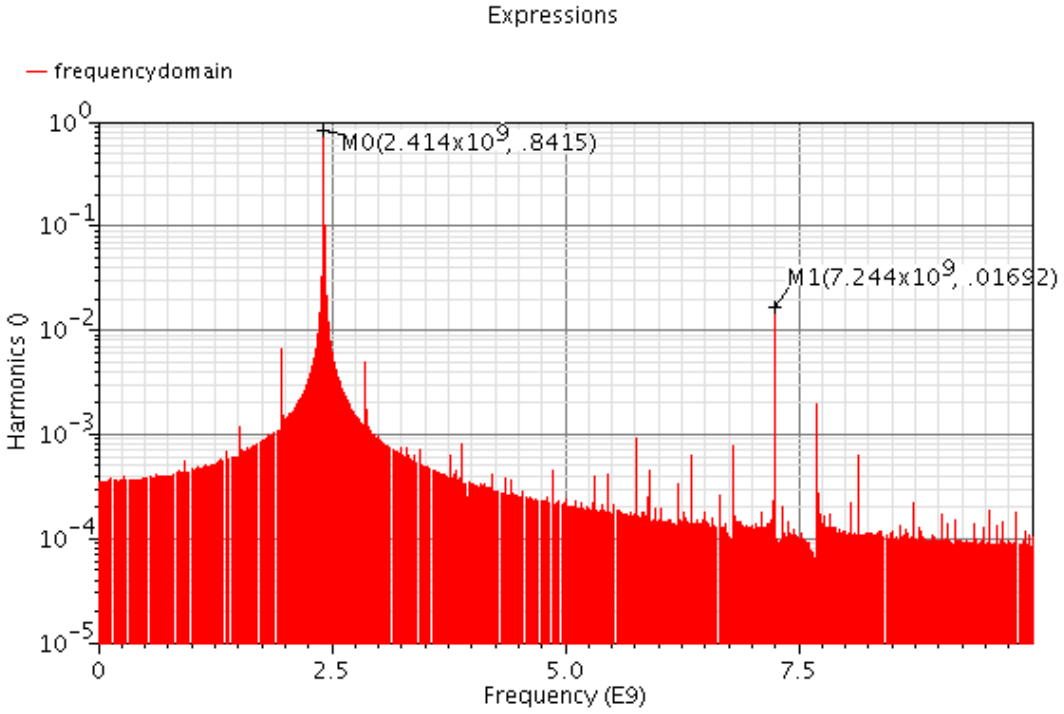

Expressions
Harmonics
M0(2.448x10^9, .847)
M1(7.343x10^9, .01802)
Harmonics 0
Frequency (E9)

(b)

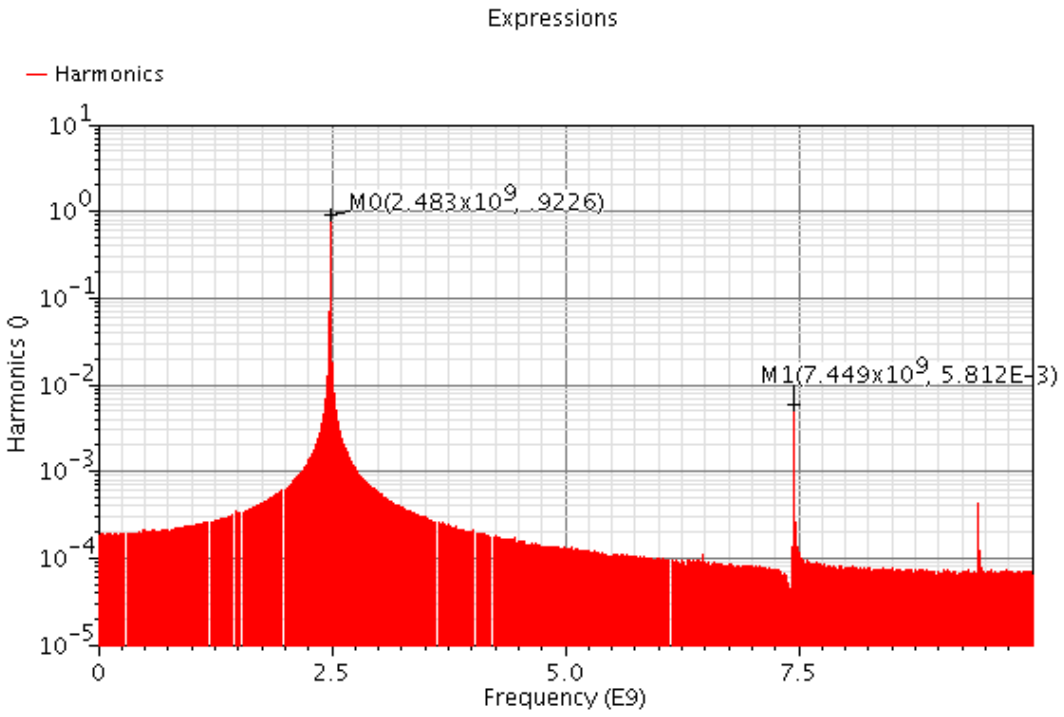


(c)

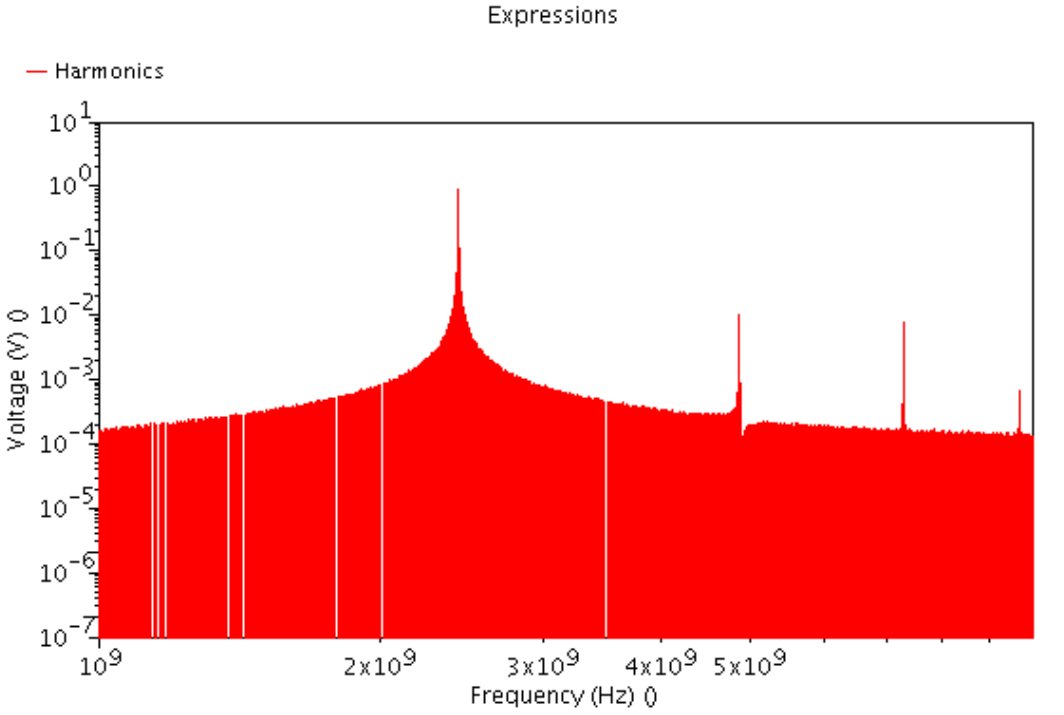
Figure 3.11 Harmonic simulation of (a) VCO1 (b) VCO2 (c) VCO3 for Experiment I.



(a)



(b)



(c)

Figure 3.12: Harmonic simulation of (a) VCO1 (b) VCO2 (c) VCO3 for Experiment II.

In Experiment II, quite similar results were achieved. Third harmonics are dominant in VCO1 and VCO2, but the second harmonic is introduced in VCO3. In VCO2, THD is reduced to less than one third when compared with VCO1. In VCO3, because the second harmonic is introduced, harmonic components are slightly increased. As concluded in Experiment I, the variation is caused by the *RC* network. However, when compared with VCO1, it still shrinks the value of THD by half.

From the analysis above, it can be concluded that the transformer does offer advantages in reducing the nonlinearity. The *RC* feedback network may influence the harmonics, but it is not always beneficial. However, when compared with the transformer, variations in harmonics caused by the *RC* feedback network are fairly small, which may be ignored.

3.6.2 Transfer Function

Because we care less about the closed-loop gains in lower and higher frequencies, only closed-loop gains between 1GHz to 10GHz are considered. The simulation results of the transfer function of the three topologies for Experiment I and II are shown in Figure 3.13(a) and Figure 3.13(b), respectively.

To evaluate the narrowness of a transfer function, the factor K has been defined to determine the integral of the closed-loop gain from the fundamental frequency to the fourth harmonic, which is represented by

$$K = \int_{f_0}^{4f_0} |H(f)| df \tag{62}$$

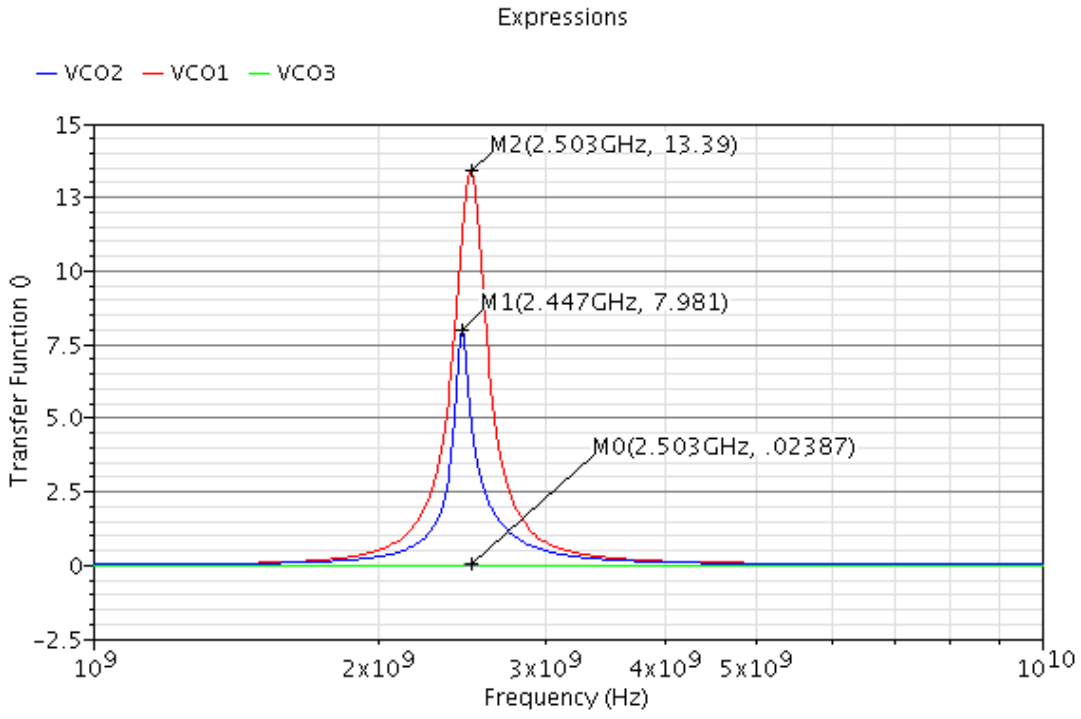
where $|H(f)|$ is the magnitude of the closed loop gain and f_0 is the fundamental frequency or center frequency. From the simulations, the transfer functions are approximated to converge to 0 when $f \to 0$ and $f \to \infty$. Note that K does not have any physical meaning; it merely shows how narrow the bandwidth of the transfer function is and how low the peak amplitude of the transfer function is. Results of K are concluded in Table 6 and Table 7 respectively for both experiments.

Table 6: Simulation results for K value for Experiment I

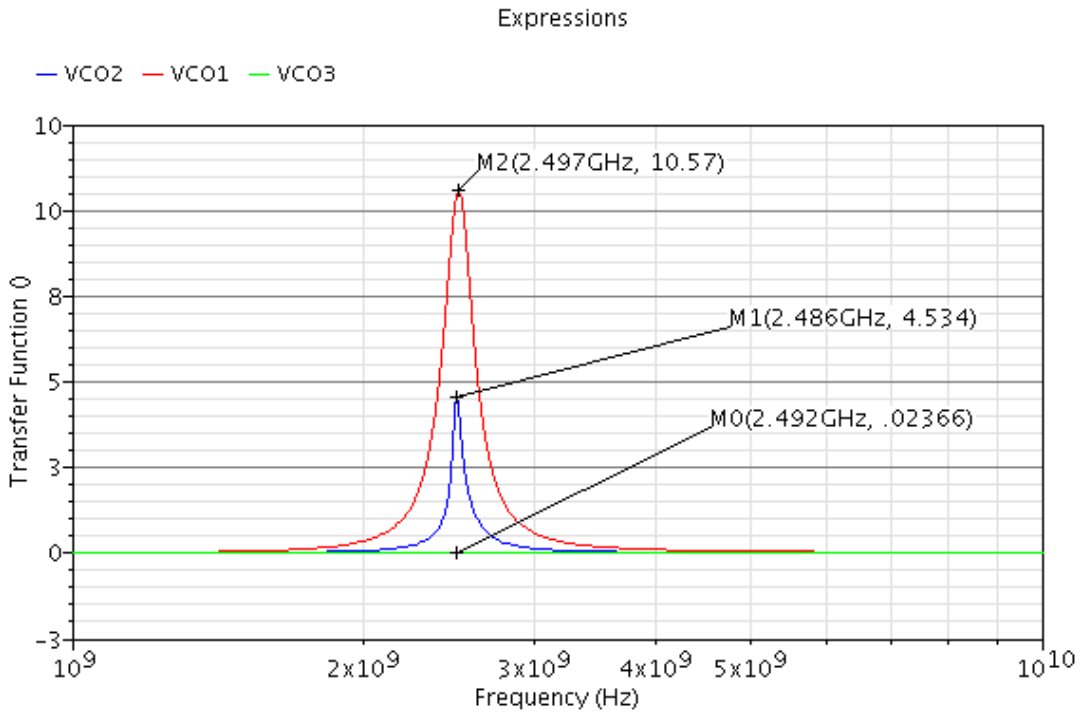
	Peak Value	K
VCO1	13.39	2.76E9
VCO2	7.98	1.62E9
VCO3	0.2387	1.36E7

Table 7: Simulation results for K value for Experiment II

	Peak Value	K
VCO1	10.57	2.16E9
VCO2	4.534	5.92E8
VCO3	0.2366	1.36E7



(a)



(b)

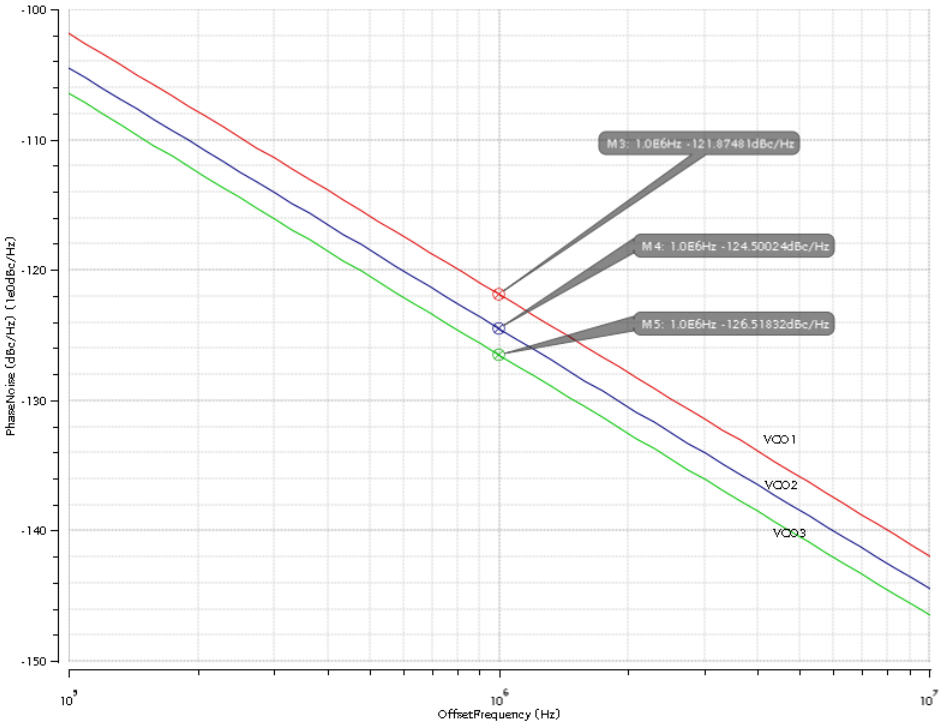
Figure 3.13: Comparison of transfer functions for (a) Experiment I (b) Experiment II.

Table 8: Simulation results for phase noise performance for Experiment I

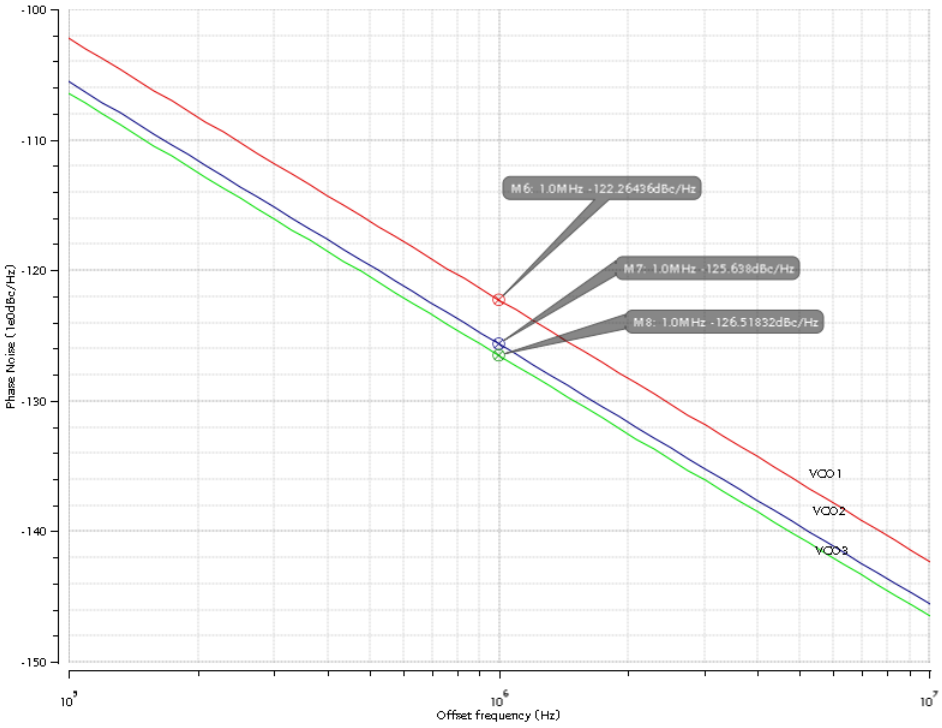
	Phase Noise @ 1MHz (dBc/Hz)
VCO1	-121.9
VCO2	-124.5
VCO3	-126.5

Table 9: Simulation results for phase noise performance for Experiment II

	Phase Noise @ 1MHz (dBc/Hz)
VCO1	-122.2
VCO2	-125.6
VCO3	-126.5



(a)



(b)

Figure 3.14: Phase noise comparison of VCO1, VCO2 and VCO3

In comparing VCO2 and VCO3, it is apparent that with the contribution of the *RC* feedback network, the magnitude and the bandwidth of the transfer function is severely reduced. When comparing VCO2 with VCO1, it can be seen that the transformer may also benefit the transfer function; however, its influence is less than that of the *RC* feedback network.

3.6.3 Phase Noise

From the analysis above, it can be seen that the proposed circuit has the ability to reduce both transfer function and harmonics efficiently. Therefore, it is not difficult to predict that the phase noise performance should be improved.

Simulation results for the phase noise performance of Experiment I and II are shown in Figure 3.14. Phase noise performances at 1MHz offset are illustrated in Table 8 and Table 9.

In both experiments, VCO3 offers the best phase noise performance among the three circuits. This is not surprising to see in Experiment I, as VCO3 had the best performance in both transfer function and harmonics. However, in Experiment II, although the harmonics in VCO3 are higher than they are in VCO2, the large decrement in transfer function is still dominant, resulting in VCO3's best phase noise performance.

3.6.4 Analysis on Flicker Noise

After exploring how the proposed circuit benefits harmonics and transfer function under the condition that flicker noise is turned off in the simulator, flicker noise coefficient is turned on again in the simulator to see how flicker noise affects the phase noise performance in this circuit.

Figure 3.15 shows the phase noise performance when Experiment I is repeated when flicker noise is turned on. Other parameters are kept same. Table 10 concludes the phase noise performance.

The differences between different flicker noise conditions in VCO1, VCO2 and VCO3 are 7.4dB, 3.1dB and 0.7dB respectively. Such differences are caused by the flicker noise. VCO1 shows worst resistance to flicker noise, while VCO3 shows best

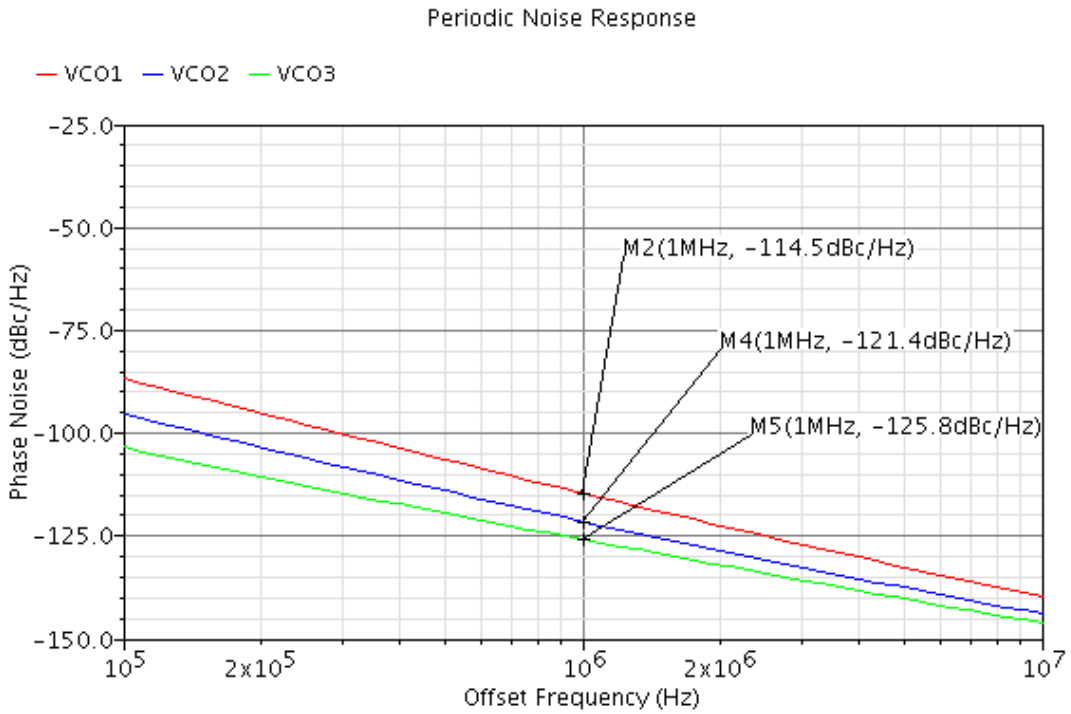


Figure 3.15: Phase noise comparison of VCO1, VCO2 and VCO3 when flicker noise is introduced.

Table 10: Simulation results for phase noise performance for Experiment I under different flicker noise condition

	Phase Noise @ 1MHz (dBc/Hz)	
	Flicker noise off	**Flicker noise on**
VCO1	-121.9	-114.5
VCO2	-124.5	-121.4
VCO3	-126.5	-125.8

performance in resisting transferring flicker noise into phase noise. This is because the coupled inductors and RC filter existing in the circuit can efficiently help filtering out part of the flicker noise. This benefit further proves the advantage of the proposed circuit in phase noise performance.

3.7 Conclusion

The above chapter has explored the mechanism on phase noise generation. Based on the research, it is found that the phase noise performance is determined by the transfer function and harmonic components of a VCO circuit.

According to the studies, VCO design guidelines have been concluded in guiding low phase noise VCO design. Based on which, a novel VCO topology has been proposed to reduce harmonic components and decrease the magnitude and the bandwidth of the transfer function, aiming to enhance the phase noise performance. According to the simulation results, this topology managed to reduce harmonic components and decrease the magnitude and the bandwidth of the transfer function. At the same time, the circuit also shows advantage in suppressing the up-conversion of flicker noise. Under the same conditions (e.g., tank, active devices), phase noise was improved as compared with the reference designs.

4 Chapter: Circuit Design

4.1 Introduction

This chapter demonstrates a VCO circuit design based on the proposed topology. The VCO is expected to have a center frequency of 2.4 GHz and a tuning range of 10%. Tank design, including the inductor and varactor design, is first introduced, followed by the design on the transformer and *RC* network designs. In each part, consideration of layout is taken into account. Lastly, simulation results are present.

4.2 Tank

In LC tank-based VCOs, the phase-noise performance is highly influenced by the tank. The higher the Q is, the better the phase-noise performance is [27]. This can be proved by Leeson's empirical (10) and a huge number of references.

In this work, single-ended *L* is chosen as 2 nH and a single-ended *C* is chosen from 1.9 to 2.4 pF. This is determined alongside several considerations. Although, theoretically, a much larger *L* would provide better phase-noise performance and save more power, in reality, a layout with a larger *L* usually brings more parasitic resistance, thus lowering the quality factor of the tank. Also, it may cause problems in designing the transformer as a result of the chip area consideration.

4.2.1 Inductor Design

A quality factor, by definition, is a dimensionless parameter that describes how underdamped an oscillator is. Further details about quality factors will be discussed in Appendix B. Higher factors indicate lower rates of energy loss relative to the stored energy of the resonator. In an LC tank, the quality factor is mainly determined by the quality factor of the inductor. For on-chip inductors, energy loss is caused by parasitic resistance. Previously, quality factors of on-chip inductors usually ranged from 3 to 5; however, now, with the progression of technology, the quality factors of on-chip inductors can reach 30 or even higher [38- 41]. Different layout methods may also contribute to higher quality factors [42].

(a) **(b)** **(c)**

Figure 4.1: Single-end planar spiral inductor layout methods. (a) Square (b) Hexagonal (c) Octagonal

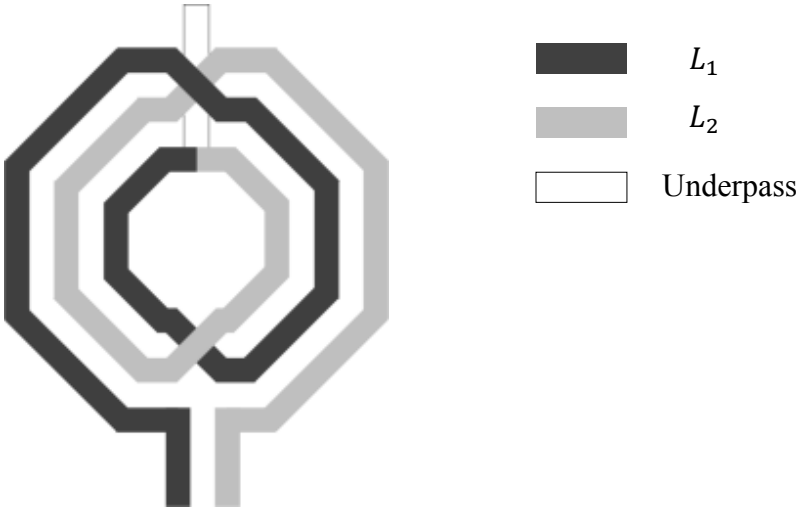


Figure 4.2: Differential symmetric layout method.

Figure 4.1 shows three different layout methods for single-end planar spiral inductors. The square version is popular because it is easy to generate in layout tools. Polygonal spirals with more than four sides are one example; hexagonal and octagonal inductors are also widely used.

However, in a differential circuit, differentially driven symmetric inductors (Figure 4.2) are more frequently used. This method not only realizes a nearly perfectly symmetrical layout, but it also improves the quality factor by differential excitation. In practice, the improvement would be lower, but still would provide 50% greater Q [42].

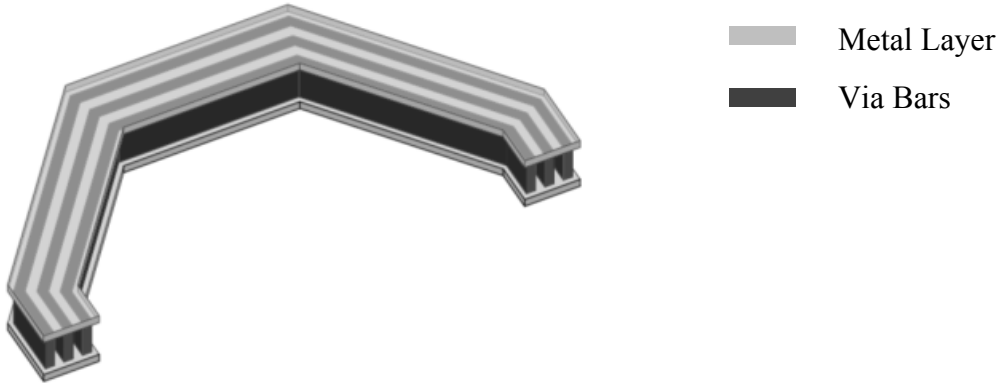


Figure 4.3: Multilayer layout method [5].

With the process in technology, multilayer inductors became more dominant because they offer higher Qs. That is, although the thickness of the inductors has less of an influence on the inductance, they severely decide the resistance of the inductors. The thicker the layer, the lower the resistance, gave a higher L_s/R_s ratio, and thus better performance. In practice, maximizing thickness is realized by connecting two layers with VIA bars (see Figure 4.3).

In this work, a differential multilayer structure has been employed. Because the thickness of the layer is certain, a large width and small turn-spacing minimize the parasitic resistance. After optimization, the quality factor at a desired frequency range (2.2–2.5 GHz) achieves around 21. Inductance is approximately 2 nH, while the resistance ranges from 1.3–1.5 Ohm. Simulation results are shown in Figure 4.4. Details regarding the device's sizes are shown in Appendix E

4.2.2 Varactor Design

There are several ways to form a varactor, diode varactor, pMOS varactor, and MOS varactor [5] [43]. MOS varactors, which allow for a better overall VCO performance, are more often favored.

MOS is a transistor with four terminals. However, when the source and drain are shorted and biased, the transistor could be used as a varactor because the capacitance of

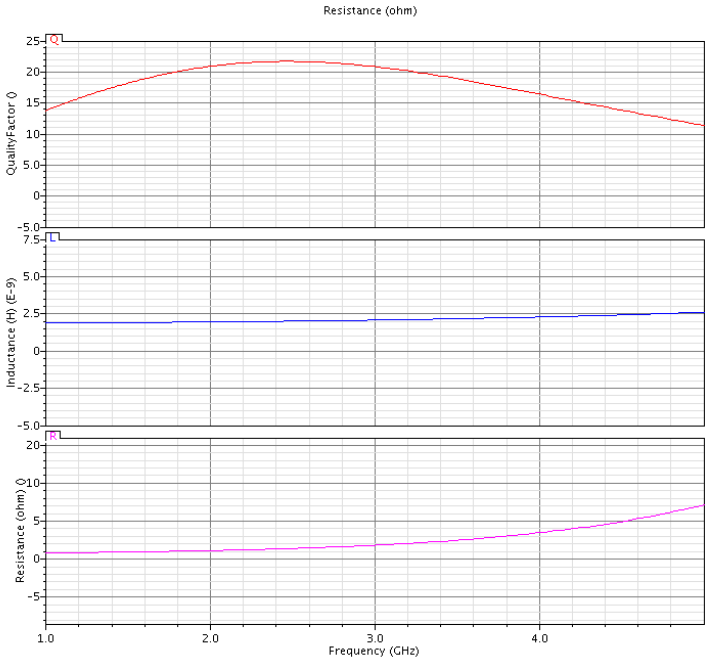


Figure 4.4: Simulation results for single-end inductors.

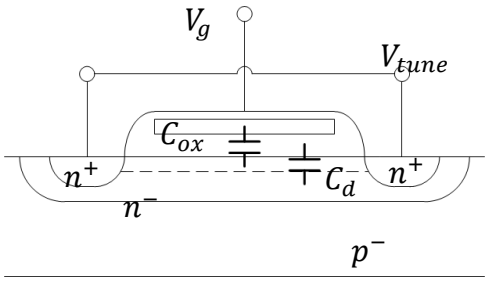


Figure 4.5: Side view of MOS varactor

the bottom plate changes with bias. Figure 4.5 shows a MOS varactor that is created by placing the n^+ diffusion regions of an NMOS device in an n-well region.

Define

$$V_{gd} = V_g - V_{tune}. \tag{63}$$

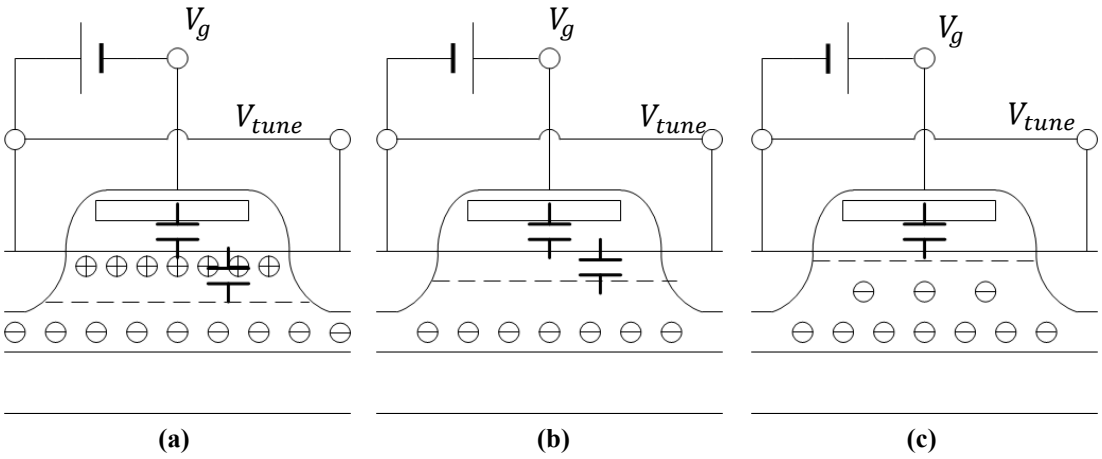


Figure 4.6: Varactors working in (a) Inversion region (b) Depletion region (c) Accumulation region.

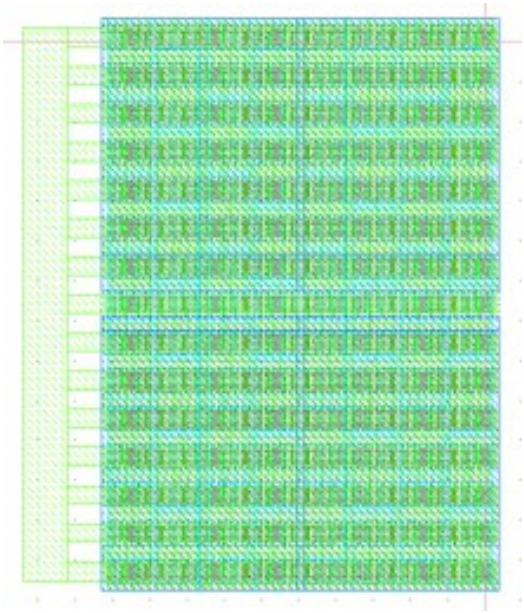


Figure 4.7: Layout for varactor arrays.

When V_{gd} is changed from negative to positive, the device operates from the inversion region to the depletion region, and, finally, to the accumulation region (see Figure 4.6).

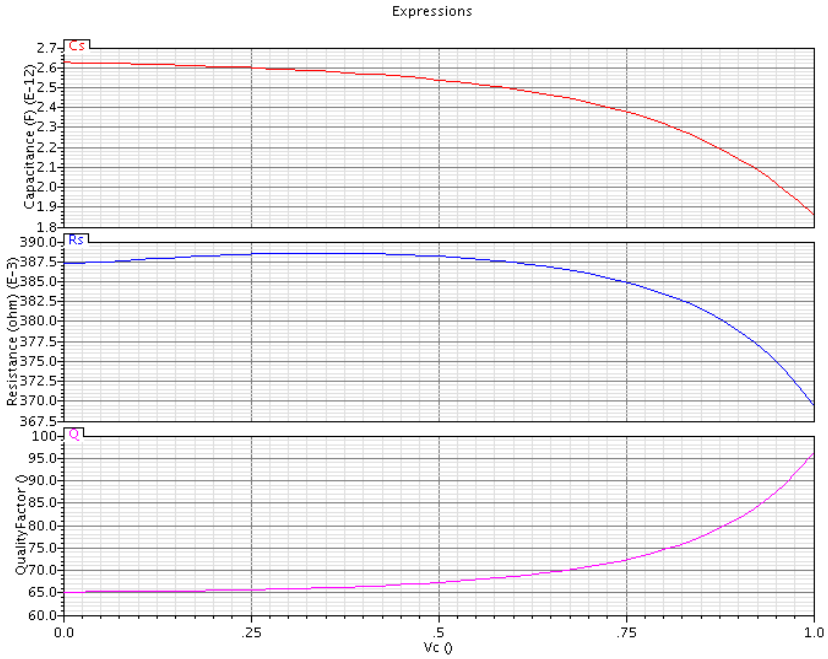


Figure 4.8: Simualtion results for the characterization of varactor arrays.

When the varactor works only in the depletion and accumulation regions, it is called an A-MOS varactor. Usually linearity is better in this region than in the inversion region. In this design, differential A-MOS varactors are used. To maximize the quality factor and Cmax/Cin, and to minimize the parasitic resistance, arrays of smallest-unit A-MOS fingers are placed in parallel to each other as shown in Figure 4.7. Parasitic resistance is around 0.37 Ohm within the frequency range. Capacitance varies from 1.9–2.4pF. Simulations are shown in Figure 4.8.

4.3 Transformer

There are several ways to design on-chip transformers [44]. Figure 4.9 shows three different realizations of on-chip transformers: tapped, interleaved, and stacked. Tapped transformers have the advantage of giving high self-inductance and low port-to-port capacitance. However, the trade-off is that it produces a relatively low mutual coupling because of spatial separation. Usually the coupling coefficient is $k \in (0.3, 0.5)$.

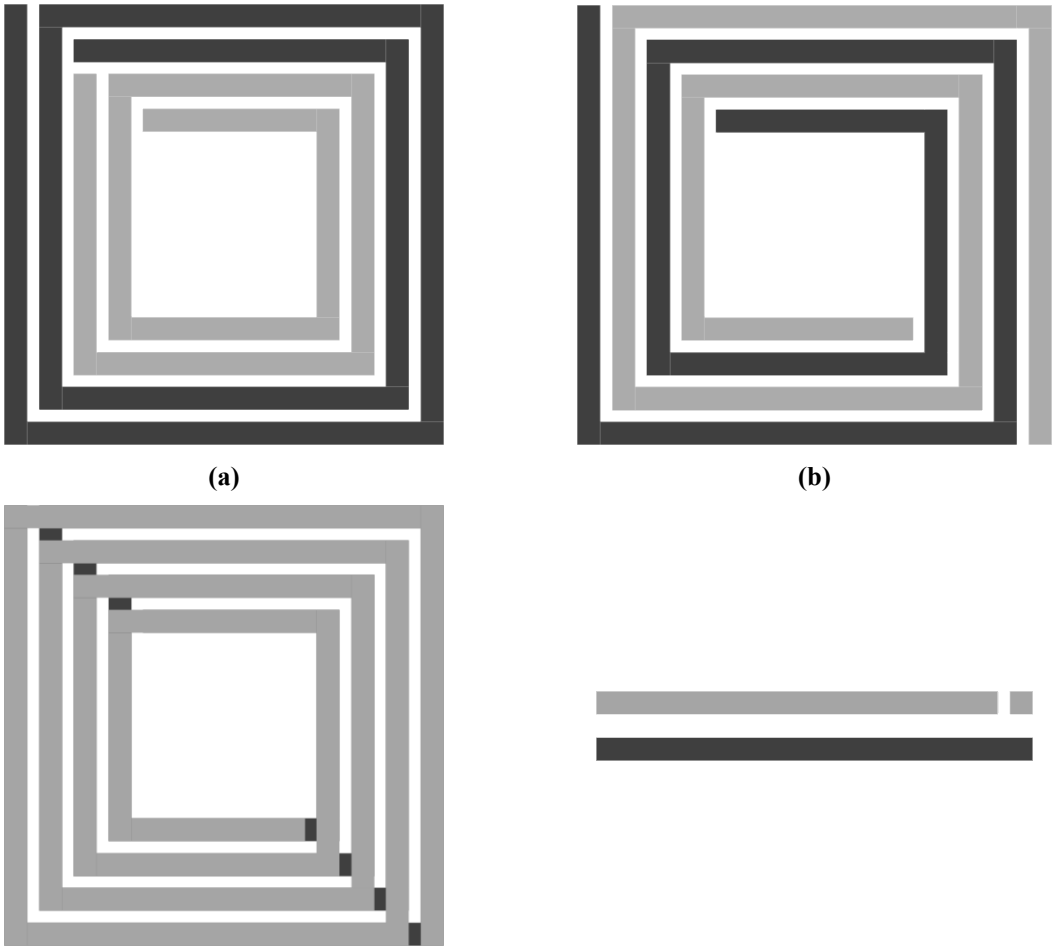


Figure 4.9: Layout method for on-chip transformers. (a) Tapped (b) interleaved (c) Stacked

Table 11: Comparison between different layout methods for on-chip transformers

	Self-inductance	**Port-to-port capacitance**	**coupling coefficient**
Tapped	High	Low	$(0.3, 0.5)$
Interleaved	Low	Low	$(0.7, 0.8)$
Stacked	Very high	High	0.9

Interleaved transformers offer a relatively high coupling coefficient ($k \approx 0.7$) and low port-to-port capacitance. However, the self-inductance is lower.

Stacked transformers are realized in multilayers, giving high self-inductance and a very high coupling coefficient (k may reach 0.9). The trade-off is the high port-to-port capacitance, which is equivalent to a low self-resonance. This can be adjusted by

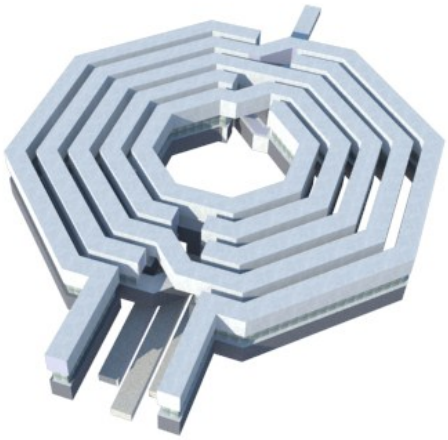


Figure 4.10: 3D view on proposed transformer

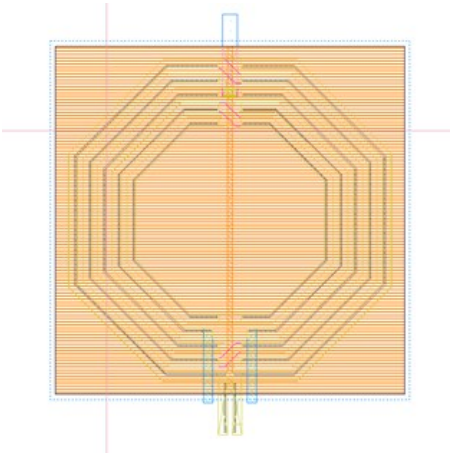


Figure 4.11: On-chip transformer with shield

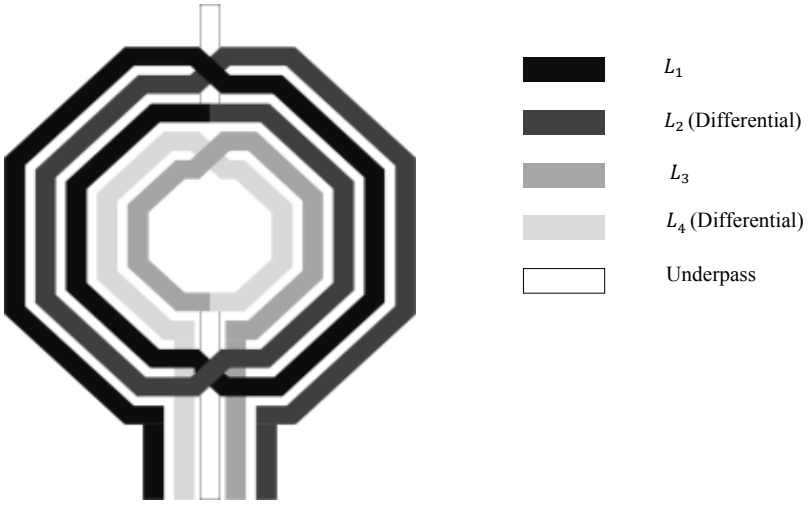


Figure 4.12: Layout method for the proposed transformer

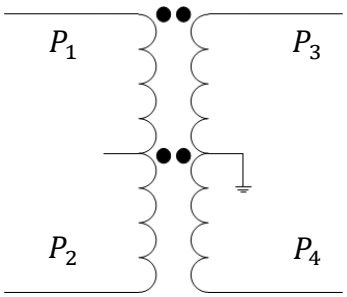
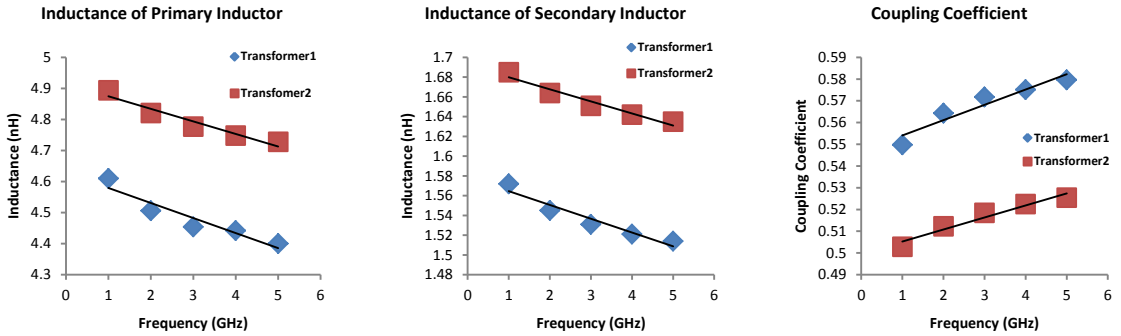


Figure 4.13: 4-port transformer

Table 12: Parameters for transformer1 and transformer2 (Square Spiral)

Parameter		Value
Primary Inductor	Outer dimension	300um
	Width	8.5um
	Space	5um
	Turn	3
Secondary Inductor	Outer dimension	219um
	Width	8.5um
	Space	5um
	Turn	2



(a) **(b)** **(c)**

Figure 4.14: Simulation results for Transformer1 and Transformer2 using ASITIC

(a) Primary inductor (b) Secondary inductor (c) Coupling coefficient

increasing the distance between the two layers or by changing the center of the two spirals.

In the proposed circuit, high self-inductance is required. High self-inductance, especially for the tank inductor, is to achieve a higher Q. The coupling coefficient is not strictly required.

Hence, the tapped type is chosen for the proposed circuit. Since tank inductors and source inductors are both differential, the four inductors can be realized by one transformer with four ports (see Figure 4.13). A top view and 3D view of the final transformer are shown in Figure 4.12 and Figure 4.10 respectively.

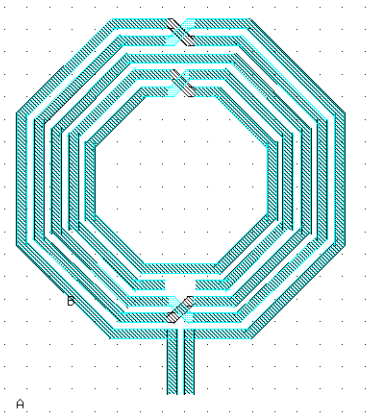


Figure 4.15: Schematic for proposed transformer using ASITIC

Table 13: Parameters for the design symmetrical transformer

Parameter		Value
Primary Inductor (Differential)	**Outer dimension**	300um
	Width	8.5um
	Space	5um
	Turn	3
Secondary Inductor (Differential)	**Outer dimension**	219um
	Width	8.5um
	Space	5um
	Turn	2

To provide a good short to the ground for the electric field, a ground shielding is placed, using the lower metal [45]. The layout view of the complete transformer with shield is shown in Figure 4.11.

To verify the transformer design, a model has been built up using ASITIC. In this software, “joinshunt” command is used to join multiple spirals in shunt. To verify the accuracy of using “joinshunt” command in simulating the multiply layer transformer, a simple experiment has been carried out to compare the coupling coefficient of a square spiral transformer using the double layer inductor created by “JoinShunt” command (Tranformer2) with the double layer inductor model exiting in the simulator

Table 14: Parameters for differential dual layer inductors

Parameter		Value
Differential Inductor	Outer dimension	300um
	Width	8.5um
	Turn	1

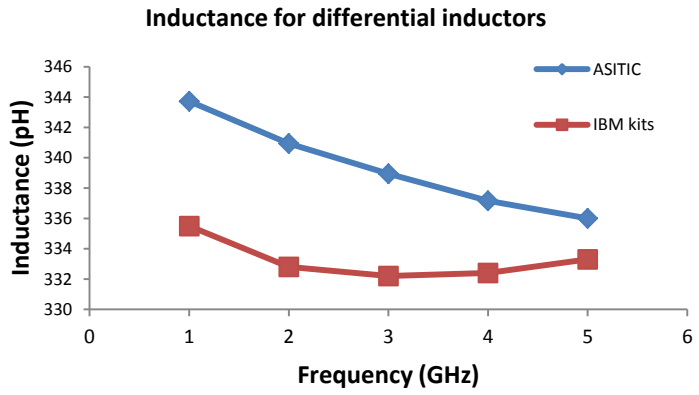


Figure 4.16: Simulation results for the differential inductance of dual layer inductors.

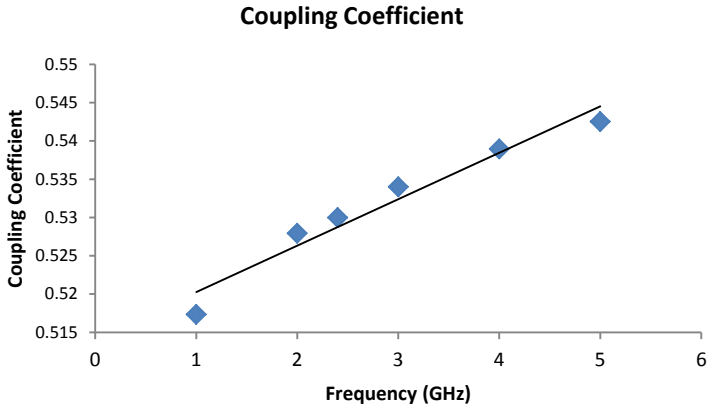


Figure 4.17: Simulation results for the coupling coefficient of proposed transformer

using "joinshunt" command (Transformer1) to the multiply layer transformer model that exists in the software (Transformer2) when other parameters are kept same. Parameters are concluded in Table 12. Results of the inductance and the coupling coefficient are shown in Figure 4.14.

From Figure 4.14, it can be observed that even though there is variance between the two methods, especially in simulating inductance. However using “joinshunt” command still can roughly predict the coupling coefficient of the transformer using double layer inductors.

To further prove the reliability of the simulator, another experiment has been carried out to compare the inductance of differential dual layer octagonal symmetrical inductor using ASITIC to the model that is provided by the IBM kits because mutual inductance is included in the differential inductors. Parameters are concluded in Table 14. Results of inductance are shown Figure 4.16: Simulation results for the differential inductance of dual layer inductors. It can be observed that results from the two simulators are very close. The difference is within 2%, which proves the reliability of ASITIC.

Schematic of the proposed transformer is shown in Figure 4.15 and design parameters are concluded in Table 13. Simulation results are shown in Figure 4.17. At 2.4GHz, the coupling factor is 0.53.

4.4 RC Network

The RC filter in the proposed design is a low-pass filter. To reduce the magnitude and the bandwidth of the transfer function around demanding frequency range, large bias resistors of around 80 MOhm are required. This is hard to realize on-chip; hence, the resistors are designed off-chip.

4.5 Simulation

Figure 4.18 shows the schematic for the proposed VCO design, including buffer. To simulate the transformer, inductors in the tank are simulated by connecting ideal inductors and series resistors. The resistance of the series resistors can be obtained from

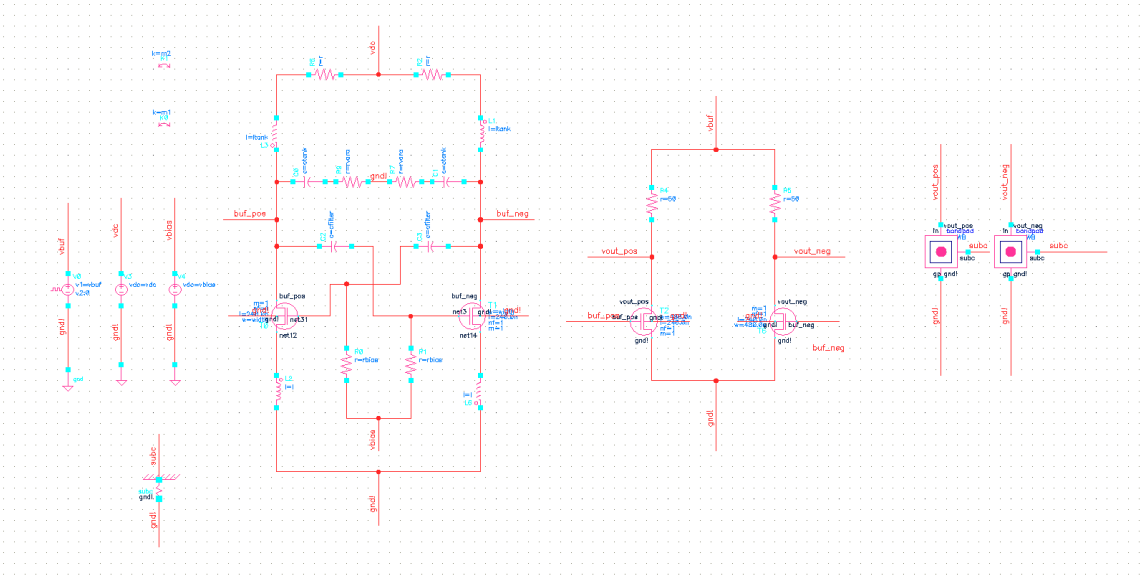


Figure 4.18: Schematic of final design, including buffer

Table 15: Design parameters

Transistors for VCO Core	12.6um/120nm
Transistors for Buffer	16um/120nm
Supply Voltage (V)	1
Bias Resistors (Ohm)	80M
Coupled Capacitors (F)	2p
Load Resistors for Buffer (ohm)	50
Coupling Coefficient	0.53

Figure 4.4. To help with PSS analysis, varactors are also simulated by connecting capacitors and resistors in series. The value of series resistance can be obtained from Figure 4.8. The bias voltage is adjusted to get best phase noise performance at different operating frequency. Other design parameters are concluded in Table 15.

The transconductance of the VCO core transistor is 4.7mA/V. The parallel resistance of the tank is about 630ohm. According to the oscillation startup condition

Table 16: Simualtion Results for proposed VCO

Center Frequency (GHz)	2.44
Tuning Range (%)	10
Phase Noise (dBc/Hz)	-132.8
Power Consumption (mW) (VCO core)	3.01
Figure-of-Merit (dBc)	195.8

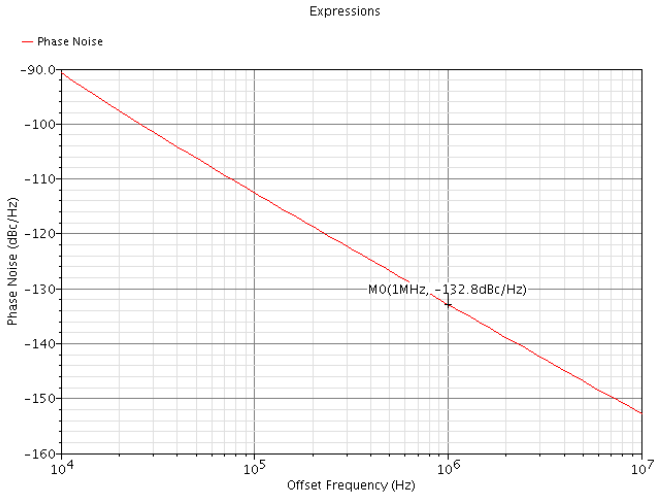


Figure 4.19: Simualtion result for the phase noise performance of the proposed VCO at 2.44GHz

Table 17: Simulation results in different corners

Corners	**Power Consumption (mW)**	**Phase Noise (dBc/Hz)**	**FoM (dBc/Hz)**
TT	3.01	-132.8	195.8
SS	2.73	-131.6	195.0
FF	3.24	-133.0	195.6
SF	2.77	-132.4	195.8
FS	3.19	-132.9	195.6

Table 18: Comparison table for the simulation results

Ref.	Tech	Freq (GHz)	Phase Noise (dBc/Hz)	Power (mW)	FoM (dBc/Hz)
[6]	130nm	4.90-5.65	< -130@3MHz	1.40	195.5
[6]	130nm	4.50-5.00	-133@3MHz	1.40	196.0
[21]	180nm	6.09-7.50	-123@2MHz	2.16	191.0
[18]	180nm	1.4±0	-129@1MHz	1.46	190.0
[18]	180nm	3.8±4.2%	-119@1MHz	0.57	193.0
This work	130nm	2.44±5%	-133@1MHz	3.07	195.8

$$g_m > \frac{2}{r_p} \tag{64}$$

the circuit should start oscillating without problem.

Table 16 shows the simulation results of the VCO. Figure 4.19 shows the phase noise performance. Table 18 lists the comparison among this design with reported VCOs. Table 17 lists the phase noise, power consumption performance and FoM for different corners. Note that power consumed by the buffer is not included in the power consumption column.

4.6 Conclusion

This chapter has presented a circuit design based on the proposed topology. Simulation results show that this design shows good performance in either phase noise or power consumption, giving a more favorable figure of merit. Compared to the reported VCOs, this design achieves relatively high FoM.

5 Chapter: Chip Design and Evaluation

5.1 Introduction

A chip based on the proposed circuit design in chapter 4 has been taped out using IBM 130nm technology. Layout consideration is discussed first, followed by chip evaluation.

5.2 Layout Consideration

As has been pointed out in Chapter 4, the circuit is integrated on a single chip except for the bias resistors, which are too large to be implemented on the chip. The key to optimization is dynamic adjustment to linearize the circuit. Also, to reduce second harmonics, the layout is made as symmetric as possible. The final floor plan is shown in Figure 5.1.

5.3 Evaluation

5.3.1 Equipment, Probes, and Station Setup

To test the chip, two RF probes, one multicontact DC probe, and 2 DC needles are needed to land from the four cardinal directions. Important properties of the probes are highlighted in Table 19.

One spectrum analyzer and four voltage sources are needed for the testing. Since power consumption is one of the most important figures of the VCO, high accuracy is in current consumption for VCO core is required. Accuracy of the power supply of the buffers and the tuning voltage of the varactors is less important. Accuracy of bias voltage is least important.

Table 20 summarizes the equipment used and its highlight properties.

Other tools needed include off-chip resistors, tweezers, glasses, instant glues, and cables. Testing station set up is shown in Figure 5.2.

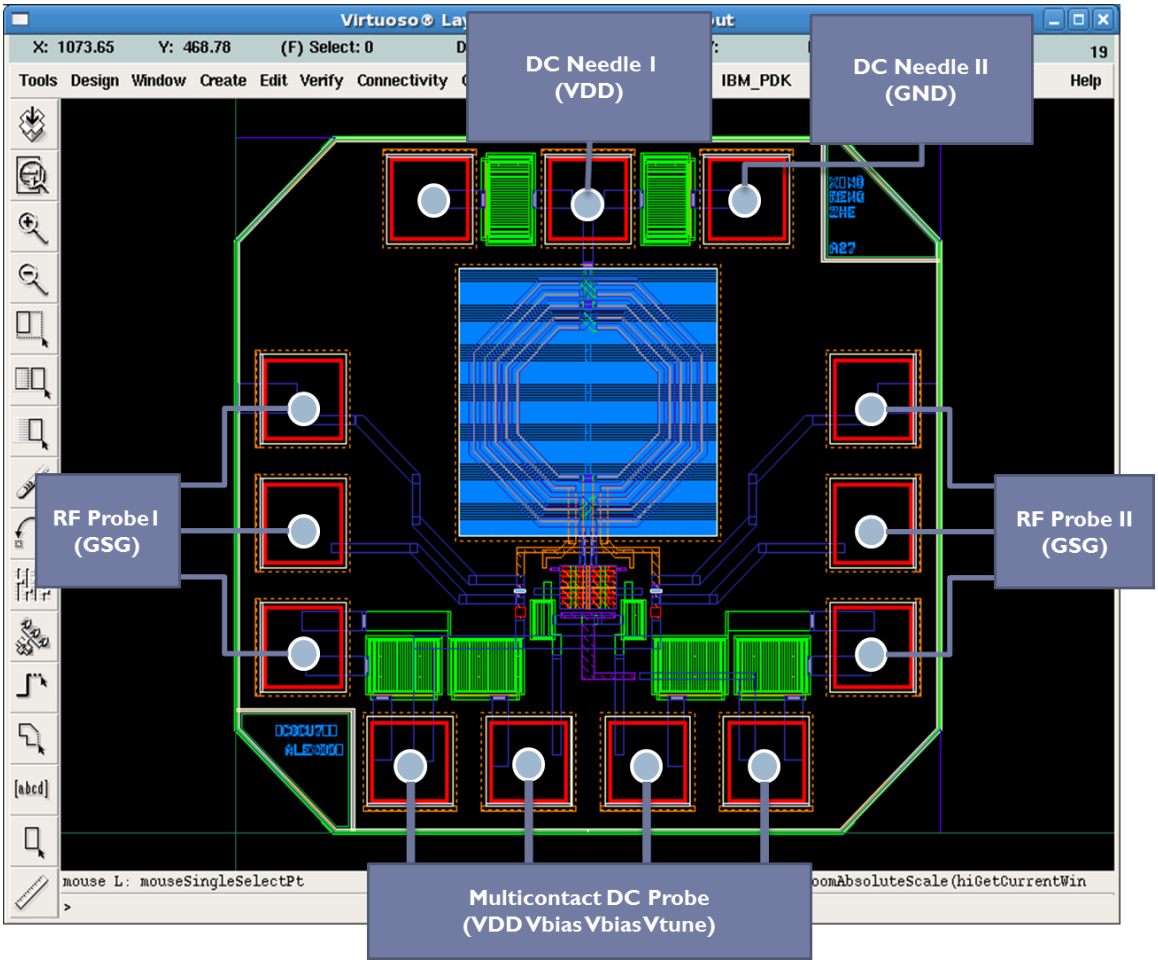


Figure 5.1: Floor plan for the chip.

Table 19: Table for probes

RF Probes (GSG) 40A-GSG-150-P Quantity: 2 • DC to 40GHz • Pitch (tip spacing) = 150um	
Multicontact DC Probes MCW-22-8667 Quantity: 1 • 4 Tips • Pitch = 150um	
DC Needles Quantity: 2	

Table 20: Table for the testing equipment

Spectrum Analyzer HP/Agilent 8564E Quantity: 1 • 30Hz to 40GHz	
DC Voltage Source I Keithley 2400 Source Meter Quantity: 2 • 0.012% basic measure accuracy with 5½-digit resolution	
DC Voltage Source II/IV HP/Agilent E3646A Quantity: 1 Readback Accuracy Voltage: <0.05% + 5 mV Current: <0.15% + 5 mA	
DC Voltage Source III HP/Agilent E3630A Quantity: 1 • 10mV, 10mA resolution	

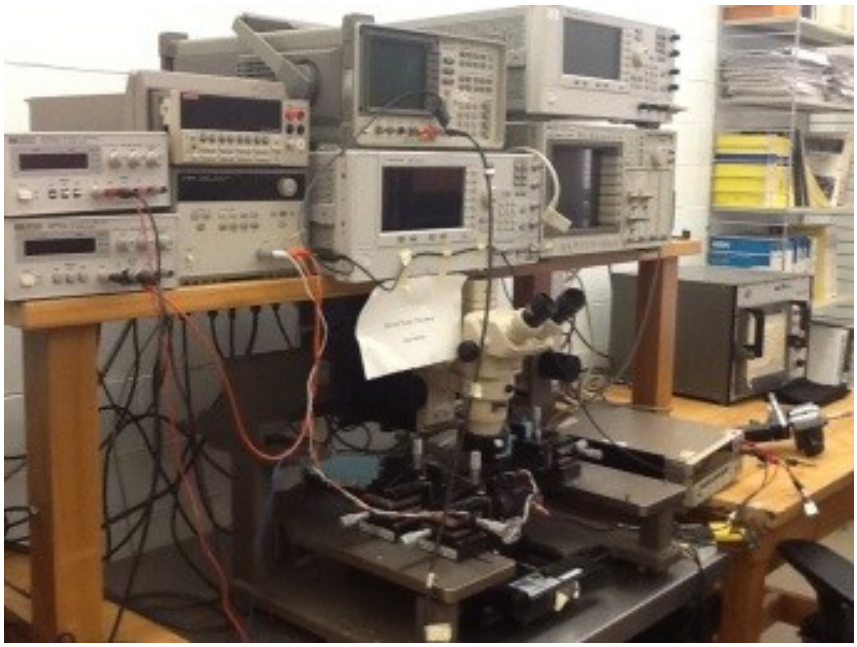


Figure 5.2: Testing station setup.

5.3.2 Measurement and Failure Analysis

Several chips were tested with no output captured on the spectrum analyzer. This indicates an absence of AC signals in the circuit. This is often caused by a failure of startup in oscillation. Figure 5.3 is the test report for one of the tested chips. It turned out the buffers worked as expected, but not the VCO core.

The reasons for failure of oscillation startup can be complicated. One of the possible causes is the topology. The circuit can be simplified as Figure 5.4. Because the cross-coupled differential pair is blocked by two capacitors $C_{filter1,2}$ from the RC feedback network, no low frequency noise is accumulated within the positive feedback loop, which thus fails to start the oscillation. Therefore, an attempt to introduce disturbance by shorting the DC current in a very short time was carried out. However, no AC outputs were shown on the spectrum analyzer.

5.3.2.1 Failure Analysis on the Quality Factor

A possible reason for this failure could be over-estimation of the Q of the tank. In this design, Q of the tank varies from 17 to 18 over the oscillating frequency according to the simulation. However, in the real case, Q can be decreased severely because of the unexpected parasitic resistance. The parasitic resistance will in turn increase energy consumption, thus larger positive feedback gain will be needed to start and keep the oscillation, namely larger g_m of the active devices is required.

There are two methods to increase the positive feedback gain in testing. One of them is to increase the supply voltage manually. In this way, drain current I_{ds} will be enlarged and g_m will consequentially increase. Another method is to increase V_{bias}. This method will change the dc operating point, giving larger conduction angle of the transistors. Hence, more current will be allowed to inject into the tank. In this way the positive feedback gain is also increased.

In fact, the second method – increasing V_{bias}, is powerful to solve "the lack of positive feedback gain" issue. According to simulations, even with a very poor Q, increasing V_{bias} to suitable voltage may still start and maintain oscillation. Figure 5.5 (a)-(c) show an case with Q = 10 with suitable V_{bias}. Note that other components in

Test Report

Chip Number： 006 Testing Date: March 25th, 2012

Oscilation Test

Test Condition: Room Temperature, Vbias = 1V, VDD(Buffer)=1V, Vtune = 1V

VDD for VCO core (V)	Range (V)	Oscillation (Y/N)
0.8	0.799904 – 0.800096	N
1	0.99988 – 1.00012	N
1.4	1.399832 – 1.400168	N
1.6	1.599808 – 1.600192	N
2	1.99976 – 2.00024	N

Note： No output on spectrum analyzer under 0.8-2V.

Current Comsuption for VCO Core Test

Test Condition: Room Temperature, Vbias = 1V, VDD(Buffer)=1V, Vtune = 1V

VDD for VCO core (V)	Range (V)	Current Consumption (mA)
0.8	0.799904 – 0.800096	0.2468
1	0.99988 – 1.00012	0.3652
1.4	1.399832 – 1.400168	1.2516
1.6	1.599808 – 1.600192	2.0493
2	1.99976 – 2.00024	2.7852

Note： N/A

Current Comsuption for VCO Buffer Test

Test Condition: Room Temperature, Vbias = 1V, VDD(Core)=1V, Vtune = 1V

VDD for VCO core (V)	Range (V)	Current Consumption (mA)
0.6	0.5947 – 0.6053	5
0.8	0.99988 – 1.00012	6
1	1.399832 – 1.400168	9
1.2	1.599808 – 1.600192	10
1.4	1.99976 – 2.00024	12

Figure 5.3: One test report example.

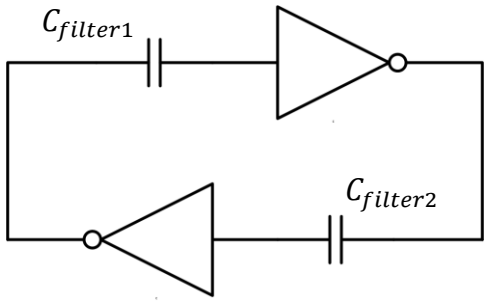
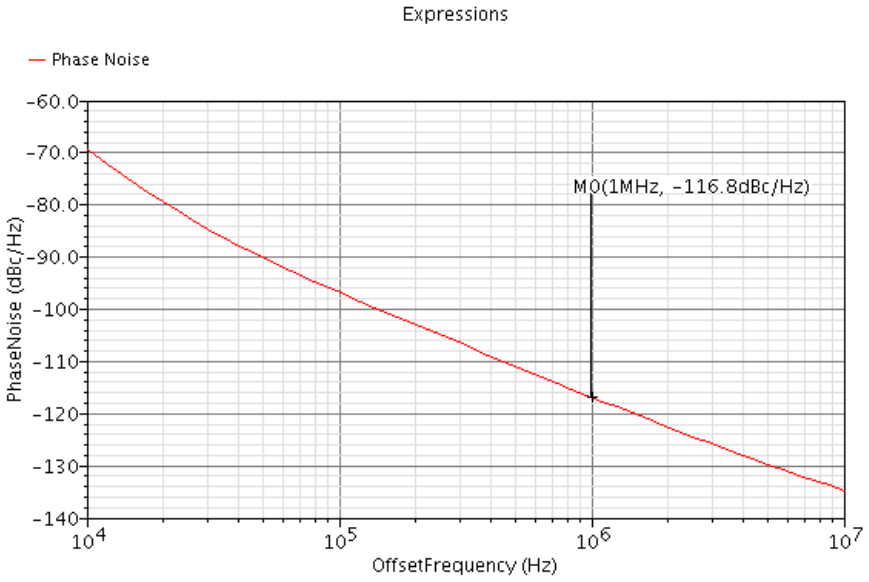
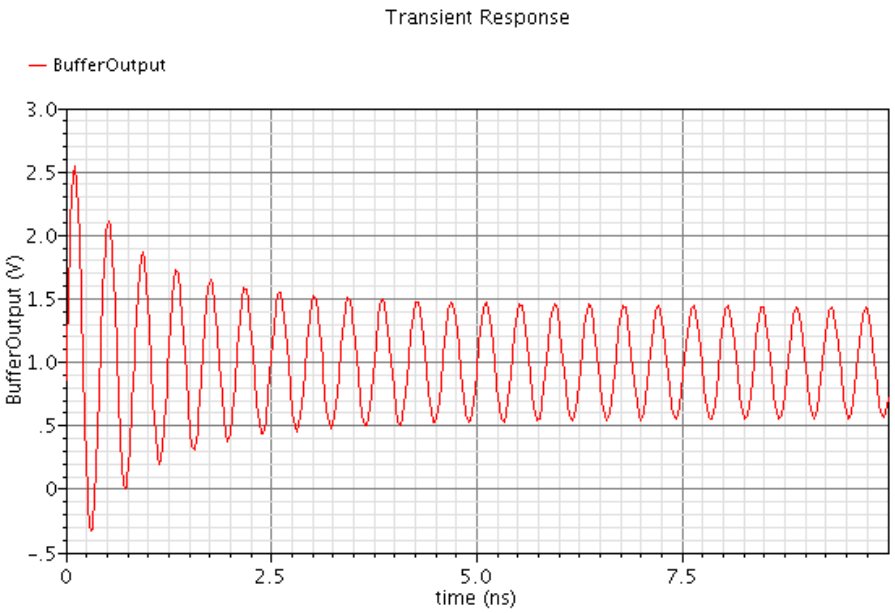


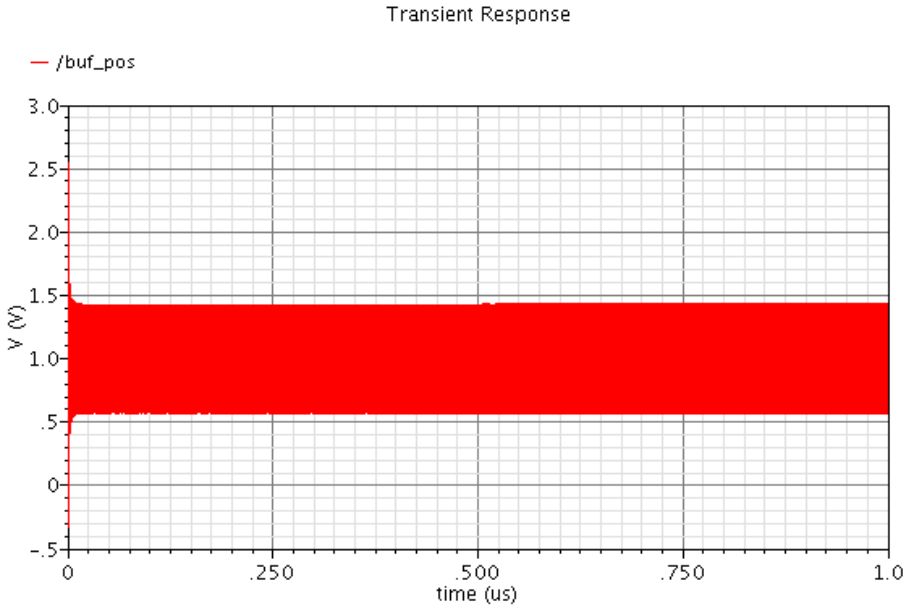
Figure 5.4: Simplified diagram for the proposed VCO.



(a)



(b)



(c)

Figure 5.5: (a) Phase Noise (b) Transient response (0-10ns) (c) Transient response (0-1us) for tank Q = 10.

the circuit remain the same. It turned out when V_{bias} is increased to 0.5V, despites the phase noise performance (see Figure 5.5(a)) is lower, the VCO is still able to work properly (see Figure 5.5 (b)(c)).

During the chip testing both of these two methods were carried out. At the same time, shorting the DC current in very short time was also tried under higher power supply or higher V_{bias} to help start oscillation. However, still no AC output showed up on the spectrum analyzer. This indicates the failure of oscillation is not caused by the reduction of Q.

5.3.2.2 Failure Analysis on the Transformer

Another possible reason could be that the coupling coefficient is not estimated appropriately. In the design, the coupling coefficient is estimated to be 0.53. However in reality the value of coupling coefficient may be much lower than expected. Hence, simulations have been carried out to verify how different coupling coefficient affects oscillation.

To simulate the worst case, coupling coefficient is set to -0.7. Other conditions are kept the same as the design. Not surprisingly, the oscillation died out after tens of nanoseconds (see Figure 5.6).

However, during the simulating, it turned out through increasing V_{bias}, the oscillation can be maintained. When V_{bias} is increased to 0.5V, the VCO is able to function although the phase noise performance and power consumption becomes worse (see Figure 5.7 (a)-(c)).

As mentioned in the previous analysis, V_{bias} was increased during testing. However still no AC output shown on the spectrum analyzer. This indicates the failure is not caused by the inaccurate estimation of transformer's coupling coefficient.

5.3.2.3 Failure Analysis on Pad Capacitance

Another possible reason comes from the underestimation of the capacitance of the pads.

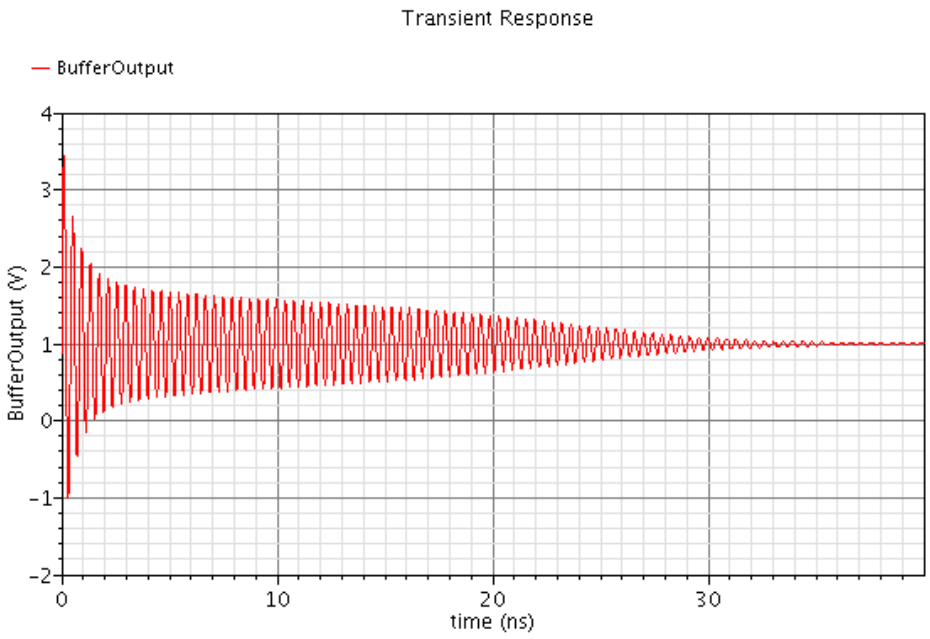
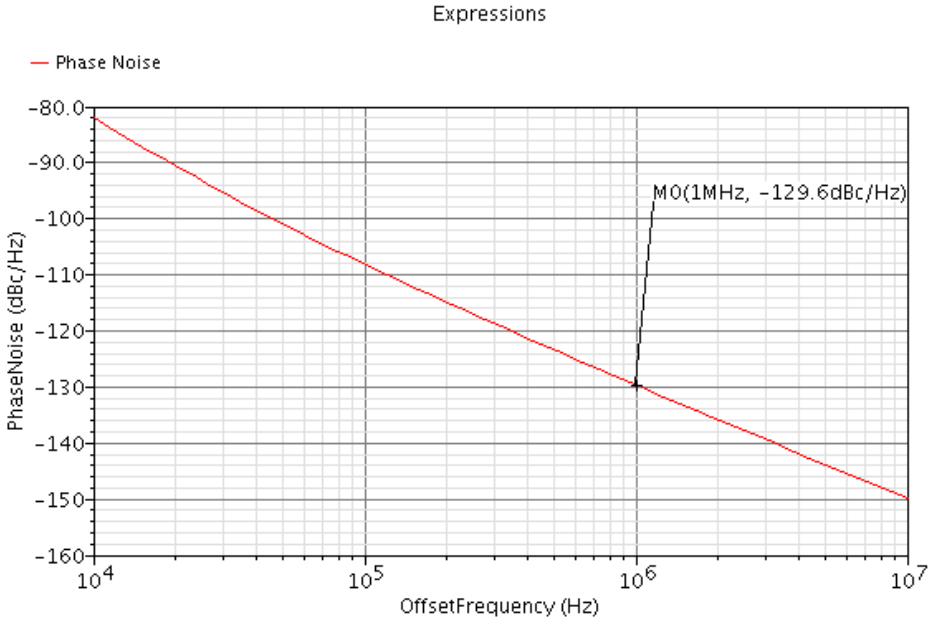
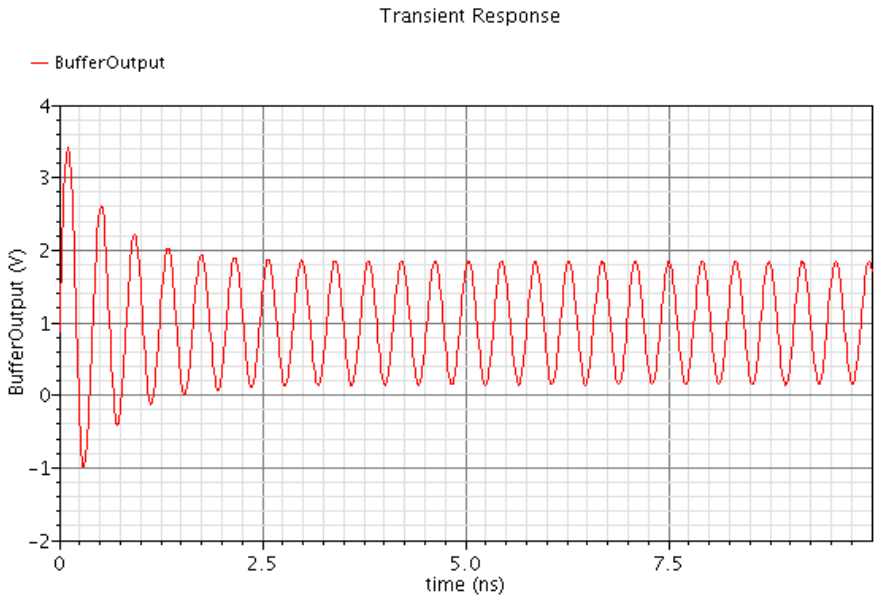


Figure 5.6: Transient response for k=0.01.



(a)



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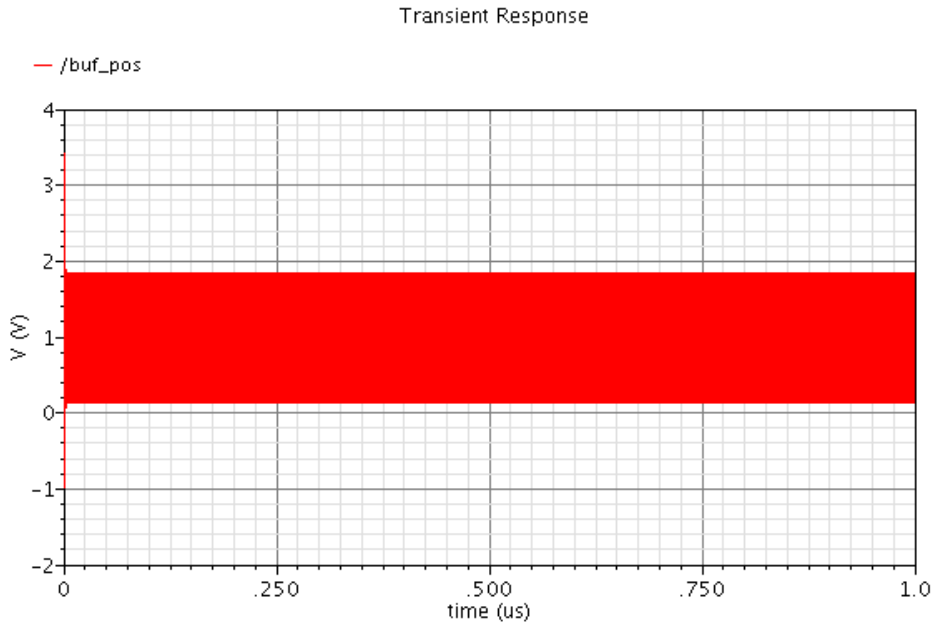


(c)

Figure 5.7: (a) Phase Noise (b) Transient response (0-10ns) (c) Transient response (0-1us) for k = 0.01 with V_{bias}=0.5V.

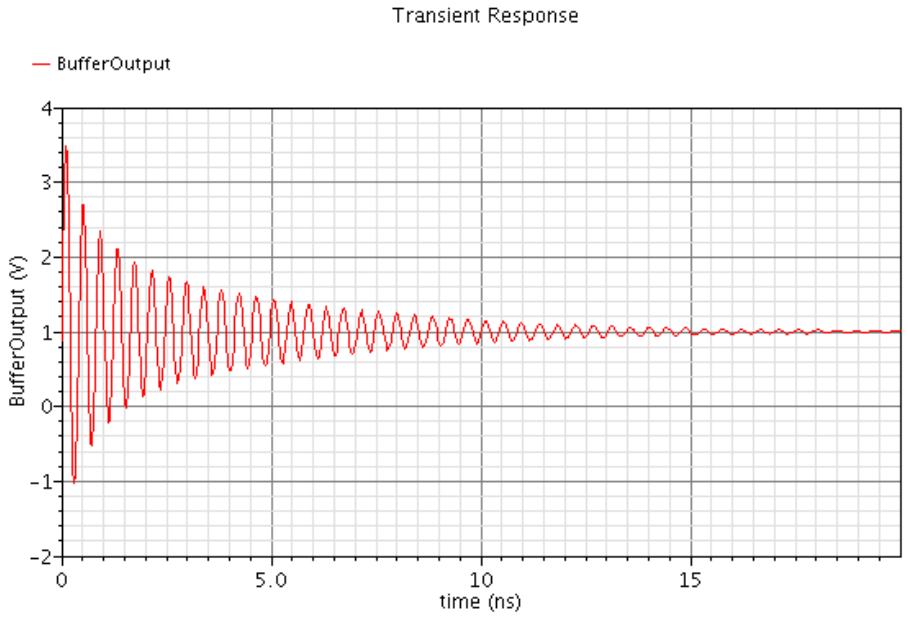
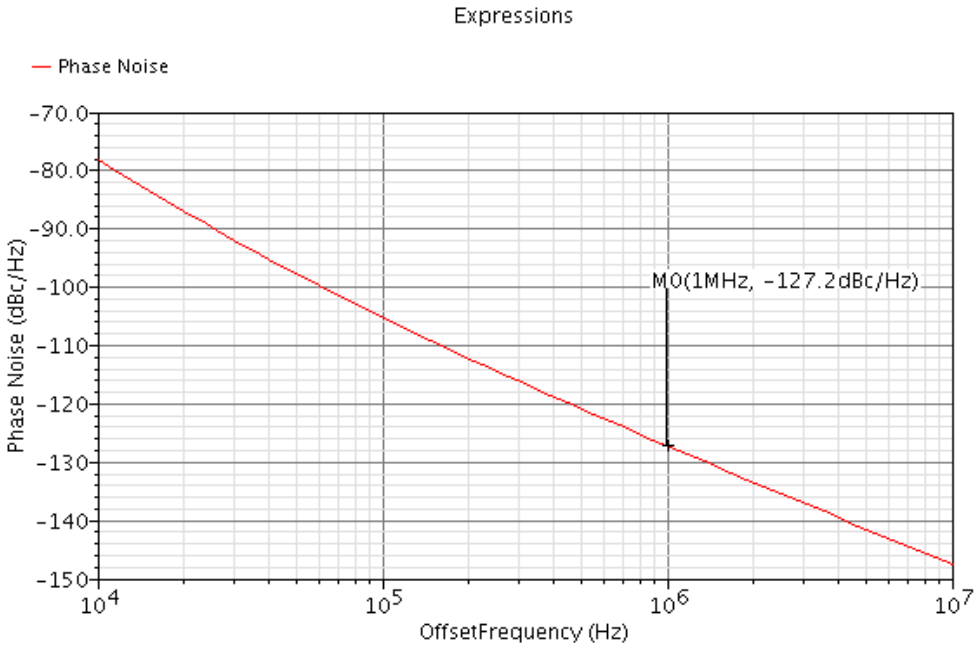
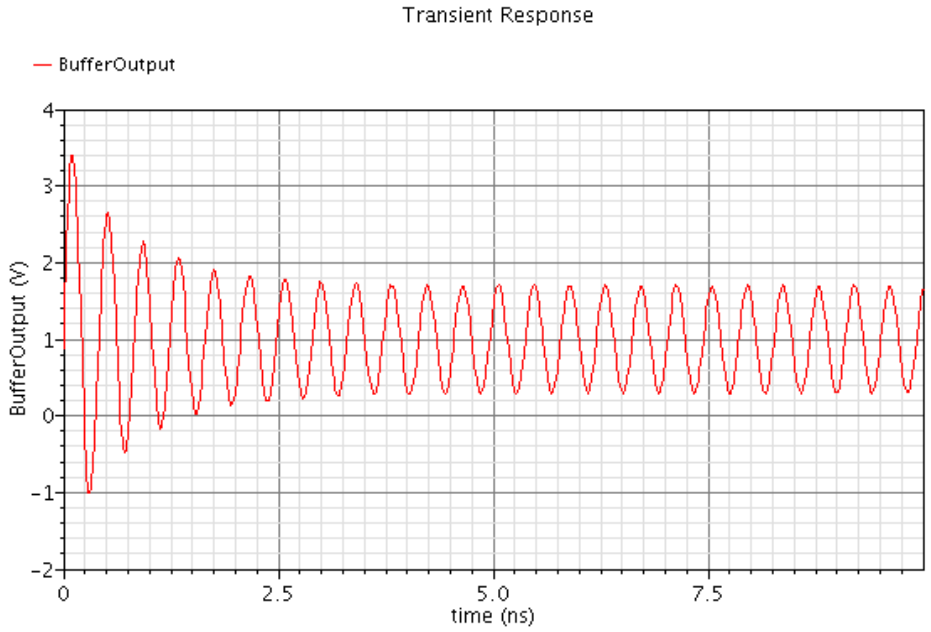


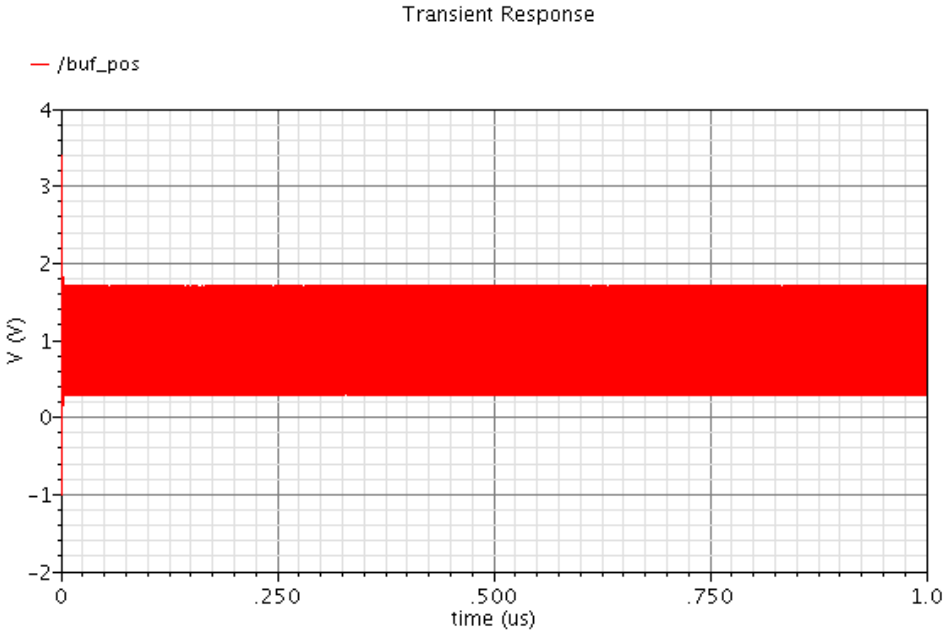
Figure 5.8: Transient response for VCO with extra pad capacitance.



(a)



(b)



(c)

Figure 5.9: (a) Phase Noise (b) Transient response (0-10ns) (c) Transient response (0-1us) for VCO with extra pad capacitance when V_{bias}=0.5V.

The extra parasitic capacitance of the pads may cause the VCO fail to drive the loads and consequentially die out.

To simulate the worst case, two extra 2pF capacitors are added onto the differential outputs of the buffer in parallel with the pads. Similar to the previous cases, the oscillation died out when all the parameters are kept same as the design (see Figure 5.8). However in simulation when V_{bias} is increased, the VCO works (see Figure 5.9). Hence the underestimation of the capacitance of the pads is not the reason to cause the startup failure.

5.3.3 Cause of Failure

After investigating the possibilities above, the layout view has been checked. Eventually, it is found that the reason to cause the failure of the oscillation is the misconnection between the primary inductors of the transformer and the varactor array of the circuit. Because of the transformer is designed by the author, the transformer is not included in the LVS verification, as well as its connection to the rest part of the circuit.

The connection part between the primary inductor and the varactor array is realized by stacking metal layer MQ, MG and LY appropriately to the top two layers. This strategy is to reduce the parasitic resistance as much as possible, aiming to maintain a high quality factor of the tank.

Figure 5.10 shows a varactor array using 8 differential varactor units. The drain sides are connected using metal layer M3. Then metal layer MQ is used to connect the differential gates. Figure 5.11 shows how three varactor arrays are connected using metal MQ. Then such pattern is repeated. Figure 5.12 shows the layer MQ in the whole varactor array (32*15 units), other layers are turned off to make the view clear. Then the odd and even number metal bars shown in Figure 5.12 are connected together by metal MG respectively. Then MG is connected to the top layer by stacking the metal layers.

However, in the connection part between the primary inductors and the varactor array, two extra pieces of MQ metal are added by mistake (see Figure 5.13, one of the

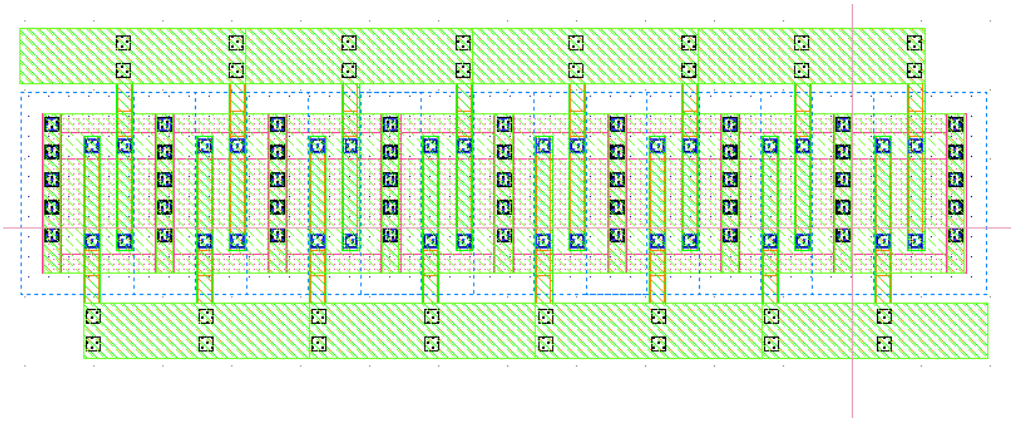


Figure 5.10: Layout view for 8*1 varactor array

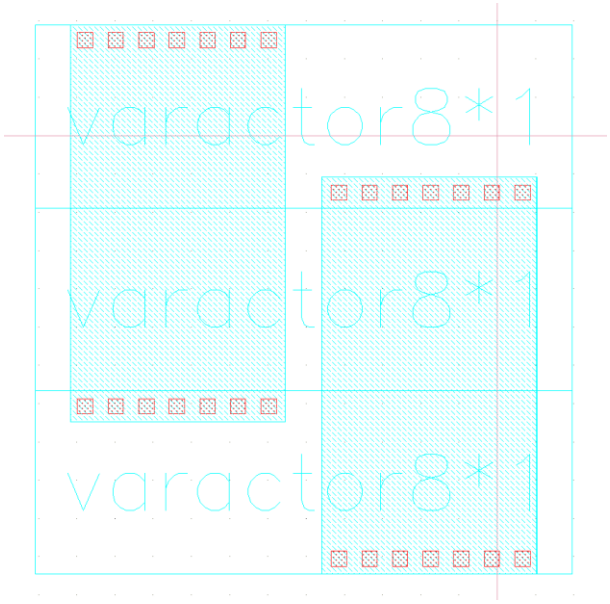


Figure 5.11: Layout view for 8*3 varactor array

unwanted metal is highlighted as an example), resulting in connecting all the gates of the differential varactor array together. The tank is then shorted as shown in Figure 5.14.

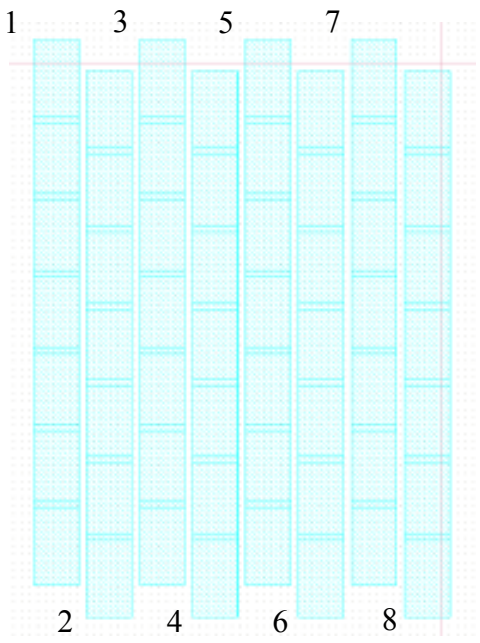


Figure 5.12: Expecting layer MQ for the entire varactor array (32*15 units)

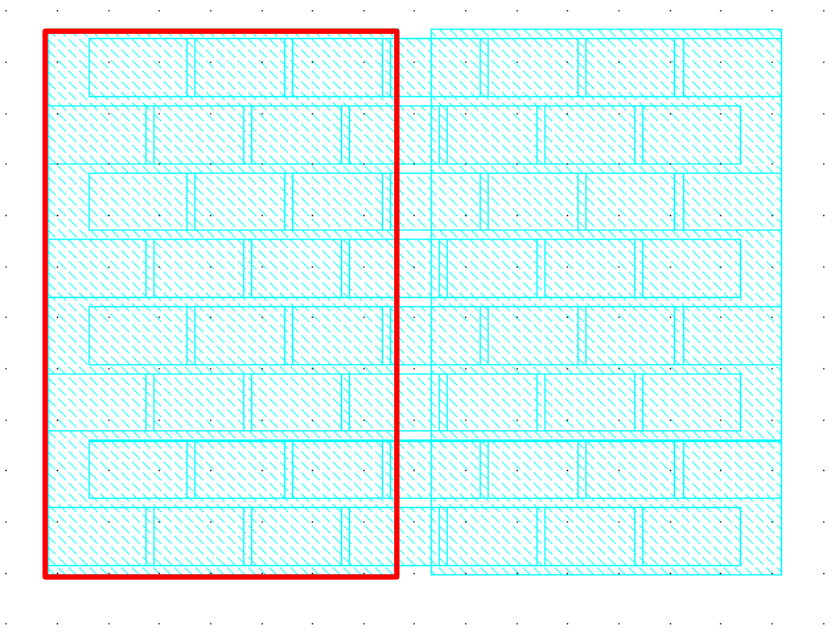


Figure 5.13: Wrong layout view for layer MQ

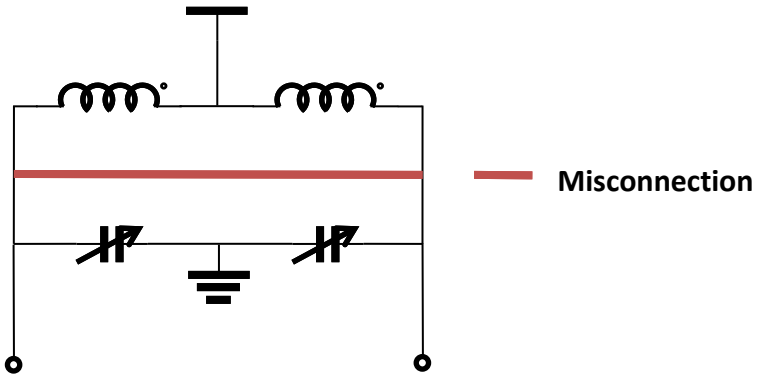


Figure 5.14: Equivalent circuit for the misconnected tank

This misconnection will make the circuit fail to oscillate no matter what adjustment in the supply voltage or bias voltage has been made. This is in accordant with the observation in the testing. Also, this misconnection is equivalent to connect the gates of the buffer amplifiers to the DC power supply (1V) directly since there is no ac signal in the tank, which also matches the testing results in the measurement.

5.4 Conclusion

This chapter presents the chip design and evaluation. Layout consideration is briefly discussed first, followed by the display on the measurement setup.

The chip did not work as expected. It failed to start oscillation. To find the problem, failure analysis has been made to find out the reason that caused the oscillation failure. After exploring the possible reasons, including tank, transformer and load capacitance, it is found the reason that causes the failure of the oscillation is the misconnection between the primary inductors and the varactor array.

6 Chapter: Conclusion

6.1 Conclusion of the Thesis

This thesis researches the relation between phase noise and non-linear behavior. In Chapter 2, previous researches on VCO theory, including both linear and non-linear approaches, have been reviewed first. Circuit examples are then reviewed with analysis.

In Chapter 3, an attempt to link the non-linear behavior to the phase noise has been made starting with a hypothesis that the phase noise is determined by the harmonic components of the circuit. Simulation results proved a definite link between the phase noise and the harmonic components. At the same time, simulation results also indicated the existence of other factors. Hence another assumption, that phase noise is determined by the transfer function and harmonics, has been put forward to explain the generation of phase noise. With this insight, harmonic content can be used as the design optimization tool in search of an optimum FoM topology. A VCO circuit using harmonic and transfer function suppression technique is then proposed to decrease phase noise. Simulations results show that the circuit has less harmonics and narrower transfer function with lower peak amplitude. The circuit provides 10dB improvement phase noise performance compared to the circuit without employing harmonics suppression and transfer function reduction techniques.

In Chapter 4, a 2.4GHz VCO using the proposed topology has been designed with IBM 130nm technology. Design issues, including devices selection (inductors, varactors, transformer, etc), circuit optimization and layout consideration have been discussed first, followed by simulations. Results show that the phase noise performance and FoM of this design is among the state of arts.

Chapter 5 presented the chip evaluation and failure analysis process. Measurement set up is shown at first. Measurement results indicated that the chip is

failed to start up oscillating. Then several possible reasons are listed and discussed. Finally the reason that fails the oscillation is the misconnection between the primary inductors and the varactor array.

6.2 Conclusion of the Contribution

The contribution of this thesis is an exploration of the relation between non-linear behavior and phase noise. Although people may have been aware of the relation between harmonics and phase noise, studies on examining this relation have not been reported.

6.3 Future Work

This thesis showed an attempt to link the phase noise performance with transfer function and harmonic components. Although the reported research proved the hypothesis, evidences are still demanded to make it general.

Another topic is to expand work on the VCO circuit topologies using the proposed VCO design guideline.

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Appendices

Appendix A Middlebrook Method

Middlebrook's method provides a way of finding accurate closed-loop gains in a feedback system. In conventional feedback system analysis, the loop gain is obtained in the following manner: first, the loop is broken to reach the feedback ratio, K, hence the loop gain T can be determined by

$$T = AK \tag{A.1}$$

where A is the forward gain. Then, the closed-loop gain H is given by

$$H = \frac{AK}{1 + AK}. \tag{A.2}$$

However, in the actual hardware circuit, this conventional method of analysis is inaccurate. For instance, the input impedance of an op-amp is not infinite, and thus the signal transmission is bidirectional. Also, the DC operating points and small signal AC impedance on both sides of the breaking point are normally different.

Middlebrook's method can solve the problems mentioned above. By injecting a small test voltage signal V_t and a small current signal I_t Figure A.2, the voltage gain T_v and current gain T_i can be given respectively by

$$T_v = \frac{V_f}{V_t} \tag{A.3}$$

$$T_i = \frac{I_f}{I_t}. \tag{A.4}$$

$$T = \frac{T_v \cdot T_i - 1}{T_v + T_i + 2}. \tag{A.5}$$

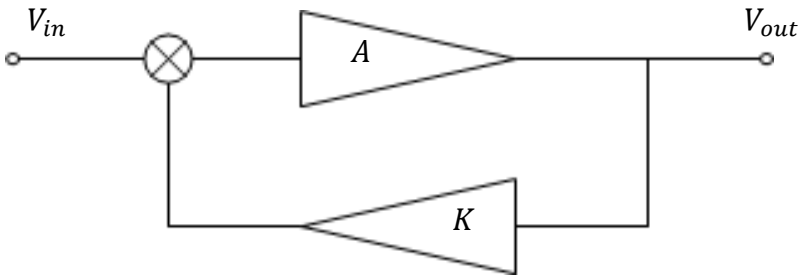

Figure A.1: Block diagram for typical negative feedback system

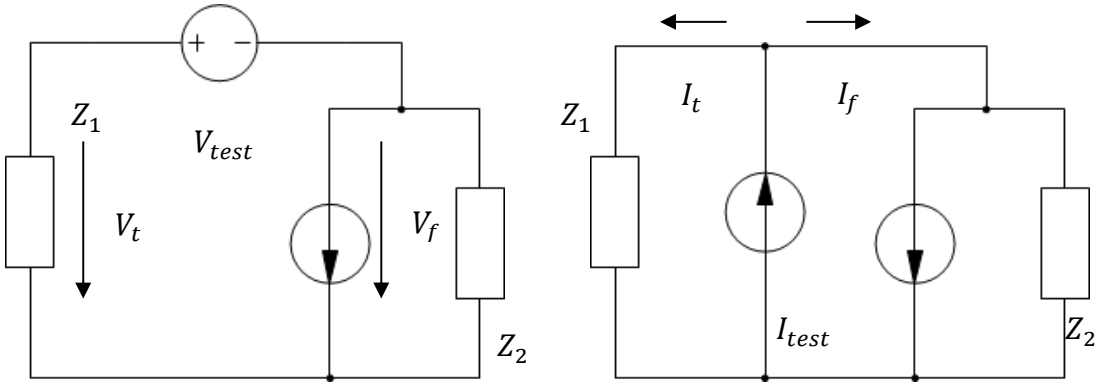

Figure A.2: Testing signal placement. (a) Voltage (b) Current

Note that the both T_v and T_i are complex gain.

Appendix B Definition of Q

There are many definitions for the quality factor Q in various applications.

B.1 Energy Approach

The one most widely used definition is from the energy approach, which is the energy stored, divided by the energy dissipated per cycle:

$$Q_E = \omega \frac{E_{stored}}{E_{diss}}. \tag{B.1}$$

This definition is very general and can be applied in multiple contexts, from optical systems to mechanical systems. Providing an analogy of this definition, Q of passive components (inductors and capacitors) can be defined as,

$$Q_{c,L} = \frac{reactive\ impedance}{real\ impedance} = \frac{im(y11)}{re(y11)}. \tag{B.2}$$

B.2 Bandwidth Approach

From the bandwidth approach, Q is defined for bandpass characteristics as the center frequency divided by the 3 dB bandwidth is

$$Q_{BW} = \frac{\omega_c}{\Delta\omega_{3dB}}. \tag{B.3}$$

B.3 Stability Approach

From the phase stability approach, Q is defined as the slope of the phase at center frequency, given that

$$Q_{phase} = -\frac{\omega_c}{2}\frac{d\varphi}{d\omega}|\omega = \omega_c. \tag{B.4}$$

However, no matter the approach, when applying these definitions to an LC tank, Q may be derived into a similar expression, or

$$Q = \omega\frac{L_s}{R_s} \tag{B.5}$$

where L_s and R_s represent the series inductance and series resistance, respectively.

Appendix C Simulation Issues on Inductors

Since transformers have been employed in this topology, using the existing inductor models in the library provided by the foundry has become impossible. Instead, the inductor should be modeled by an inductor connected with a resistor in series. The aim of adding the resistor is to model the parasitic resistance of the inductor.

To get the inductance and parasitic resistance at the oscillating frequency, a port is connected to the inductors in parallel and ground one side to implement characterization. Then the quality factor, inductance and parasitic resistance can be obtained through simulations by inductors

$$Q = \frac{Im(Z11)}{Re(Z11)} \tag{C.1}$$

$$L = \frac{Im(Z11)}{\omega} \tag{C.2}$$

$$R = Re(Z11). \tag{C.3}$$

Then these values can be used in the VCO simulation.

Appendix D Issues on Transformers

The transformers can be modeled using *mind* elements in *analoglib* library in Cadence. However, the problem is how to estimate the coupling coefficients k for on chip transformers. Although many software can be used to get accurate$k$, it is unworthy to consume so much time using those software to guide VCO designing. In fact, for tapped and interleaved transformers, the inductances can be calculated from geometric parameters, such as the outer dimension, coil width spacing and number of turns. Therefore, an easy approximation in [44] is used here to find an estimation of k.

First, mutual inductance can be found by

$$M = (L_T - L_1 - L_2)/2 \tag{D.1}$$

where L_T is the total inductance of a single spiral with all the segments of both primary and secondary traces, L_1 and L_2 are the self-inductances of the primary and secondary coil respectively, and M is the mutual inductance.

Then k can be calculated by

$$k = \frac{M}{\sqrt{L_1 L_2}}. \tag{D.2}$$

Appendix E Tank Inductor

Except for the turns (*N*) of differential inductors, another three parameters that determine the performance of inductors are: outer dimension (*O*), coil width (*W*) and spacing (*S*) (see Fig. Figure E.1). Quality factor (*Q*), inductance (*L*) and parasitic resistance (*R*) can be calculated with these parameters, however usually it is not accurate. Hence simulations are taken to help choosing the appropriate parameters for the inductors. High quality factor and high inductance are desirable.

Fig. Figure E.2 – Fig.Figure E.4 show how *N* influence *Q*, *L* and *R* with certain *O*, *W* and *S* when *N* = 1, 2, 3. Table 21 concludes the results. It turns out *N* is a crucial factor to determine *Q*, *L* and *R*. Considering sparing area for the secondary coil, the maximum of the turns is set to be 3. When *N* = 3, although *R* is largest (*R* is proportional to the length of the inductor), it still provides largest *Q* and *L* around the target center frequency (2.4GHz). Hence *N* is chosen to be equal to 3.

Fig. Figure E.5 – Fig. Figure E.7 demonstrate how *O* influence *Q*, *L* and *R* with certain *W, S* when *N* = 3. Results are concluded in Table 22. Around 2.4GHz, *Q*, *L* and *R* increase with the increment of *O*. Hence, to obtain largest *Q* and *L,* as well as providing more area to the secondary coil, *O* is chosen at 300um.

Fig Figure E.8 – Fig. Figure E.10 show how *W* influence *Q*, *L* and *R* with certain *S* when *N* = 3 and *O* = 300um. Results are concluded in Table 23. It turns out larger width is harmful to both quality factor and inductance. Hence, *W* is set as the minimal width that provides by the technology.

Fig. Figure E.11 – Fig. Figure E.13 demonstrate how *S* influence *Q*, *L* and *R* with when *N* = 3 , *O* = 300um and *W* = 8.5um. Table 24 concludes the results. It turns out larger S is harmful to both quality factor and inductance, but does not affect *R* severely. Taking saving area for secondary coil into account, *S* is set to the minimal in this technology.

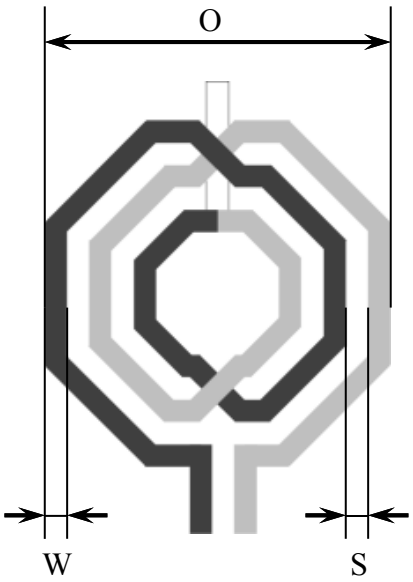

Figure E.1: Parameters of inductors.

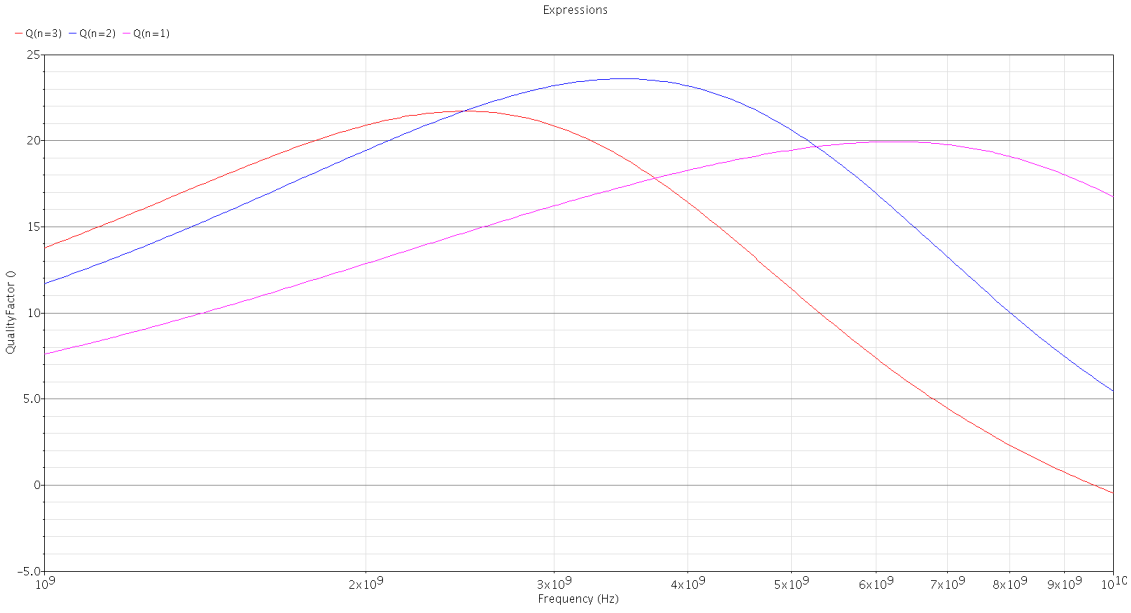

Figure E.2: Quality factor vs. Turns.

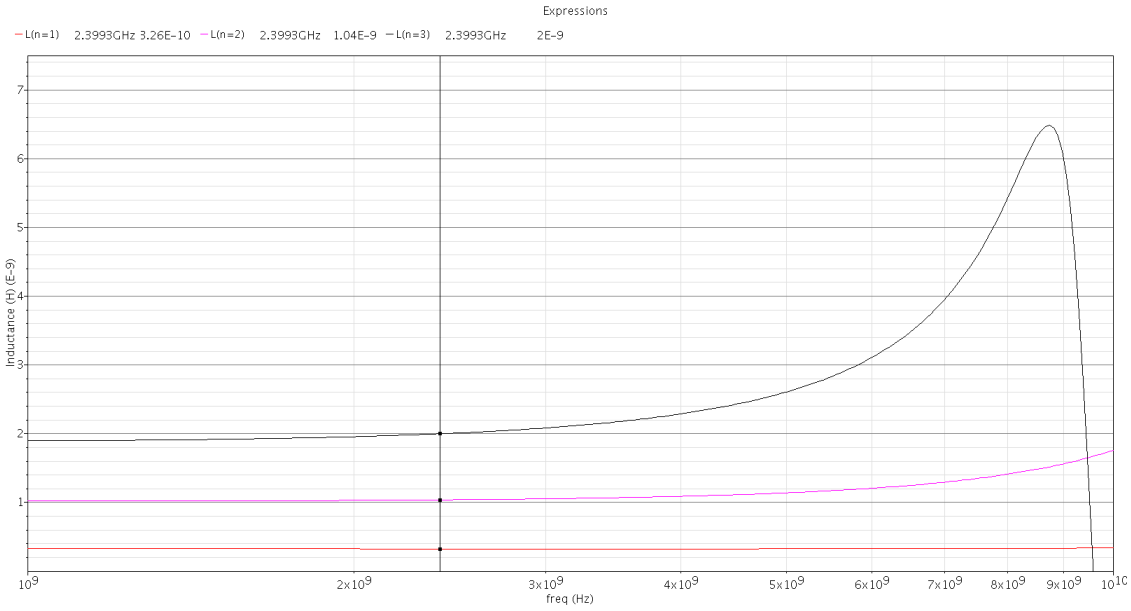

Figure E.3: Inductance vs. Turns.

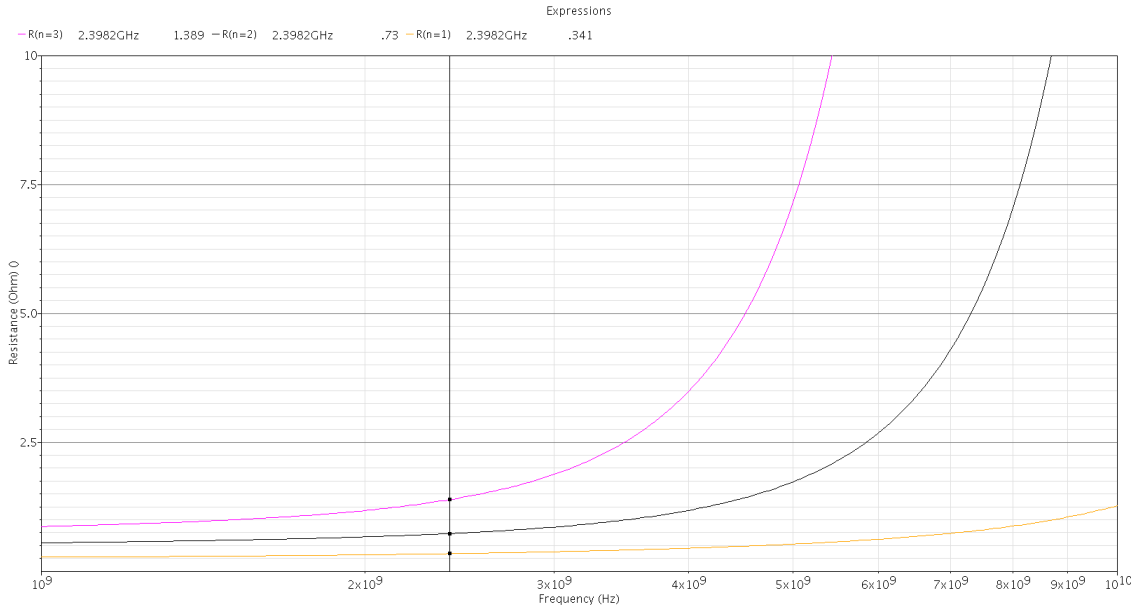

Figure E.4: Resistance vs. Turns.

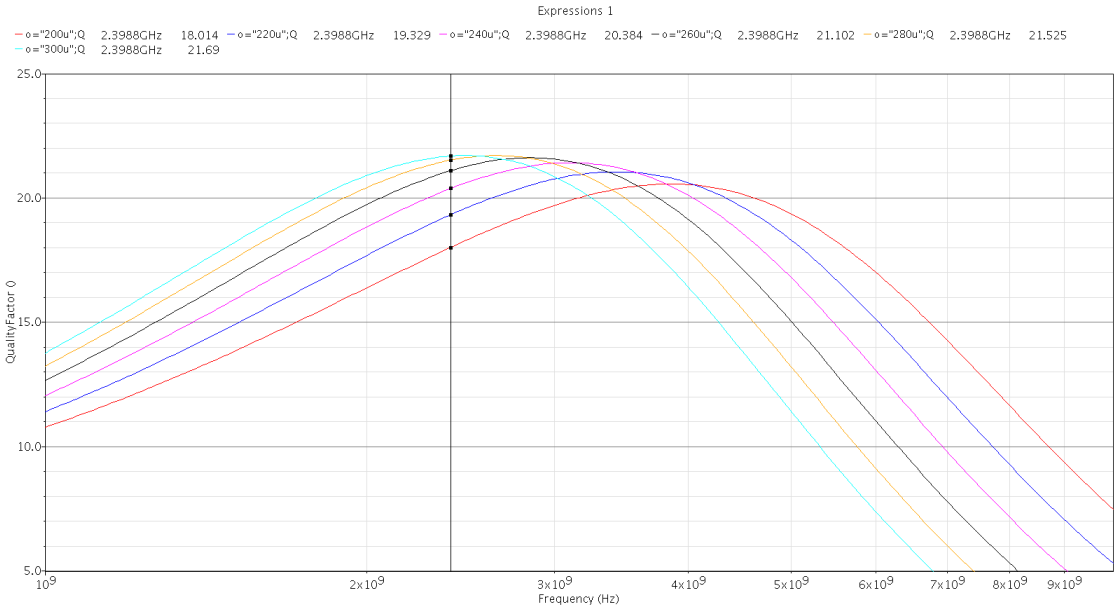

Figure E.5: Quality factor vs. Outer dimension.

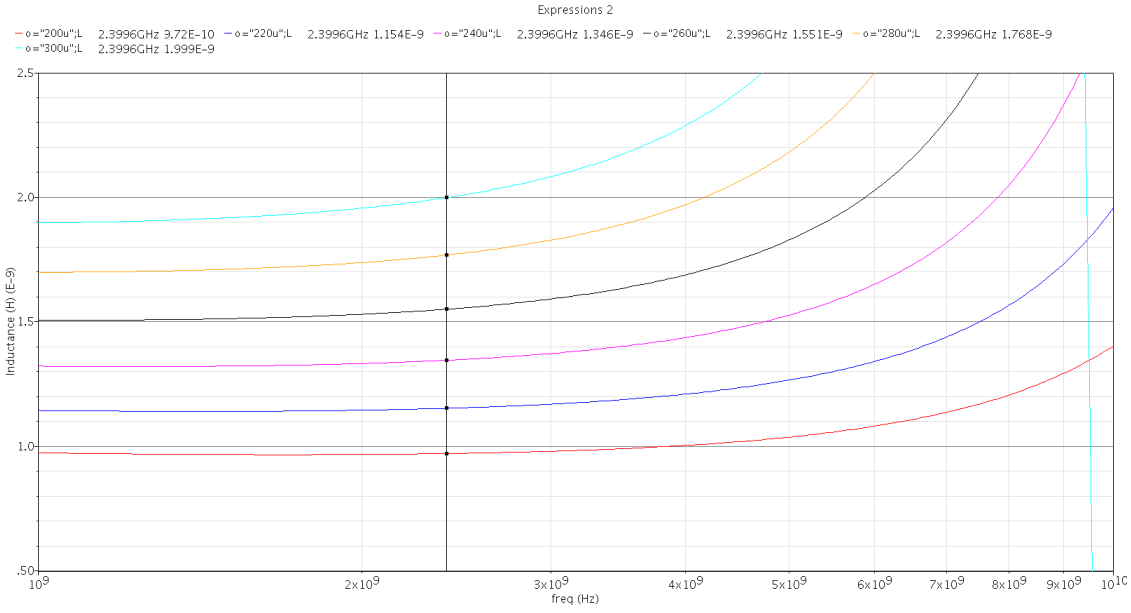

Figure E.6: Inductance vs. Outer dimension

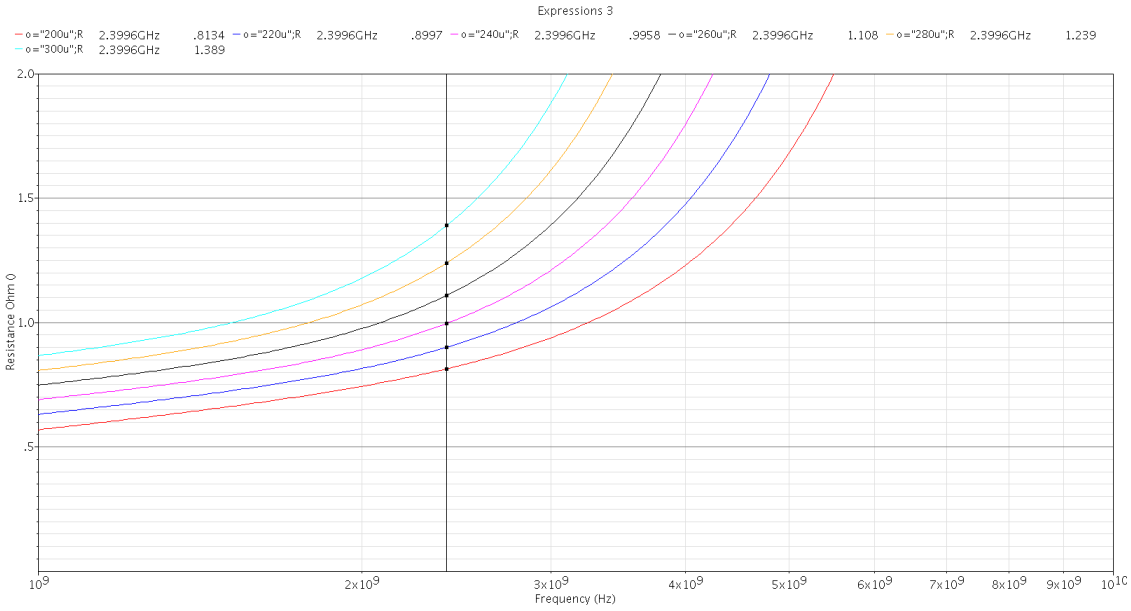

Figure E.7: Resistance vs. Outer dimension.

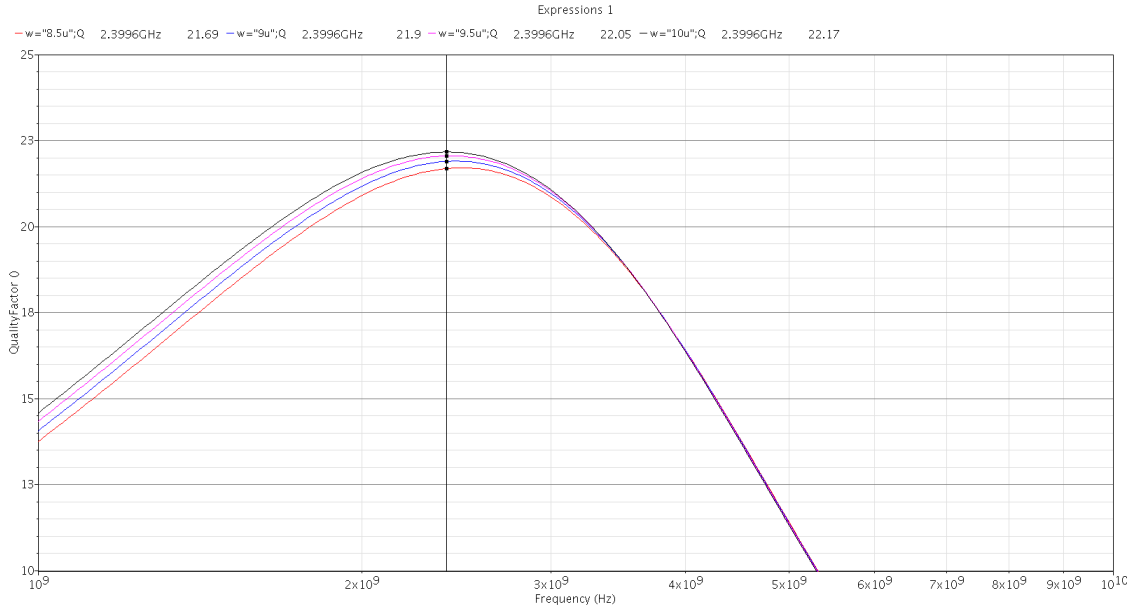

Figure E.8: Quality factor vs. Coil width

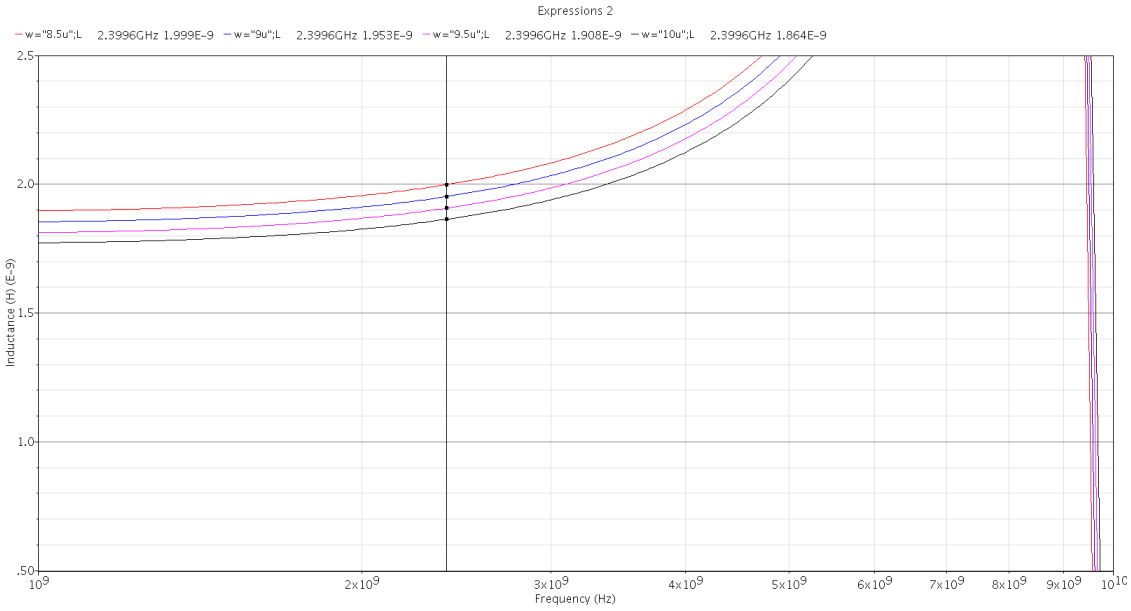

Figure E.9: Inductance vs. Coil width.

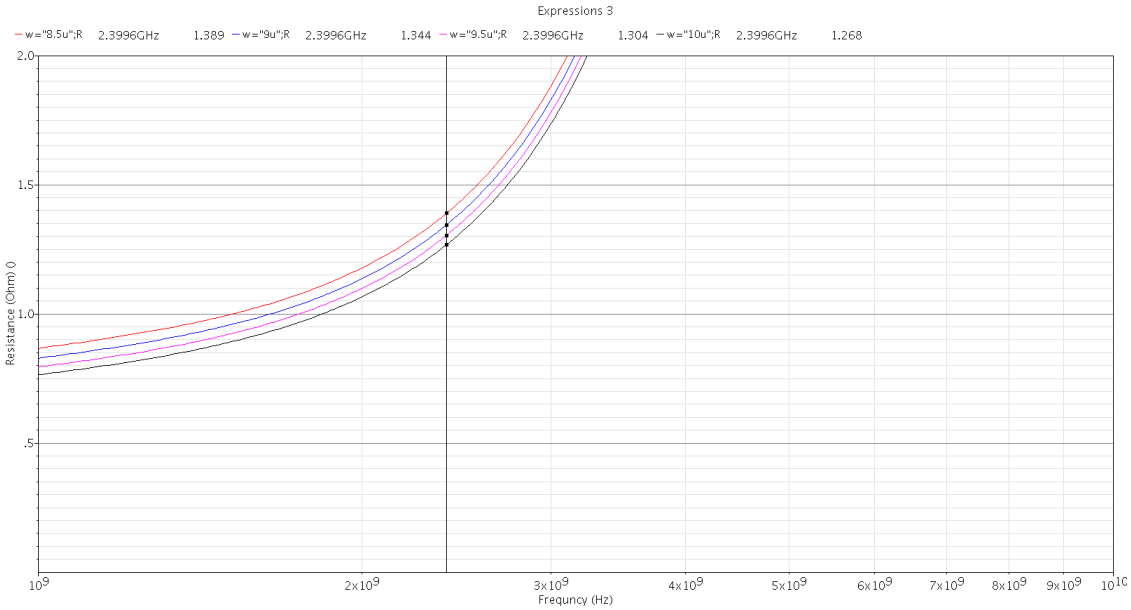

Figure E.10: Resistance vs. Coil width.

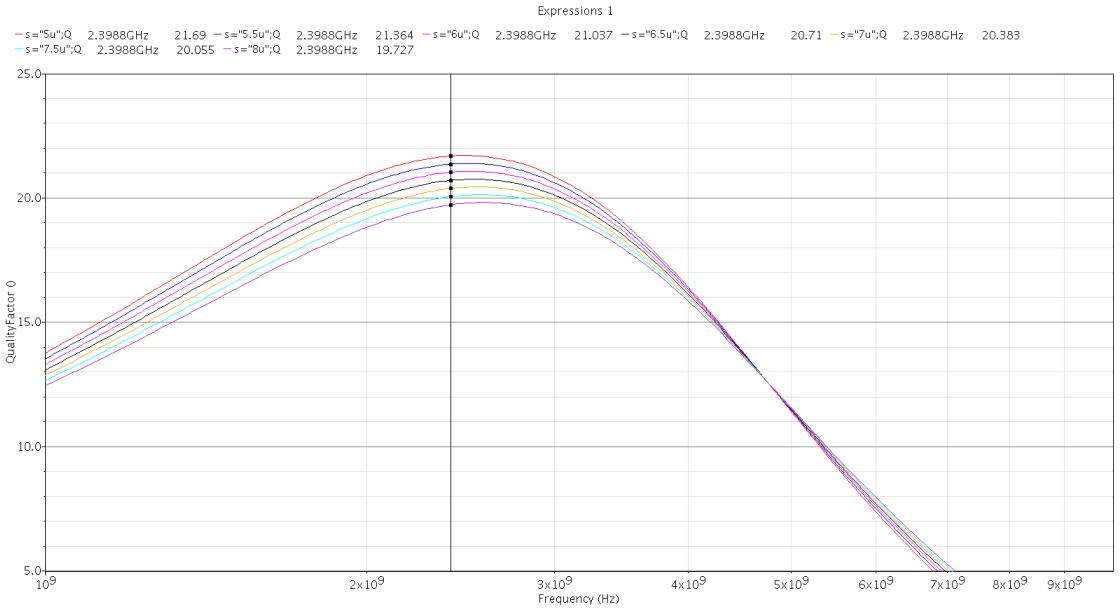

Figure E.11: Quality factor vs. Space

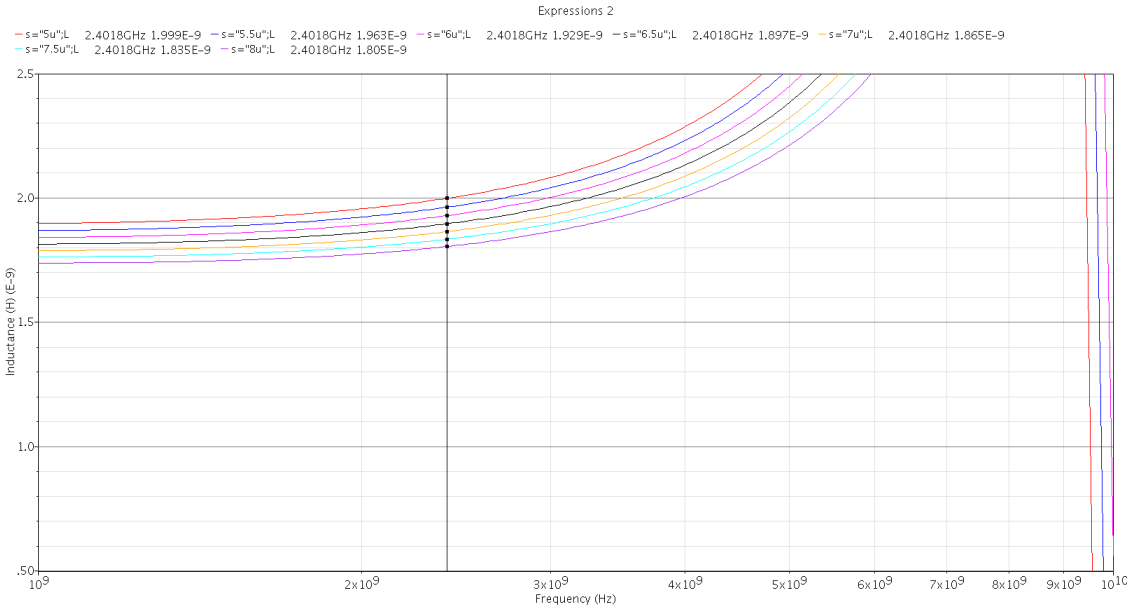

Figure E.12: Inductance vs. Space

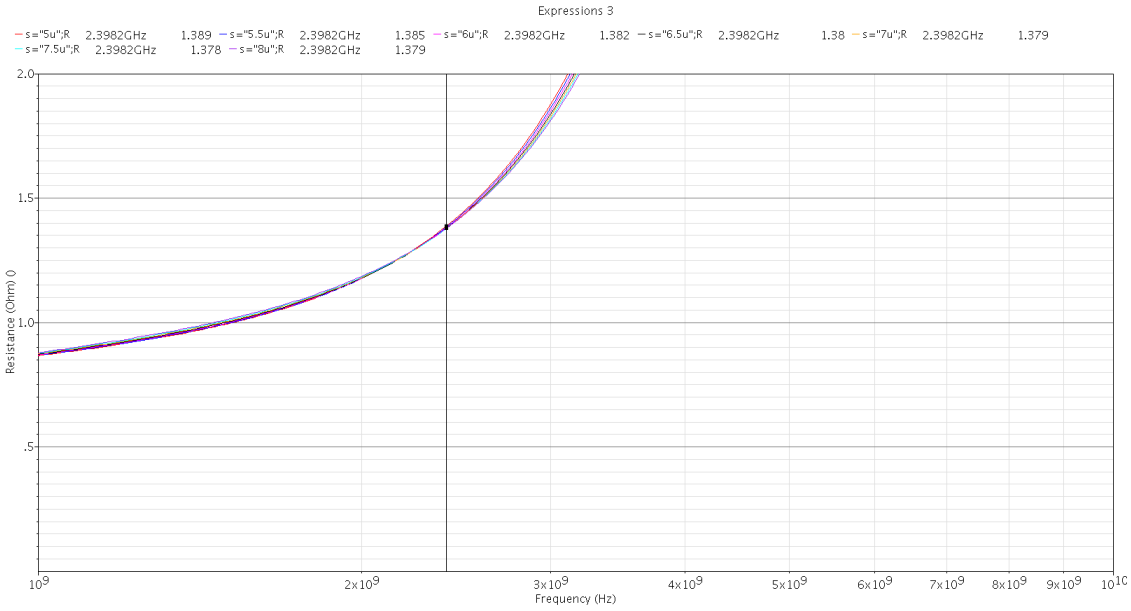

Figure E.13: Resistance vs. Space

Table 21: *Q*, *L*, *R* vs. *N* at 2.4GHz.

	Q	***L* (nH)**	***R*(ohm)**
***N* = 1**	15.4	0.126	0.342
***N* = 2**	21.2	1.04	0.71
***N* = 3**	21.7	2.00	1.389

Table 22: *Q*, *L*, *R* vs. *O* when *N* = 3 at 2.4GHz.

	Q	***L* (nH)**	***R*(ohm)**
***O* = 200um**	18.014	0.972	0.8134
***O* = 220um**	19.329	1.154	0.8997
***O* = 240um**	20.384	1.346	0.9958
***O* = 260um**	21.102	1.551	1.108
***O* = 280um**	21.525	1.768	1.239
***O* = 300um**	21.69	2.00	1.389

Table 23: *Q*, *L*, *R* vs. *W* when *N* = 3 and *O* = 300um at 2.4GHz.

	Q	***L* (nH)**	***R*(ohm)**
***W* = 8.5um**	21.69	2.00	1.389
***W* = 9.0um**	21.9	1.953	1.344
***W* = 9.5um**	22.05	1.908	1.304
***W* = 10.0um**	22.17	1.864	1.268

Table 24: *Q*, *L*, *R* vs. *S* when *N* = 3, *O* = 300um and *W* = 8.5um at 2.4GHz

	Q	***L* (nH)**	***R*(ohm)**
***S* = 5.0um**	21.69	2.00	1.389
***S* = 5.5um**	21.364	1.963	1.385
***S* = 6.0um**	21.037	1.929	1.382
***S* = 6.5um**	20.71	1.897	1.38
***S* = 7.0um**	20.383	1.865	1.379
***S* = 7.5um**	20.055	1.835	1.378
***S* = 8.0um**	19.727	1.805	1.379

Note that all the inductance and resistance are single-ended value.