***A Study in Low-Power Wireless Transceiver
Architectures in Submicron CMOS
Technology***

by

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Abstract

Wireless radio transceiver design has experienced tremendous advances in the past few years. This is mainly attributed to the emergence of a large number of applications for wireless communications, as well as the rapid advancements in fabrication technologies. The designers' aim is always for a simpler, more compact, less power hungry transceiver architecture. To achieve these goals, most of the transceiver building blocks should be integrated within the transceiver chip, with as minimum number of off-chip components as possible. In addition, a suitable transceiver topology that renders itself easily for integration should be adopted. Furthermore, an implementation technology that can readily accommodate mixed signal integration at a smaller form factor, less power dissipation and lower price is desired.

In an attempt to address the above mentioned challenges in wireless transceiver design, this research presents a study towards the implementation of a simple, low-power and compact full transmit path based on Q-enhanced techniques, using one of the leading technologies in wireless transceiver design, namely, CMOS technology. A transmitter structure, based on the well-known direct conversion architecture, is proposed. Within the proposed structure, the frequency synthesizer is based on *Subharmonic Injection Locking* technique, using a low-power, low-frequency clock PLL as an injection source. This is intended as a replacement for the usual high power RF PLL used for tuning the transmitter to different channels. A theoretical analysis of subharmonic injection locking using a periodic square waveform as an injection source is performed. Voltage controlled

oscillators, with different centre frequencies, are implemented to validate the derived formulas predicting the locking bandwidths using subharmonic injection. Using direct digital frequency tuning of the oscillator's centre frequency, the local oscillator pulling "*LO pulling*" by the strong power amplifier output, a well-known problem in direct conversion transmitter architectures, is alleviated without the need of any additional circuitry.

The proposed transmitter structure relies on the sharing of circuits between the receiver and the transmitter to save silicon area as well as required power. To this end, a Q-enhanced LC filter used in the receive chain as a band select filter is reused in the transmit chain as a local oscillator. This prompted a detailed study into the structure of these filters, the possibility of fully integrating them, their power consumption, and their tuning algorithms. Important practical considerations surrounding the implementation of high frequency Q-enhanced LC filters in 0.18 μ m silicon CMOS process are investigated, including realizing the necessary on-chip spiral inductors and Q-enhancement circuits, predicting frequency and Q tolerances and temperature stability, and developing real-time direct digital frequency and Q tuning mechanisms. A prototype filter intended for the 5-GHz band of communications is designed to validate theoretical predictions. The promising experimental results obtained for the implemented prototype illustrate that Q-enhanced LC filters can play an important role in the development of future integrated transceiver products.

To my parents, my wife, and my children

Mariam and Abdel-Rahman

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List of Symbols and Abbreviations

Symbols

B	Filter bandwidth
C_{gs}	Gate-Source capacitance
e	Input signal into an injection-locked oscillator
F	Noise factor
$f(e)$	Nonlinear relation between the input and output of an oscillator
f_o	Filter (Oscillator) center frequency
f_s	Sampling frequency
Δf_o	Frequency offset from an oscillator's center frequency
Δf_n	Injection-locked oscillator locking bandwidth when locked using n^{th} harmonic of a low frequency clock
$\Delta\Sigma$	Delta-Sigma
g_p	Equivalent parallel loss transconductance of on-chip inductor at resonance
g_{mn}	Negative transconductance designed for offsetting the circuit losses
g_i	Input transconductance
g_o	Output transconductance
K	Boltzmann's Constant
mS	milli-Siemens (1/1k Ω)
P_{osc}	Oscillator output power at 1-dB compression point

Q	Quality Factor
Q_o	Un-enhanced Quality Factor
Q_l	Loaded quality factor
u	Output signal of an injection-locked oscillator
v_o	Oscillator output voltage
V_o	Complex oscillator output voltage
v_{inj}	Injection voltage
T	Absolute temperature in Kelvin
x	A constant that ranges between (1-1.22)
$\delta(f)$	Delta Dirac Function

Abbreviations

ADC	Analog to Digital Converter
ACPR	Adjacent Channel Power Ratio
BPF.....	Band Pass Filter
BPSK.....	Binary Phase Shift Keying
CCDF	Complementary Cumulative Distribution Function
CMOS.....	Complementary Metal-Oxide Semiconductor
CP	Charge Pump
DAC	Digital to Analog Converter
DR	Dynamic Range
dB	decibel
dBc	decibels with respect to the carrier
dBm	milli-decibel (decibels with respect to 1 mW)

EVMError Vector Magnitude
 FIB.....Focused Ionized Beam
 FPGA.....Field Programmable Gate Array
 FUMFrequency Upconverter Mixer
 GSMGlobal System for Mobile Communications
 GPS.....Global Positioning System
 GPIB.....General Purpose Interface Bus
 HRM.....Harmonic Rejection Mixer
 ICIntegrated Circuit
 IFIntermediate Frequency
 ILFDInjection-Locked Frequency Divider
 ILOInjection Locked Oscillator
 IP2Second Order Inter-modulation Product intercept point
 IP3Third Order Inter-modulation Product intercept point
 LNA.....Low Noise Amplifier
 LBWLocking BandWidth
 LO.....Local Oscillator
 LPFLow Pass Filter
 MOSFETMetal-Oxide-Semiconductor Field Effect Transistor
 NF.....Noise Figure
 OPLL.....Offset Phase-locked loop
 PA.....Power Amplifier
 PAN.....Personal Area Network
 PCS.....Personal Communications Systems

PFD.....Phase/Frequency Detector
 PLL.....Phase-Locked Loop
 PREAMPPreamplifier
 PSD.....Power Spectral Density
 RFRadio Frequency
 RFICRadio Frequency Integrated Circuit
 RxReceiver
 SAWSurface Acoustic Wave
 SRDRSpurious Free Dynamic Range
 SNRSignal to Noise Ratio
 SO.....Synchronous Oscillator
 SOC.....System On-a-Chip
 TxTransmitter
 VCOVoltage Controlled Oscillator
 VCXO.....Voltage Controlled Crystal Oscillator
 WLANsWireless Local Area Networks
 WPANsWireless Personal Area Networks

Chapter 1. Introduction

1.1 Introduction

Recent advancements in integrated circuit analog/RF electronic design can be attributed to the continuous research in wireless communications due to the huge increase in wireless applications. With the advent of cellular/cordless phones and other battery-operated portable Personal Communications Systems “PCS”, and the widespread use of Wireless Local/Personal Area Networks “WLANs/WPANs”, the development of a fully integrated and more power/size efficient front end architectures has become a key issue for the implementation of new generations of wireless RF transceivers. In an attempt to do so, research efforts have proceeded on many fronts, with the major effort dedicated to communications systems architectures, circuit design, and semiconductor technology areas [1]-[6].

Earlier transceiver implementations usually used a mix of technologies to implement the various functions. As the push for high-integration implementations increased, the use of a single technology for most of the transceiver functions became inevitable [2]. While the use of Complementary metal-oxide semiconductors “CMOS” is the preferred choice for implementing the digital part of the transceiver, Radio Frequency Integrated Circuits “RFICs” have traditionally been implemented using silicon Bipolar, Gallium Arsenide or Si-Ge technologies. The use of CMOS in RFIC design was not seriously considered until the mid-1990s [6]. CMOS technologies have lately developed a

strong presence in the commercial world for RFIC design. Furthermore, they are now dominant for applications such as WLANs/WPANs, and are making inroads into areas such as Global System for Mobile Communications “GSM” cellular transceivers and Global Positioning System “GPS” receivers [6].

1.2 Focus of the Thesis

The focus of this thesis is the design and implementation of a compact, small, cheap, and low-power wireless transmitter architecture that renders itself easily for fabrication. This architecture is intended mainly for use in low-power applications like the fast growing WLANs/PANs networking applications aimed at the Industrial, Scientific and Medical unlicensed frequency band “ISM”. In due course, a transmitter architecture is proposed. All the circuits in the transmit path are designed and implemented using the standard fabrication technology, TSMC 0.18 μ m standard CMOS . A simple and power efficient technique that alleviates Power Amplifier “PA” pulling is used. A structure that allows channel selection using a low-frequency clock synthesizer, rather than a power hungry RF synthesizer, is proposed.

1.3 Thesis Motivation

Based on the brief overview of wireless transceiver design presented in section 1.1, this thesis is mainly motivated by a desire to implement a highly integrated transmit path based on Q-enhanced techniques, with CMOS as the technology of choice. In an attempt to do so, Q-enhanced filter design is explored with an emphasis on implementing higher frequency filters with direct digital tuning. A direct conversion architecture is adopted as the best choice for a simpler, more compact structure. In addition, the proposed transmit structure reuses some of the receiver circuits for better integration.

Specifically, one of the Q-enhanced filters used for band selection in the receive path is converted to a Local Oscillator “LO” in the transmit path.

Two major problems have to be solved before the proposed structure can work satisfactorily. First, direct conversion transmitter architectures suffer from a major problem known as “LO pulling”, where the strong Power Amplifier “PA” output can corrupt the LO signal. Second, is the poor phase noise of the standalone Q-enhanced oscillator, since the circuit is not optimized to work as an LO. To overcome these problems, a low-power technique has to be applied. Injection-locking the LO with an external signal is chosen as a simple and inexpensive solution to overcome the above mentioned hurdles. For this purpose, the area of Injection-Locked Oscillators “ILOs” is reviewed and the different types of injection locking are explored. An emphasis is directed towards subharmonic injection locking, which presents an attractive alternative in the proposed transmit structure. Based on the information introduced in the literature, the mathematical formulation of subharmonic injection locking is presented; the different parameters affecting the locking range and the phase noise at different subharmonic orders are addressed.

1.4 List of Contributions

The original contributions emerging from this work can be summarized as follows:

- (i) *Proposing a structure for a transceiver transmit path that makes use of Q-enhancement techniques, and reuses some of the receiver blocks thus minimizing the required silicon area and needed power.*
- (ii) *Derivation of a general expression for the Locking BandWidth “LBW” of an injection locked oscillator using the n^{th} harmonic of a periodic pulse waveform.*

- (iii) Application of the derived LBW general expression to specific orders of injection, and using this to arrive at closed form formulas for the LBW of a subharmonic ILO using the third, fifth, seventh, ninth, and eleventh harmonics of the injected signal.*
- (vi) Implementation of a digitally controlled subharmonic injection-locked VCO, with very good phase noise, using a clock PLL while dissipating minimal power.*
- (v) Introducing a simple, effective, and very low power consumption method of alleviating LO pulling in direct conversion transmitters.*
- (vi) Design and Implementation of the first to be reported 5 GHz CMOS Q-enhanced filter with a direct digital tuning structure.*

1.5 Thesis Organization

The thesis is organized into seven chapters and three appendices. A brief description of the contents of each chapter and appendix is presented hereafter.

Chapter 1 provides a general introduction to the thesis. It explains the focus of the thesis and the motivation behind this work. Furthermore, it outlines the list of contributions emerging from this research and briefly presents the thesis organization.

Chapter 2 discusses the various available transmitter architectures with an emphasis on the direct-conversion structure. The design parameters of radio transmitters are explained. The most recently reported work on highly integrated wireless transceiver chips intended for wireless networking are covered.

Chapter 3 presents the concept of injection locking of oscillators. Phase noise of oscillators and its effects on both the receiver/transmitter is explained. The different

available types of oscillator injection locking are presented, with emphasis on subharmonic type of injection. A review of the analysis, reported in the literature, of the locking bandwidth and phase noise of subharmonic injection locked oscillators is presented.

Chapter 4 introduces the concept of Q-enhanced filters, their basic architecture, tuning algorithms, noise and dynamic range expressions. The use of a Q-enhanced filter, as a free running oscillator, is then clarified.

Chapter 5 presents a proposed simple structure, based on subharmonic injection, for a highly integrated transmitter intended for WLANs/WPANs applications. The functional building blocks for this direct conversion architecture are explained. A detailed analytical study for the LBW of a subharmonic injection locked oscillator using the n^{th} harmonic of a periodic pulse waveform is presented. Then formulas depicting the LBW of an ILO using up to the eleventh subharmonic are derived. Comparison between analytical results and measurement results is presented, using different subharmonics for injection. Based on obtained injection locking results, a method for alleviating LO pulling by the PA is suggested and verified. The circuit design and simulation/measurement results of the implemented RF building blocks of the proposed transmitter structure are explained. A quantification of the performance of the proposed transmit structure is presented.

Chapter 6 introduces a proposed Q-enhanced filter architecture to be used in the transceiver structure presented in chapter 5. This architecture is applied towards the design of a high frequency, 5 GHz, Q-enhanced filter intended for use as a front-end RF filter. The simulation and circuit design of the designed filter are included, followed by

the obtained measurement results. Comparison of the filter to existing reported designs is then presented.

Chapter 7 outlines the conclusions drawn from this research. It also proposes some future research possibilities initiated by this work.

Appendix “A” provides the designed chips’ layout diagrams.

Appendix “B” presents the Matlab code used for tuning of the proposed Q-enhanced filter.

Appendix “C” provides some mathematical polynomial & trigonometric functions used in the derivations presented in the thesis.

References cited within the context of the document are listed in order at the end of the thesis.

Chapter 2. Transceiver Architectures

2.1 Introduction

The major challenge in RF transceiver design is to utilize, more effectively, the continuously scaling technologies in order to improve the integration level of RF transceivers. This should result in further improvements in power dissipation, form factor, and cost [2]. A wireless transceiver consists of 2 main parts, an analog RF front-end which performs frequency upconversion/downconversion of the modulated information signal, and a digital back end where the actual modulation/demodulation of the signal takes place, through extensive use of digital signal processing techniques. Although the continued downscaling of current technologies has resulted in better integration and lower power consumption in the transceiver back end, this is not the case for the front end, where integration level and lower power consumption is more related to the physical limitations of the transceiver topology rather than the used technology. Thus, it is this analog transceiver front-end, the part which represents the interface between the antenna and the digital signal processing back end, that is the main bottleneck for advancements in RF transceiver design [7].

CMOS technology rapidly took over the digital market owing to their lower power dissipation, smaller size and increased number of devices [8]. It took some time until CMOS challenged other technologies in the RF field with CMOS circuits operating in the GHz band. Until the early 90s, FETs were always considered slower and noisier

than their bipolar counterparts, yet the rapid scaling in their processing technology, the device miniaturization, and the lower power dissipation and fabrication cost have made CMOS a highly desirable technology for RF integration [9][10][11].

Wireless transceiver design, and the need for creating a compact, power efficient system-on-a-chip requires that both the digital and analog/RF circuitry to be implemented on the same chip. CMOS has proved to be a strong contender in this field, with the larger amount of digital circuitry benefiting from a higher transistor density and therefore smaller size and lower fabrication cost [10]. This explains the greater tendency, in recently published RF-CMOS work, towards single-chip transceiver realization than seen in contemporary IC's for cellular and cordless telephones developed in industry [3], [5], [11]-[15].

Most of the research effort has been directed towards the CMOS implementation of fully integrated wireless receivers [16]. Very few researchers have addressed the transmitter side [17]. The focus of this thesis is to demonstrate a low-power, simple solution that would help eliminate the need for costly discrete components and allow for a fully integrated CMOS transmitter.

In the following section, an overview of the different existing transmitter architectures is presented together with advantages and disadvantages of each structure.

2.2. Transmitter Architectures

Transmitter implementations to date have used a variety of architectures, each exhibiting its own features that makes it well suited for implementing a specific standard. The choice of a transmitter structure is mainly determined by two important factors: wanted and unwanted emissions requirements and the number of required oscillators and

external filters. In general, the architecture and frequency planning of the transmitter must be selected in conjunction with that of the receiver to allow sharing hardware and possibly power [18].

2.2.1. Direct-Conversion Architecture (Homodyne; Cartesian)

In direct-conversion transmitters, the modulated baseband signal is directly upconverted to the carrier frequency when mixed with an oscillator output running at the same carrier frequency i.e. there is no intermediate frequency involved. The modulation and upconversion of the signal usually occurs in the same circuit. The simplicity of the topology has made it an attractive choice especially for the newer emerging transceivers that aim at higher levels of integration and smaller form factor. Figure 2.1 depicts an example of direct conversion transmitter architecture.

Figure 2.1 A Direct Conversion Transmitter Architecture

Though being extensively used in the past few years for implementing transceivers for portable devices as well as wireless LANs, direct conversion does not come without disadvantages. The fact that the LO frequency is the same as the transmitted frequency creates 2 main problems. The first, is the inevitable large crosstalk or feedthrough of the LO signal to the RF output of the upconversion mixer [7]. The second and most serious problem, is the “*Injection Pulling*” of the LO by the PA output.

The disturbance of the LO by the PA output is a natural issue that arises because the PA output is a modulated high power waveform that's centered around the LO frequency. This may corrupt the LO output. This problem becomes more severe when the PA is integrated on the same chip.

Different methods of alleviating this problem have been proposed in the literature. The majority of these approaches use a method that offsets the LO frequency from the transmit frequency. However, they differ in how this is implemented. For example, a commercial product introduced by Maxim in 2000, the MAX2720/2721 has an external LO running at half the transmit frequency which then goes through an on-chip doubler before mixing it with the baseband signal. The chip functional diagram is shown in Figure 2.2.

Figure 2.2 Functional Diagram of MAX2720/2721 © 2000 Maxim

Another approach introduced in [19], depends on adding an extra VCO, see Figure 2.3. The outputs of the two VCOs, at ω_1 and ω_2 , are first mixed together. The

resulting signal, at $\omega_1 + \omega_2$, is used as the reference LO signal for upconversion. In this case, neither of the VCOs runs at the transmitted PA frequency.

Figure 2.3 A Direct-Conversion Transmitter with additional VCO

2.2.2. Heterodyne Architecture (Two-Step)

Another approach to circumvent the problem of LO pulling in transmitters is to upconvert the baseband signal in two (or more) steps so that the PA output is far from the frequency of the LO VCO. It can be viewed as the transmitter version of the superheterodyne receiver structure.

The Heterodyne transmitter topology is still the most often used transmitter topology. Its basic structure is shown in Figure 2.4. The baseband signal is frequency translated to a fixed IF, at frequency ω_1 . Then the IF signal is upconverted to the RF transmitted signal, at frequency $\omega_1 + \omega_2$. The heterodyne transmitter structure has a number of advantages over its homodyne counterpart. First, LO feedthrough is reduced owing to the lower frequency used in the modulator. Second, LO pulling is approx. alleviated since neither oscillator is operating at the transmitter frequency. A major drawback of the Heterodyne transmitter topology is the design of the second BPF following the final upconversion. The final mixing process results in both sidebands with equal magnitudes; the filter has to reject the unwanted sideband by typically between 50

and 60 dB. Owing to the high frequency of operation, this filter is usually implemented as a passive off-chip, relatively expensive, filter [18].

Figure 2.4 A Heterodyne (Two-step) Transmitter Architecture

2.2.3. Offset-PLL (OPLL) Architecture

This is a transmitter topology suited for low cost, high performance systems utilizing constant-envelope modulation. It was primarily introduced to meet the stringent requirements on the GSM compliant transceivers [20][21].

Figure 2.5 shows the concept of an Offset-PLL “OPLL” transmitter architecture. An OPLL consists of an offset downconverter mixer, a phase detector, a loop filter, a Tx-VCO, and an RF-VCO. When the OPLL gets locked to the reference IF signal, the frequency of the Tx-VCO is offset from the frequency of the RF-VCO by f_{IF} ($f_o = f_{RF} - f_{IF}$). The OPLL acts as a tracking narrowband BPF centered around the transmit frequency, f_o , thereby suppressing the out-of-band noise floor generated by the quadrature modulator and upconversion. If the loop bandwidth of the PLL is chosen appropriately, the phase information in f_{IF} is transferred faithfully to f_o while the output noise at large frequency offsets is determined solely by the Tx-VCO [20].

Figure 2.5 Offset PLL Transmitter Architecture

The main advantage of the offset-PLL topology is that it provides low out-of-band noise, which allows the transceiver to get rid of the duplexer all together, thereby saving a portion of the power produced by the PA and reducing the overall system cost. On the other hand, offset-PLL topology has a number of disadvantages. It is more complex than the above described two topologies. In addition, it requires more circuitry in the form of two high frequency VCOs and a relatively selective filter [18].

2.2.4. Direct Modulation Architecture

One of the possible configurations for the transmitter is by directly frequency modulating the transmitter PLL frequency synthesizer in an architecture called “*Direct Synthesizer Modulation*”, shown in Figure 2.6 [22]. This method is attractive because it eliminates the upconversion mixer and offers a potentially less size, and power solution to both frequency synthesis and modulation. Unfortunately, it suffers from a very important drawback, namely attenuating modulation components that lie within its bandwidth. This problem is more severe especially at higher data rates, due to the need

for higher loop bandwidth to allow modulation to pass through [22]. A higher PLL loop bandwidth contradicts the need for a narrower bandwidth to suppress the higher levels of quantization noise of the phase/frequency detector, and the modulator.

Figure 2.6 Direct Synthesizer Modulation Transmit Architecture

To circumvent this problem, a two-point modulation direct modulation scheme has been introduced as an alternative, with the modulation applied in two paths; a low frequency path to the PLL reference input & a high frequency path to the PLL VCO. Thus, the PLL presents a LPF response for the signal applied to its reference input, while it presents a HPF response to the signal applied to its VCO, resulting an overall flat frequency modulation response versus modulation frequency [24].

An example implementation based on a PLL using multi-modulus divider driven by a multi-bit Delta-Sigma “ $\Delta\Sigma$ ” modulator intended for use in a transmitter conforming to the IEEE 802.15.4 communications standard is shown in Figure 2.7 [23].

The 2-point PLL combines the LO frequency synthesis with the modulation circuits to achieve a compact modulation structure with the minimum number of analog components. Since it eliminates the upconversion section of the transmitter altogether,

the 2-point modulation scheme is an attractive choice for transmitters where size, cost and power consumption are the main steering factors [22]. Although the two-point modulation structure adds complexity to circuit design, it is primarily in the digital circuit part, which in most modern IC technologies adds little to die size [23].

Figure 2.7 A Two-Point $\Delta\Sigma$ PLL Transmitter for IEEE 802.15.4 Standard

Among the drawbacks of such a structure is the risk associated with modulation of the reference oscillator. The reference in the same time is the basic clock frequency for the baseband digital circuitry. This may cause problems for other parts of the transceiver using the same clock source. In addition, it is not suitable for all types of synthesizers [22]. Another problem is that of calibrating the high frequency VCO modulation path. This problem has been addressed by several researchers [24][25].

2.3 Transmitter Performance Measures

Transmitter performance measurements can be classified as either in-band or out of band measurements, regardless of the technology used or standard followed [26]. A brief description of the most popular measurements needed for transmitters is presented in the following subsections

2.3.1 In-Band measurements

In-band measurements are measurements performed within the frequency band allocated for the system. In-band measurements can be classified as either in-channel or out-of-channel measurements.

A. In-Channel measurements

A.1 Channel bandwidth

A transmitter spectrum must be tested to ensure that no major errors exist in the design. For example, for a transmitter with a root-raised cosine filter, as in the IEEE802.15 standard used in Wireless Personal Area Networks (PANs), usually the 3 dB bandwidth of the modulated frequency channel is approx. equal to the channel symbol rate.

A.2 Carrier frequency

A designer must ensure that the transmitter is operating on the correct carrier frequency. The carrier frequency of a specific channel should always be located at the center of the spectrum for most modulation formats. It can be approximated by calculating the center of the 3dB bandwidth.

A.3 Channel power

Channel power is the average power in the frequency bandwidth of the signal of interest.

Though this measurement is usually done by integrating the power over the frequency band of interest, the actual measurement method usually depends on the specific communication standard followed.

A.4 Occupied Bandwidth

Occupied bandwidth indicates how much frequency spectrum is covered by some given percentage (usually 99%) of the total power of the modulated signal. Any distortion, whether harmonic or intermodulation, dissipates some power outside the specified bandwidth.

A.5 Peak-to-average Power Ratio and CCDF Curves

These are statistical measurements on the time domain signal. They are particularly important in digitally-modulated systems because the statistics may vary.

The Peak-to-average ratio is the ratio of the peak envelope power to the average envelope power of a signal during a given period of time. Some instruments may provide peak-to-average power statistics; the peak envelope power is not given as an absolute value, but rather as the power level associated with a certain probability.

The power statistics of the signal is usually characterized by performing several of these measurements and displaying the results in a graph known as the Complementary Cumulative Distribution Function "CCDF". The CCDF curve shows the probability that the power is equal or above a certain peak-to-average ratio, for different probabilities and peak-to-average ratios. The higher the peak-to-average power ratio, the lower the probability of reaching it.

A.6 Error Vector Magnitude "EVM"

Error Vector Magnitude "EVM" is the most widely used modulation quality metric in digital communications systems. When performing EVM measurements, the analyzer samples the transmitter output to capture the actual signal trajectory. The signal is demodulated and a reference signal is mathematically derived. The error vector is the

vector difference at a given time between the ideal reference signal and the measured signal. Figure 2.8 shows an interpretation of the error vector.

Figure 2.8 Error Vector Definition

The EVM is the root-mean-square value of the error vector over time at the instants of the symbol clock transitions. It is usually normalized to either the amplitude of the outermost symbol or the square root of the average signal power. An example of an actual measurement showing the constellation diagram, the magnitude and spectrum of the signal EVM, as well as a summary table is shown in Figure 2.9.

Figure 2.9 Example of an EVM Measurement

B. Out-of-Channel measurements

B.1 Adjacent Channel Power Ratio (ACPR)

Regardless of the technology used for building up the transmitter or the standard followed, Adjacent Channel Power “ACP” measurements are required to make sure that the transmitter is not interfering with adjacent or alternate channels. Adjacent Channel Power Ratio “ACPR” is defined as the ratio of the average power in the adjacent frequency channel to the average power in the transmitted frequency channel. ACPR is often measured at multiple offsets (adjacent and alternate channels). Figure 2.10 shows an example of ACPR measurement, where the power is measured across a bandwidth of 1-MHz for both the transmitted and adjacent upper and lower channels.

Figure 2.10 ACPR Measurement Example

B.2 spurious emissions

Spurious emissions are undesired signals caused by different combinations of signals in the transmitter. They can lie either within, or out of the system’s band. Spurious emissions that fall within the system’s band should be below some level specified by the specific communication standard. Usually each standard specifies a “Transmission Mask” that all the transmitters conforming to this specific standard should

abide to. The power produced at any transmitting channel should fall below this mask to guarantee minimum interference with other channels in the system. Figure 2.11 shows examples of the transmit masks for two different standards targeting the WLANs/WPANs applications, namely the relaxed low-data rate IEEE 802.15.4 WPAN and the more strict higher data rate Hyper LAN IEEE 802.11a WLAN.

Figure 2.11 Transmitter Mask for Different WLAN/PAN Standards

2.3.2. Out-of-Band Measurements

Out of band measurements, include measuring levels of out of band spurious and harmonic emissions that lie out of system's standard band to ensure minimum interference with other communication systems. Figure 2.12 shows an example of out-of-band spurious (marker "B") and harmonic emissions (marker "A").

Figure 2.12 Out-of-Band Spurious and Harmonic Measurement

2.4 Recent Reported Research in Wireless Transceiver Design

A highly integrated narrowband transmitter, based on a heterodyne (2-step) transmitter architecture, is introduced in [17]. The block diagram of the reported chip is shown in Figure 2.13. Implemented in $0.35\mu\text{m}$ CMOS, the designed chip integrates the whole transmitter path on the chip except for an RF filter following the used class “C” PA. The use of a class “C” power amplifier makes the above transmitter only suitable for constant envelope modulation standards, like the DCS-1800. The integration of the transmitter implemented in this chip, has been facilitated by the use of a *Harmonic Rejection Mixer “HRM”*, and a wide-loop-bandwidth PLL. The HRM enabled the elimination of an IF filter between the mixer output and the PA input, a normal building block in any heterodyne architecture, which is usually implemented off-chip due to the high quality factor required of this filter. The high power consumption of the proposed architecture is mainly attributed to the implementation of two different synthesizers, one for each LO signal and the use of the HRM.

Figure 2.13 Harmonic Rejection Transmitter Block Diagram [17]

Figure 2.15 A Fully Integrated CMOS RFIC for Bluetooth Applications [29]

The transceiver presented in [30], and shown in Figure 2.16, again uses a direct conversion transmit architecture. However it uses a different scheme for dealing with the LO pulling problem.

Figure 2.16 A 2.4-GHz Transceiver for Bluetooth in 0.35 μ m CMOS [30]

To alleviate LO pulling, the VCO used runs at 1.6 GHz (approx. 2/3 of the transmitted RF frequency of 2.4 GHz used for the Bluetooth standard). Its output is divided by two to produce quadrature 800 MHz signals. The VCO output signal and the 800 MHz quadrature signals are then mixed up to the desired RF of 2.4 GHz, which is

then applied to the TX mixers. Thus, to implement the VCO frequency offsetting from the RF transmitted frequency, two additional mixers are added as shown in

Figure 2.17. The transceiver chip, implemented in $0.35\mu\text{m}$ CMOS, dissipates 47 mA when transmitting 4 dBm output signal, while being powered up by a (2.7-3.3) V supply.

Figure 2.17 VCO Offsetting Scheme used in [30]

A low-power consumption Bluetooth transceiver chip from Ericsson is introduced in [32]. Figure 2.18 shows the radio block diagram, implemented in $0.18\mu\text{m}$ CMOS.

Figure 2.18 A Bluetooth Radio in $0.18\mu\text{m}$ CMOS from Ericsson [32]

As shown in the above figure, the transmitter uses a direct IQ-upconversion architecture. The low frequency I- and Q-signals are generated by a ROM and fed to a DAC. After low pass filtering, mixing and amplification, an on-chip differential PA delivers the required 4 dBm output to the chip pins. The VCO runs at 5 GHz (approx. twice the transmitted frequency). It is then divided by 2 to generate the necessary carrier at 2.4 GHz.

Another low-power CMOS transceiver intended for Bluetooth is introduced in [35]. The block diagram of the implemented transceiver architecture is shown in Figure 2.19 (a). The transceiver, implemented in 0.25 μm CMOS, uses a double conversion architecture for both the receive and transmit paths. The silicon area of the chip and the reported power consumption makes this architecture a contender to the dominating direct conversion architectures. A single frequency synthesizer, running at 1.6 GHz, is used for both the receive and transmit paths. A divide-by-two circuit produces the needed quadrature LO signals at 800 MHz, needed for the first conversion in the transmit path, thus avoiding the need for power-hungry polyphase filters. The authors use circuit stacking techniques for the LNA+mixer combination in the receive side and for the PA in the transmit side, which provides significant power savings (see Figure 2.19 (b)).

Figure 2.19 A Low-power 2.4-GHz Transceiver CMOS IC [35]

A complete Bluetooth radio is presented by Toshiba in [36]. As shown in Figure 2.20, the transceiver uses direct open loop modulation architecture for the transmit path. The shaped data directly modulates the VCO, which runs at the same transmit frequency. To alleviate the VCO frequency pulling, buffers are used to isolate the VCO from both the mixer and the power amplifier. Furthermore, buried n-wells, requiring extra fabrication masks, are used to improve isolation between different analog blocks on the transceiver chip.

Figure 2.20 A Single-Chip CMOS Bluetooth Transceiver from Toshiba [36]

A summary of the most recently reported, highly integrated, wireless transceiver chips is presented in Table 2.1. Important measures, including technology used, transmitter architecture, occupied silicon area, power consumption, and targeted application are mentioned.

Table 2.1 Recent Reported Work in Integrated Wireless Transceiver Design

No.	Published Reference/Year/ Author	Circuit	Used Technology	Transmitter Architecture	Silicon Area [mm ²]	Current [mA]		Supply Voltage [V]	Application
						Rx	Tx		
1.	ISSCC2001 [27] <i>F. O. Eynde, Alcatel</i>	RF+BB	0.25 μ m CMOS	Direct	40	50	70	2.5	Bluetooth
2.	ISSCC2001 [28] <i>N. Filiol, Conexant</i>	RF	0.5 μ m SiGe BiCMOS	2-point $\Delta\Sigma$ modulation	12	16	12	1.8-3.6	Bluetooth
3.	ISSCC2001[29] <i>A. Ajjikutira, et al.</i>	RF	0.35 μ m CMOS	Direct	18	66	47	2.7-3.3	Bluetooth
4.	JSSC2001 [30] <i>H. Darabi, Broadcom</i>	RF	0.35 μ m CMOS	Direct	20	46	47	2.7-3.3	Bluetooth
5.	CICC2001 [31] <i>C. Dürdodt, Infineon</i>	RF+BB	0.25 μ m CMOS	2-point $\Delta\Sigma$ modulation	18.5	N/A	N/A	2.65	Bluetooth
6.	JSSC2002 [32] <i>P. V. Zeijl, et al,</i>	RF	0.18 μ m CMOS	Direct	5.5	30.5	35.5	2.5-3	Bluetooth

Table 2.2 Recent Reported Work in Integrated Wireless Transceiver Design (continued)

No.	Published Reference/Year/ Author	Circuit	Used Technology	Transmitter Architecture	Silicon Area [mm ²]	Current [mA]		Supply Voltage [V]	Application
						Rx	Tx		
7.	ISSCC2002 [33] <i>G. Chang, Silicon Wave Corp.</i>	RF+BB	0.35μm SOI BiCMOS	Direct	19.5	39	37	2.7	Bluetooth
8.	ISSCC2002 [34] <i>J. Cheah, et al.</i>	RF	0.25μm CMOS	Direct	16.5	45	36	3	Bluetooth
9.	JSSC2003 [35] <i>A. Zolfaghari, B. Razavi</i>	RF	0.25μm	Heterodyne	3.66	17.5	16	2.5	Bluetooth
10.	ISSCC2003 [36] <i>Toshiba</i>	RF+BB	0.18μm CMOS, triple-well, MIM capacitor	Direct	29.6	N/A	N/A	2.5	Bluetooth
11.	JSSC2003 [37] <i>P. Choi, et al.</i>	RF	0.18μm CMOS	Direct	8.75	5	10	1.8	802.15.4

2.5 Conclusion

In this chapter, the different existing transmitter architectures are discussed. The various necessary transmitter measures are highlighted. Finally, the most recent work on integrating wireless transceivers on a SOC are reviewed. Most of the reported SOC's are dedicated to the fast evolving wireless networking standards for short-range communication applications like the IEEE802.15.1 "*Bluetooth*" standard. Although the introduction of a complete CMOS wireless transceiver SOC was not until 2001, most of the presented implementations are in CMOS technology. This is mainly attributed to its cost effectiveness for high volume applications as well as better capability of integrating both digital baseband as well as analog RF circuitry without excessive setbacks. The transmitter structure for most of the reported chips relies on a direct conversion scheme to achieve low power consumption and higher degree of integration. Meanwhile, different design schemes are applied to alleviate its known drawback, namely the LO pulling by the PA output.

Chapter 3. Injection Locking of Oscillators

3.1 Introduction

The increase in wireless applications have drawn tremendous research efforts on radio-on-a chip solutions of CMOS transceivers. For wireless transceivers, RF carrier generators are, generally, of PLL-based architecture, and consume significant portion of the whole transceiver power. The VCO and the prescaler, which operate at the highest frequency, dissipate a major part of this power [38]. To minimize the power consumption of RF frequency synthesizers, research efforts have been directed towards implementation of low-power communications-grade integrated VCOs [39][40][41]. Reduction of synthesizer overall power consumption still pushed for other alternatives of frequency division techniques. Most PLLs designed for wireless systems use flip-flop-based digital frequency dividers. Although these types of dividers are capable of operating at very wide bandwidth, their power consumption increases drastically with increasing increments of frequency [42]. This has driven researchers to explore other types of analog dividers. Regenerative as well as parametric frequency dividers were some of the analog alternatives but both had their own drawbacks. The former needs many functional blocks which makes them not the best solution for low-power systems, while the latter are not amenable for integration since they need high Q passive elements, something that cannot be done in contemporary silicon technologies [42]. This has initiated more interest in a third type of analog dividers, namely *injection-locked dividers*.

Injection-Locked Frequency Dividers “ILFDs” are capable of very high frequency of operation while dissipating relatively low power, but at the expense of narrow locking range [43]. Since most wireless transceivers are narrowband, injection locked dividers can be used to trade off bandwidth for power and maximum frequency of operation. Therefore, they present a viable solution for low power and high frequency wireless applications [44].

The process of injection locking is a fundamental property of oscillators [45]. Injection locking is used to lock a free-running oscillator to an incident reference signal, with a presumably better phase noise. When a free running oscillator is injected with a periodic signal f_c it will lock to and track the injected signal over a Locking BandWidth “LBW” or Locking Range “LR” given by “ $f_c \pm \text{LBW}/2$ ”. Within this locking range, the process can be modeled as a true first order PLL [46]. Thus, the phase noise of the output tracks the phase noise of the injected reference over a certain bandwidth analogous to the loop bandwidth of conventional PLLs [47]. The LBW is generally dependent on the level of the injected signal, the oscillator output power, the type of injection used, and the oscillator active core nonlinearity. To accommodate process and environment variations, typical RF applications require an LBW of 25-50 MHz greater than the signal bandwidth. Achieving this LBW requires a large injection signal power [46].

3.2 Phase Noise of Oscillators

3.2.1 General

Oscillators, like any other electronic circuit, are susceptible to noise. This noise causes fluctuations in the oscillator’s amplitude and frequency. Short-term frequency fluctuations of any oscillator, as opposed to long-term fluctuations due to aging, are

caused by internal circuitry noise and external interference sources. Thermal, shot and flicker noise constitute the sources of internal noise, while substrate and supply noise represent the external interferers [48]. These fluctuations are best characterized by two popular quantities, namely, *phase noise* and *timing jitter*. While phase noise is a measure most commonly used by analog/RF designers to characterize oscillators and synthesizers in the frequency domain, timing jitter is the preferred measure for digital designers mainly dealing with clock signals in the time domain.

In the following, a brief overview of oscillator phase noise is presented, the effects of this phase noise on both the receive and transmit paths are mentioned with more emphasis on the transmit side.

3.2.2 Definition

The output of an ideal oscillator, with no random fluctuations, will simply be an impulse at the resonating frequency ω_o . For a practical oscillator, however, the output spectrum exhibits sidebands, or skirts, close to the frequency of oscillation. These sidebands are generally referred to as phase noise sidebands, see Figure 3.1.

Figure 3.1 Output Spectrum of an Ideal and an actual Oscillator

Phase noise is usually defined at an offset $\Delta\omega_o$ with respect to the oscillator carrier ω_o . The noise power, measured in a unit bandwidth, is calculated at this specific

offset, and the result is subsequently divided by the oscillator average carrier power to obtain the phase noise expression.

3.2.3 Phase Noise Expression

One of the most well-known models that describe the phase noise for tuned tank oscillators is presented by Leeson [49]. Based on a linear time-invariant approach, Leeson's model expresses the normalized single-sideband phase noise for oscillator at an offset Δf_o from its free running frequency f_o as [48],

$$\mathcal{L}(\Delta f_o) = 10 \log \left\{ \frac{FKT}{2P_s} \cdot \left[1 + \left(\frac{f_o}{2Q_l \Delta f_o} \right)^2 \right] \left(1 + \frac{f_c}{\Delta f_o} \right) \right\} \quad (3.1)$$

where F is the oscillator active device thermal noise factor

T is the absolute temperature in degree Kelvin

P_s is the average power dissipated in the resistive part of the tank

Q_l is the loaded quality factor of the oscillator tank

f_c is the flicker noise corner frequency

Figure 3.3 shows a typical example plot illustrating the different regions and slopes that can normally be noticed in an oscillator phase noise measurement [50].

Figure 3.2 SSB Oscillator Phase Noise Spectrum

As shown in Figure 3.2, at large offsets, there is a flat noise floor representing the oscillator noise floor. At small offsets, there are two distinct regions with slopes of $1/f^2$ (-20 dB/decade) and $1/f^3$ (-30 dB/decade), respectively, with the corner between them labeled as ω_{1/f^3} .

3.2.4 Effects of Oscillator Phase Noise on Transceivers

On the receive side, oscillator phase noise can lead to increased bit error rates in digital communication systems, and demodulation errors. Furthermore, it can lead to contamination of adjacent channels and receiver desensitization due to reciprocal mixing where out of band signals are translated into the IF [51].

Phase noise is also a very important issue in the transmitter design [52]. Oscillator phase noise can lead to adjacent channel interference and modulation errors. The effect of a transmitter phase noise on adjacent channels can be explained as follows; Assume a noiseless receiver is to detect a weak signal at ω_2 while a powerful, nearby transmitter generates a signal at ω_1 with substantial phase noise. Then the phase noise tail of the transmitter corrupts the wanted signal as shown in Figure 3.3 [53].

Figure 3.3 Effect of Phase Noise in Transmitters

3.3 Types of Injection Locking

Depending upon the ratio of the injection frequency to the free-running oscillation frequency, injection locking can be categorized into three distinct types; First-harmonic (Fundamental), Subharmonic, and Superharmonic [42]. In a first-harmonic Injection-Locked Oscillator “ILO”, the oscillation frequency is the same as the fundamental frequency of the incident signal. Whereas, in a superharmonic ILO, the incident frequency is a harmonic of the oscillation frequency. Likewise in a subharmonic ILO, the incident frequency is a subharmonic of the oscillation frequency. Superharmonic ILOs have found wide application range as frequency dividers, where they proved to be power efficient if compared to the conventional widely used digital dividers [42][43][44]. On the other hand, subharmonic ILOs were mainly used for implementation of MMIC VCOs/synthesizers at millimetric frequencies, where they provide an easy and cheap way of synchronizing high frequency oscillators to lower frequency sources that have high spectral quality. Amongst the applications targeted by such VCOs/synthesizers are automotive control applications, radar applications, and synchronization of optically controlled phased array antennas for satellite communication [54]-[59]. Their use to create a high frequency synthesizer, using a low frequency PLL has been illustrated in [60].

3.4 Subharmonic Injection Locking

Most of the literature has dealt with applications using a locking signal at the same frequency “*Fundamental Locking*”, or at a higher frequency “*Harmonic Locking*” [61]. It has been illustrated that it is possible to lock oscillators with an injected signal, the frequency of which is a sub-multiple of the free-running oscillating frequency

[62][63][64]. The prospect of using subharmonic locking leads to some important potential applications, in particular the generation of a stable high frequency reference signals [61].

Subharmonic injection locking requires only a fraction of the oscillating frequency for injection. Subharmonic locking phenomenon is caused by nonlinearities in the active device, which create the appropriate harmonic of the input signal. Subharmonic Injection locking has found a vast field of application in laser and MMIC applications [54]-[59].

The major disadvantages of conventional subharmonic injection-locked oscillators are the lack of feedback control of the synchronized output signal and the small locking ranges, especially when using higher order subharmonics as the reference signal. Thus, frequency drifts of the oscillator due to temperature effects can result in loss of synchronization, when small locking ranges exist [54].

Figures of merit, such as the locking range and the FM noise degradation of subharmonically injection-locked oscillators, have a great impact on the frequency stability and the noise behavior of the generated carrier. In designing subharmonic injection-locked oscillators, it is very important to know what locking range and phase noise are required of the oscillator, which subharmonic can achieve this locking range and phase noise, and the effect of injection signal power on the locking range and phase noise. To answer these questions, a concrete mathematical understanding of subharmonic injection locking is important. In the following subsections, the mathematical formulation of the locking bandwidth and the phase noise of Subharmonic ILOs is reviewed. This review is based on the work introduced by Daryoush and *al.* in [65] and [66].

3.4.1 Locking BandWidth for Subharmonically ILOs

Several authors have addressed the mathematical interpretation behind the locking phenomenon of oscillators [65]. A simplified mathematical formulation, describing the mechanism of injection-locking for a small injected signal, has been introduced by Adler in [45], who came up with an important figure of merit of injection locked oscillators, namely the *locking range* or *locking bandwidth*. This figure of merit explains the performance of different types of oscillators, by a common relationship relating the locking gain to the locking range and Q of the oscillator. Based on Adler's formulation, some authors extended the analysis to specific types of injection-locked oscillators.

Daryoush was the first author who, starting from Adler's formula, reached a complete mathematical formulation for Locking Range of Subharmonic injection locked oscillators [65]. In his attempt to do so, Daryoush proposed a nonlinear model for the oscillator under forced oscillations. The model block diagram is shown in Figure 3.4. It consists of a pure nonlinear network $f(e)$ representing the input-output nonlinearity of the active device in the oscillator, and a pure linear feedback network $H(\omega)$, representing the frequency selective network. In the model, v_{inj} is the injected signal, e and u are the input and output of the oscillator respectively, and v_o is the signal from the feedback network. The signal e can be considered the input voltage at the gate of a MOSFET, whereas u can be considered as the output drain current.

Figure 3.4 Model for an Injection-Locked Oscillator

The operation of the oscillator is described by the following equations,

$$e = v_o + v_{inj} = u \cdot H(\omega) + v_{inj} \quad (3.2)$$

and,

$$u = f(e) = f(v_o + v_{inj}) \quad (3.3)$$

A single tuned circuit is assumed to constitute the linear feedback network; the transfer function of such a feedback network can be approximated as [65],

$$H(\omega) = \frac{H_o}{1 + j2Q \frac{\Delta\omega_o}{\omega_o}} \quad (3.4)$$

where H_o represents the net parallel resistance across the tank at the resonant frequency ω_o , Q is the quality factor of the tuned feedback circuit, and $\Delta\omega_o$ is the frequency deviation from the resonating frequency ω_o of the feedback circuit. This provides a steady state solution of the feedback signal of the form,

$$v_o = u_o \cdot H(\omega) = E \cos \omega t \quad (3.5)$$

where E is the maximum amplitude of the input signal to the oscillator (e.g. voltage).

The locking signal is assumed to be small and of the form,

$$e_i = (V/2) \left\{ e^{j(\omega_{inj}t + \varphi)} + e^{-j(\omega_{inj}t + \varphi)} \right\} = V(\cos \omega_{inj}t + \varphi) \quad (3.6)$$

where V and φ are the maximum amplitude and phase of the subharmonic injection signal at a frequency $\omega_{inj} \approx \omega_o/n$ (n is an integer, signifying the order of the subharmonic used).

Based on the above assumptions, Daryoush finally reached the following expression for the locking range $\Delta\omega_n$ of a subharmonically ILO at a subharmonic frequency of $\omega_o \approx n\omega_{inj}$ [65],

$$\Delta\omega_n = [(\omega_o/2Q)(V/E)]H_o \left\{ \begin{array}{l} A_{0,1}E \sin \varphi + \\ + (V/2)A_{1,2}E \cos 2\varphi \\ + (V/2)^2 A_{2,3}E \cos 3\varphi \\ + (V/2)^3 A_{3,4}E \cos 4\varphi \\ + (V/2)^4 A_{4,5}E \cos 5\varphi \\ + \dots \end{array} \right\} \quad (3.7)$$

where the coefficients $A_{m,n}$ are given by [65],

$$A_{m,n}(E) = \frac{1}{2\pi} \int_{-\pi}^{\pi} f^m(E \cos \alpha) \cos(n\alpha) d\alpha \quad (3.8)$$

The first square bracket is identified as Adler's figure of merit for locking range at the fundamental frequency. Equation (3.7) shows that the locking range for subharmonic ILOs depends on the active device nonlinearity, the oscillator output power as well as the injected signal power.

The fundamental locking range can also be expressed as a function of the input and output power as follows [65],

$$2\Delta\omega_A = (\omega_o/Q)(V/E) = (\omega_o/Q)\sqrt{P_i/P_o} \quad (3.9)$$

where P_i and P_o are the injected signal power and the output power of the injection-locked oscillator, respectively.

3.4.2 Phase noise of Subharmonic ILOs

A thorough theoretical and experimental analysis of the noise behavior of Subharmonically ILOs has been presented in [66]. The work reported shows that the minimum FM noise degradation factor of an n^{th} order subharmonically ILO is " n^2 " when the injection power is sufficiently strong.

The output FM Noise-to-Carrier ratio of an n^{th} order subharmonically ILO, at a frequency offset $\Delta\omega_o$ from the carrier, can be expressed as a function of the injection signal FM Noise-to-Carrier ratio $\mathfrak{F}_{inj}(\Delta\omega_o)$ and the main oscillator intrinsic noise P_N by,

$$\begin{aligned}\mathfrak{F}_n(\Delta\omega_o) &= \frac{\Delta\omega_n^2 n^2 \mathfrak{F}_{inj}(\Delta\omega_o) + \left(\frac{\omega_o}{2Qb}\right)^2 \frac{P_N}{P_{out}}}{\Delta\omega_o^2 + \Delta\omega_n^2} = \\ &= \frac{\Delta\omega_n^2 n^2 \mathfrak{F}_{inj}(\Delta\omega_o) + \Delta\Omega^2}{\Delta\omega_o^2 + \Delta\omega_n^2}\end{aligned}\quad (3.10)$$

where P_N is the equivalent intrinsic noise power density at the input of the oscillator, P_{out} is the oscillator output power, and b is the linear feedback network coupling factor. The second term in the numerator is the variance of the free running LO oscillation frequency, ω_o , caused by noise power in 1 Hz bandwidth.

Taking into account the near-carrier noise of a MOSFET-based oscillator, equation (3.9) can be modified to be,

$$\mathfrak{F}_n(\Delta\omega_o) = \frac{\Delta\omega_n^2 n^2 \mathfrak{F}_{inj}(\Delta\omega_o) + \left(1 + \frac{\omega_c}{\Delta\omega_o}\right) \Delta\Omega^2}{\Delta\omega_o^2 + \Delta\omega_n^2} \quad (3.11)$$

where ω_c is the corner frequency for the $1/f$ flicker near carrier noise of the MOSFET device.

To fully understand the effect of injection on the phase noise of subharmonically ILOs, a closer analysis of the close-in phase noise should be considered. For close-in frequencies, i.e. for small offset $\Delta\omega_o$, and provided $\Delta\omega_o \ll \Delta\omega_n$, equation (3.11) can be simplified as,

$$\mathcal{L}_n(\Delta\omega_o) \approx n^2 \mathcal{L}_{inj}(\Delta\omega_o) + \frac{\left(1 + \frac{\omega_c}{\Delta\omega_o}\right)}{\Delta\omega_n^2} \Delta\Omega^2 \quad (3.12)$$

If the locking bandwidth is small, the second term of the phase noise expression describing the contribution of the free running oscillator noise to the phase noise expression is dominant. In this case, the phase noise is related to the locking bandwidth in an inverse square manner. Thus, as the injection power increases, the locking bandwidth, correspondingly, increases which decreases the phase noise in an approx. inverse square manner. This suggests that, at a constant injection subharmonic and a constant frequency offset from the carrier, a larger locking bandwidth $\Delta\omega_n$, or alternatively a higher injection power, enhances the phase noise of the subharmonically locked oscillator. As the locking bandwidth increases, the first term starts to overtake the contribution of the second term and the inverse square relation is no longer dominant. The phase noise still decreases but with a much smaller slope. When the locking bandwidth becomes large enough, the phase noise can be approximated by,

$$\mathcal{L}_n(\Delta\omega_o) \approx n^2 \mathcal{L}_{inj}(\Delta\omega_o) \quad (3.13)$$

In this case, the term defining the jitter of the free running oscillator can be neglected, and the phase noise of the locked oscillator is merely the phase noise of the injection signal degraded by the square of the order of the subharmonic. Thus, the phase noise approaches a lower limit equal to the phase noise of the injection signal degraded by a factor of n^2 .

3.5 Conclusion

Injection locked oscillators (sometimes referred to as *synchronous* oscillators) are merely free running oscillators that lock in phase and frequency to an externally applied reference injected signal. The reference signal can be a subharmonic, a superharmonic or the same frequency as the free running oscillator fundamental frequency; this gives rise to the three distinct types of injection, namely subharmonic, superharmonic and fundamental, respectively. Once locked, ILOs follow closely the reference within their locking bandwidth, where they behave much like a first-order PLL. The usage of ILO in frequency synthesis, as opposed to conventional PLLs, is mainly driven by the fact that they have simple structures and dissipate less power. The choice between the different types of injection depends on the application at hand and the feasibility of creation of the reference needed for injection.

Chapter 4. *Q-enhanced Active LC Filters*

4.1 Introduction

RF and IF filtering has always been a hurdle towards integration of the whole transceiver. Despite increasing levels of integration in modern radio transceivers, they still generally rely on discrete LC, ceramic, and electro-acoustic devices “SAW filters” for realization of RF and IF bandpass filtering. Considerable research has been directed at developing suitable replacements for these filters using switched-capacitor and Gm-C based filters, yet the reported designs up to date suffered from lower frequencies of operation or poor dynamic range, respectively [67][68][69].

The advent of Q-enhanced filters has shown more promise to the possibility of the integration of the IF and RF bandpass filters into the transceiver chip. They proved superior to their Gm-C counterparts both for the dynamic range achieved and the power consumption. A critical problem faced by reported Q-enhanced active filter implementations is found to be the power consumption required to achieve narrow fractional bandwidths and an acceptable dynamic range. A key contributor to the power consumption in Q-enhanced filters is the complex, usually master-slave architecture, tuning control circuits required to tune both the frequency and the Q of the filters. This increased power consumption made their use inconvenient for portable wireless transceiver designs. In addition, there were difficulties in extending these filter designs to higher frequencies due to the poor Q of on-chip inductors [67].

In the following sections, a description of Q-enhanced filters' architecture is presented. Then a brief overview of Q-enhanced filters' design is introduced. A study of the noise sources in Q-enhanced filters together with the different reported dynamic range expressions is introduced. The use of Q-enhanced filters as a free-running oscillator is explored.

4.2 Basic Structure of a Q-enhanced LC filter

Although the Q of on-chip inductors employed is typically small ($Q < 10$), negative resistance circuits can be used to increase the effective Q to arbitrarily high values. Hence, very small fractional bandwidths ($< 2\%$) can be obtained. Moreover, even a small inductor Q is shown to provide significant increases in dynamic range over that achievable in fully active filter designs.

A basic Q-enhanced filter design is illustrated in Figure 4.1. This structure is based on a simplified second order topology using parallel mode realization, where R_p represents the approximate equivalent parallel loss resistance of the on-chip finite-Q inductor and accompanying circuitry at resonance. Transconductance g_{mn} indicates the negative resistance designed for offsetting the circuit losses. Transconductances g_i and g_o provide input and output buffering and together with the Q-enhancement transconductor complete the second order filter structure.

Figure 4.1 Simplified Q-enhanced Filter Circuit Diagram

The transfer function for such a filter can be shown to be [72],

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{\frac{g_i}{C}s}{s^2 + \frac{g_p - g_{mn}}{C}s + \frac{1}{LC}} \quad (4.1)$$

Equation (4.1) can be put in the form of the well-known 2nd order function as follows,

$$H(s) = \frac{\left(\omega_0 \cdot g_i \sqrt{\frac{L}{C}} \right) s}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \quad (4.2)$$

where Q is the enhanced quality factor of the filter and is thus given by [67],

$$Q = \frac{\omega_0 C}{g_p - g_{mn}} = \frac{1}{g_p - g_{mn}} \times \frac{1}{\omega_0 L} = \frac{1}{1 - g_{mn} R_p} \cdot Q_o \quad (4.3)$$

where Q_o is the initial Q of the resonant circuit (without enhancement and typically inductor limited i.e. $Q_o \approx R_p / \omega_o L = 1 / g_p \omega_o L$) and ω_o is the filter center frequency given by,

$$\omega_o = \frac{1}{\sqrt{LC}} \quad (4.4)$$

This means that the filter has a midband gain of,

$$A_m(\omega_0) = \frac{\left(\omega_0 \cdot g_i \sqrt{\frac{L}{C}} \right)}{\frac{\omega_0}{Q}} = g_i Q \sqrt{\frac{L}{C}} = g_i Q \omega_o L \quad (4.5)$$

It is clear from equation (4.3) that through suitable setting of the enhancement transconductance g_{mn} , the filter enhanced- Q can be theoretically very large. Furthermore, setting g_{mn} equal to g_p can convert the filter into an oscillator.

4.3 Noise in Q -enhanced filters

Noise is an important issue in the design of active filters, especially if the filter is to be used in the front end of a transceiver. There are several sources of noise in Q -

enhanced filters. Referring to Figure 4.1, sources of noise in Q-enhanced filters may be summarized in the noise contributed by the input transconductance g_i , the enhancement transconductor g_{mn} , and the lossy inductor thermal noise.

For a differential transconductance, the differential output noise current density may be approximated by [73],

$$i_n^2 = 4kTFg_m \quad (4.6)$$

where g_m is the transconductance value and F is a factor, ranging between 1 and 2, that accounts for the actual implementation of the transconductance.

For a resistance of value " R_p ", the noise current spectral density is given by [53],

$$i_n^2 = 4kT \frac{1}{R_p} \quad (4.7)$$

Thus, the total noise current entering the tank circuit is given by,

$$i_{nt}^2 = 4kT(F_i g_i + F g_{mn} + 1/R_p) \quad (4.8)$$

For high Q operation, the value of g_{mn} is set almost equal to the losses in the tank (g_p) i.e.,

$$g_{mn} \approx g_p \quad (4.9)$$

This means equation (4.8) can be approximated by,

$$i_{nt}^2 = 4kT(F_i g_i + (F + 1)g_{mn}) \quad (4.10)$$

The gain of the filter at the center frequency is equal to the quality factor of the filter. Thus the above expression for the noise current at frequency f_o should be multiplied by the quality factor, yielding,

$$i_{nt}^2(f_o) = 4kT(F_i g_i + (F + 1)g_{mn})Q^2 \quad (4.11)$$

Thus the output noise voltage power spectral density at the tank can be obtained by multiplying this total noise current by the square of the amplitude of the capacitor's impedance,

$$\begin{aligned} v_n^2(f_0) &= i_{nt}^2(f_0) \times \left(\frac{1}{\omega_0 C} \right)^2 = \\ &= 4kT(F_i g_i + (F + 1)g_{mn})Q^2 \left(\frac{1}{\omega_0 C} \right)^2 \end{aligned} \quad (4.12)$$

Examining the expression for the noise in equation (4.12) reveals that both the input transconductance and the enhancement transconductance contribute to the overall filter noise floor. Since the input transconductance is usually chosen much smaller than the enhancement transconductance, it is the enhancement transconductance, which usually dominates the filter noise floor. This is true as long as no gain is required out of the filter. If the filter is required to provide some gain, the condition that $g_i < g_{mn}$ does not hold anymore since the input transconductance has to be increased to provide the required gain. Thus the contribution of the input transconductance to the filter noise floor cannot be ignored. In fact at one point, if a large gain is required of the filter, the input transconductance noise can dominate the noise floor of the filter. To clarify this, a numerical example follows which explains the above argument.

Assume we have a Q-enhanced filter with an on-chip inductor of 6.5 nH and a Q_o of 6 at the filter center frequency of 2.4 GHz. Thus, the losses in the filter is approx. given by,

$$g_{mn} \approx g_p = \frac{1}{R_p} = \frac{1}{Q_o \omega_o L} = \frac{1}{6 \times 2\pi \times 2.4 \times 6.5} \approx 1.7 \text{ mSiemens} \quad (4.13)$$

If the filter is to operate at a Q of 120, then using equation (4.5), the filter midband gain is given by,

$$A(\omega_0) = g_i \cdot Q\omega_0 L \approx g_i \cdot 11.8k\Omega \quad (4.14)$$

If the filter midband gain is set to unity, then the required value for g_i will be approx. 0.085 mSiemens, which can be neglected when compared to the value of g_{mn} for any filter noise calculations.

Alternatively, if it is required of the filter to provide a midband gain of 80 V/V (~ 38 dB), then the required value for g_i will be approx. 6.8 mS. This means that g_i in this case is approx. 4 times as large as g_{mn} , and consequently the input transconductance is the dominant noise source for the filter.

4.4 Dynamic range of Q-enhanced filters

Dynamic range is a very important factor in quantifying the performance of a bandpass filter. If a filter is to be used in the front end, then the dynamic range is an even more crucial design measure in the filter design. Using a Q-enhanced filter as an RF filter directly at the input of a receiver mandates that this filter should achieve large enough dynamic range for the specific standard specifications and the anticipated interferers. In this section, a compact study of the dynamic range of Q-enhanced filters is introduced.

In general, the dynamic range of an active filter can be defined as,

$$DR = \frac{P_{\max}}{P_{\min}} \quad (4.15)$$

where $P_{\max}$ is the maximum allowable signal power and $P_{\min}$ is the minimum allowable signal power or simply the filter noise floor. Taking into account that $P_{\max}$ and $P_{\min}$

should be taken at the same circuit node, an analogous expression for the dynamic range, in terms of voltage, is given by,

$$DR = \frac{V_{\max}^2}{V_{\text{noise}}^2} \quad (4.16)$$

where $V_{\max}$ is the maximum allowable signal voltage and V_{noise} is total noise voltage within the specified bandwidth. Since $V_{\max}$ is a function of the circuit topology, biasing conditions and power consumption, the dynamic range is mainly determined by the noise introduced by the circuit.

Starting with equation (4.16), the dynamic range for Q-enhanced filters has conventionally been expressed by the following expression [67][74],

$$DR = \frac{V_{\max}^2 C}{kT(F+1)} \cdot \frac{Q_0}{Q} \quad (4.17)$$

Although the above expression has been extensively used, it ignores the dependence of the maximum output voltage on the filter enhanced Q. A more accurate expression has been reached in [75], and is given by,

$$DR = \frac{4C^2(x-1)}{K_N^2 LkT(F+1)Q^2} \quad (4.18)$$

where x is a factor that defines the filter output compression, and ranges between 1 and 1.122. If a 1 dB compression is assumed (i.e. $x = 1.122$), equation (4.18) can be written as,

$$DR = \frac{0.488C^2}{K_N^2 LkT(F+1)Q^2} \quad (4.19)$$

The above expression shows the importance of the linearity of the enhancement transconductor on the overall dynamic range. The dependence on Q can be reduced if the dependence of g_{mn} versus the maximum tank voltage is reduced.

4.5 Tuning of Q -enhanced filters

Continuous time filters suffer from poor absolute accuracy in the filter time constants, due to the tolerances in the component values building up the filter. This mandates that some sort of tuning of the filter frequency response be applied to ensure correct filter operation. Filter tuning can be done either manually or automatically. In a manual tuning scheme, the filter performance is continuously measured and the filter components are adjusted until the filter operates as desired. Drawbacks of manual tuning include the addition of an expensive step to the manufacturing process, making the filter less flexible, and preventing the filter from accommodating circuit changes that may occur during operation, such as temperature changes [78].

On the other hand, in an automatic tuning scheme, circuitry is designed that is able to measure the filter performance and adjust it to specifications when the chip is operating. This is traditionally accomplished using analog circuitry that “locks” the filter into place [78]. This type of loop locking is very similar to that of a PLL. Figure 4.2 shows typical block diagrams of automatic Q and frequency tuning. In both cases a master filter or VCO is used to perform the tuning measurement and the resulting control signal is used to tune the slave filter.

The frequency and Q tuning of Q -enhanced filters has conventionally been implemented with some variant of the so-called master-slave approach [77], like that shown in Figure 4.2. A master circuit identical to the actual filter of interest (slave) is

placed in a feedback loop and is forced to track an external reference (typically a crystal clock). The resulting tuning signal is used to tune both the master and the slave. The drawback of the master-slave architecture is that extra circuitry is needed to implement a filter and during operation of the tuning circuitry, the power consumption is increased. In addition, the accuracy of the tuning depends on the matching between the master and slave filters. For a high Q LC filter, matching tolerances make it difficult to implement the master-slave architecture. For example, at a Q of 500 and a center frequency of 500 MHz, the maximum frequency deviation between master and slave has to be on the order of 0.1 % (less than half the filter bandwidth). This would require the inductor and capacitor matching to vary by no more than 0.2 %, which is difficult to achieve.

Figure 4.2 Master-Slave Implementation of Automatic Tuning

Another option for tuning of a filter is to use direct tuning. This involves measuring the filter parameters directly from the slave filter without the use of an extra master filter. Figure 4.3 shows an example of a direct tuning scheme. Direct tuning

requires a switch at the input of the filter to switch the input signal off during tuning. Registers or lock-in amplifiers hold the tuned control voltages during the operation of the filter. The drawback of this type of implementation is that a tuning cycle is required, in which the filter cannot be used. For many applications, this is a feasible solution [77].

Figure 4.3 Example of Direct Tuning Scheme

4.6 Q-enhanced filter as a free-running oscillator

As mentioned in section 4.3, if the amount of enhancement or positive feedback is large, the filter can operate as an oscillator. The Q-enhanced filter shown in Figure 4.1 will turn into an oscillator if g_{mn} (negative transconductance designed for offsetting the inductor losses) is set equal to g_p (transconductance representing the losses in the circuit and mainly inductor-dependent). In other words, if the noise contributed by the enhancement transconductance is increased to the extent that it dominates the filter circuit noise, the filter is converted into an oscillator. The oscillation frequency is mainly specified by the value of the inductance and the varactor capacitance. The use of a Q-enhanced filter as a free running oscillator has been explored earlier [76], where a Q-

enhanced filter has been used as a local oscillator (master oscillator) used for tuning the frequency of the main filter.

To use a Q-enhanced filter as a local oscillator, it must have sufficiently low phase noise. A detailed study of the phase noise performance of Q-enhanced oscillators has been previously presented in [76], where the following expression has been reached for the phase noise of a Q-enhanced oscillator relative to the oscillator output power,

$$\frac{N_{op}(\Delta f)}{P_{osc}} = \frac{KT(F+1)}{2P_{osc}} \frac{1}{Q_0^2} \left(\frac{f_o}{\Delta f_o} \right)^2 \quad (4.20)$$

where P_{osc} is the oscillator 1-dB compression output power, f_o is the oscillator center frequency, and Δf_o is the offset from the oscillator center frequency at which the phase noise is measured.

4.7 Conclusion

With the growing momentum for full-integration of transceivers, the need to get rid of expensive and bulky off-chip components is more demanding. A hurdle that always prevented inductor integration in standard silicon technologies is their limited achievable quality factors. Enhancing the on-chip inductors' quality factor by active means has resulted in GHz-range filters with dynamic range adequate for certain applications. Q-enhanced filters are now a valid alternative that allows on-chip integration of IF/RF filters. Though research is still continuing for better dynamic range & more power efficient Q-enhanced filters' realizations, they proved to have better dynamic range and power consumption when compared to their Gm-C counterparts.

Chapter 5. Proposed Transmit Chain Circuit Implementation

5.1 Introduction

In this chapter, a proposed structure for a simple, low-power, compact transmitter intended for Low-Power LP-WLANs' applications, where the design specifications are more relaxed [79], is introduced. The key advantages of the proposed structure are explained. Then, a detailed description of the building blocks is presented. The circuits are presented in chronological order.

The backbone of the proposed structure is the use of a subharmonic injection-locked-based frequency synthesizer structure. A thorough theoretical analysis for subharmonic injection locking technique within the synthesizer structure is presented. Some important results are reached. Mathematical formulas that describe the injection locking range are derived. A comparison between the theoretical results and practical results are presented. Then, the circuit designs and necessary simulations for the voltage-controlled oscillator "VCO", and the PA are detailed. The obtained measurements, where applicable, are presented.

In an attempt to validate the proposed structures, two chips are designed and implemented using standard 0.18 μ m CMOS process. The first chip has Q-enhanced filters (to be used as oscillators in transmission) at various frequencies covering the

different frequency ranges used in the ISM band for LP-WLANs' applications, namely the 915 MHz, the 2.4GHz, and furthermore the 5 GHz. In addition, a single-ended power amplifier is included. The second chip, on the other hand, has the complete transceiver circuits together with the necessary SPI digital control circuitry used for biasing and control. The chips' layouts are included in appendix "A".

5.2 Proposed Transmitter Structure

5.2.1 General Description

The complete transceiver is based on the use of Q-enhanced techniques. The receiver uses a digital IF architecture [80], while the proposed transmitter uses a direct conversion architecture, with a Synchronous Oscillator SO-based synthesizer similar to that introduced in [60], [82]. Figure 5.1 shows the overall transceiver system architecture, with the implemented transmit chain portion highlighted. The clock PLL shown in Figure 5.1(b) and used for injection is not implemented since the design and implementation of the whole synthesizer structure was beyond the scope of this research.

(b) Transmit Chain

Figure 5.1 Proposed CMOS Transceiver Architecture

The top part of the figure shows the receive chain which consists of an input RF switch (1), an LNA (2), a Q-enhanced band select filter (3), an attenuator (4), a transconductor (5), a Q-enhanced channel select filter (6), an RF amplifier (7) and a sub-sampling mixer (8).

The lower block diagram shows the transmit chain which consists of an injection lock amplifier (9), an injection lock VCO (10), an up-converting mixer (11), a preamp (12) and a PA (13). For transmit, the Q-enhanced band select filter (3) is converted to the injection lock VCO (10) by increasing its bias current. Also note that the tank circuit of the Q-enhanced channel select filter (6) is used for the tank of the mixer (11) in the transmit chain. All parts of the transceiver are controlled by 8 or 16-bit control DACs (14) that can be used to digitally control the frequency and Q of the injection-locked VCO and transmit chain tuned mixer. A TX DAC (15) is used to convert data from the baseband processor.

5.2.2 Reuse of Circuitry

As shown in Figure 5.1(a), the receiver chain uses a fourth order Q-enhanced filter in the form of two cascaded 2nd order filters, as RF band select and channel select filters. The channel selection is done in RF prior to subsampling of the signal to produce the digital IF used both for demodulation of the signal as well as direct digital control of the filters' Q and frequency [80]. Since most of transceivers operate in a semi-duplex communication topology, i.e. reception and transmission are usually offset in time, the idea of reusing some of the receiver circuitry for the transmit side is attractive for reduced silicon area and power consumption. A Q-enhanced filter can easily be converted into an oscillator as explained in chapter 4, by increasing the amount of enhancement, (see equation (4.3)). Thus, instead of building a separate LO for the transmit chain, the band select filter of the receive chain is converted into an oscillator and acts as the LO for the transmit chain, Figure 5.1 (b).

Two main issues occur with this architecture. First, since a direct conversion architecture is to be used for the transmitter with the PA included on the same transceiver chip, LO pulling by the PA output may occur (as discussed in section 2.2). A second issue is the phase noise requirement of the transmitter that must be kept to a minimum so as not to degrade reception of nearby receivers. Although the simulated and measured phase noise of a free-running Q-enhanced oscillator can be low, it is generally inadequate for most of the communication standards.

To address the above-mentioned issues, a subharmonic injection locking approach is explored to injection lock the LO. It is a simple, low power solution that requires minimal additional circuitry.

5.2.3 Frequency Synthesizer

Locking of the VCO to its frequency is usually done through the use of a power hungry RF PLL [60]. Another easy and inexpensive method, which can use an existing clock PLL, is to injection lock the LO. In chapter three, the concept of injection locking of oscillators has been introduced with its different types, fundamental, subharmonic and superharmonic. The problem is which type to use and how to generate the locking signal in each case. For both the fundamental and superharmonic injection locking types, a signal at the same frequency or at a higher order harmonic, respectively, has to be generated for the injection process. This does not simplify the proposed structure, and requires a high power RF PLL for creation of the injection signal. Alternatively, in the subharmonic injection type, harmonics of a much lower reference signal can be used for injection. Since the transceiver usually has a low-frequency PLL for generation of baseband clock signals, this same PLL can be used for injection locking the LO using one of its harmonics. A clock PLL usually runs at a much lower frequency than the transmit frequency. This necessitates that a higher order harmonic of the clock frequency be used for injection locking.

Subharmonic injection locking has been discussed in detail in the chapter three. Amongst the shortcomings of subharmonic injection locking are the limited LBW and the degraded phase noise as higher order harmonics are used for injection.

The limited LBW can be accommodated easily in the proposed scheme. The proposed scheme does not require a large LBW. One of the main attributes of the designed Q-enhanced filters is that their center frequencies are digitally tunable within 20% of their center frequency. Implemented digitally controlled switched capacitor

banks, presented later on, can change the filter center frequency with a fine resolution of 300 KHz. So instead of applying the conventional subharmonic injection locking scheme and depending on the LBW achieved using a specific subharmonic, the LO center frequency is brought to within 300 KHz of the injection signal which guarantees locking even with relatively small injection locking power.

On the other hand, the degradation in the phase noise of a subharmonic injection-locked oscillator is at least n^2 , where n is the order of the subharmonic used, as discussed in chapter three. Using the tenth harmonic, for example, means a phase noise degradation of at least $10\log(10^2)=20$ dB. Putting into consideration that the locking signal is crystal based, with a phase noise usually in the order of better than -130dBc/Hz @100 KHz offset, a degradation of 20 dB will still produce a very reasonable phase noise for many of the existing standards.

Based on the above discussion, the synthesizer structure, intended to be used within the proposed transmit chain, should resemble the synchronous oscillator SO-based double-loop synthesizer presented in [60][82], and shown in Figure 5.2. The main difference is that the synchronization circuit used in [60][82], shown in Figure 5.2(b), to create a current pulse waveform at the desired frequency, is no more needed in our proposed structure. Instead, the output of the low-frequency PLL is directly injected into the oscillator input through an injection tuned amplifier, which serves as an amplifier to the needed injection subharmonic, as well as an isolation between the PLL output and the LO input.

Figure 5.2 SO-based Double-loop Frequency synthesizer used in [60][82]

5.2.4 Power Amplifier

To increase the versatility of our proposed structure and to accommodate any existing communications standard, whether using constant or variable envelope modulation schemes, a linear differential amplifier is used in our model. The amplifier is basically a 2-stage fully differential amplifier, consisting of a PREAMP and a PA, with its output power controlled digitally. The exact design and simulation results will be presented section 5.6.

5.2.5 Transmitter Integration

Since the aim is for a low-power transmit chain configuration that may compare well to the existing transmit architectures, the low power clock PLL should be integrated within the transmit structure. It is necessary to have a low-jitter clock PLL that will

translate directly to a low-phase noise injection source. Phase noise has been described in chapter three for a free running oscillator. On the other hand, jitter is an equivalent noise measure for clock generators that digital designers' prefer to use [48].

To quantify this, an estimate for the overall transmitter power consumption should be done. One of the main blocks in the proposed transmitter architecture is the clock PLL used for injection locking the local oscillator. Though this may mean more area and power, some practical examples are necessary to back our reasoning. In [51], a fully integrated low power clock PLL implemented in $0.35\mu\text{m}$ CMOS is presented. The PLL area is 0.21mm^2 while its power consumption does not exceed 1.5mW @ 1.35V bias voltage. Another example is presented in [83]. Implemented in $0.18\mu\text{m}$ CMOS, the clock PLL presented, consumes 2mW of power @ a supply voltage of 1.5V while occupying an area of 0.216mm^2 .

5.3 Mathematical Analysis of Subharmonic Injection Locking

Previous work dedicated to the analysis of subharmonic injection locking of oscillators has always assumed a sinusoidal injection signal [61][63][64][65]. Researchers have always argued that it is mainly the nonlinearity of the oscillator active core, which is responsible for creation of the needed subharmonic used for injection. In addition, the amount of nonlinearity of the active core has been limited to a third order, and in some cases to a fifth order, due to the complexity of the analysis required [65].

Another interpretation for the mechanism of subharmonic injection (synchronization) assumes that this type of injection occurs mainly due to the injected signal harmonics. In other words, this interpretation assumes that the waveform used for

injection locking of an oscillator should be a periodic pulse whose period is “ n ” times the oscillation period of the free running oscillator [84].

Based on the latter interpretation, the analysis that follows uses a periodic pulse signal with 50% duty cycle (i.e. square wave) as an injection signal. The Cartesian Fourier series expansion of the periodic square waveform, shown in Figure 5.3, can be expressed as [85],

$$\begin{aligned} v_{inj} &= \sum_{n=0}^{\infty} a_n \cos n\omega_{inj}t + \sum_{n=1}^{\infty} b_n \sin n\omega_{inj}t \\ &= \frac{V_s}{2} + \sum_{n=odd} \frac{2V_s}{\pi n} \sin n\omega_{inj}t \\ &= \frac{V_s}{2} + \sum_{n=odd} \frac{2V_s}{\pi n} \cos(n\omega_{inj}t - \frac{\pi}{2n}) \end{aligned} \quad (5.1)$$

Figure 5.3 Periodic Pulse (Square) Waveform

As seen from equation (5.1), all even harmonics have disappeared due to the odd symmetry of the periodic square wave. On the other hand, odd harmonics decay in amplitude compared to the fundamental amplitude ($2V_s/\pi$) with the inverse ratio of their order, i.e. $1/n$.

The power spectral density “PSD” of the periodic square waveform shown in Figure 5.3, can be expressed by [85],

$$PSD = \sum_{n=-\infty}^{\infty} \left(\frac{V_s}{2} \right)^2 \left(\frac{\sin(n\pi/2)}{n\pi/2} \right)^2 \cdot \delta(f - nf_{inj}) \quad (5.2)$$

where $\delta(f - nf_{inj})$ are Dirac delta functions at odd multiples “ n ” of f_{inj} .

The graphical representation of equation (5.2) is illustrated in Figure 5.4. As shown in the figure, the PSD of such a waveform consists of a dc value, the fundamental and its odd harmonics weighted by the inverse square of their order, relative to the fundamental.

Figure 5.4 Power Spectral Density for Square Waveform shown in Figure 5.3

For a zero DC level signal, equation (5.1) can be simplified to,

$$v_{inj} = \sum_{n=odd} \frac{2V_s}{\pi n} \cos(n\omega_{inj}t + \varphi_n), \text{ where } \varphi_n = -\frac{\pi}{2n} \quad (5.3)$$

Therefore, in principle, a free-running oscillator can be synchronized or locked to any odd harmonic in the injected pulse spectrum, provided that it has the right frequency and sufficient power. This type of injection, using a harmonic of a square wave, is very well suited to differential oscillators where even harmonics are attenuated owing to the common mode rejection nature of these circuits.

The system block diagram for the intended ILO is illustrated in Figure 5.5. The free running oscillator is resonating at a frequency f_o . When the input of the oscillator is perturbed by the injection signal, the overall input voltage to the nonlinear core of the oscillator is the sum of the output voltage of the oscillator and the injection signal voltage. Denoting this summation by an error voltage “ e ”, it can be expressed as,

$$e = v_i = v_o + v_{injn} \quad (5.4)$$

where v_o is the oscillator output or the input voltage to the nonlinear oscillator core with no injection signal, and v_{injn} is the voltage of the n^{th} harmonic of the injection square wave. They can be expressed as follows,

$$v_o = V_o \cos \omega_o t = \frac{V_o}{2} \left[e^{j\omega_o t} + e^{-j\omega_o t} \right] \quad (5.5)$$

$$v_{injn} = V_{injn} \cos(n\omega_{inj} t + \varphi_n) = \frac{V_{injn}}{2} \left[e^{j(n\omega_{inj} t + \varphi_n)} + e^{-j(n\omega_{inj} t + \varphi_n)} \right] \quad (5.6)$$

where n represents the order of the input pulse harmonic used for injection and V_{injn} is its amplitude given by,

$$V_{injn} = \frac{2V_s}{\pi n} \quad (5.7)$$

To simplify the analysis, the conjugate terms in equations (5.5) and (5.6) can be dropped. Voltages v_o and v_{injn} can thus be simply expressed as,

$$v_o = \frac{V_o}{2} e^{j\omega_o t} \quad (5.8)$$

$$v_{injn} = \frac{V_{injn}}{2} e^{j(n\omega_{inj} t + \varphi_n)} \quad (5.9)$$

Figure 5.5 Injection-Locked Oscillator System Block Diagram

The resulting error signal “ e ” is then applied to the nonlinear core of the oscillator, represented by the active device. Due to the nonlinearity of the oscillator’s core, some mixing operation takes place between these 2 input voltages. The result of the mixing process can be expressed by the function $u(t)$ as follows [65],

$$u(t) = f(e) = f(v_o + v_{inj}) \quad (5.10)$$

The function $u(t)=f(e)$, describing the mixing process within the nonlinear core of the oscillator, can be defined as the relation between the output current w.r.t. the input voltage. This relation can generally be put in the form of a power series as follows,

$$i = \sum_{n=1}^{\infty} a_n v_i^n = a_1 v_i + a_2 v_i^2 + a_3 v_i^3 + \text{higher order terms} \quad (5.11)$$

Furthermore, owing to the periodicity of its arguments, $f(e)$ is periodic w.r.t. both $\omega_o t$ and $n\omega_{inj}t + \phi_n$. For simplicity, we’ll denote each of $\omega_o t$ and $n\omega_{inj}t + \phi_n$ by β and θ , respectively. For every value of β , we can define a function $h(\theta)$, which is even and periodic. It can thus be represented by its Fourier series expansion as follows,

$$h(\theta) = \sum_{k=0}^{\infty} G_k(\beta) \cos(k\theta) \quad (5.12)$$

The Fourier series coefficients $G_k(\beta)$ are given by,

$$G_o(\beta) = \frac{1}{2\pi} \int_0^{2\pi} f(V_o \cos \beta + V_{inj} \cos \theta) d\theta \quad (5.13)$$

$$G_k(\beta) = \frac{1}{\pi} \int_0^{2\pi} f(V_o \cos \beta + V_{inj} \cos \theta) \cos k\theta d\theta \quad (5.14)$$

But the Fourier coefficient G_k is also even and periodic with period 2π , so it can be analogously represented by its Fourier series as follows,

$$G_k(\beta) = \sum_{m=0}^{\infty} A_{k,m} \cos(m\beta) \quad (5.15)$$

where the coefficients $A_{k,m}$ are defined as,

$$A_{k,0} = \frac{1}{2\pi} \int_0^{2\pi} G_k(\beta) d\beta \quad (5.16)$$

$$A_{k,m} = \frac{1}{\pi} \int_0^{2\pi} G_k(\beta) \cos(m\beta) d\beta \quad (5.17)$$

Substituting equation (5.15) into equation (5.12) and replacing $h(\theta)$ by $f(v_o + v_{inj})$, we get,

$$\begin{aligned} u(t) = f(e) = f(v_o + v_{inj}) &= \sum_{k=0}^{\infty} \sum_{m=0}^{\infty} A_{k,m} \cos(k\theta) \cos(m\beta) \\ &= \sum_{k=0}^{\infty} \sum_{m=0}^{\infty} A_{k,m} \cos(k(n\omega_{inj}t + \varphi_n)) \cos(m\omega_o t) \end{aligned} \quad (5.18)$$

Depending on the amount of the nonlinearity in oscillator core, higher order intermodulation products are generated. The result of the mixing process $u(t)$ is then passed back to the input of the oscillator, through the linear tuned circuit. The tuned resonator circuit is responsible for filtering out all intermodulation components that land away from its resonance frequency ω_o . Only the intermodulation components with frequency ω_o are to be taken into consideration, i.e. terms such that $|kn\omega_{inj} - m\omega_o| = \omega_o$. Since an n^{th} order subharmonic injection is assumed in the analysis, i.e $\omega_o = n\omega_{inj}$,

inertmodulation terms with $m = k \pm 1$ possess a frequency equal to “ n ” times the injected frequency. The terms of $u(t)$ that land at a frequency of ω_o can be expressed by $u_{\omega_o}(t)$ as,

$$u_{\omega_o}(t) = A_{0,1} \cos(\omega_o t) + \frac{1}{2} \sum_{k=1}^{\infty} A_{k,k\pm 1} \cos(\omega_o t + k\varphi_n) \quad (5.19)$$

Equation (5.19) can be rewritten with the cosine terms replaced with their complex exponential representations as follows,

$$u_{\omega_o}(t) = e^{j\omega_o t} \left[\frac{1}{2} A_{0,1} + \frac{1}{4} \sum_{k=1}^{\infty} A_{k,k\pm 1} e^{jk\varphi_n} \right] \quad (5.20)$$

This $u_{\omega_o}(t)$ is passed through the resonator circuit, where it represents the output of the ILO. This output is also fed back to the input. Using harmonic balance of the frequency ω_o at node “X” allows the ILO output voltage to be expressed as,

$$v_o(t) = \frac{V_o}{2} e^{j\omega_o t} = u_{\omega_o}(t) \times \frac{H_o \cdot R_L}{1 + j \left(\frac{2Q\Delta\omega_n}{\omega_o} \right)} \quad (5.21)$$

where $H(\omega) = \frac{H_o}{1 + j \left(\frac{2Q\Delta\omega_n}{\omega_o} \right)}$ is the resonator transfer function

The term “ $\Delta\omega_n$ ” defines the maximum single-sided locking range, at a given injected voltage, when using the n^{th} harmonic of the fundamental injection frequency. R_L is the ILO load resistance.

Substituting for $u_{\omega_o}(t)$ from equation (5.20), the ILO output voltage can be expressed by,

$$\mathbf{V}_o = \left[A_{0,1} + \frac{1}{2} \sum_{k=1}^{\infty} A_{k,k\pm 1} e^{jk\varphi_n} \right] \times \frac{H_o \cdot R_L}{1 + j \left(\frac{2Q\Delta\omega_n}{\omega_o} \right)} \quad (5.22)$$

Equation (5.22) can be factored into real & imaginary parts by multiplying the numerator and denominator of the RHS by the conjugate $[1 - j(2Q\Delta\omega_n / \omega_o)]$. The resulting real and imaginary parts can be expressed by equations (5.23) and (5.25), respectively,

$$V_o = \left[A_{0,1} + \frac{1}{2} \sum_{k=1, k \neq n}^{\infty} A_{k,k\pm 1} + \frac{1}{2} A_{n,n\pm 1} \left(\cos n\varphi_n + \sin n\varphi_n \cdot \left(\frac{2Q\Delta\omega_n}{\omega_o} \right) \right) \right] \times \frac{H_o \cdot R_L}{1 + \left(\frac{2Q\Delta\omega_n}{\omega_o} \right)^2} \quad (5.23)$$

$$0 = \left[A_{0,1} \cdot \left(\frac{-2Q\Delta\omega_n}{\omega_o} \right) + \frac{1}{2} A_{n,n\pm 1} \left(\sin n\varphi_n - \cos n\varphi_n \cdot \left(\frac{2Q\Delta\omega_n}{\omega_o} \right) \right) + \frac{1}{2} \sum_{k=1, k \neq n}^{\infty} A_{k,k\pm 1} \cdot \left(\frac{-2Q\Delta\omega_n}{\omega_o} \right) \right] \times \frac{H_o \cdot R_L}{1 + \left(\frac{2Q\Delta\omega_n}{\omega_o} \right)^2} \quad (5.24)$$

Equation (5.24) can furthermore be rearranged so that it takes the form,

$$0 = \left[\left(A_{0,1} + \frac{1}{2} \sum_{k=1, k \neq n}^{\infty} A_{k,k\pm 1} \right) \cdot \left(\frac{-2Q\Delta\omega_n}{\omega_o} \right) + \frac{1}{2} A_{n,n\pm 1} \left(\sin n\varphi_n - \cos n\varphi_n \cdot \left(\frac{2Q\Delta\omega_n}{\omega_o} \right) \right) \right] \quad (5.25)$$

Equations (5.23) and (5.25) are the basic equations that describe the performance of a subharmonic ILO when it is forced to lock to the n^{th} harmonic of a periodic square

waveform applied to its input. They can be solved simultaneously to obtain the output level of the oscillator V_o and the locking range $\Delta\omega_n$ for any injected voltage V_{inj} and any incident frequency ω_{inj} . Although they are very general, they provide very limited intuition about the nature of the locking.

Using the equation for the imaginary, the n^{th} single-sided LBW, $\Delta\omega_n$, can be solved for by substituting for the value of φ_n from equation (5.3). This implies that at both ends of the locking range $\pm \Delta\omega_n$, the phase difference between the n^{th} harmonic of the injection signal and the free running oscillator should be $\pm \pi/2$. In other words, a phase shift of $\varphi_n = \pm(\pi/2n)$ corresponds to the edges of the locking range for the n^{th} used harmonic. Thus, the *cosine* term, in equation (5.25), is eliminated while the *sine* term is reduced to one. Therefore, equation (5.25) can be rewritten as follows,

$$A_{n,n\pm 1} = \left(2 \cdot A_{0,1} + \sum_{k=1, k \neq n}^{\infty} A_{k,k\pm 1} \right) \cdot \left(\frac{2Q\Delta\omega_n}{\omega_o} \right) \quad (5.26)$$

Thus, the one-sided locking bandwidth using the n^{th} harmonic of a periodic square waveform can be easily expressed by,

$$\Delta\omega_n = \frac{\omega_o}{2Q} \cdot \frac{A_{n,n\pm 1}}{\left(2 \cdot A_{0,1} + \sum_{k=1, k \neq n}^{\infty} A_{k,k\pm 1} \right)} \quad (5.27)$$

where the coefficients $A_{0,1}$, $A_{n,n\pm 1}$ and $A_{k,k\pm 1}$ are defined by equations (5.16) and (5.17); they basically depend on the amount of nonlinearity used to define the nonlinear core of the oscillator.

Due to the complexity of the mathematics involved, formulas describing the locking bandwidth of subharmonic ILOs have always been restricted to lower orders of

injection. Most work reported in the literature is based on weak nonlinearity, with researchers considering only up to third order nonlinearity for the oscillator nonlinear core, to derive a second order subharmonic injection locking bandwidth [61][63][65].

To gain more design insight, higher orders of nonlinearities, are considered in the following subsections, so that the locking bandwidth of a subharmonic ILO using up to the eleventh subharmonic can be calculated. Comparison between theoretical (using derived formulas) and experimental results is then performed for different cases in an attempt to prove the validity of the derived formulas.

5.3.1 Third subharmonic injection “n=3”

In this case, a fourth order nonlinearity is assumed, that is equation (5.11) is reduced to,

$$i = a_1 v_i + a_2 v_i^2 + a_3 v_i^3 + a_4 v_i^4 \quad (5.28)$$

Equations (5.16), and (5.17) together with the trigonometric identities and the algebraic polynomial expansions in appendix “C”, are used to expand higher order terms in equation (5.27). Due to the use of a periodic square waveform, the contribution of the even terms in equation (5.28) is nullified. Based on this, the nonlinearities assumed in the next subsections is only restricted to the same order of injection. The following expression is reached for the third subharmonic single-sided injection locking bandwidth,

$$\Delta\omega_3 = \frac{\omega_o}{2Q} \times \frac{a_3 \left(\frac{V_{inj3}}{2} \right)^3}{a_1 \left(\frac{V_o}{2} \right) + 3a_3 \left[\left(\frac{V_o}{2} \right)^3 + \left(\frac{V_o V_{inj3}^2}{4} \right) \right]} \quad (5.29)$$

where $V_{inj3}=2V_s/3\pi$ is the amplitude of the third pulse harmonic

5.3.2 Fifth subharmonic injection “n=5”

In this case, a fifth order nonlinearity is assumed. The following expression is reached for the fifth subharmonic injection single-sided locking bandwidth,

$$\Delta\omega_5 = \frac{\omega_o}{2Q} \times \frac{a_5 \left(\frac{V_{inj5}}{2} \right)^5}{a_1 \left(\frac{V_o}{2} \right) + 3a_3 \left[\left(\frac{V_o}{2} \right)^3 + \left(\frac{V_o V_{inj5}^2}{4} \right) \right] + 10a_5 \left[\left(\frac{V_o}{2} \right)^5 + 1.5 \left(\frac{V_o^3 V_{inj5}^2}{8} \right) + 15 \left(\frac{V_o V_{inj5}^4}{16} \right) \right]} \quad (5.30)$$

where $V_{inj5}=2V_s/5\pi$ is the amplitude of the fifth pulse harmonic.

5.3.3 Seventh subharmonic injection “n=7”

Based on a seventh order nonlinearity, the following expression is reached for the seventh subharmonic injection single-sided locking bandwidth,

$$\Delta\omega_7 = \frac{\omega_o}{2Q} \times \frac{a_7 \left(\frac{V_{inj}}{2} \right)^7}{\left\{ a_1 \left(\frac{V_o}{2} \right) + 3a_3 \left[\left(\frac{V_o}{2} \right)^3 + \left(\frac{V_o V_{inj}^2}{4} \right) \right] + 10a_5 \left[\left(\frac{V_o}{2} \right)^5 + 1.5 \left(\frac{V_o^3 V_{inj}^2}{8} \right) + 15 \left(\frac{V_o V_{inj}^4}{16} \right) \right] + 35a_7 \left[\left(\frac{V_o}{2} \right)^7 + 3 \left(\frac{V_o^5 V_{inj}^2}{32} \right) + 9 \left(\frac{V_o^3 V_{inj}^4}{64} \right) + \left(\frac{V_o V_{inj}^6}{32} \right) \right] \right\}} \quad (5.31)$$

where $V_{inj7}=2V_s/7\pi$ is the amplitude of the seventh pulse harmonic.

5.3.4 Ninth subharmonic injection “n=9”

Similarly, based on a ninth order nonlinearity, the following expression is reached for the ninth subharmonic injection single-sided locking bandwidth,

$$\Delta\omega_9 = \frac{\omega_o}{2Q} \times \left[a_9 \left(\frac{V_{inj9}}{2} \right)^9 \right]$$

$$\left\{ \begin{aligned} & a_1 \left(\frac{V_o}{2} \right) + 3a_3 \left[\left(\frac{V_o}{2} \right)^3 + \left(\frac{V_o V_{inj9}^2}{4} \right) \right] + 10a_5 \left[\left(\frac{V_o}{2} \right)^5 + 1.5 \left(\frac{V_o^3 V_{inj9}^2}{8} \right) + 15 \left(\frac{V_o V_{inj9}^4}{16} \right) \right] \\ & + 35a_7 \left[\left(\frac{V_o}{2} \right)^7 + 3 \left(\frac{V_o^5 V_{inj9}^2}{32} \right) + 9 \left(\frac{V_o^3 V_{inj9}^4}{64} \right) + \left(\frac{V_o V_{inj9}^6}{32} \right) \right] \\ & + 126a_9 \left[\left(\frac{V_o}{2} \right)^9 + 2.5 \left(\frac{V_o^7 V_{inj9}^2}{64} \right) + 7.5 \left(\frac{V_o^5 V_{inj9}^4}{64} \right) + 2.5 \left(\frac{V_o^3 V_{inj9}^6}{32} \right) + 2.5 \left(\frac{V_o V_{inj9}^8}{256} \right) \right] \end{aligned} \right\} \quad (5.32)$$

where $V_{inj9}=2V_s/9\pi$ is the amplitude of the ninth pulse harmonic.

5.3.5 Eleventh subharmonic injection “n=11”

Finally, based on an eleventh order nonlinearity, the following expression is reached for the eleventh subharmonic injection single-sided locking bandwidth,

$$\Delta\omega_{11} = \frac{\omega_o}{Q} \times$$

$$a_{11} \left(\frac{V_{inj11}}{2} \right)^{11} \left\{ \begin{aligned} & a_1 \left(\frac{V_o}{2} \right) + 3a_3 \left[\left(\frac{V_o}{2} \right)^3 + \left(\frac{V_o V_{inj11}^2}{4} \right) \right] + 10a_5 \left[\left(\frac{V_o}{2} \right)^5 + 1.5 \left(\frac{V_o^3 V_{inj11}^2}{8} \right) + 15 \left(\frac{V_o V_{inj11}^4}{16} \right) \right] \\ & + 35a_7 \left[\left(\frac{V_o}{2} \right)^7 + 3 \left(\frac{V_o^5 V_{inj11}^2}{32} \right) + 9 \left(\frac{V_o^3 V_{inj11}^4}{64} \right) + \left(\frac{V_o V_{inj11}^6}{32} \right) \right] + 126a_9 \left[\left(\frac{V_o}{2} \right)^9 + 2.5 \left(\frac{V_o^7 V_{inj11}^2}{64} \right) + 7.5 \left(\frac{V_o^5 V_{inj11}^4}{64} \right) + 2.5 \left(\frac{V_o^3 V_{inj11}^6}{32} \right) + 2.5 \left(\frac{V_o V_{inj11}^8}{256} \right) \right] \\ & + 462a_{11} \left[\left(\frac{V_o}{2} \right)^{11} + 7.5 \left(\frac{V_o^9 V_{inj11}^2}{512} \right) + 37.5 \left(\frac{V_o^7 V_{inj11}^4}{512} \right) + 12.5 \left(\frac{V_o^5 V_{inj11}^6}{128} \right) + 37.5 \left(\frac{V_o^3 V_{inj11}^8}{1024} \right) + 1.5 \left(\frac{V_o V_{inj11}^{10}}{512} \right) \right] \end{aligned} \right\} \quad (5.33)$$

where $V_{inj11} = 2V_s/11\pi$ is the amplitude of the ninth pulse harmonic.

From the above analysis, and as will be experimentally validated later, it can be concluded that to derive the locking bandwidth of an ILO using the n^{th} harmonic of a lower frequency periodic pulse reference, it's usually sufficient to assume an n^{th} order nonlinearity for the nonlinear core of the oscillator. More terms can still be used for expressing the nonlinearity, but higher order terms are usually of less significance, and they do not serve but to add complexity to the calculations.

5.3.6 Calculation of Oscillator a -parameters

To use the above derived formulas directly, the nonlinear frequency and bias-dependent a -parameters of the nonlinear oscillator have to be extracted. They characterize the nonlinear current-voltage relationship in the gain block of the oscillator. Two methods can be directly used to extract the nonlinear a -parameters of the oscillator. One method is to monitor power levels of the harmonics of the free running oscillation frequency at a specific load, so that the nonlinear current-voltage relation can be identified [65]. Another method, introduced in [86], is based on extracting the a -parameters directly from the simulation, by utilizing a well-established nonlinear model for the transistors. The method applied here, and described hereafter, is similar to that used in [86].

For a certain bias point, a time domain simulation (eg. Transient simulation in ADS) is first run to determine the input gate voltage under oscillation condition, $v_i(\omega_o)$. Once this voltage is determined, the oscillator is used as an amplifier with an input applied to it that generates the same input value obtained from the transient simulation. A frequency domain simulation (eg. Harmonic Balance in ADS) is then run for this amplifier circuit, using the same biasing values used in the time domain simulation, and the current spectrum is monitored at the output. This current spectrum gives the output current at each harmonic frequency of the oscillation frequency. The a -parameters can thus be defined by dividing the harmonic currents by the input gate voltage as follows,

$$a_k = \frac{I_k(k\omega_o)}{v_i^k(\omega_o)} \quad (5.34)$$

where a_k depicts the a -parameter corresponding to the k^{th} harmonic of the oscillator free running frequency.

Figure 5.6 explains the sequence used for the calculation of the a -parameters using the described method.

Figure 5.6 Determination of Oscillator frequency-dependent a -parameters

In the following section, the design of some ILOs is detailed. Different harmonics of an applied periodic square waveform are used to lock the oscillators. Experimental results are compared with those obtained using the formulas derived in this section. Furthermore, effect of injection on the phase noise enhancement of the oscillators is analyzed.

5.4. Injection Lock Amplifier and VCO Design

For the purpose of verifying the subharmonic injection locking theoretical results derived in the previous section, two versions of oscillators are used. The oscillators are implemented on 2 separate designed chips ICFCUMA1 and ICFCUMA2 (refer to appendix “A” for complete layouts of the chips). The oscillator on the first chip had the tank totally implemented on-chip, while the second chip oscillator makes use of off-chip inductors. A test board is designed and implemented for each chip.

5.4.1 Circuit Design

Figure 5.7 illustrates a simplified circuit diagram of the implemented injection-amplifier and VCO [87]. The circuit consists of three basic parts, an input

transconductance or amplifier stage, a tank circuit and a negative resistance or Q-enhancement transconductance. More details of the circuit design are presented later in chapter six.

Figure 5.7 Injection Amplifier and VCO Circuit Diagram

The oscillator on the first chip uses differential MOS transistors in the strong inversion mode for tuning. Several banks of varactors are placed with fuses implemented in metal 6 that connect them to on-chip inductor, to be able to go higher in frequency (see Figure 5.8). Through the cutting of some laser fuses, achievable frequencies of 1.1 GHz and 2.4 GHz are reported.

Figure 5.8 Varactors for first chip VCO Tuning

On the other hand, the second chip oscillator tank circuit makes use of off-chip inductors for better quality factor, less power consumption, and increased testing flexibility. Switched capacitor banks are used in place of the conventional MOS varactors since they provide higher Q, larger tuning range, more precise frequency tuning and better noise rejection operation [80]. The capacitors are vertical capacitors, created using the fringing capacitance between adjacent metal lines. These capacitors are shown to have higher capacitance density and better matching than their parallel plate equivalent. The circuit diagram of the capacitor DAC is shown in Figure 5.9. PMOS transistors are used to switch the bottom plate of the binary weighted capacitor from high impedance to Vdd.

Figure 5.9 Frequency DAC

System simulations have shown that a center frequency offset of 300 kHz has little effect on the overall performance. This minimum step size is achieved by the use of small (approximately 5 fF) capacitors. Although it is desirable to have the capacitors as far from the substrate as possible to minimize parasitic capacitance to the substrate or nwell, metal 4 and 5 are used owing to their smaller minimum design rules.

A guard ring, that is left floating, surrounds the capacitors shown in Figure 5.10. The capacitors are connected in one direction by metal three and in the other by metal

five5. The switch transistors add a parasitic capacitance to the bottom plate of the capacitor of approximately 2.5 fF.

Larger banks of capacitors are used to switch between broad frequency ranges. These capacitors are designed so that there is sufficient overlap between the ranges to account for process mismatch and modeling inaccuracies. The larger unit capacitor uses metal layers 1 through 5 for the inter-digitated fingers and metal 6 for interconnection. This capacitor is approximately 50 fF and is used in banks of 8.

Figure 5.10 Unit Capacitors for fine and coarse Frequency Tuning

On both chips, driver stages are used for testing the outputs of the injection locked oscillators with a 50 ohm load.

5.4.2 Injection Lock VCO Tuning

Tuning of the VCO is achieved using direct digital tuning that does not require an input reference [89]. While most of the tuning components are external for the first chip VCO, this is not the case for the second chip, where a sample and hold circuit as well as a bandpass $\Sigma\Delta$ ADC are included on-chip. Though the description applies to both chips, it is more biased to the second chip case. A more detailed description of the tuning of the first chip VCO is presented in chapter six.

A sub-sampling mixer, a typical sample and hold circuit with an input bandwidth large enough to handle RF signals, is used to sample the RF signal to a much lower digital IF signal. A low-frequency clock PLL is used to generate the sampling frequency and an ADC, similar to that in [90], is used to digitize the signal. A digital baseband circuit that is used for receive signal demodulation is reused to measure the frequency of the VCO. An on-chip microcontroller uses the measured frequency to digitally adjust the free running VCO frequency. The digital control is achieved by turning the tank circuit switched capacitor banks on and off. Using the small unit capacitor size of 5 fF, introduced in the previous subsection, the free running frequency can be adjusted by 300 KHz steps over a 20% tuning range.

Once the VCO has been tuned close enough to the desired injection locking harmonic frequency, the clock PLL frequency is switched to the injection locking fundamental frequency and applied to the injection-lock amplifier. The injection locking fundamental frequency is typically higher than the receive sub-sampling frequency to minimize phase noise (i.e. use a lower harmonic) and reduce transmit spurs by having non-desired harmonics of the clock PLL out of band.

5.4.3 Experimental Results

5.4.3.1 Locking Bandwidth Results (Chip One)

The first tests were performed using the oscillators implemented on the first chip, with on-chip tanks. The test setup is shown in Figure 5.11. Agilent 81134A, 3.35-GHz pulse/pattern generator, as well as HP E2903A 1-GHz data generator system, is used as the injection source. It can produce low jitter (~low phase noise) pulse signals with high accuracy. The output pulse amplitude can be finely controlled between 50mV to 2V peak

to peak, i.e. it can produce an output power that varies between -22 and 10 dBm into a 50 Ω output. For lower values of injection power, HP8495B (70dB/10dB step) and HP8494B (11dB/1dB step) step attenuators are used for coarse and fine attenuation steps, respectively. HP8564E spectrum analyzer, with phase noise module installed, is used to examine the test board output. Keithley 2400 series programmable source meters were used for biasing, frequency and gain control for simplifying the testing procedure.

a. Testsetup

b. First Test Board

Figure 5.11 Testsetup and a Closer Look of the First Test Board

Since the circuits have both differential inputs and output, baluns are used to convert differential to single-ended signals. For the lower frequency boards, Minicircuits TC4-14 balun, with a frequency range that extends between 200-1400 MHz, is used. On the other hand, a Macom ETC1.6-4-2-3 transmission line balun is used for higher frequency boards. Its frequency range extends between 500-2500 MHz. Both baluns have 1:4 impedance transformation ratio with a center-tapped secondary winding. Matching to 50 Ω is achieved using off-chip relatively low-cost components.

Input and output matching of the 1.1 GHz, and the 2.4 GHz VCOs are shown in Figure 5.12 and Figure 5.13, respectively. As can be seen from the figures, input

matching is better than -20 dB, while the output matching is better than -17 dB for both boards.

Figure 5.12 Input and Output Matching of the 1.1 GHz VCO

Figure 5.13 Input and Output Matching of the 2.4 GHz VCO

Figure 5.14 shows the captured spectrum of the 1.1 GHz free running oscillator, as well as the oscillator spectrum after being locked using fundamental injection. With no injection, the free running oscillator had an output of approx. -26 dBm. When fundamental injection is applied with an input signal of -55 dBm injected into the oscillator input through the injection lock amplifier, the output level of the ILO does not

change considerably. As the injection power exceeds -55 dBm, the ILO output power slightly changes as shown in Figure 5.15.

a. Free running Oscillator

b. Fundamental-locked Oscillator

Figure 5.14 Captured Output of Free-running and Fundamental-locked oscillator

Figure 5.15 Change in Oscillator Output level vs. Injection Signal Level

Several subharmonics, up to the eleventh harmonic, are used for injection. For each subharmonic used, the fundamental injection power is varied over a wide range and the corresponding locking range is recorded at each injection level. The achieved locking bandwidth is measured for different levels of injected signals, and will be shown later.

In order to compare the theoretical results, obtained using the derived formulas in section 5.3, with the measured results, we have to calculate the resonator Q as well as the oscillator a -parameters.

First, the measured results for fundamental locking, together with Adler's locking range expression for fundamental injection (equation 5.35), are used to extract the value of the unloaded resonator Q . The extracted value of Q is approx. 22.

$$\Delta\omega_o \approx \frac{\omega_o}{2Q} \times \frac{V_{inj}}{V_o} \quad (5.35)$$

Then the values for frequency/bias dependent transconductance a -parameters of the oscillator circuit, under the used test conditions, are calculated using the scheme outlined in subsection 5.3.6. From the time domain test bench, the input voltage for the oscillator circuit under oscillation condition is found to have an amplitude of approx. 288 μ V. This value is used in the frequency domain test bench, and accordingly the magnitudes for the output current spectrum of the VCO are summarized in Table 5.1. Using the values in Table 5.1, together with the value of the input voltage under oscillation condition, we can substitute in equation (5.34) to arrive at the required oscillator a -parameters at this specific bias point. The obtained values for the a -parameters can be summarized in Table 5.1.

Table 5.1 Magnitudes of VCO Output Current Spectrum

Output Current Spectrum	Magnitude
$I_1(\omega_o)$	$7.730e^{-7}$
$I_3(3\omega_o)$	$2.177e^{-14}$
$I_5(5\omega_o)$	$5.724 e^{-19}$
$I_7(7\omega_o)$	$1.896e^{-19}$
$I_9(9\omega_o)$	$1.121e^{-18}$
$I_{11}(11\omega_o)$	$7.168e^{-19}$

Table 5.2 Oscillator Frequency-dependent a -parameters

a -Parameter	Magnitude
a_1	$2.684e^{-3}$
a_3	$9.113e^{-4}$
a_5	0.2890
a_7	$1.154e^6$
a_9	$8.224e^{13}$
a_{11}	$6.340e^{20}$

Having obtained the values for the resonator Q and the oscillator a -parameters, at the required bias point, substitution in equations (5.29) through (5.33) is straightforward. The theoretical values for the single-sided locking bandwidths, using different subharmonics, as a function of fundamental injection power are calculated. The calculated values are multiplied by a factor of two to obtain the double-sided locking bandwidths.

A comparison between the measured locking bandwidths and the predicted theoretical values is shown in Figure 5.16. Except for a mismatch for the fifth harmonic case originating from some errors in measurements, the close matching between theory and measurement suggest that the assumptions used in deriving equations (5.29) through (5.33) are valid. In other words, when using an odd harmonic of a periodic square waveform to injection lock a free running differential oscillator, it is sufficient to assume an order of nonlinearity for the active core of the oscillator that is the same as the order of the harmonic used for injection. Such an assumption will reduce the complexity of calculations especially when higher harmonics are used. For example, we can safely assume a third order of nonlinearity for an oscillator's active core to predict the locking bandwidth using the third harmonic of a square wave as an injection signal.

Figure 5.16 Comparison of LBW vs. Injection Power for Different Subharmonics

Furthermore, Figure 5.16 reveals some interesting results. Fundamental locking represented by the brown curve, as opposed to subharmonic injection locking, has the widest tuning range. With a signal power as low as -60 dBm of fundamental injection power, a locking bandwidth of 1 MHz can still be achieved.

When harmonics of the fundamental square signal are used for injection, the needed fundamental injection power is higher to achieve the same locking bandwidth. This is because the harmonic often has significantly lower power than the fundamental, as explained in section (5.3), which therefore must have an even larger power for correct locking. As higher harmonics are used, the amount of injection power becomes unreasonably high to achieve limited locking bandwidths. For example, to achieve a locking bandwidth of 10 MHz using the input pulse's ninth harmonic, a fundamental

input power of -10 dBm is required, an impractical figure for on-chip low power operation anticipated of such an injection scheme. Meanwhile, this same locking bandwidth can only be achieved with approx. -28 dBm of fundamental injection power, if the fifth harmonic is used instead.

Therefore, one may jump to the conclusion that using higher harmonics for injection is not power efficient. As higher harmonics may still be required, especially for higher frequency applications, an alternative low power solution has to be presented to allow their use efficiently; if the oscillator free running frequency is guaranteed to be close to the injection harmonic frequency, independent of process and environmental variations, the required LBW can be greatly reduced. As a result, the unreasonable increase in fundamental injection signal power, for higher harmonics, and associated power dissipation can be avoided. This directly suggests the idea of pretuning the free running oscillator to within a small offset from the used harmonic. The concept of pretuning is applied and the improvements in obtained results are presented in a later subsection.

5.4.3.2 Phase Noise Results (Chip One)

To quantify the source used for injection, the phase noise of the pulse generator is measured in two cases; first with a 100 MHz clock output, while the other with a 1 GHz clock signal. In both cases, the source is set at -10 dBm output power, and the phase noise measurement is performed. The obtained measurements are -122.67 dBc/Hz and -106.33 dBc/Hz @ 100-KHz offset from the carrier, respectively. For the lower frequency clock, the actual phase noise of the source should be better than the measured figure, since the value reported is mainly limited by the measuring instrument noise floor. According to

the manufacturer's manual, the noise floor of the HP 8564E spectrum analyzer is approx. -133 dBm, and its amplitude measurement accuracy is ± 2.5 dB when the measured signal is at least 10 dB above its noise floor [91]. A more precise value for the phase noise of a 100 MHz clock signal, generated using the Agilent 81134A pulse generator, would be approx. -130 dBc/Hz @ 100 KHz offset as shown hereafter.

Figure 5.17 Agilent 81134A Pulse Generator Sample Phase Noise Measurement

The phase noise of several different harmonics of the 100 MHz clock signal is measured. A sample of these measurements is shown in Figure 5.18 for the seventh and eleventh harmonics respectively.

According to equation (5.2), the PSD of the odd harmonics of a periodic square wave signal are related to the fundamental by the inverse square of their order. Thus, under the same test conditions, the seventh and eleventh harmonics should have a phase noise which is worse than the fundamental at 100 MHz by $\{10 \log(1/n^2)\}$, or -17dB and -20.8dB, respectively. According to the values obtained from the respective phase noise measurement, the fundamental clock signal should have a phase noise which is equal to

$\{-113+(-17)\}$ or $\{-110+(-20.8)\}$, which is equal to approx. -130 dBc/Hz @ 100 KHz in both cases.

Figure 5.18 Phase Noise Measurements of Harmonics of the 100-MHz Clock Signal

Having defined the injection source, the Agilent 81134A pulse/pattern generator is used to produce various clock signals ranging between 84 to 366 MHz. The appropriate harmonics of these different clock signals are used for injection-locking the free-running oscillator @ 1.1 GHz. In all these tests, the injected amplitude of the clock signal is always fixed at 100 mV peak to peak (~ -16 dBm of injection power), to fairly compare the different cases. The phase noise measurement results are displayed in Figure 5.19.

For example, considering the case of using the eleventh harmonic of a 100 MHz clock source for injection, the measured phase noise of the ILO is approx. -110 dBc/Hz, which is the same as the phase noise of the eleventh harmonic of the 100 MHz clock, shown in Figure 5.18. The phase noise degradation is approx. $10\log(n)^2 = 10\log(121) = -20.8$ dB less than the fundamental, as predicted by equation (3.12) defining the phase noise of a subharmonic ILO. The measured LBW in this case is approx. 2.5 MHz which is quite larger than the offset of 100 KHz, where the phase noise is measured.

Figure 5.19 Phase Noise Measurements using Different Fundamental Frequencies Harmonics

Another important conclusion that can be drawn from the above results, is the fact that using a lower harmonic of a higher frequency reference to lock an oscillator is

equivalent to using the higher harmonic of a lower frequency one. This is clear by comparing the use of the third harmonic of a 366 MHz clock signal to that of the eleventh of a 100 MHz clock signal one. This leaves the designer with the freedom to use whichever clock reference that can easily make use of the existing clock data reference, and abide by the constraints imposed on power consumption within the circuit.

5.4.3.3 Locking Bandwidth Results (Chip Two)

Later tests were carried out using the oscillator on the second chip, the transceiver chip. A sub-sampling frequency of 45-MHz is used for tuning the free running VCO. A frequency of 100 MHz is used for the injection locking fundamental. The VCO is locked to the 11th harmonic of the clock PLL at 1.1 GHz.

In the free-running mode, the VCO is biased using a 1.6V supply with a bias tail current of 270 μ A and has a tuning range from 990 MHz to 1.21 GHz. To injection lock the VCO, a bias current of 160 μ A is applied to the injection-locking amplifier to give an overall bias current of 430 μ A.

Figure 5.20 shows the locking bandwidth as a function of the injected signal power. It can be seen an eleventh harmonic signal power of -53 dBm is sufficient to lock the VCO as long as the free running frequency is within 1 MHz of the injection signal. The free running VCO tuning algorithm is insensitive to process and environment conditions and allows the VCO to be tuned to within 300 KHz of the injection harmonic frequency using a small unit capacitor size switched capacitor, described earlier in subsection (5.4.1). This allows the VCO to be locked with minimal injection harmonic power. Without the tuning algorithm it would typically require more than 20 MHz of LBW and an injection locking harmonic power of more than -25 dBm.

Figure 5.20 Locking Bandwidth vs. Injected Signal Power

5.4.3.4 Phase Noise Results (Chip Two)

Figure 5.21 shows the measured output spectrum of the VCO. As can be seen, the spur due to the 9th harmonic is -54.3 dBc relative to the injection locked 11th harmonic. The 10th harmonic is an even harmonic of the PLL square wave output and is therefore greatly attenuated. It is measured at -68.8 dBc using a smaller resolution bandwidth for the spectrum analyzer. These spurs should be further suppressed when passed through the tuned mixer, PA matching circuit and antenna.

Figure 5.22 shows the phase noise performance of the injection locked VCO before and after injection locking. The free running VCO has a phase noise of -79.7 dBc/Hz at 50 KHz offset. The apparent flattening of the oscillator's close-in phase noise is mainly attributed to the drift in the oscillator signal during measurement and the

inability of the tracking algorithm built in the phase noise measurement module to track it. When injection locked with a 100-MHz PLL signal, the phase noise is improved to -99.8 dBc/Hz at 50 KHz offset. Furthermore, at high frequency offsets, $> 1\text{MHz}$, the two measured phase noise curves converge to the same noise level. In other words, at larger frequency offsets from the carrier, the phase noise of the ILO is dominated by the phase noise of the free running oscillator, a result expected from equation (3.12).

Figure 5.21 1.1GHz Oscillator Spectrum

Figure 5.22 Phase Noise of 1.1GHz VCO before and after Injection Locking

5.4.3.5 Solution to LO Pulling

The effect of “LO pulling” on the 1.1 GHz injection-locked oscillator, presented in the previous subsection, is studied. Figure 5.23 shows the required injection signal power as a function of the transceiver radiated power at different frequency offsets from the locking signal. The radiated power is measured using two calibrated quarter wave “ $\lambda/4$ ” whip antennas with 0 dBi gain.

Figure 5.23 Measured Injected Signal Power vs. Radiated Power
@ Different Frequency Offsets from Locking Signal

The worst case scenario, “Green Curve”, occurs if no pretuning of the VCO is performed and the VCO signal is at 25 MHz offset from the injected signal. It can be seen from the figure, the impractical injected signal level needed to prevent pulling (a typical clock signal of 1.6V p-to-p has an eleventh harmonic as high as approx. -13 dBm into the

LNA). Pretuning the VCO with no radiated power, “*Blue Curve*”, is efficient at low radiated power levels. As the transceiver radiated power increases, more injection power is needed to prevent LO pulling due to the drift in transmit frequency. Pretuning the VCO to within 300 KHz of the injection frequency at each radiated power level, “*Red Curve*”, allows VCO locking with injection power as low as -52 dBm, even when the transceiver is radiating 10 dBm of power.

Measurement results for the VCO performance are summarized in Table 5.3 [87].

Table 5.3 Summary of VCO Performance Results

Technology		Standard 0.18 μ m CMOS
Power Supply		1.2 – 1.8 V
Center Frequency		990 – 1210 MHz
Harmonic Spurs		< -54.34 dBc
Phase Noise (@ 50 kHz offset)	Free running	-79.7 dBc / Hz
	Injection-Locked	-99.8 dBc / Hz
Current	Injection Amp.	270 μ A
	VCO	160 μ A
TOTAL POWER (VDD = 1.6 V)		688 μ W

5.5 The Power Amplifier Design

5.5.1 Circuit Design

A fully differential power amplifier is designed and implemented for the transceiver chip. It consists of two stages, a preamplifier to provide the required signal swing and a driver for driving off-chip 50-ohm load. The power amplifier simplified circuit diagram is shown in Figure 5.24.

The preamplifier is a cascode differential pair loaded by an on-chip resistive load. A resistive load is chosen for this stage so that the PA can be used for the two different

ISM bands, 915 MHz and the 2.4 GHz. In the design of submicron CMOS PAs, oxide breakdown voltage is a key limitation, which limits the available voltage swing at the drain of the transistor. A cascode structure has been adopted for the preamplifier. This prevents oxide breakdown, ensures the PA stability and provides better isolation between the PA output and the mixer output [17].

The driver is a simple differential pair with off-chip load inductors for multiple band operation. The interstage matching is fully integrated. It is in the form of a high pass circuit consisting of an on-chip capacitor and an on-chip inductor (for the higher frequency ISM band). For the lower frequency band, an off-chip inductor is used due to its larger size. Metal six fuses that can be blown up using either Focused Ionized Beam “FIB” or Laser are implemented to be able to disconnect the internal inductor and use an external one instead. The inductor of the interstage matching circuit serves for providing the gate bias for the output driver transistors as well.

Figure 5.24 Power Amplifier Simplified Circuit Diagram

A differential structure is adopted since it allows for more dynamic range in the circuit. The voltage swing requirement at any node is cut in half. Another benefit of a

differential architecture is the immunity to common-mode noise. The driver stage of the PA will often be generating large amounts of AC substrate current, which can cause havoc with a single-ended implementation, due to fluctuations in substrate voltage, or more generally due to large external noise that can drive the circuit to malfunction. However, in differential implementation, that noise, which can be considered as common-mode signals, can be effectively ignored.

The power amplifier circuit is preceded by a direct frequency upconversion mixer “FUM” with Q-enhancement circuitry added to get rid of the channel selection BPF that is normally placed between the mixer and the PA for suppression of unwanted frequencies generated during the upconversion process. The baseband signal is generated on-chip using a DAC and fed into a basic Gilbert cell mixer. Figure 5.25 shows a simplified circuit diagram of the mixer.

Figure 5.25 Frequency Upconversion Mixer Simplified Circuit Diagram

Due to the use of the tank circuit of the second filter in the receive path, as the tank of the mixer in the transmit path, the operation of the mixer was not as expected.

The VCO feedthrough was larger than the desired transmitted signal. Thus, the results obtained were not satisfactory and this prevented testing the whole transmit path while applying different modulation data rates.

5.5.2 Simulation Results

For simulation purposes, ideal transformers (baluns) are used to convert differential to single-ended input/output. While the input is matched to 50Ω , a transformation network at the output is used to transform the 50Ω load to a 24Ω differential load (12Ω single-ended) for maximum output power.

The simulated power gain of the PA, shown in Figure 5.26, is around 26.8 dB. The 1-dB compression point output is approx. 6.5 dBm, and occurs for an input power of -19.5 dBm. Also shown in figure is the output third order intercept point (OIP3), which is approx. 20 dBm. At 1-dB compression, the PA power added efficiency "PAE" is simulated to be approx. 14% as shown in Figure 5.27.

Figure 5.26 The PA Power Gain and 1-dB Compression Point

The adjacent channel power ratio and the transmitted spectrum is tested with a raised cosine pulse-shaped $\pi/4$ DQPSK signal, using the IEEE802.15.4 transmit PSD

mask for the 915 MHz band. The simulated ACPR is simulated to be better than -32dB for both the lower and upper channels. All spurious emissions fall beneath the transmit mask.

Figure 5.27 The PA PAE

Figure 5.28 Simulated Spectrum at the Transmitter Output

The output power of the PA is digitally controlled through the biasing of the 2 stages. The output power can be changed in steps of 2 dB. The designed PA is supposed to work in a class “A” configuration for linear operation to accommodate variable envelope digital modulation schemes. The amplifier dissipates about 17.5 mW, when powered up by a 1.6V supply voltage, with an overall power dissipation of 28 mW.

The transistor sizing for the preamplifier, and the power amplifier are listed in Table 5.4.

Table 5.4 Power Amplifier Transistor Sizing

Transistor	Length [μm]	Width [μm]	No. of Fingers	Total Width [μm]
$M_{1a,b}$	0.22	5	80	400
$M_{2a,b}$	0.22	5	80	400
$M_{3a,b}$	0.22	5	240	1200

Although the power amplifier power consumption was not optimized, the predicted overall power consumption of the transmit path when powered up by a 1.6V power supply is approx. 21 mW. This number is based on implementing a 2mW clock PLL similar to that presented in [83], to complete the frequency synthesizer structure. In the meantime, the architecture does not need any extra circuitry for *LO pulling* immunity. Therefore, the proposed transmitter structure is suitable for compact, low power applications.

The breakdown of the transmitter power consumption is shown in the chart shown in Figure 5.29.

Figure 5.29 Chart showing Proposed Transmit Path Power Consumption

5.6 Transceiver Chip Design

The transceiver test chip is fabricated in 0.18 μm standard CMOS process. The chip is bonded directly to a test board using chip-on-board bonding (see Figure 5.30 for the chip micrograph while mounted on the test board). The receiver Q-enhanced filters are located on the top left corner of the chip with their tanks placed off-chip mainly due to size limitations as well as testing flexibility. The upconverter mixer is in the top middle while the power amplifier is placed in the top right corner. The direct digital tuning circuitry for the Q-enhanced filters/oscillators, including RF amplifiers, a sample and hold circuit and a bandpass $\Sigma\Delta$ ADC, are placed directly below the power amplifier.

On the bottom of the chip is the Serial-to-Parallel interface “SPI”, used to control the various DACs included on-chip and used for biasing all circuits as well as frequency tuning of the Q-enhanced filters/oscillators.

Figure 5.30 Transceiver Chip Micrograph

5.7 Test Circuitry

Individual test boards are designed for testing the Q-enhanced filters/oscillators and the transmit chain. In both boards, a chip-on-board process is used for connecting the die to the test board.

In the chip-on-board process, a suitable PCB footprint is created for the die. The footprint consists of a gold plated copper area slightly larger than the die size and attached to the PCB ground plane, surrounded by a number of pads, connected to tracks, corresponding to the pads on the die. The die is glued on the grounded footprint using a highly conductive silver epoxy and the pads on the die are bonded directly to the printed circuit board (PCB) using Gold 1 mil thickness bondwires.

Bonding the die directly to the board has several key benefits. The lengths of the bondwires are minimized compared to those required if the die were to be placed in a standard package. The bondwire inductance (approx. 1nH/mm), can thus be minimized by moving the landing pads on the PCB as close as possible to the die. Consequently, the

effects of the bondwires on the circuit performance can be minimized. Finally, as mentioned earlier, the die footprint is connected directly to the PCB large, electrically quite ground plane. This serves to create an excellent quite electrical ground plane for the chip which helps in keeping the substrate of the chip as quite as possible. In addition, it creates a good heat sink for the die.

For the transceiver chip, all circuits are digitally controlled. A Matlab code run on a standalone PC is used to control the different DACs on-chip to provide the required DC biasing for all circuits. Through a General Purpose Interface Bus “GPIB” connector, the PC connects to a Field Programmable Gate Array FPGA Interface for Signal Handling “FISH” board. The FISH board controls the test board directly through an interface board that converts the 3.3V to 1.8-2.5V control signals. Figure 5.31 shows the testsetup for the transceiver chip.

Figure 5.31 Test Setup for the Second Transceiver Chip

5.8 Conclusion

In this chapter, a proposed compact low-power transmitter architecture, based on a subharmonic synchronized frequency synthesizer, is presented. To this end, a

mathematical analysis of subharmonic injection locking of oscillators using a periodic square waveform as an injection source is performed. A general formula expressing the locking bandwidth using any of the pulse's signal harmonics and assuming any order of oscillator nonlinearity is reached. Some special cases are considered. Locking bandwidth formulas up to eleventh order subharmonic injection are derived. The derived formulas are validated by comparing theoretical obtained results with measured results obtained from designed circuits, and proved to be accurate to a good extent. Circuit implementations of the proposed transmit structure are presented, together with the simulated & where possible, experimental results. The proposed transmit structure has low power consumption and very good immunity to LO pulling. Thus, it is suitable for low power applications like WLANs/WPANs.

Chapter 6. High Frequency Q-Enhanced Filter Implementation

6.1 Introduction

Q-enhanced filters have shown promise to the possibility of the integration of the IF and RF bandpass filters into the transceiver chip, while providing superior performance compared to their Gm-C counterparts for both the dynamic range achieved and power consumption. A critical problem faced by reported Q-enhanced active filter implementations is found to be the power consumption required to achieve narrow fractional bandwidths and an acceptable dynamic range. This increased power consumption made their use inconvenient for portable wireless transceiver designs. In addition, there were difficulties in extending these filter designs to higher frequencies due to the poor Q of on-chip inductors .

In this chapter, important practical considerations surrounding the implementation of Q-enhanced LC filters in 0.18 μ m silicon CMOS process are investigated, including realizing the necessary on-chip spiral inductors and Q-enhancement circuits, predicting frequency and Q tolerances and temperature stability, and developing real-time direct digital frequency and Q tuning mechanisms. The well-known problem of extensive power consumption in Q-enhanced filters is alleviated through the use of direct tuning method that proved more efficient in terms of power and accuracy [70]. In addition, the

possibility of extending the performance of these filters to higher frequencies is validated with an implemented prototype that is designed for the 5-GHz ISM band of communications.

To validate the feasibility of application of the proposed transceiver architecture - presented in chapter five - to higher frequencies, subharmonic injection locking is experimented on the designed high frequency filter/oscillator. A much lower frequency clock signal is used to lock the high frequency filter/oscillator. The various obtained results are presented.

6.2 Proposed Q-enhanced Filter Architecture

Classic heterodyne receivers require bandpass filters with narrow fractional bandwidths for preselection, image rejection and final channel selection prior to demodulation. The use of Q-enhanced filters in the front-end heterodyne receiver can relax the linearity requirements imposed on subsequent stages. Integrating the LNA with a Q-enhanced tunable filter structure also reduces the requirements of the RF preselection filter. Although the use of an off-chip RF filter is still desirable (to help prevent strong interferers from desensitizing the receiver), the required filters can be less expensive and with lower Q as part of the preselection is accomplished by the Q-enhanced filter structure.

The proposed filter architecture is shown in Figure 6.1. The filter is to be used in a receiver with a sub-sampling mixer/ADC that allows direct digital frequency tuning of the filter and adjustment of the required Q [70]. Since the filter has a narrow bandwidth, subsampling can be readily used without excessive degradation in performance due to noise aliasing.

Figure 6.1 Proposed Q-enhanced System Architecture

The subsampling principle is based on the fact that signal information is embedded in the signal bandwidth not in its frequency. Thus, an RF signal with a bandwidth of " Δf " can be translated to a lower band if sampled at a rate that follows the Nyquist criterion (i.e. $f_s \geq 2 \Delta f$). The use of subsampling (submixing) eliminates the need for an RF mixer and associated RF LO/synthesizer. Nevertheless, a main drawback of subsampling is the aliasing of noise (or noise folding) into the band of interest. Subsampling a signal by a factor of " m ", multiplies the downconverted noise power of the sampling circuit by a factor of " $2m$ " [53]. Though this may appear to be a problem, it is readily alleviated in the proposed architecture, owing to the very narrow bandwidth of the implemented filter (high Q). To understand this, a numerical example is hereby presented. Assume we have a filter centered at 900 MHz with a Q of 450 ($BW = 2$ MHz). Subsampling the output of this filter using a 80 MHz clock signal, i.e. a subsampling ratio of 11, creates folded noise images with the largest of these images at ± 40 MHz, approx. 9.5 octaves away from the filter center frequency. Consequently, these images are attenuated by approx. 57 dB. Thus, the added noise due to subsampling is not significant.

After subsampling, the resulting digitized IF signal can be used for both signal tuning and signal demodulation. The use of IF sub-sampling allows the signal to be mixed down and processed in the digital domain, providing potentially significant power reduction as well as increased flexibility in the receiver.

Based on the above structure, a 5 GHz Q-enhanced filter is designed and implemented in standard CMOS 0.18 μm [70]. This is the first reported CMOS Q-enhanced filter capable of operating in the 5-GHz band with a promising figure for dynamic range that can pave the road for the usage of Q-enhanced filters in the front end receivers operating in this band.

6.3 Circuit Description

Figure 6.2 illustrates a simplified circuit diagram of the complete filter. The filter consists of three basic parts, an input transconductance or gain stage, a fully integrated on-chip tank circuit and a negative resistance or Q-enhancement transconductance.

Figure 6.2 Simplified Circuit Diagram of the High Frequency Filter

The input transconductance uses a standard cascode LNA structure consisting of transistors $M_{1a,b}$ and $M_{2a,b}$. The cascode LNA provides good reverse isolation and gain and is responsible for setting the overall noise figure of the filter.

The tank circuit is totally implemented on-chip. It consists of a circular center tapped spiral inductor and differential varactors. Figure 6.3 shows the tank layout circuitry.

Figure 6.3 Tank Layout

The use of a circular shape center tapped inductor provides better high frequency performance and reduces losses. The inductor is designed using ASITIC. The simulated inductor parameters are summarized in Table 6.1.

Table 6.1 High Frequency Filter Tank Inductor Simulation Values

Radius [μm]	No. of Turns [N]	L [nH]	f_{res} [GHz]	Q_o at f_{res}
150	3	2.9	7.530	8.449

The varactor uses a MOS capacitor in inversion range with a moderate Q, better than that of diode varactors. This type of varactors is easily implemented in a standard mode operation, and provides a wide tuning range [94].

The enhancement transconductor is a basic differential pair that consists of transistors $M_{3a,b}$. This transconductor provides good linearity when using low Q on-chip inductors. The linearity can be further improved by using degeneration at the cost of higher power consumption.

Output drivers, consisting of two source follower stages, provide buffering so that the chip can drive a 50-ohm load. Off-chip baluns are used to convert the differential chip output to single-ended output.

6.4 Simulation Results

A transistor sized 40/1 is used as a varactor. Simulation results, shown in Figure 6.4, show that the transistor capacitance can vary between 85 fF and 550 fF for a tuning voltage range between 0 and 1.6V, respectively. The tank frequency response, as a function of the tuning voltage, is shown in Figure 6.5. The figure shows the tank tuned to different values within its tuning range.

Figure 6.4 Varactor Capacitance vs. Tuning Voltage

Figure 6.5 Resonator Frequency Response vs. Tuning Voltage

The power gain and noise figure of the filter are simulated. To do so, the filter is matched to 50Ω both at the input and output, using ideal components. Ideal baluns are used to convert differential to single-ended signals. The simulation results are shown in Figure 6.6 and Figure 6.7, respectively. For the power gain simulation, the filter Q is set to a value of 100 which corresponds to a bandwidth of approx. 50 MHz at a centre frequency of 5.2 GHz.

Figure 6.6 Filter Power Gain Simulation

The noise figure is simulated at a bias current of 2 mA for the input transconductance. Since this filter is intended to be used in a receiver front end, the achieved noise figure is mainly dependent on the bias current for the input transconductance as explained in chapter three. Varying the bias current and its effect on the obtained noise figure is summarized in Table 6.2.

Figure 6.7 Filter Noise Figure Simulation

Table 6.2 HF Filter Noise Figure versus Input Transconductance Bias Current

Input Bias [mA]	Operating Q	f_o [GHz]	Noise Figure [dB]
2	92	5.21	3.586
1	103	5.22	5.171
0.5	123	5.225	8.8

From the table, it is clear that the noise figure of the filter is decreased by increasing the bias current to the input transconductance stage. The minimum bias current and the corresponding acceptable noise figure is governed by the amount of amplification

needed of the input stage and the permissible noise figure the filter is allowed to present at the input of the receiver.

Post layout simulations, using the extracted circuits, are performed. As shown in Figure 6.8, the simulated post layout tuning curve shows a tuning range of approx. 1 GHz around a carrier frequency of approx. 5.5 GHz which covers the complete IEEE802.11a spectrum, extending between 5.150 GHz and 5.825 GHz.

Figure 6.8 Post Layout Simulation Results for Tuning Range of the HF Filter

6.5 Filter Tuning

Tuning of the filter is accomplished in the digital domain after mixing to an IF frequency and sub-sampling with an ADC. This is a form of direct tuning as the filter itself is tuned without the use of a master filter or VCO. Direct tuning is advantageous for RF high-Q LC filters as it can use the same ADC and digital circuits that are used for demodulating the signal. Furthermore, it eliminates the power, extra silicon area and reference oscillator interference of the master tuning circuit [78][95]. In addition, it does not suffer from matching tolerances, which make it too difficult to implement a master-

slave architecture. For example, at a Q of 240 and a center frequency of 2.4 GHz, the maximum frequency deviation between the master and slave filters has to be in the order of 0.1% (less than half the filter bandwidth). This would require the inductors and capacitors of the 2 filters to match within a maximum of 0.2%, which is very difficult to achieve.

A drawback of direct tuning is that a tuning cycle is required at which time no signal can be received. This is not a major problem as many digital transmission schemes can accommodate a small tuning period.

The tuning technique starts with an initial tuning, where no input signal is applied. The filter shapes the noise at its input according to its transfer function. The filter center frequency is first tuned with the filter in oscillation. An FFT is performed on the filter output and the peak frequency is measured in the resulting frequency response. The Q control voltage of the filter is then gradually reduced while repeatedly performing frequency tuning to accommodate for any dependence of frequency on the filter Q. The output amplitude is then measured to finely adjust the filter Q. During normal filter operation, short refresh tuning cycles are performed to update the operating center frequency and Q of the filter.

To demonstrate the filter tuning, the output of the filter was mixed down to a 485 MHz frequency using a Mini-circuits ZEM-4300 mixer. An 8-bit ADC (TLV5580) with a 700 MHz input bandwidth was used to sub-sample the down converted signal using a sampling frequency of 40 MHz (a sub-sampling ratio of approx. 12). A GPIB interface board was used to collect data from the ADC and transfer it to the controlling PC. The PC performed a 1024-point FFT, which provided a tuning resolution of 78 KHz.

The tuning algorithm was implemented on an Alterra Apex20K400 FPGA that has 20K gates, 4 Kbytes of ROM and 16 Kbytes of RAM, all clocked at a 40 MHz clock signal. The FFT process took approx. 52 μ sec. Assuming a filter refresh tuning cycle every 300 msec, the average power needed for the tuning algorithm is approx. 2.1 μ A ($< 0.1\%$ of total filter power), while achieving a Q accuracy of $\pm 0.68\%$. In comparison, a master-slave tuning architecture, such as that reported in [95], uses as much power as needed by the filter itself thus doubling the total filter power.

6.6 Experimental Results

The fabricated filter had a center frequency of 4.7 GHz instead. The deviation of the frequency from the intended frequency of 5.5 GHz is mainly attributed to the inaccuracy in the value of the implemented inductor, the inaccuracy of the cmosp18 models at such high frequencies, and the non-accounted for parasitic capacitors.

Single ended inputs and outputs were used, due to lack of baluns for the 5 GHz operation. As a result, the 4.7 GHz filter is poorly matched, especially at the input, and the measured dynamic range is significantly affected. However, the results obtained for the dynamic range of the filter demonstrate its feasibility.

Figure 6.9 shows a plot of the measured SFDR versus the filter Q for the filter. The results agree with equation (4.17), which relates the dynamic range of the filter to its Q in an inverse square manner. As seen from the plot, a SFDR of approx. 35 dB was measured at a bandwidth of 20 MHz (channel bandwidth for a transceiver using the IEEE802.11a standard) or a Q of approx. 250. An example of tuning results of the filter are shown in Figure 6.10, where the filter is shown tuned to different frequencies within its tuning range.

Figure 6.9 Measured SFDR vs. Filter Q for the 4.7 GHz Filter

Figure 6.10 Frequency Tuning of the 4.7 GHz Filter

In Figure 6.11, examples of tuning the Q to different values are shown. Measurement results for the filter's performance are summarized in Table 6.3. Package limitations prevented using off-chip matching components optimization, resulting in a

much higher noise figure for the filter. Proper design of the input transconductor for 5 GHz would improve this result (as well as the dynamic range) dramatically.

Figure 6.11 Q-Tuning of the 4.7 GHz Filter

Table 6.3 Summary of the 4.7 GHz Filter Performance Results

Measure		Value
Area		650 μ m $\times$ 650 μ m=(0.4225 mm ²)
Power Supply		1.2 – 1.8 V
Center Frequency		(4.48–4.92) GHz
Noise Figure		15 dB
Q _o (simulated)		8.449
Operating Q		235
SFDR		37 dB ¹
Current	Input Stage	2 mA
	Q-enhancement	0.8 mA
Total Power		4.2 mW

¹ Noise integrated over 20-MHz bandwidth

The filter chip micrograph, implemented in a standard digital 0.18 μ m CMOS technology, is shown in Figure 6.12.

Figure 6.12 The 4.7 GHz Filter Chip Micrograph

Table 6.4 compares the current filter implementation with previous published work.

Table 6.4 Comparison of Implemented HF Filter with Recent Publications

Author, Date	Technology	Frequency	Q range	Dynamic Range
Kuhn, 1998 [67]	0.8 μm CMOS	850 MHz (2 nd order)	20 – 250	1 dB Dynamic Range of 75 dB with Q of 45
Duncan, 1997 [69]	0.8 μm BiCMOS	750 MHz (2 nd order)	10 – 490	SFDR of 25 dB with Q of 25
Pipilos, 1996 [68]	0.8 μm Bipolar	1.8 GHz (2 nd order)	3 – 350	1 dB Dynamic Range of 40 dB with Q of 35
Wu, 1997 [96]	0.8 μm CMOS	880 MHz (2 nd order)	2.2 – 44	1 dB Compression of -30 dBm with Q of 30
Li, 2001 [95]	0.25 μm BiCMOS	1.9 GHz (4 th order)	N/A	1 dB Dynamic Range of 63 dB with BW of 150 MHz
Devries, 2001 [89]	0.18 μm CMOS	500 MHz	100-1000	1 dB Dynamic Range of 41 dB with Q of 650
		2.4 GHz		1 dB Dynamic Range of 31 dB with Q of 530
This Work, [70]	0.18 μm CMOS	4.7 GHz	50-500	SFDR of 37 dB with a Q of 235

Performance levels achieved by the prototype indicate that Q-enhanced filtering offers a viable approach to solving the on-chip bandpass-filtering problem. These filters can therefore be expected to play an important role in the development of future integrated transceiver products.

6.7 Injection Locking Results

Due to the mismatching of the filter at the input, as explained earlier, it was not possible to apply subharmonic injection to the 5 GHz filter/oscillator due to the large amount of required injection power. Fundamental Injection locking is applied instead to injection lock the free running oscillator. Figure 6.13 shows the plots for the oscillator before and after locking.

a. Free running Oscillator

b. Fundamental Injection Locked Oscillator

Figure 6.13 Captured Output of the 4.7 GHz Oscillator

6.8 Conclusion

Performance levels achieved by the prototype filter, presented in this chapter, indicate that Q-enhanced filters, implemented in standard CMOS process, can be well extended to the 5-GHz ISM band where a growing number of high-speed wireless

networking is in operation. They can provide good dynamic range at very low power consumption and reasonably small silicon area. They may offer a viable approach to solving the on-chip RF bandpass filtering problem without the usual reported excessive power consumption. These filters can therefore be expected to play an important role in the development of future integrated transceiver products.

Having established the feasibility of implementing such filters at these frequencies, the possibility of applying the proposed transmit architecture presented in the chapter five to higher frequencies is validated. This is supported by obtained experimental results of injection locking of the implemented filter.

Chapter 7. Conclusion

7.1 General

There is no doubt that communications in general, and wireless communications in particular, will remain one of the dominant drivers for the semiconductor industry. In the design of RFICs for wireless communications, the challenge is not only achieving successful operation at a relatively high frequency, but also in doing so for widely varying application environments, under tight constraints such as cost, size and power consumption.

Recently, a large number of applications for wireless communications has been widely deployed and in development. These applications range from positioning or navigation devices, to low-data rate, wireless devices used for indoor control applications, to high-speed applications. This increase in wireless communications has prompted researchers for more in-depth exploration of wireless transceiver architectures and used IC technology.

Transceiver architectures, used for both the receiver and transmitter, have been analyzed by several authors. The search has always been for architectures that render themselves easily for integration at low-power operation. Depending on the application, some architectures, like the direct conversion architecture, that once seemed impractical are now being used as plausible solutions.

Deep submicron CMOS technologies are now strong contenders for Bipolar and GaAs technologies. With transistor gate lengths less than $1\mu\text{m}$, high unity gain frequencies compared to those achieved with SiGe Bipolar transistors are possible. In addition, new MOS-appropriate circuit techniques have been developed for many of the RF, IF, and baseband blocks required in state-of-the-art wireless transceivers. Furthermore, MOS-based designs can achieve higher form factors, dissipate less power, can combine both digital and analog parts of the transceiver on the same chip, and this is achieved at a very low price. All of the above has made CMOS, the technology of choice for most wireless transceivers evolving on the market.

While most of the research effort has concentrated on the receive side, few researchers have addressed the transmit side. The aim is always for a simpler, more compact, and more power efficient transmitter.

7.2 Conclusions

In this thesis, we address the field of low power wireless transceiver design, with the transmit side as the main objective for enhancement. Simplicity, power efficiency & compactness were the main targets for improvement. To achieve these goals, several strategies are utilized. First, a simple, easy to implement direct conversion scheme is adopted for the proposed transmitter. Second, subharmonic Injection locking is used as a method for frequency synthesis. This allows the use of lower synthesizer reference frequencies, with better phase noise and less power consumption. Theoretical analysis of this type of injection is performed to have a deeper insight into its operation. While most of the reported work on using subharmonic injection locking uses a sinusoidal signal as the injection signal and depend on the oscillator nonlinear core to create the different

harmonics needed for injection, in our work we make use of a clock signal as the injection source. A periodic pulse waveform has all the necessary harmonics. These harmonics are inserted into an amplifier tuned to the desired one. Thus, only the harmonic of interest is amplified before being applied to the oscillator nonlinear core. Several Q-enhanced filters, to be used as oscillators, are designed with different centre frequencies and the subharmonic injection technique is applied to them. Comparison between the derived theoretical results and the obtained measurements reveal the close matching between the two.

This leads to the third applied concept in our proposed architecture, where no additional circuitry for the VCO is used. Instead, a Q-enhanced filter in the receive path is utilized as a VCO in the transmit path, thus saving both space and power for the whole transceiver. Specifically, the ability of a Q-enhanced filter to operate as an oscillator has triggered this advantage. Furthermore, the introduction of the direct digital tuning of the VCO, allows its locking with as minimum power as possible without the need for large locking range.

Since a major problem with direct conversion structures is LO pulling by the PA, the proposed structure has to offer immunity to this problem. It is found by experiment that this problem is alleviated in the proposed architecture even with the PA transmitting as high as 10 dBm. This verifies the robustness of the proposed structure.

Finally, the communications frequency spectrum is getting more crowded in the 915-MHz and 2.4-GHz ISM bands. Furthermore, larger bandwidths are required for increasingly demanding wireless data transfer applications. New communication frequency standards are introduced in the 5-GHz ISM band. To extend the proposed

transmit structure to such higher frequencies, the feasibility of implementing a fully integrated CMOS Q-enhanced filter operating in this band is vital. A design targeting these frequencies is implemented. It proves the feasibility of extending the operation of such filters to higher frequencies that were never explored before, giving some promise of using such filters in receivers operating in these bands. In addition, it allows us to study the possibility of applying the injection locking techniques to such filters at such high frequencies.

7.3 Future Work

There are, of course, a number of areas in which transceiver design could further be enhanced. The following can be used as some ideas for future work,

- *Studying the effects of different modulation techniques on LO pulling in the proposed transmitter structure.*
- *Studying the reduction of the phase noise of Q-enhanced filters/oscillators for better phase noise performance at large frequency offsets.*
- *Implementation of a complete monolithic, fully differential, fractional-N, Synchronous Oscillator SO-based synthesizer structure, within a whole transmit chain, and optimization of its current consumption so as to achieve overall low-power consumption.*
- *Studying the feasibility of applying the proposed transmit structure for more strict communications standards.*
- *Implementation of a complete CMOS transceiver based on Q-enhanced filters in the 5-GHz band.*

Conclusion

- *Exploring methods and structures aiming at enhancing the linearity of Q-enhancement circuitry so as increase the maximum achievable dynamic range and lower the overall noise figure of Q-enhanced active filters.*

Appendix “A” Chip Level Layouts

A.1 Chip One “ICFCUMA1”

Figure A.1 Chip Configuration of ICFCUMA1

A.2 Chip Two “ICFCUMA2”

Figure A.2 Chip Configuration of ICFCUMA2

Appendix “B” Filter Tuning Algorithm

```
% Digital Tuning Algorithm

% July 23, 2001

% variables

global data;

% nStepsCoarse = 2^10;

% nStepsFine = 2^14;

samplingFreq = 40e6;

tuneFreq = 18e6;      % frequency to tune to (between 0 and samplingFreq/2)

vf = -0.691;

%vf = 0.84834;

vQ = 0.18;

vfIncCoarse = 2e-3;    % amount to increment each step in frequency

vfIncFine = 500e-6;    % amount to increment each step in frequency

vQIncCoarse = 3e-3;    % amount to increment each step in Q

vQIncFine = 200e-6;    % amount to increment each step in Q

freqTolCoarse = 0.05e6; % tolerance for frequency tuning

freqTolFine = 0.05e6;  % tolerance for frequency tuning

RMS_limit = 9;         % limit at which to switch the attenuator/rfamp
```

```
RMS_final = 40;    % final Q to meet

RMS_tol = 0.5;

% set rfamp and attenuator at minimum

attenSet(0);

rfampSet(4.5);

pause(1);

vset(SMQ, vQ);

vset(SMf, vf);    % start frequency in the center of the band (1.08 - 1.1)

[RMS_Data, f_c] = fishcount(samplingFreq);

if f_c < tuneFreq

    fincrement = 1;

else

    fincrement = 0;

end

% coarse frequency tuning

while abs(f_c - tuneFreq) > freqTolCoarse

    if f_c < tuneFreq

        if fincrement == 0

            vflncCoarse = vflncCoarse / 2;    % decrease the increment

        end

        vf = vf + vflncCoarse;
```

```
    fincrement = 1;

    else

    if fincrement == 1

        vfIncCoarse = vfIncCoarse / 2;           % decrease the increment

    end

    vf = vf - vfIncCoarse;

    fincrement = 0;

end

vset(SMf,vf);

[RMS_Data,f_c]=fishcount(samplingFreq);

disp(sprintf('f adjusted to vf= %f, f_c = %f, Increment = %f,vf,f_c,vfIncCoarse));

%disp(sprintf('RMS= %f,f_c=%f,RMS_data,f_c));

end

Qincrement = 0;           % set previous increment to 0 meaning down

% Q tuning rfAmp @ 4.1

while abs(RMS_Data - RMS_limit) > RMS_tol

    if RMS_Data < RMS_limit

        if Qincrement ==0

            vQIncCoarse = vQIncCoarse / 2;           % decrease the increment

        end

    end

end
```

```
vQ = vQ + vQIncCoarse;

Qincrement = 1;

else

    if Qincrement == 1

        vQIncCoarse = vQIncCoarse / 2;          % decrease the increment

    end

    vQ = vQ - vQIncCoarse;

    Qincrement = 0;

end

vset(SMQ,vQ);

[RMS_Data,f_c]=fishcount(samplingFreq);

disp(sprintf('Q adjusted to vQ= %f, RMS_data = %f, Increment = ....

            %f,vQ,RMS_Data,vQIncCoarse));

if f_c < tuneFreq

    fincrement = 1;

else

    fincrement = 0;

end

% fine frequency tuning
```



```
vfIncFine_step = vfIncFine;

while ((abs(f_c-tuneFreq)>freqTolCoarse) & (RMS_Data > RMS_limit-RMS_tol)

% ensure frequency tuning is done whenever we are above the limit

% or coarse Q tuning is complete (the while loop will be finished above)

if f_c < tuneFreq

    if fincrement == 0

        vfIncFine_step = vfIncFine_step / 2;          % decrease the increment

    end

    vf = vf + vfIncFine_step;

    fincrement = 1;

else

    if fincrement == 1

        vfIncFine_step = vfIncFine_step / 2;          % decrease the increment

    end

    vf = vf - vfIncFine_step;

    fincrement = 0;

end

vset(SMf,vf);

[RMS_Data,f_c]=fishcount(samplingFreq);

disp(sprintf('vf= %f, f_c = %f, inc = %f',vf,f_c,vfIncFine_step));
```

```
end

end

disp(sprintf('finished coarse tuning, vQ = %f, frequency = %f',vQ,f_c));

% fine Q tuning rfAmp @ 4.3 no attenuation
attenSet(1); % change attenuation to minimum
rfampSet(4.3);

% 1 last fine frequency tune (with 2^14 data points)
[RMS_Data,f_c]=fishcount(samplingFreq);
disp(sprintf('FF tune: vf= %f, f_c = %f',vf,f_c));

vfIncFine = 100e-6;

while (abs(f_c-tuneFreq) > freqTolFine)

% ensure frequency tuning is done whenever we are above the limit

% or coarse Q tuning is complete (the while loop will be finished above)

    if f_c<tuneFreq

        vf = vf + vfIncFine;

    else

        vf = vf - vfIncFine;

    end

end
```

```
vset(SMf,vf);

[RMS_Data,f_c]=fishcount(samplingFreq);

disp(sprintf('FF tune: vf= %f, f_c = %f',vf,f_c));

end

[RMS_Data,f_c]=fishcount(samplingFreq);

while abs(RMS_Data-RMS_final)>RMS_tol

    if RMS_Data < RMS_final

        if Qincrement ==0

            vQIncFine = vQIncFine / 2;           % decrease the increment

            end

            vQ = vQ + vQIncFine;

            Qincrement = 1;

        else

            if Qincrement == 1

                vQIncFine = vQIncFine / 2;           % decrease the increment

                end

                vQ = vQ - vQIncFine;

                Qincrement = 0;

            end

        end

    end
```

```
vset(SMQ,vQ);

[RMS_Data,f_c]=fishcount(samplingFreq);


% filter data

% filterOrder = 80;

% filtDenCoef1 = fir1(filterOrder,[tuneFreq*2/samplingFreq-0.025
% tuneFreq*2/samplingFreq+0.025]);

% bandpass1 definition

% filtNumCoef = zeros(1,filterOrder);

% filtNumCoef(1) = 1;

% outData = filter(filtDenCoef1,filtNumCoef,outData);    % filter1 response

disp(sprintf('Q tuning, RMS level: %f, vQ: %f',RMS_Data,vQ));

end
```

Appendix “C” Algebraic Relations

Euler’s Theorem

$$e^{j\varphi} = \cos \varphi + j \sin \varphi$$

Some Trigonometric Identities

- $\cos^2 x = \frac{1}{2}(1 + \cos 2x)$
- $\cos^3 x = \frac{1}{4}(3 \cos x + \cos 3x)$
- $\cos^4 x = \frac{1}{8}(3 + 4 \cos 2x + \cos 4x)$
- $\cos^5 x = \frac{1}{16}(10 \cos x + 5 \cos 3x + \cos 5x)$
- $\cos^6 x = \frac{1}{32}(10 + 15 \cos 2x + 6 \cos 4x + \cos 6x)$
- $\cos^7 x = \frac{1}{64}(35 \cos x + 21 \cos 3x + 7 \cos 5x + \cos 7x)$
- $\cos^8 x = \frac{1}{128}(35 + 56 \cos 2x + 28 \cos 4x + 8 \cos 6x + \cos 8x)$
- $\cos^9 x = \frac{1}{256}(126 \cos x + 84 \cos 3x + 36 \cos 5x + 9 \cos 7x + \cos 9x)$
- $\cos^{10} x = \frac{1}{512}(126 + 210 \cos 2x + 120 \cos 4x + 45 \cos 6x + 10 \cos 8x + \cos 10x)$
- $\cos^{11} x = \frac{1}{1024}(462 \cos x + 330 \cos 3x + 165 \cos 5x + 55 \cos 7x + 11 \cos 9x + \cos 11x)$

Some Algebraic Polynomial expansions

- $(a + b)^2 = a^2 + 2ab + b^2$

- $(a + b)^3 = a^3 + 3a^2b + 3ab^2 + b^3$
- $(a + b)^4 = a^4 + 4a^3b + 6a^2b^2 + 4ab^3 + b^4$
- $(a + b)^5 = a^5 + 5a^4b + 10a^3b^2 + 10a^2b^3 + 5ab^4 + b^5$
- $(a + b)^6 = a^6 + 6a^5b + 15a^4b^2 + 20a^3b^3 + 15a^2b^4 + 6ab^5 + b^6$
- $(a + b)^7 = a^7 + 7a^6b + 21a^5b^2 + 35a^4b^3 + 35a^3b^4 + 21a^2b^5 + 7ab^6 + b^7$
- $(a + b)^8 = a^8 + 8a^7b + 28a^6b^2 + 56a^5b^3 + 70a^4b^4 + 56a^3b^5 + 28a^2b^6 + 8ab^7 + b^8$
- $(a + b)^9 = a^9 + 9a^8b + 36a^7b^2 + 84a^6b^3 + 12a^5b^4 + 126a^4b^5 + 84a^3b^6 + 36a^2b^7 + 9ab^8 + b^9$
- $(a + b)^{10} = a^{10} + 10a^9b + 45a^8b^2 + 120a^7b^3 + 210a^6b^4 + 252a^5b^5 + 210a^4b^6 + 120a^3b^7 + 45a^2b^8 + 10ab^9 + b^{10}$
- $(a + b)^{11} = a^{11} + 11a^{10}b + 55a^9b^2 + 165a^8b^3 + 330a^7b^4 + 462a^6b^5 + 462a^5b^6 + 330a^4b^7 + 165a^3b^8 + 55a^2b^9 + 11ab^{10} + b^{11}$

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