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**DESIGN, MODELING, AND OPTIMIZATION OF ECL INTERFACE
CIRCUITS FOR BiCMOS INTEGRATED SYSTEMS**

Neil S. Pickles, B.Sc. (Eng.)

**CARLETON UNIVERSITY
Ottawa, Canada**

**A thesis submitted to
the Faculty of Graduate Studies and Research
in partial fulfillment of
the requirements for the degree of
Master of Engineering**

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**"Design, Modeling, and Optimization of ECL Interface
Circuits for BiCMOS Integrated Systems"**

**submitted by Neil S. Pickles, B.Sc. (Eng.)
in partial fulfillment of the requirements for
the degree of Master of Engineering**

Thesis Supervisor

Chairman, Department of Electronics

Carleton University

April 15, 1993

Abstract

With the emergence of BiCMOS process technology, it is possible to exploit the inherent benefits of CMOS and bipolar transistors on the same wafer. Specifically, emitter-coupled logic (ECL) is suited for I/O circuits due to its fast speed and enhanced drive capabilities. This thesis analyzes temperature and voltage compensated ECL input and output buffers with the goal of developing fast circuits which consume minimum power. Sensitivity analysis of standard buffers is described in order to understand which circuit parameters contribute to delay. A method of macromodeling individual buffers is also developed which produces accurate delay information suitable for inclusion in a timing simulator. The macromodels can be used to predict propagation delay and output rise and fall times for a given input voltage rise time, circuit power, and output capacitive loading. It is shown how mathematical techniques can be applied to the resultant equations to optimize the circuits for minimum delay. Non-standard ECL I/O circuits are also described which have potential for even higher speed.

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Chapter 1

Introduction

1.1 Perspective

Emitter-coupled logic (ECL) is a popular logic family for integrated circuit design which is used for its high speed and enhanced drive capabilities. As BiCMOS processes are becoming available for the realization of VLSI circuits, ECL is an important logic family that may be used to exploit the advantages of having CMOS and bipolar transistors on the same wafer. ECL can be used in those sections of a chip where the fastest speed is required. One such application is for input and output buffers where ECL can be used to interface internal CMOS and BiCMOS logic with off-chip systems operating at ECL levels. Typically, enhanced drive is required to charge and discharge large capacitive loads and ECL is ideally suited for this task. Possible applications for ECL buffers include heterogeneous system integration and multiple chip modules.

For optimizing high-speed circuitry, modeling of signal path delays and transient times is of great importance, as too often simulation times are excessive with device level simulators. Although simulators such as HSPICE[Meta90] can produce highly accurate delay information, computation times increase rapidly with the number of modeled devices. Macromodels can be developed to avoid this problem by considering each circuit logic block as a cell where the performance characteristics of the cell are functions of internal parameters and boundary conditions. In the case of an ECL buffer the internal parameters consist of transistor sizes and switching currents. Boundary conditions include the input voltage waveform and load capacitance.

The objective of macromodeling is to characterize the delay timing of a logic block in a form which may be used by a large scale circuit simulator. The characteristics of

each logic block can be expressed in closed form for inclusion in a standard cell library. An important reason for doing this is to enable large complex circuits to be simulated accurately with reasonable computation time. A further reason for developing macro-models is that the characterizing equations can be used for performance optimization. Mathematical techniques can be applied to the equations to produce optimum circuits across chip boundaries.

1.2 Objective

The main goal of this thesis is to study high-speed ECL input/output interface buffers in the context of BiCMOS technology. Of particular interest is the investigation of a method of optimizing circuit performance in terms of power, delay, and area trade-off. To this end, three specific objectives have been identified. The first objective is the complete design, including layout, of I/O buffers under specific constraints. The second objective is the application of classical circuit analysis techniques to these circuits. This provides meaningful insights into optimization opportunities and strategies. The final objective is the application of mathematical performance optimization techniques based on accurate timing macromodels derived from SPICE simulations.

1.3 Outline of Thesis

To meet the objectives, the thesis is organized into 7 chapters. Chapter 2 lays the foundation of the study by presenting principles of ECL circuit design with emphasis on standard ECL topology and desired transistor characteristics. The principles for a temperature and voltage insensitive reference voltage are also described. The design of standard ECL I/O circuits is then presented in Chapter 3. This chapter provides a method of circuit design which includes schematic modeling and layout. As well, simulation data is presented and this forms the basis for further analysis. In order to under-

stand which of the buffer parameters are important to minimize, transient time delay expressions based on classical RC sensitivity techniques are presented in Chapter 4. The derived equations are then analyzed with a cursory view towards optimization. Chapter 5 expands on the desire to develop fast circuits by presenting an accurate timing macromodel. Algorithms used to develop the model and results are presented. Chapter 6 then examines ECL I/O circuit topologies which differ from those previously presented but which have the potential for even faster speed. Finally, Chapter 7 provides conclusions and recommendations for further research.

Chapter 2

ECL Overview

Emitter-coupled logic (ECL) has been chosen to develop fast BiCMOS I/O buffers because it is the fastest known logic family for silicon integrated circuits. Compared with TTL and IIL bipolar logic families, higher speeds are possible due to the reduced voltage swing and because switching transistors are not allowed to saturate. Increased layout area is necessary for monolithic design of ECL, however, because each logic gate requires additional circuitry in the form of bias circuits and current sources. Similar auxiliary circuits are not required for most other logic families which are slower. The lower circuit density is often not limiting because ECL logic also consumes the most power. Integrated package power limitations may restrict the number of ECL gates that can be placed on a wafer.

2.1 Basic ECL Logic Gates

The basic NOR/OR ECL gate is shown in Figure 2.1 where the sources V_{EE} and I_{CS} define the circuit power and resistors R_{L1} and R_{L2} define the logic swing.

Figure 2.1: Basic ECL Gate

The heart of the ECL logic gate is the difference amplifier which has transistor emitters connected together: hence the name "emitter coupled logic". Unlike other logic families which have transistors switching between the cut off and saturation regions, transistors in ECL circuits operate in either the cut off or active regions. The circuits can operate faster because excess charge, consisting of minority carriers, need not be removed from the base during transitions from the on-state to the off-state[Mill79].

The transistors are forced to operate in the active region by limiting the collector current such that $I_B \leq I_C/\beta_F$, where I_B and I_C are the base and collector currents respectively. To avoid saturation it is necessary to maintain the base current at a level just large enough to ensure $I_B = I_C/\beta_F$. Because of the wide variance of β_F , it is practical to control the collector current with the constant current source rather than by controlling the base current. In this way, if $V_{CE} \geq 300mV$, the transistors are forced to operate in the active region.

The input transistors steer the current I_{CS} between the two circuit legs shown in Figure 2.1. If the base voltage of the input transistor is held sufficiently below the reference voltage then the transistor will be cut off and there will be no current through its collector. In this case, all of I_{CS} will flow through the reference transistor. When the input voltage equals the reference voltage, the current will be equally split between the two switching transistors. As the input voltage is increased further, the emitter voltage rises because V_{BE} is nominally constant. The reference transistor therefore becomes cut off and the current produced by the current source is switched to the input circuit leg. Because the collector currents are exponentially dependent on the base-emitter voltages, it requires only a small change in the input voltage to switch the currents. For

a practical current source, the difference in total emitter current between the two logic states is less than 2%[Elma83].

The basic circuit of Figure 2.1 shows that ECL gates have complementary outputs of OR and NOR which may be convenient for certain applications. Typically, the voltage signals at the collectors of the differential amplifier transistors are connected to emitter followers to provide buffering and a low output impedance. The buffering level shifts the output by V_{BE} of the transistor and the logic high level is therefore clamped to about -0.85V . The low logic level, on the other hand, is dependent on the voltage drop due to the current through the load resistor R_L . Typically, a voltage swing of about 0.85V is chosen to ensure adequate noise margins. This results in a logic low level of about -1.7V .

Unlike other bipolar digital logic families such as RTL, DTL, and TTL, it is common in ECL circuits to ground the positive end of the supply. The reason for doing so is to minimize output voltage perturbations for induced power supply noise. By referring the output to the positive supply, power supply noise is attenuated across the collector-emitter junction of an emitter follower transistor which buffers the output[TaSc77]. This occurs because for a small-signal model, the collector to emitter impedance in the active region is the resistance seen looking out from the base divided by $h_{FE} + 1$. Almost all the noise, therefore, is seen across the emitter follower pull down resistor because this resistance value is about 500 times greater. For compatibility with external systems and test equipment such as signal sources and measuring devices, this reference supply (the positive supply) is usually grounded[Herb85].

The transfer characteristics of a typical ECL gate is shown in Figure 2.2. From this diagram it is clear that the maximum input low voltage, $V_{IL(max)}$, and the minimum input high voltage, $V_{IH(min)}$, are at about the same potential difference from the refer-

ence voltage, V_{ref} . The reference voltage and the value of the dropping resistors are chosen such that the output potentials straddle the reference voltage. The high and low noise margins are thus equivalent.

Figure 2.2 Typical ECL Transfer Characteristic

The asymmetrical character of the NOR output is a distinguishing feature of the transfer characteristics and its explanation serves to highlight circuit operation. With an applied voltage of $V_{IL(max)}$, the input transistor is cut off and the NOR output voltage is $1 V_{BE}$ drop below ground. When the input voltage rises above $V_{IH(min)}$, and all of the emitter current is transferred to the input transistor, a further increase in input voltage results in an increase in collector current. The output therefore continues to fall until the input transistor becomes saturated. At this point the output voltage begins to rise and V_{CE} of the input transistor falls below the saturation limit of about 0.3V. Any further increase in input voltage now causes an increase in the NOR output voltage as current is diverted to the base and away from the collector[TaSc77].

2.2 Band-gap Voltage Reference Principles

Temperature independent biasing sources are necessary circuits for implementing ECL logic gates. In the literature, two basic techniques for implementing such sources are described: the Zener diode current reference and the band-gap voltage reference.

Temperature independent currents can be obtained with a Zener diode reference but the NPN transistors of such circuits typically exhibit breakdown voltages between 6 and 8 volts thus necessitating a large supply voltage[Greb84]. Because ECL logic typically operates with a supply voltage magnitude less than 5.5V, the circuit is impractical for this application. More suitable, however, is a band-gap reference network.

The band-gap reference network may be used to produce a temperature compensated voltage to supply a current source. The current source of Figure 2.1 can be implemented by applying a constant voltage to the base of a transistor as shown in Figure 2.3. The collector current is approximately equal to $(V_{CS} - V_{BE})/R$, where V_{CS} is supplied by a band-gap reference.

Figure 2.3: Current Source

A band-gap reference supplies constant voltage by effectively summing two derived terms of equal magnitude but opposite sign. It is well known that for a constant collector current, V_{BE} of a transistor falls at a rate of about $-2\text{mV}/^\circ\text{C}$ [Greb84]. Likewise, V_T of a transistor exhibits a temperature coefficient of about $+0.085\text{mV}/^\circ\text{C}$. By scaling these two quantities and summing the result, a constant voltage of about 1.25V with respect to V_{EE} may be obtained. It can be shown mathematically that this output voltage is related to the band-gap voltage for silicon and from this dependence, the

circuit obtains its name. The principle of operation of a band-gap reference circuit is shown graphically in Figure 2.4[extracted from Greb84].

Figure 2.4: Principle of Band-gap Reference Circuit Operation

A practical realization of a band-gap circuit is shown in Figure 2.5 which is a basic circuit proposed by Widlar[Widl71]. The output voltage is equal to the base-emitter drop of Q_3 plus the voltage drop across R_2 . Constant output voltage is maintained for increased temperature by increasing the current through R_2 to compensate for the reduction of $V_{BE,Q3}$. The current is increased as the emitter voltage of Q_2 rises. This voltage rises for increased temperature because the current density in Q_1 is about 6 times greater than it is in Q_2 . For rising temperature, $V_{BE,Q1}$ changes less than that of $V_{BE,Q2}$. The temperature insensitive output is dependent on the circuit parameters as described in Appendix A.

An important parameter of merit for a band-gap reference is the variation in output voltage that occurs over the expected temperature range. This parameter is described in Appendix B as TC_F . For temperatures of $-55^\circ C$ to $125^\circ C$, TC_F is usually less than

40ppm/°C. However, for the designated temperature range for 100K ECL, which is 0°C to 85°C, TC_F improves to about 20ppm/°C[Greb84].

Figure 2.5: Band-gap Voltage Source

2.3 Simulation of High-Speed ECL Circuits

One of the most important figures of merit for a bipolar transistor is the transit frequency f_T . This is defined as the frequency at which the common-emitter short circuit current gain attains unity magnitude. The value of f_T and its dependence on collector current must be precisely known for accurate simulation of high-speed circuits since both the forward transit time τ_F and the emitter-base junction capacitance C_{JE} are derived from them[Rein83]. Maximizing f_T also ensures the fastest circuits [Chua92].

A typical graph of f_T vs. I_C is shown in Figure 2.6. This graph shows f_T dependent on collector current as it reaches a maximum and then falls off. f_T has been shown to vary as a function of collector current as in Equation 2.1[Getr84].

$$\frac{1}{2\pi f_T} = \tau_F + \frac{kT}{qI_C}(C_{JE} + C_{JC}) + R_C C_{JC} \quad (2.1)$$

Figure 2.6: Typical f_T vs. $\log I_C$

The decrease in f_T at low collector current is caused by the second term on the right-hand side of Equation 2.1. At low currents the parasitic surface recombination of carriers in the base-emitter depletion region is primarily responsible for the lower f_T . f_T is relatively constant in the mid-current region, however, as the I_C term becomes negligible and τ_F remains constant. In the high-current region an abrupt decrease in f_T occurs due to three effects: decrease of emitter efficiency, emitter-crowding, and the Kirk effect. The decrease in emitter efficiency is caused by a large number of excess minority carriers which exist in the base to reduce the effective base resistivity near the base-emitter junction and the emitter-crowding effect is caused by the ohmic drop within the active base region due to increased base current[Greb84]. The Kirk effect also causes the decrease in f_T at high current densities as this causes τ_F to increase. When the minority carrier density in the base-collector junction approaches the doping density of the collector, the transistor region boundary adjacent to the neutral base layer is displaced towards the collector. The resulting widening of the base layer increases τ_F as the base storage time increases[Kirk62].

For applications in high-speed ECL design, the above discussion is significant with consideration to circuit simulation techniques. The Gummel-Poon models used in HSPICE simulations may not be exact enough to accurately simulate the switching behavior in the high-current region. In the Gummel-Poon model, the current dependence of τ_F is determined by parameters extracted from the measured dc characteristics. The high-current effects are then simulated by noting the value of knee-current, I_K , above which τ_F increases. This dependency is shown in Figure 2.7[extracted from Elma83].

Figure 2.7: τ_F vs. $\log I_C$ Demonstrating High-Current Effect on Forward Transit Time

Stubing has noted that because of large errors in τ_F , this approach is not suited for accurately simulating the switching behavior in the high-current region[Stub87]. Consequently, the collector current at maximum f_T should be interpreted as the starting point of τ_F rise and ECL circuits should not operate beyond that current density. Specifically, the switching transistors chosen for the ECL I/O buffers should be large enough to ensure that high-current effects are not a concern. Ideally, the transistors should operate in the region of the f_T curve slightly to the left of maximum near the peak.

2.4 Overview of ECL Logic Families

Two major semiconductor companies market ECL discrete components: Motorola and Fairchild. Among the available ECL families, the popular series are designated 10K and 100K. Both of these families contain over 50 elements consisting of gates, buffers, flip-flops, latches, multiplexers, counters, etc. As can be seen from the basic gate characteristics of Table 2.1, the major difference between the 10K and 100K series is the slower rise times and propagation delays of the 10K family. Slower speeds prevent significant ringing and avoid the necessity of critical system layout at the expense of decreased throughput. The other families which are listed may be used to match their properties to an intended application.

As can be seen from Table 2.2 [Fair95, Moto91], the logic levels of the 10K and 100K families are nearly equivalent, which allows for their interconnection. The recommended power supply differs, however, as 10K is powered with a nominal supply of $-5.20 \pm 5\%V$ as opposed to $-4.50 \pm 7\%V$ for 100K. Additionally, Motorola's 100K series can operate with a supply voltage within the range of $-4.2V$ to $-5.46V$.

family	Typical Gate Characteristics				
	propagation delay (ns)	transition time (ns)	input power (mW)	speed power product (pJ)	max. flip-flop count frequency (MHz)
MECL 10K	2.0	3.5	25	50	50
MECL III	1.0	1.0	60	60	300
MECL 10KH	1.0	1.0	25	25	250
F10K	2.0	1.0	25	50	50
F95K	2.0	1.0	25	50	50
F100K	0.5	0.85	50	38	400
F11C	0.7	0.7	62	43	600

Table 2.1: ECL Family Characteristics

	MECL 10K	Fairchild 100K
$V_{OH(max)}$ (V)	-0.81	-0.88
$V_{OH(min)}$ (V)	-0.96	-1.03
$V_{OL(max)}$ (V)	-1.65	-1.62
$V_{OL(min)}$ (V)	-1.85	-1.81

Table 2.2: ECL 10K and 100K Logic Levels

While both 10K and 100K families have voltage compensation in the form of a voltage regulator circuit for V_{CS} , the MECL 100K, F95K, and F100K series have additional temperature compensation in the form of a cross-coupled diode network and series resistor connected between the output nodes[Fair95, Moto88, Mull72].

Changes in current source biasing also exist between the logic families. The current source for the 10K series is designed to provide constant current by maintaining constant V_{BE} of the current source transistor. The current source for the 100K series, however, is designed such that a constant base voltage of the current source transistor results in increased emitter current as V_{BE} decreases with temperature. The base voltage, in this case, is provided by a band-gap reference circuit. The 100K logic family transfer characteristics are therefore more stable with temperature but the circuit sensitivity to power supply variations is comparable. The sensitivity of output voltage to changes in temperature and supply voltage is listed in Table 2.3[Moto91].

	ECL family	
	10K	100K
$\Delta V_{OH} / \Delta T$ (mV/°C)	1.4	0.15
$\Delta V_{OL} / \Delta T$ (mV/°C)	0.6	0.30
$\Delta V_{CS} / \Delta T$ (mV/°C)	1.0	0.20
$\Delta V_{OH} / \Delta V_{EE}$ (mV/V)	20	20
$\Delta V_{OL} / \Delta V_{EE}$ (mV/V)	30	30
$\Delta V_{CS} / \Delta V_{EE}$ (mV/V)	20	20

Table 2.3: Voltage Sensitivity to Temperature and Supply Voltage

2.5 Summary

Principles of ECL circuit operation have been described in this chapter. The emphasis has been on the ECL NOR/OR gate as this circuit forms the basic building block from which other circuits can be developed. The band-gap reference has also been presented as an important circuit block when implementing ECL logic as it provides a temperature insensitive reference voltage. Its theory and a practical application of this circuit have been described. Principles for high-speed ECL design have been explained with a view towards maximizing the transistor transit frequency (f_T). A comparison between commercial ECL logic families has also been given in order that I/O buffers can be made compatible with industry standards.

Chapter 3

Design of Standard I/O Buffers

A set of input and output buffers have been designed for interfacing on-chip ECL voltage signals with off-chip systems. The circuits have been designed using a proprietary BiCMOS technology using circuit principles described in the previous chapter. A method for design of circuit schematics and layout is described so that the completed designs can be included in a standard cell library.

3.1 Design Constraints

The design of standard input and output buffers is constrained by the process technology which is available for production of the wafers. Design of the circuits also depends on target speed, logic compatibility, and the desirability that the circuits can be placed adjacent to similar pad macros which interface CMOS and TTL I/O signals.

The target process is a BiCMOS process by Northern Telecom Electronics[Hada91]. It is a 0.8 μ m twin-well BiCMOS technology which features buried layers to minimize parasitic resistance and there are three levels of metal interconnect: the first and second layers are made of tungsten, because of its superior electromigration behavior as compared with aluminum, and the top layer is made of an aluminum-silicon-copper alloy. The process has three layers of polysilicon: the first layer is used to define MOSFET gates and capacitor bottom plates, the second layer is used to define polypoly capacitors, and the third layer is used to define NPN emitters and linear resistors. CMOS and bipolar NPN transistors, capacitors, and resistors can be implemented.

The bipolar transistor models do not scale with size in order to produce accurate HSPICE simulations. This constrains circuit design in such a way that discrete devices must be chosen from existing transistor designs. HSPICE models are provided for transistors which have been sized by emitter area. The smallest emitter size is designated 1x and has an emitter area of $4.0 \times 0.8 \mu\text{m}^2$. Other transistors are designated 2x, 4x, 5x, 15x, 30x, and 45x, as each has an emitter length a multiple of the smallest emitter size. For example, a 4x transistor has an emitter size $16.0 \times 0.8 \mu\text{m}^2$. All of the available transistors have been considered for placement in the buffer circuits. In addition, two 4x transistors in parallel have been considered in order to provide an effective transistor size between the 4x and 15x sizes. Plots of the transit frequency dependence on collector current, derived from simulation, are shown in Figure 3.1. This figure features a range of transistor choices suitable for high-speed ECL design.

Although the input and output buffers could be made compatible with any of the commercial logic families, the 100K series is one of the most popular due to its fast operation and stable output. Hence, it is desired to design the circuits to be as similar as possible to this logic family. A target rise and fall time of 400ps has therefore been chosen as this speed is comparable to speeds obtained with ECL 100K standard components. The buffer circuits cannot be identical, however, as constraints are imposed by the requirement that they be compatible with other pad macros to be included in a standard cell library.

As it is desired to include the final layouts in a standard cell library, the supply voltages and bus connections restrict the placement of layout instances. The number of CMOS

Figure 3.1: f_T vs. I_{CS} for 2x, 4x, 2-4x, 15x, 30x, and 45x Transistors

logic gates on a BiCMOS wafer is usually far in excess of the number of logic gate comprised of bipolar transistors. This is true because CMOS transistors consume almost no static power compared with bipolar transistors. To ensure CMOS compatibility, the power buses are therefore supplied at +5V and ground: standard CMOS voltages. The layout area available for each buffer is restricted by the location of supply buses and by the desirability that the pad openings be placed in a standard location. The available area for layout is shown in Figure 3.2 which indicates that the height of each buffer must be restricted to 585.4 μ m. The minimum width, on the other hand, is constrained by the minimum pitch distance between the pad openings. The width can be made arbitrarily large, however.

Figure 3.2: Layout of Power Buses

3.2 Design of an ECL 100K Compatible Output Buffer

The standard ECL output buffer interfaces on-chip ECL voltage signals and drives large off-chip capacitive loads. The circuit topology is similar to the basic ECL OR/NOR gate described in Chapter 2: a differential amplifier is supplied by a constant current source which is controlled by a band-gap reference. An additional compensation network has been added in order to produce circuit characteristics similar to the 100K logic family. In this way the output voltage has been made insensitive to variations in temperature and supply voltage.

3.2.1 Output Buffer Circuit

A schematic of the output driver is shown in Figure 3.3. The design process is straightforward because speed is inversely proportional to input power if the transit frequency

(f_T) of the switching transistors is adequate for the proposed operating frequency. In initial computer simulations, appropriate transistor sizes must be estimated and appropriate models selected. For example, it is necessary to use a large transistor for the emitter follower, $Q4$, as this transistor must be capable of carrying an emitter current of about 21mA during a logic high state.

Figure 3.3: Fully Compensated Output Driver

A logic low level of -1.705V (assuming $V_{CC} = 0\text{V}$) is maintained during initial simulations by varying the current source and changing the load resistors, $R1$ and $R2$. The cross-coupled network of $D1$, $D2$, and $R3$ is for temperature compensation and mod-

elling these elements is not necessary for initial simulations. Simulations show that if I_{CS} is set to 6mA, enough drive will be provided to ensure a nominal rise/fall time of 400ps.

With the switching current determined, the final circuit is established by completing additional computer simulations. An important part of this task is to choose optimum transistor sizes such that f_T is maximized for the specific collector current. Optimum transistors are chosen by noting f_T from Figure 3.1. Transistor sizes for $Q1$ and $Q2$ are chosen such that the emitters are 15 times greater (15x), and output transistor $Q4$ is chosen to be 45 times greater (45x), than the emitter size of the smallest available transistor.

When the output is V_{OL} the circuit automatically compensates for changes in temperature. Because V_{BE} of a bipolar transistor decreases at a rate of about $-1.5\text{mV}/^\circ\text{C}$, the current produced by the current source increases with increased temperature. This results in a larger voltage drop across $R2$ which compensates for the decrease in V_{BE} of $Q4$. The output therefore remains stable.

The cross-coupled network comprised of $D1$, $D2$, and $R3$ is necessary to provide temperature compensation when the output is V_{OH} [Mull72]. Without compensation, the output voltage increases with increased temperature due to the change in V_{BE} of the output transistor, $Q4$. The compensation network, however, lowers the base voltage of $Q4$ by a similar amount to maintain constant output voltage. If the temperature rises, the current through $R1$ increases due to the lower V_{BE} of the the current source transistor, $Q3$. The voltage drop across this resistor falls at a nominal rate of $-1.5\text{mV}/^\circ\text{C}$. In addition, the voltage drop across $D1$ also falls but at a nominal rate

of only $-0.5\text{mV}/^\circ\text{C}$. This results in a net decrease of $-2.0\text{mV}/^\circ\text{C}$ across the series combination of $R2$ and $R3$. In order to compensate for the approximate $-1.5\text{mV}/^\circ\text{C}$ voltage change in V_{BE} of $Q4$, the voltage is distributed by the voltage divider of $R2$ and $R3$. $R2$ is three times the value of $R3$ so that 75% of the node voltage is seen at the base of $Q4$.

In other literature, the value of the temperature compensation resistor $R3$ is equal to that of $R1$ and $R2$ [Fair91, Moto88]. In the buffer design, however, this resistance is three times less than the load resistance to produce an adequate temperature sensitive voltage at the base of $Q4$. Implementing a smaller resistor is necessary because the voltage across $D1$ decreases at a rate of about $-0.5\text{mV}/^\circ\text{C}$, as opposed to the expected value of $-1.5\text{mV}/^\circ\text{C}$. This decreased temperature sensitivity can be explained from Figure 3.4, which shows a typical graph of diode current vs. voltage for two temperatures.

Figure 3.4: Diode Current vs. V_{BE}

If diode current is maintained constant, V_{BE} will be temperature dependent at the usual rate of about $-1.5\text{mV}/^\circ\text{C}$. This is shown in Figure 3.4 as the operating point moves from point A to point B with rising temperature. However, the current through diode $D1$ increases due to the increased source current and the operating point moves to

point B' . In this manner, the rate of change in diode voltage is reduced to only $-0.5\text{mV}/^\circ\text{C}$. The series combination of the voltage drop across $R1$ and $D1$ requires an appropriate choice for the value of $R3$ to maintain a constant output.

Small transistors can be used to implement the cross-coupled network diodes because they affect the steady-state output and are not involved in current switching. Hence, maximizing f_T is not a concern. Because currents of less than 1mA flow in this branch, the smallest available transistors are used to minimize the parasitic capacitances between the transistor nodes.

3.2.2 Band-gap Reference for Output Buffer

The band-gap reference circuit of Figure 3.5 has been designed to supply the current source of the differential amplifier. HSPICE simulations show that the output voltage has a temperature sensitivity of $TC_F = +19\text{ppm}/^\circ\text{C}$. Over the temperature range of 0°C to 85°C , the maximum change in the nominal voltage is only 0.002mV . The results shown in Figure 3.6 can be obtained by using the OPTIMIZE feature of HSPICE[Meta90].

When the band-gap circuit of Figure 3.5 is connected to the output driver of Figure 3.3, the output voltage remains stable for changes in ambient temperature and supply voltage.

Figure 3.5: Band-gap Voltage Source for Output Driver

Figure 3.6: Output Driver Band-gap Voltage vs. Temperature

3.2.3 Layout of Output Buffer

A layout for the output buffer is shown in Figure 3.7. The pad has been laid out using the available BiCMOS process and has been designed for inclusion in a standard cell library which includes CMOS and TTL drivers.

The output driver is supplied from a set of power buses which is separate from that used to supply internal logic gates. As can be seen from the layout, the buses labelled *vddring!* and *gndring!* supply the buffer which reduces the phenomena of ground bounce. When large currents switch, an induced voltage is seen in the parasitic inductance of the micro-wires connected to the pads. By keeping the supplies to the I/O buffers separate, internal logic is isolated from these transients.

Electrostatic discharge (ESD) protection has been implemented by connecting discharge diodes from the pads to the supplies. The diodes are connected to the pad openings as shown in the schematic of Figure 3.8(a). Their implementation is shown in the simplified process cross-section of Figure 3.8(b) and a close up of the diode layout is also shown in Figure 3.9. A current limiting resistor is not connected in series with the diodes as its inclusion increases the delay unacceptably. To provide as much protection as possible within these limitations a guard ring therefore encircles the large emitter follower transistor *Q4*. Guard rings have also been laid out around each of the circuits' transistors and most of the resistors.

One of the most difficult devices to manufacture within tight tolerances is the integrated resistor. The difference between the extracted resistance obtained from the models and the actual resistance within the wafer may be greater than 10%. This is clearly a concern when constructing ECL circuits. For example, if *R4* of Figure 3.3 has

an actual resistance 10% higher than its desired value of 70Ω , then I_{CS} can be expected to decrease by a proportional amount. If the output is low, and $R2$ is kept constant at 156Ω , V_{OL} will rise due to the reduced voltage drop across $R2$.

The key to producing reliable circuits is to ensure that resistor values scale proportionally for process variations. This can be done by constructing each resistor as parallel and series combinations of one standard resistor size. Figure 3.10 demonstrates this technique as it shows the resistor layout for $R2$ of the output driver. Six resistor tiles, each with a value of 931Ω , are placed in parallel to comprise a total resistance of 155Ω . V_{OL} is made invariant for changes in nominal resistance due to this layout technique. For example, if $R4$ is 10% higher than expected, then $R2$ should rise by a similar 10% because it is adjacently located on the same wafer. In a similar manner, if $R2$ and $R3$ are constructed from standard resistor sizes, then temperature compensation will remain adequate. Buffer delay times, are of course affected by the shifted switching current.

Figure 3.7: Output Buffer Layout

(a) Connection of Discharge Diodes to Pad Openings

(b) Process Implementation of Discharge Diodes

Figure 3.8: Circuit ESD Protection

Figure 3.9: Layout of ESD Diodes

Figure 3.10: Layout of Resistor Tiles

3.2.4 Simulation Results

The transient response of the extracted output driver layout is shown in Figure 3.11 for a negligible load capacitance connected across the 50Ω resistor. HSPICE simulations indicate that with input signals having a rise time of 80ps, the circuit has a nominal output rise time of 389ps and a propagation delay of 136ps. For these conditions the circuit can operate at a frequency up to 1GHz. As can be observed from the plot, a distinguishing feature of the simulation is the peaked response during a high to low transition.

Figure 3.11: Transient Response for Output Driver

The sensitivity of the transfer characteristics of the output buffer to variations in temperature and supply voltage is shown in Figure 3.12. Additionally, Figure 3.13 shows the dependence of the delays on output capacitance (C_L).

Figure 3.12: Temperature (a) and Voltage (b) Sensitivity of Output Driver

Figure 3.13: Output Rise Time (a) and Propagation Delay τ_D (b) vs. C_L

3.3 Capacitive Feedthrough and C_{JC} Compensation in Switching Circuits

The voltage spikes seen in Figure 3.11 are caused by capacitive feedthrough as current is induced in the collector junction capacitance as a result of abrupt voltage changes at each transistor base. Peaking is due to capacitive feedthrough as Q_2 switches on and this is illustrated in Figure 3.14. This figure shows that the parasitic base-collector capacitance, C_{JC} , and the load resistor, R_2 , comprise an RC circuit. When the input voltage at the base of Q_2 is abruptly raised, a current is induced in the collector junction capacitance. The current through R_2 is then seen as a voltage spike at the output. Clearly, if a current of equal magnitude with a phase displacement of 180° is supplied to the collector of each switching transistor, the reverse transmission through C_{JC} can be reduced[Mata68].

Figure 3.14: Capacitive Feedthrough Producing Voltage Peaking at the Collector Node

In the balanced differential stage used for the input and output buffers seen in Figure 3.15(a), the ac voltages at the collectors of $Q1$ and $Q2$ have the same amplitude but differ in phase by 180° . By connecting capacitors of value C_{JC} from each switching transistor collector to the base of the opposing transistor, it is possible to neutralize capacitive feedthrough. To produce a neutralizing current, the scheme requires that C_1 and C_2 have capacitance values equal to C_{JC} of the transistors. In monolithic circuits, this can be done by connecting similarly sized transistors as shown in Figure 3.15(b).

Connecting additional capacitance to the switching circuit, of course, reduces circuit speed and this can be noted from the HSPICE simulation of Figure 3.16. With C_{JC} compensation, voltage spiking is eliminated at the expense of circuit speed.

Figure 3.15: (a) Output Driver with C_c Compensation and (b) Actual Transistor Implementation

Figure 3.16: Transfer Function Showing Effect of C_c Compensation

3.4 Operation of Output Buffer at Low Voltage

As previously explained, the output voltage of the band-gap reference is dependent on a ratio of currents. This is advantageous for low voltage operation. HSPICE simulations of the output driver band-gap reference indicate that a temperature stable voltage of 1.151V can be supplied if V_{EE} is reduced to -2.3V. This is shown graphically in Figure 3.17.

A consideration of the output driver transfer function shows that for HSPICE models, -2.3V is the minimum supply voltage before the dc transfer function is affected and the circuit can no longer operate with the reduced supply. For typical HSPICE models, V_{CS} in the band-gap reference drops from 1.273V to 1.151V and it is necessary to decrease the current resistance ($R4$) from 70 Ω to 50 Ω to increase the current and obtain the same switching speed. This is shown in Figure 3.18. The output driver supply is limited to -2.3V before $Q3$ moves from the active region towards saturation. Simulations show that V_{CE} of $Q3$ changes from 2.63V to 0.55V as V_{EE} changes from -4.5V to -2.3V.

Figure 3.17: Output Buffer Band-gap Voltage (a) vs. Temperature for $V_{EE} = -4.5V$ and $-2.3V$ and (b) vs. V_{EE} for $T = 25^\circ C$

Figure 3.18: Output Buffer Transfer Function for Different Values of V_{EE} and R_{CS}

A comparison of the power dissipation of the output buffer with the normal and minimum supply voltages shows the power savings. A breakdown of the power consumption is given in Table 3.1.

circuit	$V_{EE} = -4.5V$ $R_{CS} = 70\Omega$	$V_{EE} = -2.3V$ $R_{CS} = 50\Omega$
band-gap reference power:	4.2mW	1.2mW
current switch power:	27.2mW	13.8mW
emitter follower power: V_{out} HIGH	11.7mW	11.8mW
V_{out} LOW	43.1mW	43.2mW
total: V_{out} HIGH	43.1mW	26.8mW
V_{out} LOW	74.5mW	58.2mW

Table 3.1: Output Buffer Power Consumption at Normal and Low Voltage

As can be seen from the table, most of the power reduction comes from the current switch portion of the buffer. HSPICE simulations show that only 6% of this power dif-

ference occurs due to the lowering of R_{CS} . 94% of the improvement comes from the reduced power consumption of $Q3$ due to its lower collector-emitter voltage V_{CE} .

3.5 Design of an ECL 100K Compatible Input Buffer

The standard ECL input buffer interfaces off-chip ECL signals to drive on-chip logic and consists of a differential amplifier supplied by a constant current source. The current source is controlled by a band-gap reference which also supplies a constant voltage to the base of a reference transistor. Similar to the output buffer described in Section 3.2, the input buffer is compatible with the 100K logic family.

3.5.1 Input Buffer Circuit

The design process for the input buffer is similar to that described for the output buffer. The input driver circuit is shown in Figure 3.19. As the input driver is configured for single ended input, a constant voltage of about $-1.3V$ with respect to V_{CC} must be supplied to the base of the reference transistor $Q2$.

Figure 3.19: Fully Compensated Input Driver

3.5.2 Band-gap Reference for Input Buffer

The band-gap reference circuit of Figure 3.20 has been designed to supply both the reference transistor of the differential amplifier and the current source. HSPICE simulations show that the temperature sensitivity of the reference voltage and current source voltage are $+93\text{ppm}/^{\circ}\text{C}$ and $-84\text{ppm}/^{\circ}\text{C}$ respectively. The temperature sensitivities are larger than the value obtained for the band-gap reference of the output driver previously described. When using the OPTIMIZE feature of HSPICE the TC_F

of V_{BB} and V_{CS} move in opposing directions and a compromise must therefore be made if $R1$ and $R3$ are to have the same resistance values. The band-gap output voltages are shown as a function of temperature in Figure 3.21.

Figure 3.20: Band-gap Voltage Source for Input Driver

Figure 3.21: Input Buffer Band-gap Voltage vs. Temperature

3.5.3 Layout of Input Buffer

A layout of the input buffer is shown in Figure 3.22. The layout is similar to that previously described for the output buffer as power is supplied by buses of the same pitch. In this way both the input and output buffers can be placed adjacent to each other on the periphery of the wafer. As with the output pad macro, ESD protection is provided by back-to-back diodes and by guard rings.

Figure 3.22: Input Buffer Layout

3.5.4 Simulation Results

The transient response of the extracted input driver layout is shown in Figure 3.23 for a small capacitive load (0.1pF).

Figure 3.23: Transient Response for Input Driver

HSPICE simulations show that with an input rise time of 80ps, the circuit has a nominal output rise time of 294ps and a propagation delay of 147ps. The circuit can operate at a frequency of up to 1GHz. The sensitivity of the input buffer transfer characteristics to variations in temperature and supply voltage is shown in Figure 3.24. In addition, Figure 3.25 shows the dependence of output capacitance (C_L) on the output rise time and propagation delay (τ_D).

Figure 3.24: Temperature (a) and Voltage (b) Sensitivity of Input Driver

Figure 3.25: Output Rise Time (a) and Propagation Delay (b) vs. C_L

3.6 Operation of Input Buffer at Low Voltage

HSPICE simulations of the input driver show that -3.0V is the minimum permissible voltage before the circuit fails to produce equal complementary outputs for high and low inputs. Upon a cursory examination of the schematic, this value is shown to be close to the expected limit assuming that the output voltages are maintained near their original values. Assuming a minimum voltage of 0.3V for V_{CE} of Q_3 , summation of nominal values of V_{BB} and V_{CS} yields 2.9V which can be noted from Figure 3.26.

Figure 3.26: Voltage Limitation of Input Driver Band-gap Reference

The effect of reduced supply voltage on the input buffer transfer function is shown in Figure 3.27. As is the case for the output buffer, R_{CS} must be decreased to obtain the same switching current because V_{CS} is lower. Although for supply voltages greater than $-3.0V$, adequate dc characteristics can be obtained by changing the resistance values of R_L and R_{CS} , the desired transient characteristics cannot be met. Circuit ac performance is degraded as $Q3$ is saturated for low V_{IN} .

A tabulation of the power savings due to the reduced supply voltage is given in Table 3.2. As before, less power is consumed by the differential pair as an improvement comes from the reduced power consumption of $Q3$ due to its lower collector-emitter voltage V_{CE} . For this buffer, however, additional savings are realized from the emitter followers as power is reduced here with the square of the applied voltage.

Figure 3.27: Input Buffer Transfer Function for Different Values of V_{EE} and R_{CS}

circuit	$V_{EE} = -4.5V$ $R_{CS} = 180\Omega$	$V_{EE} = -3.0V$ $R_{CS} = 143\Omega$
band-gap reference power:	4.2mW	2.1mW
current switch power:	9.4mW	6.5mW
emitter follower power:	14.4mW	5.1mW
total:	28.0mW	13.7mW

Table 3.2: Input Buffer Power Consumption at Normal and Low Voltage

3.7 Summary

This chapter has described the complete methodology for the design and layout of standard output and input buffers. The available BiCMOS process has been used to design circuits with output rise times less than 400ps. In addition to the differential amplifier which is the heart of both buffer circuits, a method has been implemented to compensate the output signal for variations in temperature and supply voltage. Buffer schematics and layouts have been given and the extracted dc transfer and tran-

sient characterizations have been presented. The ability of the buffers to operate with reduced voltage has also been analyzed and absolute voltage limits have been given. In order to reduce power consumption, while maintaining the same circuit speed, the minimum supply voltage of the output buffer is recommended to be -2.3V . Similarly, the minimum supply voltage for the input buffer is recommended to be -3.0V . A technique for reducing voltage spiking in the transient response of the buffers has also been described. This technique involves connecting cross-coupled capacitors between the base and the collector of adjacent transistors.

Chapter 4

Classical Analysis of I/O Buffers

In order to determine the parameters of an I/O buffer which limit speed, a delay expression can be derived which is the sum of circuit RC time constants. The resulting equation can then be examined to show the contribution to delay from each of the constant terms. This technique is applied to the standard output and input buffers which are described in the previous chapter. Predicting optimum load resistance, and hence current, can also be investigated with the derived equations.

4.1 Obtaining a Delay Expression

It is seen in the literature that the propagation delay (τ_D) of bipolar circuits can be written as the sum of RC time constants each weighted by a factor determined by the circuit topology[Chor88, Fang90]. The derivation of such an expression is possible because propagation delay is a linear function of resistance and capacitance if the changes in these values are kept small. For example, each transistor of the output buf-

Figure 4.1: HSPICE Transistor Model

Figure 4.2: Propagation Delay vs. Capacitance/Resistance of 15x Transistors

–fer described in the previous chapter has been modelled with the HSPICE equivalent circuit of Figure 4.1 [Getr84, Meta90]. The delay changes linearly when values of resistance and capacitance are increased by multiples of their original values. This can be seen from Figure 4.2 as each delay plot is obtained by changing the HSPICE model parameters (cjc , cjs , rb , rc , re , cje) while keeping the other model parameters constant. The multiplying factor shown on the horizontal axis of the figure indicates the multiple that the resistance or capacitance model parameter was increased by to obtain each value of propagation delay.

Figure 4.3: Output Buffer

For the ECL output buffer shown in Figure 4.3, Equation 4.1 gives the propagation delay from the contribution of the 15x transistors as well as from $R_L C_L$. Whereas similar derivations in the literature have assumed equal transistor sizes for the switching and emitter follower transistors, a complete delay expression may be obtained by find-

ing the contribution from the 45x emitter follower transistor as well as the 1x cross-coupled diodes.

$$\begin{aligned}
 \tau_D = & K_{01}\tau_{F,15x} + K_{02}\tau_{R,15x} \\
 & + R_{B,15x}(K_{03}C_{JC,15x} + K_{04}C_{JE,15x} + K_{05}C_{JS,15x} + K_{06}C_{DE,15x} + K_{07}C_{DC,15x}) \\
 & + R_{C,15x}(K_{08}C_{JC,15x} + K_{09}C_{JE,15x} + K_{10}C_{JS,15x} + K_{11}C_{DE,15x} + K_{12}C_{DC,15x}) \\
 & + R_{E,15x}(K_{13}C_{JC,15x} + K_{14}C_{JE,15x} + K_{15}C_{JS,15x} + K_{16}C_{DE,15x} + K_{17}C_{DC,15x}) \\
 & + R_L(K_{18}C_{JC,15x} + K_{19}C_{JE,15x} + K_{20}C_{JS,15x} + K_{21}C_{DE,15x} + K_{22}C_{DC,15x}) \\
 & + \dots \text{similar terms for 1x cross-coupled diodes} \\
 & + \dots \text{similar terms for 45x emitter-follower transistor} \\
 & + \dots \text{other RC time constants between transistors of different sizes} \\
 & + K_{xx}R_L C_L
 \end{aligned} \tag{4.1}$$

In Equation 4.1, R_B is the combined intrinsic and extrinsic base resistance; R_C and R_E are the collector and emitter parasitic resistances respectively; C_{JE} is the depletion capacitance of the base-emitter junction; C_{JS} is the collector-substrate capacitance; C_L is the load capacitance; C_{DC} is the diffusion capacitance of the base-collector junction; and C_{DE} is the diffusion capacitance of the base-emitter junction.

From a preliminary examination of the expression, it is evident that insignificant time constants can be discarded. For example, the delay contribution from the reverse transit time constant τ_R and from the collector-base diffusion capacitance C_{DC} can be neglected because the base-collector junction is never reverse biased in the ECL buffer. Also, the $R_L C_{DE}$ term is redundant because $C_{DE} = \tau_F/R_L$ for the output buffer and $C_{DE} = 2\tau_F/R_L$ for the input buffer[Chor88]. Appendix C shows how these terms are derived from the small-signal circuit of the differential pair.

The emitter follower resistance (R_{EF}) is negligibly small and is not included in the expression. This can be explained by noting that the output resistance of the emitter fol-

lower is low, $\approx R_L/(1 + \beta_F)$, and the total output impedance is not significantly altered when the 50Ω resistance is connected in parallel.

4.2 Derivation of Constants in Delay Expression

The weighting factors of each term in Equation 4.1 can be determined by sensitivity analysis using the HSPICE circuit simulator[Meta90]. An input voltage having a rise time of 80ps is applied in each simulation and the propagation delay is obtained by observing the waveform at the output pad. As usual, propagation delay is measured between the 50% transition points from input to output.

The K constants can be determined by taking partial derivatives of Equation 4.1 to obtain each K as a function of circuit parameters. For example, to obtain K_{I0} for the 15x transistors, applying second partial derivatives to both sides of the equation yields:

$$\frac{\partial^2 \tau_D}{\partial R_C \partial C_{JS}} = 0 + \dots + K_{I0} + 0 + \dots + 0 \quad (4.2)$$

This can be rearranged to obtain:

$$K_{I0} = \frac{\partial}{\partial C_{JS}} \left[\frac{\partial \tau_D}{\partial R_C} \right] \quad (4.3)$$

Hence, the value of K_{I0} can be determined by observing the rate of change of τ_D vs. R_C for values of C_{JS} increased by multiples designated as the capacitance multiplying factor. The HSPICE model for the 15x transistors, in this case, is changed which impacts on all the 15x transistors in the buffer ($Q1$ and $Q2$). Figure 4.4 shows how the slope of each τ_D vs. R_C plot increases as the C_{JS} capacitance is increased. The measured slopes can then be plotted as a function of C_{JS} as in Figure 4.5. The slope of this graph gives the value of K_{I0} . All the K values can be derived in this manner with the exception

of the $R_L C_{DE}$ constant. $C_{DE} = \tau_F / R_L$ for the output buffer and, therefore, K_{01} and K_{21} must be completed jointly. This is necessary because τ_F is common to both expressions.

Figure 4.4: τ_D vs. R_C for Different Values of C_{JS}

Figure 4.5: Slope of $\{\tau_D$ vs. R_C for Different Values of $C_{JS}\}$ vs. C_{JS}

The above technique is different than that described in the literature. Fang has described a method whereby R_C is increased from R_{C1} to R_{C2} at $C_{JS} = C_{JS1}$ to obtain a difference in delay τ_{D1} [Fang90]. The same simulation program is then run at a higher collector-substrate capacitance $C_{JS} = C_{JS2}$ to obtain a second delay τ_{D2} . By subtracting the two delays, K_{10} can be approximated as:

$$\begin{aligned}
 K_{10} &= \frac{\Delta\tau_{D2} - \Delta\tau_{D1}}{(R_{C2} - R_{C1})(C_{JS2} - C_{JS1})} \\
 &= \frac{\Delta(\Delta\tau_D)}{\Delta R_C \Delta C_{JS}} \approx \frac{\partial^2 \tau_D}{\partial R_C \partial C_{JS}} \quad (4.4)
 \end{aligned}$$

An advantage of the technique described by Fang is that only four simulations are required to determine each K factor. The values chosen for R_i and C_i are, however, critical for determining each value of K . These must be selected in such a way that the change in propagation delay ($\Delta\tau_D$) is large enough to eliminate any unwanted mathe-

mathematical error. In addition the circuit must continue to operate near its original operating point. In practice, this is not realizable when second order effects are modelled with HSPICE. Whereas Fang reports to have successfully derived the circuit constants using this technique, his modelling ignored the decrease in β_F at high and low current densities, the effect of intrinsic base-resistance decrease at high and low current densities, the effect of intrinsic base resistance decrease at high collector current density, the Early effect, and the Kirk effect. If these second order effects are accounted for in the simulation model, the Fang technique does not produce definite K values as these depend on the chosen capacitance values. For example, as depletion layer recombination, basewidth modulation, and high-level injection are accounted for in the Gummel-Poon models of HSPICE, the resultant value of K_{I0} changes depending on the chosen parameters of Equation 4.4. This is shown graphically in Figure 4.6. With R_{C2} being 2 times, 4 times, and 6 times the actual value, and C_{JS2} ranging to 40 times its original value, K_{I0} is shown to vary between 1.2 and 1.4. This ambiguity is avoided by using the technique of partial derivatives. With this method, a definitive value of $K_{I0} = 1.25$ is determined at the expense of more computation time.

Figure 4.6: Range of K_{I0} Determined by Fang Technique

4.3 Propagation Delay Expression for Output Buffer

The K constants of Equation 4.1 have been determined and the non-zero values are listed in Table 4.1. From this table it can be seen that the predicted propagation delay is 6% less than that computed by direct HSPICE simulation. When the derived expressions are used to predict delay for the same circuit with different switching transistors and load resistors, the predicted and HSPICE derived delays are listed in Table 4.2. The worst case error is 15.2% which compares with an average error of 7.2%.

The parameters of the circuit which contribute most to delay include R_L , $C_{JC,45x}$, $C_{JS,15x}$, $C_{JC,15x}$, and $\tau_{F,45x}$. The base-collector and collector-substrate junction capacitances of the 45x and 15x transistors affect the speed of the buffer the most. Clearly, faster circuits can be developed by lowering these process capacitances as they contribute about 60% of the total delay.

From the derived expression it is clear that there is an optimum value of R_L to achieve minimum propagation delay. If the value of R_L is lower than this value then not only will the power consumption increase but the propagation delay will suffer. By setting $\partial\tau_D/\partial R_L = 0$ the optimum value of R_L can be estimated. This expression is given by Equation 4.5 which predicts a load resistance of 23 Ω whereas the optimum value of R_L determined from direct HSPICE simulation is 38 Ω . This discrepancy is shown in Figure 4.7, where the HSPICE derived propagation delay is plotted against load resistance. Determining the optimum R_L in this way is shown only to provide a resistance which is of the same order as that of the HSPICE predicted value. This difference in accuracy suggests that the equation is accurate for small perturbations about an origi-

n..l operating point. Accuracy suffers, however, when circuit parameters are chosen which significantly differ from those of the original values.

$$R_{L,OPT} = \sqrt{\frac{1.16R_{B,15x} \times \tau_{F,15x}}{0.48C_{JC,45x} + 0.92C_{JS,15x} + 0.53C_{JC,15x} + 2.86C_{JE,1x} + 0.05C_{JE,45x} + 0.61C_{JS,1x}}} \quad (4.5)$$

term	K value	delay	% of total delay
$R_L \times C_{JC,45x}$	0.48	41.17ps	32.2%
$R_L \times C_{JS,15x}$	0.92	21.33ps	16.7%
$\tau_{F,45x}$	1.78	17.01ps	13.3%
$R_L \times C_{JC,15x}$	0.53	15.16ps	11.9%
$R_L \times C_{JE,1x}$	2.86	6.73ps	5.3%
$\tau_{F,15x}$	0.58	5.54ps	4.3%
$R_L \times C_{JE,45x}$	0.05	5.17ps	4.0%
$R_L \times C_{JS,1x}$	0.61	4.33ps	3.4%
$R_{C,45x} \times C_{JC,45x}$	1.54	2.18ps	1.7%
$R_{B,15x} \times \tau_{F,15x} / R_L$	1.16	2.02ps	1.6%
$R_{B,45x} \times C_{JC,45x}$	0.21	1.62ps	1.3%
$R_{C,15x} \times C_{JC,15x}$	1.13	1.60ps	1.3%
$R_{C,15x} \times C_{JS,15x}$	1.25	1.44ps	1.1%
$R_{B,45x} \times C_{JC,15x}$	0.21	0.54ps	0.4%
$R_{B,15x} \times C_{JE,15x}$	0.08	0.50ps	0.4%
$\tau_{F,1x}$	0.04	0.50ps	0.4%
$R_{B,45x} \times C_{JE,45x}$	0.04	0.37ps	0.3%
$R_{C,1x} \times C_{JC,15x}$	0.01	0.20ps	0.2%
$R_L \times C_L$	0.01	0.16ps	0.1%
$R_{B,45x} \times C_{JE,15x}$	0.04	0.12ps	0.1%
$R_{E,45x} \times C_{JE,45x}$	0.31	0.08ps	0.1%
Totals = >		128ps	100%
HSPICE = >		136ps	

Table 4.1: Derived K Constants for Output Driver

I_{CS}	R_L	switching transistor size	predicted delay	HSPICE delay	difference
2mA	466 Ω	4x	259ps	305ps	-15.2%
2mA	466 Ω	15x	313ps	356ps	-11.9%
4mA	233 Ω	15x	174ps	188ps	-7.6%
6mA	156 Ω	15x	128ps	136ps	-6.0%
8mA	116 Ω	15x	105ps	109ps	-4.5%
10mA	93 Ω	15x	91ps	96ps	-4.6%
10mA	93 Ω	30x	111ps	110ps	-0.6%

Table 4.2: Predicted Delay Compared to HSPICE

Figure 4.7: Propagation Delay vs. R_L for Output Buffer

4.4 Propagation Delay Expression for Input Buffer

The K constants have also been derived for the input buffer shown in Figure 3.19. Similar to the output buffer, R_L is the resistance connected to the collectors of the switching transistors ($Q1$ and $Q2$) and C_L is the load capacitance connected across each of the emitter follower resistors. The circuit topology used to derive the constants is different from that used for the output buffer, however. Because the input pad macro requires

only a single input signal, the circuits can be connected in a chain to account for the high-to-low and low-to-high transitions. Such a scheme is shown in Figure 4.8.

Figure 4.8: Delay Chain For Input Driver

The delay time is measured from the input of buffer 2 to the output of buffer 3. By measuring the delay between these points, both the rise and fall times are accounted for and the average propagation delay may be considered to be half their sum. The K values derived in this manner are listed in Table 4.3. It can be seen from this table that R_L and the circuit junction capacitances of the 4x transistors contribute the most to delay. As for the output buffer, if the process junction capacitances can be reduced the circuit can operate faster.

As previously described, the resistor size which minimizes propagation delay can be determined by setting $\partial \tau_D / \partial R_L = 0$. Solving for R_L , the resulting expression is given in Equation 4.6.

$$R_{L,OPT} = \sqrt{\frac{2.98R_{0,A6} \times \tau_{FA6}}{5.60C_{JE,A6} + 2.31C_{JC,A6} + 1.69C_{JS,A6} + 1.61C_{JS,L6}}} \quad (4.6)$$

term	K value	delay	% of total delay
$R_L \times C_{JE,4x}$	5.60	110.76ps	31.9%
$R_L \times C_{JC,4x}$	2.31	67.92ps	19.6%
$R_L \times C_{JS,4x}$	1.69	57.25ps	16.5%
$\tau_{F,4x}$	4.10	45.63ps	13.1%
$R_L \times C_{JS,1x}$	1.61	31.84ps	9.2%
$R_{B,4x} \times C_{JE,4x}$	1.61	8.32ps	2.4%
$R_{C,4x} \times C_{JC,4x}$	3.79	7.39ps	2.1%
$R_{B,4x} \times \tau_{F,4x} / R_L$	2.98	6.67ps	1.9%
$R_{B,4x} \times C_{JC,4x}$	0.87	5.14ps	1.5%
$R_{C,4x} \times C_{JS,4x}$	1.90	4.27ps	1.2%
$R_{E,4x} \times C_{JE,4x}$	3.24	0.85ps	0.2%
$R_{E,4x} \times C_{JC,4x}$	1.50	0.45ps	0.1%
$R_{D,4x} \times C_{JS,4x}$	0.04	0.27ps	0.1%
$\tau_{F,1x}$	0.02	0.25ps	0.1%
$R_{B,1x} \times C_{JS,1x}$	0.01	0.15ps	0.0%
$R_{E,1x} \times C_{JS,1x}$	0.04	0.06ps	0.0%
Totals = >		347ps	100%
HSPICE = >		330ps	

Table 4.3: Derived K Constants for Input Driver

The predicted value of 65Ω compares with an HSPICE derived optimum resistance of 245Ω . Clearly, a value of optimum resistance cannot be predicted with high accuracy in this manner. The circuit with the optimum R_L is significantly changed from the operating conditions used to develop the original equation.

4.5 Summary

In order to determine the circuit parameters which affect the speed of I/O buffers, the standard output and input circuits have been analyzed using RC sensitivity analysis. Expressions for delay have thus been determined. A technique used to find the coefficients for each RC circuit combination has been described which differs from that previously presented in technical journals. Although the new method requires more computation time, high accuracy of the final equations may be obtained. The predicted

delays of the buffers have been shown to be within 6% of the values obtained from HSPICE. The parameters which limit speed the most are the transistor base-collector and collector-substrate junction capacitances. Using the equations to predict optimum load resistance is not recommended, however, as the circuit with optimum R_L is significantly altered from the conditions used to derive the original expression.

Chapter 5

Macromodeling and Optimization of I/O Buffers

A macromodeling approach for timing simulation is presented in this chapter. Precise polynomial expressions for delay and output rise and fall times are developed for use in a circuit simulator. Finally, it is shown how the equations can be used to optimize buffers in order to produce the fastest circuits within given constraints.

5.1 Macromodeling Overview and Design Space Definition

In integrated circuit design, the traditional attributes of interest include circuit power, layout area, and propagation delay. Each of these can be optimized if the input voltage transit time and load capacitance are known. The circuit of Figure 5.1 is used to consider this problem in the context of an output buffer.

Figure 5.1: Buffer Circuit With Independent Parameters for Optimization

The three parameters of Figure 5.1 which determine circuit performance are input voltage rise and fall time (τ_{IN}), switching current (I_{CS}), and load capacitance (C_L). In addition, the size of the switching transistors $Q1$ and $Q2$ can be chosen from standard transistors which are available in the BiCMOS process. The emitter-follower ($Q3$) transistor size is fixed at 45x, which is the size most suited for its expected collector current of up to 21mA when the output is high.

In order to optimize the circuit of Figure 5.1, a reasonable range of variables is chosen to bound the design space suitable for high-speed ECL I/O. The limits in Table 5.1 are therefore imposed.

	minimum	maximum
input voltage rise and fall time (τ_{IN})	50ps	2050ps
switching current (I_{CS})	0.5mA	21.0mA
load capacitance (C_L)	1pF	101pF
switching transistor sizes: 2x, 4x, 2-4x*, 15x, 30x, 45x		

* two 4x transistors in parallel

Table 5.1: Output Buffer Design Space

Timing simulations can be completed at intervals spanning the design space and this data may be curve fitted to determine closed form polynomial expressions. The resulting equations can be used in a circuit simulator as they predict steady-state operating characteristics and transit times. Furthermore, because the equations are linear, they may be used to optimize the buffer with respect to power, layout area, and propagation delay.

5.2 Effect of Process Variations

Production process variations significantly alter the expected transit times of I/O buffers. This can be seen from Figure 5.2 which shows this effect on a typical plot of delay vs. switching current for the set of transistor models. For a given switching current, I_{CS} , the maximum delay is always obtained with the worst model parameters. Hence, if a maximum delay time is specified, and it is desirable to find the switching current necessary to guarantee a delay time which is less, the minimum I_{CS} is found based on simulations with the worst models. The shaded area of the figure shows the range of I_{CS} which will ensure the delay time is less than the specified maximum.

The value of R_L , necessary to obtain a desired $V_{LOW} = -1.7V$, is dependent on transistor process variations because of the change in V_{BE} of $Q3$. R_L is therefore obtained with typical models by keeping the base voltage of $Q3$ fixed. A unique value of R_L thus corresponds to each discrete value of I_{CS} .

Figure 5.2: Effect of Process Variations on Delay

5.3 Collection of Empirical Data

The propagation delay and output rise and fall times are obtained by completing HSPICE simulations covering the design space. The buffer is designed to operate with V_{LOW} fixed at the standard ECL voltage of $-1.7V$. This is obtained by a judicious selection of load resistance and switching current. For a given I_{CS} , R_L is adjusted such that the base voltage of $Q3$ results in the desired V_{LOW} .

The nominal value of V_{HI} is $-0.9V$ but this value changes depending on the value of load resistance. $Q2$ is cut-off during the high output state and the base current of $Q3$ is thus determined by R_L . As $V_{CE,Q3}$ is a function of this base current, V_{HI} may vary by about $\pm 0.2V$ from nominal which results in a shift of the output signals. This must be accounted for when measuring propagation delays and transit times.

As usual, propagation delay is defined as the time between the 50% points of input and output voltages. Output rise and fall time is defined as the time for the output voltage to move from 10% to 90% of its full range.

To derive the delays over the complete design space, a program written in C calls upon three HSPICE decks to ultimately produce a data file which contains complete dc transfer and transient analysis information for each simulation. For the reasons stated in the previous section, R_L is found using typical transistor models and V_{HI} and the transient times are found using the worst HSPICE transistor models. The program flow is shown in Figure 5.3.

Figure 5.3: Program Flow for Obtaining Propagation Delay and Rise Times

The parameters which make up the design space are increased in regular increments to produce data. For example, the input rise and fall time is varied in 100ps steps from 50ps to 2050ps. Similarly, the switching current is varied from 0.5mA to 21.0mA in 0.5mA steps. The load capacitance, conversely, is incremented with two step sizes in order to capture a drop in output rise and fall time for load capacitances less than about 13pF. This characteristic is evident in Figure 3.13(a). To capture this part of the curve, the load capacitance is incremented in 2pF steps up to 13pF, and then in larger 8pF steps to a maximum of 101pF. The total number of HSPICE simulations is thus 15,876 for each of the switching transistor sizes. Simulations are run with each chosen

transistor size for $Q1$ and $Q2$ to obtain a complete set of data suitable for optimization. The following information is thus obtained for each simulation (.mt0 file in Figure 5.3):

- 1) switching current, I_{CS} (mA)
- 2) input voltage rise and fall time, τ_{IN} (ps)
- 3) load capacitance, C_L (pF)
- 4) differential pair load resistance, R_L (Ω)
- 5) high output voltage, V_{HI} (V)
- 6) propagation delay for V_{IN} rising, T_{PLH} (ps)
- 7) propagation delay for V_{IN} falling, T_{PHL} (ps)
- 8) output voltage rise time, T_R (ps)
- 9) output voltage fall time, T_F (ps)

5.4 Typical Simulation Data

A snapshot of derived data is shown in Figure 5.4 and Figure 5.5. For the 15x switching transistor the average propagation delay and average rise and fall time are shown as a function of two variables while keeping the third variable fixed. Although the program flow of Figure 5.3 is used to derive data over the complete design space with worst case transistor models, the illustrative plots are obtained with typical models by varying the three parameters in regular increments to obtain properly scaled graphs. The data has been shown for typical models because worst case simulation results are proprietary to Northern Telecom. As can be seen from the plots, propagation delay and output rise and fall time vary linearly with respect to output capacitance and parabolically with respect to switching current. The rise time of the input voltage is shown to have the least effect on the measured values, although this is more pronounced with small switching currents.

Figure 5.4: Dependence of Average Propagation Delay on I_{CS} , τ_{IN} , and C_L with 15x Typical Switching Transistors

(a) Delay as a Function of I_{CS} and τ_{IN} with $C_L = 20\text{pF}$

(b) Delay as a Function of I_{CS} and C_L with $\tau_{IN} = 500\text{ps}$

(c) Delay as a Function of τ_{IN} and C_L with $I_{CS} = 6\text{mA}$

Figure 5.5: Dependence of Average Output Rise and Fall Time on I_{CS} , τ_{IN} and C_L with 15x Typical Switching Transistors

- (a) Rise and Fall Time as a Function of I_{CS} and τ_{IN} with $C_L = 20\text{pF}$
- (b) Rise and Fall Time as a Function of I_{CS} and C_L with $\tau_{IN} = 500\text{ps}$
- (c) Rise and Fall Time as a Function of τ_{IN} and C_L with $I_{CS} = 6\text{mA}$

5.5 Curve Fitting

A program, based largely on an algorithm described by Shum, generates the model equations from the data[ShLe92]. The objective of curve fitting is to derive an accurate polynomial expression. In doing so, it is desirable that the expression contain a minimum number of terms in order to minimize the time taken to evaluate the expression. As well, an equation with fewer terms can be stored in a more compact data file to be used by a circuit simulator or optimizer. Obviously, more accuracy can be obtained by increasing the number of polynomial terms. It is desirable, therefore, to find a polynomial with a sufficient number of terms such that adding additional terms only negligibly increases the accuracy beyond the level which is desired.

5.5.1 Program Overview

Figure 5.6 shows a block diagram for the C program which curve fits HSPICE data. The program executes to produce final polynomial expressions by accepting initial polynomials from separate files. Terms of each initial polynomial can then be reduced until an equation with a desired accuracy is obtained (accuracy refers to the closeness of the curve fit to the actual data). In the program a polynomial of seven terms is used to curve fit the parameters R_L and V_{HI} and an initial polynomial of 216 terms is used to curve fit the remaining delay parameters. The R_L and V_{HI} variables are only dependent on I_{CS} and their equation takes the form of Equation 5.1.

$$R_L \text{ or } V_{HI} = a_0 + \frac{a_1}{I_{CS}} + \frac{a_2}{I_{CS}^2} + \frac{a_3}{I_{CS}^3} + a_4 I_{CS} + a_5 I_{CS}^2 + a_6 I_{CS}^3 \quad (5.1)$$

No term reduction is done from this initial equation as the polynomial is already sufficiently small. The initial polynomial used to express the delay parameters is larger, however, and is a function of three variables: I_{CS} , τ_{IN} , and C_L . Each term in this equa-

tion takes the form: $a_{xx} I_{CS}^{exp} \tau_{IN}^{exp} C_L^{exp}$, where the exponents for each of the parameters vary as $-1, -\frac{1}{2}, 0, \frac{1}{2}, 1$, and 2 . This initial polynomial thus has $6^3 = 216$ terms which describe the propagation delay and output rise and fall times.

Figure 5.6: Overview of Curve Fitting Program

The data to be fitted, initial polynomials, and the minimum required accuracy are provided to a C program. An algorithm, similar to that described by Shum, is then used to reduce the polynomial to a desired accuracy[ShLe92]. The final output equations and related data are subsequently written to separate output files.

Accuracy is defined within the program as being the percentage of predicted values which fall within a specified percent difference of data obtained from simulation. This gives a quantitative measure of the normal distribution of predicted data. In the program the percentage difference has been specified to be 5.5%. 100% accuracy then means that all of the predicted datapoints are within 5.5% of those obtained from HSPICE.

The algorithm used to determine the final polynomial equation is shown in Figure 5.7. Whereas Shum's algorithm allowed for "bounding back" if removing a term caused the change in accuracy to decrease below a specified minimum, the algorithm de-

scribed here does not include this capability. In this case, the initial polynomial contains 216 terms as opposed to the 22 term equation that Shum has described. The computation time necessary to remove and test subsequent terms, once the accuracy drops below a specified minimum, is excessive if a large number of initial terms is specified. Furthermore, simulation has shown that if removing a term causes the change in accuracy to drop below a specified minimum, it is unlikely that removing other terms will significantly improve the curve fitting results.

```

Input:      P = an initial polynomial; A = a matrix of simulation data
              TARGET_ACCURACY = required percentage of accuracy for final
              polynomial
Output:    P_OUT = a simplified polynomial; X_OUT = term coefficients of P_OUT

Begin
  X = curve fit data to determine term coefficients of P {Least mean square fit};
  ACC = accuracy of P;
  i = least important term in P;
  flag = TRUE;
  if ( ACC < TARGET_ACCURACY ) then
    flag = FALSE;
    X_OUT = X;
    P_OUT = P;
  end if
  while ( flag = TRUE )
    i = term in P with the least importance;
    P = P with i removed;
    X = run curve fitting to determine coefficients of P {Least mean square fit};
    ACC = accuracy of P;
    if ( ACC > TARGET_ACCURACY )
      P_OUT = P;
      X_OUT = X;
    else
      flag = FALSE;
    end if
  end while
  return P_OUT, X_OUT;
End

```

Figure 5.7: Curve Fitting Algorithm

A commercial collection of subroutines has been supplied by IMSL and these have been used to solve the curve fitting algorithm[IMSL91]. The subroutines use a method of least squares to obtain the a_{α} constants of each term, defined as $a_{\alpha} I_{CS}^{\exp} \tau_{IN}^{\exp} C_L^{\exp}$. Although the terms are not linear, the values of $I_{CS}^{\exp} \tau_{IN}^{\exp} C_L^{\exp}$ are calculated as discrete values which allows for linear mathematical techniques. The basic problem, therefore, is to minimize $\|\Phi \vec{a} - \vec{b}\|_2$, where $\vec{a}$ is the vector of term constants each of the form a_{α} , $\vec{b}$ is the vector of HSPICE data points, and Φ is an $m \times n$ matrix which contains the calculated values of $I_{CS}^{\exp} \tau_{IN}^{\exp} C_L^{\exp}$. The curve fitting subroutine recursively uses Householder's transformation to produce the QR factorization of the given Φ matrix. A least squares fit is then performed using the factorized matrices by solving a set of linear equations to obtain the minimum. The complete details of the procedure are adequately described elsewhere and will not be presented in this thesis [GoVL89, ShLe92].

To increase the accuracy of the curve fit, the Φ matrix is first normalized with $\vec{b}$ such that $\vec{b}$ is transformed into an array of 1's. This also facilitates accuracy checking of the resultant polynomial as the terms in each row should add to 1. The data is further conditioned by varying the rows and columns of Φ such that the smaller elements are placed in the top left hand corner of the array. This is necessary because the Householder reduction is performed starting from the last row which has consequences for rounding errors in large matrices [Wilk65].

5.5.2 Obtaining the Polynomial Expressions

As previously described, the polynomial expression for R_L and V_{HI} contains seven terms. Although each of these equations meets the defined accuracy of 100%, closer examination reveals that each curve fitted point precisely matches that of HSPICE. This is to say that all the predicted points are equivalent to the data obtained from HSPICE simulation. The dependence of R_L and V_{HI} as a function of current is illustrated in Figure 5.8, where these values are shown as a function of I_{CS} in an output buffer configured with 15x sized switching transistors.

To ensure precise curve fitting of propagation delay and transit time information, an accuracy of 98% is selected such that 98% of the predicted values from each equation fall within 5.5% of the data derived with HSPICE. Terms in each equation are subsequently reduced until removing an additional term causes the accuracy to fall below 98%. The polynomial with the least number of terms with this accuracy is then written to the output file.

Figure 5.8: Load Resistance (a) and High Output Voltage (b) vs. Switching Current for 15x Transistors

The results of reducing the 216 term polynomial are shown in Table 5.2 and Table 5.3. Table 5.2 shows the accuracy of curve fitting the delay variables with the initial 216 term polynomial and Table 5.3 indicates how many terms are required in each expression in order to obtain 98% accuracy.

switching transistor size	T_{PLH}	T_{PHL}	T_R	T_F
2x*	100.00%	99.96%	100.00%	98.61%
4x	100.00%	99.83%	100.00%	98.68%
2-4x	100.00%	100.00%	100.00%	100.00%
15x	100.00%	100.00%	100.00%	100.00%
30x	100.00%	99.95%	100.00%	100.00%
45x	99.91%	99.91%	100.00%	99.99%

*current is limited to 11mA for simulations with 2x transistors

Table 5.2: Full 216 Term Accuracy

Q size	terms in final equation			
	T_{PLH}	T_{PHL}	T_R	T_F
2x*	130	98	97	185
4x	117	116	98	186
2-4x	27	78	39	85
15x	13	90	40	84
30x	48	87	49	108
45x	51	83	71	131

*current is limited to 11mA for simulations with 2x transistors

Table 5.3: Number of Polynomial Terms Required for 98% Accuracy

The values predicted with the derived equations can be compared with the original datapoints to observe how precisely the data has been fitted. The distribution of error gives a measure of this which can be observed by viewing error histograms. One such distribution is shown in Figure 5.9, which shows graphs for each of the derived delay equations for an output buffer comprised of 15x switching transistors. The error is shown to be normally distributed, which is a requirement for the best curve fitting re-

Figure 5.9: Error Histograms for 15x Transistors (a) T_{PLH}
 (b) T_{PHL}
 (c) T_R
 (d) T_F

sults. It is shown that most of the predicted values fall within 1.5% of the HSPICE data, although a few terms fall well beyond the desired accuracy of 5.5%. These terms have been found to correspond to datapoints obtained with circuit parameters unlikely to

be physically realized – for example, minimum switching current and maximum load capacitance. If desired, the results could be improved by removing the outlying points before rerunning the curve fitting algorithm.

The original 216 term equation has been reduced to 98% accuracy with a reduction in the number of terms. If less terms are desired at the expense of decreased accuracy, however, the polynomial can be further reduced. For example, the accuracy with reduced terms for T_F with 4x transistors is shown in Figure 5.10(a). Histograms have been shown for this example because the data obtained with the 4x switching transistors is the hardest to curve fit. This is evident from Table 5.3 as this case requires the most terms to meet the target accuracy. From Figure 5.10(a) it is evident that a large number of terms are required to ensure reasonable accuracy – at least 118 terms are required to ensure that 90% of the predicted datapoints fall within 5.5% of those predicted with HSPICE.

Figure 5.10: Polynomial Reduction for T_F with 4x Transistors Indicating (a) Accuracy, and (b) Sum of the Squares of Residual Errors

It is evident from Figure 5.10(a) that for equations of about twenty terms, removing additional terms can cause the accuracy to increase. This apparent anomaly arises due to the chosen definition for accuracy. Even though accuracy may increase, the total residual error monotonically increases when removing terms. This can be seen from Figure 5.10(b), which plots the sum of the squares of residual error for equations with six or more terms. If accuracy increases with an equation of fewer terms, then the predicted datapoints beyond the defined range (5.5% in this case) must have larger residual errors.

5.6 Optimization With Derived Equations

Optimization of circuit power, layout area, and delay can be considered with the derived equations. Specifying a maximum load capacitance, C_{Lmax} , and maximum input voltage rise time, τ_{INmax} , the types of optimization for consideration include:

- $$\left. \begin{array}{l} 1) \text{ minimize } P \text{ subject to } \begin{array}{l} D \leq D_{max} \\ A \leq A_{max} \end{array} \\ 2) \text{ minimize } A \text{ subject to } \begin{array}{l} P \leq P_{max} \\ D \leq D_{max} \end{array} \\ 3) \text{ minimize } D \text{ subject to } \begin{array}{l} P \leq P_{max} \\ A \leq A_{max} \end{array} \end{array} \right\} \begin{array}{l} \text{given} \\ C_L \leq C_{Lmax} \\ \tau_{IN} \leq \tau_{INmax} \end{array}$$

where P = circuit power (mW)

A = layout area (μm^2)

D = output voltage rise and fall time (T_R , T_F , $T_{average}$) or propagation delay (T_{PLH} , T_{PHL} , $T_{Paverage}$) (ps)

Of the above variables of circuit power (P), layout area (A), and delay (D) a quantitative expression can be derived for P and D using techniques of simulation and curve fitting. Obtaining such an expression for A is difficult, however, because much of the buffer layout area consists of resistor tiles. As previously described, resistors are con-

structured of tiles in order to minimize the effect of process variations. A single resistor value must therefore be chosen such that the current source resistor and load resistors can each be constructed from a series and parallel combination. As it is desired to keep the total number of tiles to a minimum, the value of tile resistance must be carefully chosen to meet these constraints. Determining the best resistance value is not trivial and requires iteration.

As a result of the absence of a quantitative expression for layout area, minimizing power or delay for a given maximum layout area cannot be considered. This does not, however, detract from the ability to minimize layout area for constraints of power and delay. This problem is trivial as area increases monotonically for increasing switching currents. Layout area of the switching transistors increases as larger transistors must be selected to dissipate increased power and to satisfy f_T requirements. Of the transistor sizes listed in Table 5.1, only the total area of the 2–4x transistors in parallel is not intuitive because of the necessary interconnection between them. These two transistors in parallel are, however, sized smaller than that of a single 15x transistor. The layout area for each of the transistors is shown in Figure 5.11.

Figure 5.11: Transistor Layout Area

Other layout considerations include metal layer wire widths which must be increased for larger currents. As well, thermal limitations restrict the size of resistor layouts. For a larger current, resistor size must be increased to maintain a constant minimum power dissipation necessary to prevent fusing. As layout area increases with increased power consumption, the problem of optimization is considerably simplified. An optimization problem in three variables is thus reduced to one in two dimensions.

5.6.1 Program Overview

Figure 5.12 shows a block diagram for the optimizing program which uses the equations derived from the curve fitting procedure. Polynomial expressions are provided to a C program which runs within a MATLAB frame. MATLAB is an engineering software tool which readily allows for the manipulation and graphing of matrix data[PROM89]. Given two of the three independent variables in a delay expression, the value of $f(I_{CS}, \tau_{IN}, C_L)$ can be plotted as a function of the third variable and the given transistor switching size. R_L and V_{HI} can also be plotted as a function of I_{CS} .

Figure 5.12: Overview of Optimization and Plotting Program

One of the inherent advantages of creating equations for the data is that polynomial expressions can readily be used to find the remaining unknown. As an example, the program provides complete dc transfer and transient characteristics when I_{CS} , τ_{IN} , and C_L are input. Conversely, one of I_{CS} , τ_{IN} , or C_L can be obtained if the value of $f(I_{CS}, \tau_{IN}, C_L)$ is given. The method used to find the roots of the polynomial in this case is Muller's Method which is called upon by a subroutine of IMSL[CSdC72, IMSL91, PGTP73].

The expressions can be manipulated in the above manner to develop an optimized output buffer. Power can be minimized subject to a minimum required delay and load capacitance. Conversely, the delay can be minimized subject to a maximum power limitation and load capacitance. For optimization, it is necessary to apply a constraint which limits the collector current through each transistor. High-current effects are avoided by limiting I_{CS} to a level less than that which results in f_{Tmax} . Figure 3.1, which

plots f_T vs. I_C for each transistor size, is used to obtain the maximum currents and these are listed in Table 5.4.

Q size	current for f_{Tmax}
2x	1.1mA
4x	1.8mA
2-4x	4.0mA
15x	5.7mA
30x	11.3mA
45x	15.1mA

Table 5.4: Maximum Transistor Collector Current

The output buffer is optimized by finding the unknown variable of current or delay with each transistor size. Because optimizing current is the same as optimizing power, the program uses current as a parameter. Current can be considered synonymous with power because the supply voltage is fixed. The optimizing procedure is therefore straightforward and can be explained from Figure 5.12.

The average propagation delay is obtained from the transient times derived from both a rising and falling input voltage. In the example from Figure 5.13, its dependence on switching current is shown for $C_L = 20\text{pF}$ and $\tau_{IN} = 100\text{ps}$. If it is desirable to minimize delay, the program calculates all the delays for the maximum current provided to the program. The transistor size that gives the minimum delay, within current constraints, is chosen as optimum. From this, R_L and V_{HI} are then obtained to characterize the optimum circuit. In a similar manner the minimum switching current can be obtained if the maximum delay is input.

Figure 5.13: Average Propagation Delay vs. I_{CS} and Design Space Transistor Sizes from (a) 0mA to 21mA and (b) 1mA to 7mA ($C_L = 20\text{pF}$; $\tau_{IN} = 100\text{ps}$)

5.7 Summary

The development of macromodels for a standard output buffer has been described in this chapter. Although accurate timing information can be extracted from the models, of equal significance is the fact that the equations can be used for optimization. The basic procedure is to complete HSPICE simulations which cover the design space defined as input voltage, switching current, and load capacitance. A method of curve fitting has then been described which uses matrix techniques to curve fit data to a specified accuracy. Finally, a method for optimization has been illustrated which accounts for delay, power, and layout area. Because layout area is shown to monotonically increase for increased power the optimization problem has been shown to be reduced to one in two dimensions. Hence, only current, synonymous with power, and delay need be considered. A computer program and numerical techniques have been described which predict the optimum values given a set of boundary conditions.

Chapter 6

Non-Standard ECL I/O Circuits

In order to produce fast I/O buffers, circuits which differ from the standard topologies can be examined. In particular, two output buffer circuits are investigated which have the potential to significantly reduce delay time.

6.1 External Pull-Up I/O Buffer

In order to increase the switching speed of I/O buffers, it is necessary to reduce the parasitic capacitances and resistances. From the analysis of the output buffer presented in Chapter 4, it is evident that about 50% of the delay can be attributed to the emitter-follower circuit. If this stage is eliminated, the buffer will operate with increased speed. Such a circuit is shown in Figure 6.1(a) where external 50Ω pull-up resistors are connected to the collectors of the switching transistors. The output signal is taken as the voltage difference between the pads. Because there is no level shifting, V_{HI} is at ground and V_{LOW} is determined by the voltage drop across the external resistor. This circuit topology has been demonstrated to be useful as a buffer for both a 2:1 and 4:1 multiplexer (MUX) where the bit rate is as high as 2.5Gbit/sec[Rein88].

The buffer interfaces standard on-chip ECL logic with off-chip systems which do not have standard ECL voltages. For this topology, this is desirable as the standard input voltages ensure that the transistors remain active. By ensuring that V_{IN} and $\overline{V_{IN}}$ remain at least 1 diode drop below ground, the transistor emitter voltages are fixed to at least $2 V_{BE}$ volts below ground. The transistors will remain active if the collector voltages are kept about 0.3V above this.

Figure 6.1: 50Ω Pull-Up Resistor Circuit (a) and Band-gap Reference (b)

The buffer of Figure 6.1(a) may be controlled by the band-gap reference of Figure 6.1(b). This circuit is comprised of the same band-gap circuit which is used to control the output driver described in Chapter 3. To provide adequate temperature compensation, however, an additional transistor (Q5) is connected as a diode and this is placed in series with the band-gap circuit. The voltage of V_{CS} is thus increased by one diode drop to a nominal value of 2.1V with respect to V_{EE} . As the temperature increases, V_{BE} of Q3 in Figure 6.1(a) decreases but this is compensated by a reduction in V_{CS} . The output voltage of the band-gap reference circuit is reduced by a similar amount because $V_{BE,Q5}$ also falls. The switching current is thus maintained constant and V_{LOW} remains unaffected by variations in temperature. The dc transfer character-

istics for the buffer are given in Figure 6.2. This figure shows the output voltage stability for variation in temperature and supply voltage.

Figure 6.2: Temperature (a) and Voltage (b) Sensitivity of 50Ω Pull-Up Driver

If a 0.8V voltage swing is maintained, the switching current will be 16mA. Now, if the same 45x transistors are used, the circuit can be compared with the standard circuit consisting of an emitter-follower connected to the standard load of 50Ω. The new circuit is shown with HSPICE to have an average output rise time of 121ps and an average propagation delay of 51ps. The standard output driver, without cross-coupled temperature compensation diodes, on the other hand, is shown to have an average output rise time of 266ps and an average propagation delay of 84ps. In addition to this speed improvement, the 50Ω pull-up buffer consumes less power because power need not be supplied to an emitter-follower.

Circuit speed can further be improved by decreasing ΔV of the output. The output voltage swing can be reduced to a minimum of about 0.4V. Voltages lower than this do not have adequate margin for signal noise and process and temperature variations.

2 of/de 2

MICROCOPY RESOLUTION TEST CHART
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STANDARD REFERENCE MATERIAL 1010a
(ANSI and ISO TEST CHART No. 2)

low output voltage (V_{LOW}) is compensated for variations in temperature. The increased current due to the decrease in $V_{BE,Q3}$ results in a greater voltage drop across the 50Ω resistor. This compensates for the decreased voltage across $D3$. The high output voltage (V_{HI}) is compensated by the cross-coupled diode network.

Diodes placed in series with the base of the switching transistors are required for this circuit. These lower the signal of the input voltages in order to maintain the transistors in the active region. Resistors $R4$ and $R5$ are required to form a voltage divider to shunt the base charge of the differential pair transistor when the input goes low. As can be seen from Figure 6.4, if the diodes are removed from the circuit, the output voltage increases beyond the level that is required for low V_{IN} . This circuit has an average output rise time of 224ps and an average propagation delay of 120ps for input signals having a rise time of 80ps. This is faster than the standard output driver of the previous chapter but not as fast as the circuit of Figure 6.1.

Figure 6.4: Effect of Series Input Diodes on DC Transfer Characteristics

6.3 Summary

Output buffers have been presented which eliminate the emitter-follower stage in order to minimize delay. The circuits connect off-chip resistors directly to the collectors of the switching transistors to produce output signals with non-standard and standard ECL voltages. Techniques to compensate the output voltage for variations in temperature and supply voltage have been described.

Chapter 7

Conclusions and Recommendations for Future Research

7.1 Summary

This thesis has examined fast interface circuits for BiCMOS integrated systems. The foundation for the study was laid by describing principles of ECL circuit operation. Implementation of the basic ECL NOR/OR gate was explained as this circuit forms the basic building block from which buffer circuits can be designed. The band-gap reference circuit has been described as an auxiliary circuit necessary for ECL design. Principles to produce a practical temperature insensitive voltage source have been shown. As well, the importance of maximizing the transistor transit frequency (f_T) has been discussed with a view towards producing reliable and fast circuits.

Basic principles were applied to produce standard ECL I/O buffers using a $0.8\mu\text{m}$ BiCMOS process. Each of the buffers was designed so that the nominal output rise time is less than 400ps. The buffers are compatible with the 100K ECL commercial series with the desirable attributes that the output voltage is insensitive to temperature and supply voltage variations. The standard buffers have been designed for temperatures between 0°C and 85°C and a supply voltage between -4.2V and -5.2V . Simulation results and the complete dc transfer and timing characterization of the buffers have been presented. As well, layouts have been provided with remarks on the design techniques necessary to produce realizable circuits that correspond to the mathematically modeled one.

An analysis of the buffers was then completed using classical sensitivity analysis in order to determine the circuit parameters which most affect circuit speed. Delay expres-

sions were thus determined as a sum of each RC time constant. It has been shown that the coefficients of each term can be derived by applying sensitivity analysis using simulation. In doing so, an approach to the problem has been described which differs from that previously explained in journals. Although the technique requires more computation time, the method has been shown to produce accurate results while accounting for circuit second order effects. Propagation delays have been successfully predicted using this technique to within 6% of those predicted with HSPICE. Not as accurate, however, is the value of optimum load resistance predicted with the same equation. Although analysis of the output buffer predicted an optimum resistance of 23Ω , the optimum HSPICE predicted resistance was 38Ω . Analysis of the input buffer, on the other hand, resulted in values of 65Ω and 245Ω respectively. The delay expressions have been shown to be inadequate for predicting optimum resistance as the circuit characteristics are changed from those used to derive the original expressions.

Much of the work in this thesis involved deriving macromodels for an output buffer. The models are suitable for inclusion in a circuit simulator and they can also be used for optimization. More precise modeling is desired than that obtained with RC sensitivity analysis. A technique has thus been described where computer simulations are completed covering a design space suitable for optimization of high-speed ECL I/O. A technique of curve fitting which uses matrix techniques to obtain closed form polynomial expressions has been described. The number of terms in the delay equations can be reduced to a level of defined accuracy.

With the derived equations, a method to optimize delay, power, and layout area was discussed. A method to determine layout area within constraints of power and delay is not trivial as the basic resistor tile must be chosen such that buffer resistors can be made up of a series and parallel combination of this. Furthermore, because layout

area was shown to monotonically increase with greater circuit power consumption the optimizing problem was simplified. Optimizing became a problem in only two dimensions.

Finally, non-standard ECL circuits have been presented. Output buffers are described which eliminate the emitter-follower and require external 50Ω pull-up resistors connected to the collectors of the differential pair transistors. These circuits have been shown to be about 50% faster than the standard I/O circuits.

7.2 Accomplishments

A study has been done to produce fast ECL buffers suitable for interfacing BiCMOS systems. Beginning with a complete review of standard circuit techniques and topologies, these same principles have been applied to macromodeling and optimization. This is significant as circuit techniques which were once only applicable for bipolar integrated circuits may find new areas of application in BiCMOS processes. The techniques described in this thesis can be directly applied to this technology.

7.3 Recommendations for Future Research

There are many opportunities to continue the work described in this thesis. Although the basic circuits for ECL have been used successfully for many years, the principles can be applied to other buffers which interface different logic families. Specifically, circuits to interface TTL-ECL and CMOS-ECL logic families could be investigated.

Further work can also be done to refine the macromodeling technique. A contribution could be made if an expression could be developed to express layout area as a function of transistor size and resistor tiles. New algorithms could also be developed to reduce the number of polynomial terms in each delay equation in order to provide the same accuracy in a simplified expression. Conversely, a new approach, whereby the delay

is approximated by a piecewise linear function, could be studied. This has potential to reduce the amount of information ultimately stored to represent the data. Of much greater interest, however, may be to expand upon the presented macromodeling techniques by including the models in a comprehensive logic and timing simulator. The full potential of the macromodeling approach would then be realized.

Appendix A

Band-gap Reference Voltage Derivation

This appendix shows the derivation for the band-gap output voltage of Figure 2.5.

From the figure, it is evident that the output voltage is equal to the base-emitter voltage of $Q3$ plus the voltage drop across $R2$. Hence:

$$V_{ref} = V_{BE,Q3} + V_2 \quad (A.1)$$

The collector current in a transistor can be approximated by the diode equation which gives the current through the device as a function of base-emitter voltage. Assuming that the collector voltage and base voltage are equal:

$$I_C = I_o \left(e^{\frac{V_{BE}}{V_T}} - 1 \right) \quad (A.2)$$

Manipulating this equation to obtain V_{BE} as a dependent variable yields:

$$\ln\left(\frac{I_C}{I_o}\right) = \frac{V_{BE}}{V_T} - \ln(1) \quad (A.3)$$

$$V_{BE} = V_T \ln\left(\frac{I_C}{I_o}\right) \quad (A.4)$$

Now, the voltage across $R3$ is equal to the difference between the base-emitter voltage of $Q1$ and the base-emitter voltage of $Q2$. As $\beta \gg 1$, this is represented as:

$$I_2 R_3 = V_{BE,Q1} - V_{BE,Q2} \quad (A.5)$$

The collector currents from the low-current biasing transistors $Q1$ and $Q2$ can now be substituted into the above equation to obtain:

$$I_2 R_3 = V_T \ln \left(\frac{I_1}{I_2} \right) \quad (\text{A.6})$$

Equation A.6 can be substituted into the following:

$$V_2 = \frac{R_2}{R_3} (I_2 R_3) \quad (\text{A.7})$$

to yield:

$$V_2 = V_T \frac{R_2}{R_3} \ln \left(\frac{I_1}{I_2} \right) \quad (\text{A.8})$$

Finally, equation A.8 can be substituted into equation A.1 to obtain the output voltage:

$$V_{ref} = V_{BE,Q3} + V_T \frac{R_2}{R_3} \ln \left(\frac{I_1}{I_2} \right) \quad (\text{A.9})$$

Appendix B

Temperature and Voltage Sensitivity Parameter for Band-gap Reference Circuits

This appendix describes a figure of merit to quantify the temperature and voltage sensitivity of a band-gap voltage source.

The temperature sensitivity of the output voltage, at a specific voltage, can be expressed in units of parts-per-million per degree Celsius (ppm/°C) as:

$$TC = \frac{1}{V} \frac{\partial V}{\partial T} \quad (\text{B.1})$$

As the parameter of interest in reference sources is the variation in output voltage encountered over the entire temperature range, an effective TC_F can be defined as:

$$TC_F = \frac{1}{V_{nom}} \left(\frac{V_{max} - V_{min}}{T_{max} - T_{min}} \right) \quad (\text{B.2})$$

where the minimum and maximum output voltages and ambient temperatures are specified and V_{nom} is the nominal voltage.

The same form of equations B.1 and B.2 can be used to quantify the output sensitivity to changes in supply voltage. In this case, $V_{EEmax} - V_{EEmin}$ can be substituted for the temperature difference of $T_{max} - T_{min}$. This parameter is often referred to as the Power Supply Rejection Ratio (PSRR).

Appendix C

Derivation of C_{DE} for Buffer Circuits

This appendix describes the derivation for the base-emitter diffusion capacitance, C_{DE} , for the input buffer. A similar method can be used to determine C_{DE} for the output buffer.

The small-signal model for the input buffer differential pair is shown in Figure C.1. The base of the reference transistor is grounded because it is supplied by a constant dc source (V_{ref}).

Figure C.1: Small-Signal Equivalent Circuit for Input Buffer

Now, the base-emitter diffusion capacitance is defined as the rate of change of injected charge with respect to the base-emitter voltage:

$$C_{DE} = \frac{dQ_{DE}}{dV_{BE}} \quad (C.1)$$

dQ_{DE} can be approximated as the collector current (i_c) multiplied by the forward transit time (τ_F) and dV_{BE} is v_2 from Figure C.1. Hence:

$$C_{DE} = \frac{\tau_F i_c}{v_2} \quad (C.2)$$

From Figure C.1:

$$i_c = g_m v_2 = \frac{-v_{O2}}{R_L} \quad (C.3)$$

and assuming R_{EE} is large,

$$v_2 = \frac{-v_{IN}}{2} \quad (C.4)$$

Substituting C.3 and C.4 into C.2, one obtains:

$$C_{DE} = \tau_F \left[\frac{2 v_{O2}}{R_L v_{IN}} \right] \quad (C.5)$$

v_{O2} equals v_{IN} as the output voltage follows the input voltage. The input buffer base-emitter diffusion capacitance is therefore:

$$C_{DE} = \frac{2 \tau_F}{R_L} \quad (C.6)$$

For the output buffer: $C_{DE} = \frac{\tau_F}{R_L}$. This is derived in a similar fashion assuming a small-signal source connected to the base of both transistors.

References

- [Chor88] Chor, E.F. *et al.*, "A Propagation-Delay Expression and its Application to the Optimization of Polysilicon Emitter ECL Processes", *IEEE Journal of Solid-State Circuits*, Vol. 23, No. 1, pp. 251-259, February 1988.
- [Chua92] Chuang, C.T. *et al.*, "On the Leverage of High- f_T Transistors for Advanced High-Speed Bipolar Circuits", *IEEE Journal of Solid-State Circuits*, Vol. 27, No. 2, pp. 225-228, February 1992.
- [CSdC72] Conte, S.D., de Boor, C., *Elementary Numerical Analysis: An Algorithmic Approach*, McGraw-Hill Book Company, Second Edition, 1972.
- [Elma83] Elmasry, M., *Digital Bipolar Integrated Circuits*, John Wiley & Sons, Inc., 1983.
- [Fair95] Fairchild Camera and Instrument Corporation, *F100K ECL User's Handbook*, 1985.
- [Fang90] Fang, W., "Accurate Analytical Delay Expressions for ECL and CML Circuits and Their Applications to Optimizing High-Speed Bipolar Circuits", *IEEE Journal of Solid-State Circuits*, Vol. 25, No. 2, pp. 572-583, April 1990.
- [Getr84] Getreau, I.E., *Modeling the Bipolar Transistor*, Amsterdam: Elsevier, 1984.
- [GoVL89] Golub, G., Van Loan, C., *Matrix Computations*, Second Edition, The John Hopkins University Press, 1989.
- [Greb84] Grebene, A., *Bipolar and MOS Analog Integrated Circuit Design*, John Wiley & Sons Inc., 1984.
- [Hada91] Hadaway, R. *et al.*, "A Sub-Micron BiCMOS Process for Telecommunication Circuits", *Proceedings of 21st European Solid-State Device Research Conference, ESSDERC '91*, Lausanne, September 1991.
- [Herb85] Herbst, L.J., *Monolithic Integrated Circuits*, Oxford University Press, 1985.
- [IMSL91] *IMSL Math/Library User's Manual*, IMSL Inc., 1991.
- [Kirk62] Kirk, C.T. Jr., "A Theory of Transistor Cutoff Frequency (f_T) Falloff at High Current Densities", *IRE Transactions on Electron Devices*, Vol. ED-9, pp. 164-174, 1962.

- [Mata68] Mataya, J.A. *et al.*, "I-F Amplifier Using C_C -Compensated Transistors", *IEEE Journal of Solid-State Circuits*, Vol. SC-3, pp. 410-407, December 1968.
- [Meta90] Meta-Software Inc., *HSPICE User's Manual H9001*, 1990.
- [Mill79] Millman, J., *Microelectronics: Digital and Analog Circuits and Systems*, McGraw Hill Inc., 1979.
- [Moto88] Motorola Semiconductor Products Inc., *MECL System Design Handbook*, Fourth Edition, 1988.
- [Moto91] Motorola Semiconductor Products Inc., *ECLinPS Data*, 1991.
- [Mull72] Muller, H.H. *et al.*, "Fully Compensated Emitter-Coupled Logic: Eliminating the Drawbacks of Conventional ECL", *IEEE Journal of Solid-State Circuits*, Vol. SC-8, No. 5, pp. 362-367, October 1972.
- [PGTP73] Phillips, G.M., Taylor, P., *Theory and Applications of Numerical Analysis*, Academic Press (London) Inc., 1973.
- [PROM89] *PRO-MATLAB User's Guide*, The MathWorks Inc., 1989.
- [Rein83] Rein, H.M., "Proper Choice of the Measuring Frequency for Determining f_T of Bipolar Transistors", *Solid-State Electronics*, Vol. 26, No. 1, pp. 75-82, 1983.
- [Rein87] Rein, H.M. "A Compact Physical Large-Signal Model for High-Speed Bipolar Transistors at High Current Densities- Part II: Two-Dimensional Model and Experimental Results", *IEEE Transactions on Electron Devices*, Vol. ED-34, No. 8, pp. 1752-1761, August 1987.
- [Rein88] Rein, H.M., "Multi-Gigabit-Per-Second Silicon Bipolar IC's for Future Optical-Fiber Transmission Systems", *IEEE Journal of Solid-State Circuits*, Vol. 23, No. 3, pp. 664-675, June 1988.
- [ShLe92] Shum, R.S., Lefebvre, M.C., "An Empirical Timing Characterization Method and its Application to CMOS Logic Circuits", *Proceedings of Canadian Conference on Very Large Scale Integration (CCVLSI)*, October 1992.
- [Stub87] Stubing, H., Rein, H.M., "A Compact Physical Large-Signal Model for High-Speed Bipolar Transistors at High Current Densities- Part I One-Dimensional Model", *IEEE Transactions on Electron Devices*, Vol. ED-34, No. 8, pp. 1741-1751, August 1987.

- [TaSc77] Taub, S., Schilling, D., *Digital Integrated Electronics*, McGraw-Hill Inc., 1977.
- [Widl71] Widlar, R., "New Developments in IC Voltage Regulators", *IEEE Journal of Solid-State Circuits*, Vol. SC-6, No. 1, pp. 2-7, February 1971.
- [Wilk65] Wilkinson, J.H., *The Algebraic Eigenvalue Problem*, Oxford University Press, 1965.
- [Wilk71] Wilkinson, J.H., Reinsch, C., *Linear Algebra*, Springer-Verlag Berlin, 1971.

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