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**Pseudomorphic Silicon/Germanium
Superlattices in MOS Capacitors towards
Sub-Surface Channel Heterostructure
p-type MOSFETs**

by

BRENT RONALD CYCA. B.Sc.(Hons.), M.Sc.

A thesis submitted to
the Faculty of Graduate Studies and Research
in partial fulfillment of
the requirements of the degree of

Master of Engineering

Department of Electronics

Ottawa- Carleton Institute for Electrical Engineering

Carleton University

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**"Pseudomorphic Silicon/Germanium Superlattices in MOS Capacitors
towards Sub-Surface Channel Heterostructure p-type MOSFETs"**

submitted by

Brent Ronald Cyca. B.Sc.(Hons.), M.Sc.

in partial fulfillment of the requirements of the degree of
Master of Engineering

Prof. N. G. Tarr. Thesis Supervisor

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3 May 1995

Abstract

Silicon-germanium strained layer superlattices for use as buried channels in silicon pMOSFETs have been investigated. A superlattice avoids alloy scattering and potentially has a higher hole mobility than SiGe alloys.

Numerical modelling demonstrated hole population in a Si/SiGe/Si heterostructure sub-surface channel is highly dependent on germanium distribution. The superlattice structure has superior hole confinement in the sub-surface channel compared to other designs.

$(\text{Si}_7\text{Ge}_7)_p$ ($p = 1, 2, 3$) superlattice metal-oxide-semiconductor heterostructure (MOSH) capacitors were fabricated. Quasi-static $C-V$ measurements confirmed that onset of an inversion layer in the sub-surface channel occurs at lower $|V_G|$ than inversion in the surface channel. Sub-surface channel hole sheet density was found to be $\approx 3 \times 10^{12} \text{ cm}^{-2}$, in good agreement with theoretical predictions.

Acknowledgements

I would like to first thank my supervisor, Garry Tarr, for his advice and guidance in not only semiconductor device physics and process engineering, but also in career searching, car maintenance, wilderness conservation, and hiking, canoe and nordic ski routes.

I owe thanks to many people for their technical assistance. Thanks to those at the Institute for Microstructural Sciences of the National Research Council for various fabrication and processing procedures and technical advice, including J.-P. Noël (now at Bell-Northern Research), Dan Xia Xu, Dolf Landheer, and John McCaffrey for the TEM. Other technical assistance from members of the Department of Electronics, including Carol Adams, Lyall Berndt, Chris Peters (now at Northern Telecom Electronics) is sincerely appreciated. Thanks also to Roger Grant at the University of Waterloo and Rudy Beerkens at Northern Telecom. I owe sincere gratitude to Greg Snider at Cornell University, who supplied the Schrödinger-Poisson modelling program, made requested changes, and advised me in its use. For any problems that exist in this thesis, I cannot (unfortunately) blame any of these people.

For Sunita, who is for me both an inspiration and a distraction, and, despite geography, is never far from my mind.

Thanks to C.D. McDuff for thoughtful discussions, and to Zeus the cat.

Finally, a warm thanks to my parents, who have supported and encouraged me throughout my prolonged academic career.

In memory of Peter Kirkby.

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Chapter 1

Introduction

Advances in silicon technology over the past two decades have been impressive and pervasive. A fundamental factor determining the capability of electronic systems is the operating speed of their component devices. Over the past years, miniaturization has been the key to faster performance. However, there is justified concern that future advances cannot continue at the same rate nor to the same extent due to physical limitations. Other semiconductors, such as gallium arsenide, have higher electron mobility which enable complementary III-V HFETs to show superior performance to Si CMOS. Yet there is great reluctance to move to a technology based on a different semiconductor that is not compatible with present silicon technology.

There has been recent interest in a silicon compatible technology which incorporates a Si/SiGe/Si heterostructure in the substrate of a MOSFET. A buried channel formed by the SiGe/Si heterostructure can increase device

transconductance for a given size MOSFET. Advantages of band engineering of the binary SiGe also become possible, which are otherwise absent in silicon.

This thesis discusses an investigation into the use of a sub-surface (or buried) channel formed by a superlattice of alternating Si and pseudomorphic Ge layers built on a silicon substrate to enhance the performance of a p-MOSFET. Chapter 2 discusses the motivation for such an investigation and provides a background survey of previous research on SiGe channels in p-MOSFETs. There are several reasons why such a structure could show superior performance to all-silicon design transistors, but also inherent difficulties that must be considered. Modelling of SiGe structures using the Poisson and Schrödinger equations is discussed in Chapter 3. Experimental work, including fabrication and measured data, comprises Chapter 4. Conclusions are presented in Chapter 5.

Chapter 2

Background of SiGe MOSFETs

The development of SiGe for use in MOSFETs has been dependent on material quality. The success of utilizing SiGe/Si heterojunctions has been limited by understanding the effects of strain and control of growth conditions. In principle, strained SiGe potentially has significant advantages over Si, notably carrier mobility and possibilities of band engineering in a SiGe/Si heterostructure. However, several technological problems and issues arise in introducing SiGe into Si compatible MOSFETs. Some of these problems have been addressed, others are still under investigation.

2.1 Mobility and Scattering in a MOSFET

Carrier mobility in a metal-oxide-semiconductor field-effect-transistor (MOSFET) is limited by several factors. The most fundamental limit is the mo-

bility of a carrier in undoped substrate material — this is the intrinsic bulk mobility. Mobilities of three semiconductors used in transistor technology are shown in Table 2.1.

Semiconductor	Electron Mobility	Hole Mobility
Si	1500	450
Ge	3900	1900
GaAs	8500	400

Table 2.1: Intrinsic bulk Carrier Mobility of Semiconductors, measured in units of $\text{cm}^2/\text{V}\cdot\text{s}$, from [Sze81].

Note that the mobility of holes for most semiconductors is less than that of electrons. The purpose of incorporating Ge into Si compatible MOSFETs has been to use the greater hole mobility of Ge. The goal is a CMOS silicon technology that has high and nearly equal electron and hole mobilities.

Mobility is determined by several scattering mechanisms. For nonpolar semiconductors, such as Si and Ge, acoustic and nonpolar optical phonon scattering significantly affect mobility. Optical phonon scattering affects polar semiconductors, such as GaAs. For alloy semiconductors, additional scattering would be present due to the random placement of atoms in an alloy. The presence of ionized impurities affects the mobility of all semiconductors.

Scattering mechanisms have a cumulative effect on carrier mobility. The total mobility is determined by the summation of reciprocal mobilities, known

as Matthiessen's rule:

$$\frac{1}{\mu} = \sum_i \frac{1}{\mu_i}. \quad (2.1)$$

It is possible to distinguish separate forms of scattering and determine their magnitudes.

Specifically in a MOSFET, carriers travel near a silicon/silicon-dioxide¹ interface. The lattice of the crystal silicon substrate is discontinuous at this interface (the "surface"). This interface is rough (although the extent of roughness depends on surface treatment and oxidation conditions). This roughness introduces interface scattering. Additionally, fixed charges that exist in the oxide are also scattering centers. An added problem is the interface traps that also serve as scattering centres, lower the transconductance due to trapping of carriers, and also act as recombination centres for holes and electrons.

The transconductance of a MOSFET in the linear (or triode) region is

$$g_m = \frac{W}{L} \mu C_i V_D. \quad (2.2)$$

where W is the channel width, L is the channel length (or gate length), and V_D is the drain voltage. C_i is the insulator capacitance per unit area which equals ϵ_i/t_{ox} , where t_{ox} is the oxide thickness. The transconductance is directly related to carrier mobility. Current CMOS design typically uses greater channel widths in silicon p-MOSFETs to overcome lower hole mobil-

¹Silicon-dioxide is typically referred to simply as "oxide" in microelectronics literature.

ity. However, this technique results in larger transistor sizes and reduces the density of devices. Hence there is desire to increase hole mobility.

It is possible to create a buried channel p-MOSFET, in which the conducting layer of holes is confined $\approx 50 - 100$ nm below the surface. This structure can be created (and routinely is, in CMOS processes) using a blanket boron threshold adjust implant, which counterdopes the top region of an n-well to p-type. Such a structure reduces interface scattering, but increases short-channel effects. Impurity scattering also increases as a result. Due to boron diffusion and the lateral spread of the implant, the actual depth of the buried channel is difficult to control.

A SiGe heterojunction sub-surface channel p-MOSFET can be seen as an evolution of the homojunction buried channel MOSFET. ("Sub-surface channel" will implicitly refer to a heterostructure channel.) Carrier confinement in a heterojunction is superior to that of counterdoping, and avoids impurity scattering. In a silicon buried-channel p-MOSFET, the channel quickly moves to the surface as $|V_G|$ is increased. In contrast, the surface channel hole population in a heterojunction p-MOSFET dominates the sub-surface hole population only at much higher values of $|V_G|$. A SiGe sub-surface channel also has the potential advantage of a higher hole mobility of silicon-germanium alloys over that of silicon, as will be discussed in a separate section.

Before discussing the SiGe MOSFET in detail, it is worthwhile to examine

the properties of SiGe layers on a (100) Si substrate.

2.2 Properties of SiGe Strained Layers

2.2.1 Critical Layer Thickness

Silicon and germanium are completely miscible over the entire compositional range. Silicon, germanium and SiGe alloys have the diamond crystal structure, which is face centered cubic with a $[\frac{1}{4}\frac{1}{4}\frac{1}{4}]$ basis. Whereas the difference between the lattice constants of constituent semiconductors of many technologically important heterostructures is generally less than 0.001 nm, the Si/Ge combination is remarkably different. The lattice constants of bulk Si and Ge at room temperature are 0.357 nm and 0.357 nm respectively, a 4.2% difference. By depositing a SiGe alloy on a thick Si substrate, the mismatch will be accommodated either by a tetragonal distortion of the lattice (pseudomorphic, or two dimensional growth), or by a generation of misfit dislocations at the interface (three dimensional growth). See Figure 2.1.

Deposition conditions dictate whether pseudomorphic growth is favoured. A deposited pseudomorphic layer is under biaxial stress, and the lattice constant in the plane of the substrate conforms to that of the substrate. Tetragonal distortion of the deposited layer results. Under different conditions, misfit dislocations are encouraged to nucleate and may thread through the deposited layer. Strain relaxes by this mechanism, especially at high tem-

Figure 2.1: A two dimensional representation of pseudomorphic growth. (a) Unstrained SiGe and Si. (b) Pseudomorphic growth, in which the lattice constant difference is accommodated by tetragonal distortion. (c) Formation of dislocation misfits is another mechanism to accommodate lattice mismatch. From [IPS+89].

peratures, such as during growth or post-growth annealing. It is imperative to maintain crystal integrity in order to prevent dislocations (which may introduce traps or recombination centers) from forming, and maintain uniform stress on the thin film, which affects the band structure of Ge.

Critical thickness is defined as the maximum thickness for pseudomorphic growth; in this case, of $\text{Si}_{1-x}\text{Ge}_x$ on a Si substrate. There has been much debate on this issue, but no satisfactory theory has been proposed [IPS+89, pp 2045-6, and references contained therein]. Van der Merwe defined critical thickness as the maximum film thickness for which it was energetically favourable to contain the misfit by elastic energy stored in the distorted crystal. Matthews and Blakeslee proposed a definition in terms of the mechanical

equilibrium of a pre-existing threading dislocation. People and Bean have proposed a simple model that considers nonregularly spaced dislocations, and compared their predictions to the former two in [PB86b], which is reproduced here in Figure 2.2. There is some agreement that the critical thickness of pure Ge on Si is about 1.0 nm.

2.2.2 Hole Mobility in SiGe

In unstrained $\text{Si}_{1-x}\text{Ge}_x$ alloys, hole mobility remains relatively constant for $x < 0.5$. For Ge enriched alloys, hole mobility increases as the fraction of Ge increases. The Hall mobility of holes in unstrained $\text{Si}_{1-x}\text{Ge}_x$ has been measured [Lev55].

Theoretical studies of hole lattice mobility in pseudomorphic $\text{Si}_{1-x}\text{Ge}_x$ matched to (100) Si showed increases in mobility due to strain. One study investigated the effect of biaxial compressive strain on transport by first examining the band structure changes via deformation potential theory. The next step involved examining transport using a generalized Monte Carlo approach. The study concluded that in-plane hole mobility (μ_{xx}) was significantly higher than in the unstrained alloy, and a lesser improvement in out-of-plane mobility (μ_{zz}) was also evident [HSS89].

Another theoretical study calculated a first-order perturbation solution of the Boltzmann transport equation [MN91]. The calculations of the lattice mobility were based on three scattering mechanisms: 1) nonpolar optical,

2) acoustic phonon and 3) alloy scattering, combined using the Mathiessen rule. In strained $\text{Si}_{1-x}\text{Ge}_x$, the valence band is compressed which results in a decrease in the hole effective mass. The resulting components of mobility are significantly higher than those of unstrained $\text{Si}_{1-x}\text{Ge}_x$. These calculations confirm the earlier study by [HSS89], but extend up to $x = 1$.

The hole mobilities of strained and unstrained $\text{Si}_{1-x}\text{Ge}_x$ calculated in this study are shown in figure 2.3. The measured Hall mobility of unstrained $\text{Si}_{1-x}\text{Ge}_x$ is also shown for comparison. It is worth noting that μ_{xx} of strained Ge is predicted to be nearly *two orders of magnitude* greater than the mobility in unstrained Si, and one order of magnitude greater than unstrained Ge.

Interface Scattering in SiGe/Si Heterojunctions

Some experimental researchers suggest that interface scattering at $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ heterojunction interfaces decreases effective hole mobility in $\text{Si}_{1-x}\text{Ge}_x$. One report [VVC⁺94] stated abrupt Ge concentration discontinuities across the heterojunction resulted in pinholes observed in the overlying Si layer (5.0 nm thick) by high resolution TEM. These and other groups (such as Voinigescu *et al.* [VSNK91]) have recommended grading the Ge concentration linearly to 0% over ~ 2.5 nm to reduce interface scattering.

2.2.3 Energy Band Structure

Bulk $\text{Si}_{1-x}\text{Ge}_x$, also referred to as unstrained or relaxed, has a smaller fundamental band gap than Si. For $x \leq 0.85$, $\text{Si}_{1-x}\text{Ge}_x$ retains a silicon-like structure with the smallest gap occurring at the Δ -point near the X Brillouin zone boundary in the (100) direction. At greater concentrations of Ge, the smallest indirect gap occurs near the L Brillouin zone boundary — a characteristic of bulk Ge. The bandgap decreases more rapidly with increasing x for $x > 0.85$. At room temperature, unstrained Ge has a bandgap of ≈ 0.7 eV. The bandgap of unstrained $\text{Si}_{1-x}\text{Ge}_x$ has been measured experimentally over the range $0 \leq x \leq 1$ by Braunstein *et al.* [BMH58].

The band structure of strained $\text{Si}_{1-x}\text{Ge}_x$ is dependent on the strain conditions. Of relevant interest is pseudomorphic strained $\text{Si}_{1-x}\text{Ge}_x$ on unstrained (or cubic) Si. Theories have been introduced predicting this bandgap by People and Bean [Peo85], [PB86a] and Van de Walle and Martin [dWM86]. Both theories predict a significantly lower indirect bandgap relative to unstrained $\text{Si}_{1-x}\text{Ge}_x$. The six-fold degenerate conduction band of SiGe is split under strain. SiGe is under compressive strain when pseudomorphically grown on Si, and this strain raises the two-fold degenerate band {referred to as $\Delta(2)$ or E_2 } above the four-fold degenerate band $\Delta(4)$. Compressive strain in SiGe also splits the light hole and heavy hole bands in the valence band, whereby the light hole band is shifted upwards in energy compared to the heavy hole band [Ism92].

The bandgap of strained $\text{Si}_{1-x}\text{Ge}_x$ was measured by photocurrent spectroscopy by Lang *et al.* [LPBS85]. Measurements of $\text{Si}_{1-x}\text{Ge}_x$ were taken for $0.0 \leq x \leq 0.7$, and were in good agreement with the previously mentioned theories. Figure 2.4 shows the experimental data of this study along with the results of the unstrained bulk alloy. *To date, no measurements of the bandgap of strained $\text{Si}_{1-x}\text{Ge}_x$ on Si for $x > 0.7$ have been taken.*

Van de Walle and Martin [dWM86] compared their calculations of E_g to the experimental data of Lang *et al.* Although there was very good agreement between theory and experiment of the energy gap of strained $\text{Si}_{1-x}\text{Ge}_x$ on Si for $x = 0.4$, there were increasing discrepancies for $0.5 \leq x \leq 0.7$. In this range, the theory underestimated the measured values. The theoretical prediction of the bandgap energy of 0.49 eV of strained Ge on Si is also likely an underestimation.

The band gap and band offsets of coherently strained $\text{Si}_{1-x}\text{Ge}_x$ on (100) $\text{Si}_{1-y}\text{Ge}_y$ substrates were further calculated using the theory of Van de Walle and Martin and the experimental data by Lang in a study by People and Bean [PB86a]. In this study, the authors extracted a linear relationship of the valence band offset on the Ge content of the substrate y , which accounts for strain. The authors also assumed a linear interpolation of the Ge content in the strained layer x , such that

$$\Delta E_v(\text{Ge}_x\text{Si}_{1-x} \text{ on } (100) \text{ Ge}_y\text{Si}_{1-y}) = (0.74 - 0.53y)x \quad (2.3)$$

Combining ΔE_v with the experimental values of the energy gap of strained

$\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ by Lang, the authors were able to determine the band alignment for arbitrary structures of $\text{Si}_{1-x}\text{Ge}_x$ on $\text{Si}_{1-y}\text{Ge}_y$. The results are shown in Figure 2.5. Strain conditions and Ge content in both substrate and epitaxial layer influence the band alignment. Note the cases of strained $\text{Si}_{1-x}\text{Ge}_x$ on unstrained Si – the entire energy gap of the SiGe alloy is contained within the Si gap. The conduction band offset is 0.02 eV. Most of the bandgap difference is due to the offset in the valence band. By this theory, the offset in the valence band of strained Ge on cubic Si would be 0.74 eV, predicting $E_g = 0.43$ eV. In contrast, a rough extrapolation of the data by Lang *et al.* would predict $E_g \approx 0.55$ eV.²

Quantum Well

A double heterojunction is comprised of one material sandwiched between layers of the other material, in this case, SiGe between Si. If the SiGe layer is sufficiently thin, the electron (or hole) wavefunction will be coherent in this region, and the structure is known as a *quantum well*. Recall that the probability of finding a particle in a specific position is proportional to the square of the wavefunction in that position.

Due to the discontinuity of the valence band in a $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ heterojunction, a quantum well can be formed by a Si/SiGe/Si structure, provided the heterostructure is sufficiently thin. In this case of cubic silicon and strained

²This value is used later in this thesis.

SiGe, the conduction band is, to first order, continuous, leaving the electron population unaffected, and the discontinuity in the valence band forms a quantum well for holes. The quantum well would be much more highly populated with holes than the neighboring silicon, due to the well being a more energetically favourable location for the holes to reside.

2.3 The SiGe MOSHFET and MOSH Capacitor

The SiGe metal-oxide-semiconductor-heterostructure field-effect-transistor (MOSHFET)³ incorporates an Si/SiGe/Si heterostructure as a sub-surface channel. The MOSHFET has advantages over both the standard Si MOSFET and the buried-channel p-MOSFET. Unlike the MOSFET, the MOSHFET reduces surface scattering of holes, and the SiGe sub-surface channel has an equal or higher hole mobility than bulk Si. The sub-surface heterojunction in a MOSHFET provides superior hole confinement than the counterdoped buried channel (homojunction) MOSFET. Moreover, due to boron diffusion and the lateral spread of the implant, the depth of a counterdoped buried channel is difficult to control and is generally sufficiently deep to introduce undesirable short-channel effects. The depth of a heterostructure can be more

³distinguished from the standard Si MOSFET --- see Appendix A. Note that this term is coined here.

precisely controlled and be kept closer to the surface to avoid short-channel effects.

The typical design of a MOSHFET begins with a moderately doped n-type (100) silicon substrate. A *buffer* layer of undoped Si is grown epitaxially on the substrate, followed by the SiGe heterostructure. Above the SiGe is a Si *cap* layer, also undoped. Other regions, including the oxide and metal layers, source and drain, are similar to the standard MOSFET design. (A specific design of MOSHFET is shown in Figure 2.8, to be discussed later.) The addition of a δ -doping layer underneath the buffer layer has also become a common feature in some designs.

For very small drain voltages V_D and long channel lengths in a MOSHFET, a one dimensional analysis perpendicular to the surface is valid. This analysis then ignores source and drain regions. Such a structure is a MOSH capacitor, which can be studied theoretically and experimentally, while still providing insight into MOSHFET characteristics.

2.3.1 Recent Investigations on SiGe MOSHFETs

It is not the intent of this section to be an exhaustive survey of the work in this field, but rather to acknowledge some of the research which motivated this thesis. In 1989, Iyer *et al.* [IPS⁺89] wrote an excellent review of the research into SiGe used for heterojunction bipolar transistors, an article which is still useful although dated. A minority of the research on SiGe has gone

into its use in MOSHFETs, although this body of literature is still large. A few of these investigations are discussed here. (For the remainder of this thesis, the term "MOSHFET" will be used to distinguish the SiGe heterostructure system from Si MOSFETs, although previous authors did not use this terminology. Also implicit in this thesis is charge carriers in the SiGe channel are holes, hence the devices are p-MOSHFETs.)

Nayak, Woo, Park, Wang and MacWilliams

In April 1991, Nayak *et al.* [NWP⁺91] reported the fabrication of an enhancement mode quantum well Si_{0.8}Ge_{0.2} MOSHFET. They noted that the previous lack of interest in Si_{1-x}Ge_x MOSHFETs was mainly due to the difficulty in achieving a high-quality SiO₂ on a Si_{1-x}Ge_x strained layer. This group used rapid thermal wet oxidation at 870°C to thermally grow oxide on Si as the gate dielectric, and rapid thermal annealing at 770°C for the post-implant anneal. (No mention of the effect of the thermal budget on the SiGe heterostructure was made. Since an alloy with such a low Ge content has a high critical thickness and low level of strain, the thermal budget would presumably be higher than those of Ge enriched layers.)

Fabrication began by growing 500 nm of Si, with $5 \times 10^{16} \text{ cm}^{-3}$ n-type doping, on an n-type (100) Si substrate. Above this layer a 10 nm Si buffer layer, a 15 nm Si_{0.8}Ge_{0.2} layer, and a 10 nm Si cap layer were grown by MBE. All these thin layers were grown without intentional doping, but had

$\approx 5 (10^{15}) \text{ cm}^{-3}$ n-type background doping. A 5 nm gate oxide was thermally grown. Similarly processed Si MOSFETs were fabricated for comparison.

The SiGe devices showed good saturation and subthreshold behaviour, and the channel mobility was found to be higher than for the MOSFETs.

Garone, Venkataraman, Liu and Sturm

This group first reported an investigation into hole confinement in SiGe MOSH capacitors [GVS91b]. They developed a numerical model which solved the one-dimensional Poisson's equation for a MOSH capacitor at a given gate bias. The modelling demonstrated that the $\text{Si}_{1-x}\text{Ge}_x$ sub-surface well populated with holes at lower $|V_G|$ than the surface channel. A figure of merit was introduced, the *crossover point*, at which the hole population in the sub-surface well equals the hole population at the surface. The objective of a MOSHFET is to maximize the hole density at crossover. The group related the crossover point to hole density, Si cap thickness, and Ge fraction in the well (for $0.05 \leq x \leq 0.4$).

A MOSH capacitor was fabricated having a 7.5 nm Si cap layer, 10 nm thick $\text{Si}_{0.6}\text{Ge}_{0.4}$ well, a 10 nm plasma deposited gate oxide, and an aluminum metal gate. Low frequency (quasi-static) capacitance versus gate voltage measurements showed a plateau in the inversion region below C_{ox} . This plateau was verification that holes were populating the $\text{Si}_{1-x}\text{Ge}_x$ well. Figure 2.6 is reprinted from this work, which illustrates MOSH capacitor mea-

measurements at both low and high frequencies, a low frequency MOS capacitor measurement, and a modelled MOSH quasi-static capacitance versus voltage curve. A MOSH Hall device also measured hole sheet density confirming modelling predictions.

Two later investigations into mobility enhancement in MOSHFETs found increased sub-surface hole mobility at low temperatures [GVS91b] [GVS92]. This trend cannot be explained by a reduced effective hole mass in the SiGe channel, hence mobility can be characterized by bulk and surface scattering. Referring to the total, or measured, mobility of holes in the (surface) inversion layer of a Si MOSFET as $\mu_{inversion}$, then according to Matthiessen's rule,

$$\frac{1}{\mu_{inversion}} = \frac{1}{\mu_{bulk}} + \frac{1}{\mu_{surface}}.$$

Since μ_{bulk} is well known, the researchers assumed that the surface scattering was proportional to the square of the distance of the holes to the Si/SiO₂ interface Z , ie.

$$\mu_{surface} \propto Z_{av}^2 \quad (2.4)$$

Different cap layer thicknesses in MOSHFETs were used, enabling the investigators to determine the extent of surface scattering.

Drain currents of a control Si MOSFET and three SiGe MOSHFETs were measured. The MOSHFETs had, respectively, SiGe channels comprising of 20%, 30% and 40% Ge content. The hole mobility in the Si_{0.7}Ge_{0.3} MOSHFET was $\sim 50\%$ greater than the MOSFET. The mobility of the Si_{0.6}Ge_{0.4} MOSHFET was much lower than the all-silicon control device. The authors

attributed the difference to misfit dislocations at the Si/Si_{1-x}Ge_x interface. The authors mention that 10 nm of Si_{0.6}Ge_{0.4} is almost twice the equilibrium critical thickness defined by Matthews and Blakeslee. It was not known whether the dislocations were process-induced or had relaxed. The perils of misfit dislocations are clearly demonstrated.

Another investigation into alloy scattering in Si_{1-x}Ge_x was reported by this group [VLS93, and references therein]. The theoretical description of alloy scattering limited mobility of a two dimensional electron gas (2DEG) at low temperatures is

$$\mu_{\text{alloy}} = \frac{K}{V_{\text{alloy}}^2 x(1-x) n^{1/3}} \quad (2.5)$$

where x is the concentration of Ge, n is the electron concentration, and K is a function of atomic volume, transverse effective mass and dielectric constant. This group fabricated a strained Si_{1-x}Ge_x layer on a relaxed Si_{0.62}Ge_{0.38} buffer which created a 2DEG at the interface in the strained Si_{1-x}Ge_x. Experimental measurements of the 2DEG found a significant mobility limitation due to alloy scattering. Measurements on Si_{1-x}Ge_x layers with Ge content $0.00 \leq x \leq 0.20$ were performed, and the alloy disorder potential $V_{\text{alloy}} = 0.8 \pm 0.1$ eV fit the data. Impurity scattering was assumed to be the only other significant contributor to scattering, as the 2DEG was removed from the surface by a thick spacer layer.

These investigators examined the hole mobilities in Si/SiGe/Si heterostructures previously reported by other research groups. In these previous reports,

the low hole mobilities found at low temperatures were attributed to remote impurity scattering or poor sample quality. However, Venkataraman *et al.* found these results fit well to the alloy scattering model using $V_{\text{alloy}} = 0.6$ eV. They conclude that alloy scattering and not sample dependent effects limit hole mobility in SiGe/Si heterostructures.

Verdonckt-Vandebroek, Crabbé, Meyerson, Hame, Restle, Stork and Johnson

Verdonckt-Vandebroek *et al.* have published several articles on modulation-doped graded SiGe channel p-MOSFETs [VVC+91a] [VVC+91b] [VVC+94]. This group interchangeably refers to these structures as MODFETs and MODMOS. The modulated doping refers to a delta-doping of boron used for a threshold voltage adjust. The cap layer, the SiGe channel and the buffer layer are undoped. The SiGe channel, which is between 5 nm and 25 nm in depth, is graded, such that the Ge content is linearly ramped from 25% to 15%, the higher concentration being nearer the surface. This group introduced the unusually deep placement of the doping spike between 30 nm and 35 nm below the Si/SiO₂ interface, hence about 5 nm *below* the SiGe channel.

These authors distinguish four critical SiGe MOSFET design parameters: gate material, threshold voltage adjustment, Ge profile, and silicon-cap and gate-oxide thicknesses. Each are investigated using a one-dimensional

Poisson simulator. Quantum effects are ignored because SiGe widths are equal to or exceed 5 nm.

This group introduced a partially graded (or trapezoidal) Ge profile to both maximize hole concentration in the SiGe channel and insure adequate confinement up to high gate voltages. This profiling is superior to a flat channel profile in both respects. These authors argue that a discontinuity in Ge content at the bottom SiGe/Si heterointerface is required for n^+ -poly gate MOSHFETs where modulation doping is used to ensure negligible conduction in the boron-doped layer. However, a p^+ -gate would not require the offset at this interface, and fully-graded 0% to 39% Ge content channels would be possible. Comparisons are done using the crossover voltage as a figure of merit. The authors note that for the range of x studied ($0 < x < 0.4$) for $\text{Si}_{1-x}\text{Ge}_x$ channels, the cross-over voltage is linearly proportional to x . Also, for a common quantity of Ge over the same channel thickness, grading the channel with the maximum Ge concentration at the channel top increases the cross-over voltage. Hence grading the channel instead of a constant concentration results in a larger current drive, since the mobility of holes in the SiGe channel is higher than in the Si cap layer. The authors use the Matthews-Blakeslee critical layer thickness limit [MB74] to determine the maximum allowable thickness of the $\text{Si}_{1-x}\text{Ge}_x$ channel layer.

By minimizing the thicknesses of the Si cap and the gate oxide, the gate-to-channel capacitance and hence transconductance can be increased. Sim-

ulations indicated that decreasing the Si cap thickness would increase the cross-over voltage. To increase the cross-over voltage by varying the gate oxide thickness, the thickness had to be increased.⁴

For thin Si cap layer thicknesses (≈ 3 nm), interface scattering would begin to degrade hole mobility. A thinner cap layer would increase channel-to-gate capacitance, so a trade-off between mobility and capacitance exists in order to maximize transconductance.

Voinigescu and Salama

These authors state that a significant improvement in the hole mobility of SiGe channels over Si devices requires Ge concentrations of 40% or higher [VS92] [VSNK94]. As this Ge content would require a thin channel, these researchers avoid this problem by fully grading the Ge content from 0% to 40% for a 15 nm thick SiGe channel - a triangular Ge profile. These authors developed a one-dimensional modelling program that solved both Poisson's and Schrödinger's equations, and demonstrated for an identical MOSHFET to the one described in [VVC⁺91a], except for the Ge distribution in the channel, an increase of hole mobility of a triangular Ge profile channel over a trapezoidal profile channel. These authors argue the trapezoidal profile is not required to prevent sub-surface channel holes from interacting with the

⁴It should be mentioned that cross-over voltage will be affected by cap layer and gate oxide thickness alterations, although the sub-surface channel hole sheet charge at cross-over will remain unaffected. The cross-over voltage cannot be used as the sole figure-of-merit for such comparisons.

δ -doped layer, since the Ge grading and Si buffer layer prevent this problem. Higher values of the cut-off frequency f_T were also found for the fully-graded channel MOSHFET. These authors have also reported that the presence of a δ -doped p-type layer beneath the Si buffer increases hole population in the SiGe sub-surface channel, while having minimal effect in the surface channel.

2.3.2 Analysis of the SiGe MOSH Capacitor

Iniewski and Voinigescu *et al.* have published excellent analysis of the MOSH capacitor [IVAS93] [VIL⁺94]. The analysis assumes the cap layer, the SiGe heterostructure and buffer layer are undoped. Below the buffer layer is a δ -doped layer and a uniformly doped substrate.

The onset of strong inversion is defined at which the concentration of minority carriers (in this case holes) is equal to the substrate doping concentration $N_B = N_D - N_A$. The threshold surface potential ψ_{TS} for strong inversion at the surface is

$$\psi_{TS} = 2\psi_B \quad (2.6)$$

where

$$\psi_B = \frac{kT}{q} \ln\left(\frac{N_D}{n_i}\right). \quad (2.7)$$

The threshold potential ψ_{TH} at the top heterointerface is

$$\psi_{TH} = 2\psi_B + \frac{\Delta E_v}{q} \quad (2.8)$$

assuming the density of states in the valence bands of Si and SiGe are (nearly) equal. ΔE_v is the offset in the valence band.

Similarly, the gate voltage which causes strong inversion at the top heterointerface, V_{TH} , can be calculated and distinguished from the gate voltage causing strong inversion at the surface, V_{TS} .

$$V_{TH} = V_{FB} + \psi_{TH} - qN_B x_{dmax} \left(\frac{x_{cap}}{\epsilon_{Si}} + \frac{t_{ox}}{\epsilon_{ox}} \right) \quad (2.9)$$

$$V_{TS} = V_{FB} + \psi_{TS} - \frac{qN_B x_{dmax}}{C_{ox}} \sqrt{1 + H(\psi_H)} \quad (2.10)$$

where x_{dmax} is the maximum depletion layer thickness, and

$$H(\psi_H) = \frac{2\epsilon_{SiGe} N_B kT}{(qN_B x_{dmax})^2} \exp \left(\frac{q(\psi_{TH} - \psi_{TS})}{kT} \right) \quad (2.11)$$

where ψ_H is the potential at the top heterointerface.

The gate voltage window

$$\Delta V_T = V_{TH} - V_{TS} \quad (2.12)$$

can be measured experimentally from quasi-static capacitance-voltage curves. See Figure 2.7.

The authors have developed analytic methods to determine the cap layer thickness x_{cap} , V_{TS} and V_{TH} from "apparent doping profiles" (described in the article), and interface trap density D_{it} and fixed charge Q_f from experimental and simulated profiles. The reader is referred to these publications for further detail.

2.4 Pseudomorphic Ge on Si

As mentioned previously, no satisfactory theory has been proposed to predict the critical thickness of $\text{Si}_{1-x}\text{Ge}_x$ on cubic Si. Consequently, there is no agreement whether pseudomorphic Ge can be grown on silicon. Fortunately, this issue has been investigated recently by experiment by Lockwood *et al.* [LBJ+93].

The purpose of this investigation was to study the nature and thermal stability of the Si/Ge interface, particularly strain relaxation and interdiffusion resulting from growth and post-growth annealing. The study investigated single $(\text{Ge})_n$ epitaxial layers (epilayers) (where n is the number of monolayers) grown on a Si substrate, with ≈ 33 nm cap layer of Si above the Ge. For $2 \leq n \leq 5$, X-ray interference measurements confirmed a two dimensional pseudomorphic Ge layer. For $n = 5$, X-ray measurements indicate the Ge layer thickness to be 0.90 nm. Another growth with $n = 12$ showed the Ge layer underwent a transition from two dimensional to three dimensional growth, first indicated by X-ray and confirmed by cross-sectional transmission electron microscopy. Clearly, it is possible to grow pseudomorphic Ge directly on Si. Lockwood's study imposed an upper limit on the critical thickness of 1.70 nm, but also demonstrated pseudomorphic growth of 0.90 nm of Ge buried in Si. This is in agreement with the theories of People and Bean and Matthews and Blakeslee.

The interplanar distance (ie. a monolayer (ML)) of strained pseudomor-

phic Ge on Si is taken to be 0.146 nm, as calculated in this study using classical elasticity theory. This value is greater than the bulk value, due to strain in which the lattice is stretched in the growth direction to preserve coherency at the Si/Ge interface. For bulk Ge, the interplanar distance is one quarter of the lattice constant, which gives a value of 0.1415 nm.

2.4.1 Si/Ge Strained Layer Superlattice

In the present investigation, a superlattice of pure Si and pure Ge layers was studied. The notation used to describe the superlattice is $(\text{Si}_m\text{Ge}_n)_p$, where m and n are the number of epilayers of Si and Ge respectively, and p is the number of periods of alternating Si and Ge.

The superlattice is an extension of the concept of a single quantum well to an alternating, multi-layered periodic structure of several heterojunctions. In cases in which the layers are sufficiently thick that the wave functions are independent from each other and do not overlap, the result is a structure known as a multi-quantum well. However, in cases that the layers are sufficiently thin that the wave functions are not independent and interfere with each other, the resulting structure is a superlattice.

In the analysis of the periodic potential of an atomic lattice, the nearly free electron model led to the description of an energy spectrum as a function of the wave vector (or crystal momentum) $\mathbf{k}$ in reciprocal lattice space ($\mathbf{k}$ -space).

In a superlattice, it is assumed the overlap of the wavefunctions is finite but small enough for the tight-binding approximation to remain valid. The energy as a function of wave vector in the direction of the superlattice axis is similar to the description of an atomic lattice, but the parameters of the isolated quantum well replace those of the atom. The free-electron mass is replaced by the effective mass from the conduction or valence band edge, and the superlattice period d replaces the interatomic distance. The resulting superlattice Brillouin zone (BZ) is then $2\pi/d$, which is much finer than the atomic BZ. In addition, the valence (or conduction) band is divided into a series of minibands (or subbands) separated by minigaps at the BZ boundary, as in the case of an atomic lattice [Jar89]. "Brillouin zone folding" created by superlattice periodicity may lead to the predicted direct band gap of Si/Ge superlattices [GC74]. This interesting phenomenon is not considered here.

2.5 Growth and Processing Considerations

2.5.1 Epitaxial Growth

Early attempts to grow pseudomorphic SiGe alloys on Si were unsuccessful due to surface tension and strain which lead to non-pseudomorphic growth and islanding. Two competing temperature requirements must be addressed for epitaxial growth. The first requirement is a sufficiently high growth temperature for adatom mobility to achieve high quality epitaxial growth. The

second requirement is a sufficiently low temperature to prevent islanding and strain relaxation. The first attempts to grow SiGe by molecular beam epitaxy failed because the temperatures of $\geq 750^{\circ}\text{C}$ were too high[BFF⁺84]. Temperatures of $\approx 500 - 550^{\circ}\text{C}$ were later found to be appropriate.

There are two essential concerns that must be addressed for any Si process: 1) the initial cleaning of the deposition surface, and 2) maintaining a high-purity environment during growth. Conventional chemical vapour deposition employs high temperatures ($T > 1000^{\circ}\text{C}$) to accomplish these objectives, which is not suitable for pseudomorphic growth of SiGe on Si. The technique of ultra-high vacuum CVD developed by Meyerson[Mey92] has successfully produced SiGe films at a growth temperature of 550°C . This method precludes oxygen and carbon contamination. In contrast, conventional CVD relies on chemical equilibrium to reduce oxygen content in deposited layers at higher temperatures. UHV conditions are standard in MBE. Elemental species directly impinge upon a heated substrate in this growth technique. The growth rate and film composition are largely dependent only on the impinging species; temperature and substrate orientation have only minor effects. The low processing temperature suppresses segregation and relaxation kinetics [IPS⁺89, and references contained therein]. Both MBE and UHV/CVD rely on proper vacuum techniques to obtain a high quality interface and maintain low contaminant levels.

2.5.2 Thermal Stability

The structural integrity of strained layer Si/Ge superlattices and effects of strain relaxation and interdiffusion caused by elevated temperatures are of utmost concern in processing. Of particular relevance are studies by Lockwood *et al.* [LBL92] [LBJ+93], who investigated growth quality and the effects of annealing of $(\text{Si}_m\text{Ge}_n)_p$ superlattices using several experimental methods — Raman scattering, extended X-ray absorption fine structure, and X-ray reflectometry. Measured X-ray reflectivity data from the as-grown $(\text{Si}_4\text{Ge}_4)_5$ and $(\text{Si}_5\text{Ge}_5)_4$ superlattices were compared to calculations assuming different degrees of interfacial mixing. The results suggested that appreciable mixing exists at the Si-Ge interfaces from the MBE growth process.

The effects on these superlattices due to annealing at 700°C for 20, 200 and 2000 s were measured by X-ray reflectivity and Raman scattering. It was found that considerable intermixing and partial relaxation of Ge-Ge bonds occurred for very short times at 700°C. Even for anneal times of 20 s, significant strain-enhanced intermixing was found to occur, evidenced by the change of the ratio of interatomic bonds between Si-Ge and Ge-Ge. The X-ray reflectivity data were compared to data from a $\text{Si}_{0.5}\text{Ge}_{0.5}$ alloy, and it was found that after the 20 s anneal at 700°C, the superlattice structure could not be easily distinguished from a homogeneous alloy of the same average composition.

Raman spectra were measured for the two SL and alloy layers as-grown

and after annealing for 20 s at 500, 600 and 750°C. The SL were not affected by the 500°C anneal. Evidence of diffusion across the Si-Ge interface was seen after the 600°C anneal. This was attributed to diffusion and strain relief. After the 750°C anneal, the spectra of the SL were very similar to the as-grown alloy spectrum. The Raman spectrum of the alloy layer showed no effects due to annealing, suggesting that little or no interdiffusion occurred between the alloy layer and the surrounding Si cap and buffer layers.

At longer times, the bond ratio continues to increase, but at a slower rate consistent with diffusion.

2.6 Si/Ge Superlattice Sub-Surface Channel MOSHFET and MOSH Capacitor

The purpose of this thesis is to investigate another possible solution to the problem of Ge distribution in a SiGe channel and the strain related effects.

The novel concept of using a $(\text{Si}_n\text{Ge}_m)_p$ superlattice as a sub-surface channel MOSHFET is introduced in this thesis. A Si/Ge strained-layer superlattice MOSHFET would be similar to SiGe MOSHFETs described previously, but a superlattice would replace the $\text{Si}_{1-x}\text{Ge}_x$ alloy forming the channel. Other considerations, such as background doping levels and delta-doping, Si cap and buffer layer thicknesses, would be considered independent of the sub-surface channel. A drawing of such a MOSHFET is shown in Figure 2.8.

Although a sub-surface SiGe MOSHFET has increased hole mobility due to increased distance of the carriers from the oxide interface, alloy scattering in $\text{Si}_{1-x}\text{Ge}_x$ significantly limits the hole mobility. A strained layer superlattice of pure Ge and Si layers could reduce alloy scattering, hence further increasing hole mobility in the sub-surface channel. Further advantages from increased in-plane hole mobility in strained Ge could also be expected. The hole distribution in a superlattice is dependent on quantum effects, unlike holes in a larger SiGe alloy heterostructure. Accordingly, the hole distribution in a superlattice must be modelled using both Poisson's and Schrödinger's equations, which is discussed in the following chapter.

A MOSH capacitor has the same structure as a MOSHFET, but without source and drain. A capacitor requires fewer fabrication steps, yet permits measurement and analysis of the superlattice.

The remainder of this thesis investigates the feasibility of a Si/Ge superlattice sub-surface channel MOSHFET. Chapter 3 discusses theoretical analyses, and Chapter 4 summarizes experimental work on Si/Ge superlattice MOSH capacitors.

Figure 2.2: Critical layer thickness plotted as a function of Ge content, from [PB86b, and references contained therein]. Open circles are experimental single layer critical thickness results from Bean *et al.* Filled circle (at $x = 0.7$) is a commensurate layer thickness for GeSi layer in a superlattice (*ibid.*). The solid square at $x = 1$ is the experimental result from Bevk *et al.* Theoretical predictions by People and Bean (solid line), Van der Merwe (dashed line) and Matthews and Blakeslee (dot-dash) are included.

Figure 2.3: a. Cross section illustrating direction of tensorial mobility components. b. Strained (tensorial) and unstrained hole mobilities (in units of $\text{cm}^2/\text{V}\cdot\text{s}$) for $\text{Si}_{1-x}\text{Ge}_x$ as a function of Ge fraction at room temperature. From [MN91].

Figure 2.4: Measured band gap of unstrained $\text{Si}_{1-x}\text{Ge}_x$ and pseudomorphic $\text{Si}_{1-x}\text{Ge}_x$ on Si. The $\pm 1/2$ and $\pm 3/2$ notation refers to spin. Circles represent data from 7.5 nm SiGe wells, triangles represent data from 3.3 nm SiGe wells. From [LPBS85, and references therein].

Figure 2.5: Band offset in SiGe/Si heterojunction due to strain, from [PB86a].

Figure 2.6: MOSH capacitance versus voltage, from [GVS91b].

Figure 2.7: Simulated quasi-static C-V curve of SiGe MOSH capacitor showing threshold voltages and capacitance plateau, from [VIL⁺94].

Figure 2.8: Si/Ge Superlattice p-MOSHFET

Chapter 3

Theory and Modelling

This chapter undertakes a theoretical investigation of the feasibility of using a Si/Ge superlattice sub-surface channel to increase hole confinement in a MOSH structure.

A numerical modelling program was used which simultaneously solved Poisson's and Schrödinger's equations, and which determined hole distribution, electric field and energies of the conduction and valence bands edges as a function of depth. The non-trivial task of modelling hole mobility, though relevant and quite desirable information, was not available with this program and is beyond the scope of this thesis.

3.1 Poisson-Schrödinger Equations Solver

The objective of the modelling for this thesis was to investigate the carrier occupancy of a Si/Ge superlattice incorporated in a MOSH structure. Unlike most other analyses of SiGe MOSH FETs that solved Poisson's equation alone, the Schrödinger equation must be considered for the device structures of interest here, and be solved self-consistently with Poisson's equation. Due to the extremely narrow width of the layers in the superlattice, quantum effects had to be considered. Hole populations in a superlattice (SL), due to tunnelling and quantum interference, would be different than would be predicted by Poisson's equation. For instance, the layers of a $(\text{Si}_7\text{Ge}_7)_3$ superlattice are approximately 1 nm thick. When the thickness of a layer is reduced to the order of the de Broglie wavelength, two dimensional quantization occurs. The Schrödinger solution results in a series of discrete energy levels given by the bound-state energies of a finite quantum well [Sze81, p729].

A software package written by G. Snider [TSC'H90] was used. The program uses the method of finite differences to find the band diagram of a semiconductor structure. The program calculates the conduction and valence band energies, the hole and electron concentrations, and the electric field as a function of position. With inclusion of the Schrödinger equation, the heavy hole and light hole wavefunctions and energies were calculated. The effective masses and temperature were used to implicitly determine the

density of states in the conduction and valence bands. Details of the mathematical algorithm of the program are outlined in Appendix B.

The program was intended to model charge distribution in semiconductors, and was unable to model an insulating material. It was also limited in the boundary conditions available. A Schottky barrier boundary condition in thermal equilibrium (ie. no bias) was therefore used in order to simulate applied gate voltages in a MOS structure. For a metal-(n-type)-semiconductor junction, the Schottky barrier height $q\phi_{Bn}$ is the energy difference between the Fermi level (in both the metal and the semiconductor) and the conduction band edge at the interface. The extent of the band bending in thermal equilibrium is the built-in potential V_{bi} .

This band bending in the Schottky barrier is equivalent to the band bending in a metal-oxide-(n-type)-semiconductor in inversion. The surface potential ψ_s is negative, and is equal in magnitude to V_{bi} . The difference between the Fermi level E_F and the intrinsic Fermi level E_i is ψ_B , defined in equation 2.7 on page 23.

We can define ψ_o as the difference between E_F and the conduction band energy E_c , such that

$$\psi_o = \frac{E_g}{2} - \frac{kT}{q} \ln\left(\frac{N_D}{n_i}\right). \quad (3.1)$$

It is clear that

$$\psi_s = -\phi_{Bn} + \psi_o \quad (3.2)$$

which relates the ϕ_{Bn} of the Schottky barrier to the surface potential of a

Figure 3.1: Energy diagram showing the equivalence of a Schottky-(n-type)-semiconductor junction and metal-oxide-(n-type)-semiconductor junction in inversion.

MOS structure. See Figure 3.1. This description ignores the SiGe heterostructure and second-order effects to the surface.

Assuming the absence of charge in the oxide, the electric field will be constant throughout the oxide. The oxide potential ψ_{ox} can be related to the electric field in the semiconductor at the interface by

$$\psi_{ox} = \mathcal{E}_{ox} t_{ox} = \mathcal{E}_{Si}(x=0) \frac{\epsilon_{Si}}{\epsilon_{ox}} t_{ox} \quad (3.3)$$

since the displacement field $\mathcal{D} = \epsilon \mathcal{E}$ is continuous. The electric field in the semiconductor at the interface $\mathcal{E}_{Si}(x=0)$ is provided by the modelling program. The metal semiconductor workfunction for a p^+ poly gate on an

n-type semiconductor is

$$\phi_{ms} = \frac{E_g}{2} + \frac{kT}{q} \ln\left(\frac{N_D}{n_i}\right) \quad (3.4)$$

which is the final term necessary to determine the gate voltage, namely

$$V_G = \psi_{ox} + \psi_S + \phi_{ms}. \quad (3.5)$$

In the program, ϕ_{Bn} is the independent variable, which is then related back to V_G through these equations.

The energy gap E_g of $\text{Si}_{1-x}\text{Ge}_x$ was explicitly included in the input files. The values of E_g for $x < 0.7$ were taken from the data of Lang [LPBS85]. For $x = 1$, ie. strained pseudomorphic Ge on Si, the value of 0.55 eV was used, determined by extrapolating the experimental data. This value is greater than values predicted by theory, as mentioned earlier.

At submicron gate lengths, short channel effects become severe for n^+ poly gate p-channel MOSFETs. For this reason, p^+ poly gates are preferable for p-MOSFETs. The difference of the workfunction of n^+ and p^+ gates results in a lowering of $|V_T|$ equal to the silicon bandgap.

3.2 Poisson-Schrödinger Modelling Results

The graphs generated by the Poisson-Schrödinger equations solving program show conduction and valence band edges, hole density, electric field etc. along a chosen line in a two dimensional structure. The ordinate of the graphs

display characteristics along the line perpendicular to the surface and into the substrate. Hence, the distance scale of the abscissa is depth, and zero depth indicates the silicon/oxide interface. The region is directly beneath the gate of a MOSH capacitor. The model makes calculations based on a 300 nm thick substrate.

Unless otherwise stated, the structures modelled assume a p^+ poly gate, a gate oxide thickness of 10 nm, have n-type doping of $N_D = 10^{15} \text{ cm}^{-3}$ in the top 30 nm (which includes the cap layer, the heterostructure (or superlattice), and buffer layer), on a substrate doped $N_D = 10^{17} \text{ cm}^{-3}$. Quoted applied voltages assume these conditions for a MOSH structure.

The textbook delta-depletion model predicts a maximum depletion width $x_{D,inv}$ at inversion.

$$x_{D,inv} = \sqrt{\frac{2\epsilon_{Si}(2\phi_B)}{qN_D}} \quad (3.6)$$

Assuming a constant $N_D = 10^{17} \text{ cm}^{-3}$ (which underestimates $x_{D,inv}$) and ignoring the Si/Ge superlattice or heterostructure (which would overestimate $x_{D,inv}$ due to the additional charge), $x_{D,inv}$ is calculated to be 105 nm, within the 300 nm thickness modelled. Hence the effects from the back of the sample are insignificant.

Two superlattice structures will be studied and compared to similar alloy heterostructures. Discussion on single sub-surface Ge layers and superlattices follows. The capacitance-voltage characteristics are also calculated.

3.2.1 Comparison of $(\text{Si}_7\text{Ge}_7)_3$ with $\text{Si}_{0.4}\text{Ge}_{0.6}$

In order to compare a Si/Ge superlattice with a $\text{Si}_{1-x}\text{Ge}_x$ alloy quantum well, two structures were studied. A $\text{Si}_{0.4}\text{Ge}_{0.6}$ alloy 5.0 nm thick was investigated alongside a $(\text{Si}_7\text{Ge}_7)_3$ superlattice. The total quantity of Ge is held constant and is confined within 5.0 nm. (It should be noted parenthetically that such an alloy is extremely rich in germanium.) Other characteristics, such as doping, cap and buffer layer thicknesses, were kept constant.

Figure 3.2 illustrates the conduction and valence bands of a $(\text{Si}_7\text{Ge}_7)_3$ superlattice and a $\text{Si}_{0.4}\text{Ge}_{0.6}$ alloy heterostructure, each 5.0 nm thick. The zero line of energy represents the Fermi energy. The 10 nm cap layer of silicon is evident. As stated previously, a thin gate oxide and p^+ poly gate are assumed to be present for purposes of modelling applied voltage. This structure is thus part of a sub-surface channel p-type MOSHFET or MOSH capacitor. There is negligible change of the conduction band across the heterojunction, since the offset occurs primarily across the valence band. The valence band offset in the superlattice is greater than in the $\text{Si}_{0.4}\text{Ge}_{0.6}$ alloy.

Figure 3.2 is a detail of the Figure 3.3, the latter showing the band diagram of the superlattice (alone) to the full modelled depth of 300 nm. This figure confirms the calculation of a maximum depletion depth of ≈ 100 nm, and provides confidence that no edge (or back) effects are introduced. Note the change of slope in the conduction band at ≈ 100 nm, which is evidence of charge in the superlattice.

Band Diagram of SiGe

Figure 3.2: Conduction and Valence Bands of a SiGe superlattice and $\text{Si}_{0.4}\text{Ge}_{0.6}$ alloy heterostructure, 10 nm below the oxide/silicon interface.

The valence band offset in both the strained Si/Ge superlattice and the SiGe single quantum well provide for hole confinement in the Ge rich layers. Results of the calculations of the conduction and valence band edges by the Poisson equation and combined Poisson-Schrödinger equations are virtually identical. However, calculations of carrier densities for the superlattice structure are quite different than for the single quantum well. The

Band Diagram - Extended Range

Figure 3.3: Band Diagram over Full Modelled Range.

results are shown in Figure 3.4. The solution of Poisson's equation predicts a hole density variation that is as sharp as the Si/Ge interface. The results of the combined Poisson-Schrödinger equations predict a more realistic hole distribution which varies more gradually. The hole population calculated by solving the combined Poisson-Schrödinger equations is both qualitatively and quantitatively different than the result obtained by solving Poisson's equation alone.

The quantum mechanical effects of the superlattice can be confirmed by examining the hole wavefunction. Shown in Figure 3.5 are three distinct

wavefunctions for this three layer superlattice structure. In the simplest sense, the wavefunction indicates the positional dependence of the hole distribution — the square of the wavefunction (or $\psi\psi^*$ specifically) equals the probability of finding a hole in that location. These specific wavefunctions correspond to the three heavy hole energy levels that are confined in the superlattice quantum well. Not shown is the one wavefunction corresponding to the confined light hole energy level. Quantum interference is evident by the overlapping areas of the wavefunctions, and that the wavefunctions have different shapes. At this specific energy, only these three heavy and one light hole energy levels are bound. The Schrödinger solver only finds subbands corresponding to bound states. At higher $|V_G|$, the number of occupied hole states in the quantum wells increases.

Application of a gate voltage has an effect on the conduction and valence bands and the hole population. Figure 3.6 illustrates the effect of the gate voltage on the energy bands. It can be seen that the region of the bands nearest the gate are affected the most.

In Figure 3.7, the hole densities of the superlattice and the single quantum well are overlaid for comparison. The total integrated Ge content is conserved with a $\text{Si}_{0.4}\text{Ge}_{0.6}$ alloy forming the single quantum well, as shown in Figure 3.2. The hole density of the superlattice structure is higher near the uppermost Ge layer in comparison to the single quantum well at the same depth (≈ 11.0 nm). (It can also be seen that the top Ge layer in the

superlattice has the most significant sub-surface hole population.) This effect is shown quantitatively by the cumulative sum of the hole populations. This sum is effectively an integration of the hole density which gives an effective hole sheet charge, measured in units of carriers/cm². Although this difference is slight, this hole distribution in the superlattice is more favourable than in the alloy, since it is desired to maximize hole density in the sub-surface channel and minimize hole density near the oxide interface.

Analysis at various gate voltages of hole densities of the superlattice and the single quantum well are summarized in Figure 3.8. Shown are the hole populations of the surface channel and the sub-surface channel as a function of gate voltage. In this analysis, the surface channel population is defined to be the cumulative sum from the surface to 7.0 nm, and the sub-surface channel population is defined as the cumulative sum from 7.0 nm to 17.0 nm. (The total population is, of course, the sum of the two.) Crossover is defined as the point for which the hole populations of the surface and sub-surface channels equal. Crossover is characterized by both the gate voltage at crossover and the sheet charge in the surface and sub-surface channels. The objective is to maximize the crossover voltage, and to maximize the sheet charge of sub-surface holes at crossover.

3.2.2 Comparison of $(\text{Si}_{12}\text{Ge}_3)_8$ with Other $\text{Si}_{0.8}\text{Ge}_{0.2}$ Profiles

The $(\text{Si}_{12}\text{Ge}_3)_8$ superlattice is less rich in germanium than the $(\text{Si}_7\text{Ge}_7)_3$ superlattice, having $\approx 20\%$ Ge content. This superlattice was compared to three other SiGe alloys of the same average Ge content (20%), heterostructure thickness (15 nm), and depth, ie. cap thickness of 10 nm. The first SiGe alloy has a constant 20% Ge content — a rectangular profile. The second alloy has a positively graded trapezoidal profile, similar to the design of Verdonckt-Vandebroek *et al.* The trapezoidal profile has 25% Ge at the top of the heterostructure, linearly ramped to 15% at the bottom. The third alloy has a positively graded triangular profile, from 40% to 0%, similar to the design favoured by Voinigescu. Figures 3.9 and 3.10 show the conduction and valence band structure and hole distribution of all four structures respectively.

Shown in Figure 3.10 is the hole density as a function of depth, and the effective hole sheet charge. It is desired to minimize hole sheet charge in the surface channel, and maximize hole sheet charge in the sub-surface channel. Of the four structures investigated, the triangular profile shows the best confinement, followed by the superlattice, then trapezoidal and finally the rectangular profile. The level of confinement is very strongly influenced by the distribution of Ge in the sub-surface channel.

The voltage and hole sheet charge at crossover are quantitative compar-

isons of channel confinement. It is desired to maximize the absolute value of the crossover voltage, but more importantly to maximize hole sheet charge at crossover (ie. maximize hole sheet charge in sub-surface channel). These values have been determined for the four structures, and are presented in Table 3.1. Also included in the table is the channel hole sheet density in the surface and sub-surface channels (which are equal, by definition of crossover).

Ge profile	crossover voltage (Volts)	hole sheet density in channel (10^{12} cm^{-2})
triangular	-1.2	0.80
superlattice	-0.80	0.55
trapezoidal	-0.58	0.23
rectangular	-0.41	0.075

Table 3.1: Crossover voltages of four SiGe profiles, each with 20% average Ge content across a 15 nm thick heterostructure.

Figures 3.11 and 3.12 show the heavy and light hole wavefunctions of the superlattice and trapezoidal structures. The eight Ge layers of the superlattice are evident in the hole wavefunctions. There is also a greater confinement to the sub-surface channel in the superlattice compared to the trapezoidal profile alloy.

3.2.3 Discussion on Hole Density in Si/Ge Superlattice and Single Ge layers

It can be seen from hole density and sheet charge graphs that the most significant sub-surface hole populations in superlattices reside in the top Ge layers.

Further modelling investigated the $(\text{Si}_7\text{Ge}_7)_p$ superlattices, for $p = 1, 2$, and 3. ($p = 1$ corresponds to a single Ge layer.) Only a minor increase was seen in the integrated hole population in $p = 3$ superlattice compared to the $p = 1$ single Ge layer. As can be seen in Figure 3.7, the integrated hole population, when viewed on a logarithmic scale, is insignificantly affected by the sheet charge in the bottom two Ge layers. This result suggests that significant advantage can be gained by using a single Ge_n buried layer, in place of a superlattice or a thick $\text{Si}_{1-x}\text{Ge}_x$ alloy heterostructure. This result also suggests that a significantly lower integrated Ge content can be used without significant disadvantage.

However, this result is dependent on the thickness of the Ge_n layer. In the $(\text{Si}_{12}\text{Ge}_3)_8$ superlattice, the sheet charge in the secondmost top Ge layer does contribute a significant amount to the integrated hole population. In Figure 3.10, the sheet charge in the second Ge layer is approximately 50% of the sheet charge in the top Ge layer. Sheet charge in lower Ge layers becomes insignificant.

For these reasons, the experimental component of this thesis investigated

sub-surface $(\text{Si}_7\text{Ge}_7)_p$ superlattices, for $p = 1, 2$ and 3 . This work is presented in the next chapter.

3.2.4 Capacitance vs. Voltage Modelling

The capacitance of a sub-surface $(\text{Si}_7\text{Ge}_7)_3$ superlattice MOSH structure was determined. Several input files with different values of the Schottky barrier height (hence gate voltage) were numerically solved with the Poisson-Schrödinger solver. The integrated minority charge was determined for each bias condition. As capacitance is defined as $\partial Q / \partial V_G$, the difference between these individual points gave the capacitance. The results of the numerical modelling are shown in Figure 3.13.

Since only the minority (ie. hole) charge was calculated, only the inversion region of the CV curve is shown in Figure 3.13. The accumulation and depletion regions were not determined. The inversion region of the C-V curve shows the behaviour of the capacitance rising from C_{min} (with increasing $|V_G|$) to C_{ox} , due to the inversion charge. The threshold voltage of the heterostructure V_{TH} corresponds to the formation of an inversion layer in the sub-surface channel. The value of the capacitance is referred to as $C_{plateau}$. Only at higher voltages of $|V_G|$ does the surface channel become inverted, at V_{TS} , at which the capacitance takes the value of C_{ox} . This behaviour has been previously modelled by Garone [GVS91a] and Voinigescu [VIL+94] as discussed in Chapter 2.

It is clear that the capacitance does not rise to the value of C_{ox} ($\approx 3.2 \text{ fF } \mu\text{m}^{-2}$) at low values of $-|V_G|$, but, as expected, a plateau region exists. In this case, $V_{TH} \approx -0.2 \text{ V}$, and $V_{TS} \approx -1.0 \text{ V}$. The plateau capacitance $C_{plateau} \approx 2.3 \text{ fF}/\mu\text{m}^2$. These values are close to the values determined by Voinigescu [VIL⁺94] for a similar structure. Experimentally, these results can be compared to quasi-static capacitance measurements.

3.2.5 Electric Field in MOSH Capacitors

The electric field reflects the distribution of charge. As discussed previously, the threshold potential and threshold voltage differ for the surface and sub-surface channels. The electric field in a depletion region is linear and dependent on the background ionized donor (or acceptor) concentration. In an inversion region, the electric field is more dependent on the minority charge.

Figure 3.14 shows the electric field in a MOSH capacitor for three gate voltages. The sub-surface channel is a 5 nm thick $\text{Si}_{0.4}\text{Ge}_{0.6}$ heterostructure with the top heterointerface 10 nm below the surface. The modelling program assumes a linear interpolation of the dielectric constant between those of bulk Si and Ge. This dielectric constant offset accounts for the discontinuity in the electric field at both the top and bottom heterointerfaces.

At lower gate voltages, the sub-surface channel is in inversion, but the surface channel is not inverted but only depleted. Only at higher gate voltages does the surface channel become inverted, which is reflected in the electric

field. The electric field changes slope at 30 nm due to the higher doping level at this depth.

3.3 Interface Trapped Charge

Interface trapped charge Q_{it} is ubiquitous in Si/SiO₂ interfaces as well as in heterojunctions. Charges are trapped at such interfaces due to the interruption of the periodic lattice structure.

The energy levels of interface traps (also known as fast surface states) exist within the forbidden gap of a semiconductor. An interface trap can be considered a donor if it can become neutral or positive by donating (losing) an electron, or an acceptor if it accepts an electron. Interface trap energy levels move with the conduction and valence bands when a voltage is applied. A change of charge in the interface trap occurs when it crosses the Fermi level. Consequently, interface traps contribute to the capacitance. The interface trap density D_{it} can be determined by capacitance measurement [Sze81].

The subthreshold current in a MOSFET is defined as the drain current when the gate voltage is below the threshold voltage. When a MOSFET is used as a switch in digital logic or memory applications, the subthreshold current determines how the MOSFET turns on and off. The figure of merit used is the subthreshold swing S , where

$$S \equiv \ln 10 \cdot \frac{dV_G}{d(\ln I_D)} \quad (3.7)$$

In the case that

$$2 \frac{\epsilon_s}{\epsilon_i} \frac{t_{ox}}{L_D} \gg \frac{C_D}{C_i}, \quad (3.8)$$

where L_D is the Debye length and C_D is the depletion layer capacitance, then

$$S \simeq \frac{kT}{q} \ln 10 \cdot \left(1 + \frac{C_D}{C_i} \right) \quad (3.9)$$

according to [Sze81].

The effect of interface traps becomes apparent when the capacitance due to interface traps, $C_{it} = qD_{it}$, is on the order of C_D . These capacitances act in parallel, resulting in

$$S \simeq \frac{kT}{q} \ln 10 \cdot \left(1 + \frac{C_D + C_{it}}{C_i} \right). \quad (3.10)$$

Interface trap density can be related back to the transconductance (in the subthreshold region) since

$$\frac{1}{g_m} = \frac{S}{\ln 10} \frac{1}{I_D} \quad (3.11)$$

which obviously leads to

$$g_m = \frac{qI_D}{kT} \left(\frac{C_i}{C_i + C_D + C_{it}} \right). \quad (3.12)$$

It is clear that maintaining low interface trap density is necessary to take advantage of a higher transconductance gained from a SiGe sub-surface channel. Qualitatively, the effects of interface trap density on the transconductance above threshold is expected to be similar.

Poisson and Schrodinger Carrier Densities

Figure 3.4: Hole and electron densities as calculated by the Poisson equation alone and combined Poisson-Schrödinger equations. The electron distribution calculated by Poisson-Schrödinger equations does not exceed 10^{10} cm^{-3} in this region.

Si/Ge Superlattice Wavefunctions

Figure 3.5: Wavefunctions of Interfering Quantum Wells (Superlattice). Structure is as in previous figure.

Effect of Gate Voltage on Energy Bands

Figure 3.6: Dependence of Conduction and Valence Bands on Applied Gate Voltage

Hole Density of SL and SQW

Figure 3.7: Hole Density of Si/Ge Superlattice and Si_{0.4}Ge_{0.6} Well with -1.70 gate voltage.

Crossover Voltage

SL vs. SQW

Figure 3.8: Crossover voltage of Si/Ge superlattice (SL) and $\text{Si}_{0.4}\text{Ge}_{0.6}$ single quantum well (SQW) with conserved integrated Ge content. Solid lines represent superlattice, dashed lines represent SiGe single quantum well. The crossover voltage for both structures is -2.25 V. Total hole population is the sum of the surface and sub-surface channel populations.

Band Diagram of Four Ge profiles

Figure 3.9: Band Diagram of superlattice, rectangular, trapezoidal and triangular Ge profiles in the sub-surface channel.

Hole Densities of Four Ge Profiles

Figure 3.10: Hole densities of superlattice, rectangular, trapezoidal and triangular Ge profiles in the sub-surface channel. All have same total Ge content. See text for details.

$(\text{Si}_{12}\text{Ge}_3)_8$ Hole Wavefunctions

-0.26 V gate voltage

Figure 3.11: $(\text{Si}_{12}\text{Ge}_3)_8$ Hole Wavefunction

Hole Wavefunctions

Figure 3.12: Trapezoidal $\text{Si}_{0.8}\text{Ge}_{0.2}$ Hole Wavefunctions

Capacitance vs. Voltage

minority charge, inversion region

Figure 3.13: Capacitance vs. Voltage modelling results.

Electric Field in MOSH capacitors

Figure 3.14: Electric field in MOSH capacitors

Chapter 4

Fabrication and Characterization

4.1 Substrates

The starting material for these experiments was n-type silicon with 8 - 12 $\Omega\cdot\text{cm}$ resistivity (corresponding to doping level $\approx 5 \cdot 10^{14} \text{ cm}^{-3}$). Three wafers were grown epitaxially by MBE by J.-P. Noël at the National Research Council. A wafer surface passivation before growth was done with 5% hydrofluoric acid. The growth temperature was 500°C, the total pressure during growth was 2 (10^{-8}) torr, with the background gas consisting mostly of hydrogen, with a CO partial pressure of 10^{-10} torr. The silicon growth rate was 0.2 nm/s. An undoped buffer layer 30 nm thick was first grown on the silicon substrate. (Background doping was expected to be $\approx 10^{14} \text{ cm}^{-3}$

p-type in this layer.) The number of Ge layers, each ~ 1.0 nm thick, is indicated in Table 4.1. Multiple Ge layers are separated by Si layers, each

Wafer Number	Number of Periods	Label
FET 1501	3	C
FET 1502	1	A
FET 1503	2	B

Table 4.1: Number of Periods p in $(\text{Si}_7\text{Ge}_7)_p$ superlattices.

~ 1.0 nm thick. Lastly, a Si cap was grown above the superlattice. The original specifications called for a cap thickness of 15 nm, but further Transmission Electron Microscopy (TEM) measurements showed the thickness was approximately 18 nm. The original process flow called for growth of the gate oxide in a wet oxygen ambient. It was anticipated that ≈ 5.0 nm of the silicon cap would be lost due to silicon dioxide growth and RCA cleaning. The structures were intended to closely resemble those simulated in the modelling described in the previous chapter.

TEM measurements of sample FET 1501 confirmed Ge and Si superlattice layer thicknesses of 1.08 ± 0.06 nm. The bottom-most Ge layer interface was sharp, the next Ge layer interface was less sharp, and the topmost Ge layer interface was diffused. This top Ge layer shows signs of stress. Photomicrographs of this sample are included in Figure 4.1. Using the interplanar distance of pseudomorphic Ge on Si of 0.146 nm, the Ge layers are more precisely 7.4 monolayers thick.

4.2 Test Device Design

A test device layout was created, using Ledit version 5. A Mead-Conway type design rule convention was followed where appropriate. The total size of the layout on the wafer was 3 mm square.

The layout includes eighteen large capacitors, $300\text{ }\mu\text{m} \times 300\text{ }\mu\text{m}$ in size, and eighteen smaller capacitors, $10\text{ }\mu\text{m} \times 10\text{ }\mu\text{m}$ in size. Additional test devices were included to permit additional uses for this layout.

Several transistors were designed, having different gate length and gate width combinations. The minimum gate length was $2.5\text{ }\mu\text{m}$. Transistor designs included both enclosed and open geometries.

Mask layers include source and drain regions for MOS(H)FETs, device well, metal contact holes, and metal. A p-guard implant mask was also designed, but not used. The purpose of this mask was to allow for an additional implant to prevent surface inversion.

A diagram of the circuit layout is included in Appendix C.

4.3 Process Flow

Multiple gate oxide and cap layer thicknesses were desired, firstly to investigate effects of layer thickness, and secondly to avoid potential problems arising from excessively thin layers. It is widely thought that very thin oxide layers are stressed due to lattice mismatch between Si and SiO_2 . Micropores

may exist in thin oxides, which may result in the gate material being in direct contact with the silicon.

An array of gate oxide and cap thicknesses was produced. This array is shown in Table 4.2. A nomenclature for wafer pieces according to both wafer

		gate oxide thickness	
		12 nm	20 nm
Si cap thickness	10 nm	2	4
	12.5 nm	1	3

Table 4.2: Array of gate oxide and cap thicknesses in sample nomenclature.

label in Table 4.1 and the gate oxide / cap array was created. For example, C4 would have three Ge layers in the superlattice, a cap thickness of 10 nm, and a gate oxide thickness of 20 nm.

The limited thermal budget the superlattice can withstand precluded the thermal growth of the gate oxide in a wet oxygen ambient originally planned. It was therefore necessary to remove a thickness of the silicon cap layer equal to that which would have been consumed during gate oxidation. A low-rate isotropic silicon etch was developed for this task.

The low-rate isotropic silicon etch used the ingredients of a polysilicon etch but with significantly lesser amounts of HF. Positive photoresist (PR) was spun on wafer test pieces, which were then exposed under a mask. Etch times of ten minutes were used. After the etch, the PR was removed. Etch rates were estimated using a Dektak surface profilometer to measure depth.

The etch rate was increased by adding HF. The Ge layers were clearly visible when etching reached the superlattice depths. Germanium was seen a dark shade of grey in contrast to the light grey of surrounding silicon. This etch is described with the process flow.

The low temperature metal anneal also served as an anneal for the oxide. However, this temperature (400°C) is unusually low for an oxide anneal. A high density of trapped interface charges usually results.

The complete process flow is included in Appendix D. Due to technical problems, only a subset of the above mentioned array has been fabricated.

4.4 Capacitance Measurements

Capacitance measurements were taken using the Keithley Package 82 system. This system made simultaneous quasistatic and high frequency CV measurements, avoiding the problems inherent in sequential voltage sweeps. Sequential measurements introduce voltage stress from sweeping the voltage twice which can cause misalignment of the CV curves [NB82]. Included in this system was a Keithley 590 100 kHz CV Analyzer and a Keithley 595 Quasistatic CV Meter. The expected error from these capacitance measurements is within 2%.

Shown in Figure 4.2 are capacitance-voltage curves for a $500\mu\text{m} \times 300\mu\text{m}$ capacitor on wafer A2. Both quasi-static and high frequency (100 kHz) curves are shown. The quasi-static curve shows a plateau below C_{ox} in the inversion

region. The plateau is due to an inversion layer in the sub-surface channel, without an inversion layer in the surface channel. This effect was modelled using the Poisson-Schrödinger solver (Figure 3.13) in Chapter 3. Quantitatively, the measured value of $C_{ox} = 3.2 \text{ fF}/\mu\text{m}^2$, which compares well to the modelled value of $2.8 \text{ fF}/\mu\text{m}^2$ for a similar structure. The values of $C_{plateau}$ for the measured and modelled structures are both $\approx 2.3 \text{ fF}/\mu\text{m}^2$. The differences between the values of (oxide) capacitance are attributed to variation in gate oxide and cap layer thicknesses and substrate doping between the modelled structure and the fabricated device. Different gate materials (p^+ poly versus aluminum) explain the voltage offset.

Importantly, the quasi-static capacitance-voltage curve confirms hole population in a single, thin pseudomorphic Ge layer. This amount of Ge is significantly less than the integrated Ge content of other studies that typically used heterostructures 10 – 15 nm thick, with 20% – 40% Ge alloys.

The density of interface traps in the same capacitor on wafer A2 was measured and is illustrated in Figure 4.3. The interface trap density D_{it} is rather high for this, and other, capacitors.

An identically sized capacitor on A3 was measured. The quasi-static C-V curve (not shown) shows a less well-defined V_{TH} and V_{TS} . Whereas C_{min}/C_{ox} is less than one third in A2, this ratio is $\approx 1/2$ for A3. However, the plateau for A3 extends wider than for A2. Capacitance measurements suggest $t_{ox} = 18.5 \text{ nm}$.

Figures 4.4 and 4.5 are C-V measurements on wafers B2 and C2 respectively. (Along with A2, these three samples differ only in number of Ge layers — gate oxide and cap thicknesses are constant.) There are no significant differences between A2 and B2, although the quasi-static C-V curve of B2 has a slightly lower plateau level than A2. According to the analysis by Voinigescu [VIL⁺94], this effect suggests that the cap layer thickness in B2 is greater than in A2. Equivalently, this result can also be interpreted that the centroid of the hole population is lower in B2, which suggests significant hole population in the second (bottom) Ge layer.

The quasi-static C-V curve of C2 has a higher C_{min} than both A2 and B2, and also shows an anomalous capacitance at $V_g < -3$ V. The latter effect is likely due to current through the oxide layer. In this (A,B,C)2 series, t_{ox} was determined from accumulation capacitance to be 11.7 ± 0.3 nm. Conventional analysis of the C-V curves determine $N_D = (1.4 \pm 0.4)10^{15}\text{cm}^{-3}$ from the value of C_{min} .

4.5 Analysis and Discussion

Capacitance measurements on samples A1, A2 and B2 only are of sufficient quality to permit analysis. Low-frequency capacitance shows the threshold voltage of the heterojunction channel V_{TH} and the threshold voltage of the surface channel V_{TS} . The difference of these voltages is $|\Delta V_T|$. The value of the plateau capacitance $C_{plateau}$ can also be estimated from the capacitance

measurement. A simplistic estimation of the sub-surface channel charge is

$$Q_H = C_{\text{plateau}} \cdot |\Delta V_T| \quad (4.1)$$

and the sheet charge density can be determined by dividing by the area of the capacitor ($300 \mu\text{m} \times 300 \mu\text{m}$). This analysis is summarized in Table 4.3. Note that the errors for $|\Delta V_T|$ and C_{plateau} are quite high, which makes quan-

Sample	$ \Delta V_T $ $\pm 0.1 \text{ V}$	C_{plateau} $\pm 10 \text{ pF}$	Sheet Charge $\pm 10\% \text{ cm}^{-2}$
A1	2.1	215	$3.1 (10^{12})$
A2	2.0	210	$2.9 (10^{12})$
B2	1.9	195	$2.6 (10^{12})$

Table 4.3: Sub-surface channel hole sheet charge determined from capacitors.

titative comparisons between the capacitors dubious. However, the average value obtained for the hole sheet charge of $\approx 3 (10^{12}) \text{ cm}^{-2}$ is within very good agreement of theoretical modelling presented in the previous chapter. (Recall theoretical predictions of sub-surface channel hole sheet densities of the $\approx 2 (10^{12}) \text{ cm}^{-2}$ for similar structures).

It was mentioned on page 54 that the density of interface traps affects the transconductance. For equation 3.9 to be true, the condition in equation 3.8 must be met. This condition can be re-written as

$$2 \frac{\epsilon_s}{L_D} \gg C_D \quad (4.2)$$

since $C_i = \epsilon_i/t_{\text{ox}}$. For $N_B = 10^{15} \text{ cm}^{-2}$ (as found from measurement), the Debye length L_D equals $1.31 (10^{-5}) \text{ cm}$, hence this condition requires $C_D \ll$

160 nF/cm². In comparison, C_i equals 290 nF/cm⁻², and if we take $D_{it} \approx 10^{12}/\text{cm}^2\cdot\text{eV}$, then $C_{it} \approx 160 \text{ nF/cm}^{-2}$. The condition in equation 4.2 is not met. Obviously, the density of interface traps is significant and will adversely affect transconductance. Interface traps can be reduced by low temperature (450°C) hydrogen annealing.

Figure 4.1: TEM of $(\text{Si}_7\text{Ge}_7)_3$ superlattice.

Figure 4.2: Capacitance-Voltage curves, wafer A2

Figure 4.3: Density of interface traps in A2 capacitor

Figure 4.4: Capacitance-Voltage curves. wafer B2

Figure 4.5: Capacitance-Voltage curves. wafer C2

Figure 4.6: Capacitance-Voltage curves, wafer A1

Chapter 5

Conclusion

The research presented in this thesis can be understood as an intermediate phase to fully investigating the feasibility of a $(\text{Si}_n\text{Ge}_m)_p$ superlattice sub-surface channel MOSHFET.

The objective of SiGe metal-oxide-semiconductor-heterostructure field-effect-transistors (MOSHFETs) is to maximize transconductance by increasing hole mobility in a sub-surface channel. Theoretical understanding of pseudomorphic $\text{Si}_{1-x}\text{Ge}_x$ on (100) Si as well as results of previous SiGe MOSHFET designs suggest very high Ge mole fractions are required to obtain significant increases in performance. Only Ge rich strained SiGe layers offer significant advantages in mobility and carrier concentration. The unique aspect of the Si/Ge superlattice sub-surface channel p-MOSHFET is the presence of pseudomorphic Ge layers, albeit thin layers. This design is distinguished from other SiGe MOSHFET designs which involved various

profiles of $\text{Si}_{1-x}\text{Ge}_x$ alloys (in which x is not necessarily constant within the heterostructure).

This thesis presented modelling of several MOSH structures using self-consistent solutions of Poisson's and Schrödinger's equations. The inversion hole distribution in surface and sub-surface channels was of particular interest. The crossover point, defined by equal surface and sub-surface hole populations, is characterized by both applied gate voltage and channel hole population. Several structures were compared, each having 20% average Ge content in a 15 nm thick heterostructure, the top of which was 10 nm below the surface. Other characteristics, such as doping, were held constant. It was shown that Ge distribution has a significant effect on the crossover point. The superlattice structure had a higher crossover point than both rectangular and trapezoidal Ge profiles, but lower than the triangular profile. Also evident was that only the top Ge layers in $(\text{Si}_n\text{Ge}_m)_p$ superlattices have significant hole sheet charge, suggesting significantly fewer periods, hence lower Ge content, could be used without disadvantage. Capacitance vs. gate voltage characteristics due to minority charge (holes) in the inversion region were also determined. The existence of a plateau in the inversion region was seen. This plateau is due to an inversion layer in the sub-surface channel but without an inversion layer in the surface channel. These results compared well to previous theoretical investigations of MOSH capacitance-voltage behaviour.

Fabrication of $(\text{Si}_7\text{Ge}_7)_p$ superlattice MOSH capacitors was undertaken

for this thesis. Parameters included number of periods p in the superlattice, gate oxide thickness, Si cap layer thickness, and capacitor size. Quasistatic capacitance-voltage measurements clearly showed a plateau in the inversion region. This plateau is due to the onset of inversion in the sub-surface channel at lower $|V_G|$ than inversion in the surface channel. Values of oxide capacitance and plateau capacitance compare well to the modelling in this thesis. This experimental evidence confirms predictions of hole population in thin, pseudomorphic Ge layers.

Fabrication of MOSHFETs would involve processing steps beyond those of MOSH capacitors. Si/Ge superlattice MOSHFETs were not fabricated during the course of research for this thesis. Previous studies have shown that the thermal budget which Si/Ge superlattices can withstand is extremely limited. The need to anneal source/drain implant damage in a MOSHFET therefore presents a very difficult processing problem.

More research into Si/Ge superlattice MOSH structures can be investigated without fabricating MOSHFETs. Studies into hole mobility in these structures would be desirable. A MOSH Hall device could be used to measure Hall mobility. Further studies using the Imiewski-Voinigescu analysis technique for MOSH capacitors could provide more accurate values of V_{TH} and V_{TE} , and determine the cap layer thickness, the valence band offset and sub-surface hole sheet charge. Another open question is whether the critical thickness of a pseudomorphic Si/Ge superlattice varies from an alloy

of the same average Ge content, in which both theoretical and experimental investigations would be justified. The energy gap of the structure could be measured using photocurrent spectroscopy. This investigator also leaves capacitors with different gate oxide and Si cap layer thicknesses near completion.

2 of/de 2

PM-1 3½"x4" PHOTOGRAPHIC MICROCOPY TARGET
NBS 1010a ANSI/ISO #2 EQUIVALENT

PRECISIONSM RESOLUTION TARGETS

Appendix A

A Plethora of Names

Like most instances in which many names are used to describe a single class of items, the SiGe MOSFET has a history of cousins that once shared names.

MESFET — **M**etal **S**emiconductor **F**ield **E**ffect **T**ransistor. A metal semiconductor rectifying contact is used for the gate electrode. The first MESFETs were fabricated using a GaAs epitaxial layer on semi-insulating GaAs substrates and remain the most common type of MESFET, although others have been made with Si and InP.

MOS — **M**etal **O**xide **S**emiconductor (or **S**ilicon). A specific case of the metal insulator semiconductor system. Amongst all semiconductor materials, only silicon has a technologically useful insulator, namely silicon dioxide (“oxide”). Hence MOS is generally understood to specifically refer to the Si/SiO₂ system. (The “metal” is often replaced by heavily doped conducting polycrystalline silicon, referred to as “poly”).

HEMT — High Electron Mobility Transistor. The name HEMT has historically applied to GaAs n-type field-effect-transistors. However, due to the absence of an adequate insulator for the GaAs system, these were necessarily MESFETs. Due to the Schottky contact, only a low positive gate voltage could be applied, hence requiring a low threshold voltage.

MODFET — MODulated-doping Field Effect Transistor. As GaAs HEMTs evolved, a delta doping layer was utilized to alter the threshold voltage. This technique of modulated doping has gained favour in some SiGe MOSFET circles, although the term MODFET historically implied Schottky metal-semiconductor gate contacts.

MODMOS — MODulated-doping MOS. Although MOS refers specifically to the Si/SiO₂ system, modulated doping can be used in SiGe heterostructure or standard Si MOSFETs, so this name is ambiguous. Additionally, modulated doping is not a requirement for SiGe heterostructure MOSFETs.

HFET — Heterojunction Field Effect Transistor. This nomenclature is ambiguous between SiGe/Si and GaAs/GaAlAs heterostructure transistors.

MOSHFET -- Metal Oxide Semiconductor Heterostructure Field Effect Transistor. This designation removes ambiguity between GaAs and SiGe systems, explicitly mentions the heterostructure, does not refer to modulated doping, is a logical extension of HFET, and is pronounceable.

Appendix B

Poisson–Schrödinger Solving Algorithm

The Poisson equation in one dimensional is

$$\frac{d}{dx} \left(\epsilon_s(x) \frac{d}{dx} \right) \phi(x) = -\frac{q}{\epsilon_0} [N_D(x) - N_A(x) + p(x) - n(x)] \quad (\text{B.1})$$

where ϵ_s is the relative dielectric constant, ϕ is the electrostatic potential, N_A and N_D are the ionized acceptor and donor concentrations respectively, and p and n are the hole and electron density distributions.

The single particle, time independent one dimensional Schrödinger equation is

$$-\frac{\hbar^2}{2} \frac{d}{dx} \left(\frac{1}{m^*(x)} \frac{d}{dx} \right) \psi(x) + V(x)\psi(x) = E\psi(x), \quad (\text{B.2})$$

where ψ is the wave function, E is the energy, V is the potential energy, $\hbar$ is Planck's constant divided by 2π , and m^* is the effective mass of the particle.

To find the hole distribution in the valence band, one may set the potential energy V to be equal to the valence band energy. In a quantum well of arbitrary potential energy profile, the potential energy and electrostatic potential are related by

$$V(x) = q\phi(x) + \Delta E_v(x) \quad (\text{B.3})$$

where ΔE_v is the pseudopotential energy due to the band offset at the heterointerface. The wave function is related to the hole density by

$$p(x) = \sum_{k=1}^m \psi_k^*(x) \psi_k(x) p_k \quad (\text{B.4})$$

where m is the number of bound states, and p_k is the hole occupation for each state, which can be expressed by

$$p_k = \frac{m^*}{\pi \hbar^2} \int_{-\infty}^{E_k} \frac{1}{1 + e^{(E_F - E)/kT}} dE \quad (\text{B.5})$$

where E_k is the eigenenergy.

The program uses an iteration procedure to obtain self-consistent solutions for the Poisson and Schrödinger equations. Beginning with an initial potential $V(x)$, the wave functions and their corresponding eigenenergies are used to calculate the carrier density distribution using Eqs. B.4 and B.5. The computed $p(x)$ and a given acceptor concentration are used to calculate $\phi(x)$ by Eq. B.1. The potential energy $V(x)$ is recalculated with Eq. B.3. Further iteration yields the self-consistent solutions for $V(x)$ and $n(x)$. The reader is referred to [TSCH90] for further details of the numerical method.

B.1 Example Input File

```
#Eg105Nd17
```

```
# no applied voltage on Schottky barrier
```

```
# superlattice of alternating Si and pure Ge layers
```

```
# 3 monolayers, each 10 Angstroms thick
```

```
# with 1.05V Schottky barrier, used to simulate MOS gate voltage
```

```
start regions
```

```
Si      0  0   1um  100  Nd=1e15
```

```
SiGe    0  100  1um  110  Nd=1e15 x=0.99 Eg=0.55
```

```
Si      0  110  1um  120  Nd=1e15
```

```
SiGe    0  120  1um  130  Nd=1e15 x=0.99 Eg=0.55
```

```
Si      0  130  1um  140  Nd=1e15
```

```
SiGe    0  140  1um  150  Nd=1e15 x=0.99 Eg=0.55
```

```
Si      0  150  1um  200  Nd=1e15
```

```
Si      0  200  1um  300  Nd=1e15
```

```
Si      0  300  1um  3000 Nd=1e17 dy=60
```

```
stop regions
```

```
bc 0 0 1um 0 schottky=1.05 v1
```

```
v1 0.0
```

```
temp=300
```


1D

schrodinger 0 0 10 300

fullyionized

dx=0.1um

dy=2

Appendix C

Diagram of Test Device Layout

The test device layout is shown in Figure C.1. Five masks were made for this layout: device well, p-guard implant (not used), source/drain regions, metal, and metal contact.

Figure C.1: Test Device Layout

Appendix D

Process Run Sheet

SiGe capacitors

STARTING MATERIAL:

FET1501 (3 Ge layers): C1, C2, C3, C4, C5

FET1502 (1 Ge layer): A1, A2, A3, A4, A5

FET1503 (2 Ge layers): B1, B2, B3, B4, B5

Note: pieces A5, B5 and C5 are to be used in case of breakage.

1. SILICON ETCH

- On sample (A,B,C)(1.3) etch ≈ 5 nm of Si from the surface of the wafers, using low rate silicon etch (20 s).
- On sample (A,B,C)(2.4) etch ≈ 7.5 nm of Si from the surface of the wafers, using low rate silicon etch (30 s).

2. FIELD OXIDE DEPOSITION

The field oxide stip will be done in two groups to test the RCA procedure. The first group contains A1, B1, C1 and A2. The remainder goes to the second group.

- Caro's acid, 80°C, 2 min, DI rinse, no HF dip
- RCA clean (new recipe, modified (see below))
- Deposit PECVD SiO₂ (LOTOX), target: 200 nm
 - Program S105-C018 (1.8 sccm SiH₄, 35 sccm N₂O, 960 He, 1.95 Torr, 390°C, 20W)
 - Condition for 40 min
 - Do one test run first

3. DEVICE WELL LITHOGRAPHY (PE) (mask CU-164-03)

- IPR 504, prime, spin, prebake, expose, postbake
- etch in siloxide etchant until Si exposed
- strip PR in Caro's acid

4. GATE OXIDATION

- modified RCA clean
- Deposit PECVD SiO₂

- Program S105-C018 (1.8 sccm SiH₄, 35 sccm N₂O, 960 He, 1.95 Torr, 390°C, Power=50W)
- Condition for 40 min
- Do one test run first
- Samples (A,B,C)(1,2), target thickness: 12 nm, thickness measured: 11 nm
- Samples (A,B,C)(3,4), target thickness: 20 nm, thickness measured: 20.5 nm

5. ALUMINUM GATE DEPOSITION

thermal evaporation Al

target thickness: 100 nm

6. GATE POLY ETCH (mask CU-161-05)

- apply, prebake, expose, develop, postbake POSITIVE PR
- etch in phosphoric acid 60°C until Al removed, about 1 min
- strip PR in Microstrip 2001, 1 hour rinse

7. BACK METALLIZATION

e-beam evaporation

target thickness: 0.5 μm actual thickness: μm

8. METAL ANNEAL

tube temperature: 400°C 15 min anneal H₂

D.1 Modified RCA Clean

1. RCA1: 20:1:4 H₂O:NH₄OH:H₂O₂ 70°C, 5 min
2. HF (1:100): 30 seconds
3. RCA2: 6:1:1 H₂O:HCl:H₂O₂ 80°C, 5 min
4. HF (1:100): 30 seconds

(comments; - step 1) a standard 5:1:1 at 80 C removes about 2 nm Si -
modified step 2) hardly removes any Si)

D.2 Low Rate Silicon Etch

- 150 mL HNO₃, 50 mL H₃PO₄, 75 mL H₂O, 5 mL 10% HF

on p-type Si test wafers, etch rate $\approx$ 10 nm/min

on n-type SiGe edge pieces, etch rate $\approx$ 15 nm/min

This is a modified polysilicon etch with much less HF.

Bibliography

- [BFF⁺84] J. C. Bean, L. C. Feldman, A.T. Fiory, S. Nakahara, and L.K. Robinson. $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ strained layer superlattice grown by molecular beam epitaxy. *Journal of Vacuum Science and Technology*, A2(2):436–440, 1984.
- [BMH58] Rubin Braunstein, Arnold Moore, and Frank Herman. Intrinsic optical absorption in Germanium-Silicon alloys. *Phys. Rev.*, 109:695–710, March 1958.
- [dWM86] C. G. Van de Walle and Richard M. Martin. Theoretical calculations of heterojunction discontinuities in the Si/Ge system. *Phys. Rev. B*, 34(8):5621, 1986.
- [GC74] U. Gnutzmann and K. Clausecker. Theory of direct optical transitions in an optical indirect semiconductor with a superlattice structure. *Appl. Phys.*, 3:9, 1974.

- [GVS91a] P. M. Garone, V. Venkataraman, and J. C. Sturm. Hole confinement in MOS-gated $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ Heterostructures. *IEEE Electron Dev. Lett.*, 12(5):230-2, May 1991.
- [GVS91b] P.M. Garone, V. Venkataraman, and J. C. Sturm. Mobility enhancement and quantum mechanical modeling in $\text{Ge}_x\text{Si}_{1-x}$ channel MOSFETs from 90 to 300 K. In *IEDM 1991*, pages 29-32. IEEE, 1991.
- [GVS92] P.M. Garone, V. Venkataraman, and James C. Sturm. Hole mobility enhancement in MOS-gated $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ heterostructure inversion layers. *Elcc. Dev. Lett.*, 13(1):56-8, January 1992.
- [HSS89] J.M. Hinckley, V. Sankaran, and J. Singh. Charged carrier transport in $\text{Si}_{1-x}\text{Ge}_x$ pseudomorphic alloys matched to Si - strain-related transport improvements. *Appl. Phys. Lett.*, 55(19):2008, 1989.
- [IPS+89] S.S. Iyer, G.L. Patton, J.M.C. Stork, B.S. Meyerson, and D.L. Harnam. Heterojunction Bipolar Transistors using Si-Ge alloys. *IEEE Transactions on Electron Devices*, 36(10):2043-2064, October 1989.
- [Ism92] K. Ismail. *Low-Dimensional Electronic Systems - New Concepts*, volume 111 of *Springer Series in Solid-State Sciences*,

chapter Si/SiGe Quantum Wells: Transport, Properties and Possible Devices, pages 333–342. Springer-Verlag, 1992.

- [IVAS93] K. Iniewski, S. Voinigescu, J. Atcha, and C.A.T. Salama. Analytical modeling of threshold voltages in p-channel Si/SiGe/Si MOS structures. *Solid State Electronics*, 36(5):775–83, 1993.
- [Jar89] M. Jaros. *Physics and Applications of Semiconductor Microstructures*. Semiconductor Science and Technology - 1. Oxford Science Publications, 1989.
- [LBJ+93] D.J. Lockwood, J.-M. Baaribeau, T.E. Jackman, P. Aebi, T. Tylliszczak, A.P. Hitchcock, and R.L. Headrick. Influence of annealing on the interface structure and strain relief in Si/Ge heterostructures on (100) Si. *Scanning Microscopy*, 7(2):457–71, 1993.
- [LBL92] D.J. Lockwood, J.-M. Baribeau, and H.J. Labbé. Investigation of interdiffusion in $(\text{Si}_m\text{Ge}_n)_p$ superlattices and Ge_n buried layers by Raman and X-ray techniques. *Can. J. Phys.*, 70:852–9, 1992.
- [Lev55] A. Levitas. Electrical properties of germanium-silicon alloys. *Phys. Rev.*, 99:1810, 1955.

- [LPBS85] D.V. Lang, R. People, J.C. Bean, and A.M. Sergent. Measurement of the band gap of $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ strained-layer heterostructures. *App. Phys. Lett.*, 47(12):1333, 1985.
- [MB74] J.W. Matthews and A.E. Blakeslee. Defects in epitaxial multilayers I. Misfit dislocations in layers. *Journal of Crystal Growth*, 27:118–125, 1974.
- [Mey92] Bernard S. Meyerson. UHV/CVD growth of Si and Si:Ge alloys: chemistry, physics and device applications. *Proceedings of the IEEE*, 80(10):1592–1608, October 1992.
- [MN91] T. Manku and A. Nathan. Lattice mobility of holes in strained and unstrained $\text{Si}_{1-x}\text{Ge}_x$ alloys. *Elec. Dev. Lett.*, 12(12):704, 1991.
- [NB82] E.H. Nicollian and J.R. Brews. *MOS Physics and Technology*. Wiley, New York, 1982.
- [NWP+91] D.K. Nayak, J.C.S. Woo, J.S. Park, K.-L. Wang, and K.P. MacWilliams. Enhancement-mode quantum-well $\text{Ge}_x\text{Si}_{1-x}$ PMOS. *IEEE Elec. Dev. Lett.*, 12(4):154–6, April 1991.
- [PB86a] People and Bean. Band alignments of coherently strained $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ heterostructures on (001) $\text{Ge}_y\text{Si}_{1-y}$ substrates. *App. Phys. Lett.*, 48(8):538, 1986.

- [PB86b] R. People and J.C. Bean. Erratum: Calculation of critical layer thickness versus lattice mismatch for $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ strained-layer heterostructures. *Appl. Phys. Lett.*, 49(4):229, 1986. Erratum of APL 47, 322 (1985).
- [Peo85] R. People. Indirect band gap of coherently strained $\text{Ge}_x\text{Si}_{1-x}$ bulk alloys on (001) silicon substrates. *Phys. Rev. B*, 32(2):1405, 1985.
- [Sze81] S.M. Sze. *Physics of Semiconductor Devices*. Wiley Interscience, 1981.
- [TSCH90] I-H. Tan, G.L. Snider, L.D. Chang, and E.L. Hu. A self-consistent solution of Schrodinger-Poisson equations using a nonuniform mesh. *Journal of Applied Physics*, 68(8):4071-76, 15 October 1990.
- [VIL⁺94] S.P. Voinigescu, K. Iniewski, R. Lisak, C.A.T. Salama, J.-P. Noel, and D.C. Houghton. New technique for the characterization of Si/SiGe layers using heterostructure MOS capacitors. *Solid-State Electronics*, 37(8):1491, 1994.
- [VLS93] V. Venkataraman, C.W. Liu, and J.C. Sturm. Alloy scattering limited transport of two-dimensional carriers in strained $\text{Si}_{1-x}\text{Ge}_x$ quantum wells. *Appl. Phys. Lett.*, 63(20):2795-7, 15 November 1993.

- [VS92] S. Voinigescu and C.A.T. Salama. Optimal channel grading in p-type Si/SiGe metal oxide semiconductor field effect transistors (MOSFETs). *Can. J. Phys.*, 70:975–8, 1992.
- [VSNK94] S.P. Voinigescu, C.A.T. Salama, J.-P. Noel, and T.I. Kamins. Optimized Ge channel profiles in VLSI compatible Si/SiGe p-MOSFETs. *IEDM 94*, page 369, 1994.
- [VVCM⁺91a] S. Verdonckt-Vandebroek, E.F. Crabbé, B.S. Meyerson, D.L. Harame, P.J. Restle, J.M.C. Stork, A.C. Megdanis, C.L. Stanis, A.A. Bright, G.M.W. Kroesen, and A.C. Warren. High-mobility modulation-doped graded SiGe-channel p-MOSFET's. *IEEE Electron Device Letters*, 12(8):447–9, August 1991.
- [VVCM⁺91b] S. Verdonckt-Vandebroek, E.F. Crabbé, B.S. Meyerson, D.L. Harame, P.J. Restle, and J.M.C. Stork. Design issues for SiGe heterojunction FETs. In *1991 IEEE Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits*, 1991. TK7871.96 M53 I13 1991.
- [VVCM⁺94] S. Verdonckt-Vandebroek, E.F. Crabbé, Bernard Meyerson, D.L. Harame, P.J. Restle, J.M.C. Stork, and J. B. Johnson. SiGe-Channel Heterojunction p-MOSFET's. *IEEE Transactions on Electron Devices*, 41(1):90 – 101, January 1994.

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