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Smart Receiver Using Baseband Digital Signal Processing

By

Shijun Yang

A thesis submitted to the
Faculty of Graduate Studies and Research
In partial fulfillment of the requirements
For the degree of
Master of Engineering

Ottawa-Carleton Institute of Electrical Engineering,
Department of Electronics,
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and Research acceptance of the thesis

Smart Receiver Using Baseband Digital Signal Processing

Submitted by Shijun Yang (B. Eng)
in partial fulfillment of the requirements
For the degree of
Master of Engineering

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ABSTRACT

In this thesis, techniques used in baseband signal processing, modulation, and RF front end of digital wireless communication systems are investigated.

This thesis presents a novel solution for the power saving for the front-end receiver. Power dissipated by the front end is adaptively controlled by baseband signal processing. The system uses a low-power RF front-end when the received signal is strong, and uses a high-power RF front-end when the signal is weak, or the interference is high. A GSM system model was built and simulated, taking into account system requirements, such as BER, FER, SNR, etc.

To demonstrate an adjustable component, a CMOS low noise amplifier was designed in a standard CMOS .35 μm process. The simulation provides a gain of 21 dB at 1.9 GHz with a noise figure of 1.4 dB while drawing 6.5 mW from a 1.5 V supply. Also it is demonstrated that better performance can be achieved with an increase in power consumption. Measurements show correct operation. However, performance was impaired by packaging limitations.

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List of Terms

ADC	Analog to Digital Converter
ADS	Advanced Design System
BER	Bit Error Rate
BFSK	Binary Frequency Shift Keying
BPF	Band Pass Filter
BPSK	Binary Phase Shift Keying
CODEC	Coding and Decoding
DSP	Digital Signal Processing
DAC	Digital to Analog Converter
FER	Frame Error Rate
FEC	Forward Error Correction
FSK	Frequency Shift Keying
GMSK	Gaussian Minimum Shift Keying
GSM	Global System for Mobile System
I	Inphase

IF	Intermediate Frequency
IIP3	Input Third-order Interception Point
IP3	Third-order Interception Point
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Low Pass Filter
MSK	Minimum Shift Keying
MODEM	Modulation and Demodulation
NF	Noise Figure
OIP3	Output Third-order Interception Point
PLL	Phase Lock Loop
Q	Quadrature or Quality Factor
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
SNR	Signal to Noise Ratio
VCO	Voltage Control Oscillator
VLSI	Very Large Scale Integration

1 Introduction

1.1 RF Front End, DSP, VLSI

Digital wireless communication systems and their applications have grown rapidly in recent years. This is driven by increasingly high demand from subscribers and supported by the constant advances in digital signal processing (DSP) and very large scale integration (VLSI) technology. To accommodate the tremendous growth in the number of subscribers, advanced digital wireless systems such as Global System for Mobile (GSM), U.S. Digital Cellular (USDC) IS-54/136 and Code Division Multiple Access (CDMA) IS-95, etc., have been developed and deployed and are already in their maturity [Grag96, Rappaport96]. As the world moves to data, new standards such as IMT-2000, cdma2000, have been proposed and are under development [ITU96b, ITU98]. Applications vary from inexpensive low-end wireless e-mail services to fully equipped high performance portable multimedia terminals.

The evolution in wireless communications sets new requirements for the transceivers used in these applications. Higher operating frequencies, lower power supply voltages, lower power consumption and a very high degree of integration, are new design specifications which require design techniques quite different from the traditional RF techniques. New digital techniques allow for the use of complex modulation schemes and

sophisticated demodulation, encryption, error correction, and speech coding algorithms. This results in high quality wireless links with low bit error rates. In these new transceivers it is the analog front end, which is the interface between the antenna and the DSP, that forms a major bottleneck for further advancement.

In this thesis, an attempt is made to ease the design of the front end by using baseband signal processing. Since high speed data is the trend in next century wireless communication, power consumption is taken first as the target for improvement.

1.2 Objective and Contribution

1.2.1 Objective

Power consumption is a crucial design specification in portable system. Lower power consumption yields longer battery time or longer standby or active time.

It can be argued that that most of the power consumed by a PCS handset is drawn by the receiver. A pager, for example, will typically receive only. The receiver is turned on all the time, or is periodically turned on, whether it is in active listening, talking or standby mode, while the transmitter is only turned on in active talking mode. As technology advances, digital circuits consume less power, while the analog front end, including low noise amplifier (LNA), Mixer, Local Oscillator, and A/D converter dissipate almost the same amount of power. Therefore, the design of an analog front end with lower power

consumption becomes crucial. However, better performance and lower power consumption often contradict each other and complicate the design.

In this thesis, baseband digital signal processing is used as a solution for power saving. When the received signal is strong, the front end powers down (or is set at a low bias) at the expense of a lower performance front end. When the received signal is weak or interference is strong, front end power is increased (or set at a high bias) to improve the performance. In both cases the minimum system specification (frame error rate or bit error rate, S/I , etc.) are met. This scheme is referred to as a smart receiver.

Power control in traffic channel might limit the usefulness of the Smart Receiver. However, the smart receiver can still be helpful in standby mode.

1.2.2 Contributions

The major contributions of this thesis are summarized as follows:

- A 1.9 GHz low noise amplifier was designed in a standard CMOS .35 micron process. Simulations indicate that the amplifier has a gain of 21 dB with a noise figure of only 1.4 dB while drawing 6.5 mW from a 1.5 V supply. It is further shown higher performance can be obtained with a higher power RF front end [Yang99a]. The results match or exceed those of recently reported CMOS LNAs [Chang93], [Karanicolas96], [Sheng96], [Rofougaran96], [Shaeffer97].
-

- A novel idea is proposed and demonstrated to reduce power consumption of the RF front end by using a smart receiver in which the power dissipated by the front end is adaptively controlled by baseband signal processing. [Yang99b]
- An RF and baseband DSP co-simulation bench is designed and built using the HP Advanced Design System. The transceiver system includes data coding and decoding, GMSK modulation and demodulation, RF transmitter and receiver, propagation channel and baseband signal processing. The RF receiver's performance is controlled by the baseband DSP. System simulation results including: sensitivity, co-channel interference, adjacent channel interference, and intermodulation performance, are given and analyzed in detail. [Yang99b]

1.3 Organization

This thesis is divided into five chapters. Chapter 1 presents an introduction describing the challenges in the design of commercial digital wireless communication system. The smart receiver concept is also addressed.

The concept and theory of wireless transceivers is addressed in Chapter 2. Basic knowledge of wireless transmitters and receivers is provided first. Speech coding, channel coding, interleaving and digital modulation techniques are then presented. LNAs, mixers, and local oscillators, which form RF front ends, are also discussed with theoretical and practical issues of the LNA elaborated in detail.

Detailed design of an LNA is presented in Chapter 3. A complete circuit description and design strategies are given first, followed by simulation results of the LNA. Measurements are given and analyzed.

In Chapter 4, the concept of the smart receiver is first introduced. As an example application, the GSM receiver specifications are then described. A GSM transceiver system model using HP Advanced Design System (ADS) is built and discussed in detail. Model components include GMSK modulation and demodulation, RF transmitter and receiver, propagation channel and baseband signal processing. System simulation results, including sensitivity, co-channel interference, adjacent channel interference, and intermodulation performance are presented and analyzed in detail.

Chapter 5 presents conclusions and suggestions for future work.

2 Background and Overview

In this chapter, the general concept of wireless transceiver is introduced. In Section 2.1 the typical architecture is presented. Key building blocks for baseband signal processing are discussed in Section 2.2. Section 2.3 provides a RF front end receiver overview.

2.1 Wireless Transceiver Architecture

A transceiver is the two-way interface between an information source and the communication channel in which the information will be exchanged. The transmitter translates a data stream into a form which is suitable for the communication channels. The receiver does the reverse operation, i.e. translates what is received from communication channels into a data stream.

There are many different types of communication channels. Examples vary from analog twisted-pair copper, optical fiber and satellite links, to digital cellular wireless channels [Proakis95]. All wireless applications have two aspects in common: they operate in a passband around a carrier frequency and the carrier frequencies are constantly increasing with newly introduced applications. Both aspects are related to the fact that all wireless applications have to share their medium. Band limited operation prevents interference between applications. The use of higher operating frequencies together with lower

transmission radii and smaller cells is the primary method for increasing bandwidth and has a large impact on the design of modern wireless transceivers [Crols97]. Because of the nature of the wireless channels (passbands around high operating frequencies), almost all wireless transceivers consist of two main parts: a front-end which performs the frequency conversion and a back-end in which modulation or demodulation of the signal is performed. A third part, referred to as user-end, performs the information conversion between the back-end and the user [Crols97]. This latter part is not considered in this thesis. Figure 2-1 shows a typical configuration. On the receiver side, the antenna signal consists of a very broad band spectrum of many different channels, as well as interference and noise sources. The desired signal is only a very small part of this antenna signal. The front end converts this antenna signal into a signal which can be demodulated by the back-end. On the transmitter side, the information generated by the user-end is transformed by the modulator in the back-end and upconverted by the front-end to a signal suitable for the wireless communication channel. A duplexer is used to switch between the transmitter and the receiver.

Figure 2-1 Transceiver Basic Configuration.

2.1.1 Receiver

An example superheterodyne receiver block diagram is shown in Figure 2-2. The received RF signal is low-noise amplified by an LNA and band-pass filtered for image rejection. It is then combined with a variable local oscillator LO1 in the first mixer to convert the RF signal to an IF signal. This IF signal is filtered for selectivity and image rejection, then amplified and mixed with a pair of quadrature signals provided by a fixed local oscillator LO2 to provide baseband In-phase (I) and Quadrature (Q) signals. After being digitized by a pair of Analog to Digital Converters (ADCs), the I and Q signals are passed to a baseband DSP for demodulation, filtering, timing recovery, carrier recovery, equalization, diversity combining, deinterleaving, decoding, etc.

Figure 2-2 A Typical Receiver.

2.1.2 Transmitter

Figure 2-3 shows an example transmitter architecture. The data from the information source first goes through the baseband DSP for encoding, interleaving and signal shaping. It is then complex digitally modulated to form the in-phase and quadrature signals. The I and Q signals are then converted to analog I and Q signals through a pair of Digital to Analog Converters (DACs). The analog I and Q signal are low-pass filtered for image rejection and then mixed with a pair of quadrature signals provided by local oscillator LO2. The two signals are then combined and band-pass filtered for image rejection to form the IF signal. The IF signal is then combined with a variable local oscillator LO1 in MIXER1 to generate the RF signal. The RF signal is then band-pass filtered and power amplified to form the transmitted signal.

Figure 2-3 A Typical Transmitter.

2.2 Baseband Signal Processing and Digital Modulation

Having described the wireless transceiver in general, a more detailed description of the receiver is given in the following sections. In this first section, the basic digital signal processing in a wireless communication system is introduced. The baseband DSP block diagram is shown in Figure 2-4. Speech coding, channel coding, interleaving, digital modulation techniques are introduced and discussed.

Figure 2-4 Baseband DSP Functional Block Diagram.

2.2.1 Speech Coding

In digital cellular communication systems, the service provider frequency spectrum is for voice communication. The lower the bit rate at which a speech coder can achieve satisfactory quality, the more voice channels can be allocated within the given spectrum.

Speech coding is a technique for transmitting, storing and/or synthesizing speech with a minimum number of bits or bandwidth while maintaining a given quality [Spanias94].

There are three different techniques in speech coding, waveform coding, vocoder (parametric coding), and hybrid coding.

Speech Coding Techniques

Waveform coders

Waveform coders focus on representing the speech waveform in the time domain or spectral domain as faithfully as possible without exploiting a voice production model [Spanias94]. Among this type of speech coder, there are a number of schemes including Pulse Code Modulation (PCM), Differential PCM (DPCM), Adaptive DPCM (ADPCM), Adaptive Prediction Coding (APC), Subband Coding (SBC), Adaptive Transform Coding (ATC), etc.

Waveform coders usually yield superior speech quality but operate at a relatively high bit rate. PCM at 64 kbps and ADPCM at 32 kbps became ITU-T (formerly, CCITT) standards at the corresponding bit rate in 1972 and 1984 respectively [CCITT72, CCITT84]. There is a significant degradation in quality when the bit rate is below 16 kbps.

Vocoders (Parametric Coders)

Vocoders rely on speech models and focus on producing perceptually intelligible speech without matching the waveforms of the speech [Spanias94]. Vocoders are able to operate at a bit rate below 2.4 kbps but tend to produce speech of poor (synthetic) quality.

Vocoders rely on speech analysis-synthesis which is mostly based on a source-system model. The basic speech production model of vocoders assumes a clear separation between excitation and vocal tract. The excitation is the sound production mechanism, whereas the vocal tract is the filter to shape the sound. Parameters of the excitation and

the vocal tract are extracted separately. Using this assumption, speech is encoded separately with a substantial decrease in the bit rate.

Among this category, there are several schemes including Channel Vocoder, Formant Vocoder, Homomorphic Vocoder, and Linear Predictive Vocoder [Spanias94]. The Linear Predictive Vocoder have been the most widely researched and used techniques for the last twenty years. Its algorithm, known as linear predictive coding, is also widely used in hybrid vocoders. The LPC vocoder (LPC-10) was adopted by the U.S. Federal Standard FS-1015 for secure communications at 2.4 kbps [Tremain82].

Hybrid Vocoders

Hybrid coders combine the coding efficiency of the vocoder with the high quality potential of waveform coders. They model the spectral properties of speech and extract the vocoder parameters, while at the same time provide waveform matching like a waveform coder. Modern hybrid coders can achieve communication quality at 8 kbps and below at the expense of increased complexity.

Speech coders for digital cellular system such as GSM, IS54, and IS95, currently all use a hybrid vocoder. Low-delay code-excited-linear-prediction (LD-CELP) and conjugate-structure algebraic-code-excited linear-prediction (CS-ACELP) became ITU standards in 1992 and 1996 at the bit rates of 16 kbps and 8 kbps respectively [CCITT92, ITU96a].

Performance of speech coders

A speech coding algorithm is evaluated based on the bit rate, the quality of the reconstructed speech, the complexity, the delay introduced, and the robustness to the channel errors and acoustic interference [Spanias94]. In general, high quality speech coding at low bit rates is achieved using high complexity algorithms. For example, real time implementation of a low bit rate hybrid algorithm must be done on a digital signal processor capable of executing 12 or more million instructions per seconds (MIPS). The one way delay (coding plus decoding) introduced by such algorithm is usually between 50 to 60 ms [Spanias94]. This is unacceptable in wireline communications. Since the propagation delay plus the delay introduced by error correction coding is usually quite large in wireless or satellite communications, this is not critical for these applications.

In digital communications, speech quality is classified in the following four categories.

Broadcast quality--referring to wideband transmission with high quality speech at rates 64 kbps.

Toll or network quality--referring to speech comparable to classical analog speech and can be achieved at rates above 8 kbps.

Communication quality-- referring high intelligible, somewhat degraded speech. but adequate for telecommunications, which can be achieved at 4.8 kbps.

Synthetic quality--intelligible, but unnatural (machinelike), and unable to recognize the speaker.

Speech coders of digital cellular systems can typically produce speech with quality between toll quality and communication quality at rates between 8 kbps and 13 kbps.

2.2.2 Channel Coding

The basic purpose of channel coding is to introduce redundancies in the data to improve the communication link performance which is especially important for the wireless channels. The introduction of the redundant bits increases the raw data rate and therefore increases the bandwidth required for a fixed source data rate. It can however provide improved BER performance at a given SNR values [Proakis95].

Channel coding protects digital data from errors by selectively introducing redundancies in the transmitted data. Channel codes that can detect errors are called error detection codes, while codes that can correct errors are called error correction codes. There are two basic types of error correction and detection codes, block codes and convolutional codes.

Channel coding techniques

Block Codes

Block codes are typical forward error correction (FEC) codes that enable a limited number of errors to be detected and corrected. In block codes, parity bits are added to blocks of information to make code words or code blocks. In a block encoder, k information bits are encoded into n code bits. A total of $n-k$ redundant bits are added to the k information bits for the purpose of detecting and correcting errors. The block code

is referred to as an (n, k) code, and the rate of the code is defined as $R_c = k/n$ and is equal to the information rate divided by channel rate.

Convolutional codes

Convolutional codes are fundamentally different from block codes in that information bits are not grouped into distinct blocks before encoding. Instead, a continuous sequence of information bits is mapped into a continuous sequence of encoded outputs.

For example, a convolutional code can be generated by passing the information sequence through a finite shift register. In general, the shift register contains N (k -bit) stages and n linear algebraic function generators based on the generator polynomials as shown in Figure 2-5. The input data is shifted into and along the shift register k bits at a time. The number of output bits for each k bit input data sequence is n bits. The data rate is $R_c = k/n$. The parameter N is called the constraint length and indicates the number of input data bits that the current output is dependent upon. It determines how powerful and complex the code is.

Figure 2-5 Convolutional Coder Block Diagram.

It can be argued that convolutional codes can achieve a larger coding gain (see below) than can be achieved using a block code with the same complexity [Proakis95]. This is why all the second generation digital cellular systems adopted convolutional coding as their channel coding schemes [Rappaport96]. A rate $1/2$ convolutional code with constraint length of 5 is used by GSM. Similarly a rate $1/2$ convolutional code with constraint length of 6 was adopted by IS-136 and IS-54. In IS-95, a rate $1/2$ convolutional code with constraint length of 9 is used for the forward link, while a rate $1/3$ convolutional code with constraint length of 9 is used for the reverse link.

Turbo codes

Turbo codes have become more popular in third generation digital cellular systems [ITU98]. A general turbo encoder is shown in Figure 2-6 [ITU98]. The turbo encoder employs two systematic recursive convolutional codes connected in parallel with a turbo

interleaver preceding the second recursive convolutional encoder. The two recursive convolutional codes are called the constituent codes of the turbo code. The information bits are encoded by both encoders. The first encoder operates on the input bits in their original order, while the second encoder operates on the input bits as permuted by the turbo interleaver. The information bits are always transmitted across the channel. Depending on the code rate R_c , the parity bits from the two constituent encoders are punctured (i.e., some of them are discarded) before transmission.

Figure 2-6 General Turbo Encoder.

Coding Gain

The advantage of channel codes, whether they be block codes, convolutional codes, or turbo codes, is that they provide coding gain for the communication link. The coding gain describes how much better the decoded message performs as compared with the raw bit error performance of the coded transmission. Coding gain measures the amount of

additional SNR that would be required to provide the same BER performance for uncoded information. Coding gain is what allows a channel error rate of 10^{-2} to support decoded data rates which are 10^{-5} or better [Rappaport96].

2.2.3 Interleaving

Interleaving is used to obtain time diversity in a digital communication system without adding any overhead. Interleaving has become an extremely useful technique in all digital cellular systems. An interleaver is used to spread the information bits out in time so that if a deep fade or noise burst happens, a block of source of data are not corrupted at the same time which is quite crucial to modern digital speech coders. It is typical for many speech coders to produce several 'important' bits in succession.

An interleaver can be one of two forms, a block or a convolutional interleaver. A block interleaver formats the encoded data into a rectangular array of m rows and n columns, and interleaves $n*m$ bits at a time. Source bits are sequentially read into the interleaver column-wise, while the interleaved data is read out row-wise and transmitted over the channel. This has the effect of separating the original source bits by m bit periods. Recently bit-reversed interleaver have become more popular in third generation digital cellular systems [ITU98]. The interleaver structure remains the same. Source bits are sequentially read into the interleaver column-wise, while the interleaved data is read out row-wise. However, the row number to be read out is bit reversed.

Convolutional interleavers can be used in place of block interleavers in much the same fashion. Convolutional interleavers are ideally suited for use with convolutional codes.

There is an inherent delay associated with an interleaver since the received message cannot be fully decoded until all the $n \cdot m$ bits arrive at the receiver. In general, human ears can tolerate a delay of less than 40 ms. That is why all wireless data interleavers have delays which do not exceed 40 ms.

2.2.4 Digital Modulation

Modulation is a process of translating information from a message source to a form suitable for transmission. It normally involves transforming a baseband signal to a bandpass signal at frequencies that are very high when compared to the baseband frequency. The baseband signal is called the modulating signal while the bandpass signal is called modulated signal. Modulation may be done by varying the amplitude, phase, or frequency of a high frequency carrier in accordance with the amplitude of the message. Demodulation is the process of extracting the baseband signal from the carrier so that it could be processed and interpreted by the intended receiver.

Digital Modulation offers many advantages over analog modulation. Some advantages include greater noise immunity and robustness to channel impairments, easier multiplexing of various forms of information, and greater security.

Digital Modulation Techniques

Digital modulation techniques may be classified as linear and nonlinear.

Linear Modulation

In linear modulation techniques, amplitude of the transmitted signal varies linearly with the digital modulating signal. Linear modulation techniques are bandwidth efficient and hence are very attractive for use in wireless communication systems where there is an increasing demand to accommodate more and more users within a limited spectrum. Linear modulation schemes usually do not have a constant envelope. In this category are BPSK, QPSK, Offset QPSK and $\pi/4$ QPSK, etc.

While linear modulation has very good spectral efficient, the signal must be transmitted using linear RF amplifiers which have poor power efficiency. Using power efficient non-linear amplifiers results in the regeneration of filtered sidelobes which can cause severe adjacent channel interference, and leads to the loss of spectral efficiency gained by linear modulation. However popular linear modulation techniques such as pulse shaped QPSK, Offset QPSK and $\pi/4$ QPSK, have been developed to overcome these difficulties.

Constant Envelope Modulation (Nonlinear Modulation)

Many practical mobile radio communications systems use nonlinear modulation methods, where the amplitude of the carrier remain constant, regardless of the variation of the digital modulating signal. Low out-of-band radiation can be easily achieved by constant modulation. Power efficient class C power amplifiers can be used without introducing regeneration of filtered sidelobes. Non-coherent detection can be used, which simplifies

receiver designs and provides high immunity against random FM noise and signal fluctuation due to Rayleigh fading. However, constant envelope modulation generally occupies a larger bandwidth than linear modulation. In this category are Binary Frequency Shift Keying (BFSK), Minimum Shift Keying (MSK), Gaussian Minimum Shift Keying (GMSK), etc.

Spread Spectrum Modulation Techniques

Spread spectrum techniques use a transmission bandwidth which is several orders of magnitude greater than the minimum required signal bandwidth. While this system is very bandwidth inefficient for a single user, the advantage of spread spectrum is that many users can simultaneously use the same bandwidth without severely interfering with others. In a multiple-user, multiple access environment, spread spectrum systems can become very bandwidth efficient.

In spread spectrum techniques, the spreading or modulating signal is controlled by a pseudo-noise sequence or pseudo-noise (PN) code, which is a binary sequence that is random but can be reproduced in a determined manner by the intended receivers. Spread spectrum signals are demodulated at the receiver through cross-correlation with a locally generated version of the PN code. Cross-correlation with the correct PN code despreads the spread spectrum signal and restores the message in the same baseband as the original one, while cross-correlation with an undesired PN code results in a very small amount of wideband noise at the receiver output.

Direct Sequence Spread Spectrum (DSSS) and Frequency Hopping Spread Spectrum (FHSS) are two widely used techniques. The most important advantage of spread spectrum is its inherent interference rejection capability. Resistance to multipath fading is another fundamental reason to use spread spectrum systems for wireless communication.

2.3 RF Front End Receiver

In this section, the RF front end receiver components, (i.e., low noise amplifier (LNA), mixer, local oscillator (LO)) are introduced. The theoretical and practical issues of the LNA will be elaborated in detail, and a 1.9 GHz CMOS LNA design will be introduced in Chapter 3.

2.3.1 LNA

The first stage of a receiver is commonly a low-noise amplifier (LNA), whose main function is to provide enough gain to overcome the noise of subsequent stages (such as mixers), but not so much to cause the mixers to overload. Secondly, LNA should add as little noise as possible, since any noise it adds has a great impact on the overall noise performance of the receiver. Thirdly, an LNA should accommodate large signals without distortion (i.e. provide good linearity). Frequently, an LNA must also present a specific impedance, such as 50 Ohms, to the input source, which is particularly important if a passive filter precedes the LNA, since the transfer function of many filters are quite

sensitive to the quality of the terminations. In addition, the LNA should operate with low power consumption which is especially important in portable systems.

The design of an LNA is full of trade-offs between optimum gain, lowest noise figure, optimum input matching, high linearity and low power consumption. The apparent simplicity of an LNA is misleading. The design should be easy because there are relatively few components but these trade-offs complicate the design.

While the literature is full of examples of LNA work in GaAs and bipolar technologies, there are few examples of CMOS designs. However, CMOS provides the possibility of the integration of complete communication systems. Recently, more and more people have been involved in CMOS LNA designs, and recent work has demonstrated the viability of CMOS LNA at 900 MHz to 1.5 GHz [Shaeffer97].

Common Architectures

Figure 2-7 shows the four commonly used LNA architecture in simplified form. The first technique uses resistive termination of the input port to provide a $50\ \Omega$ impedance, which degrades the LNA's noise figure [Chang93]. The second approach, shown in Figure 2-7(b), uses the source or emitter of a common-gate or common-base stage as the input termination. Theoretical analysis give a lower bound on noise figure (1.7 dB) in bipolar devices, while the minimum achievable noise figure for short channel MOS devices tends to be 3 dB or greater [Shaeffer97]. Figure 2-7(c) shows another topology, which uses resistive shunt and series feedback to set the input and output impedance of the LNA.

Amplifiers using shunt-series feedback often have extraordinarily high power dissipation compared to others with similar noise performance [Shaeffer97].

The fourth architecture, inductive source degeneration, is the most prevalent method used in bipolar or BiCMOS. It has also been used in CMOS technologies recently. It offers the possibility of achieving the best noise performance of any architecture [Lee98]. This method generates a real term in the input impedance at the resonant frequency (desired frequency), making it a narrow band approach.

Figure 2-7 Common LNA Architectures. (a) Resistive Termination, (b) $1/g_m$ termination, (c) Shunt-Series Feedback, (d) Inductive Degeneration.

Noise Model and Noise Figure

The standard MOS noise model is shown in Figure 2-8.

Figure 2-8 MOS Noise Model.

The dominant noise source in MOS devices is channel noise or shunt noise current, given below.

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f \quad \text{Amp}^2 \quad \text{Equation 1}$$

Where $k = 1.38 \times 10^{-23}$ Joules/Kelvin. T is the working temperature in Kelvin. g_{d0} is the zero-bias drain conductance of the device. γ is a bias dependent factor which, for long channel device satisfies $\frac{2}{3} \leq \gamma \leq 1$, but for short channel device can be as large as two or three, depending on bias conditions. [Shaeffer97, Lee98]

Another source of noise in MOS devices is the noise generated by the distributed gate resistance. This noise can be modeled by a series resistance in the gate circuit and an accompanying white noise generator, which results in,

$$\overline{v_{rg}^2} = 4kT\delta R_g \Delta f \quad \text{Volt}^2 \quad \text{Equation 2}$$

Where δ is the coefficient of gate noise, classically equal to 4/3 for long channel devices, and R_g is the gate resistance. Since the gate resistance can be minimized through interdigitation without the need of increased power dissipation, it is generally considered less important. [Shaeffer97]

Flicker noise or 1/f noise is an additional noise source for MOS device, especially for low frequency application. For radio frequency circuits, it is often neglected.

A useful measure of the noise performance of a system is the noise factor, usually denoted F, and defined as

$$F = \frac{\text{total output noise power}}{\text{output noise due to input source}} \quad \text{Equation 3}$$

An equivalent measure, referred to as noise figure and denoted as NF, is defined as

$$NF = 10 \log_{10} \frac{\text{total output noise power}}{\text{output noise due to input source}} \quad \text{Equation 4}$$

Input and Output Match

Most radio frequency instruments and coaxial cables have a standardized impedance of 50 Ω , and so input and output impedances are often matched to 50 Ω . Another way to represent the input and output match is to use S-parameters, S11 and S22.

S11 is simply the input reflection coefficient, while S22 is the output reflection coefficient. When input and output are perfectly matched, S11 and S22 are 0, and no reflection occurs.

Figure 2-9 shows the input stage of the LNA. By using two inductors as shown and an appropriate choice of transistor size and bias current, one can achieve good impedance match and low noise figure. A simple analysis of the input impedance [Lee98] shows that

$$Z_{in} = s \left(L_s + L_g \right) + \frac{1}{sC_{gs}} + \left(\frac{g_{m1}}{C_{gs}} \right) L_s, \quad \text{Equation 5}$$

$$= \omega_T L_s \quad (\text{At resonance})$$

Where unity gain bandwidth

$$\omega_T = \frac{g_{m1}}{C_{gs}} \quad \text{Equation 6}$$

At the series resonance of the input circuit, the first two terms of Equation 5 cancel and the input impedance is purely real and proportional to L_s . By choosing appropriate L_s , the real term can be made equal to 50 Ω . This gives the possibility of implementing an on

chip matching network. However, since this is a tuned circuit, this a narrow band approach.

Figure 2-9 Inductively Degenerated Common Source Amplifier.

Linearity and IP3 (Third-order Intercept Point)

Although there are many measures of linearity, the commonly used measure is IP3. In general, nonlinearity can be modeled as a power series as given in below:

$$v_o = k_1 v_i + k_2 v_i^2 + k_3 v_i^3 + \dots \quad \text{Equation 7}$$

where v_i , v_o are the input and output voltage. k_i , ($i=1,2,3, \dots$) is the coefficient of the i th-order term.

Now consider two sinusoid input signals of equal amplitude but slightly different frequencies given by:

$$v_i = A(\cos \omega_1 t + \cos \omega_2 t) \quad \text{Equation 8}$$

Where A is the amplitude of both signals. ω_1 and ω_2 are the frequencies of the two signals.

Since the second-order and third-order harmonic and the second-order intermodulation terms can be filtered out, nonlinearity is caused mainly by third-order intermodulation terms. It can be shown that the fundamental term and the third-order intermodulation terms (IM3) are as follow:

$$\text{Fundamental at : } \omega_1, \omega_2 = k_1 A + \frac{9}{4} k_3 A^3 \quad \text{Equation 9}$$

$$\text{IM3 at : } 2\omega_1 - \omega_2 = \frac{3}{4} k_3 A^3 \quad \text{Equation 10}$$

$$\text{IM3 at : } 2\omega_2 - \omega_1 = \frac{3}{4} k_3 A^3 \quad \text{Equation 11}$$

For small A, the fundamental output power is proportional to A, while the intermodulation is proportional to A^3 . On log-log plot the slopes will be +1 and +3 as shown in Figure 2-10.

Figure 2-10 IP3 and Measurement [Plett97].

One simple method to measure IP3 is to apply two closely spaced frequency tones to the input which are significantly larger than the noise floor but much lower than the compression point. Measuring the input power P_i and the output power of fundamental P_{01} and the intermodulation P_{03} , it can be easily shown that OIP3 (output referred IP3) and IIP3 (input referred IP3) are as follows,

$$OIP3 = \frac{1}{2}(3P_{01} - P_{03})$$

Equation 12

$$IIP3 = P_i + \frac{1}{2}(P_{01} - P_{03}) \quad \text{Equation 13}$$

In Figure 2-10 OIP3 is at 20 dBm and IIP3 is at 10dBm.

Gain and Power Dissipation

The main function of the LNA is to provide enough gain to overcome the noise of subsequent stages (such as mixers), but not so much as to cause the mixer to overload. Typically the gain of LNA is in the range of 10 to 22 dB.

Power dissipation is a key driving factor of portable systems. An LNA should consume as little power as possible.

Recent Developments in CMOS LNAs

Table 2-1 shows the recent developments in CMOS LNAs. LNAs using inductor degeneration yield relatively better results in overall performance in terms of gain, noise figure, and IP3.

Table 2-1 Summary of Recent CMOS LNA Results.

Author	NF (dB)	Gain (dB)	OIP3 (dBm)	Power (mW)	f ₀ (GHz)	Architecture	Process (μm)	Year
[Chang93]	6.0	14	NA	7	0.75	R-Term.	2	93
[Karanicolas96]	2.2	15.6	12.4	20	0.9	L-Degen.	.5	96
[Sheng96]	7.5	11.0	NA	36	0.9	Shunt-ser.FB	1	96
[Rofougaran96]	3.5	22	NA	27	0.9	1/g _m -Term.	1	96
[Shaeffer97]	3.5	22	12.7	30	1.5	L-Degen.	.5	97

2.3.2 Mixer

A mixer is fundamentally a multiplier that multiplies a signal by a sinusoid, shifting it to both a higher and lower frequency, and selects one of the resulting sidebands. A RF signal represented by

$$S_{RF}(t) = a(t) \cos \omega_{RF} t \quad \text{Equation 14}$$

is multiplied by a local oscillator (LO) signal $\cos \omega_{LO} t$ to obtain the IF signal

$$S_{IF}(t) = \frac{1}{2} a(t) [\cos(\omega_{RF} + \omega_{LO})t + \cos(\omega_{RF} - \omega_{LO})t] \quad \text{Equation 15}$$

In a receiver, the difference-frequency component is usually desired, and the sum-frequency component is often rejected by filters.

A Gilbert mixer is one of the most frequently used active mixers in wireless communication systems, an example of which is shown in Figure 2-11. It depends on a cancellation between the exponential I/V and logarithmic V/I characteristics of bipolar or on a cancellation between the square I/V and square-root V/I characteristics of CMOS transistors to produce accurate product characteristics [Larson97].

Figure 2-11 Gilbert Mixer.

There are a number of important issues that should be considered when designing a mixer. These include conversion gain, noise figure, linearity, bandwidth, leakage, power consumption, cost, etc. Linearity is commonly the most important in mixer design, since it is the last stage of the RF front end receiver.

2.3.3 LO

Local oscillators, usually voltage-controlled oscillators (VCO), are key components of all analog communication systems. They provide the precise reference frequencies for modulation and demodulation of baseband signals or IF signals up to the transmitted and received RF signals. A VCO is essentially a dc-to-RF converter that produces an RF

signal output with only a dc input signal. An oscillator consists of two chief components: an active device that acts as an amplifier and a feedback network to provides positive feedback in the system. The feedback network is frequency-sensitive and includes some type of resonator to set the operating frequency. A general block diagram of a linear oscillator is shown Figure 2-12.

Figure 2-12 Linear Oscillator Block Diagram.

The well-known expression for the closed loop gain is

$$A_f(s) = \frac{Y(s)}{X(s)} = \frac{A(s)}{1 - A(s)H(s)} \quad \text{Equation 16}$$

The loop gain is defined as

$$L(s) \equiv A(s)H(s) \quad \text{Equation 17}$$

where $s = j\omega$. If, at some frequency ω_b , the loop gain is unity, then the closed-loop gain of the system will be infinite. In other words, there will be a finite output signal at some frequency ω_b with zero input signal. The system will oscillate at this frequency. However,

typically the loop gain is designed to be greater than 1 so that the startup of oscillation can be guaranteed, with any applied noise. As the amplitude increases, nonlinearity in the active device will limit the amplitude.

The typical design emphasis of an oscillator is on low noise, high efficiency, temperature stability, bandwidth, linear and wide-band tunability, low cost, and reliability.

2.4 Summary

The concept and theory of the wireless transceiver have been introduced in this chapter. The basic knowledge of wireless transmitter and receiver was provided first. Speech coding, channel coding, interleaving and digital modulation techniques were discussed in Section 2.2. The LNA, mixer and local oscillator which form a RF front end were discussed in Section 2.3, with theoretical and practical issues on the LNA elaborated in detail.

3 CMOS Low Noise Amplifier at 1.9 GHz

Our goal for the Smart Receiver is to control power dissipation of each front end component by adjusting the bias or power supply. Since the LNA is the first stage of a wireless receiver, it is chosen to study the impact on the performance by adjusting the bias or power supply.

The detailed design process and simulation results of a CMOS LNA are presented in this chapter. The complete circuit description and design strategies are given in Section 3.1. Simulation results of the LNA are illustrated in Section 3.2. The amplifier provides a simulated gain of 21 dB at 1.9 GHz with a noise figure of only 1.4 dB while drawing 6.5 mW from a 1.5 V supply [Yang99a]. The measurement results are given in Section 3.3.

3.1 Design Approach

3.1.1 Design goals

The goal for the LNA was to match or exceed the performance of other reported LNAs which were listed in Table 2-1. Thus the goals were gain of 22 dB, noise figure of 2.2 dB, power dissipation of 7 mW, etc.

3.1.2 Design Process

The TSMC (Taiwan Microelectronics Manufactory Corporation) CMOS .35 μm process was used to design and fabricate the LNA circuit. The minimum gate length is .35 μm . Threshold voltage of NMOS V_{tn} is around 0.7 V and Threshold voltage of PMOS V_{tp} is around -0.9 V.

3.1.3 Complete Circuit

The fourth architecture discussed in Section 2.3, inductor degeneration, was used in this design. A cascode transistor was added to increase gain and improve isolation. It was found that with a single-stage cascode amplifier, only 10 dB of gain could be achieved so a second stage was added. The complete circuit is shown in Figure 3-1. It was found that a two stage amplifier was required to achieve the desired gain, and to provide good isolation between the input and output.

Figure 3-1 Complete Circuit of A 1.9 GHz, 6mW, Two Stage Single-Ended LNA.

The first stage is a cascode amplifier formed by transistors M_1 and M_2 . Inductors L_s and L_g are for input matching. Inductor L_d and capacitor C_d form a tank circuit to tune the LNA to 1.9 GHz. Transistor M_3 forms a common source output stage with matching network of inductor L_o and capacitor C_o . Transistor M_0 , resistors R_0 and R_b form a bias circuit. Transistor M_0 forms a current mirror with M_1 , while R_b prevents the bias circuit from shunting the AC input signal. Capacitor C_i is used as a DC blocking capacitor. Resistors R_s and R_L are 50 Ω source and load resistors.

3.1.4 Design Strategies

Set the size of the transistors

Channel noise can be reduced by using larger transistors or higher I_D . High current I_D will increase the noise in proportional to $\sqrt{I_D}$, but output signal is proportional to I_D . Thus using larger transistors or higher current will result in lower noise figure. In the design of the LNA, larger transistors result in lower noise but consume more power. In general there is a trade-off between the two factors. After several iterations, the size of M_1 and M_2 were set to 350 μm . Gate lengths of all transistors were set to the minimum 0.35 μm .

To minimize power dissipation, the width of M_0 and M_3 were set at 50 μm and 10 μm respectively. M_0 consumes a small portion of the overall power and since it is used simply to set the DC bias its size is not critical. Since the gate of M_3 is biased at V_{dd} , power dissipation is strongly dependent on transistor size. Seventy percent of the total power is dissipated by M_3 when the size is 50 μm . For this reason a size of 10 μm was chosen, however this limits the attainable value of IP3.

Set the Bias

The value of R_0 was adjusted so that the LNA had good gain and dissipated a minimum amount of power. A high bias voltage supply to the gate of M_1 gives high gain, because of large g_m , that is [Johns97]

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th}) \quad \text{Equation 18}$$

but also gives high drain current I_D and power consumption

$$I_D = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right) (V_{GS} - V_{th})^2 \quad \text{Equation 19}$$

In the LNA circuit implementation, R_0 is connected to a different bias voltage V_b so that there exists flexibility to adjust bias when testing the real circuit. In the final optimized circuit, R_0 was adjusted to result in 3.1 mA of current through M_1 for which the required V_{GS} of M_1 was 1.1 V.

Input Matching

Inductor L_s was first adjusted to make the real part of the input impedance 50 Ω . Then inductor L_g was adjusted to bring the imaginary part of the input impedance to zero, which results in series resonance at the input.

Tank Circuit Tuning

Values of L_d and C_d were selected to make the tank resonant at 1.9 GHz.

Output matching

Values of L_o and C_o were selected to bring output impedance to 50 Ω .

Simulation goals

Simulated gain, noise figure, power dissipation and IP3 were obtained. Circuit parameters in the LNA circuit were adjusted to achieve the goals, i.e. gain of 22 dB, noise figure of 2.2 dB, power dissipation of 7 mW, OIP3 of 12 dBm.

Inductor modeling

For radio frequency or microwave integrated circuits, passive onchip inductors are crucial to performance. However a lack of accurate models presents design challenges. At the start of this work, there were no available inductor models for the CMOS .35 μm technology. Later, an inductor modeling software package referred to as ASITIC [Niknejad98] was used to model the on-chip inductors.

Large inductors require a lot of silicon space and suffer from low self resonance and low Q. For this reason, inductors which were larger than 10 nH were placed off-chip, while those which were smaller than 10 nH were placed on chip. We assume that an off-chip inductor Q of 50 can be achieved and lacking appropriate on-chip inductor models, the on-chip inductors were initially simulated assuming they had a Q of 5 over the frequency range of simulations (1.5 to 2.5 GHz). Measurements gave a Q of 3 to 4 for CMOS .35

μm process (see Table 3-4). Off-chip components consist of C_i and C_o , L_o and L_g .

On-chip components include all transistors, all resistors, C_d , L_d and L_s .

3.2 Simulation Results

The proposed circuit was simulated using HSPICE and Cadence. The transistor model is Bsim3 for the TSMC CMOS .35 μm process.

Figure 3-2 shows the voltage gain of the LNA. The amplifier provides a forward gain of 21 dB between 1.88 GHz and 1.93 GHz while the 3-dB band ranges from 1.84 GHz to 1.99 GHz.

Figure 3-2 Voltage Gain of LNA.

Simulated noise figure is obtained and shown in Figure 3-3. The simulated LNA achieves a noise figure of 1.4 dB at 1.9 GHz while providing a noise figure of 1.5 dB or less over the range from 1.8 GHz to 2.0 GHz. Noise figure was strongly dependent on the quality of the input inductor, L_g in Figure 3-1, and for this reason it was put off chip. However, because of the gate resistance and inadequate transistor noise model in Hspice, it was expected that measured noise figure would be somewhat higher than the simulation results.

Figure 3-3 Noise Figure.

The input and output reflection coefficients (S_{11} and S_{22}) of the LNA are illustrated in Figure 3-4. This shows a highly tuned response, but if 10 dB is a good match, the input is matched from 1.7 GHz to nearly 2.2 GHz. The output is matched over a narrow region around 1.9 GHz. S_{22} indicates a highly tuned impedance matching, a result of the very high output impedance of the MOS transistor, which will be sensitive to process, temperature and power supply variation. The effects of such variation have not yet been evaluated.

Figure 3-4 S_parameters.

The layout of the amplifier is shown in Figure 3-5. This shows the initial layout of the LNA showing two inductors and active circuitry. The layout shows two sets of probe pads, (8-pins and 3 pins). The initial idea was to probe, however, matching proved to be tough, or impossible.

The layout has some flaws, in particular the inductors are too close to each other and to the active circuitry. The active area is $510\text{ }\mu\text{m} \times 250\text{ }\mu\text{m}$. The layout of the revised chip is presented in the next section.

Figure 3-5 Layout of the LNA.

The LNA simulation results in Table 3-1 show that the performance of the LNA is quite good except for IP3. Comparing initial simulations to extracted simulations demonstrates that the addition of interconnect parasitic capacitances do not affect the performance strongly. The biggest change is S22 which is the result of being tuned over a very narrow band.

Table 3-1 Simulation Results of the LNA.

Results	Schematic	Layout
Frequency	1.9 GHz	1.9 GHz
Noise Figure	1.4 dB	1.4 dB
Gain	20 dB	21 dB
OIP3	-14 dBm	-16 dBm
S11	-35 dB	-42 dB
S22	-32 dB	-20 dB
Supply Voltage	1.5 V	1.5 V
Power Dissipation	6.5 mW	6.5 mW

To demonstrate the scheme of power adjusting, the power supply for the LNA circuit was reduced to 1 V. Simulation results were obtained and are shown in Table 3-2. Up to 50% of the total power could be saved by setting the supply voltage to 1 V, however, the performance was degraded.

Table 3-2 Performance Degradation by Lowering the Power Supply.

Supply Voltage	1.5 V	1.0 V
Frequency	1.9 GHz	1.9 GHz
Noise Figure	1.4 dB	2.5 dB
Gain	20 dB	12 dB
OIP3	-14 dBm	-21 dBm
S11	-35 dB	-33 dB
S22	-32 dB	-30 dB
Power Dissipation	6.5 mW	4 mW

Adjusting bias current was also attempted. When bias was changed, C_{gs} was also changed and the input was no longer matched to $50\ \Omega$, and the LNA optimum operation frequency was no longer at 1.9 GHz. Design of bias variable circuits could be the future work.

A modified version of the LNA was designed. The gate width of the second stage amplifier was increased to $40\ \mu\text{m}$ which resulted in an improved OIP3 of +8 dBm at the expense of an increased power dissipation of 12 mW. The other performance parameters remain almost unchanged, as shown in Table 3-3. As can be seen, better performance is achieved using increased power.

Table 3-3 Performance Comparison of the Two LNAs.

Results	LNA1	LNA1	LNA2
Frequency	1.9 GHz	1.9 GHz	1.9 GHz
Noise Figure	2.5 dB	1.4 dB	1.4 dB
Gain	12 dB	20 dB	21 dB
OIP3	-21 dBm	-14 dBm	8 dBm
S11	-33 dB	-35 dB	-38 dBm
S22	-30 dB	-32 dB	-28 dBm
Supply Voltage	1.0 V	1.5 V	1.5 V
Power Dissipation	4 mW	6.5 mW	12 mW

As will be discussed in Chapter 4, power dissipated by the front end is adaptively controlled by baseband signal processing. When the received signal is strong, the front

end components are powered down (set at low bias) at the expense of lower performance. When the signal is weak, or the interference is high, the front end power is increased to improve performance. In both cases, the minimum system requirements (bit error rate or frame error rate, signal to interference ratio) must be met.

3.3 LNA Measurements

The design was fabricated in two processing runs using CMOS .35 μm technology. There were no inductor models in CMOS .35 μm technology and some of the process parameters were not available for the first run. Therefore, there were significant differences between the measured inductance values and quality factors than those that were initially expected. The inductors were redesigned using ASITIC [Niknejad98] and the LNA was resubmitted for a second run. The layout of the revised design of the LNA is shown in Figure 3-6. The LNA has inductors with better spacing, and only 8 probe pins.

Figure 3-6 Layout of the Revised LNA.

The revised chip with the LNA showed in the dashed line is shown in Figure 3-7.

Figure 3-7 Chip Layout with the Revised LNA.

The tests on the inductors for the revised design revealed that the inductor designs were reasonably accurate. The difference between tested and simulated inductance values was within 10 percent, while the quality factors were between 3.0 and 4 which is the typical value for CMOS .35 μm technology. Table 3-4 gives the measurements of the two on-chip inductors at 1.9 GHz.

Table 3-4 Measurements of On-chip Inductors.

Inductors	Simulated Inductance	Measured Inductance	Simulated Quality Factor	Measured Quality Factor
L_d	7.5 nH	7.9 nH	5.0	3.0
L_s	1.5 nH	1.62 nH	5.0	3.7

The initial idea was to probe, however, matching proved to be tough, or impossible.

The die was bonded to a package as shown in Figure 3-8. Connections are to input, output, VDD, ground and bias voltage. The die attach area is about 3mm by 3 mm.

Figure 3-8 Chip Connection to the Package.

The package was then inserted inside a Daico test fixture (formerly Tri Quint) which is shown in Figure 3-9. The package is pin guided, then pressed connected to 50 Ω transmission lines. These lines run to SMA connectors outside the box. The fixture is designed for operation up to 10 GHz. DC biasing can be provided with a Bias-T on the input and output. If the chip is internally matched to 50 Ω , then everything is fine. Otherwise, lengths of transmission lines become vitally important and matching components are very difficult to add. For example, as in the simulation, an inductor was

required from the output to VDD, but as shown in Figure 3-9, it cannot be connected directly at the chip. (Note if a DC short to ground were allowed then it could have been connected closer to the chip). Also a capacitor connection is shown on the inside of the SMA connector at the end of the transmission line.

Figure 3-9 Matching with Test Fixture.

Previously, L was shown connected at the output, but with the transmission line, it is no longer certain that an inductor is the correct matching component.

The schematic for the measurements shown in Figure 3-10 is nearly the same as previous except the bond pads are shown specifically as squares, and the fixture transmission lines are shown as thick line. As well, bias-Ts are shown at the input and the output, made up

of an RFC (for DC biasing while blocking AC), and a series blocking capacitor. The internal bias circuit (M_0 , R_0 and R_b) is replaced by a bias-T.

Figure 3-10 Schematics for Measurements.

Figure 3-11 shows an example of how the presence of a transmission line completely changes matching on the Smith Chart. On the Smith Chart real axis, $50\ \Omega$ sits in the middle, $0\ \Omega$ on the left, infinity on the right, while capacitance lies below and inductance above the real axis. S_{22} starting point is at the lower right shown as point a. This is nearly an open circuit plus parasitic capacitance. In simulation, a parallel L moves the impedance to point b where a small series capacitor brings it to $50\ \Omega$ (point c). However, with the transmission line, the impedance is rotated about the chart. Measurements show that the line is just over a quarter wavelength, so the rotation is just over halfway around

the Smith Chart to point d. In such a case, adding a parallel L moves it to point e, which is incorrect.

In this case a parallel C is needed, which would move from point d to point f or g, then series C or series L is needed to move to the $50\ \Omega$ point c. The important message is that one must realize the effect of the transmission line. With a parallel capacitor connected on the SMA connector, some measurements were performed.

Figure 3-11 Impact of Transmission Line to S22.

Without matching the response follows the outside edge of the Smith Chart as predicted. The capacitor has added the loop in Figure 3-12 with the best matching around 2 GHz. S11 shows $15 + j31\ \Omega$ at about 2 GHz as in Figure 3-13.

Figure 3-12 S₂₂ Measurement. Figure 3-13 S₁₁ Measurement.

Measurements show that both S11 and S22 are still not matched well, so gain is still poor. S21 is shown in Figure 3-14. S21 Forward gain shows roughly the right shape, and peak at 2 GHz, but the gain is very low around 2 dB. (There is a 2 dB loss due the bias-Ts and connection wires.) Calculation shows that the improvement by matching exactly is less than 2 dB, just over 1.5 dB at the output and a few tenths of a dB at the input.

Device measurements by other researchers indicated that the 0.35 micron TSMC CMOS transistors at a fixed bias point had measured current as low as half the predicted current and half the predicted Gm [Rafla99]. In their case, with a two stage amplifier, this could result in gain being low by 12 dB. The transistor model inaccuracies would also affect our circuit, but not by as much since the current level could be controlled and the bias voltage was increased until the expected current is obtained.

Figure 3-14 S21 Measurement.

S12 reverse gain gives -29 dB at 2 GHz as shown in Figure 3-15.

Figure 3-15 S12 Measurement.

3.4 Summary

In this chapter, we have demonstrated a low noise amplifier in a standard CMOS .35 μm process which can be the first amplifier in the receiver of a portable system. Based on the simulation results of this critical RF component, we believe that CMOS is a suitable technology for wireless receiver design and can provide the integration of a complete communication system on a single chip in the future.

Simulation results shows that the amplifier provides a gain of 21 dB at 1.9 GHz with a noise figure of only 1.4 dB while drawing 6.5 mW from a 1.5 V supply.

The design was fabricated in two processing runs using CMOS .35 μm technology. Since the operation frequency is quite high, some off-chip matching components should be placed between the instruments and the circuits. Attempts were made to place the circuit in some packages, on a circuit board and a test fixture. It proved to be very difficult to provide good input and output matching. Poor measurement results showed less than 2 dB of gain, which were attributed to a combination of poor matching, not including packaging model and inadequate transistor models used in simulations.

4 Smart Receiver

In this chapter the GSM receiver specifications will be described in section 4.1. A GSM transceiver system built with HP Advance Design System (ADS) will be discussed in Section 4.2. Details include discussion on the design of data coding and decoding, GMSK modulation and demodulation, RF transmitter and receiver, propagation channel and baseband signal processing. In Section 4.3, system simulation results including: sensitivity, co-channel interference, adjacent channel interference, and intermodulation performance, will be given and analyzed in detail.

Smart Receiver scheme is a generalized proposal and should be applicable to many existing or future wireless communication system. Some of the GSM radio air interface specifications are used as an example of the design and simulation of a Smart Receiver.

4.1 GSM Receiver Specifications

The GSM (Global System for Mobile) standard is the European second generation digital cellular system for voice and data communication in the 900 MHz band. GSM's success has exceeded expectations, and it is now the most popular standard for digital cellular radio and personal communications equipment throughout the world. It has been deployed in Europe, Asia, Africa, North America and South America.

GSM has separate bands of operation, with 890 MHz to 915 MHz for the reverse link and 935 MHz to 960 MHz for the forward link. Within the above two 25 MHz bands, no signal foreign to GSM system may be transmitted. The operation bands are subdivided into different communication channels with 200 kHz spacing. GSM uses TDMA (Time Division Multiple Access) and FDD (Frequency Division Duplex) with a forward and reverse channel pair separated by 45 MHz. Radio transmissions on both the forward and reverse channels are made at a data rate of 270.833 kbps using $BT = 0.3$ GMSK modulation.

The required performance for a mobile station receiver is specified as a function of the BER (bit error rate) and FER (frame error rate) which must be met for different channels and propagation conditions. The BER or FER can generally only be obtained by lengthy BER simulations on a dedicated simulator with special libraries which model the channels and propagation conditions. However, the BER and FER are a good method to specify the required performance of a GSM system as it takes into account all possible effects (such as noise, interference, fading, etc.). It is also the specification which is the most important (i.e. the amount of received useful information). With the help of a powerful convolutional coder and interleaver, the GSM system can give good performance (BER of 10^{-5} for the source data) on a channel which BER is between 1.5% to 2.5%.

The GSM radio air interface specification is used as a model for the high performance part of the smart receiver. The following is the GSM radio air interface specification with the bit error rate less than 2%. [Redl95, Crols97]

1. Signal to unwanted signal ratio: 9 dB
2. Sensitivity: -102 dBm. (The total equivalent input noise must be lower than -111 dBm.)
3. Co-channel interference: 9dB below the wanted signal level.
4. The interference performance has to be met when one of the following random modulated signal is present together with the wanted the signal.

Adjacent channel (200 kHz) interference: 9 dB above the wanted signal level.

Adjacent channel (400 kHz) interference: 41 dB above the wanted signal level.

Adjacent channel (600 kHz) interference: 49 dB above the wanted signal level.

5. Intermodulation: wanted signal (-99 dBm) at f_0 , GMSK interference (-43 dBm) at $f_0+800\text{kHz}$, sine wave (-43 dBm) at $f_0+1600\text{kHz}$.

In addition to above, the maximum allowed wanted signal level is -12 dBm.

4.2 System Architecture

A complete transceiver aimed at GSM was built in HP-ADS (Advanced Design System).

HP-ADS is an advanced tool for co-simulation of RF analog, IF and baseband digital

signal processing. Test benches can be built by adding functional boxes where the parameter values are specified.

Figure 4-1 shows the system architecture. Each functional box has its own sub-functional boxes.

Figure 4-1 A GSM Transceiver System Architecture.

The information bits coming out of the data source were differentially encoded and passed to GMSK modulation before they are mixed to the RF signal and transmitted through a wireless propagation channel with white noise and interference added to the channel. The received RF signal is received and mixed down to an IF signal by either of the two RF receivers depending on the BER. The IF signal is then GMSK demodulated and differentially decoded. The Baseband DSP block is used to measure the BER of the system and determine which RF receiver is to be used for the following data blocks.

In GSM, received signal strength and quality of the traffic channel which are sent on Slow Associated Control Channel (SACCH) can also be used to determine which RF receiver is to be used for the following data blocks. SACCH is transmitted during the thirteen frame of every speech/dedicated control channel multiframe.

There are 148 bits which are transmitted at a rate of 270.833 kbps for each GSM time slot. Out of the total 148 bits, 114 are information-bearing bits which are transmitted as two 57 bit sequences close to the beginning and the end of the burst (transmission of data). The midamble consists of a 26 bit training sequence which allows the adaptive equalizer in the mobile or base station receiver to analyze the radio channel characteristics before decoding the user data. The delay path in Figure 4-1 does not exist in real life, but it can be regarded as a path for the training bits which are known to the receiver.

The symbol duration was set at 3.7 μ s which is the inverse of the GSM data rate of 270 kbps.

The following are the brief description of each block in Figure 4-1. More detailed description will be given in the following subsections.

The differential data encoder and decoder are used to resolve the phase ambiguities introduced by the carrier recovery in the demodulator.

A BT (discussed later) of 0.3 GMSK (Gaussian Minimum Shift Keying) modulator was used in the system, which brings the baseband signal to the 70 MHz IF stage.

The RF transmitter includes a mixer, oscillator, and power amplifier.

The propagation path model includes a base station antenna, GSM propagation model, mobile station antenna, Gaussian white noise, single-tone interference, and GMSK-modulated interference.

The RF receivers include a low noise amplifier, mixer, and oscillator.

Coherent demodulation with recovered clock and carrier signals is carried out in the GMSK demodulation block.

A baseband signal processing module is added to measure the system bit error rate, and select which RF receiver is used according to a certain criteria which will be discussed later.

In this system, for simulation purpose, two different RF receivers were used instead of one receiver with variable bias.

4.2.1 GMSK Modulation

GMSK (Gaussian Minimum Shift Keying) was adopted as the digital modulation scheme for the GSM standard. GMSK may be viewed as a derivative of MSK (Minimum Shift Keying) wherein the peak frequency deviation is equal to half the bit rate. In other words, MSK is a continuous FSK (Frequency Shift Keying) with a modulation index of 0.5. The modulation index is define as

$$h = \Delta f / R_b \quad \text{Equation 20}$$

Where Δf is the total frequency difference and R_b is the data rate. A modulation index of 0.5 is the minimum frequency spacing that allows two FSK signals to be coherent orthogonal, and the name “minimum shift keying” implies the minimum frequency separation that allows orthogonal detection.

MSK is a spectrally efficient modulation scheme and is particularly attractive for use in mobile communication systems. It possesses properties such as constant envelope, spectral efficiency, good BER performance, and self-synchronizing capability. However, the transmitted power spectrum of MSK is still too wide for many applications.

One method to narrow the transmitted spectrum of MSK is by filtering the modulating data signal through a baseband Gaussian pulse-shaping filter before applying it to a FM modulator. The pre-modulation Gaussian filtering introduces ISI (Inter Symbol Interference) in the transmitted signal, but it can be shown that the degradation is not significant as long as the product (BT) of 3 dB bandwidth (B) and bit duration (T) is greater than 0.5 [Rappaport96]. Reducing BT increases the irreducible BER produced by the low pass filter due to ISI. However, the mobile radio channels induce an irreducible BER due to mobile velocity, fading, shadowing, scattering, etc. As long as the GMSK irreducible BER is less than that produced by the mobile channels, there is no penalty in using GMSK. As a result, GMSK modulation with $BT = 0.3$ is used in GSM systems.

GMSK pre-modulation filter has an impulse response given by

$$h(t) = \frac{\sqrt{\pi}}{\alpha} \exp\left(-\frac{\pi^2}{\alpha^2} t^2\right) \quad \text{Equation 21}$$

and the transfer function is given by

$$H(f) = \exp(-\alpha^2 f^2) \quad \text{Equation 22}$$

The parameter α is related to the 3 dB bandwidth B by

$$\alpha = \frac{\sqrt{2 \ln 2}}{B} \quad \text{Equation 23}$$

Figure 4-2 shows the GMSK modulation block in the simulation.

Figure 4-2 GMSK Modulation Block Diagram.

Since symbol duration was set to 3.7 μs , the bandwidth B of the Gaussian filter was set to 81 kHz. The FM carrier frequency was set at 70 MHz and the total frequency difference Δf was set at 135 kHz which is half the data rate. Figure 4-3 shows the GMSK modulated signal.

Figure 4-3 GSM Modulated Signal.

4.2.2 RF Transmitter

The modulated signal is further mixed with a local oscillator and passed to a bandpass filter before it is finally transmitted through the air.

Figure 4-4 illustrates the RF transmitter architecture.

Figure 4-4 RF Transmitter Block.

The performance parameters of RF transmitter were not optimized as the primary focus is on the RF receivers.

The LO operates ideally at 830 MHz with a power of 5 mW. No phase noise was added to this block in the simulation. The 70 MHz modulated signal was mixed up to form a 900 MHz RF signal. The mixer is operated ideally with -200 dB of RF rejection, IF rejection and image rejection and had a noise figure of 8 dB and Output IP3 of -7.5 dB. The bandpass filter was a third order Butterworth filter centered at 900 MHz. It has a pass bandwidth of 1.2 MHz with 3 dB attenuation and a stop bandwidth of 80 MHz with 50 dB attenuation. The power amplifier has a gain of 25 dB, a noise figure of 6 dB, an output IP3 of 37 dBm, and a 1-dB compression point of 27 dBm.

Figure 4-5 Gives the spectrum of the transmitted signal centered at 900 MHz with the power of 34 dBm.

Figure 4-5 Transmitted Signal.

4.2.3 Propagation Channel

The RF signal coming from the power amplifier is further amplified by the base station antenna. The signal is transmitted over a GSM radio channel with both large scale path loss and small scale fading and multipath. The signal together with additive white Gaussian noise (AWGN), single-tone interference, and GMSK-modulated interference were then collected by a mobile antenna, as shown in Figure 4-6. These are all standard blocks in ADS.

Figure 4-6 Propagation Block.

Both base station and mobile antennas have parameters of x and y coordinates to set the distance from the base station to the mobile. By changing the distance and the gains of the base station and mobile antenna, the received RF power can be adjusted. By changing the power level of the AWGN and interference, the various received signals can be achieved for the simulation of the system.

4.2.4 RF Receivers

The received RF signal is amplified by an LNA and band-pass filtered for image rejection. It is then combined with a local oscillator LO in the mixer to convert the RF signal to an IF signal.

Figure 4-7 shows the block diagram of the RF receiver.

Figure 4-7 RF Receiver Block.

Our eventual goal of the Smart Receiver is to set the bias of each front end component according to the received signal corrupted by interference and noise. However it is very difficult to implement unless circuit level behavior models of each component is available. In this system, for simulation purpose two different RF receivers were used instead of one receiver with variable bias. Table 4-1 shows the performance of the two RF receivers.

Table 4-1 Performance of the Front End Receivers.

Performance	High	Low
LNA Gain (dB)	21	2
LNA Noise Figure (dB)	1.4	3.5
LNA output IP3 (dBm)	8	-16
Mixer Noise Figure (dB)	7	10
Mixer output IP3 (dBm)	10	-10
Mixer LO Rejection	-30	-20
Mixer Image Rejection	-35	-25
Mixer RF Rejection	-30	-20
oscillator phase noise @ 400 kHz	-121	-80

The high performance receiver consists of an LNA, a mixer and a local oscillator of higher performance, while low performance receiver is made up of an LNA, a mixer and a local oscillator of lower performance. The simulation results of the LNA designed in Section 3 were used as references for the LNA specifications. The LNA we designed was centered at 1.9 GHz, however, since there is no propagation model at 1.9 GHz in HP-ADS, the GSM receiver at 900 MHz was used as our model. The specifications of the higher performance LNA were set to a gain of 21 dB, a noise figure of 1.4 dB and a OIP3 of 8 dBm. The specifications of the low performance LNA were set to a to a gain of 2 dB, a noise figure of 3.5 dB and a OIP3 of -16 dBm.

The specifications for the high performance mixer and local oscillator were set according to the GSM specifications [Crols97]. The specifications for the low performance mixer and local oscillator were set significantly worse than those of high performance ones.

4.2.5 Carrier and Timing Recovery

In digital communication systems, the output of the demodulator must be sampled periodically, once per symbol interval, in order to recover the transmitted signal. Since the propagation delay from the transmitter to the receiver is usually unknown at the receiver, symbol timing recovery must be extracted from and applied to the received signal in order to synchronously sample the output of the demodulator.

Furthermore, the propagation delay in the transmitted signal and difference between transmitter and receiver crystal frequencies also results in a carrier offset, which must be estimated at the receiver if the detection is to be phase-coherent.

Figure 4-8 shows the circuit used in the clock and carrier recovery block. This is not the same as the one typically used in GSM, however, for simulation purpose, it was chosen since it is a standard block in HP-ADS. The recovered GMSK modulated signal from the RF receivers is first squared. The spectrum of the signal at the output of the square-law component is centered at twice the input carrier frequency and has tones offset from $2f_{IF}$ at odd multiples of $1/2T$, where T ($3.7 \mu s$) is the symbol duration. The two tones at $2f_{IF} + 1/2T$ and $2f_{IF} - 1/2T$ are filtered out and recombined by frequency multipliers to produce the required carrier at f_{IF} and a clock of period of $2T$ and a duty cycle of 50 percent. The

phase of the clock is such that the positive edge of the clock can be used to sample the I channel of the demodulator output and the negative edge can be used to sample the Q channel of the demodulator.

Figure 4-8 Clock and Carrier Recovery.

The two BPFs can be replaced by PLLs. The spectral purity of the recovered carrier increases as the bandwidth decreases. However the initial transient time increases. Since the two spectral tones are spaced at $1/T$ Hz apart, the bandwidth should be much smaller than this value. In simulation, the bandwidths of both BPF were set at 10 kHz.

Figure 4-9 and Figure 4-10 show the recovered carrier and symbol timing.

The recovered carrier is centered at 70 MHz with a peak power of 7 dBm.

Figure 4-9 Recovered Carrier.

The recovered clock has a period of twice of symbol duration T ($3.7 \mu\text{s}$) with a duty cycle of 50 percent.

Figure 4-10 Recovered Clock Timing.

4.2.6 GMSK Demodulation

As discussed earlier, MSK or GMSK is FSK with a modulation index of 0.5, which is given by

$$s(t) = A \cos\left[\left(\omega_0 \pm \frac{\pi}{2}\right)t + \varphi_0\right] = A \cos\left(\omega_0 t + (\pm 1) \cdot \frac{\pi}{2}t + \varphi_0\right) \quad \text{Equation 24}$$

Where A , ω_0 and φ_0 are the amplitude, frequency, and the initial phase of the signal.

Since the carrier changes phase by 90 degree over one bit period, GMSK is regarded as a continuous phase FSK. The phase smoothly advances or retards 90 deg depending on whether the modulating signal is a 1 or -1.

By following the phase trajectory, the information sequence can be determined. The GMSK signal can be demodulated using orthogonal coherent detectors as shown in Figure 4-11.

Figure 4-11 Coherent GMSK Demodulation.

Coming from the carrier and clock recovery block, the reference LO carrier signal should be synchronized in frequency and phase to the modulated signal for proper demodulation. The clock signal should have a duty cycle of 50 percent and its frequency should equal half the transmitted data rate. Its phase should be adjusted so that the positive edge of the clock occurs at the instant when the eye of the demodulated in-phase signal is maximum, and the negative edge will occur when the eye of the quadrature signal is maximum.

A differential data encoder and a decoder are used to resolve the phase ambiguities introduced by the carrier recovery in the demodulator. Figure 4-12 shows the transmitted signal and the received signal are identical except that there is a propagation delay between them.

Figure 4-12 Transmitted And Received Baseband Signals.

4.2.7 Baseband Signal Processing

A baseband signal processing module is added to measure the system bit error rate, and to select which RF receiver is used according to a certain criteria. Figure 4-13 shows the baseband DSP block diagram. In simulation the transmitted signal is delayed and synchronized with the received signal. In real system training sequence for the adaptive equalizer can be used as the input of the transmitted signal. The total bit counter increments whenever a bit is transmitted (or received) while the error bit counter counts the number of error bit during one data block. The two counters are reset when the total bit counter reaches a length of one data block which could be one or more GSM frames. The two counters are reset when the total bit counter reaches a length of one data block which could be one or more GSM frames.

Figure 4-13 Baseband DSP Block.

In its most simple configuration, when the BER is smaller than 2% for one data block (one or several frames), the system keeps or switches to the lower performance receiver. When the BER is greater than 2% for one data block, the GSM system will keep or switch to the higher performance receiver. When the received signal is of constant power or interference, the simulation ends up in switching between the two receivers. Therefore

more complicated decision block should be used instead of just the BER. Received Signal Strength (RSS) and adjacent channel RSSs can be used as the inputs to the decision block. These will be discussed in Section 4.3.5.

4.3 System Simulation and Performance

A simulation test bench was built in HP-ADS with the system architecture shown in Figure 4-1. The Baseband DSP block is used to measure the BER of the system and determine which RF receiver is used for the following data blocks. Before simulating the entire smart receiver working, the high performance and low performance RF receivers and simulated performance is measured separately in terms of sensitivity, co-channel interference, adjacent channel interference, and inter-modulation as given in the following sub-sections. The specifications of the high performance and low performance receivers are defined in Table 4-1.

4.3.1 Sensitivity Performance

Figure 4-14 shows the sensitivity performance when the high performance RF receiver is used. The received power was adjusted by changing the base station antenna gain. When measuring sensitivity, the GMSK modulated interference and single-tone interference were disabled, while the AWGN was set to -111 dBm. A BER of 2% is shown as star '*' in the following figures. From Figure 4-14 it can be seen that BER drops under 2% when the received power exceeds -102 dBm. Therefore, the sensitivity of the high performance

RF receiver is -102 dBm. Similarly, Figure 4-15 shows the sensitivity with the low performance RF receiver is -82 dBm.

Figure 4-14 High Performance RF Receiver Sensitivity Performance.

Figure 4-15 Low Performance RF Receiver Sensitivity Performance.

4.3.2 Co-channel Interference Performance

The co-channel interference was provided by sending a different random data source through an identical signal transmitter path and added to the desired signal at the mobile antenna. So this co-channel interference is a GMSK modulated signal. The single-tone interference was disabled during this measurement. Figure 4-16 gives the co-channel interference performance when the high performance RF receiver is used. When the co-channel interference is 7 dB below the desired signal, the system BER is under 2%. Similarly, when the co-channel interference is 9 dB below the desired signal, the system BER with the low performance RF receiver is under 2%.

Figure 4-16 Co-channel Interference Performance of High Performance RF Receiver.

4.3.3 Adjacent Channel Interference Performance

The adjacent channel interference was provided by sending a different random data source through an identical signal path with the transmitted signal center frequency offset by 200 kHz, 400 kHz or 600 kHz from the desired signal and added to the desired signal at the mobile antenna. The single-tone interference was disabled during this measurement. Figure 4-17, Figure 4-18, and Figure 4-19 show the adjacent channel performance with the high performance RF receiver when an interference signal is applied to the adjacent channel at ± 200 kHz, ± 400 kHz and ± 600 kHz respectively. The figures show that the system BER is below 2% when the adjacent channel interference at ± 200 kHz, ± 400 kHz and ± 600 kHz was set at 9 dB, 45 dB, and 50 dB above the desired

signal, respectively. Similarly, we can obtain the adjacent channel performance with the low performance RF receiver. System BER is below 2% when the adjacent channel interference at ± 200 kHz, ± 400 kHz and ± 600 kHz was set at 5 dB, 27 dB, and 35dB above the desired signal, respectively.

Figure 4-17 200 kHz Adjacent Channel Interference Rejection Performance of High Performance RF Receiver.

Figure 4-18 400 kHz Adjacent Channel Interference Rejection Performance of High Performance RF Receiver.

Figure 4-19 600 kHz Adjacent Channel Interference Rejection Performance of High Performance RF Receiver.

4.3.4 Intermodulation Performance

A performance degradation will occur when two signals generate a 3rd order intermodulation signal that lies at the desired signal frequency. The system BER performance with the high performance RF receiver was met (below 2%) when the following signals were present: a desired signal of -99 dBm at f_0 , a GMSK modulated signal of -43dBm at f_0+800 kHz and a sine wave signal of -43dBm at f_0+1600 kHz. The two interference signals are 56 dB above the desired signal.

Figure 4-20 shows the intermodulation performance when the high performance RF receiver is used. The system BER with the low performance RF receiver was below 2%

when the following signals were present: a wanted signal of -79 dBm at f_0 , a GMSK modulated signal of -35 dBm at f_0+800 kHz and a sine wave signal of -35 dBm at f_0+1600 kHz. The two interference signals are 44 dB above the desired signal.

Figure 4-20 Intermodulation Performance of High Performance RF Receiver.

4.3.5 System Performance summary

Table 4-2 gives the system performance when the two receivers were used. The system performance of the high quality receiver meets the specification of GSM [Redl95, Crols97].

Table 4-2 System Performance with the Two Receivers.

Performance	High	Low
Sensitivity (dBm)	-102	-82
Co-channel interference (dB below)	7	9
Adjacent channel interference @200kHz (dB above)	9	5
Adjacent channel interference @400kHz (dB above)	45	27
Adjacent channel interference @600kHz (dB above)	50	35
Intermodulation, wanted signal at f_0, two interference at f_0+800 kHz and f_0+1600 kHz (dB above)	56	44

The original scheme was to use BER as the only criteria to make decision. When the BER is smaller than 2% for one data block (one or several frames), the system keeps or switches to the lower performance receiver. When the BER is greater than 2% for one data block, the system will keep or switch to the higher performance receiver. But simulations showed that the system would oscillate, or switch between the two receivers when the desired signal level, noise or interference is steady in between the performance levels of the two receivers as shown in Table 4-2. Received Signal Strength (RSS) and Adjacent Channel RSS (ACRSS) could be used as the inputs to the decision block shown in Figure 4-21. There are five inputs to the decision block. When the answer to any of the five questions is true, the system will keep or switch to high performance receiver. When the answers to all the five questions are false, the system will keep or switch to the low performance receiver.

Figure 4-21 Decision Block.

4.4 Summary

In this chapter the GSM receiver specifications were described in section 4.1. A GSM transceiver system was built using the HP Advance Design System (ADS) and discussed in Section 4.2. Details included discussion on the design of data coding and decoding, GMSK modulation and demodulation, RF transmitter and receiver, propagation channel and baseband signal processing. In Section 4.3, system simulation results including: sensitivity, co-channel interference, adjacent channel interference, and intermodulation performance of the system, were given and analyzed.

5 Conclusion and Future Work

5.1 Conclusion

In this thesis, techniques used in baseband signal processing, modulation, and the RF front end of a digital wireless communication systems are discussed and investigated in Chapter 2. Power consumption is a crucial design specification in portable system. Lower power consumption results in longer battery life or longer standby or talking time. Studies show that most of the power consumed by a handset is drawn from the receiver. As VLSI technology has advanced, the digital part of the receiver consumes lower power, while the power drawn by the analog part of the receiver remains almost the same. Therefore, the design of an analog front end with less power consumption becomes more and more desirable. However, better performance and lower power consumption often contradict each other and make the design complicated.

A 1.9 GHz low noise amplifier was designed in a standard CMOS .35 micron process and presented in Chapter 3. The amplifier provides a gain of 21 dB with a noise figure only 1.4 dB and a OIP3 of -16 dBm while drawing 6.5 mW from a 1.5 V supply. It was also shown that in order to have high performance RF front end, the RF front end needs more power.

Chapter 4 proposed a novel idea to save the power consumed by RF front end receiver (i.e. smart receivers), in which power dissipated by the front end is adaptively controlled by baseband signal processing. When the received signal is strong, the front end components are power reduced (set at low bias) at the expense of lower performance. When the signal is weak, or the interference is high, the front end power is increased to improve performance. In both cases, the minimum system requirements (bit error rate or frame error rate, signal to interference ratio) should be met. A GSM transceiver system with RF and baseband DSP co-simulation bench was built in HP Advanced Design System. The transceiver system includes data coding and decoding, GMSK modulation and demodulation, RF transmitter and receiver, propagation channel and baseband signal processing. The RF receiver's performance is controlled by the baseband DSP. System simulation results including: sensitivity, co-channel interference, adjacent channel interference, and intermodulation performance of the system, were given and analyzed.

5.2 Future Work

A major thrust would be including more signal processing blocks in the simulations, such as speech coding, channel coding, interleaving, equalizer, etc. The overall system performance is highly dependent on these blocks.

Adding Received Signal Strength Indicator (RSSI) to measure signal would also be desirable. The RSSI level can be used as a criteria for power adjusting in the baseband

signal processing as proposed in Section 4.3.5 to prevent oscillation between low and high performance front end receivers.

The study of different failure mechanisms, e.g. noise, interference, distortion could be applied to different solution for different problem. For example, when the received signal level is low, noise is the main source of BER. The smart receiver should provide high gain and low noise figure. When the received signal is very strong, distortion is the main source of BER. The smart receiver actually needs to reduce the gain and provide good linearity.

Circuit level study and simulation of other power adjustable components, such as the mixer and local oscillator, are also desirable. The study should include what should be adjusted and the effect of adjusting them.

It is desirable to have different feedback for the LNA, mixer and oscillator so that performance of each component can be adjusted separately. The ultimate smart receiver would be able to determine which component is responsible for the bit errors and improve only that component, leaving others at low power.

The design of a power variable RF front end components is also desirable. The design could use bias-variable or power supply variable circuits.

It is desirable to construct a prototype with the RF front end circuits and DSP chip or FPGA to do the baseband DSP algorithm for power adjusting.

References

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