A Low Power 8 to 1 Analog Multiplexer for Bio-signal Acquisition System with A Function of Amplification

by

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Abstract

This thesis proposes an ultra low power 8-1 analog multiplexer (MUX) which can deal with low voltage amplitude and low frequency bio-signal, the analog MUX is implemented in IBM 130 nm integrated circuit technology. Also, a bio-signal amplifier with low power consumption, high CMRR, and high gain is connected to the output port of the multiplexer. In this way, the bio-signals can be easily detected and selected.

The challenge of this design is how to transfer such low frequency and low amplitude bio-electricity signals from the input port to the output port with low loss, and low distortion.

For the analog multiplexer design, a parallel transmission gate structure is used to select the desired signal while keeping the power consumption of the eight-channel analog multiplexer to 807nW. For the amplifier design, a three-stage differential operational amplifier structure was used to amplify the weak bio-signal which passed through the transmission gate structures. The amplifier was designed with a high CMRR 106dB and reasonable gain of 66dB.

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List of Acronyms

AAF: Anti-aliasing Filter

ADC: Analog-to-Digital Converter

AgCl: Silver Chloride

ALU: Arithmetic Logic Unit

BW: Bandwidth

CC: Correlation Coefficient

CMRR: Common Mode Rejection Ratio

CMOS: Complementary Metal Oxide Semiconductor

CPU: Central Processing Unit

DC: Direct Current

DEMUX: Demultiplexer

ECG: Electrocardiogram

EEG: Electroencephalogram

EMG: Electromyography

ESD: Electrostatic Discharge

ESR: Equivalent Series Resistance

IA: Instrumentation Amplifier

MC: Monte Carlo

MOSFET: Metal–Oxide–Semiconductor Field-Effect Transistor

MUX: Multiplexer

OPAMP: Operational Amplifier

PCB: Printed Circuit Board

RMS: Root Mean Square

Ron: ON-resistance

SIPO: Serial-in Parallel-out

SR: Slew Rate

TG: Transmission Gate

THD: Total Harmonic Distortion

VTC: Voltage Transfer Curve

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Chapter 1

Introduction

This chapter presents the motivations and the academic contributions of the thesis, and provides a brief thesis outline.

1.1 Motivations

In recent years, electronic instruments such as electroencephalogram (EEG), electrocardiogram (ECG), and electromyography (EMG) instruments play an important role in both academic research and medical fields. The function of these instrumentations is to analyze, process, amplify the collected bioelectrical signals, and then display them, for ease of medical use. So what is bioelectricity? In nature, all of the organisms can generate electricity, thus bioelectricity is the electrical phenomenon of life processes [1]. Any subtle body movement of the human being is associated with bioelectricity. For a healthy person, the changes of bioelectricity in his brain, heart and muscle are very regular. Therefore, we can easily discover the signs of disease by observing the waveform variations of the EEG, ECG and EMG. The information that is derived from bioelectrical signals is essential to therapeutic devices in neurological, cardiac, and neuromuscular applications. In the near future, these bioelectrical signals can be used to help patients further improve their life

quality [2]. In the field of biomedical studies, how to accurately collect, transfer, process the bioelectrical signals is a challenge. Bioelectrical signals have features with very low frequency and very low amplitude. For example EEG signal, the frequency of EEG signals is in the range of 0.5Hz – 100Hz, and the amplitude of it is in the range of 2μV - 100μV. Table 1 below lists the frequencies and amplitudes of some common bioelectricity signals.

Name	Amplitude Range	Frequency Range
ECG signal	1uV-10mV	0.05Hz-100Hz
EEG signal	2uV-100uV	0.5Hz-100Hz
Surface EMG signal	50uV-5mV	0.01Hz-500Hz
EGG (electrogastrogram) signal	50uV-2mV	0.001Hz-20Hz
ERG (electroretinogram) signal	0.5uV-1mV	0.2Hz-200Hz

Table 1: A summary table shows the frequency range and amplitude range of five common bioelectricity signals [3], [4].

Considering the characteristics of the bioelectrical signals, the aim of this thesis is to design an ultra-low-power analog MUX, which can select the multiple low frequency analog bioelectricity signals from the output of the sensors and then supply these signals into a differential bio-amplifier that amplifies the expected signal components while avoiding unwanted noise components. The analog MUX design is based on the premise of sensitivity, because the faint bioelectrical signals are hard to detect and they can be easily affected by external or internal noise. The thesis take low power consumption as the main consideration is because this part of design might be used in some portable and low power bio-electrical devices.

1.2 Contribution

This research is devoted to design a low power 8 to 1 analog MUX with good linearity and low On-resistance (Ron) to accurate select and transmit the expected low amplitude and low frequency bioelectrical signals from different channels. The CMOS transmission gate (TG) with the features of less signal transmission attenuation and low power consumption plays a core role in this analog MUX, and in order to further decrease the signal attenuation, the CMOS TG has been modified to the parallel configuration and being used in each single channel, this parallel TG configuration can effectively lower the Ron compare to the traditional TG, and the lower the Ron, the less the attenuation. By proper sizing the transistors of the parallel TG, Ron can achieve good linearity during the full input swing. However, there is a tradeoff between Ron and power consumption. By lowering the Ron of TG to reduce the signal attenuation, the width of the MOS transistor increases, which will consume more power. Therefore, this research designed the analog MUX with each channel contributing less than 1% attenuation and total power consumption less than 1uW to achieve better device performance. A differential bio-amplifier [5, 6] will be connected at the output of the designed analog MUX, and used to amplify the selected bioelectrical signal. The differential operational amplifier (OPAMP) [7] with a three-stage structure can achieve a high CMRR and good gain for better amplifying the weak bio-signals. This design is based on IBM 130nm integrated circuit

technology, and all the components are highly integrated into a 1mm^2 layout area.

1.3 Thesis Outline

This thesis consists of seven chapters.

Chapter 1: Introduce the motivation, contribution and outline of the thesis.

Chapter 2: Give an overview of bio-signal acquisition system.

Chapter 3: Discuss the analog MUX design methods, and provide the principle.

Chapter 4: Present the implementation and simulation results of the analog MUX and differential amplifier.

Chapter 5: Provide and analyze the Monte Carlo simulation results. Discuss the strategy of layout design and present the layout figures.

Chapter 6: Summarize the thesis and discuss the future work of the research.

Chapter 2

Application and Organization of the design

2.1 Family Medical Monitoring System

As many as one in four US adults has two or more chronic diseases [8]. It is easy to predict that medical services will be in great demand, which leads to a soaring demand for medical equipment. Governments all over the world have to face the same problem, which is lack of medical resources. Family medical monitoring systems can effectively help to solve the above problem. These systems can be regarded as a sort of telemedicine, the core purpose of which is to monitor a patient's health status by installing a monitoring device in the patient's home or other remote locations. The family medical monitoring system has many advantages, for example, it allows people to self-monitor, so that people can easily collect and read their daily health data even at home. Long term health recording is also very useful to patients, especially for disease treatment and prevention. The system can help patients save the time of making reservation and waiting in a hospital and the cost of medical service can be controlled at a lower level. Family medical monitoring system may not be available in developing countries.

With the rapid development of family medical monitoring systems, a series of

affordable and portable home health monitoring devices have been widely used in people's lives. By using these devices, people can monitor their own health condition regularly. Usually, these sorts of systems are signal dependent, and the challenge of designing these systems is how to properly design their bio-signal sensitivity. The following sections will discuss the design from the perspective of the system.

2.2 Bio-signal Acquisition System

Nowadays, in clinical medicine, the bio-signals such as EEG, ECG, and EMG are frequently collected, recorded and analyzed. The characteristics such as extremely low amplitude, low frequency, and vulnerable common mode interference of these bio-signals have become the main barrier when designing a bio-signal acquisition system. Bio-signal acquisition system can be widely used in various locations, such as a patient's home. Typically, the bio-signal acquisition devices should offer low power consumption, small size, and portability. Usually, in bio-signal acquisition systems, the most important module is the analog front end [9].

The basic steps of acquiring the bio-signals is as follows. Firstly, acquire the original bio-signals (consisting of both bioelectrical signal and non-bioelectrical signal) from the sensors or electrodes, then process the bio-signals by passing them through the analog multiplexer, amplifier and filter to get visible and useful signals. Secondly, digitize the processed signals through the analog-to-digital converter (ADC), and transmit the digitized

signals to computers. Finally, computers will receive and analyze these amplified, filtered and digitized the bio-signals. For different design requirements, the above process may be adjusted according to the practical situation. This thesis is mainly focusing on the analog MUX and bio-amplifier modules. Figure 2.1 is a basic structure of the bio-signal acquisition system. It consists of 8 electrodes (the black and grey dots on the head), an 8-to-1 analog MUX, a bio-signal amplifier, an anti-aliasing filter, an ADC and a microprocessor which can control the front devices. The processed results can be shown in a PC monitor.

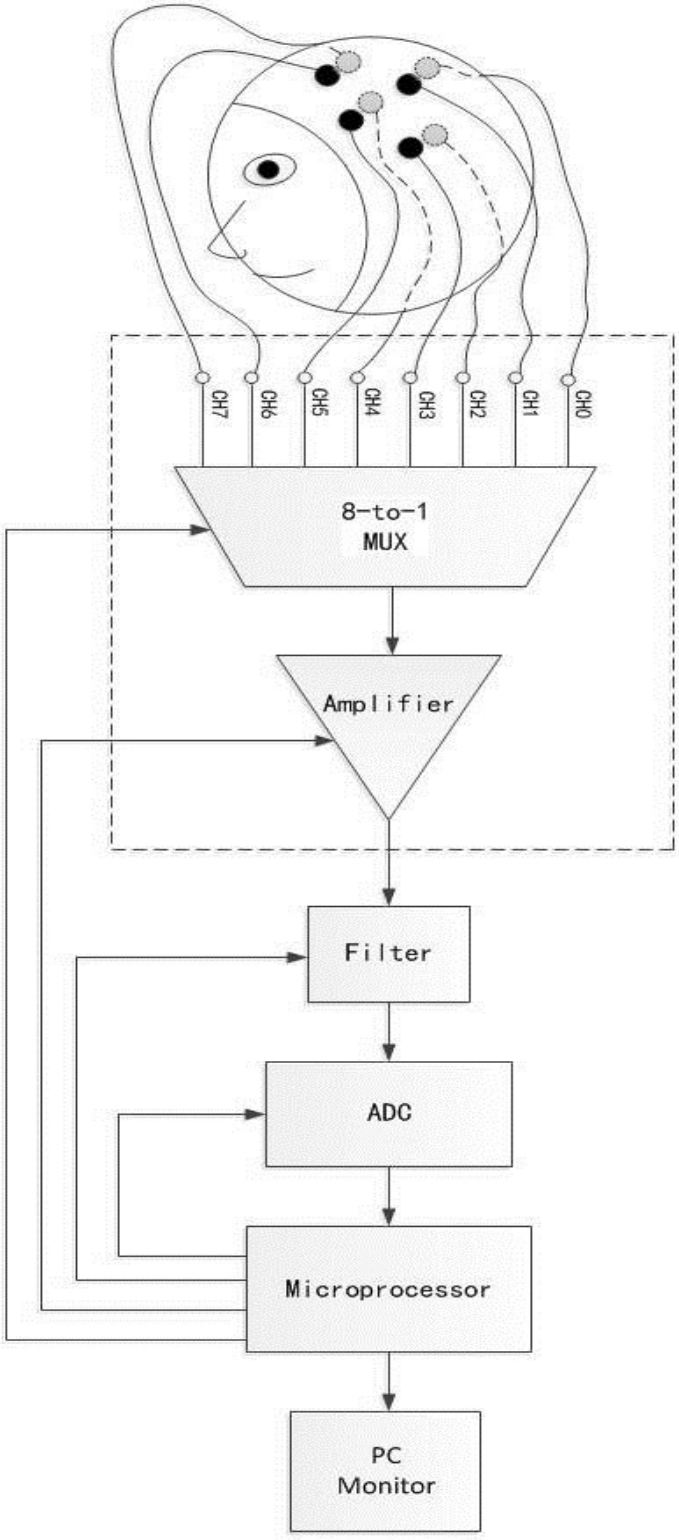

Figure 2. 1: Shows a flow chart of a bio-signal acquisition system

2.2.1 Multiplexer

This thesis is concerned with the design of analog multiplexers. In Figure 2.1, the MUX is directly connected to the 8 electrodes. This MUX is required to correctly select and transmit the bio-signals with low loss. As the output signal from the MUX may contain common mode interference, the design also needs a differential amplifier that can be connected to the output port of the MUX to eliminate the common mode component. To provide differential input signals to the amplifier, a differential MUX is required.

2.2.2 Amplifier

Generally, an instrumentation amplifier (IA) has high Common-Mode Rejection (CMRR) and high gain, and it can be regarded as an analog readout frontend; it is also an important block in the bio-signal acquisition system design. Usually, the CMRR of the IA is required to be more than 80dB, and the differential gain of the IA is required to be more than 40dB. The IA can be designed by using three operational amplifiers (op-amp). Figure 2.2 shown below is a typical three-op-amp instrumentation amplifier circuit.

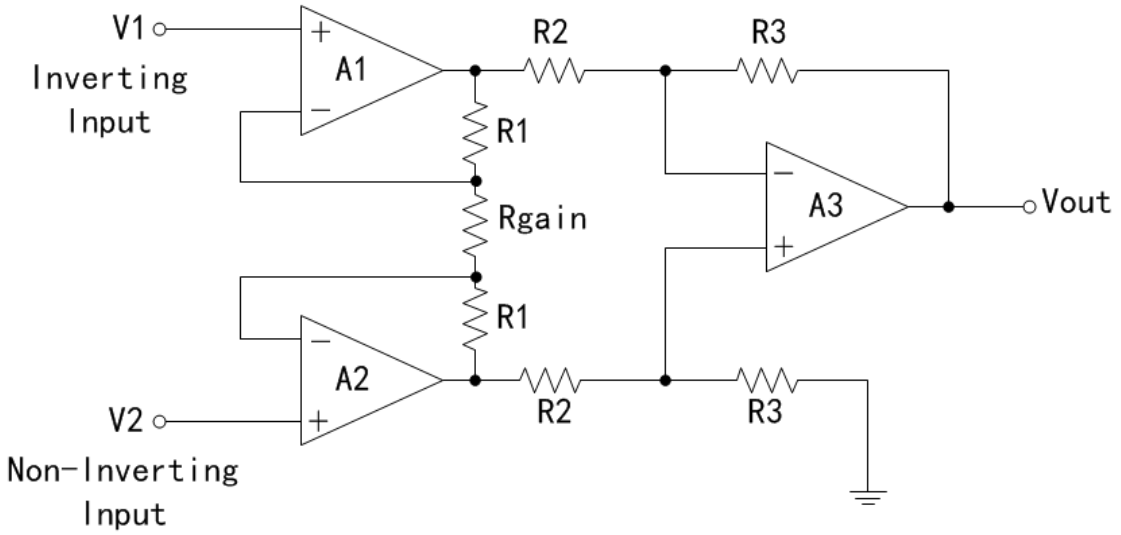

Figure 2. 2: A typical instrumentation amplifier circuit consists of three-op-amps [10]

The gain of this IA is presented as:

$$\frac{\text{Vout}}{\text{V2}-\text{V1}} = \left(1+\frac{2\text{R1}}{\text{Rgain}}\right)\times\frac{\text{R3}}{\text{R2}} \qquad (2.1)$$

An instrumentation amplifier is used to amplify the voltage difference between the differential input signals and reject the common mode voltages at the two inputs. It can extract and amplify those weak bio-signals with very low voltage amplitudes and frequencies from sensors and transducers. A high quality IA should have low DC offset, low noise, high differential gain, high CMRR and high input impedance.

However, in this thesis, instead of designing an IA, a three-stage bio-amplifier with high CMRR and gain is used, in order to lower the power consumption and reduce the layout area required.

2.3 Chapter Summary

This chapter presented the module components, functions and applications of the bio-signal acquisition system. The main function of this bio-signal acquisition system is to reliably and accurately extract the weak bio-signals from the human body, reduce the noise and external interferences.

Chapter 3

Analog Multiplexer Design and Theory

3.1 Methods of Designing Analog Mux

There are two different methods to design an analog MUX for bio-signal acquisition system. One method uses the sample and hold (S/H) circuits with TGs, the other method uses TGs only.

Figure 3.1 shows a block configuration of a single-ended 64-to-1 analog MUX, implemented with S/H circuits and TGs, and controlled by a shift register. The multiplexer consists of four major parts: input buffers, S/H circuits, output buffers and selection circuits (TGS0~TGS63). The transmission gates (TGH0~TGH63) and the capacitors (CH0~CH63) in the sample and hold (S/H) circuit are used to sample the voltage of a continuous analog signal and hold the sampling value for a period of time. The input buffers provide high input impedance to the signal sources which can reduce the signal attenuation. The shift register controls S/H circuits and selection circuits to obtain desired signals from the selected channel.

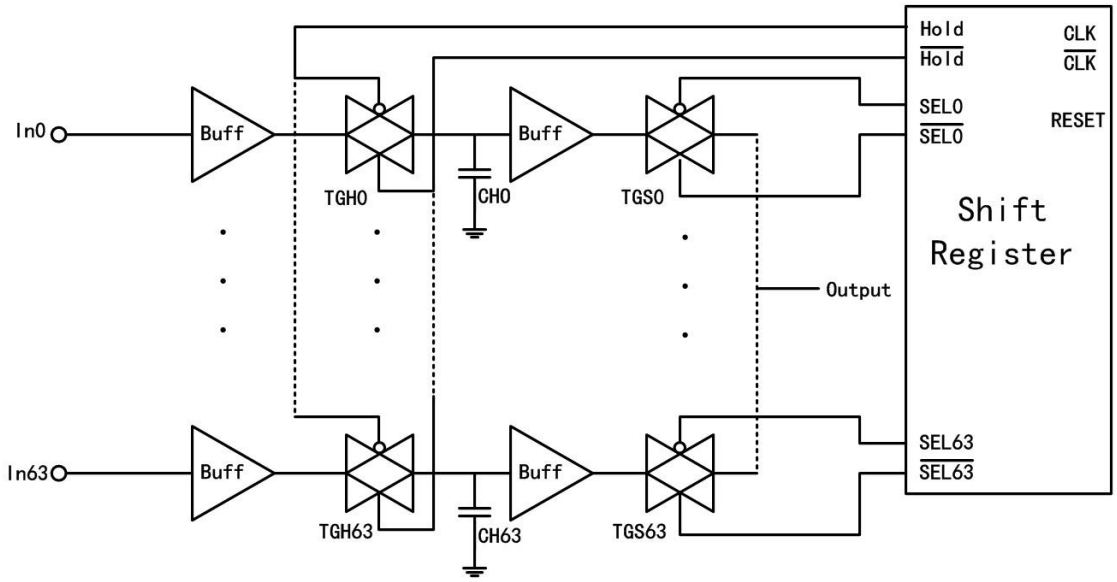

Figure 3. 1: A block diagram of a single-ended 64-to-1 analog MUX [11]

Figure 3.2 is the detailed circuit of one channel from S/H circuit. In this circuit, two source followers with a current source load act as the input buffer and output buffer, and the TG acts as the switching component, and the capacitance acts as the storage device. The input buffer provides a constant voltage to charge the capacitance. The output buffer prevents the capacitance from discharging prematurely [12]. In the sample mode, the capacitance charging follows the change of input signal. In hold mode, the TG turns off, which can cut off the connection between the input signal and the capacitance, so capacitance will hold the charge for a period of time before it is discharged by the output buffer.

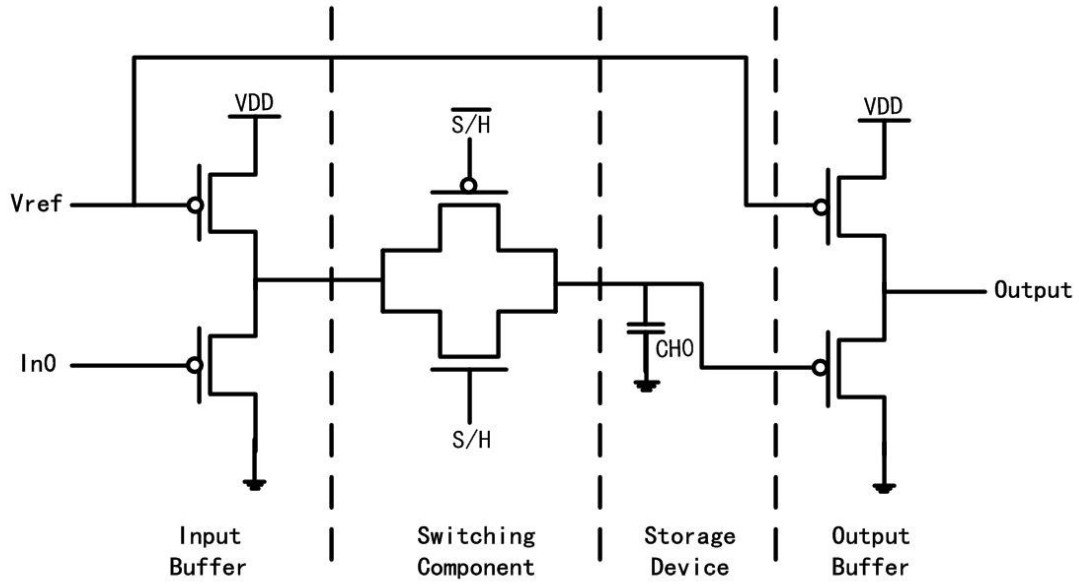

Figure 3. 2: Detailed circuit of one channel S/H circuit [11].

The advantage of the analog MUX in Figure 3.1 is that no glitch will be produced when the MUX switches between different channels. With the S/H circuit, a break-before-make (BBM) MUX is implemented. As all the operations of this MUX are related to the clock signal, and the MUX is controlled by a shift register, so the output signal of MUX has to be a sequential combination of values from the 64 channels. For example, if we need to obtain the signal from channel 54, we have to send 54 clock pulses to reach the desired channel.

In this thesis, the second design method, which builds a differential MUX without using S/H circuits, is chosen. This design method uses a decoder as the control unit. On one hand, the whole circuit is simplified by removing the S/H circuit, which reduces the complexity and power consumption of the circuit. On the other hand, by using a different binary coding combination, the MUX can select any wanted channel rapidly. By using

this design method, the MUX may generate glitches during channel switching, but for long-time recording or monitoring, this tradeoff is acceptable. Therefore, the second design method is chosen for this thesis and the detailed design steps and theory will be presented in the following section.

3.2 Design of Analog Mux

Biosignals are low amplitude and low frequency, which is hard for devices to detect and usually easily disturbed by external or internal noise. Thus when designing an analog MUX, we need to reduce the interference of noise. In addition, in the bio-signal acquisition system, in order to reduce the energy consumption of equipment and save cost, the power consumption of the MUX is one of the most important specification which need to be considered in this design. In this thesis, a low power differential 8-channel analog MUX is presented. The design chooses CMOS Transmission Gate as the core part of the MUX because of its low power consumption and high transmission precision. The main function of this analog MUX is to transmit and select the bio-signals between eight channels. The following paragraphs will present how this analog MUX works.

3.2.1 Pass Transistor

A CMOS n-type transistor or a CMOS p-type transistor can be used as a pass transistor to transmit digital signals. Take the n-type transistor as an example: consider the gate as the select terminal, drain as the data input, and source as the data output, as in Figure 3.3 (a).

When the gate is connected to logic high or "1", the transistor turns on, and data A from the input side can be transmitted to the output side. However, for analog signal transmission, if only one pass transistor is used, it is impossible to completely transmit data A to the output because the analog signal could be affected by the threshold voltage of the pass transistor during the data transmission process. This occurs because the n-type transistor is not good at transmitting the high level voltage. On the contrary, p-type transistors are not good at transmitting the low level voltage. Assume the gate of an n-type transistor is connected to V_{dd}, and the input port is also connected to V_{dd}, the output can only be charged up to V_{dd}-V_{tn}, see Figure 3.3 (b), and for the output and input transient response, see Figure 3.3 (c).

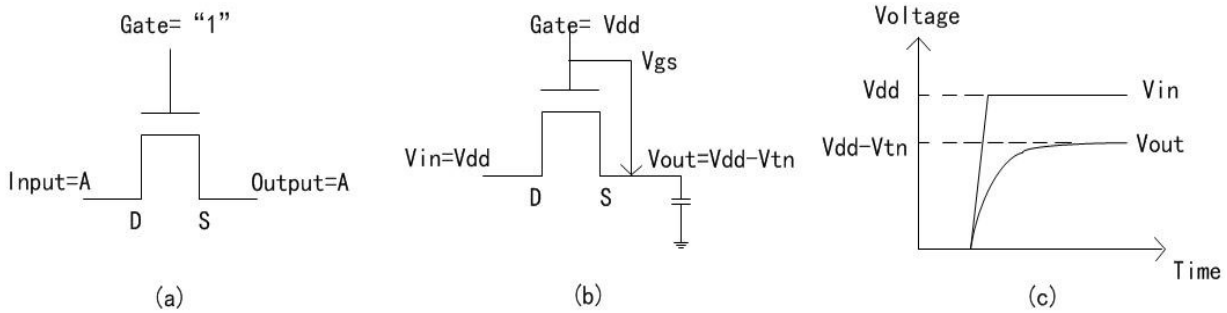

Figure 3. 3: N-type pass transistor and its transient response. (a) is an ideal NMOS pass transistor, (b) shows the practice NMOS pass transistor that can only charge the output node to Vdd-Vtn, (c) shows the input and output transient response of the transistor in (b).

In the practical condition, the above problem will be worse due to the device body effect [13]. To avoid this drawback, the transmission gate structure is introduced.

3.2.2 Transmission Gate

The TG contains one NMOS transistor and one PMOS transistor placed in parallel. One side of the TG is the signal input, the other side is the signal output, and the gates of the NMOS and PMOS devices are connected to the control signals for turning on or turning off the TG. Figure 3.4 shows a simple TG circuit. By using this CMOS transistor structure, we can reduce the effects caused by the threshold voltage of a single transistor. In addition, a transmission gate can reduce the charge injection because of its complementary structure.

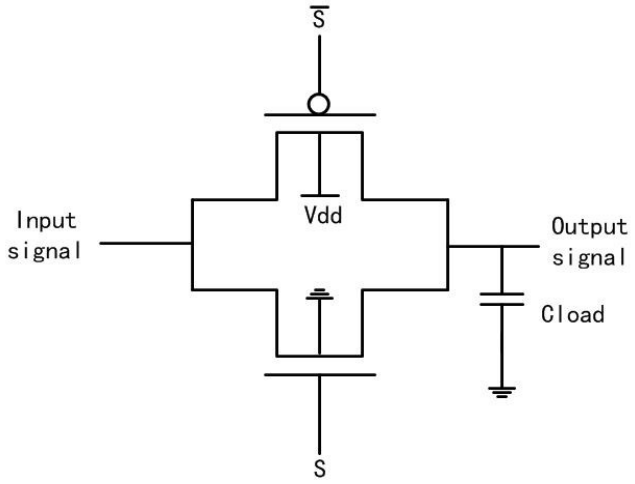

Figure 3. 4 TG circuit

Suppose V_{dd} is connected to the input terminal. If "S" is set equal to "1", the TG is enabled, and the capacitance C_{load} can be charged up to $V_{dd}-V_{tn}$ through the NMOS transistor, while the complementary PMOS transistor can continually charge the C_{load} to V_{dd}. On the contrary, if the input voltage is set equal to 0V, C_{load} is discharged down to $|V_{tp}|$ through the PMOS transistor. The PMOS turns off, and the output is pulled down to 0 by the NMOS transistor. If S is set equal to "0", the TG will be in the off state.

R_{on}: On Resistance

For a TG, one important parameter is its ON-resistance (Ron). Ron can be considered as an equivalent series resistance (ESR) between input terminal and output terminal when TG turns on. Ron can be calculated by using the voltage difference between the input and output terminals divided by the current through TG.

$$R_{on} = \frac{V_{in} - V_{out}}{I_{TG}} \tag{3.1}$$

Figure 3.5 introduces the equivalent TG model with ON Resistance.

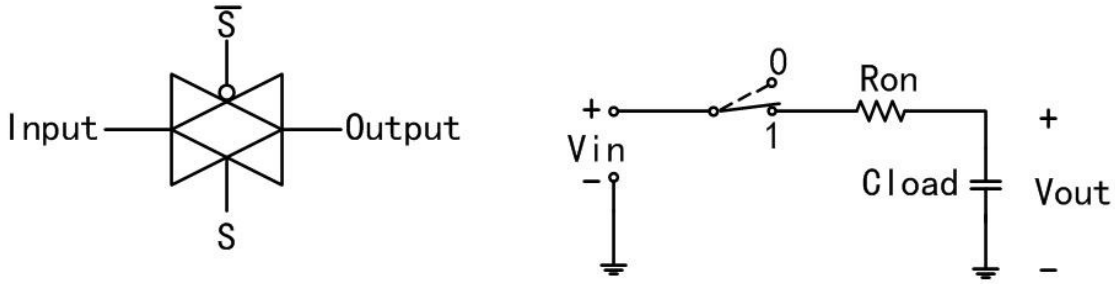

Figure 3. 5 Symbol of TG and equivalent TG model with ON Resistance [14]

There is another way to evaluate the Ron. As TG contains two MOSFETs in parallel, Ron can be regarded as the equivalent parallel resistances of the two MOSFETs. Supposing Rn is the equivalent resistance of the N-type transistor; Rp is the equivalent resistance of the P-type transistor, then Ron can be calculated as:

$$R_{on} = R_n \| R_P \tag{3.2}$$

For long-channel devices, the equivalent resistances of NMOS and PMOS can be presented as:

$$R_n = \frac{1}{\beta_n (V_{dd} - V_{tn})} \tag{3.3}$$

$$R_p = \frac{1}{\beta_p(V_{dd} - |V_{tp}|)} \tag{3.4}$$

Where β_n and β_p are the devices transconductance, which are:

$$\beta_n = k'_n \left(\frac{W}{L}\right)_n = \mu_n C_{ox} \left(\frac{W}{L}\right)_n \tag{3.5}$$

$$\beta_P = k'_P \left(\frac{W}{L}\right)_p = \mu_p C_{ox} \left(\frac{W}{L}\right)_p \tag{3.6}$$

Combine equations 3.2, 3.3, 3.4, 3.5 and 3.6, Ron can be written as:

$$\mathrm{R}_{on} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{dd} - V_{tn}) + \mu_p C_{ox}\left(\frac{W}{L}\right)_p (V_{dd} - |V_{tp}|)} \tag{3.7}$$

Equation (3.7) is used to better understand and estimate the value of Ron. However, for short-channel devices, the values of Ron will not be that accurate by using this equation. Therefore, in this thesis, the accurate value of Ron is extracted from Cadence simulation.

As MOS transistors are nonlinear electronic components, Ron can be also considered as a nonlinear resistance. For a single n-pass transistor or p-pass transistor, Ron will certainly affect the dc accuracy and cause ac distortion. Ron can introduce attenuation, a hundred ohm resistance can introduces a one percent attenuation [15], but this depends on the load. If the input and feedback resistance are sufficiently high, this distortion effect can be neglected. Anyway, the lower the Ron, the better the performance. By using a TG configuration, Ron can be greatly reduced. Figure 3.6 [14, 15] shows the on resistance behavior of NMOS transistor, PMOS transistor and TG. From this figure, it is easy to see that PMOS transistor has a large ON resistance at low input signal voltage, and the input voltage range that a PMOS switch can pass is from $|V_{TP}|$ to V_{DD}. NMOS transistor has a large ON resistance at high input signal voltage, and the input voltage range that a NMOS switch can pass is from 0 to $V_{DD} - V_{TN}$. TG has the relatively low ON resistance at the

full input signal voltage swing, it can pass input signals without threshold voltage drop. Although not shown here, the TG also improves the linearity of the Ron equivalent resistance.

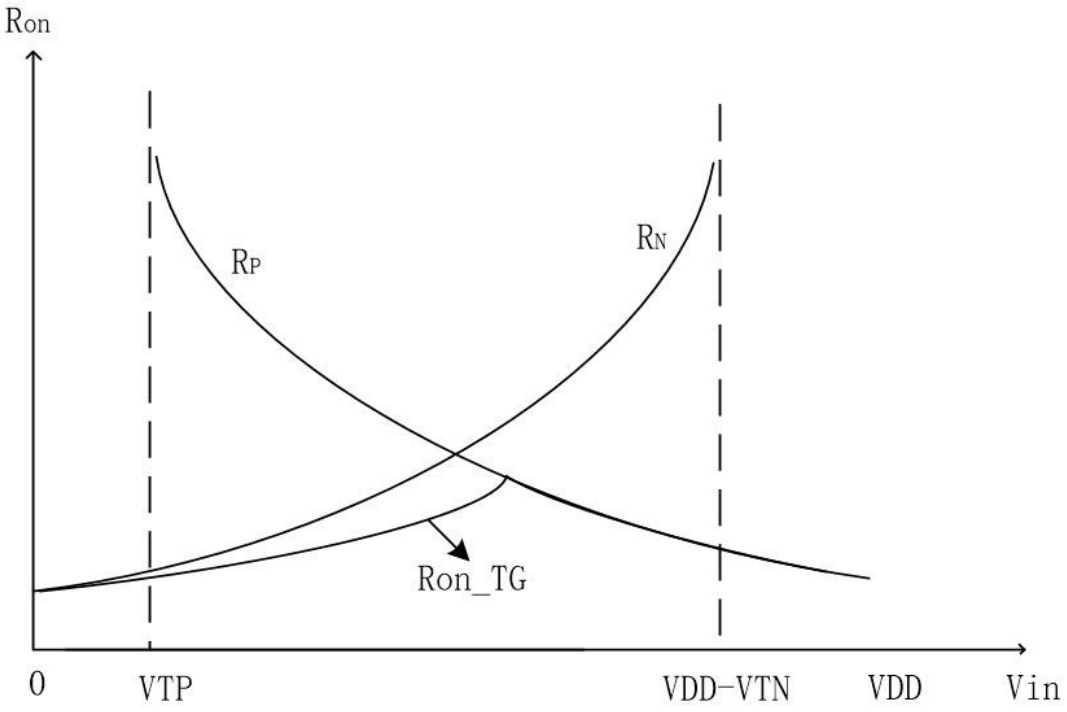

Figure 3. 6: ON resistance behavior for NMOS switch, PMOS switch and TG [14, 15].

First of all, In order to achieve a good linearity of Ron, the PMOS and NMOS transistors in the TG circuit should be sized properly. Since the Ron of the TG varies with the change of input voltage, by sweeping the input voltage and W/L ratio of PMOS and NMOS transistors, a good linearity curve of the Ron for TG can be found, at this point, the PMOS/NMOS W/L ratio can be also determined. In this thesis, 5 is chosen for this $(\frac{W_p}{L_p})/(\frac{W_n}{L_n})$ ratio. Secondly, it is also very important to achieve a low Ron while have the good linearity. When the $(\frac{W_p}{L_p})/(\frac{W_n}{L_n})$ ratio is fixed, through proper sizing the W/L ratio

for each single NMOS transistor in the TG circuit, a relatively low Ron can be achieved. For a single TG circuit, when decreasing the length and increasing the width of the NMOS transistor, the total Ron of the TG decreases, which means the larger the Wn/Ln ratio, the lower the Ron. However, larger size of NMOS and PMOS transistors will also consume more power and more layout space. As the design aim to have a low power analog MUX, this will be a tradeoff. Thus for this thesis, the Wn\Ln ratio of the NMOS transistor is chosen to be 10 to get a Ron less than 100 ohm, because as disscussed above that every 100 ohm Ron contributes 1% attenuation. With this low Ron value, the TG only contributes attenuation no more than 1% in the MUX design which is good. The detailed TG transistors' sizing method and simulation results discussion will be presented in Chapter 4.

Linearity

Total harmonic distortion (THD) [16, 17] is often used to characterize the device linearity. For an ideal TG, the input signal should perfectly pass through the TG to the output terminal without any signal attenuation. However, in practical cases, there are some non-ideal characteristics that will affect the design performance. For this thesis, the Ron of the TG is the largest contributor of the MUX nonlinearity [18]. This is reason why sizing the TG properly is so important that the design is not only aiming at minimize the Ron value, but also considering to achieve a relatively flat Ron without consuming too much power. As the input signal is very low amplitude bio-signals and a TG usually has

relatively good linearity, it is hard to observe the distortion from the output waveform, thus THD is used to measure the linearity of the design. THD is the summation of all the harmonics in the circuit, it can be calculated as the ratio of the sum of the root mean square (RMS) amplitude of all harmonics divided by the RMS amplitude of the fundamental frequency, the equations for THD calculation is shown in equation (3.8) (3.9) (3.10). Figure 3.7 shows a typical harmonic spectrum, with the harmonic amplitudes, the THD value can be obtained by using equations (3.8) (3.9) (3.10) [19], also the frequencies of the harmonics are integer times of the fundamental frequency, such as f, 2f, 3f, 4f, etc. Equations (3.8) and (3.9) are in form of the percentage which measure the data in volts and power, respectively. Equation (3.10) shows the THD calculation in dB. The lower the THD percentage, the less distortion that is present. The THD (dB) is usually a negative value, thus the larger the THD (dB) value, the better the linearity of the circuit. For this thesis, the THD is -86.05dB of a single MUX channel, the detailed simulation plots and results will be presented in the Chapter 4.

Below is the THD equation which the data are measured in volts,

$$THD(\%) = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \cdots + V_n^2}}{V_s} * 100\% \tag{3.8}$$

where V_s is the signal amplitude (RMS volts).

V_2 is the second harmonic amplitude (RMS volts).

V_n is the nth harmonic amplitude (RMS volts).

Below is the THD equation which the data are measured in power,

$$THD(\%) = \sqrt{\frac{P_2 + P_3 + P_4 + \cdots + P_n}{P_s}} * 100\% \quad (3.9)$$

Where P_s is the signal power (dB).

P_2 is the second harmonic power (dB).

P_n is the nth harmonic power (dB).

Equation (3.10) is the THD equation in form of dB,

$$\text{THD (dB)} = 20 * \log(\frac{THD\%}{100}) \quad (3.10)$$

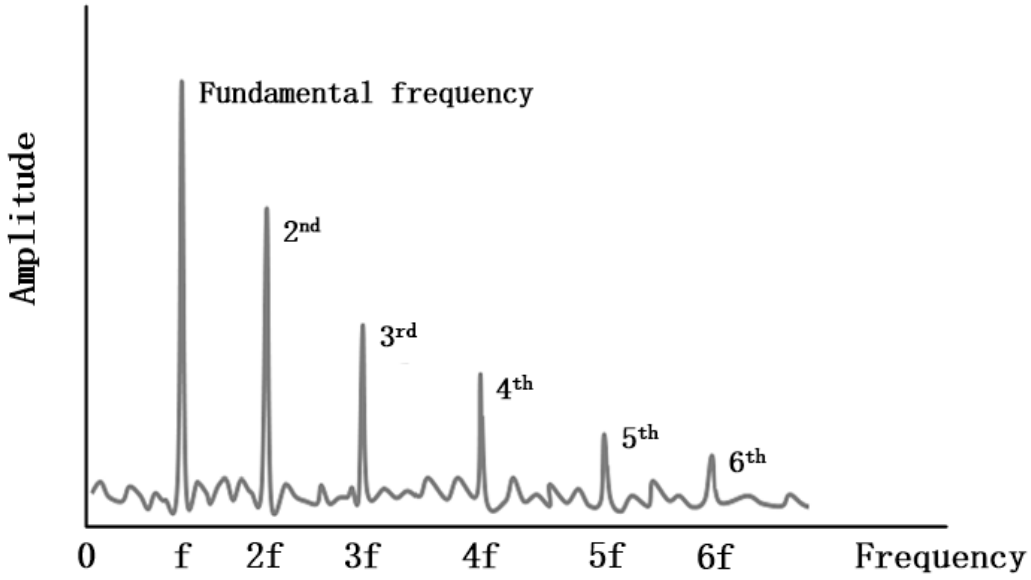

Figure 3. 7: Typical harmonic spectrum, which shows the first six harmonic amplitudes based on frequency domain.

3.2.3 Parallel TG

Since Ron of the TG affects the accuracy of the output signals, this thesis uses a parallel structure to minimize this effect [20]. As is shown in Figure 3.8, this modified TG consists of two paralleled TG; the select terminals S and $\bar{S}$ control the parallel TG operation.

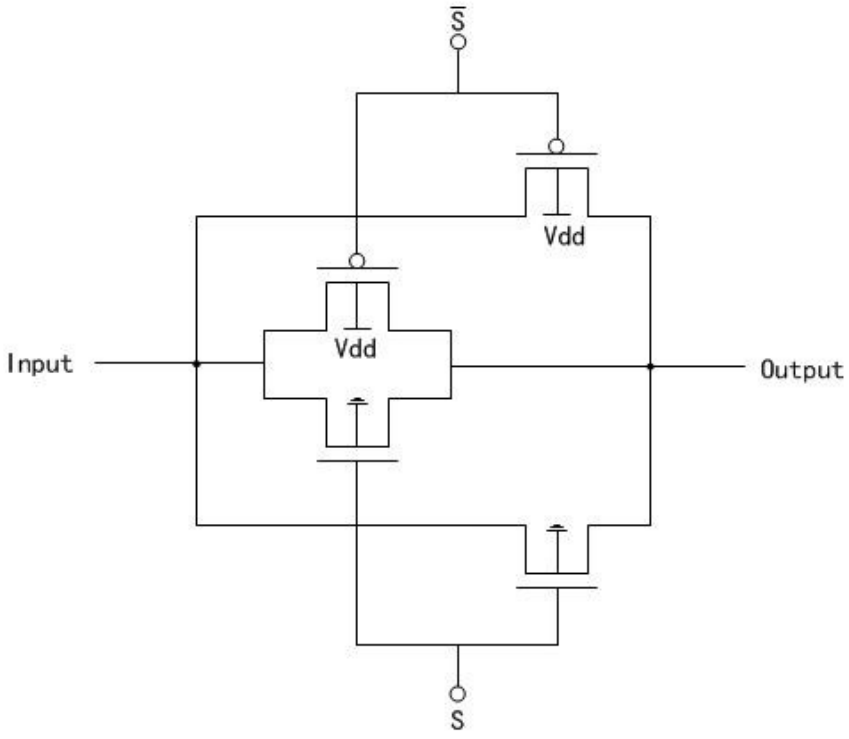

Figure 3. 8: Parallel TG.

The circuit shown in Figure 3.8 can be modeled as shown in Figure 3.9 (a),

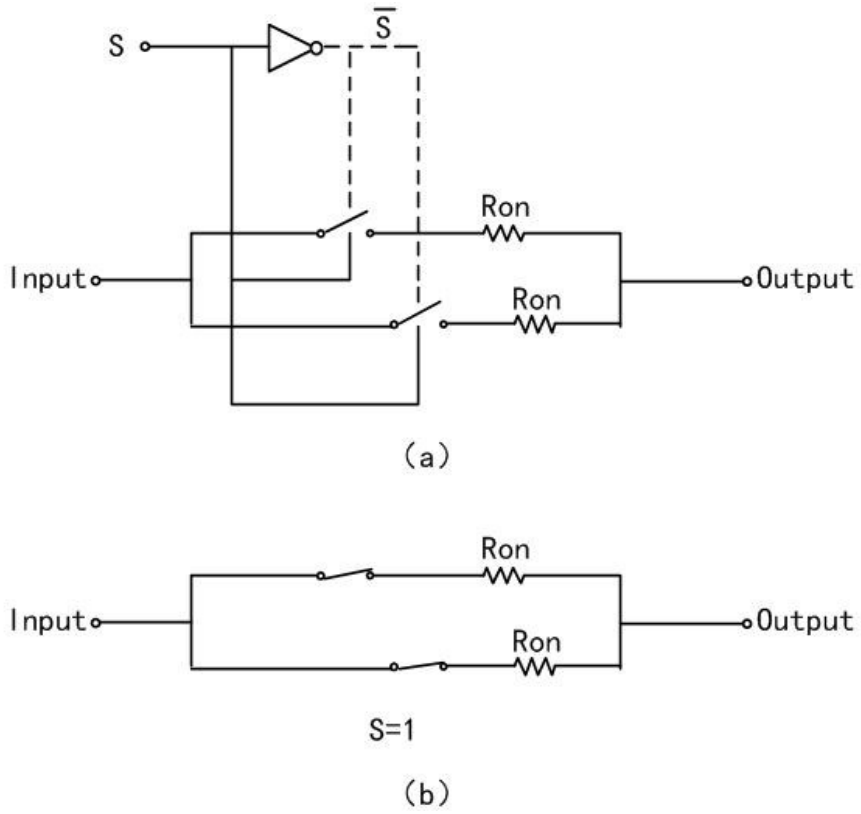

Figure 3. 9: Equivalent circuit of the parallel TG.

When the select terminal S is set to logic "1", then the circuit model shown in Figure 3.9 (a) can be simplified as in Figure 3.9 (b). In this case, the total resistance of this parallel TG can be reduced to half of that of a regular TG. However, increasing the transistor width can also decrease Ron, thus this research compares the difference between the parallel TG configuration and a double-width TG from the aspects of Ron and noise. By using the test bench (Figure 4.1) and ON-resistance equation (3.1), the Ron simulation results of these

two TG configurations are presented in Table 2, it compares the Ron value between parallel TG and double-width TG with different transistors' width and length. From this table, it can be seen that with the minimum transistor size, the Ron of parallel TG is 13% less than that of a double-width TG, when increasing the transistor width and length, this difference of Ron becomes small. In this thesis, in order to achieve a better Ron linearity and relative low Ron value, choose 5 as the PMOS to NMOS Wp/Wn ratio. At this time, the Ron values of parallel TG and double-width TG are very close, but parallel TG is still slightly less than that of double-width TG. Same parallel TG topology is chosen by reference [21, 22] to reduce Ron.

	Ron		
	Wp1= 160n Wn1=160n Ln=Lp=120n	**Wp2=5u Wn2=1u Ln=Lp=360n**	**Wp3=18u Wn3=3.6u Ln=Lp=360n**
Parallel TG (Wp=Wpi, Wn=Wni)	2.495 kΩ	264.9Ω	73Ω
Double-width TG (Wp=2Wpi, Wn=2Wni)	2.868 kΩ	267.3Ω	73.34Ω

Table 2: Shows the comparison of Ron between parallel TG and double-width TG with different transistor width and length.

Figure 3.10 and Figure 3.11 are the TG noise model and the parallel TG noise model, which including all the noise sources such as thermal noise, flicker noise, induced gate noise and channel noise. For this thesis, only the thermal noise [23-25] and flicker noise [26] are important, and since the design is for low frequency signals, thus the flicker noise is the dominant noise. Therefore, the total noise in the parallel TG can be approximately calculated by the MOSFET thermal noise plus flicker noise. The other noise sources [27,

28] should be taken into account for very low noise applications.

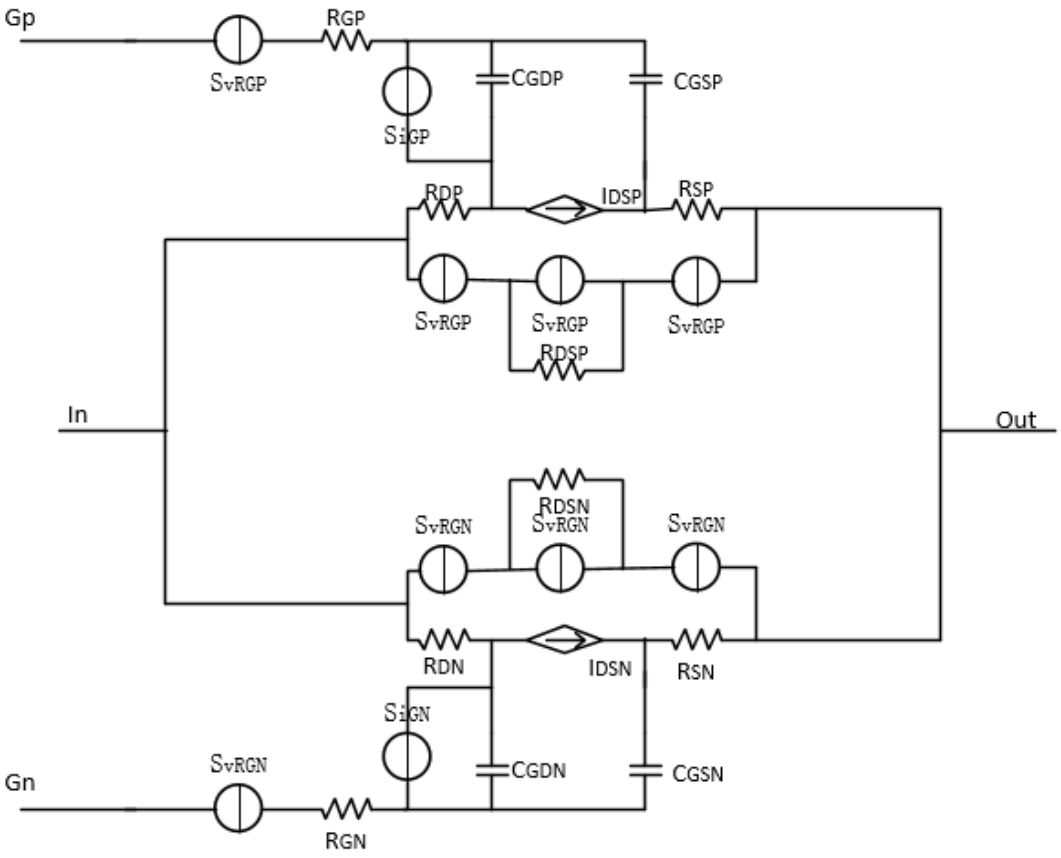

Figure 3. 10 TG noise model

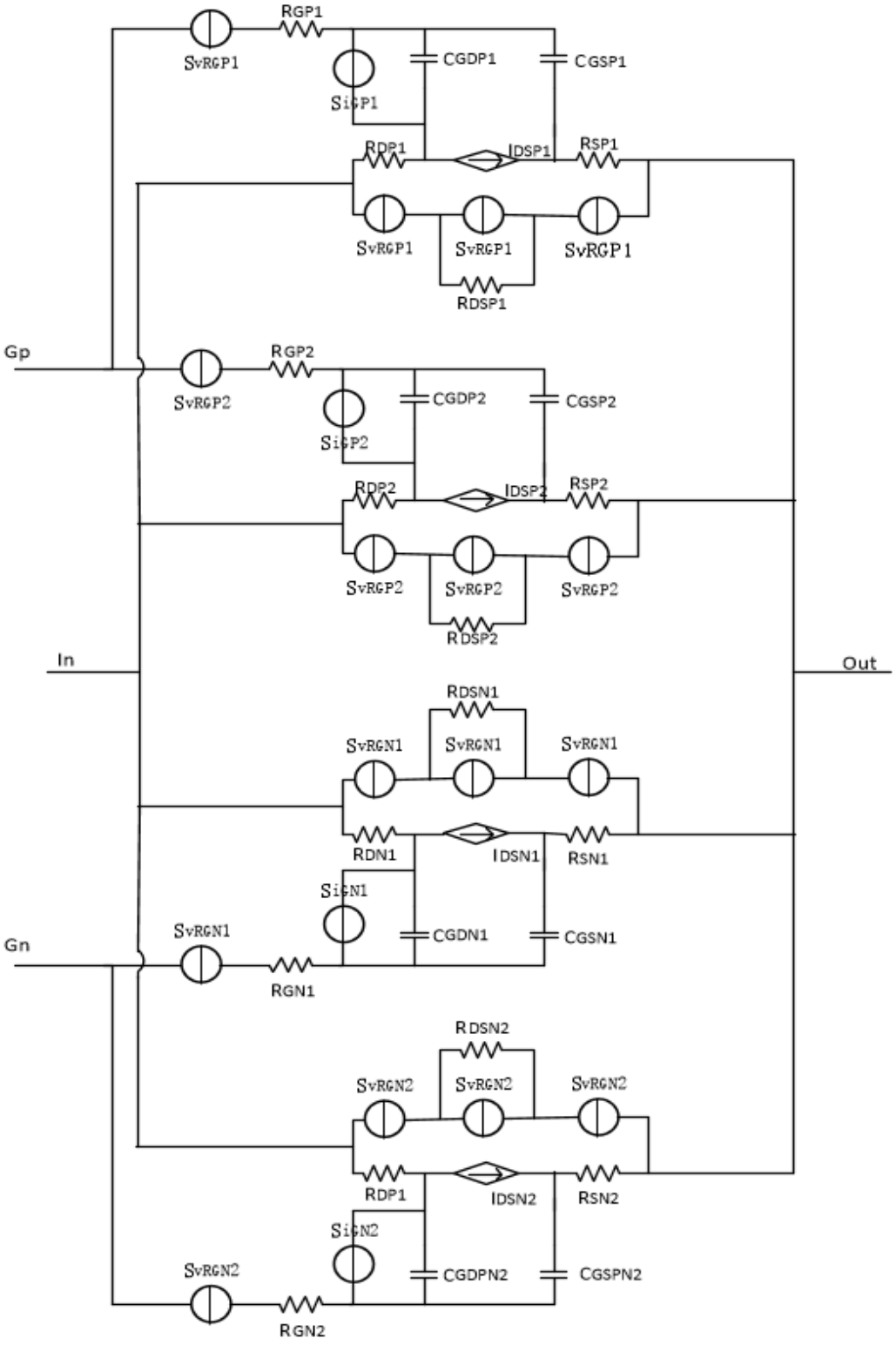

Figure 3. 11 Parallel TG noise model

MOS transistor thermal noise equation is

$$i_n{}^2 = 4KT\gamma g_m \tag{3.11}$$

K is boltzman constant.

T is absolute temperature.

γ is the complex function of the basic transistor parameters.

g_m is the transconductance of the MOSFET.

Usually parameter γ is typically $\frac{2}{3}$ for long channel, and for submicron devices it can be as high as 2.5.

In Figure 3.10 the total thermal noise is produced by R_{DP}, R_{DSP}, R_{SP}, R_{DN}, R_{DSN} and R_{SN}, which can be simplified as the Ron of a double-width TG. In the same way, for Figure 3.11 the total thermal noise is produced by the real resistance of the drain, source terminals ($R_{DP1}, R_{SP1}, R_{DP2}, R_{SP2,} R_{DN1}, R_{SN1}, R_{DN2}, R_{SN2,}$) plus the channel thermal noise of NMOS and PMOS transistors ($R_{DSP1}, R_{DSP2,} R_{DSN1}, R_{DSN2}$), which can also be equivalent to the Ron of the parallel TG. Thus the thermal noise of these two configuration can be compared by using equation 3.12

$$v_n{}^2 = 4KTR\Delta f \tag{3.12}$$

Δf is the frequency bandwidth over which the noise is measured.

As mentioned above, Ron of the parallel TG is smaller than that of double-width TG, thus the thermal noise of the parallel TG configuration is smaller.

Flicker noise (1/f noise) exists in almost all electronic devices, its power spectral density is in inverse proportion to the frequency. It mainly occurs in low frequency designs, as for high frequency application, white noise is the dominant noise.

MOS transistor flicker noise equation [29] is

$$S_{id\,(f)} = \frac{KF * {I_{ds}}^{AF}}{C_{ox} * {L_{eff}}^{2} * f^{EF}} \tag{3.13}$$

Where KF is the process-dependent constant noise parameter.

AF is the flicker noise exponent.

EF is the flicker noise frequency exponent.

f is the device operating frequency.

C_{ox} is the MOSFET gate oxide capacitance per unit area.

L_{eff} is the effective channel length.

For parallel connected MOSFET, the flicker noise [30] is given by

$$S'_{id\,(f)} = \frac{1}{N} * \sum_{j=1}^{N} S_{idj\,(f)} \tag{3.14}$$

Where N is the number of MOSFETs connected in parallel.

$S_{idj\,(f)}$ represents the flicker noise for the j^{th} device.

By combining the equation 3.13 and equation 3.14, when width is doubled, the drain current becomes lager, therefore the flicker noise of the double-width TG configuration is doubled of that of the parallel TG configuration. However, this theoretical calculation only represents a rough noise comparison. To get more accurate input referred noise values between these two configurations, the noise simulation can be done in Cadence. Table 3

shows the comparison of noise performance for a TG comprised of paralleled MOSFETs and a TG designed with double-width MOSFETs. From the table, it can be seen that the parallel TG has less noise (within the targeted EEG bandwidth). Therefore, the parallel TG structure is chosen for this thesis.

	TG	**Parallel TG**	**Double-width TG**
Transient Noise	5nV	3.8nV	4.8nV
Noise in Frequency Domain	5.6nV/$\sqrt{\text{Hz}}$	3.9nV/$\sqrt{\text{Hz}}$	4.3nV/$\sqrt{\text{Hz}}$

Table 3: Noise performance comparison for different TG configurations

3.2.4 The Control Circuits

Figure 3.12 shows part of one channel circuit of the analog MUX. There are 3 inputs and 1 output in this circuit. The 3 inputs are the enable signal, the select signal and the data input signal. The enable signal controls the MUX circuit to turn on or turn off, while the select signal determines which channel is selected to transmit the data information. For example, if the enable signal is “0”, M1 turns on, M2 turns off, Vdd or logic “1” is passed to the PFET gates of parallel TG and “0” is passed to the NFET gates of parallel TG, then the TG is off, no data information will be transferred. When the enable signal is “1”, the select signal can be passed to the parallel TG. According to the logic value of the select signal, TG can be controlled to turn on or turn off, thus, the selection of a channel is achieved.

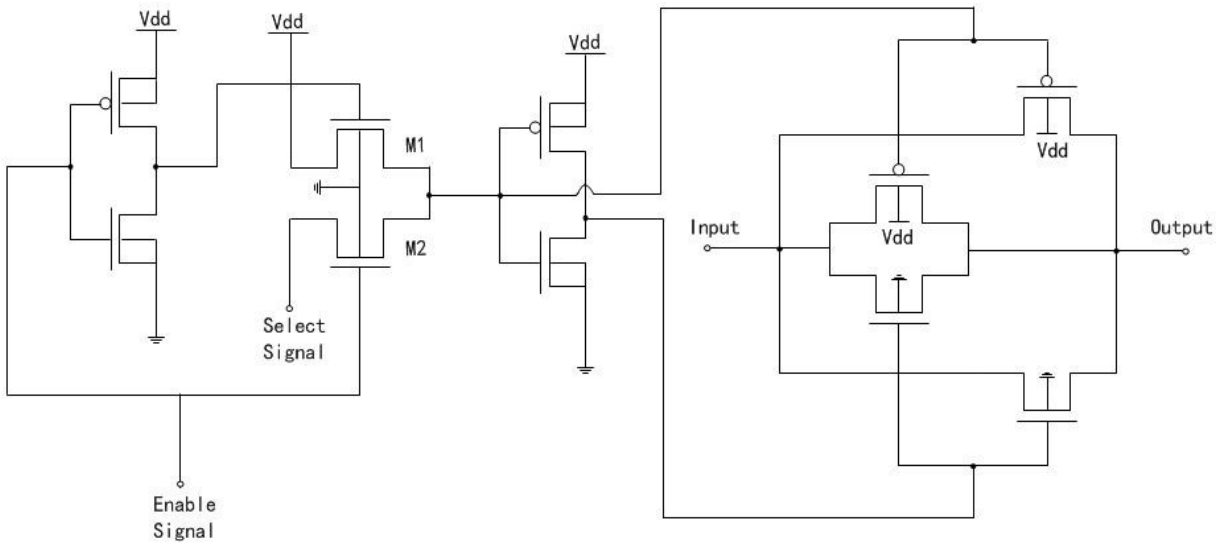

Figure 3. 12 shows the single channel circuit of the MUX, the enable signal controls the entire MUX to turn on or turn off, the select signal controls the parallel TG to turn on or off.

In this design, $\mu_n = 440\ \frac{cm^2}{v \cdot sec}$, $\mu_p = 94\ \frac{cm^2}{v \cdot sec}$, the electron mobility is 4.68 times greater than hole mobility. Therefore for the above inverter, the width of the PMOS transistor is chosen to be five times larger than the width of NMOS transistor, which can make the inverter operate in a symmetrical fashion with respect to its voltage transfer characteristic. A symmetric inverter [31] has equal rise time and fall time, which is helpful to reduce the jitter in the output signal.

In order to connect with the following differential amplifier, each channel is designed into a differential structure, which combines two channel circuits (Figure 3.12) together to form a completed single channel of the MUX. Figure 3.13 is a brief block structure of the differential bio-signal MUX with amplification function. By using this structure, the common mode effects can be reduced.

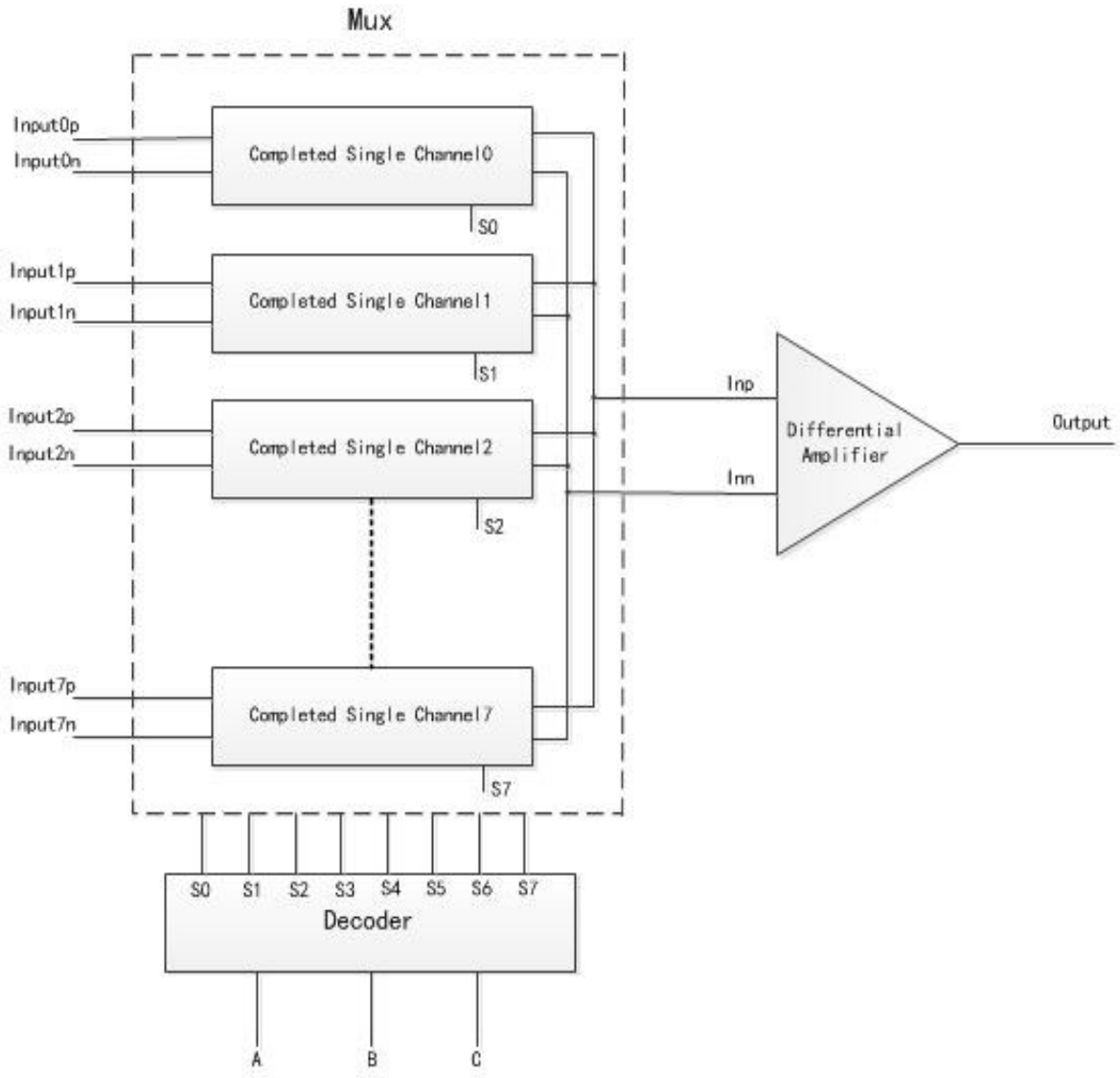

Figure 3. 13 shows the brief block structure of the differential MUX with amplification function.

3.2.5 Digital Decoder

There are two well-known methods for MUX to select a channel; one uses a shift register, the other one uses a decoder. Figure 3.14 illustrates the structure of a serial-in parallel-out (SIPO) shift register. It has two input ports and 8 output ports. The input ports are Clock and Reset. When the Reset is enabled, all the Q outputs are set to "0". No channel

is being selected. Then the $\overline{Q}$ in the last flip-flop will be set to "1", this initial data input logic "1" will be transited to the D port of the first flip-flop, the output of first flip-flop S0 will give logic "0" to the first channel of the MUX, then the MUX channel will turn on (see Figure 3.12). At the rising edge of the Clock signal, the logic "1" will be passed to the second flip-flop, then the second channel of the MUX will be selected. In this way, each channel can be selected sequentially.

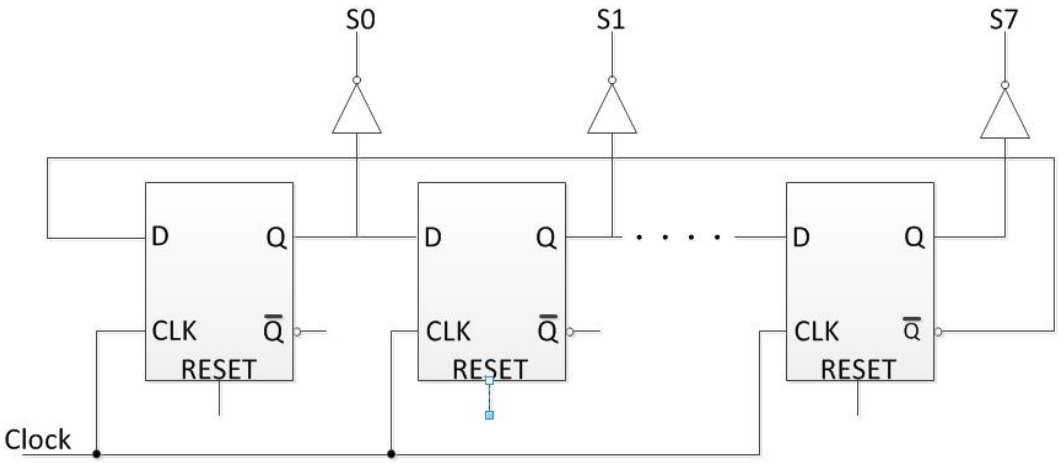

Figure 3. 14: SIPO shift register [10].

However, using a shift register to select channels has limitations. For example, the clock signal determines the switching time between different channels; if the MUX has lots of channels and the last channel needs to be selected, then we have to wait until the previous channel selections are finished. A decoder can overcome the above drawbacks. Figure 3.15 shows a 3-to-8 digital decoder. According to the different combination of the binary codes, this decoder may select any channel at any time.

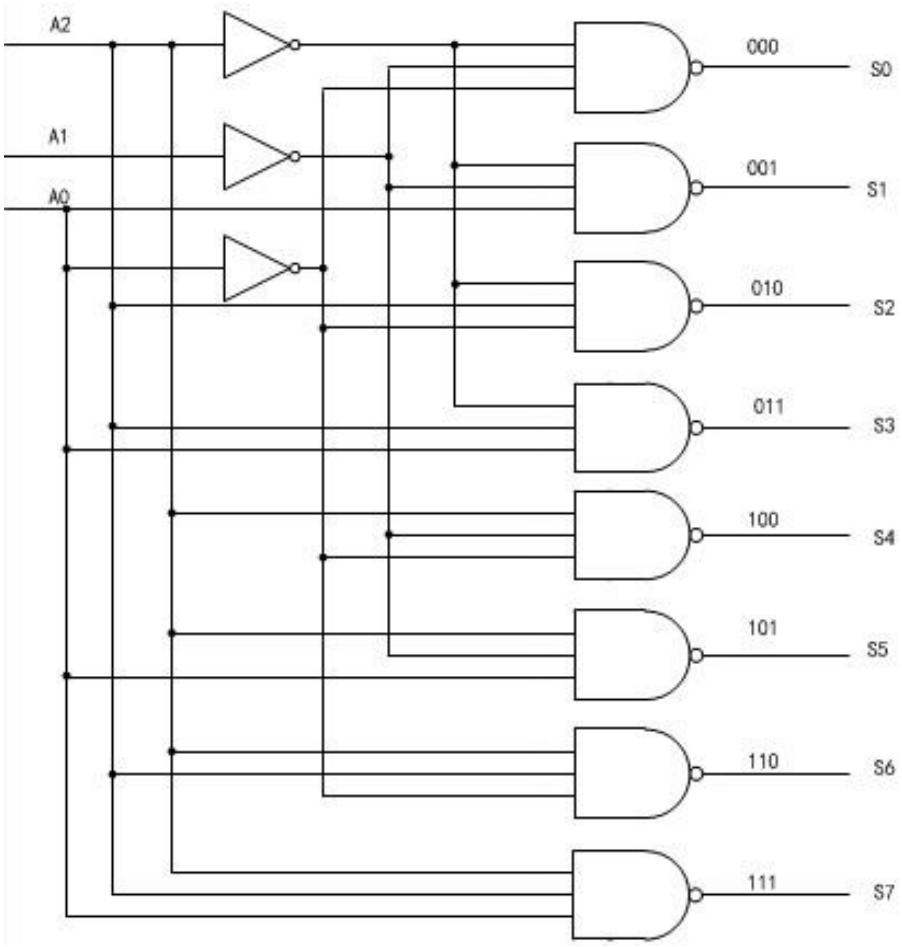

Figure 3. 15: 3-to-8 digital decoder.

Usually, a decoder has n inputs and 2^n outputs. By decoding the binary codes from the n inputs, a decoder can select one line of the 2^n outputs. A common type of decoder is the line decoder, it takes an n-digital binary number and converts it into 2^n unique output lines. This design uses a 3-to-8 line decoder to select one of eight channels of the analog MUX.

3.3 Chapter Summary

This chapter aims to design an analog MUX which can select and transmit low amplitude and low frequency bio-signals with less loss at the output terminal. This 8 to 1 analog MUX is implemented by using the parallel TG structure as one single channel switch, and by proper sizing the PMOS and NMOS transistors in the TG, a low Ron and good Ron linearity can be achieved, and then the analog signal can be transmitted with less attenuation, the detailed TG sizing method is presented in Chapter 4. A 3 to 8 digital decoder is used as the control circuit to flexibly select any desired channel from eight channels of the MUX. In this design, the single channel switch is built in a differential structure to connect with the next stage differential amplifier for reducing the common mode interference.

Chapter 4

Implementation and Simulation

This chapter will present the design specifications and simulation results of the analog MUX and bio-amplifier. The simulation tool is Cadence 6 and the design is implemented based on IBM 130nm technology.

4.1 Design Specification

The designed analog MUX and the three-stage bio-amplifier can be used in the bio-signal acquisition system. The specifications of the bio-amplifier design are listed in Table 4.

Parameters	**Specifications**
Gain	≥ 40dB
CMRR	≥ 80dB
Phase Margin	≥ 45deg
Power Dissipation	≤ 1mW

Table 4 Specifications for the bio-amplifier

4.2 Implementation of MUX

4.2.1 TG Design

As discussed in Chapter 3, properly sizing the TG circuit is the core of designing the analog MUX, and how to choose Ron is an essential measure of the TG performance [32]. Figure 4.1 shows the Ron test bench of TG. In the figure, SEL is set to logic high to keep the switch on, the Ron of the TG is the subtraction of input and output voltage divided by the current going through the TG.

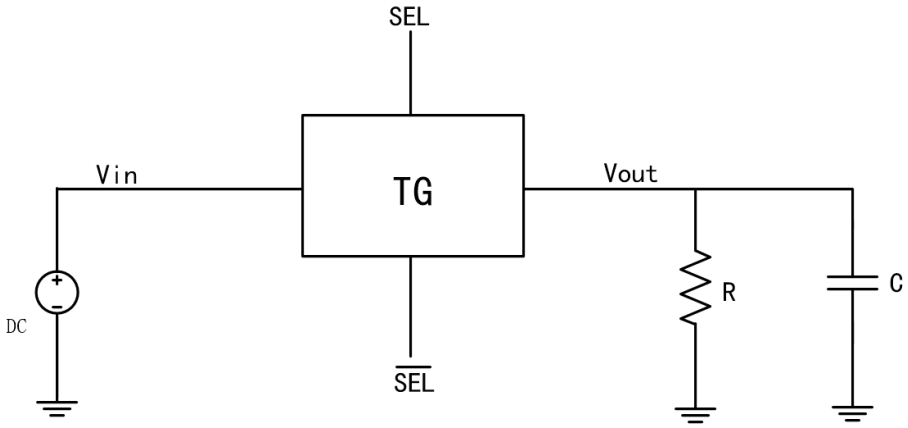

Figure 4. 1 On-resistance test bench for TG circuit.

Firstly, the design choose a small length value for the PMOS and NMOS transistors in TG to achieve a lower Ron, say Ln=Lp=360n (the minimum length in 130nm technology is 120nm, but if choose the minimum length, in the layout contact cannot be placed). When fix NMOS Wn/Ln ratio, by parametric sweeping (Wp/Lp)/(Wn/Ln) ratio from 1 to 10, the Ron of the TG is shown in Figure 4.2, from the figure, it can be seen that when Wp/Wn ratio is equal to 5, the Ron curve is more flat which means the linearity of the Ron is comparatively good.

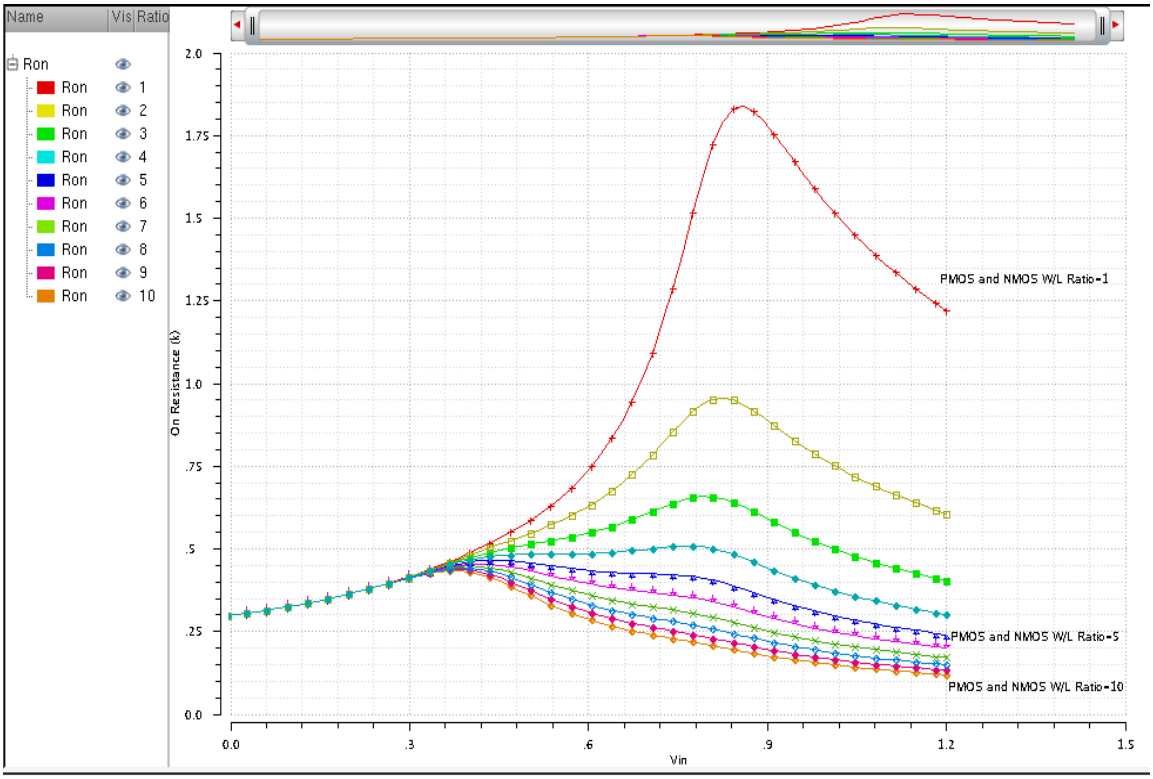

Figure 4. 2 shows the Ron versus Vin plot with different PMOS to NMOS W/L ratio.

Secondly, when Wp/Wn ratio is fixed, through parametric sweeping Wn/Ln ratio, a relatively low Ron value can be found. Figure 4.3 shows the Ron versus Vin plot for different NMOS Wn/Ln ratios. It can be seen from the figure, the larger the Wn/Ln ratio, the lower the Ron, when Wn/Ln is equal to 10, a relatively low Ron value is achieved. The maximum Ron value is equal to 90.8 ohm at 446mV input voltage, and the calculated average Ron value is about 73 ohm over the entire input voltage swing. However, large NMOS and PMOS transistor size will consume more space in the layout. Therefore, the Wn/Ln at Ron = 90.8 ohm is chosen for this design because as stated in Chapter 3 every 100 ohm Ron contributes 1% attenuation. With Wn/Ln ratio is equal to 10, the TG will only contribute attenuation less than 1%, and since the length Ln=360n is chosen, then

Wn=3.6u. In conclusion, the length of PMOS and NMOS transistor is choose to be 360n, while the width of NMOS transistor is set to be 3.6u and the width of PMOS transistor is set to be 18u for TG design.

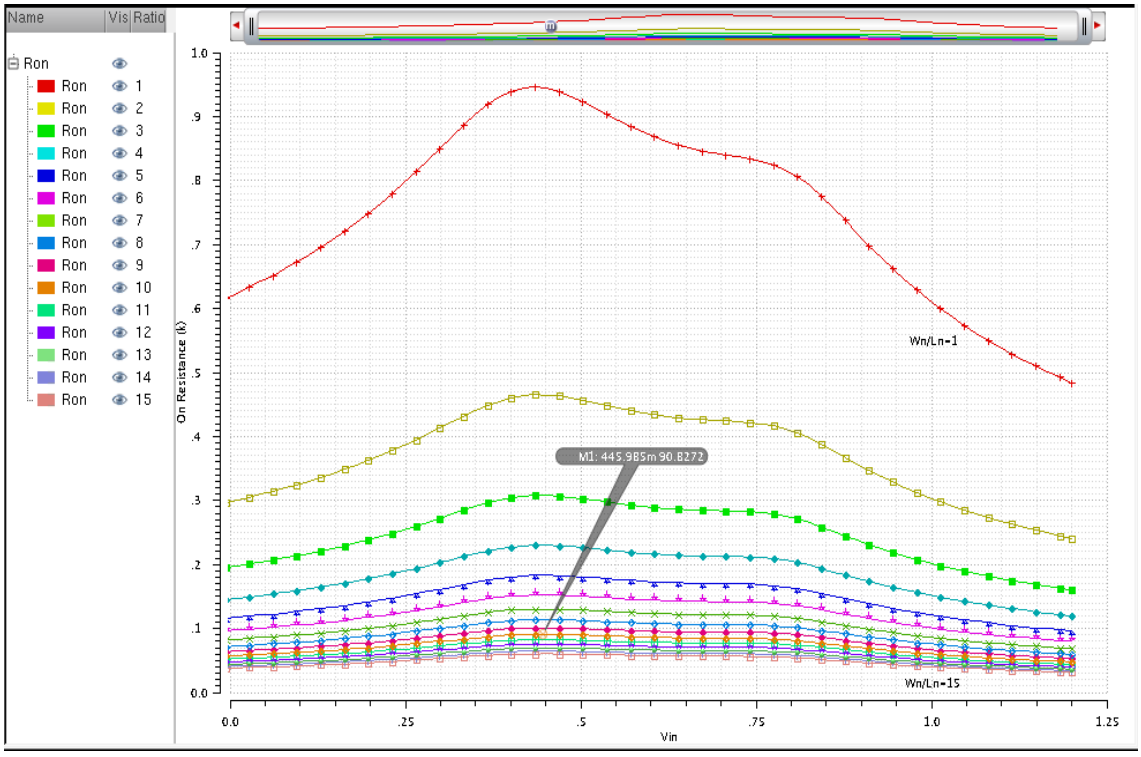

Figure 4. 3 Ron versus Vin plot with different NFET Wn/Ln ratios.

4.2.2 Single Channel Switch Design

Figure 4.4 is a single channel switch of the 8 to 1 analog MUX. The select terminal is used to control this channel turning on or off by setting the select signal to logic "1" to keep all the channels are in "ON" state. The select signal is used to turn on all the PMOS transistors in TGs, and its inversed signal is used to turn on all the NMOS transistors in TGs.

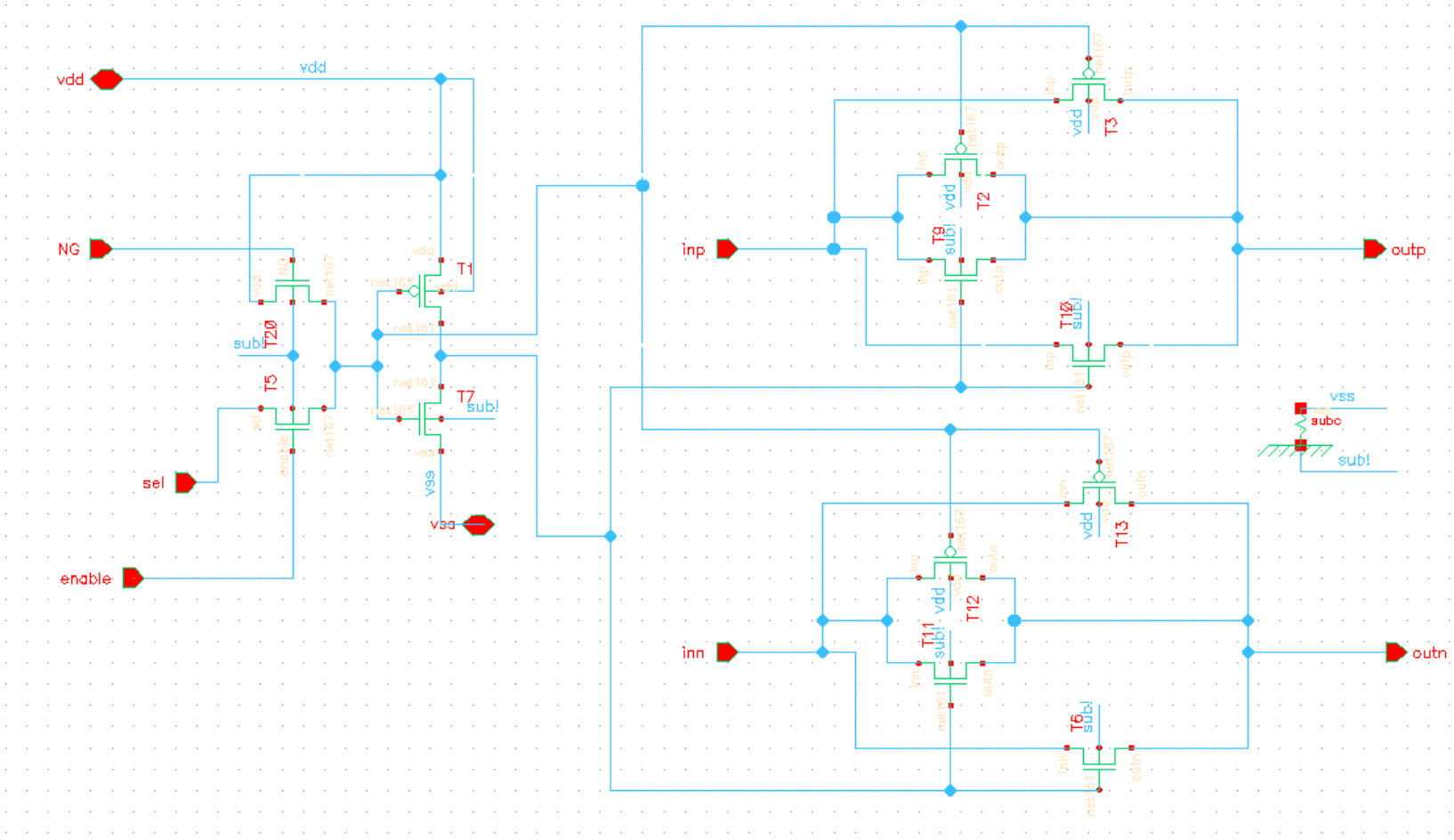

Figure 4. 4 Single channel switch of the 8 to 1 analog MUX

To properly size the inverter in Figure 4.4, the switching threshold voltage, V_M, is introduced, which is defined as the point where $V_{IN} = V_{OUT}$. In the voltage transfer curve (VTC) of an inverter, the most desirable location for the V_M is the middle of the available voltage swing, which is the $V_{DD}/2$ [13].

For short channel device, the transistors are assumed as velocity-saturated devices, the expression [33] of $(W/L)_P/(W/L)_N$ is,

$$\frac{(W/L)_p}{(W/L)_n} = \frac{k'_n V_{DSATn}(V_M - V_{Tn} - V_{DSATn}/2)}{k'_p V_{DSATp}(V_{DD} - V_M + V_{Tp} + V_{DSATp}/2)} \tag{4.1}$$

Where $k'_n = \mu_n C_{ox}$,

$k'_p = \mu_p C_{ox}$,

V_{DSATn} is the velocity − saturated V_{DS} of n − type transistor,

V_{DSATp} is the velocity − saturated V_{DS} of p − type transistor,

V_{Tn} is the threshold voltage of n − type transistor,

V_{Tp} is the threshold voltage of p − type transistor.

For long channel devices, the expression can be derived as,

$$\frac{(W/L)_p}{(W/L)_n} = \frac{k'_n (V_M - V_{Tn})^2}{k'_p (V_{DD} - V_M + V_{Tp})^2} \tag{4.2}$$

As the inverter in this design is a short channel device, so equation (4.1) is applied; the ratio of PFET and NFET from calculation is approximately equal to 5.

For this design, in order to get a good performance inverter and PMOS to NMOS W/L ratio more accurate, the VTC curve of the inverter for the single channel switch is shown in Figure 4.5. By sweeping the PMOS to NMOS W/L ratio around the estimated value 5, it can be seen from the figure that when the ratio is equal to 5.5, at M_5 point (VDD/2), the output voltage is equal to the input voltage which means the inverter has a precise switching from logic "low" to logic "high" level and vice versa.

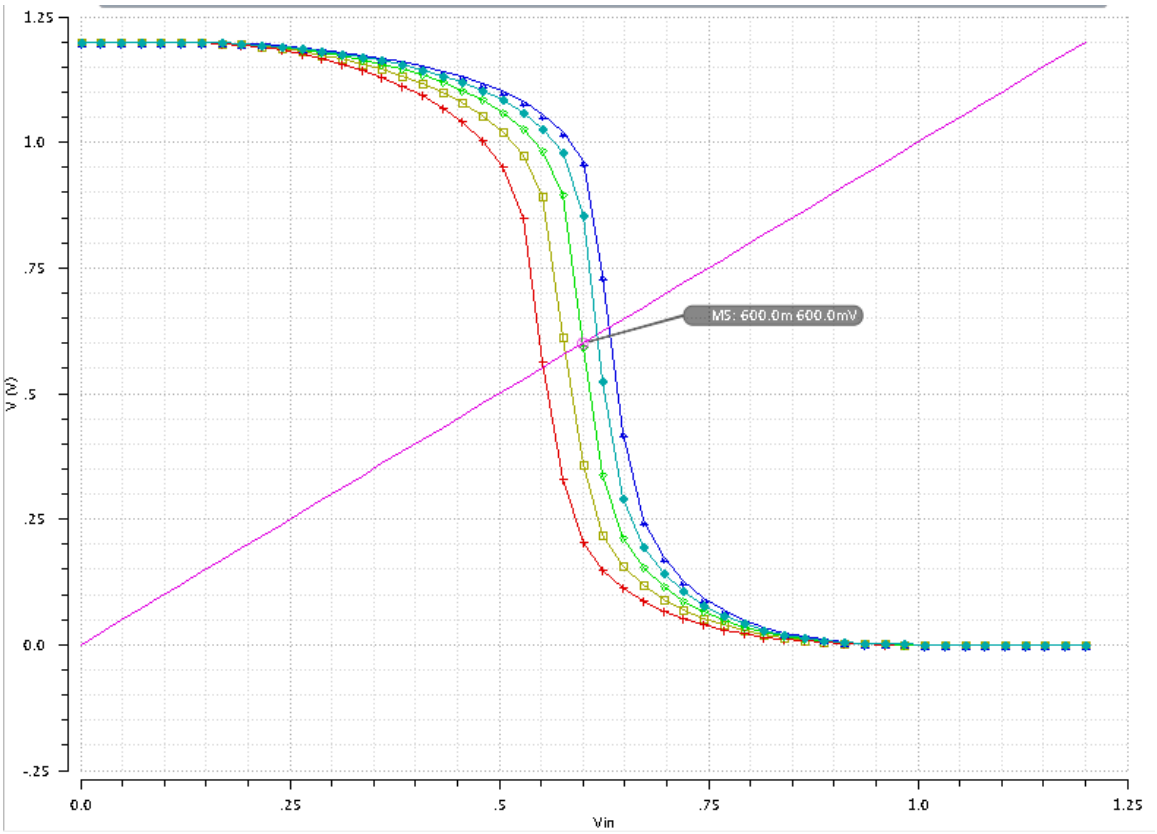

Figure 4. 5 The VTC curve of the inverter for single channel switch

Transistor sizes of the single channel switch is listed in the below Table 5

Type	Transistor	Width	Length
NMOS	T5, T7, T20	720n	360n
	T9, T10, T11, T6	3.6u	360n
PMOS	T1	4u	360n
	T2, T3, T12, T13	18u	360n

Table 5 Single channel transistors' width and length value.

Figure 4.6 is the symbol of the single channel differential switch, Figure 4.7 uses this symbol as the sub-block to build an 8 to 1 analog MUX. The pin descriptions of this symbol are shown in Table 6.

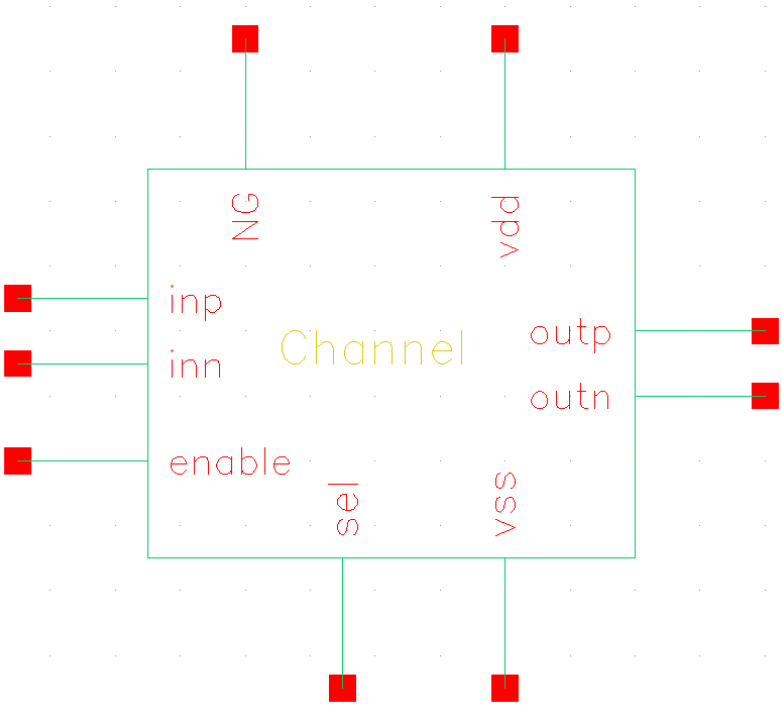

Figure 4. 6 One channel symbol of the 8 to 1 analog MUX

Pin Name	Pin Type	Pin Description
inp	Input	Differential input p
inn	Input	Differential input n
outp	Output	Differential output p
outn	Output	Differential output n
enable	Pin	Enable Pin
NG	Pin	Non-enable Pin
sel	Pin	Select Signal Pin
vdd	Pin	Supply Power Pin 1.2V
vss	Pin	Supply Ground Pin

Table 6 Channel pin description

4.2.3 Eight-Channel MUX Design

Figure 4.7 is the block structure of the 8 to 1 analog MUX, the triangular symbol is the enable component of whole analog MUX circuit, the differential inputs inp1 and inn1 to inp8 and inn8 of the 8 channels can be connected to 8 pairs of input electrodes, the 8-channel differential outputs are connected in a parallel structure and defined as outp and outn, which are connected to the differential inputs of the following differential bio-signal amplifier.

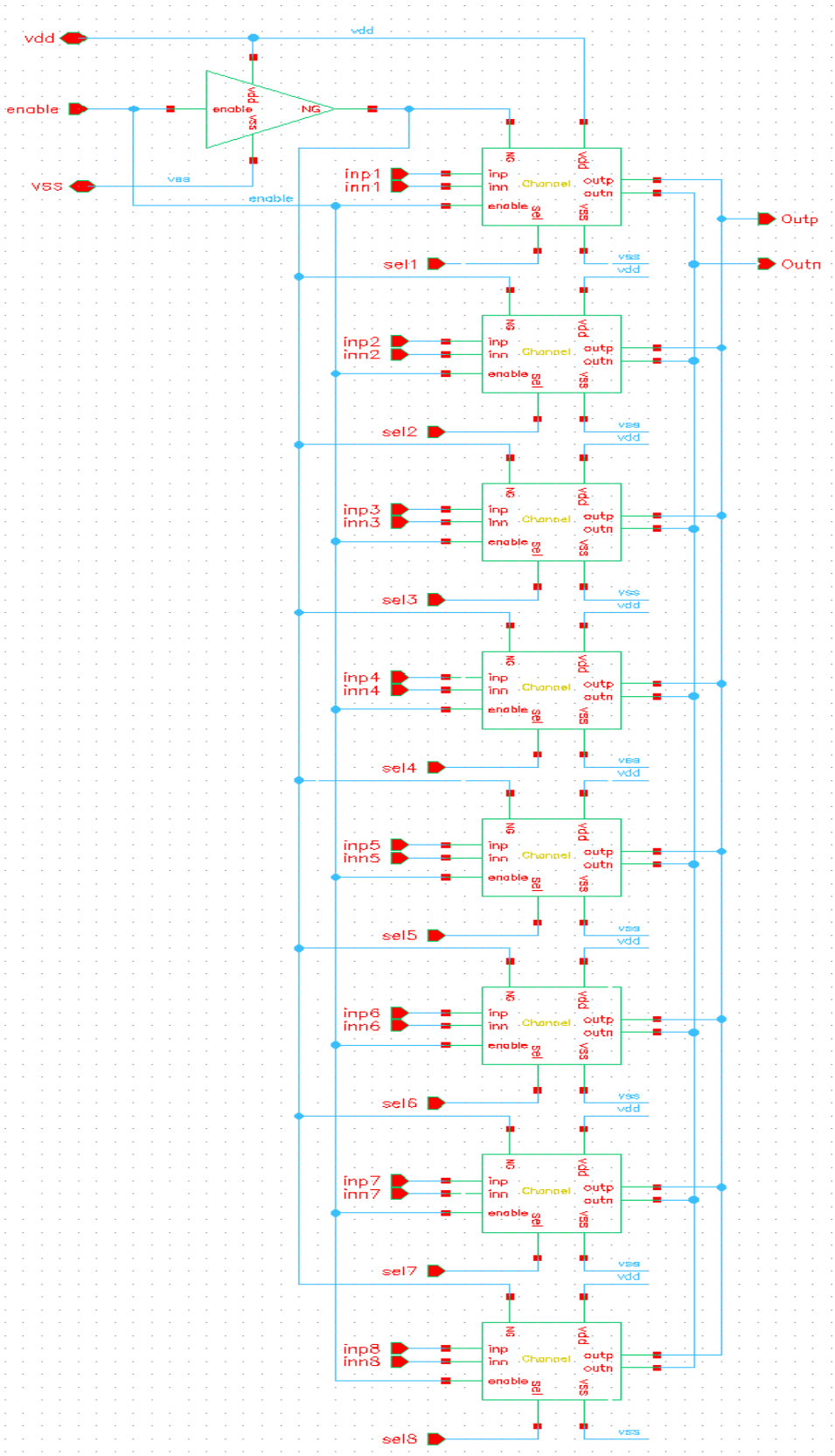

Figure 4. 7 Block structure of 8 to 1 analog MUX

Figure 4.8 is the 8 to 1 analog MUX symbol; its pin descriptions are shown in Table 7.

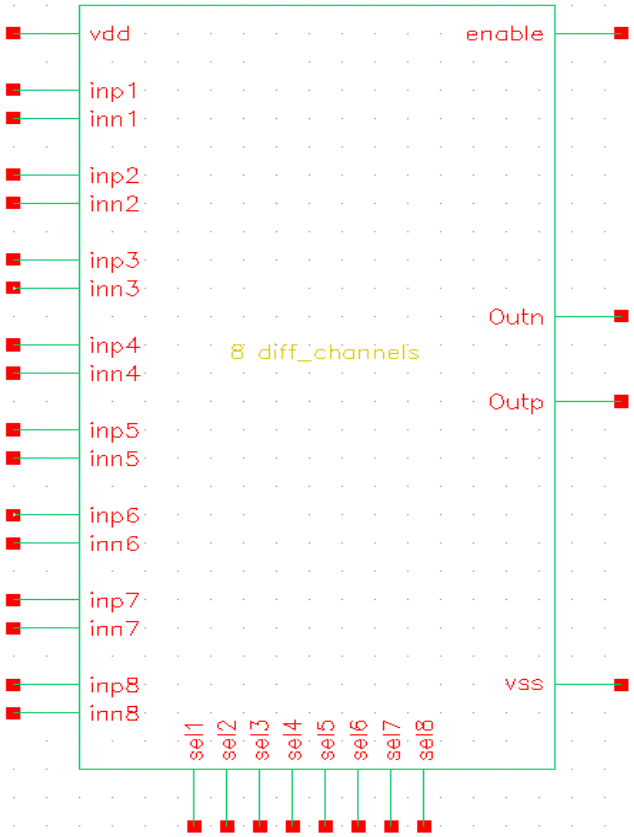

Figure 4. 8 Shows the symbol of 8 to 1 analog MUX, it includes 8 pairs of differential inputs and 2 differential outputs.

Pin Name	Pin Type	Pin Description
inp1 to inp8	Input	Channel 1 to Channel 8 differential input p
inn1 to inn8	Input	Channel 1 to Channel 8 differential input n
outp	Output	MUX differential output p
outn	Output	MUX differential output n
enable	Pin	Enable Pin
sel1 to sel8	Pin	Channel 1 to Channel 8 Select Signal Pins
vdd	Pin	Supply Power Pin 1.2V
vss	Pin	Supply Ground Pin

Table 7: 8 to 1 analog MUX pin description

In the design, the select signals (sel1~sel8) of this 8 to 1 analog MUX are generated from a 3 to 8 digital decoder. Figure 4.9 below shows the schematic of the digital decoder. Table 8 is the truth table of the decoder. The truth table shows how the decoder controls the MUX, For example, to select the signal from the 5^{th} channel, the decoder inputs should be 100. Then a "0" or a low potential voltage signal is sent to the port sel5 of the MUX, and other select ports of the MUX will receive logic "1" or a high potential voltage signals, which means except channel 5, the other channels will not be selected.

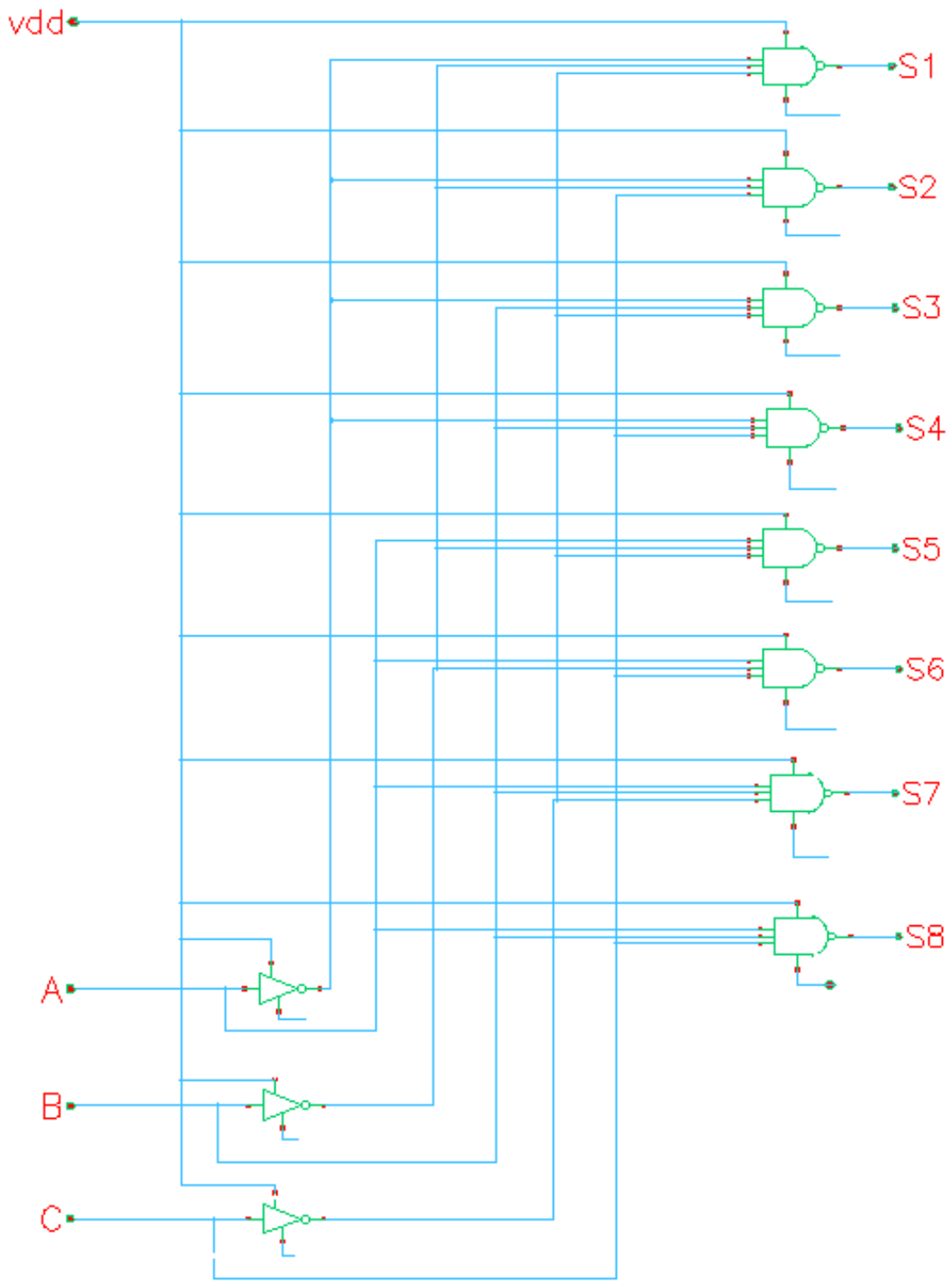

Figure 4. 9 The schematic of a 3-8 decoder, with different A, B, C logic combination, only one output terminal among S1~S8 is set to "0" which can turn on one channel of the MUX.

Channel #	1	2	3	4	5	6	7	8
Coding Combination	000	001	010	011	100	101	110	111
A	0	0	0	0	1	1	1	1
B	0	0	1	1	0	0	1	1
C	0	1	0	1	0	1	0	1
S1	0	1	1	1	1	1	1	1
S2	1	0	1	1	1	1	1	1
S3	1	1	0	1	1	1	1	1
S4	1	1	1	0	1	1	1	1
S5	1	1	1	1	0	1	1	1
S6	1	1	1	1	1	0	1	1
S7	1	1	1	1	1	1	0	1
S8	1	1	1	1	1	1	1	0

Table 8 Decoder Truth Table

Figure 4.10 shows the schematic of one NAND gate in the decoder, which is a complementary structure NAND gate. To optimize the circuit in terms of power, delay, and layout area, an aspect ratio $\mu_n/\mu_p = \mu_r$ (the mobility ratio) is introduced. Simply imagine that the pull up network (T4, T5, T6) of the NAND gate as one PFET (Tp), the pull down network (T0, T1,T2) of the NAND gate as one NFET (Tn), the PFET and the NFET form an "inverter". In order to get the same pull up and pull down drive strength, and the equal rise and fall time, size the "inverter" as $W_p/W_n = \mu_r$ (when the lengths of NFET and PFET are the same). In this design, the mobility ratio is approximately equal to 5, assuming that the width of Tn is 300nm, then the width of Tp is 1.5um. For the NAND gate structure, since the PMOS transistors (T4, T5, T6) are in parallel, thus for each transistor, $W_p = 1.5\mu m$, and because the NMOS transistors (T0, T1, T2) are

connected in series, $W_n = 900nm$. The detailed transistor sizes are shown in Figure 4.10.

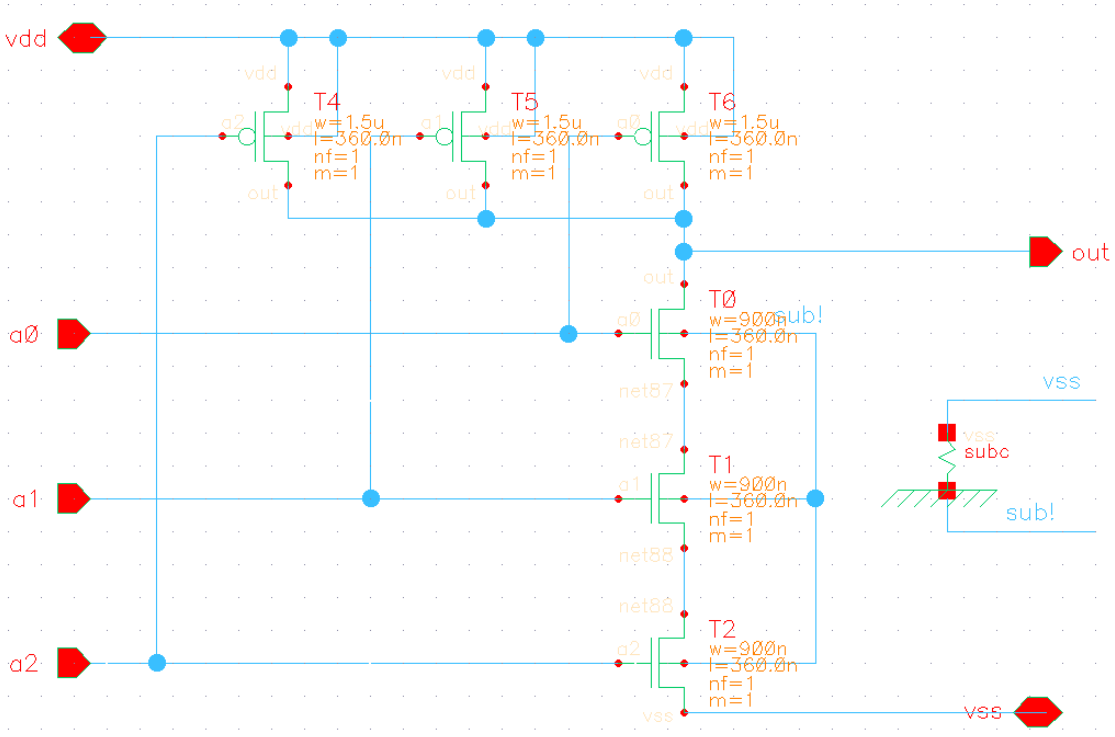

Figure 4. 10 NAND gate schematic

4.2.4 MUX Simulation Waveforms

The following two figures show the input and the output waveforms of the designed 8 to 1 analog MUX. Figure 4.11 shows the waveforms of the control signals (A, B, C), eight input signals and the output signal in 1.25 clock cycle. Figure 4.12 is the zoomed in waveforms of the control signals and differential output signals of the MUX. From these two figures, each combination of A, B, C code corresponding to one specific channel of the MUX, and the output signal follows the changes of the different on-channel input signal. By proper setting the control signals, the MUX can select any desired channel.

Table 9 shows the amplitudes and frequencies of all the input signals.

Input Signal	Frequency (Hz)	Amplitude (μV)	Phase (degree)
Inp1	10	100	0
Inn1	10	100	180
Inp2	20	80	0
Inn2	20	80	180
Inp3	30	70	0
Inn3	30	70	180
Inp4	40	60	0
Inn4	40	60	180
Inp5	50	50	0
Inn5	50	50	180
Inp6	60	40	0
Inn6	60	40	180
Inp7	80	30	0
Inn7	80	30	180
Inp8	100	10	0
Inn8	100	10	180

Table 9 The frequency and amplitude parameters of eight differential input signals are presented, all the input signals are in the forms of sine wave, each negative input signal has a 180 degree phase shift.

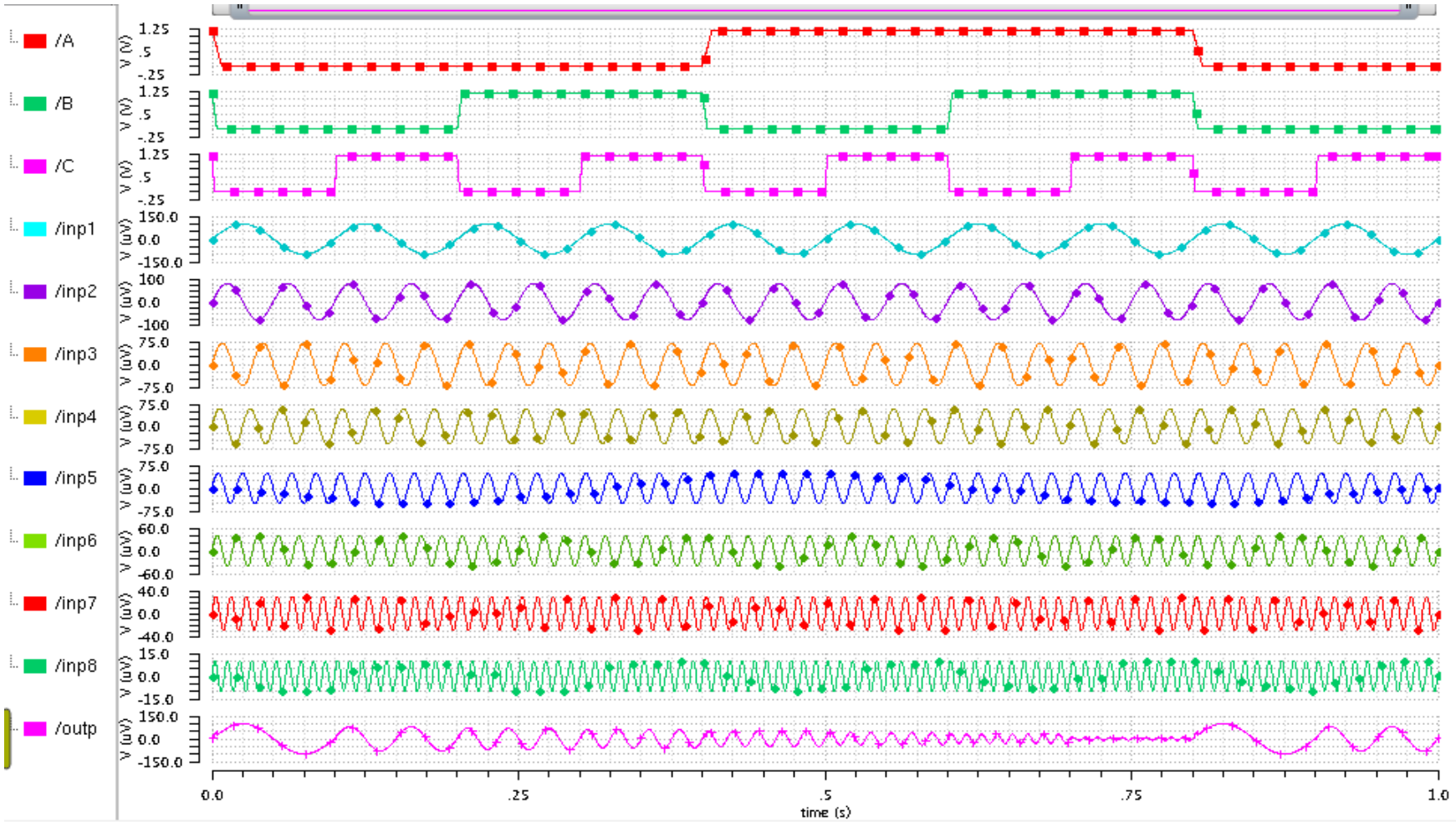

Figure 4. 11 Shows the input and output waveforms of the 8 to 1 analog MUX, the first three square waves are the decoder control signals A, B, C, and the sine waves inp1 to inp8 are the positive input signals in different amplitudes and frequencies, the outp is the positive output signals from the 8 to 1 analog MUX.

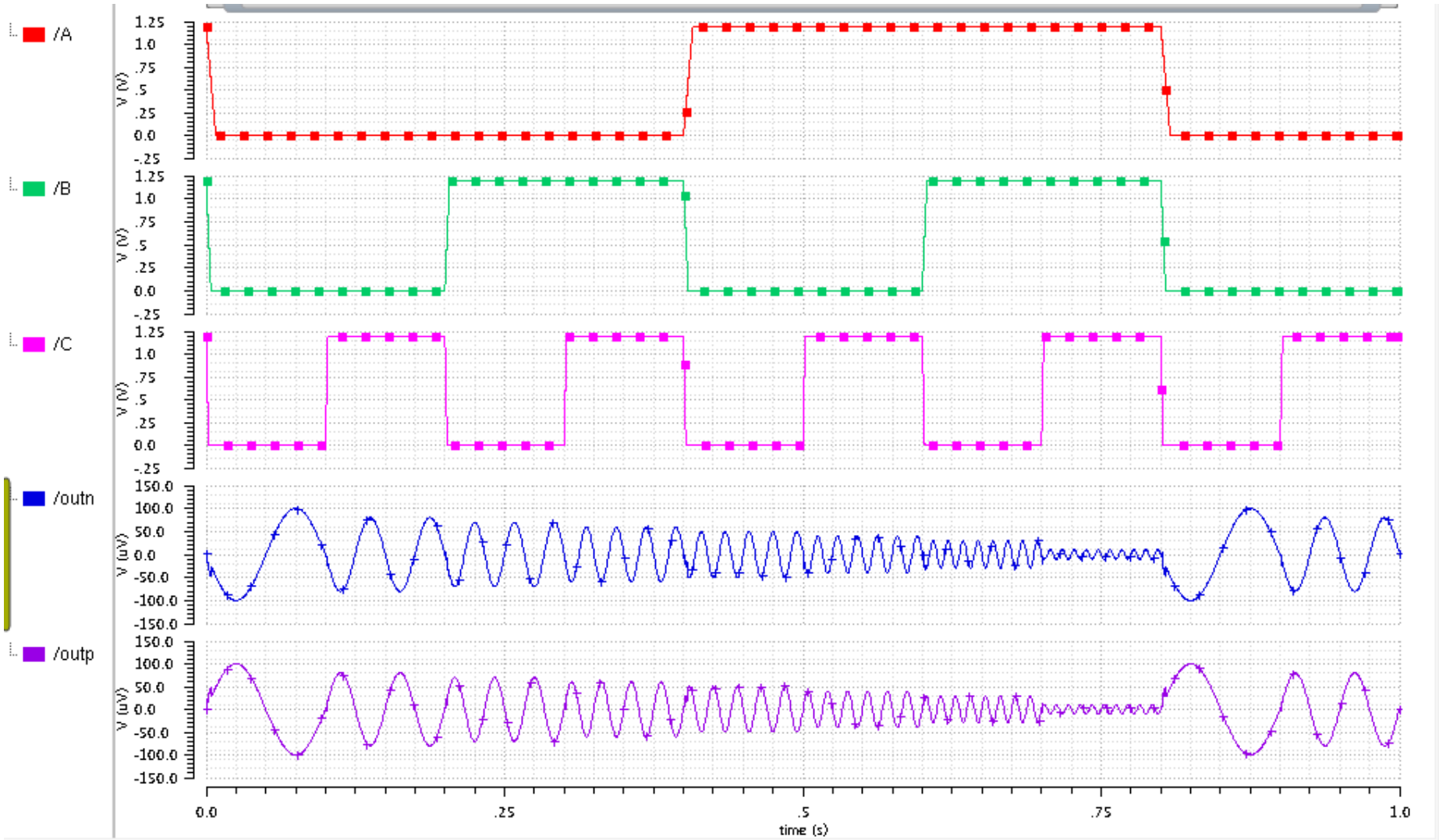

Figure 4. 12 Differential output waveforms of the 8 to 1 analog MUX.

Figure 4.12 shows the zoomed in differential output waveforms of the 8 to 1 analog MUX. From this figure, it can be observed that the glitch occurs in the output signal at the time of channel switching, this is because when control signals A, B, C switch from low to high or high to low level voltage, it causes the voltage level to be unstable in a period of time, thus leading to output errors. The existing period of glitches depends on the rise time and the fall time of the control signals, this period of time is quite short and will not affect the long-time signal.

Figure 4.13 shows the test-bench of the 8 to 1 analog MUX, which consists of a 3 to 8 decoder and eight differential MUX channels. All the differential input signals are generated by 8 pairs of sine wave voltage sources (Vsin), the amplitude range of the input signals is from 10uV to 100uV, and the frequencies range of the input signals is from 10Hz to 100Hz. The control signals A, B, C are produced by 3 square wave voltage sources (Vpulse). The detailed input settings see Table 8. The supply voltage (Vdd) is 1.2V,

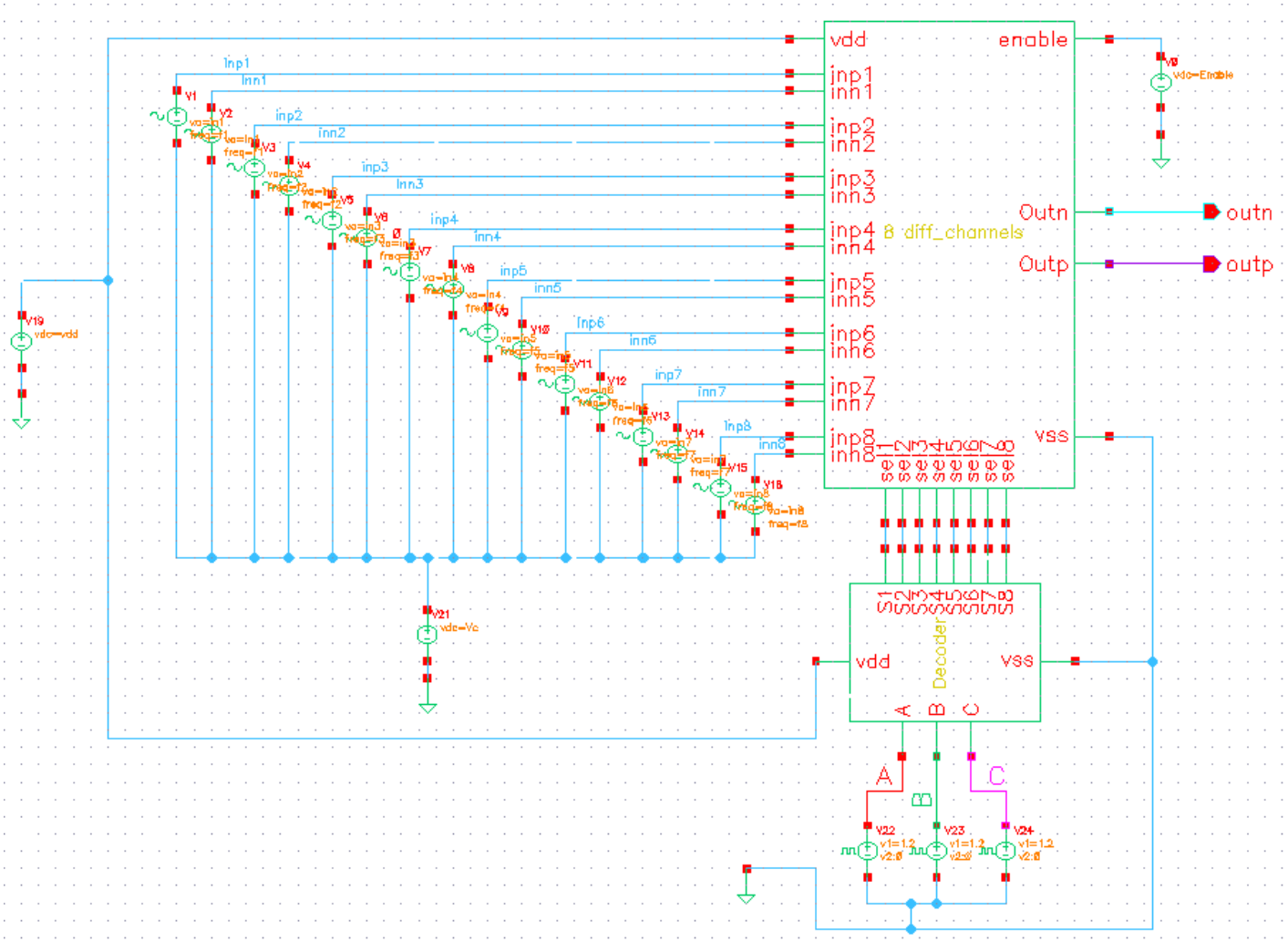

Figure 4. 13 Differential 8 to 1 analog MUX test-bench

4.2.5 Linearity of the MUX

The multiplexing signals are very low amplitude and low frequency bio-signals, in order to accurately transmit the signals, linearity of the MUX becomes very important. In this section, the THD is used to measure the linearity of the MUX.

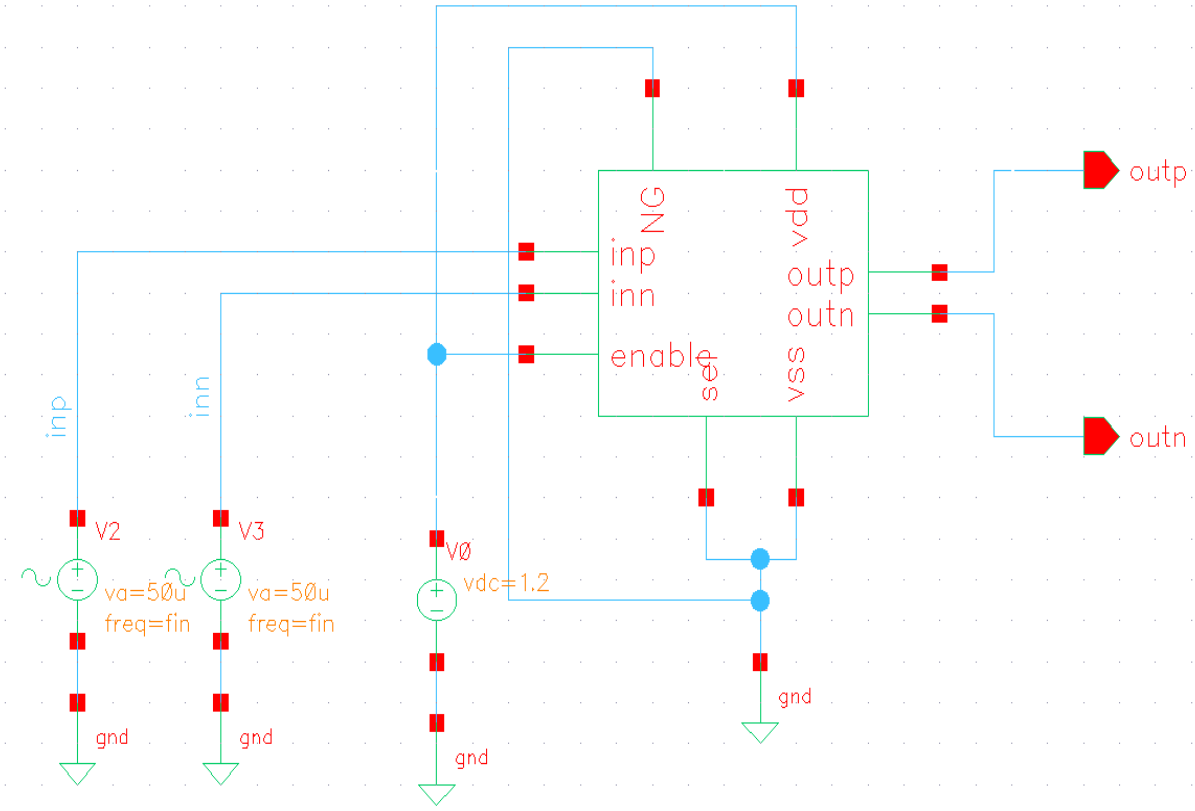

Figure 4. 14 Shows the THD test-bench of one channel of the MUX, the "sel" and "NG" is connected to ground to make the channel stay "ON".

The harmonic power spectrum of single channel of the MUX is presented in Figure 4.15. The amplitudes of the input signals are 50uV, and the frequencies are 10Hz. It can be observed that the dominant harmonic starts to appear at 190Hz and 210Hz which are the 19^{th} harmonic, and the 21^{st} harmonic. As the noise floor of the MUX is about 170dB, the power of harmonics that under the noise floor will not be taken into account. In this

harmonic power spectrum, at around 1.3KHz, the harmonic component is equal to the noise floor 170dB. Thus, the total harmonic distortion can be calculated within this frequency range. By using equation (3.8) and equation (3.9), the THD is -86.05dB, and the THD in forms of percentage is 0.00498%.

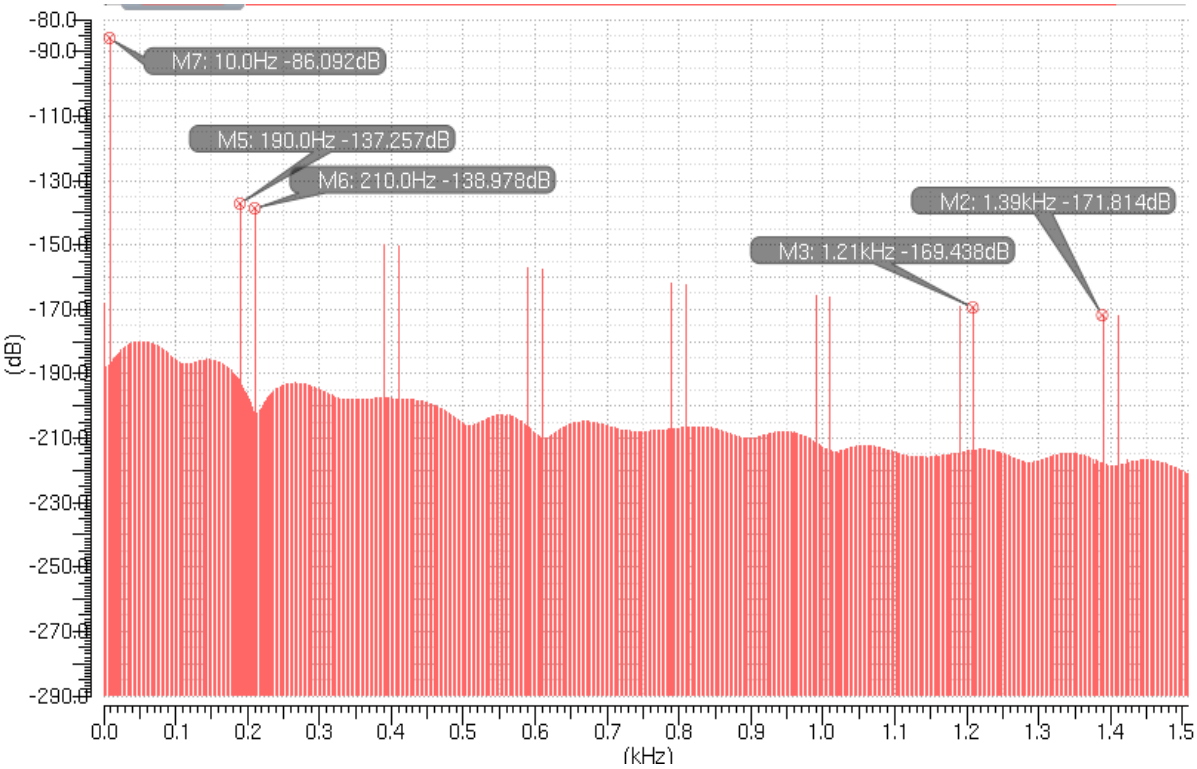

Figure 4. 15 Shows the harmonic power spectrum of the MUX (Input frequency fin=10Hz), 32768 points has been sampled.

The single channel gain of the MUX is presented in Figure 4.16 and Figure 4.17, the gain is close to 1V/V under 1MHz, which is good for the signal transmission in the MUX.

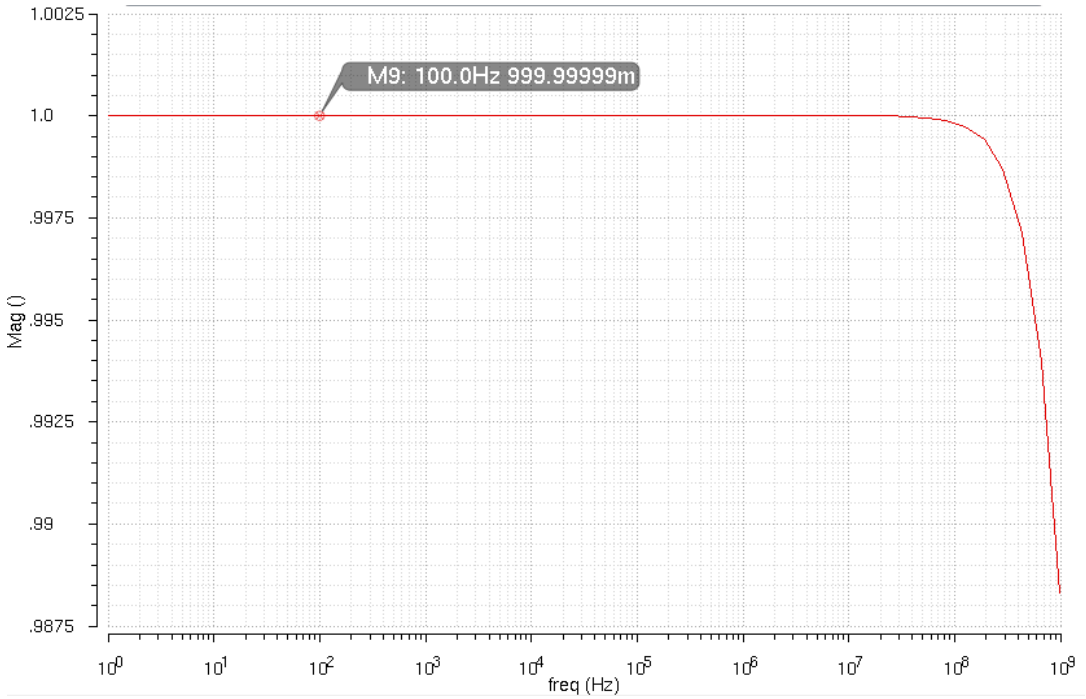

Figure 4. 16 The gain of single channel of the MUX in terms of V/V.

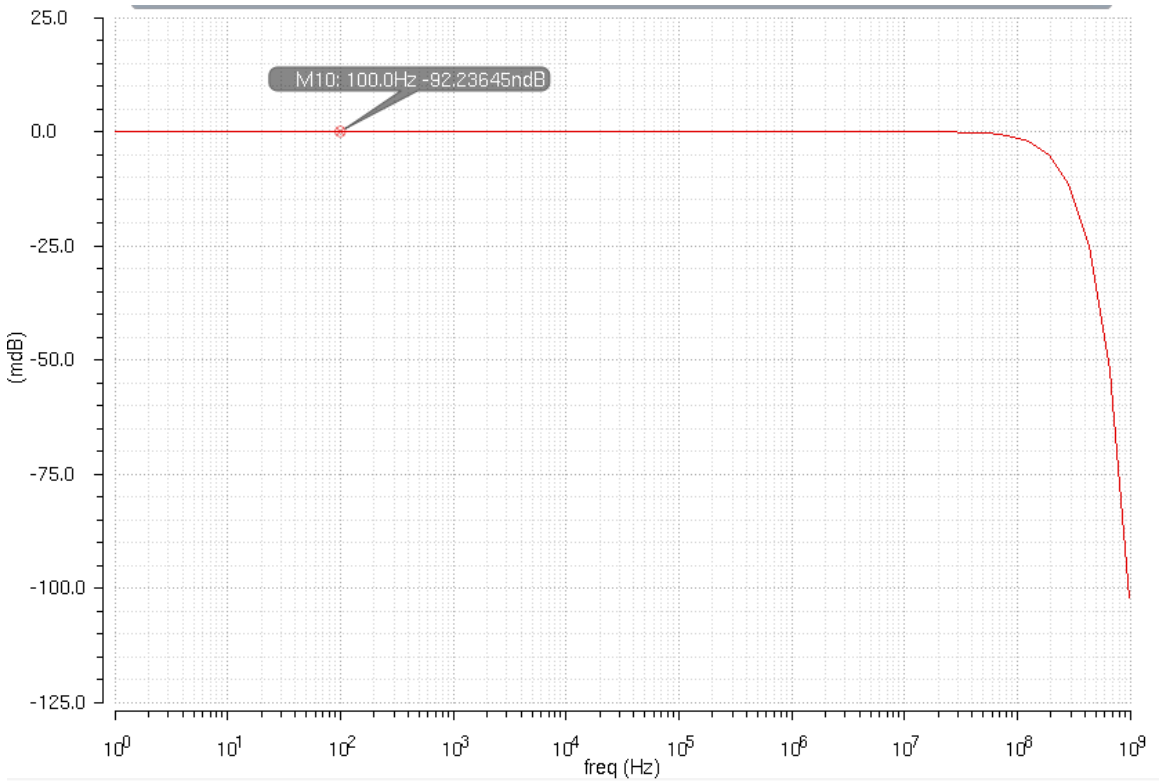

Figure 4. 17 The gain of single channel of the MUX in terms of dB.

To measure the power of the MUX, a large resistance load is connected to the MUX output. In cadence, run a transient analysis for several cycles and measure the average current drawn from the supply voltage. In this way, the total power of the MUX can be achieved which is shown in below table.

Table 10 is the comparison table between this designed analog MUX and others.

Ref	**Technology**	**Channel Number**	**Power**	**Layout size**	**Supply voltage**	**Ron**	**THD**
[32]	0.35um	1	-	-	3.3V	-	-46.389dB
[33]	45nm	8	7.8nW~98nW @0.1Hz~10K Hz	-	0.65V	10 Ω	-
[34]	180nm	8	0.79uW@10K Hz	-	400mV	27 Ω	-
[35]	180nm	8	1.08Mw@1G Hz	9000um^2	1.8V	-	-
[36]	0.35um	16	4.48Mw@5M Hz	14880 um^2	±1.65V	-	-
This work	130nm	8	807nW@10Hz	7163um^2	1.2V	73 Ω	-86.05dB

Table 10: Comparison table of the analog MUX

4.3 Implementation of Bio-signal Amplifier

4.3.1 Three Stage Bio-signal Amplifier

In this section, a three stage bio-signal amplifier topology [7] is introduced, which is used to connect to the differential outputs of the 8 to 1 analog MUX to reduce the common mode interferences and amplify the received low amplitude output signals. Figure 4.18 shows the schematic of a three stage bio-signal amplifier.

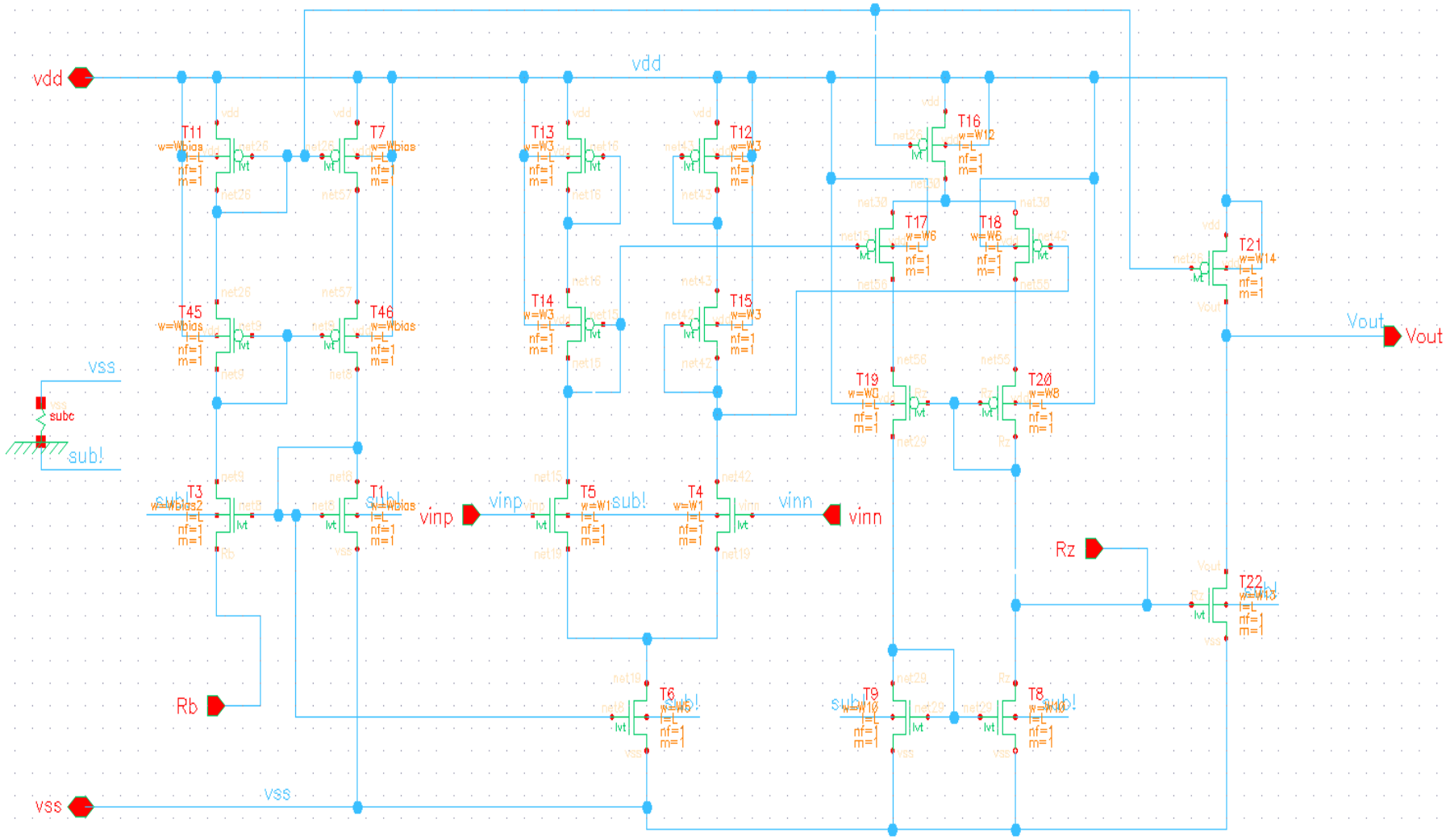

Figure 4. 18 Schematic of three stage bio-signal amplifier [7].

The amplifier symbol and its pin description are shown in the Figure 4.19 and Table 11, respectively.

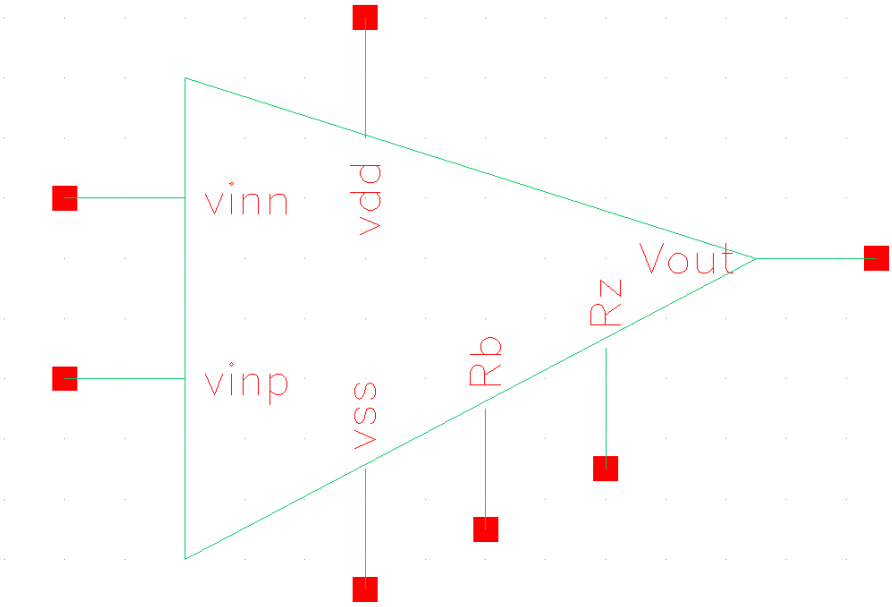

Figure 4. 19 Symbol of three stage bio-signal amplifier

Pin Name	Pin Type	Pin Description
vinn	Input	Input Pin vinn of Op-Amp
vinp	Input	Input Pin vinp of Op-Amp
Vout	Output	Amplifier Output Pin
Rb	Pin	Pin connect to biasing circuit resistor
Rz	Pin	Pin connect to compensation resistor and capacitor
vdd	Pin	Supply Power Pin 1.2V
vss	Pin	Supply Ground Pin

Table 11 Three stage bio-amplifier pin description.

4.3.2 Input Signal Setting & Output Waveform

Figure 4.20 is the bio-signal amplifier test bench, the input setting can be found in Table 12.

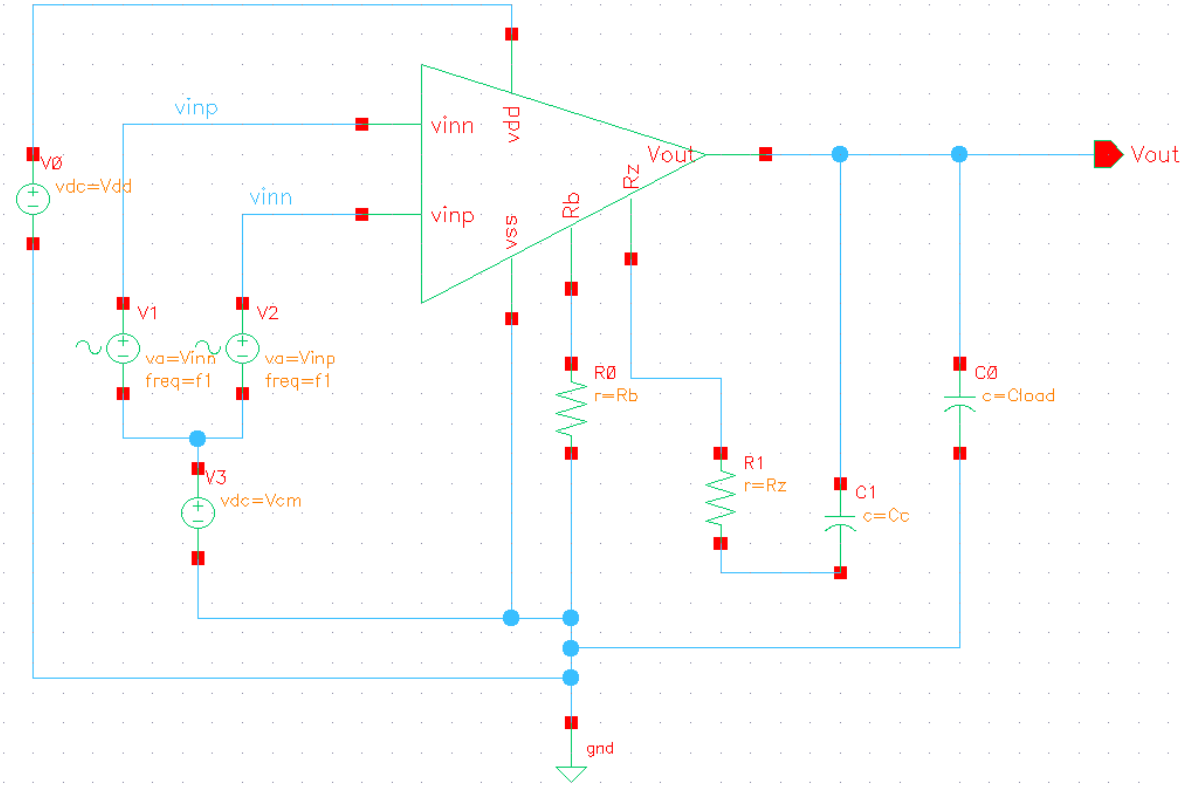

Figure 4. 20 Bio-signal amplifier test circuit

	Magnitude	Frequency	Phase
Vinp	50u	60Hz	0
Vinn	50u	60Hz	180
Vcm	600m	null	null
Vdd	1.2v	null	null

Table 12 Amplifier input setting

4.3.3 Simulation Results of the Bio-signal Amplifier

Differential Gain:

Figure 4.21 and Figure 4.22 are the differential gain of the amplifier in terms of V/V and dB, respectively. The gain is 2.14kV/V or 66.63dB at 100Hz. It can been seen from Figure 4.21, the input signal can be amplified about 2100 times. Since the frequency of the input signal is within 100Hz and its amplitude range is from 1uV to 100uV, thus just take a 50uV input signal as an example, it can be amplified up to about 100mV, which is large enough for observation.

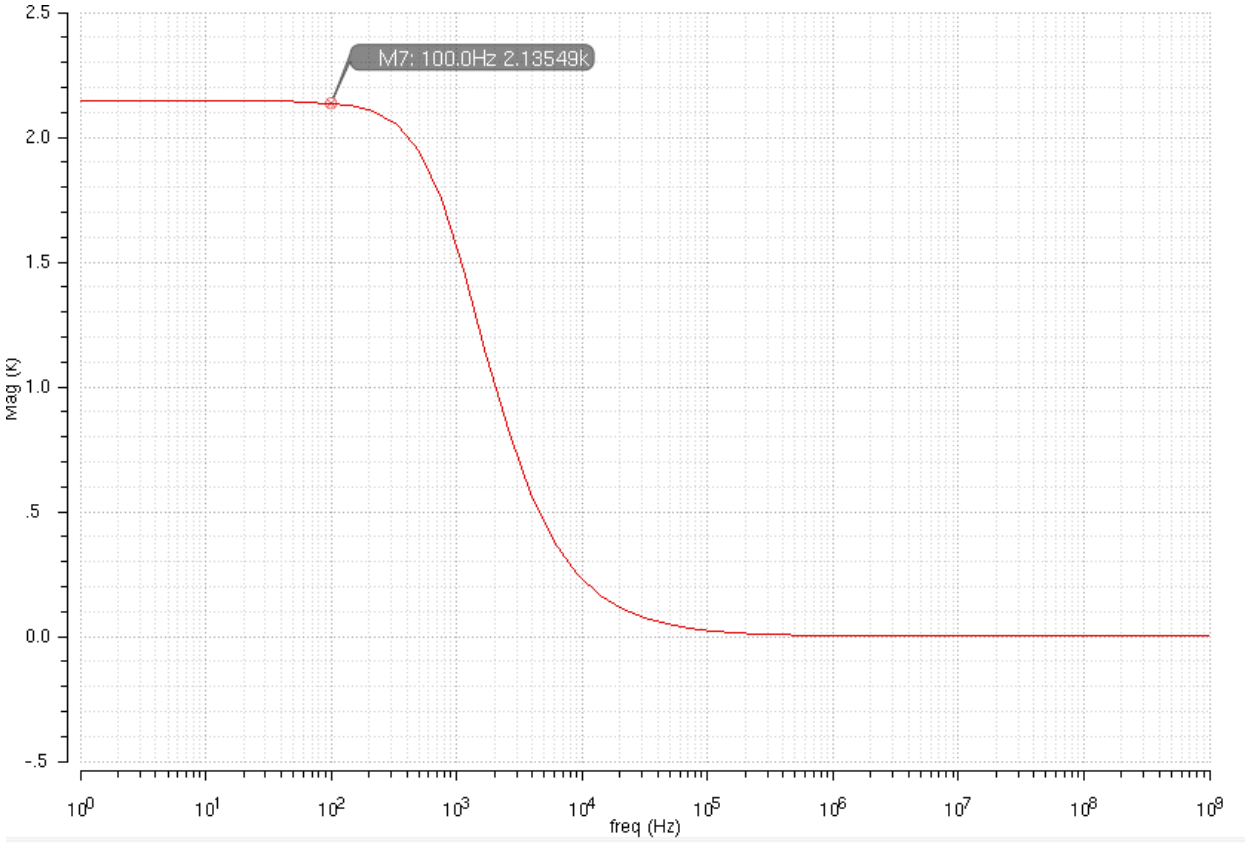

Figure 4. 21 Differential gain of the amplifier in terms of V/V.

The -3dB bandwidth of the amplifier can be found in Figure 4.22, which is about 1.08kHz. The differential gain of the amplifier (A_{diff}) is quite stable within 100Hz, which is around 66.6dB.

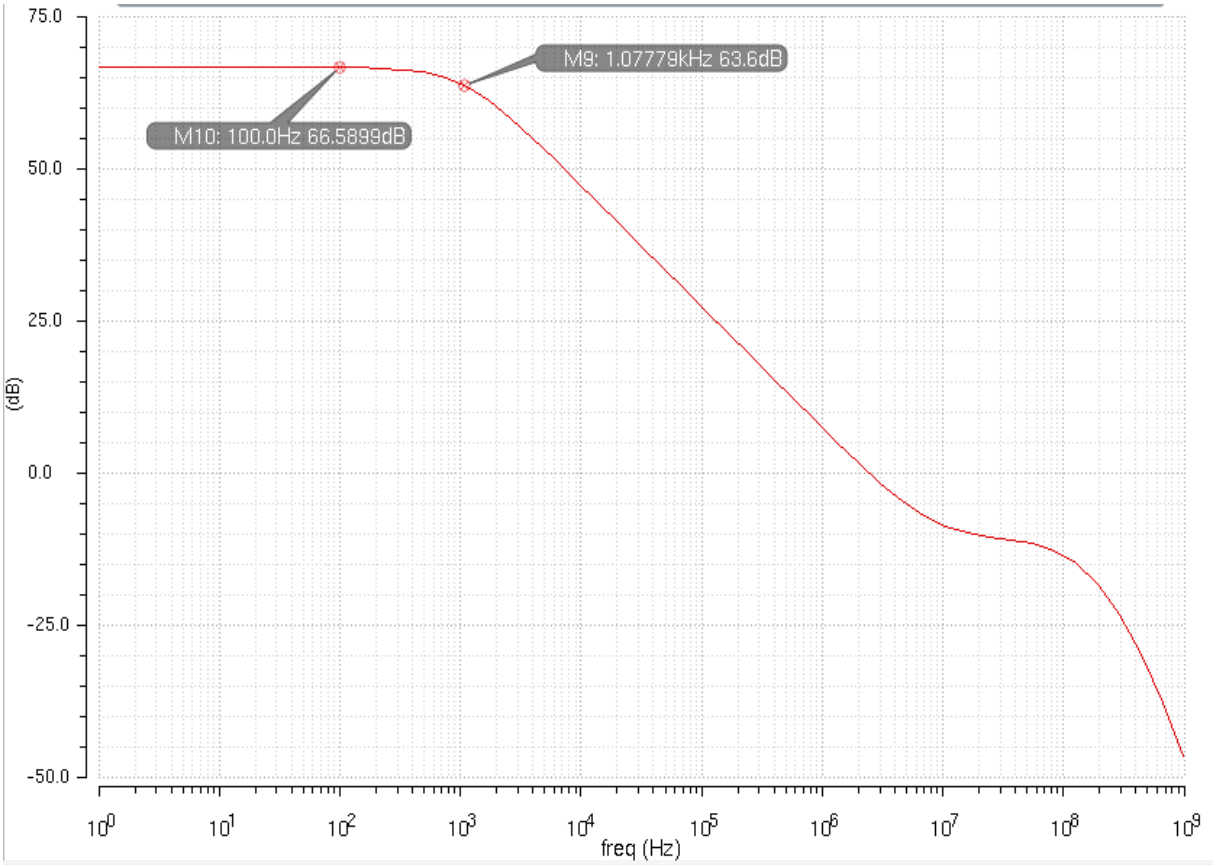

Figure 4. 22 Differential gain of the amplifier in terms of dB.

Common Mode Gain:

Figure 4.23 shows the common mode gain of the amplifier in terms of dB. The common mode DC voltage is set to 600mV for a 50uV input signal. From the figure, it can be seen that the common mode gain (A_{cm}) is very small, which is -39.3dB at 100Hz.

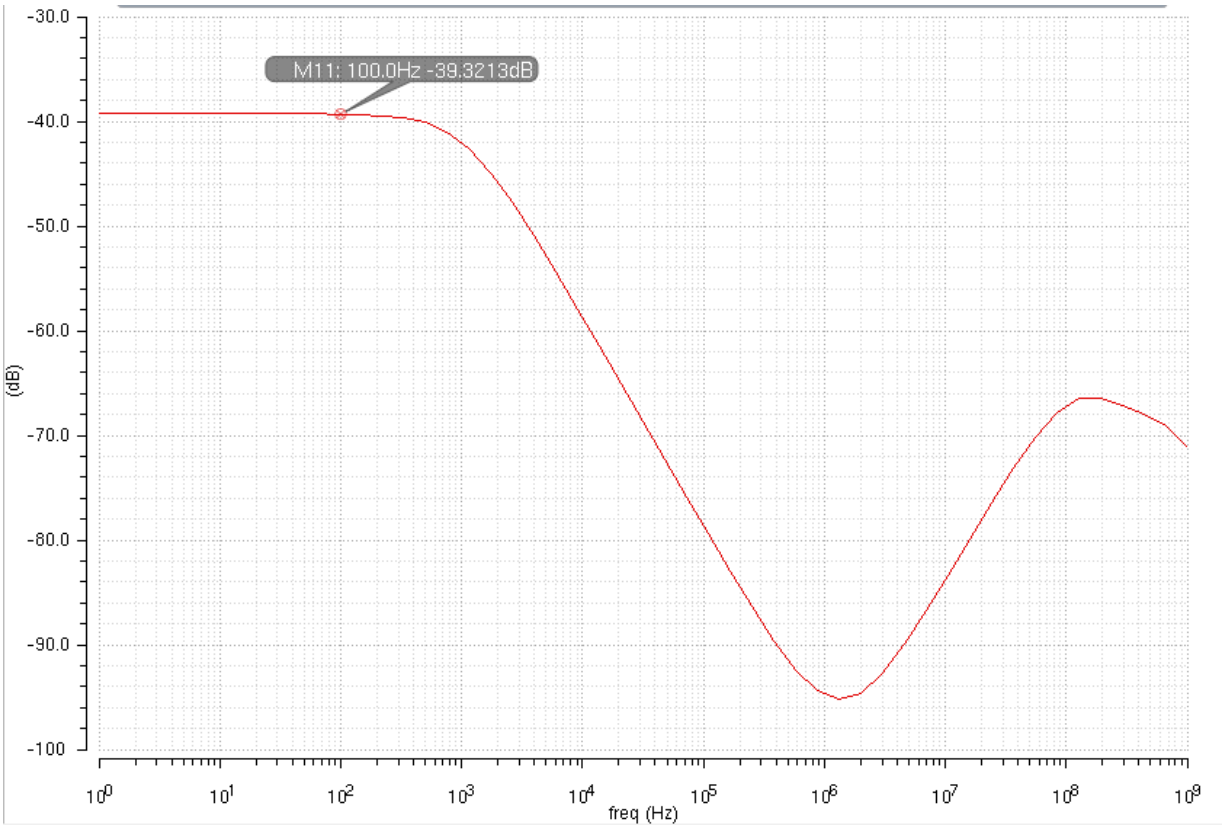

Figure 4. 23 Common Mode Gain of the amplifier in terms of dB.

CMRR:

According to the differential gain and common mode gain, CMRR can be easily calculated by using equation (4.3) or equation (4.4).

$$\text{CMRR} = \frac{A_{diff}\left(\frac{V}{V}\right)}{A_{cm}\left(\frac{V}{V}\right)} \tag{4.3}$$

$$CMRR = A_{diff}(dB) - A_{cm}(dB) \tag{4.4}$$

Figure 4.24 is the CMRR curve of the amplifier, which is around 106 dB at 100Hz.

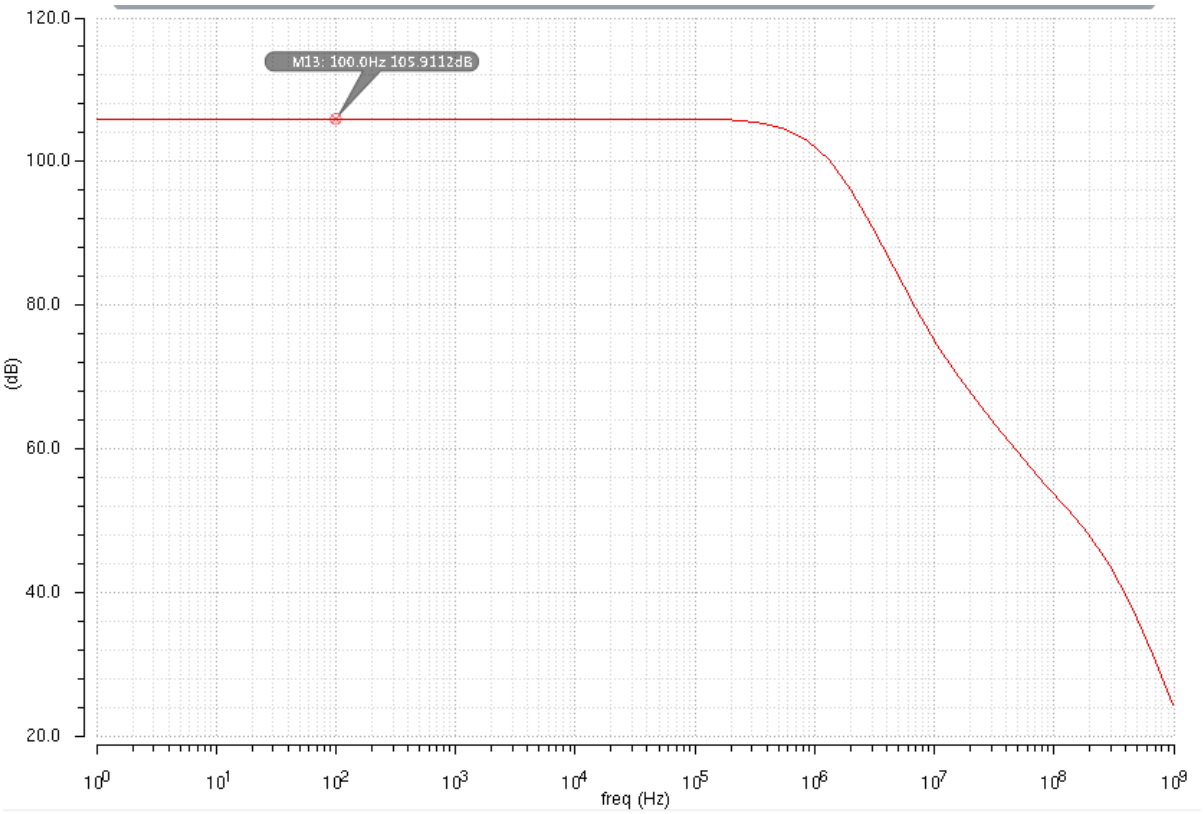

Figure 4. 24 CMRR of the amplifier

Phase Margin:

At the frequency which the amplifier gain is zero dB, the phase is -108.5 degree, see Figure 4.25. Thus, the phase margin can be calculated, which is approximately 71.5 degree.

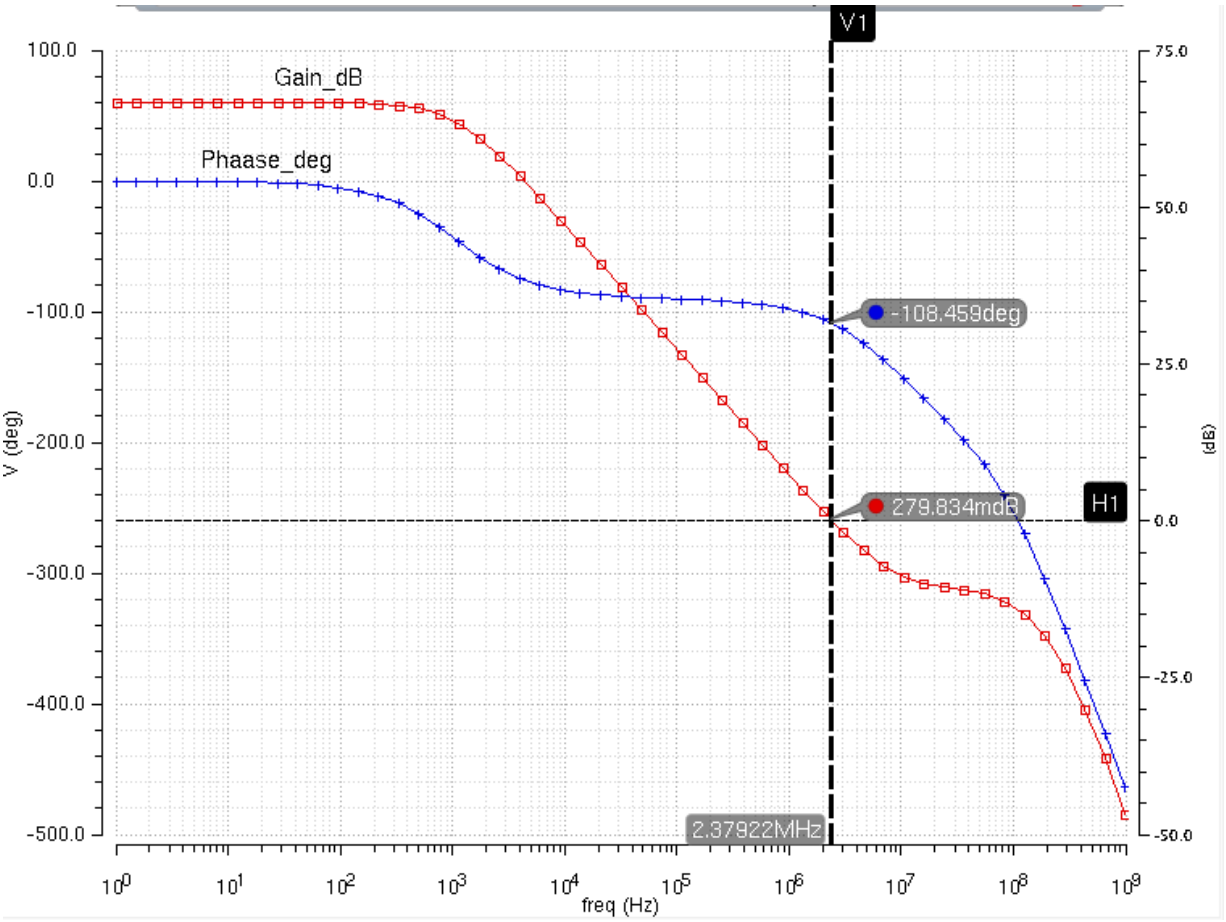

Figure 4. 25 The differential gain and phase of the Amplifier.

4.4 Summary

Table 13 is the summary of the design with clock frequency 10Hz.

Parameter	Values
Total Power Consumption	111.6uW
MUX Power Consumption	807nW
Amplifier Power Consumption	110.8uW
Total Layout Size	7163um^2
Voltage Supply	1.2V
Gain	66.6dB
CMRR	106 dB
Phase Margin	71.5°

Table 13 Summary table of design performance

Chapter 5

Monte Carlo Simulation and Layout Design

In order to reduce uncertain effects during the chip fabrication, the results of Monte Carlo simulation [37] can be used as a pre-test before chip tape-out. This chapter mainly discusses the Monte Carlo analysis and layout design strategy.

5.1 Monte Carlo Simulation

During the manufacturing of integrated circuits, small random variations will occur on designed devices and cannot be avoided. The unpredictable mismatch of devices or components affects the performance of the final products. Monte Carlo simulations are used to model the impact of random parameter variations in the manufacture's process [38]. In Cadence simulation, the Monte Carlo analysis is similar to the sweep analysis. The statistical distributions and correlations of the netlist parameters are specified, and then for each individual simulation, the Monte Carlo analysis will generate new pseudo-random values for the netlist parameters according to their specified distributions. From Monte Carlo simulation results, the performance of the device in the manufacturing can be predicted.

In this design, by running a MC simulation for the amplifier with 200 samplings without setting any correlation coefficients among the transistors, the results seem to be not satisfactory. The histogram of the power consumption shows the power has very wide range, from 25uW to 150uW, except some power samples in the expected power range, a lot of samples are in a low power range between 40uW and 60uW, which means some transistors might not work properly due to the mismatch problem, and for the differential gain and CMRR in this non-matching circuit, most samples cannot meet the specification of the design.

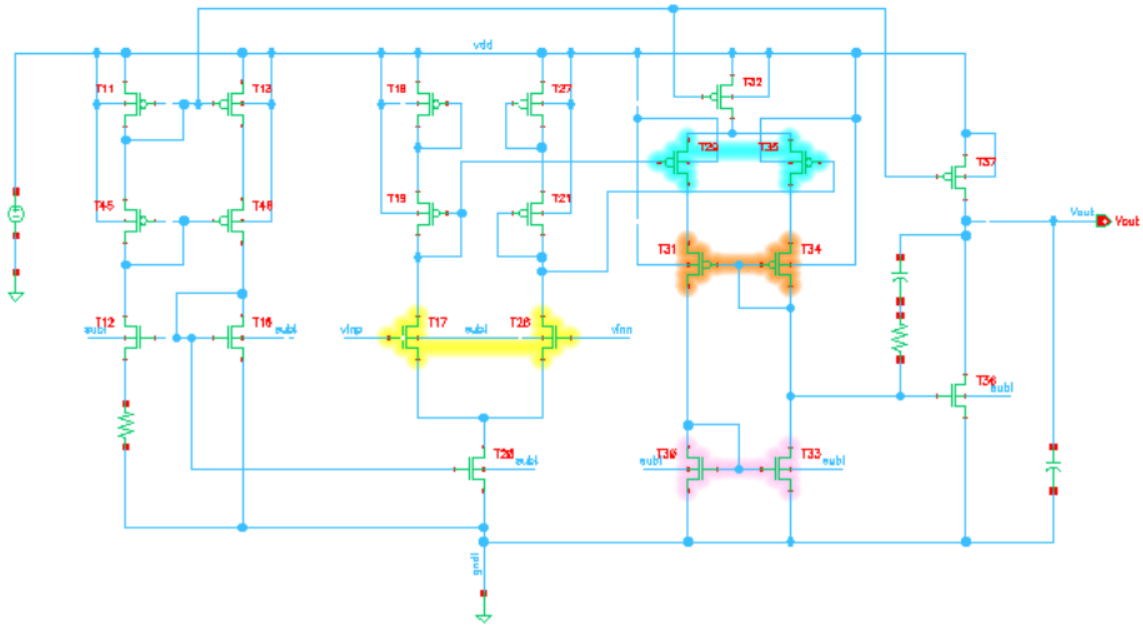

Figure 5. 1 Correlation constraints of the amplifier (for the correlated differential pair and current mirror, cc = 0.85).

As in VLSI circuit, matching the differential pairs and current mirrors can improve the performance of the circuit dramatically, at first set the constraint of the circuit as

shown in Figure 5.1, the correlation coefficient (cc) is 0.85 (the data is from design manual), sampling number is 200. The MC simulation results of the power, gain and CMRR of the amplifier are showing in Figure 5.2, Figure 5.3 and Figure 5.4, respectively.

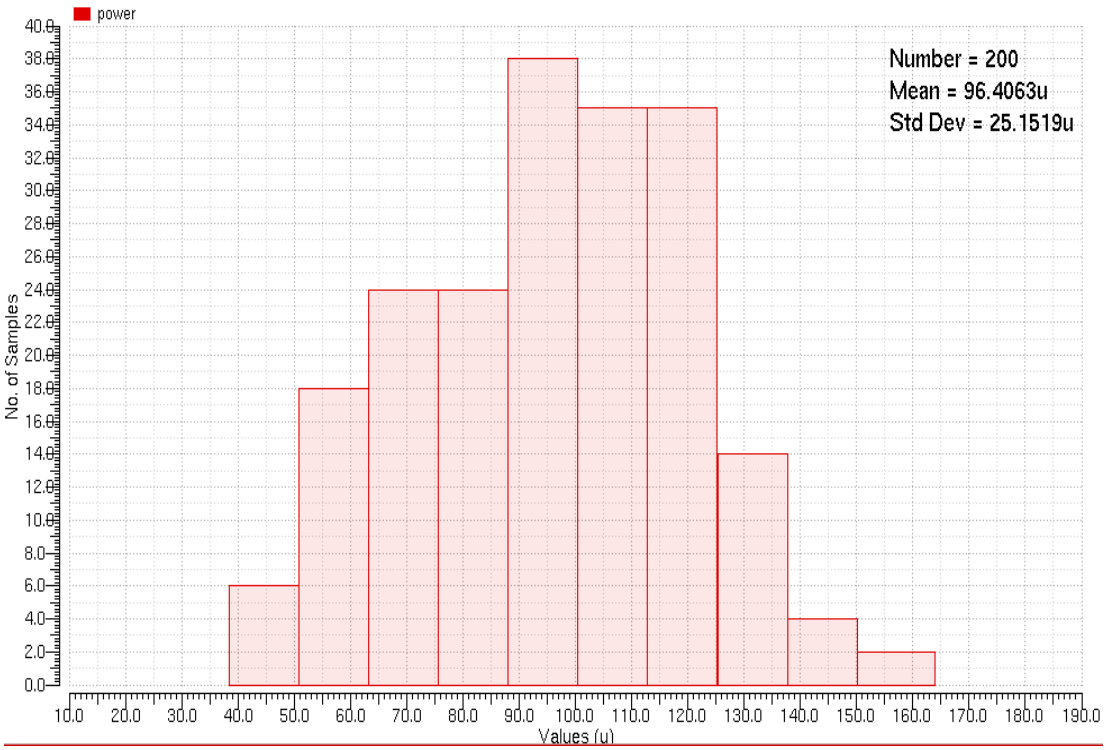

Figure 5. 2 Power histogram of the amplifier (cc = 0.85, N = 200)

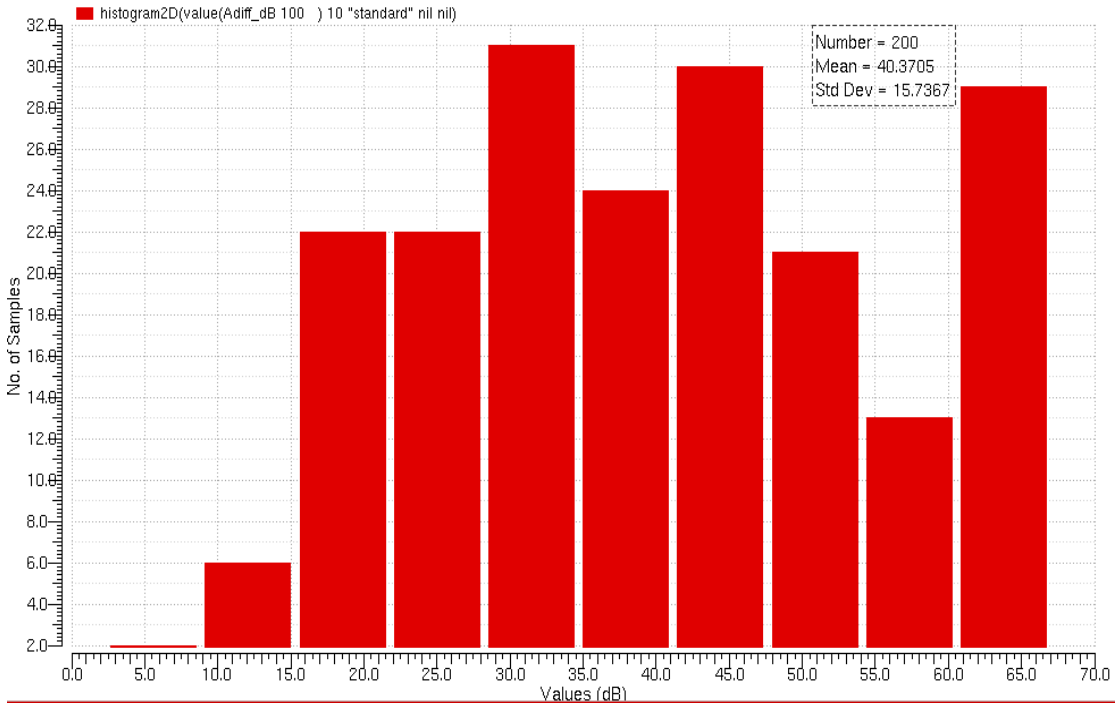

Figure 5. 3 Differential gain histogram of the amplifier at frequency = 100Hz (cc = 0.85, N = 200)

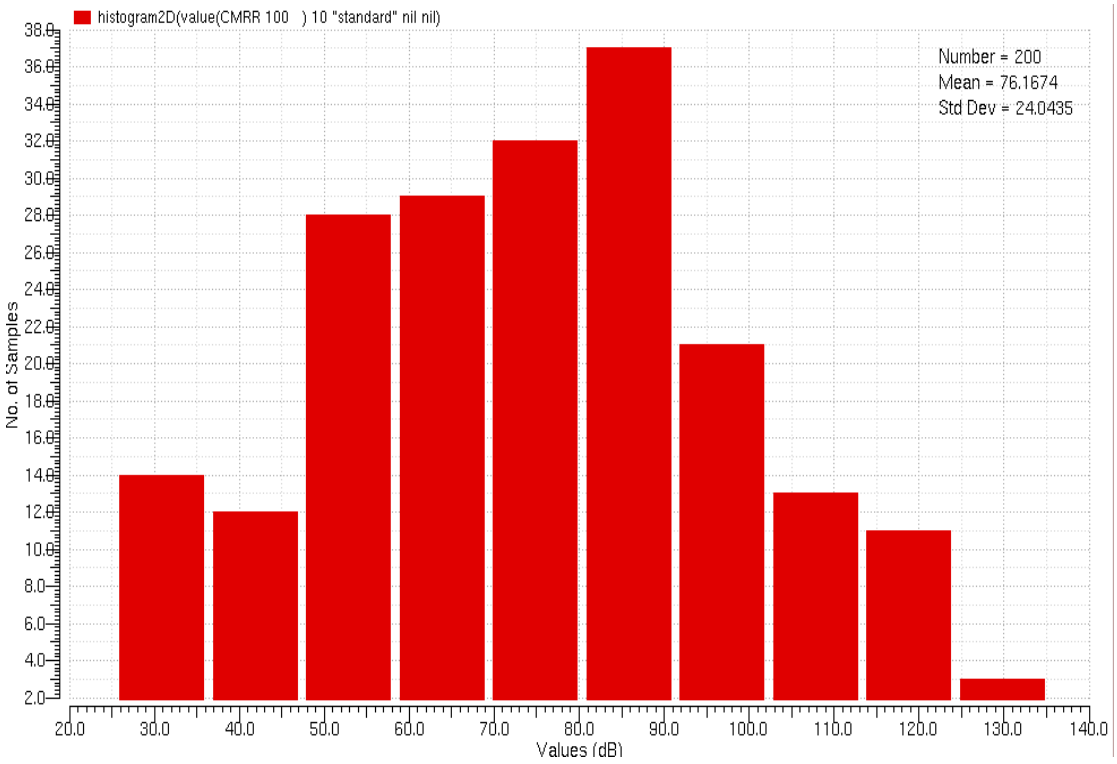

Figure 5. 4 CMRR histogram of the amplifier at frequency =100Hz (cc = 0.85, N = 200)

From above three figures, it can be found that many power samples start to concentrate around 100uW to 120uW, but there are still some sample points distributed around 70uW to 80uW, which means this MC simulation result of the power is not good enough. In the same way, it also can be found that most sample values of the differential gain and CMRR of the amplifier are lower than the previous simulation results (see section 4.3.3). As the voltage gain of first stage is proportional to the equivalent resistance of the load, which means matching these four active loads (set these active loads cc=0.85) can improve the circuit performance. In the Figure 5.5, Figure 5.6 and Figure 5.7, the MC results of the power, gain and CMRR of the amplifier all get much improved when matching the loads (T18 and T27, T19 and T21) in the first stage of the amplifier.

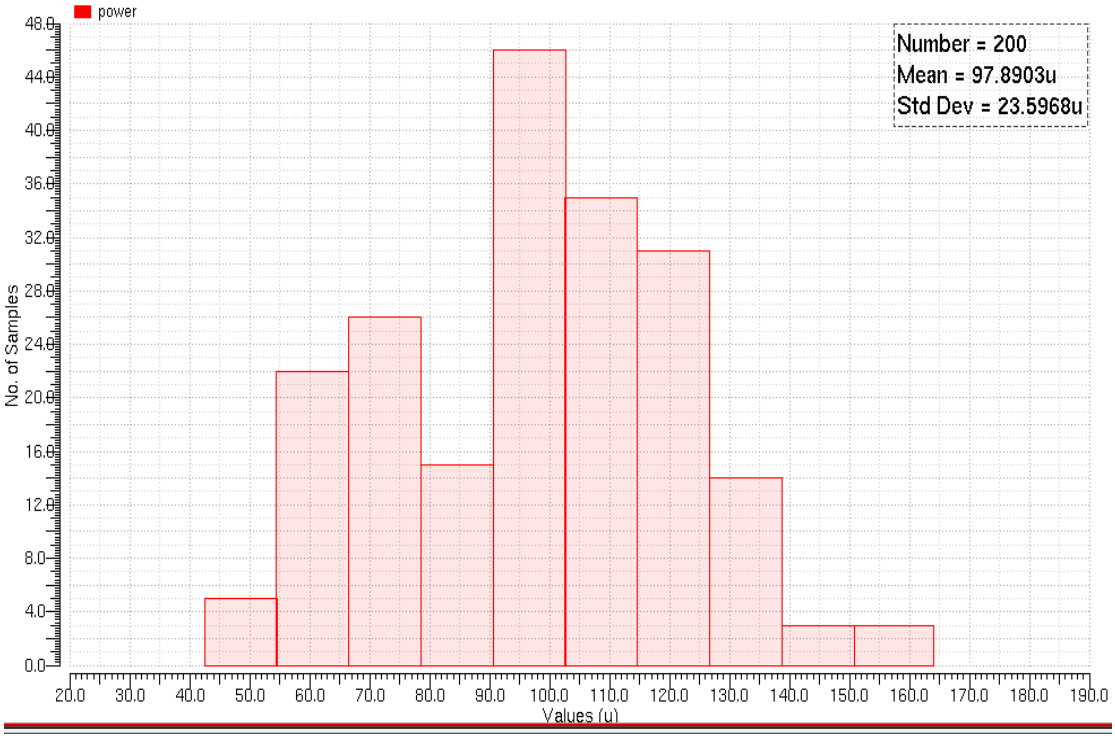

Figure 5. 5 Power histogram of the amplifier (cc = 0.85, N = 200, higher constraint)

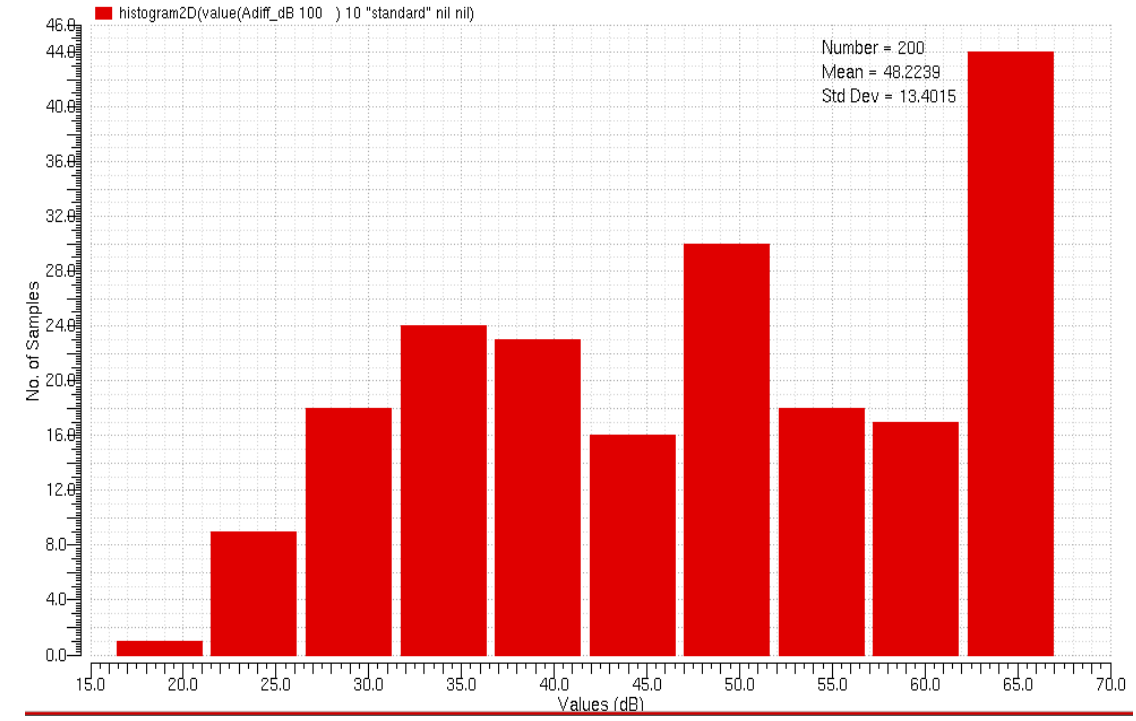

Figure 5. 6 Differential gain histogram of the amplifier at frequency = 100Hz (cc = 0.85, N = 200, higher constraint)

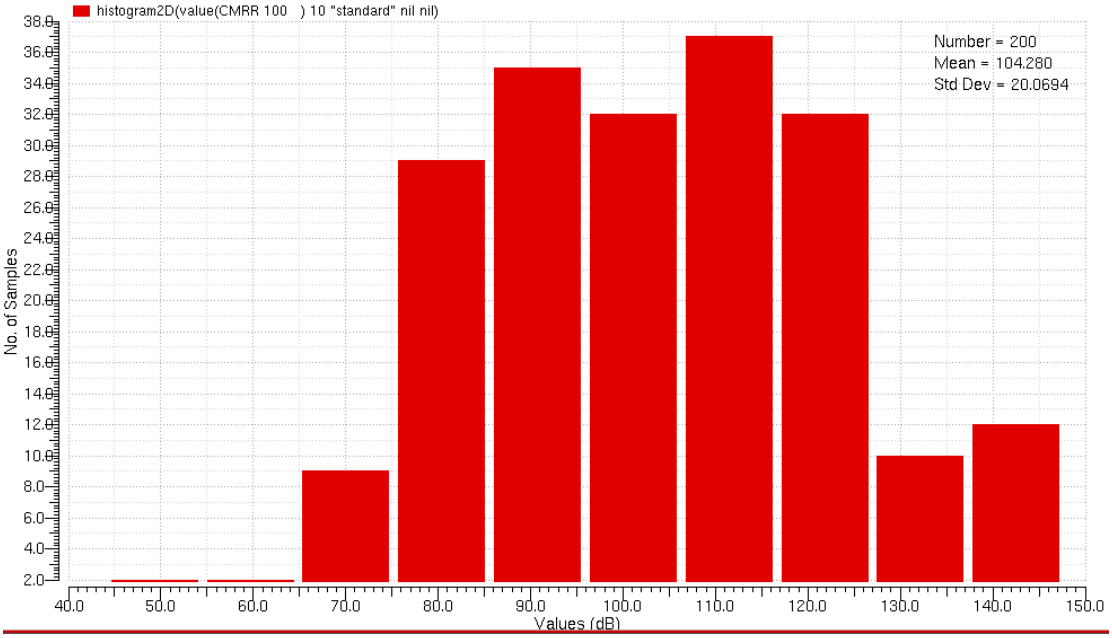

Figure 5. 7 CMRR histogram of the amplifier at frequency = 100Hz (cc = 0.85, N = 200, higher constraint)

In the layout design, matching is very important, some methods are used to enhance

the instance matching, such as common centroid technology. Suppose the correlation coefficient of the transistors can reach 0.95, and this time 500 number of points are sampled, the MC simulation results of the power, gain and CMRR of the amplifier become better. The more number of points with sampling, the more precise results will get, which means the more probability of the good results will be seen in the Monte Carlo simulation. As shown in Figure 5.8, Figure 5.9 and Figure 5.10, there are more samples points reach the expected values compared to the previous MC simulation results.

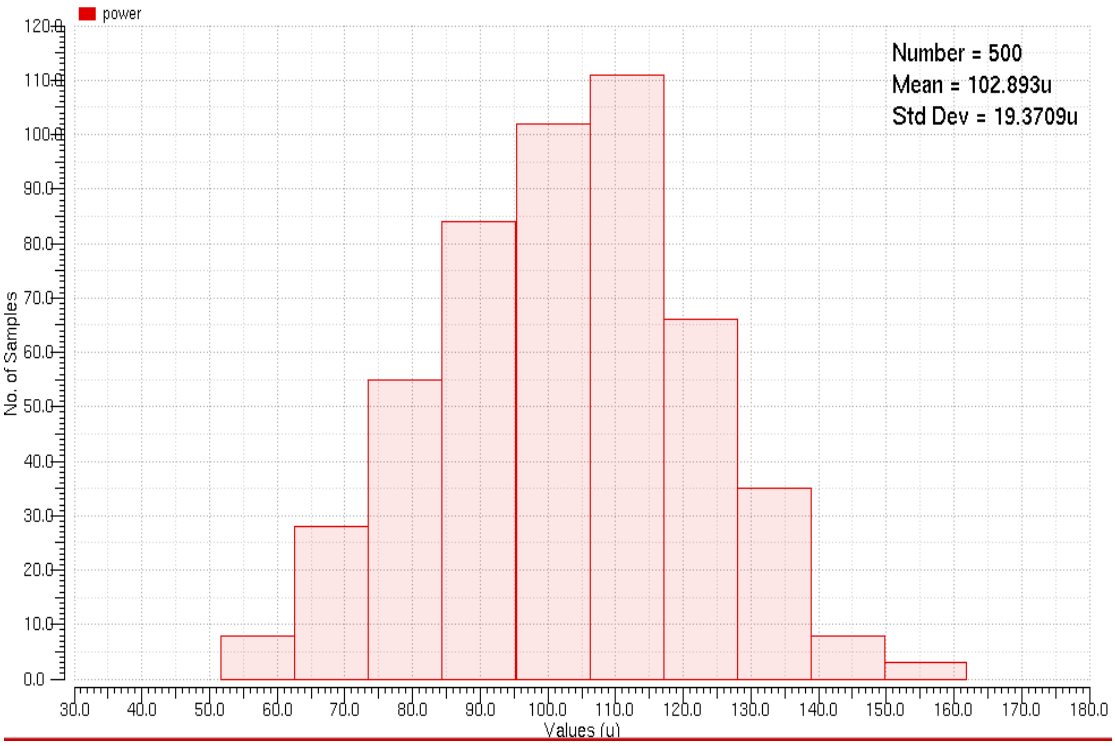

Figure 5. 8 Power histogram of the amplifier (cc = 0.95, N = 500, higher constraint)

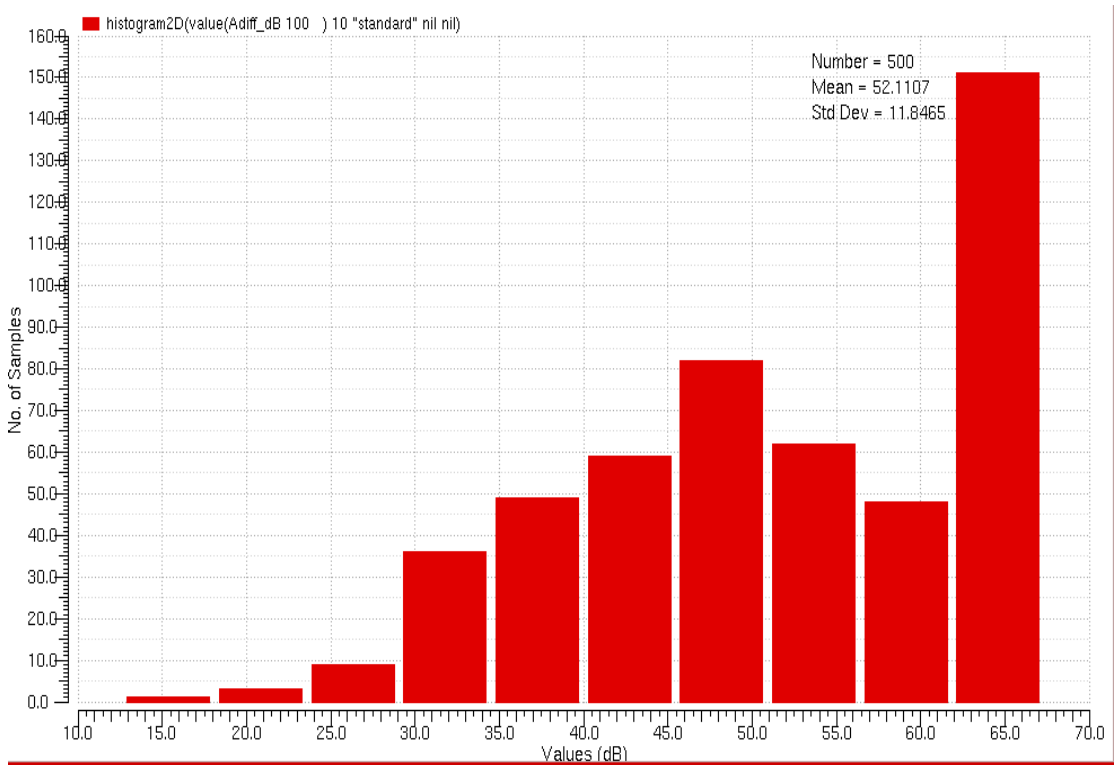

Figure 5. 9 Differential gain histogram of the amplifier at frequency = 100Hz (cc = 0.95, N = 500, higher constraint)

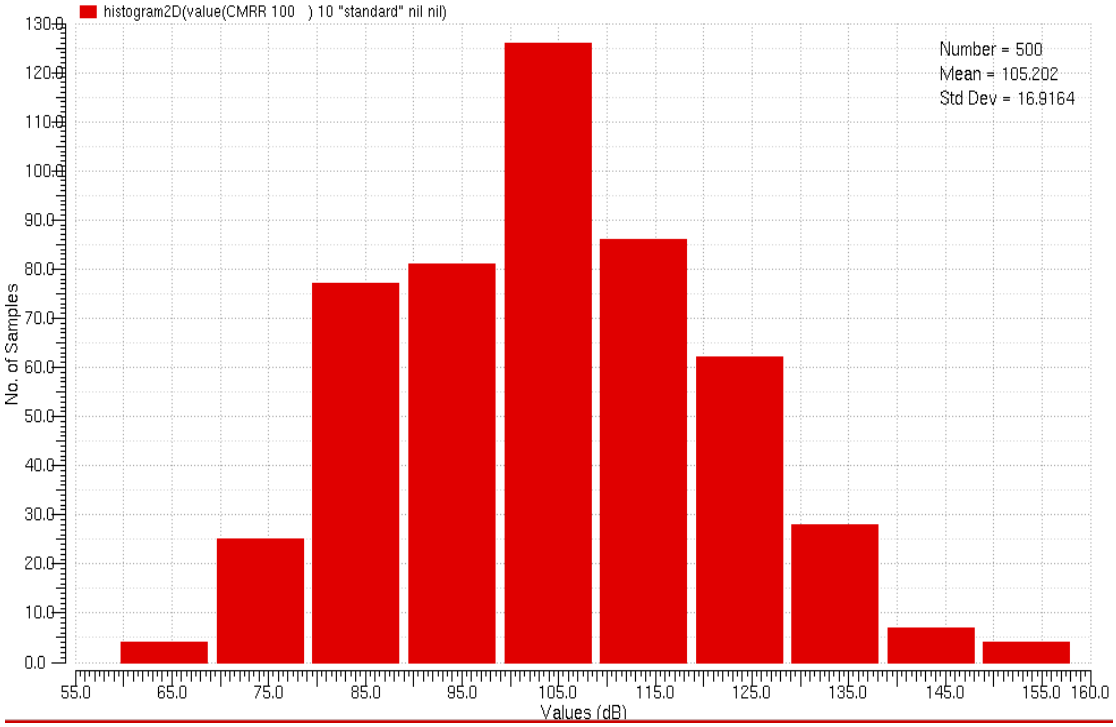

Figure 5. 10 CMRR histogram of the amplifier at frequency = 100Hz (cc = 0.95, N = 500, higher constraint)

For MUX, the matching between transistors will not affect the power consumption that much. Thus it is easier to implement the MC simulation for MUX than that for the amplifier. Figure 5.11 shows the power consumption histogram for MUX, it can be seen that most of the power samples concentrate on the range between 700nW and 800nW, which is really closed to the design result (807nW) in the normal simulation. This MC simulation result shows that the analog MUX can have a good power performance in the chip fabrication process. More MC results of the MUX will show in appendix C.

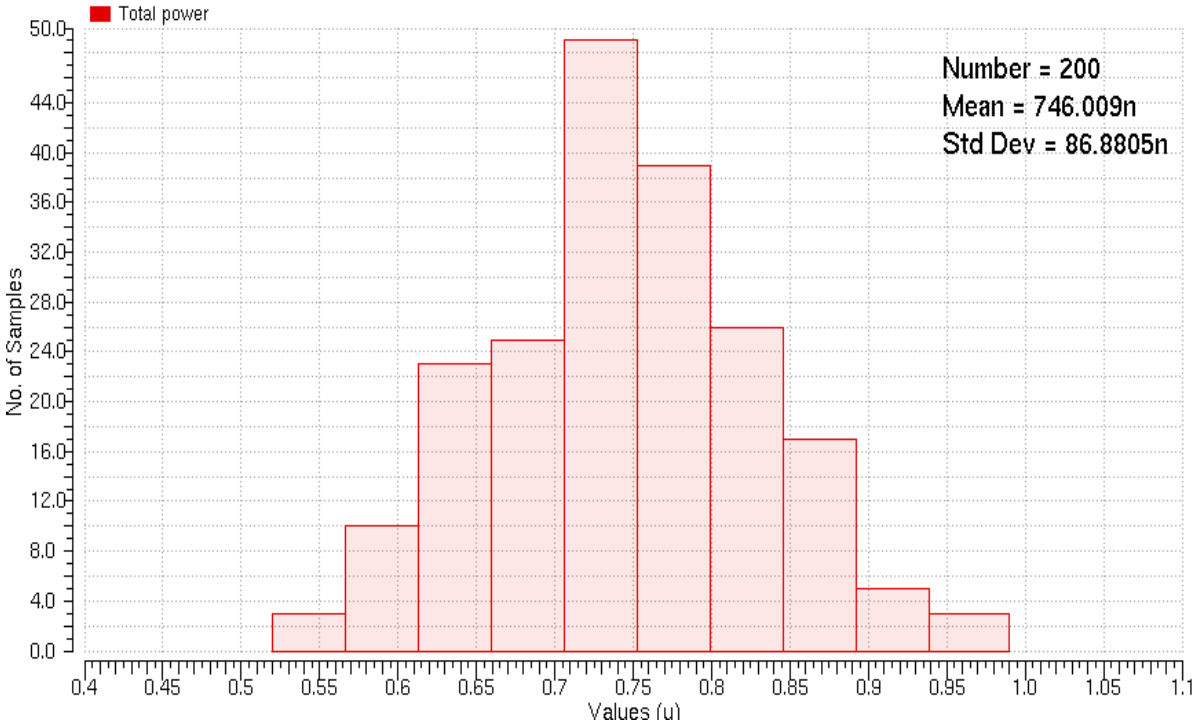

Figure 5. 11 Power histogram of the MUX (N = 200)

5.2 Layout Design

The implementation of the analog MUX and the bio-amplifier are in IBM 0.13uM CMOS technology within 1mm×1mm chip area.

Layout is a very important design step of integrated circuit manufacturing, which uses planar geometric shapes to represent the components (such as metal, oxide or semiconductor layers) of integrated circuit. The performance of the final chip will be affected by the positions and interconnections of those geometric shapes, thus through properly placing the circuit components in the layout will minimize the noise and outside interference in the circuit and then realize a high-quality circuit. There are some tips which can be followed. Firstly, routing power and ground, and placing NMOS devices near GND and PMOS devices near VDD. Secondly, place poly vertically and diffusion horizontally to keep them orthogonal. There are two types of diffusion which are ndiff and pdiff, they can't connect directly. Thirdly, for large transistors, they can be split into parallel connections by using multiple fingers for gate to reduce the overall gate resistances [39]. By following the above rules, it will become easier when wiring circuit and correcting DRC errors. In the electronic circuit, parasitic effects exist in both designed devices and wiring interconnects, parasitic extraction can create an accurate analog model with parasitic components, which is used to check if the designed circuit can still achieve the desired performance with the extra parasitic components. In high frequency circuit, the parasitic components cause unexpected phase shifts and instabilities. But, in low frequency circuit, parasitic

capacitance can usually be ignored. For this low frequency design, the post layout simulation results will not have a big difference comparing to the previous simulation results.

Also, during chip fabrication, the process variations may limit the accuracy and desired performance, matching between components becomes very important in the layout of analog circuit design. For example, mismatching in the analog MUX and the bio-amplifier will lead to undesired noise, offset, poor gain and CMRR. Therefore, in the layout of NMOS and PMOS transistors, it is very important to follow the rules of the inter-digitization and common centroid techniques in order to get a better matching between the components [40].

In this design, the differential pairs (for example: figure 5.17), NMOS current mirror (figure 5.19), PMOS current mirror (figure 5.18) are all connected by using interdigitated technique and multiple gate fingers connections in order to get a good matching. The final chip layout of the analog MUX and bio-amplifier (figure 5.21) is with bonding pads and the electrostatic discharge (ESD) protections. The bonding pads are placed on the chip which is used to connect the chip to the external devices [25]. ESD is placed on the transistor input gate which is used to protect the transistor being destroyed by the electrostatic discharged.

The layout figures of the analog MUX and the bio-amplifier are shown below.

Figure 5.12 is the layout of one channel differential MUX. The layout size is 19.02µm × 20.4µm.

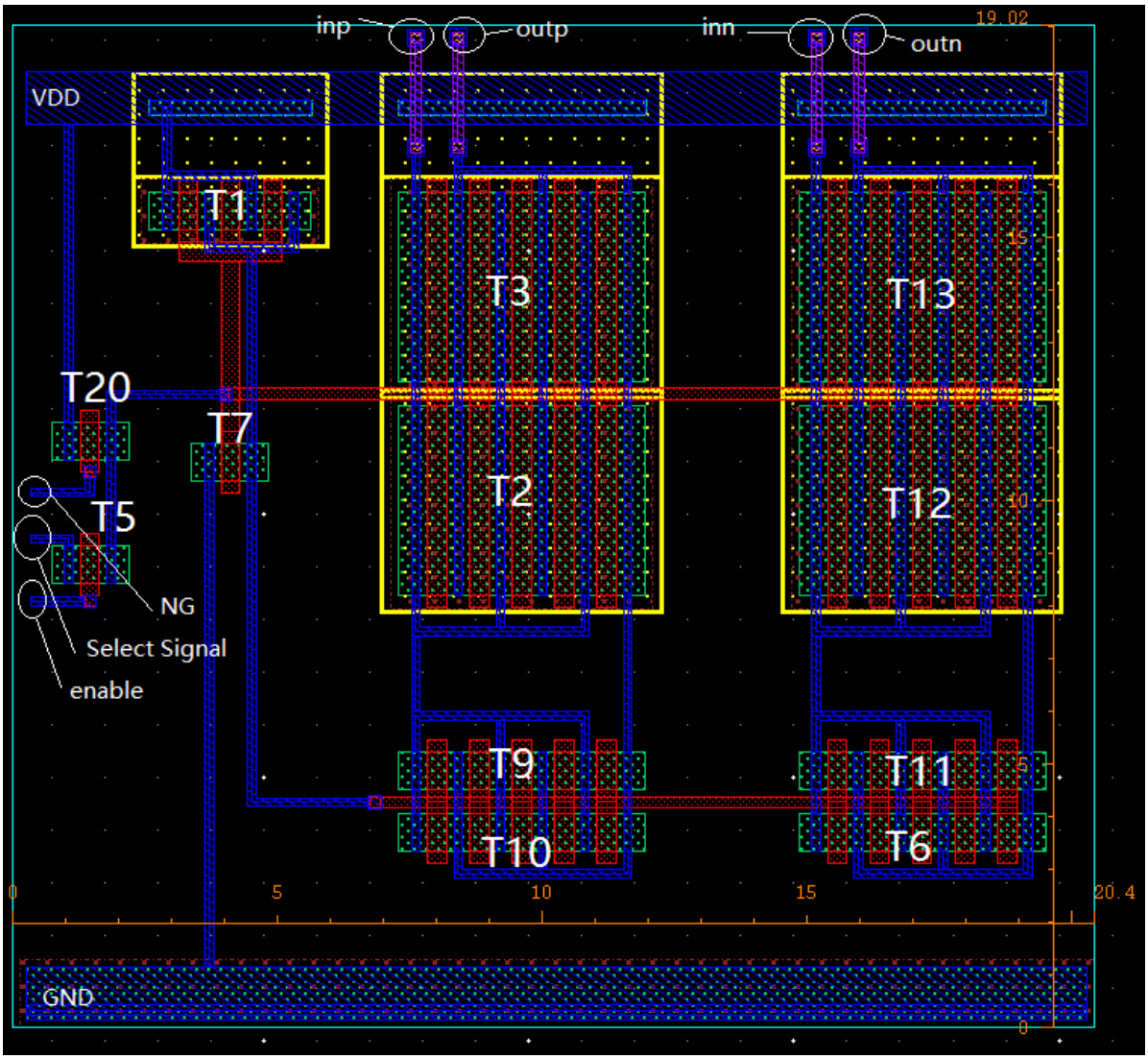

Figure 5. 12 shows one channel differential MUX layout, its corresponding schematic is presented in figure 4.4.

Figure 5.13 is the layout of eight channels differential MUX. The enable block controls the entire MUX to turn on or turn off. The select signal in each channel (see Figure 5.9) is used to switch the channel on or off. The layout size is $196.94\mu m \times 23.45\mu m$.

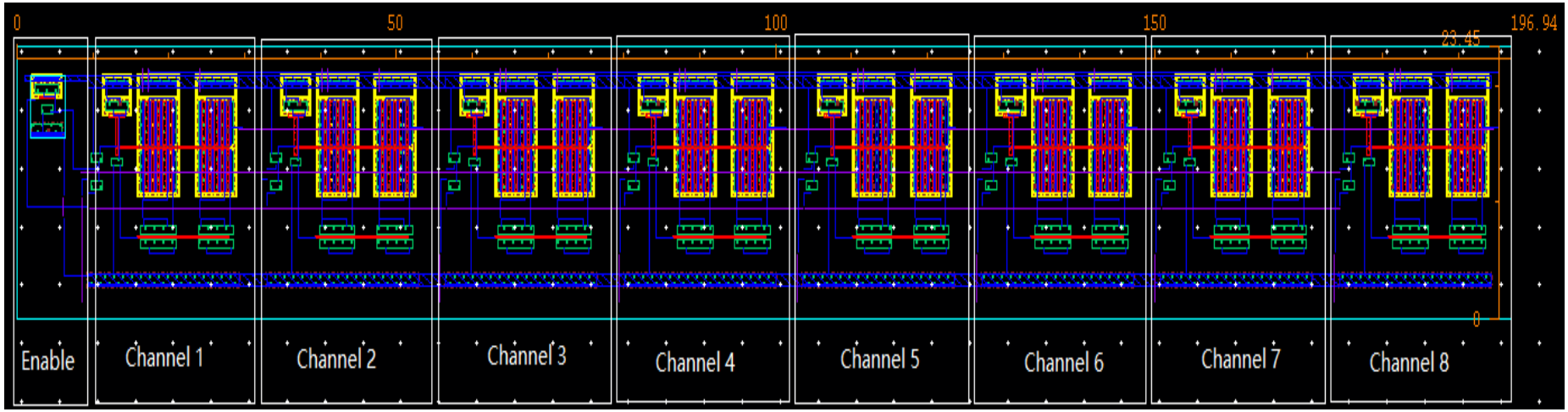

Figure 5. 13 shows eight-channel differential MUX layout, the corresponding schematic block is shown in figure 4.7.

Figure 5.14 is the layout of Nand3 gate in decoder. There are three PMOS transistors and three NMOS transistors. In order to save layout space, all the PMOS transistors share the source or drain with each other. This is also the same to NMOS transistors.

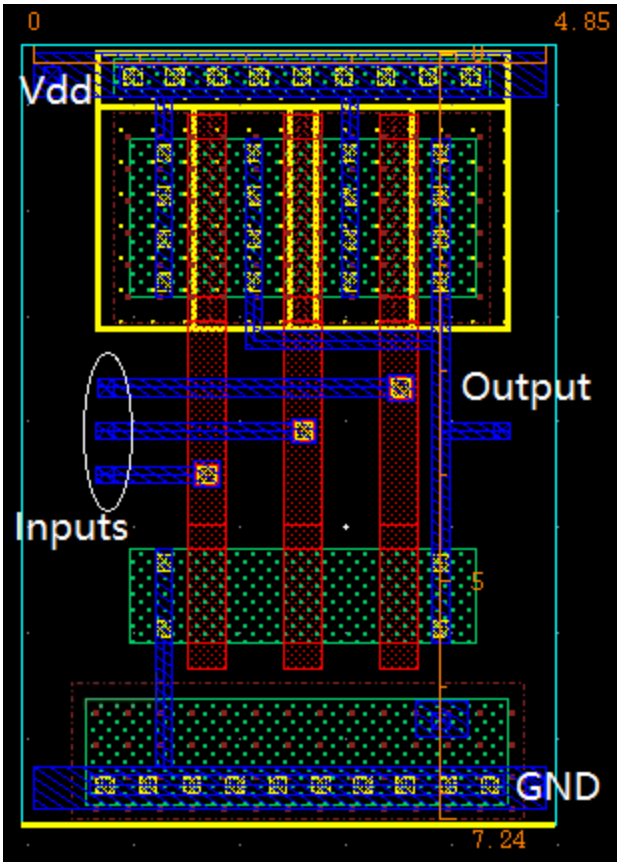

Figure 5. 14 Nand3 layout in decoder

Figure 5.15 is the layout of inverter in decoder. The PMOS transistor uses three fingers to reduce the area cost.

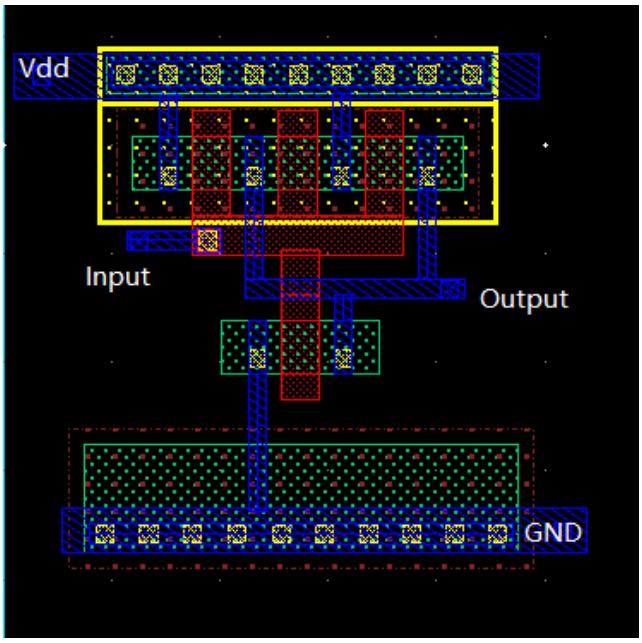

Figure 5. 15 Inverter layout in decoder

Figure 5.16 is the layout of decoder. The layout size is $42.75\mu m \times 21.1\mu m$

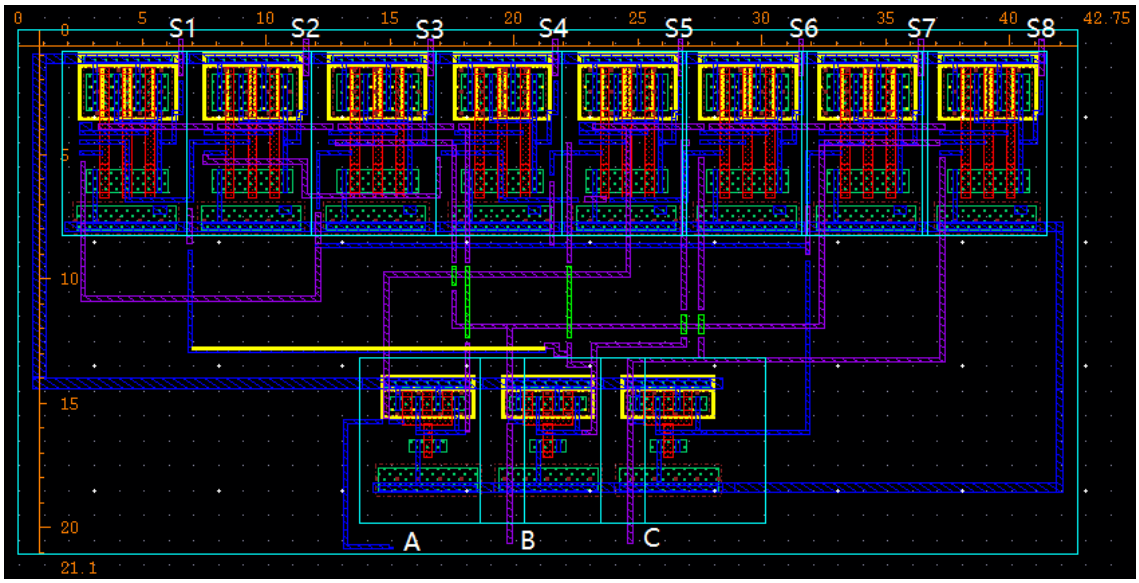

Figure 5. 16 Decoder layout

Figure 5.17 is the layout of NMOS differential pair in the first stage of amplifier. The multiplicity of the differential pair (T4, T5) is four. T4 and T5 transistors share the source terminal and they are placed by using common centroid technology. In the layout, first two and last two gates are belong to T5, the other four gates in the middle are belong to T4.

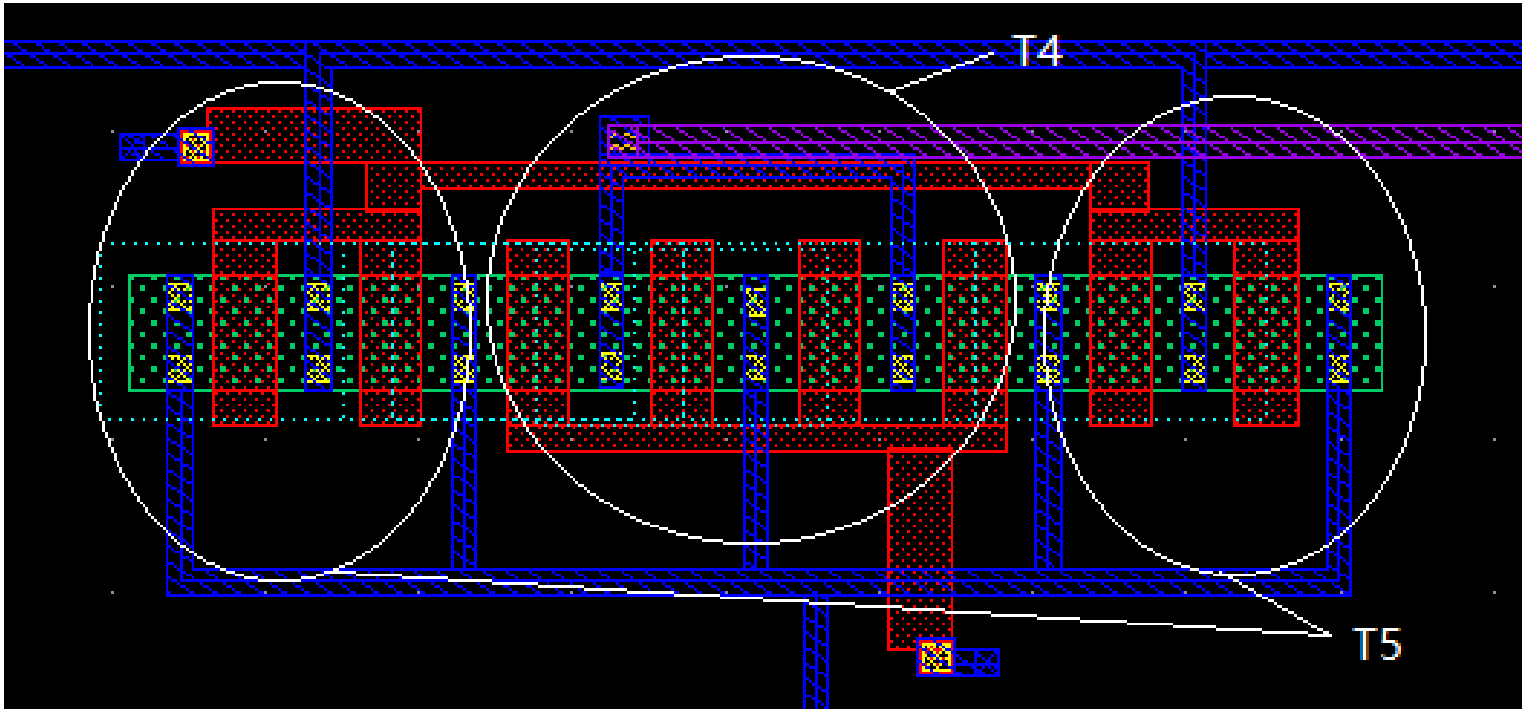

Figure 5. 17 First stage NMOS differential pair layout

Figure 5.18 is the layout of PMOS current mirror in second stage of amplifier. This layout is also used common centroid technology. The multiplicity of the differential pair (T19, T20) is four. It can be seen that the second, third, sixth and seventh gates are belong to T20, the others are belong to T19.

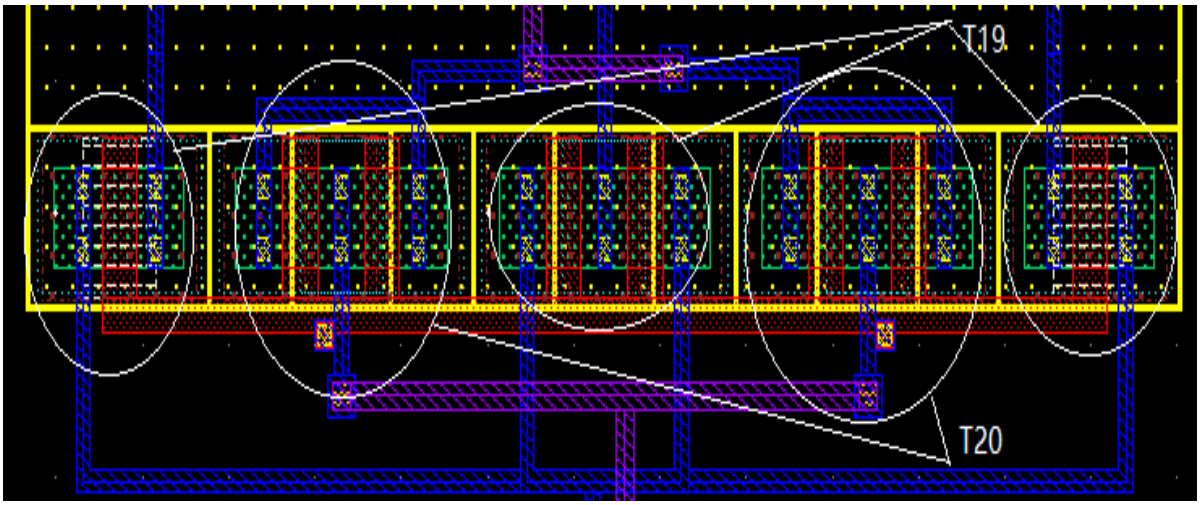

Figure 5. 18 Second stage PMOS current mirror layout

Figure 5.19 is the layout of NMOS current mirror in second stage of the amplifier.

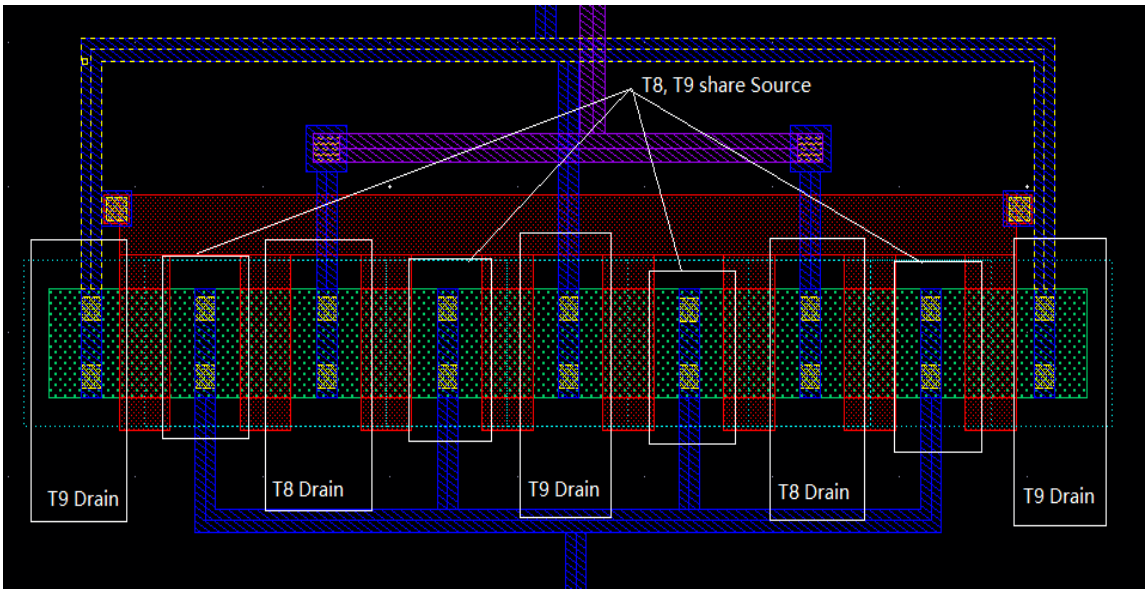

Figure 5. 19 Second stage NMOS current mirror layout

Figure 5.20 is the layout of bio-amplifier layout. The layout size is $78.79\mu m \times 20.85\mu m$

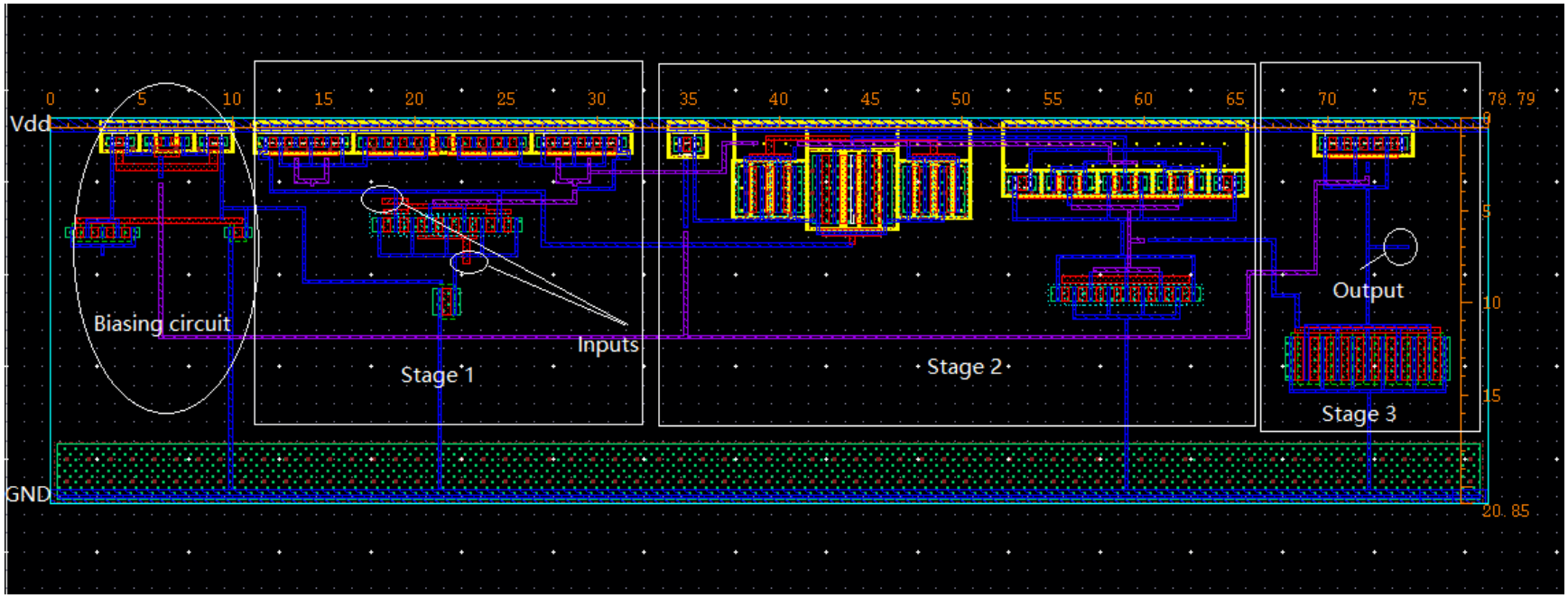

Figure 5. 20 Bio-amplifier layout

The final circuit layout with Design Rule Check (DRC) and Layout Versus Schematic (LVS) clean is shown in Figure 5.21. For ease of observation, the filler cells are not added in this figure but did in the final layout version.

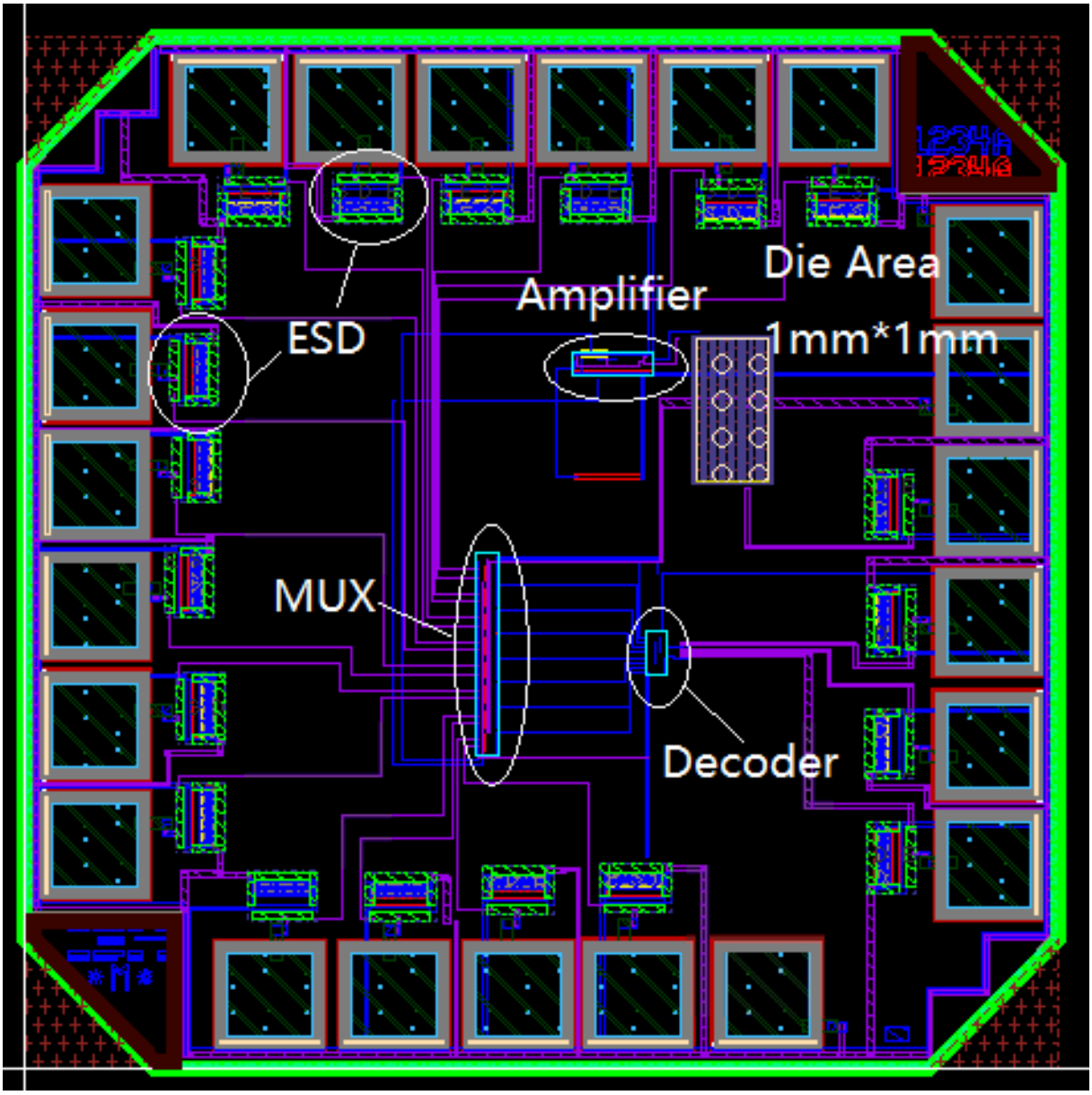

Figure 5. 21 Layout of the whole circuit (include analog MUX and bio-amplifier)

Chapter 6

Conclusion and Future Work

The core part of this thesis is the 8 to 1 analog MUX, which can be applied to medical portable devices. Thus, the linearity and power consumption are the main challenge for this research. This chapter summarizes the efforts and approaches of the research.

6.1 Thesis Summary

The designed 8 to 1 analog MUX can be widely used in the bio-signal acquisition system. The most important block that uses to implement this analog MUX is the TG. By using the parallel TG, R_{on} can be further reduced, and through properly sizing the transistors in the TG, the linearity of Ron can be greatly improved and the power consumption of eight-channel switches are optimized. Then the low frequency and low amplitude bio-signals can be accurately transmitted by the analog MUX with less attenuation.

To amplify the differential output signals of the MUX and reduce the common mode interference, a three-stage bio-amplifier topology [7] is introduced with high CMRR and high voltage gain.

This research also provides the Monte Carlo simulation results of the design. During chip fabrication, some small randomly variations and device mismatch occur, which may affect the design performance. MC simulation is used to predict the performance of the designed devices after manufactured. The MC simulation results reflect the error-tolerant rate of the devices and give insights into feasibility of the design.

In the layout design, common-centroid layout technology is used to improve the device matching. Through sharing the drain or source among the same type transistors, the layout area can be reduced.

6.2 Future Work

This research uses eight differential channels to implement the analog MUX. To further improve this research, a dummy channel can be used to replace the half of the parallel TGs in each single channel and form a differential structure with these eight channels. This method can decrease the number of transistors of the circuit, and then reduce the power consumption and the circuit complexity. Also, the comparison of the dominant noise (flicker noise and thermal noise) between a parallel TG and a single large gate transistor has been stated, but the other uncorrelated noise sources of these two type of structures are still need to be derived in mathematical method. The layout design of this work is for the future chip tape-out and a PCB (printed circuit board) will be designed for testing the chip.

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Appendix A

Multiplexer Classification

MUX can be classified into two categories. One is analog MUX which consisted of MOSFET components, the other one is digital MUX which built by using high speed logic gates. In the aspect of processing the different input signals, analog MUX and digital MUX have different advantages. Both analog MUX and digital MUX can select a simple high or low level input digital signal from multiple channels, digital MUX usually has faster signal processing capability compare to the analog MUX. When it comes to analog input signals such as sine wave signal, it is better to choose analog MUX to avoid parts of the sine signal being clipped, analog MUX is more accurate when processing analog signal. Therefore, choosing which type of MUX to design depends on the design requirements.

Digital MUX is used to deal with the signals contain high level and low level binary information, in another words, digital MUX can only process the digital signals. It utilizes the high speed logic gates to achieve the function of multiplexing, versus with analog MUX, data are processed in digital system can achieve faster processing speed. See the example [41] of a 4 to 1 digital MUX in Figure A.1(a), and its logic structure is showed in Figure A.1 (b), its logic function is presented in table 14. The function of this circuit is as follows:

For S0 = 0, S1 = 0, the output result is Y = I0,

For S0 = 0, S1 = 1, the output result is Y = I1,

For S0 = 1, S1 = 0, the output result is Y = I2,

For S0 = 1, S1 = 1, the output result is Y = I3,

And this 4 to 1 MUX can be written in the Boolean expression,

$$Y = I_0\overline{S_0}\,\overline{S_1} + I_1\overline{S_0}S_1 + I_2S_0\overline{S_1} + I_3S_0S_1 \qquad (A.1)$$

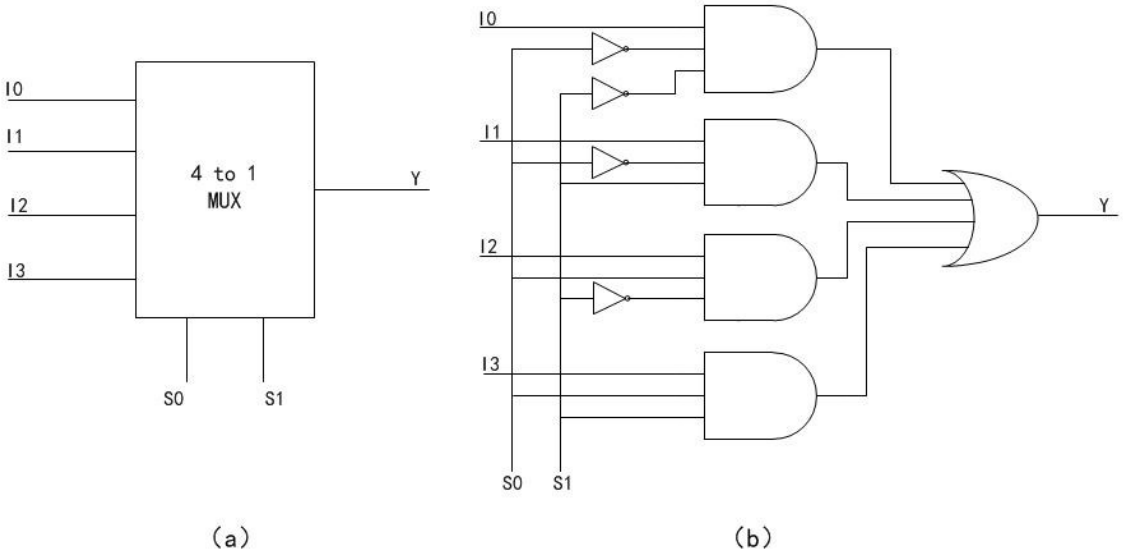

Figure A. 1（a）4 to 1 Digital MUX（b）Logic Structure of MUX

S0	S1	Y
0	0	I0
0	1	I1
1	0	I2
1	1	I3

Table 14 Function Table of 4 to 1 MUX

Analog MUX can handle both digital input signals such as binary information and analog input signals such as sine wave signals. Nowadays, CMOS switch technology has

become the main technology in analog MUX design. It is well known throughout the world by its beneficial characteristics, such as low quiescent power dissipation, less supply current while switching and cheap in materials. The analog MUX can be designed by using binary addressed decoder and a number of parallel analog switches. Generally, a MUX has an Enable pin, the Enable pin is used to control all of the channels turn on or turn off. The purpose of this type design is to minimum the number of channel select control pins [42]. Figure A.2 shows the brief connecting structure of a 4 to 1 MUX and its controller —— a decoder.

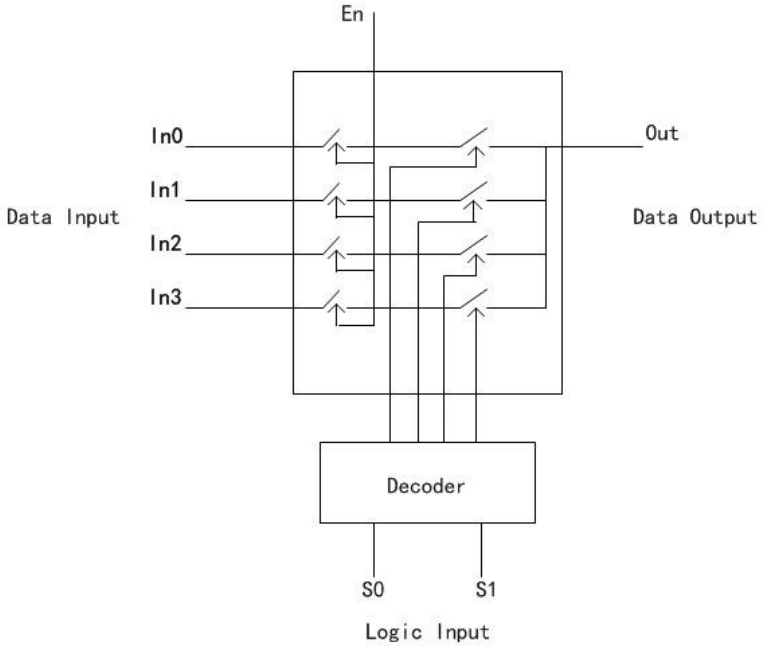

Figure A. 2 A Simple 4 to 1 MUX with a Controller

Appendix B

Op-amp parameter and characteristics

Op-amp Offset Voltage

Input offset voltage V_{os} [43] should be concerned if the DC accuracy is required of the circuit. The offset voltage is usually modeled as a voltage source which is connected in series with the inverting input of the op-amp, see the model in Figure B.1.

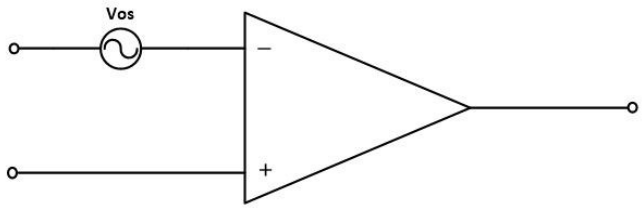

Figure B. 1 Offset Voltage

The offset voltage varies with temperature and time. The V_{os} is affected by temperature coefficient, the unit of temperature coefficient is μV/℃. Normal aging in semiconductors causes changes in the characteristics of devices, this is long term drift of the offset voltage. The unit of long term voltage drift is μV/month.

Input Common-mode Range

The input common-mode voltage is the average voltage at the inverting and noninverting input terminals [39]. The input common-mode range V_{os} is a voltage range

which can keep the op-amp maintain the normal amplification function. When the input voltage exceeds the input common-mode range, then the operational amplifier will stop working. Also, when the input common-mode voltage gets too high or too low, the operational amplifier will shut down or won't work properly. To different input stage op-amp, the input common-mode voltage is different.

Maximum and minimum differential input voltages

Figure B.2 is a differential amplifier, it can be used to calculate the maximum and minimum differential input voltages on the gate of M1 which can guarantee that neither M1 nor M2 is shut off.

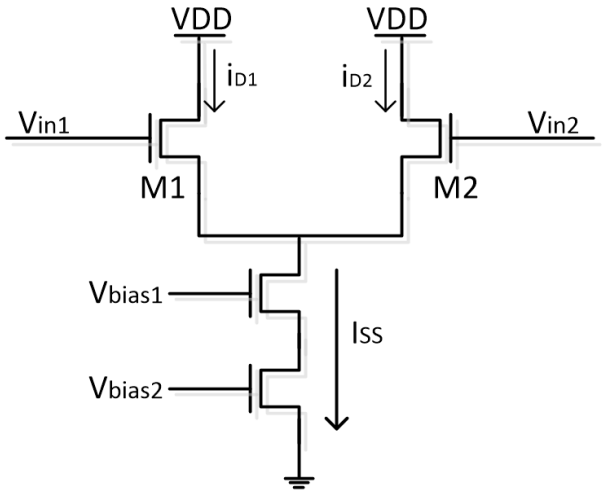

Figure B. 2 Differential Amplifier uses to find V_{DIMAX} and V_{DIMIM}

The maximum differential input voltage V_{DIMAX} can be achieved by setting i_{D1} to I_{SS} and i_{D2} to 0 which means M1 conduct all the tail bias current and M2 is off.

$$V_{DIMAX} < V_{I1} - V_{I2} = \sqrt{\frac{2 * L * I_{SS}}{KP_N * W}} \qquad \text{(B.1)}$$

The minimum differential input voltage V_{DIMIN} can be achieved by setting i_{D2} to

I_{SS} and i_{D1} to 0 which means M2 conduct all the tail bias current and M1 is off.

$$V_{DIMIN} = -V_{DIMAX} = -(V_{I1} - V_{I2}) = -\sqrt{\frac{2 * L * I_{SS}}{KP_N * W}} \quad \text{(B.2)}$$

Using (B.1) can estimate the maximum voltage on the gate of M1 which is

$$V_{I1MAX} = \sqrt{\frac{2 * L * I_{SS}}{KP_N * W}} + V_{I2}$$

The minimum voltage on the gate of M1 is

$$V_{I1MIN} = V_{I2} - (V_{I1MAX} - V_{I2}) \quad \text{(B.3)}$$

When transistor M1 and M2 are the same, then the input current are equal $I_{M1} = I_{M2} = \frac{I_{SS}}{2}$.

Maximum and minimum common-mode input voltages

Figure B.3 is a differential amplifier with both inputs tied together [39], it can be used to calculate the maximum and minimum input common-mode voltages which can guarantee that both M1 and M2 operate in the saturation region.

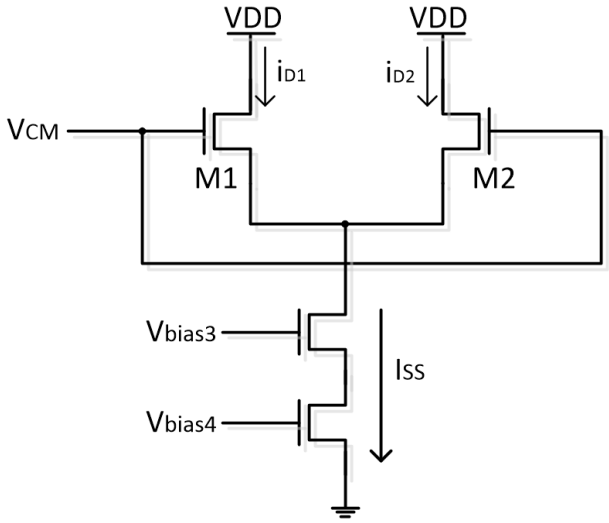

Figure B. 3 Differential Amplifier uses to find V_{CMMAX} and V_{CMMIM}

To keep both M1 and M2 operate in the saturation region

$$V_{DS} \gg V_{GS} - V_{THN} \rightarrow V_D \gg V_G - V_{THN} \quad \text{(B.4)}$$

As $V_D = V_{DD}$, then the maximum common-mode voltage can be written as,

$$V_{CMMAX} = V_{DD} + V_{THN} \quad \text{(B.5)}$$

From (B.5) we can see the input common-mode voltage can be higher than VDD before M1 and M2 move into the triode region.

The minimum common-mode voltage can be written as,

$$V_{CMMIN} = V_{GS1,2} + 2 * V_{DSsat} \quad \text{(B.6)}$$

Where the minimum voltage across the current source is assumed to be $2V_{DSsat}$.

From Figure B.10 we can understand the common-mode range is the maximum and minimum voltage which can keep both transistor M1 and M2 operating in the saturation region. The maximum common-mode voltage is V_{CMMAX} and the minimum common-mode voltage is V_{CMMIN}. When the voltage on the gate of M1 and M2 is too high, then both M1 and M2 will operate in triode region which means they behave as resistors. When the voltage on the gate of M1 and M2 is too low, then both transistors M1 and M2 will shut down. [39]

Common-mode Rejection Ratio

The common-mode rejection ratio (CMRR) of a differential amplifier measures its ability to reject a common-mode signal applied to the differential pair inputs [44]. For an ideal differential amplifier, it should have an infinite CMRR. However, in practical amplifiers, the common-mode input voltages cannot be entirely subtracted at the output,

the common-mode voltage gain is not equal to zero, which means in the amplification circuit, the output signals will also contain some amplified common-mode signals. For differential amplifiers, the higher the CMRR is, the stronger the amplification ability it has to amplify the differential signals and reject the common-mode signals.

For a practical amplifier, the output voltage can be written as,

$$V_O = A_d * (V_+ - V_-) + \frac{1}{2} A_{cm} * (V_+ - V_-) \quad \text{(B.7)}$$

Where V_+ and V_- are the inputs of the differential amplifier, V_O is the output of the differential amplifier.

The common-mode rejection ratio can be written as,

$$\text{CMRR(dB)} = 10log_{10}(\frac{A_d}{A_{cm}})^2 = 20log_{10}(\frac{A_d}{|A_{cm}|}) \quad \text{(B.8)}$$

Where A_d is the differential gain, A_{cm} is the common-mode gain.

Appendix C

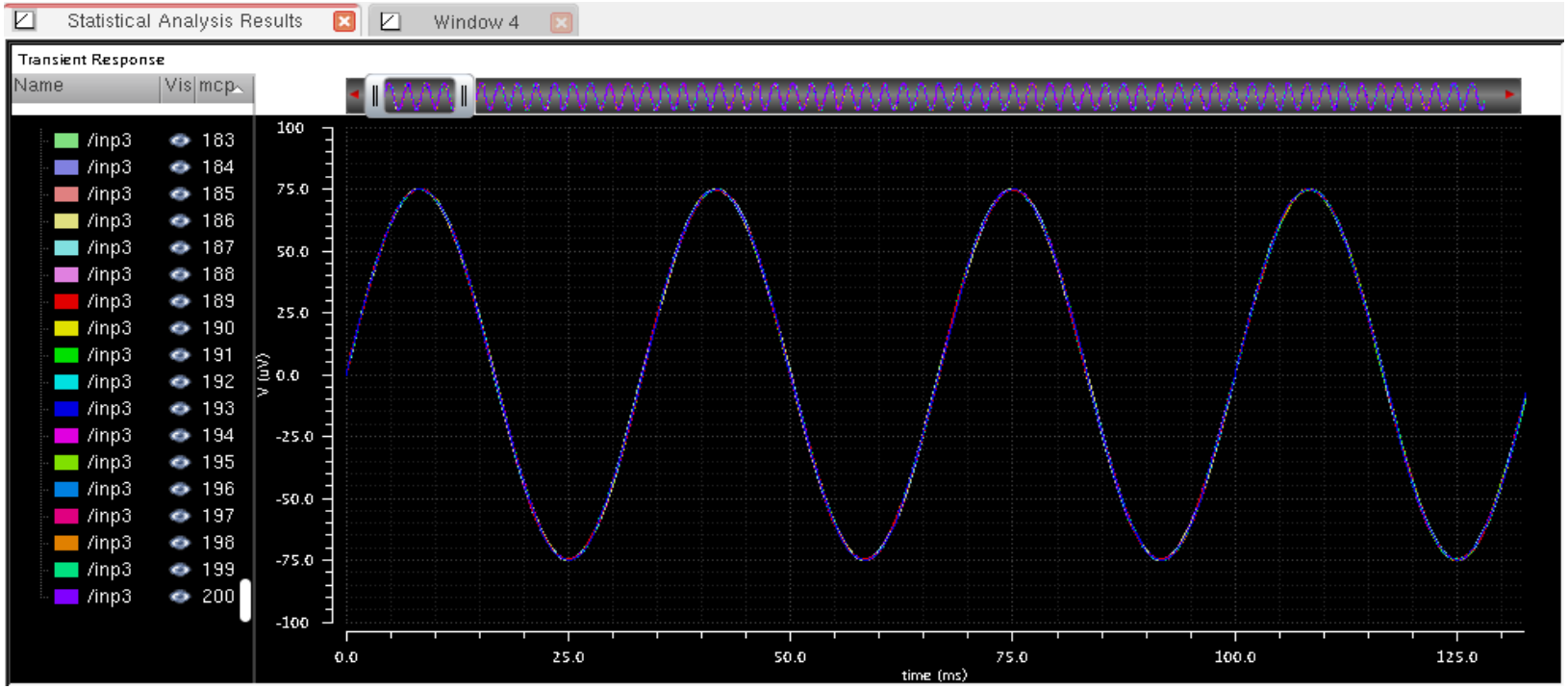

Figure C. 1 One Channel Monte Carlo Input Signal Family (example: Inp3)

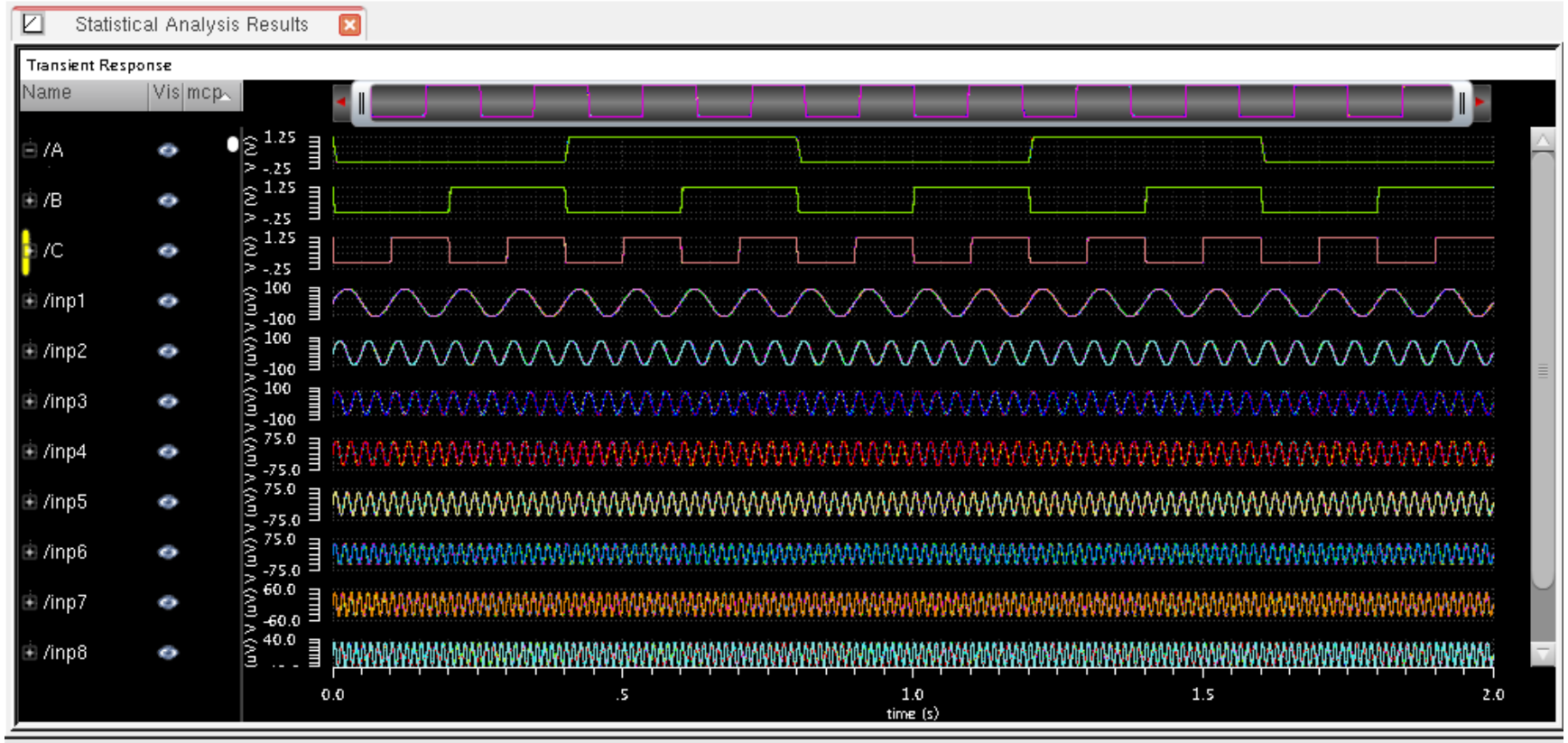

Figure C. 2 Eight-channel Monte Carlo Input Signal Families and Control Signals Families

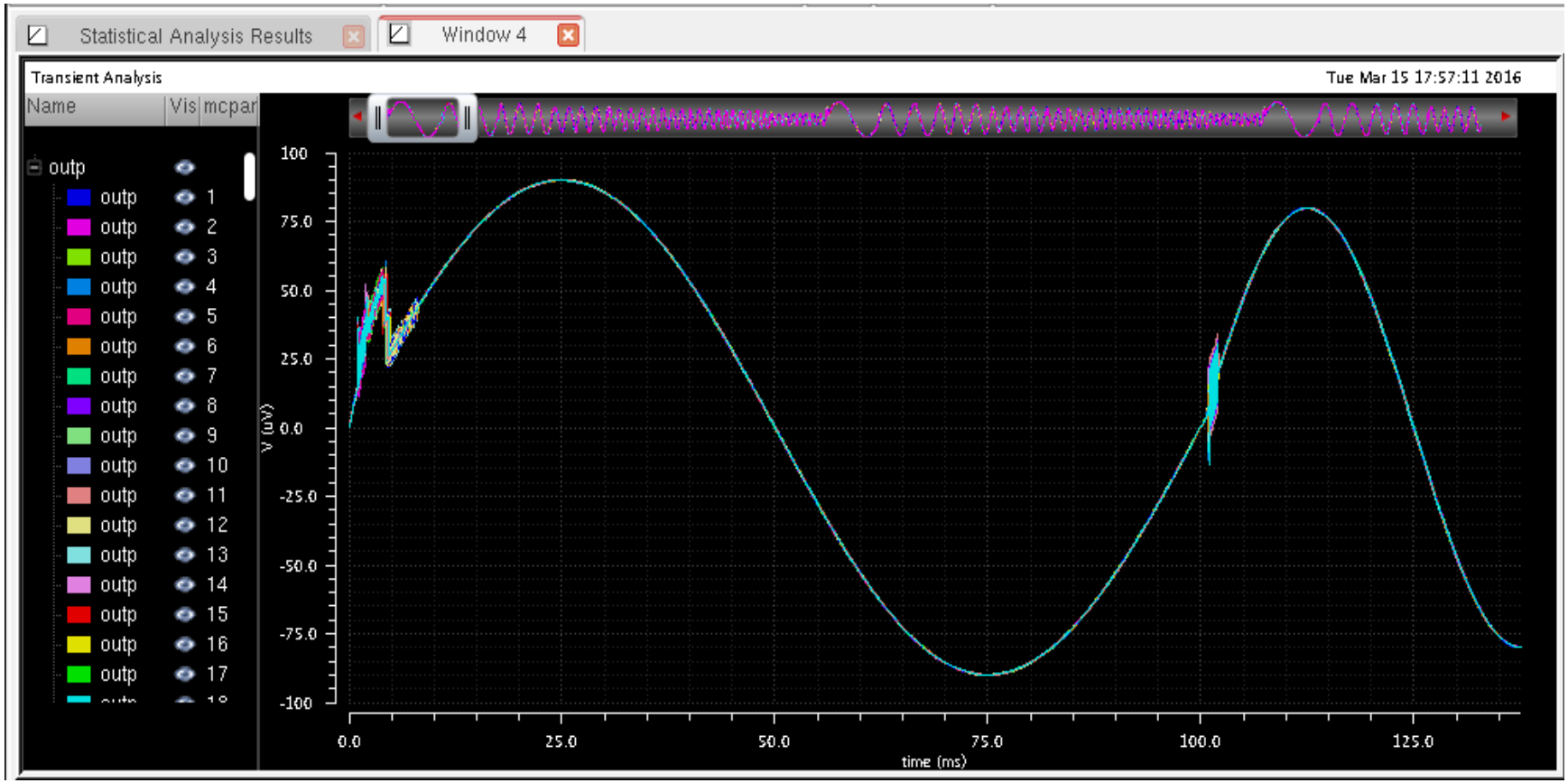

Figure C. 3 Zoomed In Monte Carlo Output Signal Family

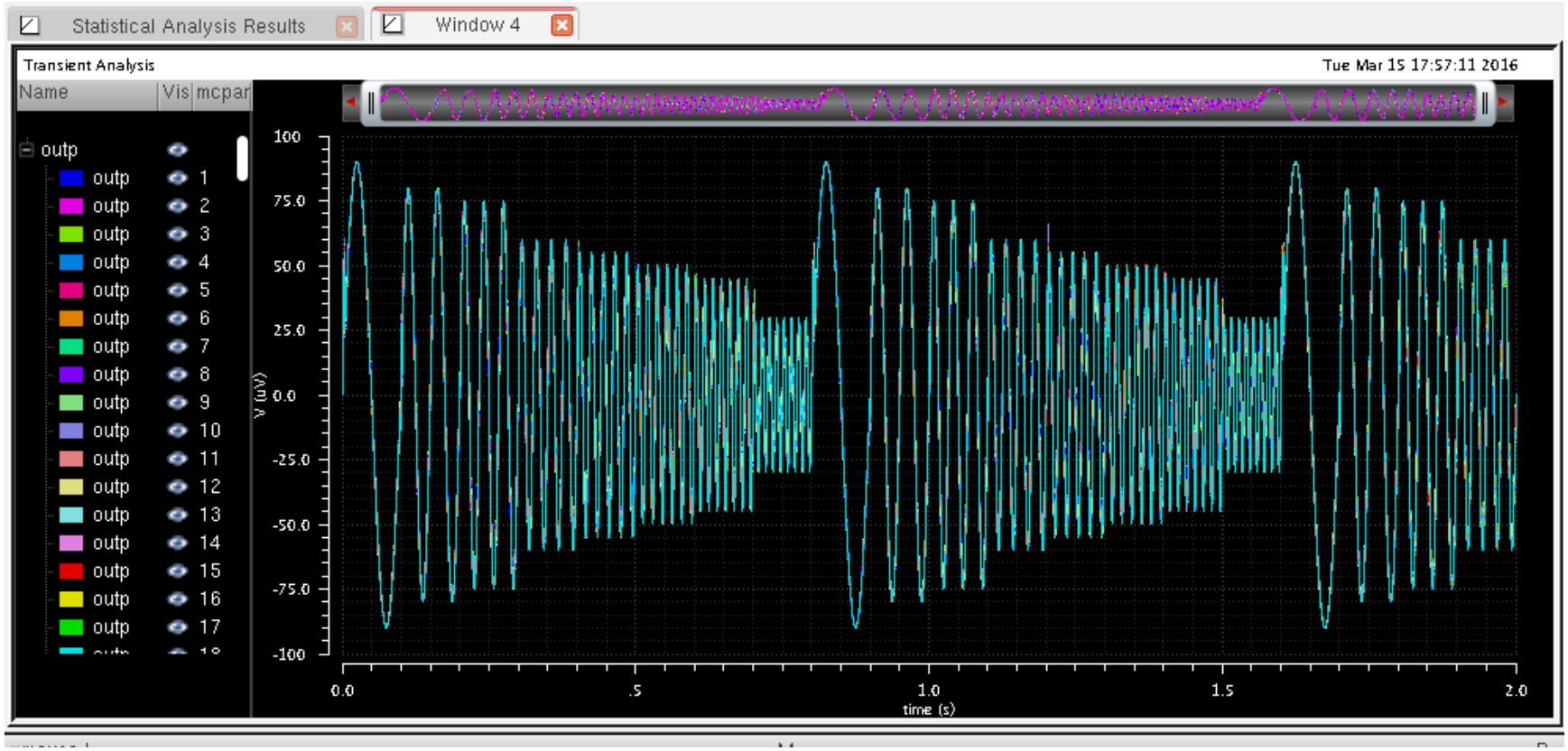

Figure C. 4 Full View Monte Carlo Output Signal Family

Appendix D

Electrodes

In bio-signal recording, biosensors are used to acquire electrical signals from the surface of the skin and emanating from bio-potential sources [10]. Figure D.1 is the simplified connection structure between wet electrodes and the body.

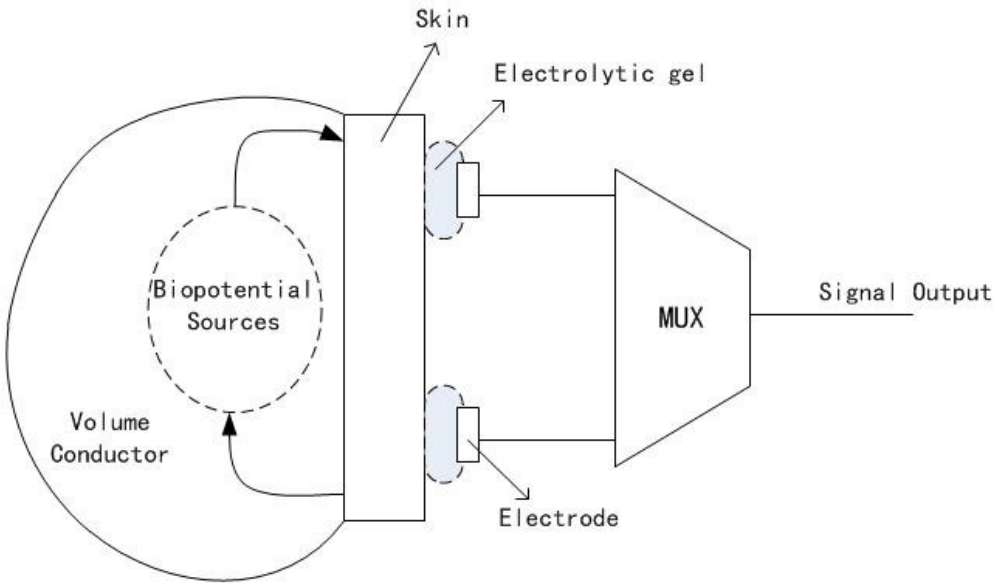

Figure D. 1: Shows the connection structure of electrode-to-skin interface [10]

There are three types of bio-electrode which are wet, dry and insulating bio-electrodes, respectively. Wet electrodes are usually made of metal Silver Chloride (AgCl), and incorporate electrolytic gel to decrease the electrical resistance and provide a conductive path between skin and electrode. Generally, this wet electrode is widely used in clinical practice. With no electrolytic gel, dry electrodes use micro-needles to penetrate the skin

layer and are placed onto the skin or scalp directly to pick up the neural activity of the body [11]. An insulating electrode is made of metal or semiconductor with a thin dielectric surface layer, and it operates with displacement currents instead of real charge currents which can extract the bio-potential without galvanic contact with the skin [11].

Wet electrodes are widely used in clinical medicine because of their simple configuration and lightweight construction. In contrast, dry electrodes and insulating electrodes need buffer circuits and external power supplies, which increases the complexity and the weight of these devices. In addition, from the hygiene perspective, wet electrodes are disposable. When compared to dry or insulating electrodes, wet electrodes are relatively cheap. Moreover, wet electrodes have sufficiently low contact impedances, which allows the devices to make a good recording [12].

However, for a long time recording, the dry electrodes and insulating electrodes are more suitable. Dry or insulating electrodes are more stable, and reliable according to their geometry and size. Moreover, comparing to the wet electrodes, dry or insulating electrodes have a longer life cycle. With the shielding configuration, dry and insulating electrodes can greatly decrease the interference causing by moving electric charge [12].

In order to detect diverse bio-signals, the proper type of sensors are applied on different surfaces of the body. Table 15 shows the sensors types and locations for different kinds of bio-signals.

Bio-signals	Sensor Type	Sensor Location
EEG signal	AgCl electrodes	Scalp
ECG signal	Disposable electrode	Thorax
EMG signal	Disposable electrode	Hand & Leg
Facial EMG	Disposable electrode	Face
Pulse (Heart rate)	Photoelectric	Finger & Earlobe
Respiration	Belt/Nose flow electrode	Thorax & Abdominal
Electrodermal Activity	Finger electrode	Hand & Foot & Forehead

Table 15: Shows various bio-signal sensors and their locations on the human body [13]

Appendix E

Amplifier design

This section provides the information of the amplifier which is used to amplify the bio-signals from the designed analog MUX. In order to eliminate the unwanted common mode component, a differential amplifier structure is implemented. Usually, the amplitude of the bio-signal is at the microvolt level, so at least we need to amplify it to the millivolt level for better observing. In other words, the designed amplifier needs a 1000 times magnification, which is 60dB. As the amplifier is for bio-signal, a wide bandwidth is not required in this design but low power consumption and high CMRR are preferred. The amplifier uses compensating circuit to increase its phase margin and stability. In the following sections, different stages of the amplifier will be discussed.

E.1 Biasing Circuit

In amplifier design, an important step is to choose the proper DC operating point for MOSFETs. The proper and stable drain current I_D and drain to source voltage V_{DS} are needed in the circuit to guarantee that the MOSFETs operate in their saturation region.

Figure E.1 shows the biasing circuit structure. Resister R_B is connected to the source of T3 which is used to fix V_{G3}, and the fixed V_{G3} can be used to bias the next stage. The gate voltage of T3 can be presented as:

$$V_{G3} = V_{GS3} + R_B I \tag{E.1}$$

When $V_{G3} \gg V_{GS3}$, drain current I is mainly dependent on V_{G3} and R_B. When V_{G3} is fixed, if drain current I increases for some reason, then V_{GS3} would decrease. According to the current equation of a MOSFET in saturation region, a decreased V_{GS3} would also cause drain current I decrease. Thus, R_B can be used to stabilize the drain current I.

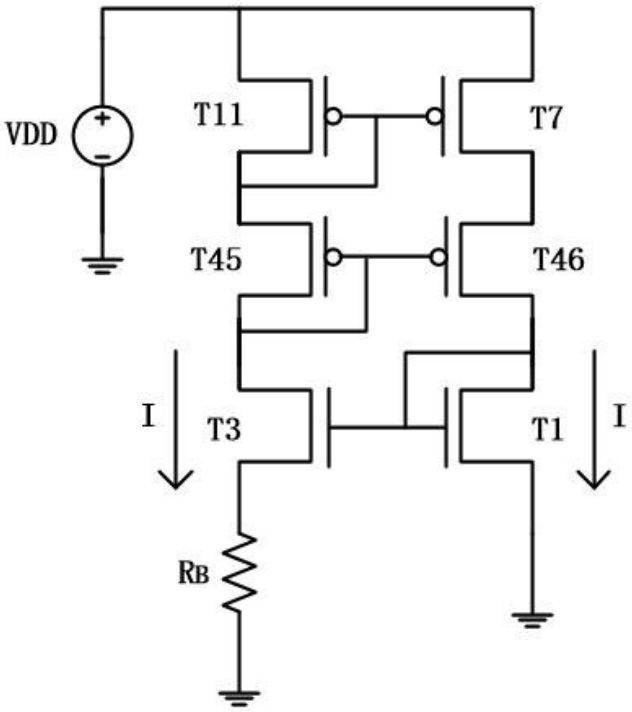

Figure E. 1 Biasing circuit of the amplifier

The transistor size ratio can be derived by the following expressions.

$$(W/L)_{11} = (W/L)_7 \Longrightarrow I_{D3} = I_{D1} \tag{E.2}$$

$$V_{gs1} = V_{gs3} + I_{D3} R_B \tag{E.3}$$

$$V_{EFF1} = V_{EFF3} + I_{D3} R_B \tag{E.4}$$

$$\sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}} = \sqrt{\frac{2I_{D3}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_3}} + I_{D3}R_B \tag{E.5}$$

$$\because I_{D3} = I_{D1} \tag{E.6}$$

$$\therefore g_{m1} = \sqrt{\mu_n C_{ox}\left(\frac{W}{L}\right)_1 I_{D1}} = \frac{2\left(1 - \sqrt{\frac{(W/L)_1}{(W/L)_3}}\right)}{R_B} \tag{E.7}$$

$$\therefore (W/L)_3 = 4(W/L)_1 \tag{E.8}$$

$$\therefore g_{m1} = \frac{1}{R_B} \tag{E.9}$$

E.2 First Stage

The aim of this stage is to achieve a high CMRR rather than a high voltage gain. Figure E.2 introduces a simple differential amplifier, it explains the effect Rd on gain. The first stage circuit is improved and derived from this simple amplifier structure.

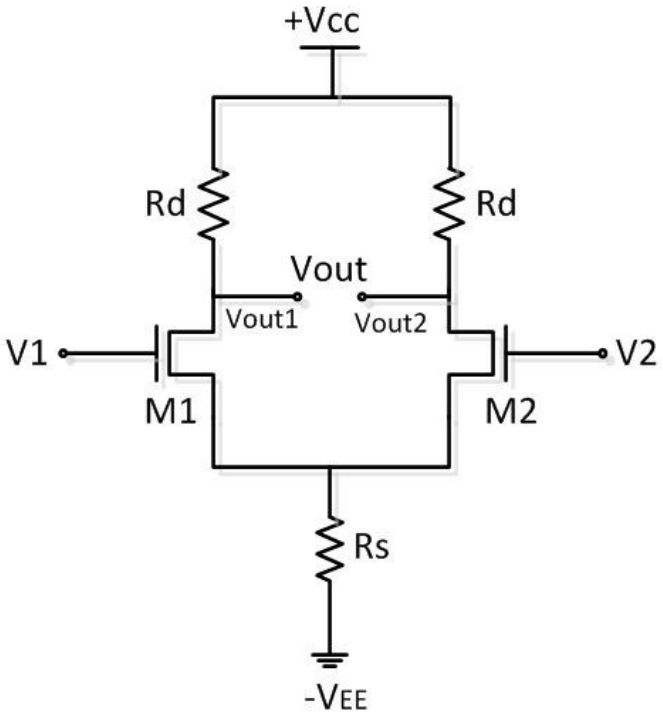

Figure E. 2 A simple differential amplifier [40]

As we all know, when G_m is fixed, the larger R_d is, the higher A_d can be achieved. However, resistors have bad precision in component matching (to implement high precision resistors in various techniques is possible, but they are costly), and integrating large resistors on a chip will require a large layout area. In this design, a diode connected transistor [45] is used to replace the load resistors. As the active load, transistors can provide a large A_d without consuming too much die area and power. Figure E.3 shows an NMOS diode connected transistor.

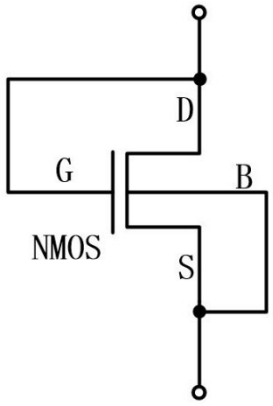

Figure E. 3 NMOS transistor in diode connected configuration

Since drain and gate are shorted, then we want to satisfy the following condition:

$$V_{DS} > V_{GS} - V_t$$

In other word, once $V_{GS} > V_t$, the transistor will conduct and enter into saturation condition. Then the drain current can be expressed as (E.10),

$$I_{DS} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{DS} - V_t)^2 \qquad \text{(E.10)}$$

Then the equivalent resistance of the transistor is,

$$\mathrm{R} = \frac{V_{DS}}{I_{DS}} = \frac{2LV_{DS}}{W\mu_n C_{ox}(V_{DS} - V_t)^2} = \frac{L}{W}\frac{2V_{DS}}{\mu_n C_{ox}(V_{DS} - V_t)^2} \qquad \text{(E.11)}$$

From equation (E.11), in order to get a larger equivalent resistance, a large L/W ratio

of transistors is needed. This is suitable for PMOS transistor as well. In this thesis, two diode connected transistors are connected in series for each branch, when a small voltage is applied across the load device, the equivalent resistance of the device will get extremely high, and a large A_d will be achieved. The tail transistor T6 is used to lower the A_{cm} of this stage. Therefore, this stage can provide high CMRR for the amplifier. The designed circuit is shown in Figure E.4.

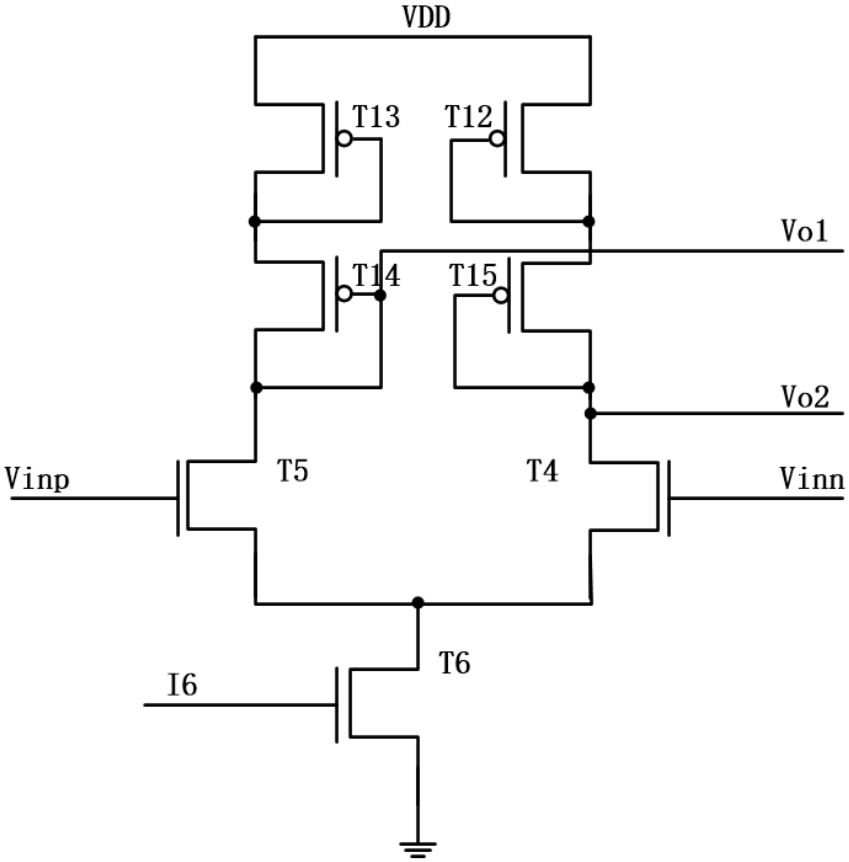

Figure E. 4 First amplification stage of the amplifier

E.3 Second Stage

The function of this stage is to transfer differential input signals into a single-ended output signal without loss. Usually, the output voltage (V_o) of the single-ended amplifier

is half of the output voltage (V_{od}) of the fully differential amplifier. From equation (E.12), we can surmise that the output gain of a single-ended differential amplifier is half of the gain of the fully differential amplifier.

$$A_{dv} = \frac{V_{od}}{V_{id}} = G_m \times R_{out} \qquad \text{(E.12)}$$

To overcome this drawback, a current mirror is used as the load of the single-ended differential amplifier. Figure E.5 shows the second stage circuit of the amplifier.

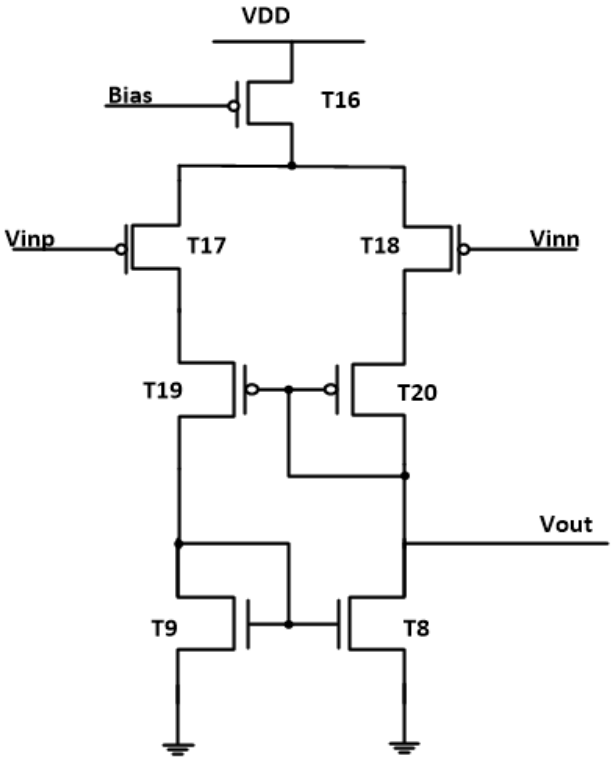

Figure E. 5 Second amplification stage of the amplifier

In this stage, the combination of T19, T20, T8 and T9 form a self-bias current mirror [46], it keeping the current of the two branches equal. This stage uses PMOS transistors as the differential pair, connecting to the NMOS common source amplifier in the next stage. For a common source amplifier, with the same drain current and transistor size，an

amplifier using an NFET has better amplifying ability compare to PFET, because NFET has a larger g_m [47]. Combined with the first stage, these two stages can be regarded as an operational transconductance amplifier.

E.4 Third Stage

The main function of the third stage is to boost the voltage gain. In this design, a PMOS transistor T21 is used as a current source load to supply drain current, the input signal of T22 comes from the gates of T19 and T20 in the second stage. Figure E.6 shows the third stage circuit of the amplifier. The voltage gain of this stage can be written as:

$$A_v = -g_m(r_{o21} \parallel r_{o22}) \tag{E.13}$$

Where r_{o21} and r_{o22} are the equivalent resistances of T21 and T22.

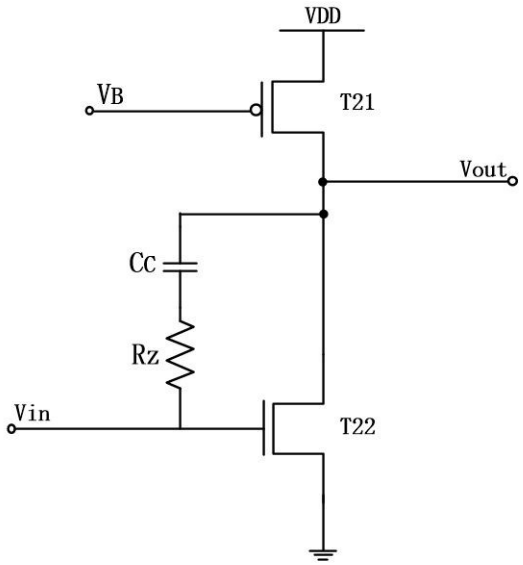

Figure E. 6 Third amplification stage of the amplifier

Below is the transistor size table of the amplifier:

#	**Width (m)**	**Length (m)**
T1, T7, T11, T45, T46	500n	400n
T3	2u	400n
T12, T13, T14, T15	2.7u	400n
T4, T5	3u	400n
T6	1.5u	400n
T16	800n	400n
T17, T18	15u	400n
T8, T9, T19, T20,	3u	400n
T21	3.5u	400n
T22	23u	400n

Table 16 Transistor sizes of the amplifier