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A STUDY OF A
CORRELATED DOUBLE SAMPLING SWITCHED-CAPACITOR FILTER

by

© Kwai-Kwong Kirby Lam, B.Eng.

Submitted to the
Faculty of Graduate Studies and Research
in partial fulfillment of the requirements
for the degree of
Master of Engineering

Department of Electronics
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Carleton University

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ABSTRACT

In this thesis, a method of reducing the $1/f$ noise in SC networks using an initializing technique is described. The novel technique performs correlated double sampling and thereby removes the input-referred offset of the operational amplifier. This gives an offset-free SC building block - a CDS integrator. The use of this integrator in first-order and second-order filters is studied analytically. Experimental results are presented and the effect of the initializing technique in $1/f$ noise reduction is observed. In addition, a new clock feedthrough cancellation circuit [36] is tested and found to be effective. Finally, an offset-free biquad providing continuous output, unlike that from the CDS-based biquads, is developed. This two-integrator state-variable biquad employs a CDS integrator and a conventional integrator to form the two-integrator loop. Although its noise performance is not as good as those of the novel biquads composed of the CDS integrators, it is better than that of the conventional biquad.

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TABLE OF CONTENTS

	PAGE
CHAPTER 1 INTRODUCTION	1
1.1 Subject of thesis	1
1.2 Historical background of switched-capacitor (SC) filters	2
1.3 Historical background of correlated double sampling (CDS) concept	7
1.4 The basic SC integrator and its CDS equivalent	13
1.4.1 The basic SC integrators	13
1.4.2 The CDS SC integrator	17
1.5 Thesis format	22
CHAPTER 2 REVIEW OF NONIDEALITIES, NOISE AND NOISE REDUCTION TECHNIQUES IN SC FILTERS	24
2.0 Introduction	24
2.1 Nonidealities and their effects in switched-capacitor filters	25
2.1.1 Finite op amp gain and bandwidth	25
2.1.2 Parasitic capacitances inherent in MOS devices	28
2.1.3 Finite on-resistance of the MOS switch	30
2.1.4 Output offset error	31
2.2 Noise sources in switched-capacitor filters	35
2.2.1 KTC switch noise	35
2.2.2 Operational amplifier broadband noise	36
2.2.3 Operational amplifier 1/f noise	38
2.3 Techniques for 1/f noise reduction in SC filters	38
2.3.1 Principle of chopper-stabilization technique	41
2.3.2 Principle of correlated-double-sampling technique	41
2.4 Summary	43
CHAPTER 3 DETAILED ANALYSIS OF CDS FILTERS	45
3.0 Introduction	45
3.1 Parasitic-free CDS integrator	45
3.2 Analysis of first-order lowpass filters	48
3.2.1 Sampled-data analysis of first-order filters	50
3.2.2 Exact analysis of first-order filters	57

3.2.3	Analysis of clock feedthrough in a novel first-order filter	67
3.3	Analysis of state-variable biquads	72
3.3.1	Sampled-data analysis of second-order bandpass filters	76
3.3.2	Exact analysis of second-order bandpass filters	83
CHAPTER 4	EXPERIMENTAL RESULTS	88
4.0	Introduction	88
4.1	Description of the test chip	88
4.2	Performance of the lowpass filters	90
4.2.1	Signal response of lowpass filters	93
4.2.2	Noise performance of lowpass filters	102
4.3	Performance of the bandpass biquads	111
4.3.1	Signal response of bandpass biquads	114
4.3.2	Noise performance of bandpass biquads	117
4.4	Summary	119
CHAPTER 5	DISCUSSION AND CONCLUSION	122
5.1	Discussion	122
5.2	Proposal for an improved biquad	125
5.3	Conclusions	133
REFERENCES		134
APPENDIX A	DERIVATIONS OF INTEGRATOR TRANSFER FUNCTION WITH OP AMP GAIN	138
APPENDIX B	AN EXAMPLE OF EXACT ANALYSIS METHOD	141
APPENDIX C	ANALYSIS OF A GENERAL STATE-VARIABLE BIQUAD	149

LIST OF SYMBOLS AND ABBREVIATIONS

A	Effective gain of the composite amplifier
A _o	Open-loop gain of an operational amplifier
a _C	Switched capacitor resistor
a, a _{c5}	Constants representing capacitor ratios
a _j th	capacitor ratio
a _p	Parasitic capacitor ratio
act.	Actual
BP	Bandpass
C	Capacitor
C _I	Initializing capacitor
C _R	Switched capacitor resistor
C _{Rj} th	switched capacitor resistor
C _i	Integrating capacitor
C _j th	capacitor
C _{pj} th	parasitic capacitor
C _s	Sampling capacitor
C _{sf}	Stray feedback capacitor due to a layout error
CCD	Charge coupled device

CDS	Correlated double sampling
conv.	Conventional
$D(s)$	Denominator of a s-domain transfer function
$D(z)$	Denominator of a z-domain transfer function
$d(t)$	Deviation function
$e_{exp}()$	Exponential function
F_k	Switching matrix for switched state k
f_c	Corner frequency or break point of the 1/f noise
f_s	Sampling frequency
G	Gain of an active circuit
G_k	Feedthrough matrix for switched state k
G'	Actual gain
G^*	Gain error
HP	Highpass
Hz	Hertz
$H(s)$	s-domain transfer function
$H(z)$	z-domain transfer function
$H_{BP}(z)$	Signal transfer function of a bandpass biquad
$H^*(z)$	Complex conjugate of $H(z)$
$H_n(s)$	s-domain noise transfer function
$H_n(z)$	z-domain noise transfer function
$H_s(z)$	z-domain signal transfer function

$H_{0,0}, H_{0,1}, \dots$ Transfer function matrices

I Identity matrix

IC Integrated circuit

id. Ideal

inv. inverting

KT Thermal constant

KT/C Nyquist noise or thermal noise

kHz Kilohertz

L Inductor

LDI Lossless digital integrator

LSI Large scale integration

MHz Megahertz

MOS Metal oxide semiconductor

MOST Metal oxide semiconductor transistor

noninv. Noninverting

OA_j^{th} operational amplifier

op amp Operational amplifier

PCM Pulse-code modulation

PSR Power supply rejection

* Pole error

p' Actual pole

Q_j^{th} switch or transistor

R Resistor

RC Networks composed of resistors and capacitors

RLC Networks composed of resistors, inductors and capacitors

R_j	j^{th} resistor
rms	Root mean square value
S/H	Sample-and-hold
$s, j\omega$	Frequency representation in an s-domain analysis
s_p	s-plane pole
T, T_o	Sampling period
$T(W)$	Closed-form transfer function matrix
t_k	Switching instant of switched state k
VLSI	Very large scale integration
V_R, V_C	Reference voltages
V_{cj}	Voltage across j^{th} capacitor
V_i	Signal input
$V_i(t)$	Continuous signal input
$V_i^{SD}(t)$	A pure sampled-data signal input
V_j	Output of j^{th} operational amplifier
$V_j/V_{j,i}$	Transfer function of j^{th} operational amplifier to signal input
$V_j/V_{j,nj}$	Transfer function of j^{th} operational amplifier to noise voltage
V_n	Input-referred noise voltage of an op amp
$V_{n_{eq}}$	Equivalent input-referred noise voltage

V_{nj}	Input-referred noise voltage of j^{th} op amp
V_o	Output voltage
V_o/V_i	Signal transfer function
$V_o/V_n, V_{out}/V_n$	Noise transfer function
V_{os}	DC amplifier input-referred offset
V_{SS}	Substrate potential or lower rail voltage supply
V'	Potential of the integrating node of the composite amplifier
ω	Frequency in radian
ω_o	Bandwidth of an operation amplifier
z	$\exp(j\omega t)$
z^{-1}	z -transform of unit delay
$z_{act.}$	Actual pole location in z -plane
$z_{id.}$	Ideal pole location in z -plane
z_p	z -plane pole
$(1 - z^{-1/2})$	Mathematical representation of CDS filtering action
$1/f$	Flicker noise of an op amp
k, m	Indices of summations
Δ_k	Duration of a switched state k
ϕ_1, ϕ_2	2-phase nonoverlapping clock pulses
ϕ_T	Transfer clock pulse
ϕ_C	Clamping clock pulse

-1
[] Inverse of a matrix
| | Magnitude
 Σ Summation
 τ Time separating the two sampling intervals for CDS process
% Percent

CHAPTER 1

INTRODUCTION

1.1 SUBJECT OF THESIS

Switched-capacitor (SC) filter techniques [1,2] have gained widespread use in recent years. Different SC topologies consisting of switched capacitors, capacitors and operational amplifiers (op amps) have been reported to realize active-RC circuits and filters [3-6]. Compounded with the tremendous growth experienced in MOS LSI technology, the use of switched-capacitor techniques allowed higher degrees of integration of a variety of analog signal processing circuits, such as speech synthesizer, audio, and PCM filters [7-11]. Recently, performance improvements for SC filter circuits are being sought (e.g. [12]).

Internal noise sources, such as thermal noise in MOS switches and the broadband noise and $1/f$ noise from op amps, set a limitation to the dynamic range of SC filters. In voiceband filtering applications, the $1/f$ noise of the op amp is dominant [12]. This thesis aims at performing experimental and analytic studies on a particular SC filter topology, which uses an initializing technique to implement correlated double sampling as a means of reducing the $1/f$ noise. Work is carried out on first-order SC lowpass filters and SC bandpass biquads, which use the novel topology as the basic building block. Nonideal circuit behaviour caused by finite op amp gain, capacitive feedthrough and noise sources in SC filters are also studied to gain a better understanding of how such behaviours affect the performance of

these filters.

1.2 HISTORICAL BACKGROUND OF SWITCHED-CAPACITOR (SC) FILTERS

Precision filters for frequency selective filtering are one of the most common circuits in telecommunications and other voiceband systems. The fundamental motivation for the development of SC filters is the long-term desire to fully integrate these filters without costly trimming on a small silicon chip.

Up to the latter 1960s, passive-RLC filters, composed of discrete resistors (R), inductors (L) and capacitors (C), were mainly used. However, inductors become large and costly for high-quality filters. Thin-film hybrid integrated circuitry with deposited RC components and discrete transistors were later developed. Not only were the size and cost reduced relatively, but also filtering and amplification were achieved simultaneously. Resistors for precision filters can be trimmed at the price of higher manufacturing cost.

Concurrently, integrated technology has continued to advance. In the mid-1960s, the introduction of the first IC (integrated circuit) op amp has created a revolution in electronics because of its performance, cost and versatility. Subsequently, it has been recognized that monolithic integrated active filters can offer the advantages of low-cost, microminiature filters with gain, essential to any electronic system integrated on a silicon chip.

There are four types of monolithic integrated analog filters [4]: classical active-RC filters, charge coupled device (CCD) filters, direct form recursive filters [13,14] and active-SC filters. They all can be integrated using MOS technology and take advantage of the technology's unique properties: superior logic density due to self-isolating transistor structures and the ability to store, sense and move charges (signal) on capacitors.

The tolerance and temperature coefficient of integrated resistors, which do not track with those of capacitors on the same chip [15], result in poorly controlled RC products and pole positions. Moreover, resistors occupy large area. These facts in turn detract from their use in monolithic active-RC filters. In contrast, high-quality capacitors and switches [15] can be fabricated using MOS technology. In addition, MOS op amps are practical which are 3-5 times smaller than their bipolar counterparts.

The CCD filters, direct form recursive filters and SC filters are sampled-data analog filters, and thus are subjected to Nyquist's criterion. The sampling rate must be at least twice the highest frequency component of the input signal to avoid aliasing effect (i.e., signal contamination).

The CCD filters, having only zeros in their transfer functions, were introduced in the early 1970s. Their use was not very favourable for two reasons: 1) The low sampling rate relative to the passband frequencies in order to minimize the number of CCD stages (i.e., to save chip area) requires a

relatively complex anti-aliasing filter [4], and 2) large insertion loss limits the available dynamic range [2]. However the CCD filters are effective in implementing transversal filter structures for matched and adaptive filters [4]. Since CCD filters are nonrecursive, a very long CCD filter utilizing large chip area is required to realize highly selective filters with long impulse response. Direct form recursive filters are a solution to this problem. However these filters suffer from a relatively high sensitivity to the values of filter coefficients which increases as the sampling frequency is raised to ease the design of the anti-aliasing filter [4]. The recursive SC filters overcome the problems associated with the other filters while the advantages of monolithic filters are preserved. The introduction of SC filters has created a new era in analog signal processing and integrated circuit techniques. Combinations of analog and digital circuits can be integrated on a single IC using MOS technology.

The idea of switched capacitors was demonstrated by Fried [16] in 1972. At that time it was overlooked, partially because of the heavy emphasis on research of CCD filters. In 1977, the idea used in active-SC filters was reintroduced simultaneously in [1] and [2]. The basic concept of switched-capacitor techniques, as illustrated in Fig. 1.1, is to replace resistors by periodically switched capacitors which transfer charges to approximately simulate the flow of current in resistors. The MOS implementation of a SC resistor having effective resistance T/C is shown in Fig. 1.1(c). The approximation of a resistor can be

I —

(a)

$$I = \frac{V_1 - V_2}{R}$$

(b)

$$I = \frac{C_R(V_1 - V_2)}{T}$$

$$\therefore R = T/C_R$$

(c)

(d)

Fig. 1.1(a) and (b). Simulation of a resistor by a switched-capacitor resistor.

(c) The MOS implementation of the SC resistor shown in (b).
 (d) Clock waveforms.

quite accurate if the sampling rate is much higher than the highest signal frequency of interest. However, the precise characteristics of active-SC filters must be obtained from the z-transform analysis to account for the effects of discrete-time sampling and charge sharing. The beauty of these filters is that the sensitivity of their response decreases with increasing sampling rate, in contrast to the other analog sampled-data filters [2]. Thus a simple second-order active-RC filter can be used as the anti-aliasing filter [10]. Also the increase in silicon area which is required to accommodate the higher sampling rate is relatively small for SC filters but large for CCD filters [4].

The most important characteristic of active-SC filters is that accurate RC time constants are determined by a stable sampling rate and well-controlled capacitor ratios ($< 0.1\%$ [15]), not the absolute capacitances. Also the frequency response depends only on capacitor ratios which are mostly independent of temperature, voltage and process variations. Hence, small-area capacitors can be used in the design. In general, an active-SC filter can be designed to occupy relatively little silicon area. The success of these filters also lies in their sensitivity properties, closely resembling those of continuous-time filters (for example, doubly terminated RLC ladder filters). As well, the established continuous-time filter design knowledge can be carried over largely to SC filters.

1.3 HISTORICAL BACKGROUND OF CORRELATED DOUBLE SAMPLING (CDS) CONCEPT

The concept of correlated double sampling (CDS), which is adopted by the novel SC filter topology under investigation in this thesis, is not new. It has been used in CCD circuits and filters. The CDS concept was first developed by Westinghouse engineers and introduced in 1974 [17]. In [17], a unique output circuit was built to provide low-noise analog signal processing for CCD line imagers. This output circuit, using the correlated-double-sampling technique, removes the Nyquist noise (i.e., KT/C noise) of the reset switch, eliminates switching transients, and removes low frequency noise such as $1/f$ noise of amplifiers. In addition to the noise sources within the CCD arrays, these noise components also appear at the output of typical CCD output circuits. In particular, the Nyquist noise [18] is a major component among the added noises. Schematic diagrams of a typical CCD output circuit [18] and the one introduced in [17] are shown in Fig. 1.2 and Fig. 1.3 respectively for comparison. The timing diagram for the CDS circuit is given in Fig. 1.3(b). Four distinct timing intervals are required to complete the CDS process [17]. They are labelled for the following discussion.

- 1) **RESET:** Prior to each signal charge transfer, the previous charge packet is discharged by closing the NMOS reset switch, thereby reestablishing the reference voltage V_R across the capacitor C_s and again introducing reset noise including the

Fig. 1.2 A typical CCD output circuit.

Fig. 1.3 (a) Schematic diagram of a CDS output circuit for CCD line imagers.
 (b) Timing diagram with four distinct timing intervals specified.

Nyquist noise and V_R power supply noise to the capacitor. At

the start of the reset interval, the signal charge is also transferred to the last well next to the transfer switch and the collecting diode.

- 2) READ RESET: After the reset switch is opened and before the transfer switch is closed, clamp switch 1 is closed. When it is opened, one side of the clamp capacitor, C_1 , stores the

reset noise and the instantaneous noise sample of the electrometer amplifier and the preamplifier, while the other side is clamped to a reference voltage V_C . For simplicity,

the reference voltage V_C can be thought of as at ground

potential. Then the voltage across C_1 is the instantaneous noise sample and the reset noise.

- 3) SIGNAL TRANSFER: At the start of this interval, ϕ_2 goes high and ϕ_T goes low to transfer the signal charge packet to the

collecting diode. The output voltage of the preamplifier is the signal plus reset noise plus the time varying noise of the electrometer amplifier and the preamplifier. However the output voltage of the buffer amplifier at the end of ϕ_T equals

circuit gain times the sum of the signal plus the amplifier noise difference at the end of ϕ_T and ϕ_C respectively (i.e.,

time-varying amplifier noise is subtracted from the amplifier noise sample). The reset noise is removed at the output of

the buffer amplifier. This is because of the subtraction process introduced by the clamp capacitor C and the fully-correlated reset noise at the two intervals.

- 4) READ SIGNAL: After the transfer switch goes off, the amplified output of the buffer amplifier is sampled and held for subsequent processing by the closure of sample switch 2.

The noise transfer function of this output circuit, which applies to any time-varying components of noise between clamp and sample intervals, may be written as [17];

$$H_n(s) = G \frac{(1 - e^{-s\tau})}{1 + \frac{s}{W_o}} \quad (1-1)$$

where G is the gain, τ is the time separating the two intervals, and W_o is the bandwidth of the preamplifier. The general frequency response for a value of $\tau = T/2$ is given in Fig. 1.4 where T is the clock period (i.e., the duration of the four intervals).

The CDS technique has several important advantages beside removing the Nyquist noise and low-frequency noise arising from power supplies (e.g. V_R). It also reduces 1/f noise of the first two amplifiers (see Figs. 1.3 and 1.4) since the output consists of the difference of low-frequency amplifier noise samples taken within a short time. Lastly, switching transients are avoided by sampling the output after the transients have damped out.

Fig. 1.4 Frequency response of a CDS output circuit with $\tau = T/2$.

However, C_1 and C_2 are subjected to noise in the clamp and sample switches and must be large enough to avoid introducing additional noise components.

1.4 THE BASIC SC INTEGRATOR AND ITS CDS EQUIVALENT

The basic building block of SC filters is the active-SC integrator which will be described below. With extra circuit elements, capacitors and/or switches, this integrator forms the basis of different types of first-order filters. With the addition of another integrator to form a two-integrator loop, a state-variable biquad is then realized [1,2,5]. Higher order filters can be synthesized by cascading a number of biquads and/or a first-order filter together, depending on the required order count. In addition, there are more complex topologies using this integrator such as ladder filters [4].

1.4.1 THE BASIC SC INTEGRATORS

An active-RC integrator is shown in Fig. 1.5(a), and its SC equivalents are included below. The integrator in Fig. 1.5(b) incorporates the so-called parallel SC resistor, which is the circuit shown inside the dashed box, while the one in Fig. 1.5(c) uses the series SC resistor. These integrators do not exactly simulate the RC integrator because of imperfect mapping from the continuous frequency (s) domain to the sampled-data (z) domain [3]. This leads to deviations in filter characteristics obtained

Fig. 1.5 (a) An active-RC integrator.
 (b) A SC integrator with the parallel SC resistor.
 (c) A SC integrator with the series SC resistor.
 (d) A SC integrator with the bilinear SC resistor.

4

from the s-domain analysis. These deviations become worse when the ratio of sampling frequency to signal frequency becomes small. Thus z-transform analysis must be used to design SC filters. An integrator providing a more ideal mapping from the s-domain to the z-domain and thus simulating the RC integrator closely is given in Fig. 1.5(d). It incorporates the bilinear SC resistor [19]. However, all these sampled-data integrators are sensitive to the parasitic capacitance C_{p1} (shown in Fig. 1.5) inherent in

MOS switches and capacitors. This capacitor periodically absorbs charge from the input source and transfers charge to the integrating capacitor C . The corresponding transfer functions are included in the figure. The notation of capacitor size (aC) in Fig. 1.5, which will be extensively used in chapter 3, is defined as follows. The constant, a , is a capacitor ratio which is obtained with respect to the integrating capacitor, C . In other words, the size of the input capacitor is " a " times that of the integrating capacitor, C .

The switched capacitor filters in use today are made insensitive to parasitic capacitances in order to avoid distortions. The parasitic-free inverting and noninverting integrators [5] are shown in Fig. 1.6. C_{p1} is still present; however, it is switched between ground and virtual ground (assuming infinite op amp gain) giving no charge transfer. Another parasitic capacitance, C_{p2} , is alternatively switched between the input voltage and ground so it does not affect the operation of the circuit. These circuit building blocks are often used together in the design of

Fig. 1.6(a) Parasitic-free inverting SC integrator with noninverting SC resistor.
 (b) Parasitic-free noninverting SC integrator with inverting SC resistor.
 (c) Parasitic-free bilinear SC integrator.

parasitic-free state-variable biquads and SC ladder filters [20] employing LDI (lossless digital integrator) timing [4], which allows the filters to closely approximate the continuous equivalents. Also a parasitic-free bilinear SC integrator was reported [21] based on the integrator of Fig. 1.6(a). Its circuit diagram is shown in Fig. 1.6(c). The z-domain transfer functions are given in Fig. 1.6 for each integrator under the assumption that the output is sampled during the same interval as the sampled-data input changes. A parasitic-free building block is a very important design consideration as it allows precise capacitor values to be known in order to meet frequency specifications.

1.4.2 THE CDS SC INTEGRATOR

The initializing technique, which is particular to this thesis, is suitable for switched-capacitor (SC) integrator-based filters discussed in the previous section. The technique is demonstrated with an inverting integrator as shown in Fig. 1.7. A noninverting counterpart can be obtained by interchanging the clock signals of the two input switches. This complementary pair is named after the CDS concept implemented by the initializing technique (i.e., inverting and noninverting CDS integrators) and is also parasitic-free. This property is verified in section 3.1.

Assume that a conventional two-phase nonoverlapping clock is used. The basic principle used is to initialize the operational amplifier. That is, its output is shorted back to the inverting input terminal on one phase, thereby storing a sample of the op

Fig. 1.7 An inverting CDS SC integrator and the clock waveform.

amp noise on a capacitor at the amplifier input. C_I is the initializing capacitor, and is chosen to be large relative to the input capacitance of the op amp. Large C_I is used to suppress clock feedthrough noise from the switch Q_5 . The symbol V_n in Fig. 1.7 represents the noise sources of the op amp, including the amplifier input referred offset as it is a special case of low-frequency noise.

The act of initialization occurs during the initializing phase (ϕ_1) by the closure of switch Q_5 . The amplifier output is thus set to an initializing level near analog ground. The value of this level depends on internal amplifier noise, power supply noise, and input offset voltage. During the same interval, capacitor C_2 is discharged through Q_2 and Q_3 while the node labelled A, a virtual ground node, is connected to analog ground by transistor Q_3 . This stores the value of V_n across C_I at the instant ϕ_1 -controlled switches open.

The purpose of the initializing capacitor C_I becomes obvious on the active phase (ϕ_2). During the time that ϕ_2 -controlled switches are closed, node A will only see, through C_I , the difference between the instantaneous value of the noise voltage (V_n) and the noise that was previously sampled at the end of ϕ_1 .

Thus the noise contribution of V_n to the amplifier output is just the noise level difference and is represented by a $(1-z)^{-1/2}$ term in the z-domain transfer function (V_o/V_n). Therefore the novel topology shows the CDS filtering action as discussed in section 1.3. The value of the exponent is $1/2$ because a half period delay is generated from the end of ϕ_1 to that of ϕ_2 . Since the energy of $1/f$ noise is concentrated in the low frequency range and since the CDS technique provides a highpass filtering action, the noise component at the output will be much reduced. This result also applies to the low-frequency power supply noise. In addition, an input offset-free amplifier is obtained (assuming infinite gain) because the DC component of the voltage at node A, the integrating node, is zero after transients are completed. The op amp and the initializing capacitor can now be thought of as an input offset-free "composite amplifier" as seen from node A in Fig. 1.7. Any input charge introduced to the integrating node by switched capacitor C_2 will be passed to the integrating capacitor C_1 , except for the effect of the $(1-z)^{-1/2}$ term. The output of the amplifier will therefore reflect the same accuracy.

Fig. 1.8 shows the output waveforms of the CDS integrator and a conventional SC filter. Since the waveform of the CDS circuit must alternate between the initializing level (on ϕ_1) and the output voltage (on ϕ_2) in every clock period, the op amp used in this circuit must have the capability to slew and be able to

Fig. 1.8(a) Output waveform of the CDS SC integrator.
 (b) Output waveform of a conventional SC filter.

settle quickly to the final voltage. These requirements complicate the op amp design and the op amp may be larger in size and consumes more power. On the other hand, the conventional waveform in Fig. 1.8(b) is a 100% sample-and-hold (S/H) type. The op amp needs to respond only once every clock period to smaller output shifts. Therefore the slew rate requirement is less demanding. Hence the op amp requirement is less stringent.

1.5 THESIS FORMAT

This thesis is composed of five chapters. Chapter 1 presents the historical background of SC filter circuits. The concept of SC filtering techniques and the state-of-the-art are described. The CDS technique in CCD technology is reviewed. The principle of the initializing technique is introduced with the CDS SC integrator.

Chapter 2 gives a review of nonidealities associated with circuit elements of SC filters and their effects on the performance of the filters. This provides the background for the discussion in chapter 3 and chapter 4. Noise sources in SC filters are described and competing techniques for $1/f$ noise reduction are discussed.

Chapter 3 introduces the design of first-order lowpass filters and biquads using the CDS integrator. A clock feedthrough cancellation circuit for these filters is proposed. Analytic results of these filters using both z -transform analysis and an

exact analysis are given.

Chapter 4 presents the experimental results of the first-order lowpass filters and bandpass biquads. Discrepancies in filter characteristics are discussed. Finally, this thesis is concluded by chapter 5 in which a discussion and a conclusion are given.

CHAPTER 2

REVIEW OF NONIDEALITIES, NOISE AND NOISE REDUCTION TECHNIQUES IN SC FILTERS

2.0 INTRODUCTION

Numerous advantages provided by SC techniques in filtering applications were discussed in the last chapter without considering the practical limitations of MOS op amps, parasitic capacitances associated with MOS switches and capacitors, and other nonidealities. The nonidealities affect the performance of SC filters in various ways. The key problems created are limited dynamic range and degraded power supply rejection. Although different topologies have been designed within the constraints set by MOS technology, these effects continue to be stumbling blocks for the further development and improvement of SC techniques.

This chapter gives a review of nonideal aspects of SC filter design and focuses on the effects of nonideal circuit behaviour in SC filter circuits. It should be emphasised that unless a better understanding of these effects is obtained, the ability to extend SC filtering techniques to high frequency applications, for instance, will be restricted. In addition, it will not be possible to take advantage of the technological ability to scale or reduce feature size in VLSI integrations.

This chapter consists of three main sections. Section 2.1 deals with nonideal properties of the SC filter components and their effects. Section 2.2 discusses noise sources in SC filters.

Circuit techniques to remove the dominant noise source (i.e., $1/f$ noise) are described in section 2.3.

2.1 NONIDEALITIES AND THEIR EFFECTS IN SWITCHED-CAPACITOR FILTERS

Each nonideality and its effects are studied separately in this section. Discussions start by considering band-limited finite-gain op amps, and continue with parasitic capacitances, switch on-resistance and output offset errors, respectively.

2.1.1 FINITE OP AMP GAIN AND BANDWIDTH

The performance of active-SC networks is strongly related to the op amp performance limitations. Yet the SC design methods in use today often assume that the op amp is ideal. There are mainly four limitations in an op amp which need to be considered, namely the settling time, slew rate, unity-gain bandwidth and open-loop gain. The first three limitations, which are somewhat related [22], require consideration usually in high frequency applications [23]. Their effects can be suppressed by having a faster and wider bandwidth op amp. On the other hand, finite op amp gain should be considered for all applications and its effects can be neglected if a very high gain op amp is used. Since the limitations interact with each other [22], the design for such high quality (i.e., high-frequency, high-gain) op amps becomes complex and the amplifier often occupies large chip area.

The major effects caused by nonideal op amps, finite gain and

bandwidth in particular, are magnitude and phase errors [24,25]. These errors in turn result in passband droop, deviations in pole frequency and in Q factor as in state-variable biquads [25]. The effect of finite-gain amplifier on parasitic-free inverting and noninverting integrators described in section 1.4.1 is discussed in the following text.

The circuit diagrams of the integrators are reproduced in Fig. 2.1 for convenience. If the op amp gain is finite, the virtual-ground assumption at the inverting input terminal is violated. The resultant nodal voltage is $-V_o/A_o$, as shown in the figure, where A_o is the open-loop gain of the op amp. As a result, a residual charge (i.e., $aC \times V_o/A_o$) remains in the input SC resistor, aC , for every charge transfer. Furthermore, the integrators are no longer parasitic-free because the parasitic capacitance aC_p can affect the circuit operations. It should be noted that this parasitic was neglected in both [24] and [25]. The effects of the finite-gain amplifier and the parasitic capacitance on the integrators are analyzed using the z-transform in Appendix A. The respective transfer functions ($H(z)$) of the inverting and noninverting integrators can be expressed in the following forms:

$$H(z) \Big|_{\text{inv.}} = \frac{-a(1-\text{gain error})}{1-(1-\text{pole error})z^{-1}} \quad (2-1)$$

$$H(z) \Big|_{\text{noninv.}} = \frac{a(1-\text{gain error})z^{-1}}{1-(1-\text{pole error})z^{-1}} \quad (2-2)$$

Fig. 2.1(a) "Parasitic-free" inverting integrator.
 (b) "Parasitic-free" noninverting integrator.
 (c) Pole locations.

where

$$\text{gain error} = \frac{(1+a+a_p)}{A_o + (1+a+a_p)}$$

$$\text{pole error} = \frac{a+a_p}{A_o}$$

The gain and pole errors are the same for the two integrators.

With the ideal op amp, each integrator has a pole at $z=1$. However, the effect of a finite-gain amplifier results in a lossy integrator as if there is a feedback SC resistor. The pole of the integrator deviates from $z=1$ towards the origin of the z -plane, as shown in Fig. 2.1(c). In addition, the finite-gain amplifier causes a gain error as if there is a capacitor ratio error. Although one can predistort the capacitor ratio to compensate for the error, this is not desirable because the filter design is complicated and the parasitic capacitance [4] is nonlinear.

2.1.2 PARASITIC CAPACITANCES INHERENT IN MOS DEVICES

The presence of parasitic elements in MOS capacitors and switches [4] has created some problems and set a limitation on SC filter techniques. For instance, parasitic capacitances associated with these circuit elements have caused transfer-function inaccuracy, clock feedthrough and power supply noise coupling. The effects of parasitic capacitances to substrate (or ground) are

discussed in this subsection.

This parasitic element is usually dominated by the p-n junction capacitances of a switch. Although the bottom-plate parasitic capacitance of a MOS capacitance is the largest [4], it is often connected to ground or switched between the low-impedance points in SC realizations such that it has no effect on the circuit operation. The junction capacitances become especially important in nonparasitic-free SC realizations. For example, the transfer function for a parallel SC resistor integrator of Fig. 1.5(b) is

$$\frac{V_o}{V_i}(z) = \frac{\frac{C_{pl}}{-(a + \frac{C_{pl}}{C})z^{-1}}}{1 - z^{-1}} \quad (2-3)$$

The junction capacitance C_{pl} appears in parallel with the input SC resistor (aC). It results in an inaccurate RC time constant and capacitor ratio error. Note that the problem cannot be corrected by predistortion due to the nonlinear characteristic of C_{pl} [4]. Moreover, the capacitance forces the integrator to have a large integrating capacitor in order to suppress its effects, and thus large chip area is required. Fortunately, the effects of parasitic capacitances between any node to ground have been eliminated by the use of parasitic-free integrators of Fig. 1.6. However, these parasitics cause degradation of power supply rejection (PSR), even in parasitic-free structures. They allow

power supply variations to couple into the integrating node and, generally, into all signal paths [26]. The degradation is more severe on the negative power supply voltage (V_{ss}), because the parasitic capacitances are connected to V_{ss} . A noisy V_{ss} couples noise directly to all circuit elements on a chip. The PSR has been improved by using minimum geometry switches and by shielding the integrating node [26]. Recently, an improved approach suggests the use of fully differential SC integrators [12,23]. This approach takes advantage of the very high common-mode rejection ratio of the op amp and of the balanced configuration to suppress the power supply coupling.

2.1.3 FINITE ON-RESISTANCE OF THE MOS SWITCH

Since the on-resistance of a switch is finite, the time constant in the charging or sampling process of the switched capacitors becomes finite. This time constant may be comparable to the duration of the charging phase. Basically, the capacitor voltage is an exponential function of the time constant. In order to ensure the capacitor is fully charged, the duration must be long enough. Hence the maximum sampling rate is set [1]. Furthermore, the size of switched capacitors with respect to that of switches is restricted because (i) large capacitors may cause incomplete charge transfer while (ii) small capacitors enhance the thermal noise of the switches (section 2.2.1). In particular, for very high frequency applications, the effects of the non-zero on-resistance should be considered since less charging time is available. Incomplete charge transfer can be avoided by

increasing the width-to-length ratio of switches, because the on-resistance is decreased, which in turn reduces the time constant.

2.1.4 OUTPUT OFFSET ERROR

A SC network's dynamic range is reduced by its output offset voltage, which is primarily due to three sources of errors [27]: p-n junction leakage current in MOS switches, clock feedthrough in switches, and input-referred DC offset voltage of operational amplifiers. Among these sources, clock feedthrough induced error is the most significant, and has received attention recently [28,29]. In applications where the output offset voltage is critical, methods for offset cancellation must be used. In the following text, these error sources are discussed.

When the input to a SC filter is zero, the leakage current [4] through the p-n junction of the switch at the amplifier input causes a periodic sawtooth waveform [3] at the amplifier output, between sampling instants. If the sampling rate is too low, the amplifier may become saturated. The minimum sampling rate of SC networks is thus set. However, since the sampling rate is usually high in order to simplify aliasing filter design, the low voltage drift is negligible [3].

In many analog applications where low level signals are processed, the amplifier input-referred offset [22] is still too high despite improvements in MOS process control [15] and in op

amp design [22]. Although the DC offset voltage does not affect the signal transfer function, the circuit dynamic range is reduced. The presence of offset voltage at the output may cause distortion by asymmetrical clipping at high signal levels. The effects get worse in a high closed-loop gain circuit since the offset voltage is amplified. The op amp may saturate immediately. Several sampled-data circuit techniques have been used to eliminate the amplifier input offset [27,28]. The basic principle is to sample and hold the offset voltage on coupling capacitors on one phase, and then to subtract from the incoming signal and offset voltage on the next phase. The initializing technique proposed in this thesis is similar to the previous techniques, although the goal is to form an input offset-free composite amplifier during the active phase.

As the effect of leakage current on the output offset voltage is normally negligible and input offset-free SC networks are achievable, clock feedthrough becomes the sole error source. Often clock feedthrough causes output offset error in input offset-free SC networks. Clock feedthrough, which is a general term for clock related noise, is a complex and significant effect. It is caused by capacitive couplings of gate-source and gate-drain overlap capacitances [4] in a switch. It also includes the effects of charge release from the channel of a MOST when the switch turns off [28] and of charge pulling onto the channel when it turns on [30]. Clock feedthrough appears as sharp steps at circuit nodes. The step height is approximately equal to the product of clock pulse height and the ratio of the overlap

capacitance to the load capacitance at the common node [1]. This relationship does not include the effects of charge release or charge pulling. When a switch turns off, the proportion of channel charge injected into the drain and source diffusions respectively (i.e., the circuit nodes) is a complex function of the clock pulse fall time and impedances connected to the two diffusions [28]. Similarly, when a switch turns on, it may pull charge away from its neighboring capacitors to form its own channel [30]. The effect of clock feedthrough is dependent on the locations of the switches in a SC structure. If a circuit node is switched on and off to low-impedance nodes such as an input voltage source, op amp output or analog ground, clock feedthrough will cause no offset error other than short glitches. This is because the overlap capacitances will be quickly charged up or discharged by these low-impedance nodes which also act as either sources or sinks to channel charge [31]. In contrast, clock feedthrough must be considered if the circuit node is switched on and off to the integrating node of an active-SC filter [31], because any transient at the integrating node introduced by the switching will appear at the output. In other words, clock feedthrough due to the switches adjacent to the inverting input of the op amp has the largest effect on the output offset error.

There are several approaches for reducing the effect of clock feedthrough. The obvious solutions are to use self-aligned MOS technology and to use small switches. Also, in SC filter circuits, the size of all capacitors can be increased to swamp out the effect of clock feedthrough. However the tradeoff among

speed, area and clock feedthrough should be considered. Charge-cancelling circuit techniques have been discussed extensively in [28]. The basic principle is to put a dummy switch adjacent to the main switch. These switches are controlled by a clock pulse and its inverse respectively. The capacitive coupling from the main switch is thus approximately cancelled by that from the dummy switch. The proportion of charge release, discussed above, is further controlled by a dummy capacitor [28].

The overlap capacitances of the input transistor at the inverting input terminal of the op amp degrade power supply rejection (PSR) [8,26]. Variations of power supplies biasing the op amp cause a displacement current into or out of the integrating node through the overlap capacitances of the input transistor, and thus change the amplifier output [8]. The PSR can be improved by using small input transistors for the input stage of an op amp [26], although this will increase the $1/f$ noise of the op amp (section 2.2.3).

Finally, it should be remarked that clock noise can be directly coupled into the integrating node by the overlap capacitance when the switch adjacent to the node is turned on [8]. The noise can be transient noise (overshoot and ringing) due to switching in the clock waveform generator and is particularly important in high frequency filters. In addition, any power supply noise which is transmitted via the clock levels themselves will feedthrough to the integrating node.

2.2 NOISE SOURCES IN SWITCHED-CAPACITOR FILTERS

The final limitation on SC filtering techniques is the noise contributions from the circuit elements - MOS op amps and switches. Noise is an important consideration because it is a fundamental constraint on the achievable dynamic range of any network. There are three noise sources in SC networks: the thermal noise of switches, and the 1/f noise (or flicker noise) and the thermal noise from op amps. The noise contribution at the output of a SC filter is determined by various transfer functions from the noise sources to the output. It should be clear that the noise output spectrum depends on filter order and configurations. In the following subsections, the three noise sources are qualitatively discussed.

2.2.1 KTC SWITCH NOISE

Thermal noise [4] is caused by random thermal motion of charges in the channel of a MOST. When a MOST is on, the thermal noise due to the finite on-resistance of the channel displays a white noise spectrum [4]. In particular, when this transistor is connected to a sampling capacitor C_s , as in a SC resistor, the lowpass filtered noise power across the capacitor is equal to [4]

$$\frac{V^2}{\text{rms}} = \frac{kT}{C_s} \quad (2-4)$$

where kT is a thermal constant. The noise due to the switch is often called KTC noise or Nyquist noise. Note that it is

independent of the value of the on-resistance. When the MOST turns off, the noise and signal are sampled and held on the sampling capacitor, C_s .

In a SC integrator, the total input-referred thermal noise from the switches within the integrator bandwidth is approximately equal to KT/C where C is the integrating capacitor [12]. This result is derived from an active-RC integrator under the assumption that the sampling rate is much larger than the frequency of interest. Since the KTC noise is inversely proportional to the integrating capacitor C , it seems logical to increase the value (i.e., size) of C to minimize the noise from switches. However this will increase the chip area, and so the sampling rate may have to be reduced to ensure complete charge transfer. Finally, the ability to scale feature size to make smaller VLSI SC filters seems to be restricted since small capacitors will enhance the filter switch noise.

2.2.2 OPERATIONAL AMPLIFIER BROADBAND NOISE

The equivalent input-referred noise spectrum of a typical op amp is given in Fig. 2.2. At low frequencies, the $1/f$ noise is dominant. After the break point, f_c (≈ 10 kHz [28]), the thermal noise corresponding to the flat portion of the noise spectrum becomes significant. The thermal noise of an op amp, which originates from its output stage [12], has a very wide noise

Fig. 2.2 Equivalent input-referred noise spectrum of an op amp.

bandwidth, relative to the sampling rate. As a result, this broadband noise can be aliased down into the passband by the following stages. Hence a low noise op amp design is a necessity in SC circuits. The broadband thermal noise can be reduced below the KTC noise by using sufficiently high transconductance input transistors in the op amp [22,23] or by removing the output stage where possible [12].

2.2.3 OPERATIONAL AMPLIFIER $1/f$ NOISE

The $1/f$ noise is due to the random fluctuation of charges in the surface states at the silicon-silicon dioxide interface of a MOST. The $1/f$ noise of an op amp is mainly from the input differential stage [22]. The op amp $1/f$ noise can be minimized by properly selecting the length-width ratios of the various devices in the input stage [32] and using large gate areas for the input transistor [9,22]. Because the $1/f$ noise is a low-frequency noise, aliasing effects can be neglected at a sufficiently high sampling rate.

2.3 TECHNIQUES FOR $1/f$ NOISE REDUCTION IN SC FILTERS

From the discussion of the previous two sections, it can be concluded that SC circuit and filter design is not simple. The design has been complicated by parasitic capacitances, finite on-resistance, clock feedthrough, circuit element noise, op amp performance, and so forth. Particularly, it has been shown that solutions to these problems involve consideration of many

tradeoffs. Parasitic capacitances, charge transfer and noise performance determine the minimum size of the capacitors, while the switch size is constrained by the speed consideration, power supply rejection, clock feedthrough and parasitic capacitance effects.

The dynamic range of a SC amplifier input offset-free filter is primarily set by the three noise sources. The $1/f$ noise of the op amp is dominant in voiceband filtering applications [12,32]. The magnitude of this noise is inversely proportional to the gate area of MOSTs on the input stage [9]. Hence increasing the size of the input MOSTs has been normally used. However it has been pointed out in section 2.1.4 that the power supply rejection (PSR) will be degraded by overlap capacitances of the MOSTs. This means that PSR and $1/f$ noise dictate the size of the input MOSTs. This becomes the stumbling block for scaling of SC filters. Alternate means of reducing the $1/f$ noise could solve this problems, and allow beneficial changes in op amp and SC filter designs.

Two techniques have been used to reduce the low frequency $1/f$ noise. A chopper-stabilization technique incorporated in an op amp used in a SC filter was reported in [12]. The correlated-double-sampling (CDS) technique's implementation in a SC filter was described in [28]. A novel implementation of the CDS technique in SC filters is investigated in this thesis. The general principles of the two techniques are discussed next.

Fig. 2.3(a) Concept of chopper-stabilization technique.
 (b) Equivalent input noise for the first-stage amplifier.

2.3.1 PRINCIPLE OF CHOPPER-STABILIZATION TECHNIQUE [12]

The chopper-stabilization technique is applied to the op amp design. The technique translates the input-referred $1/f$ noise of the op amp from the low-frequency region to a higher frequency range by modulating the noise. The concept is explained using a two-stage amplifier, as shown in Fig. 2.3(a). The chopper-stabilization technique is applied to the first amplifier. At the input and the output of the first amplifier are two multipliers which are driven by a chopping square wave. A voiceband input signal and the input-referred $1/f$ noise spectra are included in the figure. Only the signal is modulated by the first multiplier and translated to the odd harmonic frequencies of the chopping wave. After the second multiplier, the modulated signal is demodulated while the noise is modulated and translated to the odd harmonic frequencies of the chopping wave. The spectra of the signal and noise at the outputs of the two multipliers are also included in the figure. Fig. 2.3(b) shows the equivalent input noise spectrum. The $1/f$ noise density at low frequencies is due to $1/f$ fold-back noise [12]. A higher chopper frequency can further reduce the noise in the baseband.

2.3.2 PRINCIPLE OF CORRELATED-DOUBLE-SAMPLING TECHNIQUE

Fig. 2.4(a) gives the conceptual diagram [12] of the CDS technique applied to an amplifier. The input-referred $1/f$ noise spectrum of the amplifier and the clock waveform are shown in Fig.

2.4(b) and (c) respectively. On ϕ_1 , the sample-and-hold (S/H) stage stores the noise. On ϕ_2 , the noise sample taken at the end of ϕ_1 is subtracted from the incoming signal and noise. The noise-reduced signal is then amplified by G. The z-transform noise transfer function of this process is

$$H(z) = \frac{V_{out}}{V_n}(z) = G (1-z^{-1/2}) \quad (2-5)$$

The $(1-z^{-1/2})$ term represents the CDS action. The noise power z-transform transfer function is obtained by using the identity $|H(z)|^2 = H \cdot H^*$. Thus the equivalent input-referred noise, shown in Fig. 2.4(d), can be calculated as [12]

$$V_{n,eq}^2(\omega) = 2 [1 - \cos(\omega T/2)] V_n^2 \quad (2-6)$$

The zeros in Fig. 2.4(d) appear at the even integral multiples of the sampling rate. The zero at DC is the most attractive feature of the CDS technique. Ideally, total DC noise elimination can be achieved by the CDS technique.

2.4 SUMMARY

Nonideal properties of the SC filter components and their effects have been discussed in previous sections. The key problems created are limited dynamic range and degraded power

supply rejection. In addition, it is seen that tradeoffs among solutions, which reduce the nonideal effects, must be taken. Finally, two basic techniques suppressing the dominant $1/f$ noise are described. The CDS technique is chosen because of its simplicity and its important feature - total DC noise elimination. A novel implementation of the CDS technique in SC filters is thus investigated in this thesis.

CHAPTER 3

DETAILED ANALYSIS OF CDS FILTERS

3.0 INTRODUCTION

In chapter 1 the feasibility and advantages of the CDS SC integrator were discussed qualitatively. This chapter deals with this basic building block and analyzes its use in first and second order filtering applications in detail. The parasitic-free characteristic of the CDS integrator is established. Then the signal and noise transfer functions for the filters are derived using two different analyses. First, the z-transform analysis is used to get quick valuable results. Second, an exact analysis is extensively used to obtain exact filter characteristics. Non-idealities such as finite op amp gain and parasitic capacitances to ground are also considered in the exact analysis, so that their effects on the CDS-type filters can be better understood.

3.1 PARASITIC-FREE CDS INTEGRATOR

The inverting CDS integrator is shown in Fig. 3.1(a), including parasitic capacitances due to the switches and capacitors at each circuit node. The effects of capacitances C_{p1} , C_{p2} , C_{p5} , and C_{p7} can be neglected since they are connected to the low-impedance points - a signal input, an amplifier output or ground. C_{p6} can also be removed because it attaches to the virtual ground of the op amp. The simplified circuit diagram is

(a)

(b)

Fig. 3.1 An inverting CDS SC integrator with parasitic capacitances.

shown in Fig. 3.1(b). Another simplification can be made because C_{p4} is switched to ground on ϕ_1 and to the virtual ground of the composite amplifier on ϕ_2 , assuming that the amplifier is ideal (i.e., infinite gain). The output of this integrator is free from parasitic capacitances as can be verified by the following description of the circuit operation. When ϕ_1 -controlled switches are on, C_1 and C_{p3} are discharged to ground, and the op amp initializes itself. C_{p8} experiences charge redistribution from C_1 which stores charges from the previous ϕ_2 . C_{p8} may gain (or lose) charges from (or to) C_1 during the ϕ_1 clock. When ϕ_2 -controlled switches are on, the charge gained by C_{p8} during ϕ_1 can not discharge to the virtual ground of the composite amplifier, and must flow back to C_1 . This means that C_1 does not lose any charge from the previous ϕ_2 to C_{p8} . During the same interval, the input voltage V_i is coupled directly to C_1 through C_1 without error. At the end of ϕ_2 , both C_1 and C_{p3} are charged to V_i . The charge in C_1 and C_{p3} is then discharged again on the next ϕ_1 . Hence, C_{p3} only absorbs charge from V_i and discharges to ground, thereby not interfering with circuit operation. As the total charge integrated by C_1 is supplied from V_i through C_1 , the inverting CDS

integrator is parasitic-free. The analysis has also been done for the noninverting CDS integrator, and it is also found to be parasitic-free from the same type of argument.

Parasitic-free building blocks are important in SC applications. They enable transfer function accuracy since precise capacitor ratios become possible. In addition, many SC filters are required to realize a LSI system. It is extremely important that these SC filters be small in size. This can only be achieved if small-unit capacitance can be used. As discussed in section 2.1.2, the parasitic capacitance causes capacitor ratio error which increases as the size of unit capacitance decreases. For high-speed filters, the maximum sampling rate is determined by the settling time of op amps and the charging time of the capacitors [23]. These times rely heavily on the capacitor sizes. Small capacitors must be used to allow high sampling rates. Therefore parasitic-free building blocks must be employed in order to accomplish the above goals.

3.2 ANALYSIS OF FIRST-ORDER LOWPASS FILTERS

A first-order lowpass filter serves as a building block in realizing high-order filters by the cascade realization approach. Three different configurations are analyzed in this section. Two of them are novel designs based on the CDS integrator. For comparison, a conventional lowpass filter [20] realized with the parasitic-free integrator of Fig. 1.6(a) is also considered. The three inverting lowpass filters are shown in Fig. 3.2. Note that

Fig. 3.2 First-order inverting lowpass (LP) SC filters.

- (a) A conventional LP filter.
- (b) An offset-free LP filter.
- (c) A CDS LP filter.

where $C_2 = a_2 C_1$ and $C_3 = a_3 C_1$

the difference between the filters in Figs. 3.2(b) and (c) occurs in the connection of the feedback SC resistor. For convenience, each of these filters are assigned with a name. According to the order shown in Fig. 3.2, they are the conventional lowpass (LP) filter, the offset-free LP filter and the CDS LP filter, respectively. Justification of the names of the CDS-based filters will be discussed later. The filter outputs are valid at the end of ϕ_2 . Again, V_n is a general input-referred noise source (which includes $1/f$ noise, amplifier input offset, and low-frequency power supply noise).

3.2.1 SAMPLED-DATA ANALYSIS OF FIRST-ORDER FILTERS

Initially, the z-domain signal and noise transfer functions were derived separately for the three filters shown in Fig. 3.2 under the assumption that the op amp gain and bandwidth are infinite. From these results, it was found that the corresponding transfer functions can be easily modelled as shown in Fig. 3.3(a), which illustrates a general representation for the three filters at the end of ϕ_2 . The parameters J and K will be used appropriately to make Fig. 3.3(a) conform to various filters in Fig. 3.2. Except for V_n , the voltage sources represent the charge stored on the capacitors at the end of the previous ϕ_1 (for C_1 and C_3) or from the previous ϕ_2 (for C_2). The sampling instants are defined by the clock waveforms presented in Fig. 3.3(b). Applying the

(a)

(b)

Fig. 3.3(a) A general representation of filters in Fig. 3.2 at the end of ϕ_2 .

(b) Definition of sampling instants.

principle of charge conservation at node A (i.e., the virtual ground of the composite amplifier) gives:

$$\begin{aligned}
 & [V_o(n) - [V_o(n-1) - \Delta V_n(n-1)] - \Delta V_n(n)] \frac{C}{1} \\
 & + [V_o(n) - KV_n(n - 1/2) - \Delta V_n(n)] \frac{a C}{3 \cdot 1} \\
 & + [V_i(n) - \Delta V_n(n)] \frac{a C}{2 \cdot 1} = 0
 \end{aligned} \tag{3-1}$$

where

$\Delta V_n(n)$ is the variation of input-referred noise voltage during the interval $(n - 1/2)T$ to nT (i.e., $\Delta V_n(n) = V_n(n) - JV_n(n - 1/2)$),

$$\Delta V_n(n-1) = V_n(n-1) - JV_n(n-3/2)$$

and J, K are equal to 1 or 0. J and K are used to signify the type of lowpass filter analyzed and to remove redundant terms in the general z -domain equation derived from Fig. 3.3(a).

Substituting $\Delta V_n(n)$ and $\Delta V_n(n-1)$ into Eq. (3-1) and taking the z -transform gives:

$$\begin{aligned}
 & V_o(z) \left[1 + \frac{a}{3} z^{-1} \right] \\
 & = V_n(z) \left[\left(1 + \frac{a}{3} + \frac{a}{2} z^{-1} \right) (1 - Jz^{-1/2}) + K \frac{a}{3} z^{-1/2} \right] - \frac{a}{2} V_i(z)
 \end{aligned} \tag{3-2}$$

Letting V_n equal zero gives the signal transfer function:

$$H_s(z) = \frac{V_o}{V_i}(z) = \frac{\frac{a}{2}}{1 + \frac{a}{3} z^{-1}} \tag{3-3}$$

which applies to the three lowpass filters of Fig. 3.2. For V_i equal to zero, Eq. (3-2) yields the general noise transfer function:

$$H_{nl}(z) = \frac{V_o}{V_n}(z) = \frac{(1 + \frac{a}{3} + \frac{a}{2}z^{-1})(1 - Jz^{-1/2}) + Ka z^{-1/2}}{1 + \frac{a}{3}z^{-1}} \quad (3-4)$$

In the conventional LP filter of Fig. 3.2(a), the feedback switched capacitor, $a C$ is discharged on ϕ (i.e., $KV_n(n-1/2)=0$) and the initializing capacitor C is not present to store the instantaneous noise voltage at the end of ϕ (i.e., $JV_n(n-1/2)=0$). Therefore both J and K equal to zero. The general noise transfer function becomes:

$$H_{nl}(z) = \frac{V_o}{V_n}(z) = 1 + \frac{\frac{a}{2}}{1 + \frac{a}{3}z^{-1}} \quad (3-5)$$

At DC (i.e., $z = 1$), Eq. (3-5) gives:

$$H_{nl}(z=1) = 1 + \frac{a}{2} / \frac{a}{3} \quad (3-5a)$$

which agrees with the result from the well-known active-RC equivalent.

For the offset-free LP filter of Fig. 3.2(b), C_1 is present to store the noise voltage. The feedback switched capacitor is again discharged on ϕ . The noise transfer function can be calculated by letting $J = 1$ and $K = 0$ in Eq. (3-4):

$$H_{n2}(z) = \frac{V_o}{V_n} = (1 + \frac{a}{2} z^{-1/2}) (1 - z^{-1/2}) \quad (3-6)$$

Note that the existence of the $(1 - z^{-1/2})$ reflecting the CDS filtering action and the difference between Eqs. (3-5) and (3-6). At DC, the noise transfer function is:

$$H_{n2}(z = 1) = 0 \quad (3-6a)$$

This means that the output at the active phase ϕ_2 is insensitive to the amplifier input offset, thus explaining the name chosen for the filter.

In the CDS filter of Fig. 3.2(c), both J and K are equal to one since both C_1 and $a C_3$ store the noise voltage at the end of ϕ . After the substitution, Eq. (3-4) becomes:

$$H_{n3}(z) = \frac{V_o}{V_n} = (1 + \frac{a}{2} z^{-1/2}) (1 - z^{-1/2}) + \frac{a z^{-1/2}}{1 + a z^{-1/2}} \quad (3-7)$$

The transfer function at DC is:

$$H_{n3}(z = 1) = 1 \quad (3-7a)$$

Eq. (3-7a) indicates that the amplifier input offset appears at the output of the CDS LP filter, not only during the initializing phase ϕ_1 , but also during the active phase ϕ_2 (for no signal input). If this output is ac-coupled to the following SC stage, a CDS-type subtracting action removing the offset takes place. This explains the name chosen for the filter as well. This filter is especially important in the state-variable biquad realizations of this thesis, as will be discussed in section 3.3. Table 3-1 summarizes the results obtained from the z-transform analysis.

It should be emphasized that the transfer functions derived are valid only at the sampling instant (i.e., nT) [33]. The output waveform of conventional SC filters is a 100% sample-and-hold type as opposed to that of the CDS-type filters (shown in Fig. 1.8). The theoretical output spectrum of a SC filter must be obtained by multiplying the z-domain transfer function by its corresponding $(\sin x / x)$ function. Another possible deviation from the z-transform analysis is due to feedthrough which causes inaccuracies in frequency response analysis. It vanishes when either the input is sampled or there is no direct path from the input to the output or both. Referring to the circuit diagrams of the three inverting lowpass filters in Fig. 3.2, such a direct path exists during ϕ_2 . This is true because these filters use the

Table 3-1 A summary of the sampled-data analysis.

FILTER TYPE	J	K	SIGNAL TRANSFER FUNCTION (V_O/V_I)	NOISE TRANSFER FUNCTION (V_O/V_n)	NOISE TRANSFER FUNCTION AT DC
Active-RC lowpass filter	-	-	$\frac{-R/R}{1 + sCR}$	$\frac{R/R}{1 + sCR}$	$\frac{R}{1 + R}$
Conventional SC LP filter	0	0	$\frac{-a}{1 + a - z}$	$\frac{a}{1 + a - z}$	$\frac{a}{1 + a}$
Offset-free SC LP filter	1	0	$\frac{-a}{1 + a - z}$	$\frac{a}{(1 + \frac{-1/2}{1 + a - z})(1 - z)}$	0
CDS SC LP filter	1	1	$\frac{-a}{1 + a - z}$	$\frac{a}{(1 + \frac{-1/2}{1 + a - z})(1 - z)}$	1

$$R = \frac{T}{3} \text{ and } R = \frac{T}{2} \text{ and } R = \frac{T}{2}$$

57

noninverting type parasitic-free input SC resistor for C_2 . Feed-through can be avoided either by using the inverting type parasitic-free input SC resistor or by connecting a sample-and-hold (S/H) circuit to the input node. Since the op amp noise (V_n) is continuous, the z-domain transfer functions do not adequately characterize the noise performance of the filters.

3.2.2 EXACT ANALYSIS OF FIRST-ORDER FILTERS

Since the z-transform technique does not handle continuous inputs, as discussed in the previous section, the technique is not adequate for noise analysis. An exact analysis method developed by Brglez [34,35], which is computer-simulation oriented, has been used to obtain theoretical results which can be compared with the experimental results. The exact analysis method is applicable to arbitrary SC networks with arbitrary inputs (i.e., sampled-data input or continuous input) and switching sequences. The effects of sample-and-hold, feedthrough and aliasing are automatically incorporated in the analysis. Furthermore, the effects of finite op amp gain and parasitic capacitances from any node to ground can also be incorporated. Both the time and frequency responses at each node of a SC network can be calculated. Basically, the derivations are based on the concept that a voltage change at a circuit node is caused by either charge redistribution due to the initial condition(s) (i.e., charge from the previous state) or signal input(s) or both. Closing and opening of the switches in a SC network defines a distinct network configuration for each clock

phase. The interconnections of the configuration are described by the corresponding switching matrix (F) for charge redistribution and feedthrough matrix (G) for signal input(s).

The derivations have been thoroughly discussed in [34,35], so the details will not be elaborated. The closed-form transfer function matrix of a two-phase SC network for exponential input $\exp(j\omega t)$ is:

$$T(\omega) = \sum_{k=0}^{\infty} \left[\frac{1}{T_0} G + \frac{\exp(j\omega \Delta) - 1}{j\omega T_0} \left[-G + \sum_{m=0}^{\infty} H_{k,m}(z) \right] \right] \exp[-j\omega[(t_k + \Delta) - (t_m + \Delta)]] \quad (3-8)$$

where

$$H_{0,0}(z) = \begin{bmatrix} I - z^{-1} & -1 \\ 0 & 0 \end{bmatrix} G \quad (3-8a)$$

$$H_{0,1}(z) = \begin{bmatrix} I - z^{-1} & -1 & -1 \\ 0 & 1 & 1 \end{bmatrix} G z \quad (3-8b)$$

$$H_{1,0}(z) = F H_{0,0}(z) \quad (3-8c)$$

$$H_{1,1}(z) = F H_{0,1}(z) + G \quad (3-8d)$$

and

$$\begin{bmatrix} * \\ 0 \end{bmatrix} = F \begin{bmatrix} F \\ 0 \end{bmatrix}$$

$$\begin{bmatrix} * \\ 1 \end{bmatrix} = F \begin{bmatrix} F \\ 0 \end{bmatrix}$$

The indices, k and m , represent a particular switched state (e.g., state 0 = ϕ high, ϕ low). G_0 and G_1 are the feedthrough matrices for state 0 and state 1 respectively while F_0 and F_1 are the switching matrices corresponding to the particular switched state. T_0 is the period of the sampling rate. Δ_k and t_k are the duration and the switching instant of a switched state k , respectively. Finally, I is the identity matrix.

According to Eq. (3-8), matrices F_0 , F_1 , G_0 and G_1 must be specified in order to use the analysis method. Procedures required to determine these matrices are given in Appendix B. Fig. 3.4 shows an inverting CDS LP filter cascaded to an output stage. The output stage is also included in the exact analysis for the reason presented below. The output of the CDS LP filter is only valid during ϕ_2 . Therefore only the noise during this interval is of interest. In addition, the noise reduction process using the initializing technique occurs on ϕ_2 . Circuitry is thus required to perform such a noise measurement. From Fig. 3.4, it is obvious that the filter output at DC during ϕ_1 is V_n (amplifier input offset). From Table 3-1, it is evident that the filter output at DC during ϕ_2 is the sum of V_n and the output signal due to the input signal. Hence an edge signal (a net change of voltage levels) representing only the noise-free output signal is developed from ϕ_1 to ϕ_2 . For frequencies other than DC, the edge

Fig. 3.4 A first-order CDS lowpass (LP) filter with an output stage for noise measurement.

signal will be a noise-reduced output signal. The main purposes of the CDS voltage follower are to retrieve this edge signal and to measure the noise response (for no signal input). Moreover, it simulates the type of coupling used in the novel CDS biquad (section 3.3). Its operation is similar to that of the unique output circuit used in CCD line imagers (Fig. 1.3 of section 1.3).

The parasitic capacitance associated with the virtual ground of the composite amplifier is modelled by C_8 , as shown in Fig.

3.4. The effective gain of the composite amplifier during the active phase (ϕ_2) is modelled by an "imaginary" capacitor C_{sf} .

The amplifier gain is then equal to C_1 / C_{sf} which is assumed to be

much smaller than the open-loop gain of the op amp, A_o . The capacitive gain for the composite amplifier is valid because the amplifier responds to displacement signals or edge signals. The inclusion of C_{sf} as shown will become clear in chapter 4.

The switching (F's) and feedthrough (G's) matrices of the inverting CDS LP filter are given in Fig. 3.5(a). The derivation of these matrices is given in Appendix B. Matrices F_0 and G_0 are determined from the filter configuration during ϕ_1 while F_1 and G_1 are evaluated during ϕ_2 . A noninverting CDS LP filter, which has no feedthrough, has also been considered. The noninverting filter is obtained by simply interchanging the clock signals of the two input switches. With such a change, the effective input becomes

$$F_0 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

 F_0

$$G_0 = \begin{bmatrix} 0 & 1 \\ 0 & 0 \\ 0 & 1 \\ 0 & 0 \\ 0 & 1 \\ 0 & 1 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}$$

 G_0

$$G_1 = \begin{bmatrix} -\frac{c}{s} & 1-s \\ 1-\frac{c}{s} & -s \\ -\frac{(a+1)c}{s} & x-s \\ -\frac{(a+1)c}{s} & x-s \\ -\frac{ac}{s} & x \\ 0 & 0 \\ -\frac{ac}{s} & x \\ -\frac{c}{s} & -s \end{bmatrix}$$

 G_1

$$F_1 = \begin{bmatrix} 1 & \frac{c}{s} & \frac{d}{s} & \frac{e}{s} & 0 & 0 & 0 & \frac{f}{s} \\ 1 & \frac{c}{s} & \frac{d}{s} & \frac{e}{s} & 0 & 0 & 0 & \frac{f}{s} \\ -b & \frac{(a+1)c}{s} & \frac{(a+1)d}{s} & \frac{(a+1)e}{s} & 0 & 0 & 0 & \frac{(a+1)f}{s} \\ -b & \frac{(a+1)c}{s} & \frac{(a+1)d}{s} & \frac{(a+1)e}{s} & 0 & 0 & 0 & \frac{(a+1)f}{s} \\ -b-1 & \frac{ac}{s} & \frac{ad}{s} & \frac{ae}{s} & 0 & 0 & 0 & \frac{af}{s} \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ -b-1 & \frac{ac}{s} & \frac{ad}{s} & \frac{ae}{s} & 0 & -1 & 0 & \frac{af}{s} \\ 1 & \frac{c}{s} & \frac{d}{s} & \frac{e}{s} & 0 & 0 & 0 & \frac{f}{s} \end{bmatrix}$$

 F_1

Fig. 3.5(a) Switching and feedthrough matrices of the inverting CDS LP filter shown in Fig. 3.4.

$$\begin{bmatrix} 0 & 1 \\ 1 & 0 \\ 0 & 1 \\ 0 & 0 \\ 0 & 1 \\ 0 & 1 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}$$

 G_0'

$$\begin{bmatrix} 0 & 1 & -y \\ 0 & -y \\ 0 & x & -y \\ 0 & x & -y \\ 0 & x \\ 0 & 0 \\ 0 & x \\ 0 & -y \end{bmatrix}$$

 G_1'

$$a = \frac{C_1}{C_{sf}}$$

$$b = \frac{C_2 + C_8}{C_3 + C_4}$$

$$c = C_2$$

$$d = C_3$$

$$e = C_4$$

$$f = C_8$$

$$s = c + f + (1 + a)(d + e)$$

$$x = \frac{C_T(C_1 + C_{sf}) - C_1^2}{C_T C_{sf} + C_1(C_3 + C_4)}$$

$$y = \frac{C_1}{C_T} + x \left(\frac{C_3 + C_4}{C_T} \right)$$

$$C_T = C_1 + C_2 + C_3 + C_4 + C_8$$

Fig. 3.5(b) Feedthrough matrices of the noninverting CDS LP filter (with the output stage). F_0 and F_1 are the same as Fig. 3.5(a).

sampled-data input even though the original input is continuous. The feedthrough matrices of the noninverting filter are included in Fig. 3.5(b). Note the difference of the first column between the corresponding G matrices for the two filters. The difference is caused by the type of input SC resistor used (i.e., inverting or noninverting type). The second column of both G_0' and G_1' matrices are identical to those of G_0 and G_1 because the derivation procedure for this column assumes no signal input, making the configurations for both filters to noise input the same. In addition, there is no change in the switching matrices since these matrices describe charge redistribution. Finally, the offset-free and conventional LP filters, whose circuit diagrams for the exact analysis method are shown in Fig. 3.6 and Fig. 3.7 respectively, have also been analyzed. Note that the output stage for the offset-free filter (in Fig. 3.6) is just a fifty-percent duty cycle S/H circuit which is used to simplify noise measurement for the same reason discussed for the CDS filter. However, since the output of this filter is free from amplifier input offset (V_n at DC) during ϕ_2 , the CDS voltage follower cannot be used. The theoretical frequency responses of the filters (of Fig. 3.2) to signal input and noise input of same magnitude are illustrated in Fig. 3.8. It should be remarked that the signal responses for the two filter types - conventional and CDS, display approximately 6 dB ($|20 \log 1/2|$) difference. This is because of the nature of the corresponding output waveforms (see Fig. 1.8) or, in other words, the difference between the corresponding $\sin x / x$ func-

Fig. 3.6 A first-order offset-free lowpass filter with an output stage for noise measurement.

Fig. 3.7 Conventional LP filter for the exact analysis method.

Fig. 3.8 Frequency response of the three filters to signal and noise inputs of same magnitude. ($f_{\text{corner}} = 1516 \text{ Hz}$)

Fig. 3.9 Theoretical S/N ratios of the three lowpass filters for normalized inputs, i.e., assuming signal and noise have same magnitude.

tions. Furthermore, it is seen that up to the filters' corner frequency (1516 Hz), the CDS-type filters provide at least a 20 dB improvement in noise attenuation compared to the conventional filter. For a better comparison, the theoretical S/N ratios of the three filters, which can be determined from Fig. 3.8, are plotted in Fig. 3.9. The word - normalized implies that same magnitude of signal and noise inputs are assumed for obtaining the S/N ratios. The advantage of the CDS-type filters is obvious since the curves representing the S/N ratios of the filters are well above the 0 dB line as opposed to that of the conventional filter.

3.2.3 ANALYSIS OF CLOCK FEEDTHROUGH IN A NOVEL FIRST-ORDER FILTER

Clock feedthrough has been discussed in section 2.1.4. Its effects on the CDS lowpass filter are studied and presented in this section. The circuit diagram of the filter is reproduced in Fig. 3.10(a). First, the switch channel charge is considered. Then the capacitive coupling through the switch overlap capacitances is discussed. Clock feedthrough due to channel charge in switch Q_1 can be neglected because most of the charge is supplied by the analog ground when the switch is on and this charge flows back to the analog ground when the switch is off. Next, the channel charge contribution of Q_2 can be partially neglected, since the channel charge is mainly supplied by the amplifier output when the switch turns on. However, when the switch turns

Fig. 3.10 (a) The CDS LP filter.
 (b) The CDS LP filter with parasitic coupling capacitors.
 (c) The clock feedthrough model of C_{p1} .

off, a small fraction of the channel charge in Q_2 is injected to the inverting input terminal of the op amp. Last, the contribution of Q_3 is considered. When Q_3 is on, its channel charge is drawn from the integrating capacitor C_1 and the switched capacitor C_3 . When the switch turns off, unequal amounts of the channel charge will flow back to the corresponding capacitors, thereby causing errors.

Fig. 3.10(b) shows the specific overlap capacitances which also need to be considered for the clock feedthrough analysis (section 2.1.4). The following example demonstrates the significant effect of clock feedthrough due to the overlap capacitances. With the input node grounded, the capacitive-coupling model of C_{pl} when the ϕ_1 clock driving switch Q_2 goes low is shown in Fig. 3.10(c). Applying the principle of charge conservation to nodes labelled (1) and (2) gives the following clock feedthrough transfer function.

$$\frac{V_o}{V_{\phi_1}} = \frac{-C_{pl} (C_1 + C_2 + C_3)}{C_1 C_3} \quad (3-9)$$

For a high gain lowpass filter (let $C_1 = C_2 = 5$ pf and $C_3 = 0.2$ pf),

Eq. (3-9) simplifies to

$$\frac{V_o}{V_{\phi}} = -10.2 \times 10^{12} \times C_{p1} \quad (3-9a)$$

Thus the amplifier has a significant output offset error for typical values of C_{p1} and clock pulse height. Similar capacitive-coupling models for C_{p2} and C_{p3} can be derived. It is found analytically and experimentally that C_{p1} has the largest effect on the output offset error.

Several effective clock feedthrough cancellation techniques have been used to reduce clock feedthrough induced offset [12,28]. In these two papers, a fully differential (differential input, differential output) topology was used to suppress the common mode clock noise. However this technique requires a fully differential op amp, whose design is quite complex. A differential scheme [16] proposed by D. Ribner and tried in this thesis avoids the complexity of the fully differential technique since a conventional op amp (differential input, single-ended output) can be used. The clock feedthrough cancellation circuit depends on component matching and the common mode rejection of the op amps. Furthermore, this technique minimizes the effects of power supply coupling onto the inverting input, and thus improves the power supply rejection. The single-ended differential scheme CDS LP filter is shown in Fig. 3.11 as a demonstration. Note the similarity between this topology and the classical difference amplifier composed of resistors. Because of its completely symmetrical nature, mismatches of

Fig. 3.11 A single-ended output differential input CDS LP filter for clock feedthrough cancellation.

switches and capacitors should be minimized.

3.3 ANALYSIS OF STATE-VARIABLE BIQUADS

Two-integrator state-variable biquads are versatile building blocks in SC filtering applications. They can be used to realize precision high-order filters simply by cascading them. The major advantage of these SC biquads is that their filter characteristics can be independently varied by capacitor ratios and by the sampling rate. In this section, the conventional biquad [20] and two novel biquads based on the CDS integrators are studied analytically using both the z-transform and exact analysis method. These biquads are immune to parasitic capacitances (assuming infinity gain) since they are implemented by the corresponding parasitic-free inverting and noninverting integrators.

A general active-RC biquad which can realize any type of second-order filter is analyzed in Appendix C using an s-domain approach. The analysis allows a better understanding of its SC versions. The SC equivalents of the general RC biquad realized by the conventional and CDS integrators are given in Appendix C. The z-transform analysis has been carried out in Appendix C to obtain the general signal and noise transfer functions which are used in the discussion of the bandpass (BP) biquads (in section 3.3.1).

Shown in Fig. 3.12(a) is a schematic diagram of an active-RC bandpass biquad. Its conventional SC equivalent is given in Fig. 3.12(b). The switch arrangement shown embodies the LDI timing [4], which allows the conventional biquad to closely approximate

Fig. 3.12 (a) Active-RC bandpass biquad.
(b) Conventional active-SC bandpass equivalent.

the active-RC biquad. This SC configuration eliminates the extra unity-gain inverting amplifier required in the active-RC version because the inverting SC resistor ($a_{22} C_2$) of Fig. 1.6(b) simulates

the "negative resistor" (i.e., $-R_2$). Furthermore, the

noninverting SC resistors are used to simulate R_3 and R_4 . It is

important to note that the "input" terminals of the SC resistors $a_{22} C_2$, $a_{32} C_2$ and $a_{41} C_1$ are required, between the two clock phases,

to step between analog ground and the output signal of the previous integrator. An edge signal is, therefore, delivered through the respective SC resistors. Clearly, if a fixed level shift such as caused by an offset were to be added to the analog ground and the preceding amplifier output, the effective edge signal would be the same and such addition would not affect the circuit operation. According to this argument and the output characteristic of the CDS LP filter, the two input switches in the SC resistors can be dispensed with. The resulting novel CDS bandpass biquad is shown in Fig. 3.13(a). The action of the input switches is accomplished by the initializing action and the filter outputs. The other notable feature is an unity-gain noninverting amplifier. Because of the circuit operation of the CDS integrator, namely, the initializing operation, the valid output cannot be held for half a period as is required for LDI timing. The noninverting amplifier provides the half period delay by controlling the shorting switch with ϕ_2 . Due to the arrangement of the clock phases in the first integrator and the noninverting

amplifier, a double inversion occurs: one inversion is at the input capacitor C due to the clocking sequence of the integrator and the other is due to the op amp of the amplifier. The signal is therefore not inverted. The required inversion is achieved by the SC resistor $a \cdot C$, which is effectively an inverting SC
22 2

resistor. The added amplifier will have the noise-reduced advantage of the CDS integrator because of the initialization on ϕ . At DC, the output of this bandpass biquad will have the
2 input-referred offset of amplifier OAI (i.e., V_{nl}) added to the output signal, just like the CDS LP filter. This will be verified mathematically. Since the subsequent biquad stages in a high-order filter can be shown to be either capacitor coupled (e.g. bandpass biquads) or coupled via the switch-removed SC resistor (e.g. lowpass biquads) such offset at the output will cause no problem except the last stage. A CDS voltage follower or an offset-free unity-gain amplifier can be used to remove the remaining offset. Also a modified CDS-type biquad has no output offset can be used for the last stage, although four more switches are required. Such an offset-free biquad is shown in Fig.

3.13(b), which gives the bandpass characteristic.

3.3.1 SAMPLED-DATA ANALYSIS OF SECOND-ORDER BANDPASS FILTERS

The unity-gain noninverting amplifier and the three bandpass biquads are analyzed using the z -transform. The schematic equivalent of the noninverting amplifier in the CDS bandpass

biquad is shown in Fig. 3.14. The charge-conservation equation at the summing node is (at the end of ϕ):

$$(V_o(n) - V_{os})C + [-(V_i(n - 1/2) - V_{os}) - V_{os}]C = 0 \quad (3-10)$$

where V_{os} is the amplifier input offset. Taking the z-transform of Eq. (3-10) gives:

$$V_o(z) = V_i(z) z^{-1/2} + V_{os} \quad (3-11)$$

Eq. (3-11) shows that the input is delayed by half a period and is not inverted. The offset added to the delayed output will cause no problem to the following stage if the amplifier output is ac-coupled or coupled as in the novel bandpass biquads of Fig.

3.13.

The signal transfer function, $H_{BP}(z)$, for the three SC

bandpass biquads can be determined from the general signal transfer function derived in Appendix C by letting the appropriate a (capacitor ratios) equal zero (see Fig. 3.12(b) and Fig. 3.13).

Thus

$$H_{BP}(z) = \frac{V_o}{V_i}(z) = \frac{1}{z^{-2} - z^{-1} + (2 + \frac{a_3}{2} - \frac{a_2}{2} - \frac{a_4}{4}) + 1 + \frac{a_3}{3}} \quad (3-12)$$

The bandpass signal, V_1 , is available at the output of the non-

Fig. 3.14 A unity-gain noninverting amplifier.

Fig. 3.15 A two-amplifier S/H input stage.

lossy integrator. The corresponding noise transfer functions of the amplifier noise sources shown in the bandpass biquads are:

$$\frac{V_1}{V_{n1}}(z) = \frac{1}{D(z)} \left\{ (1 + Jz^{-1/2})(1 + a_3^{-1}z^{-1})(1 + a_4^{-1}z^{-1}) + Kz^{-1/2} \frac{a_2 a_4}{z^2} \right\} \quad (3-13a)$$

$$\frac{V_2}{V_{n2}}(z) = \frac{1}{D(z)} \left\{ Mz^{-1/2} \frac{a_4}{z^4} (1 + a_3^{-1}z^{-1}) - a_4 (1 + Lz^{-1/2}) \times \right. \\ \left. (1 + a_2 \frac{a_4}{z^2} + a_3 \frac{a_4}{z^3} - z^{-1} (1 + a_5^{-1})) - \right. \\ \left. M a_3 \frac{a_4}{z^4} \right\} \quad (3-13b)$$

where

$$D(z) = z^{-2} - z^{-1} (2 + a_3^{-1} - a_2 \frac{a_4}{z^2}) + 1 + a_3^{-1}$$

and V_{n1} and V_{n2} are the noise voltages associated with OP1 and OP2 respectively.

Again, the parameters J, K, L and M are used appropriately to make Eqs. (3.13a) and (3.13b) give the noise transfer functions for the specific bandpass biquad. The values of J, K, L and M are determined in the same fashion explained in the analysis of first-order lowpass filters (section 3.2.1). J and K pertain to the first integrator while L and M pertain to the second

integrator. The values of J and L indicate whether or not the integrators have the initializing capacitor C. The value of K

and M are determined by the types of SC resistor used -- conventional SC resistor or the type employed by the CDS lowpass filter.

For the conventional bandpass filter of Fig. 3.12(b), J, K, L and M are equal to zero. Its noise transfer functions are:

$$H_{n1}(z) \Big|_{\text{conv. BP}} = \frac{V_1}{V_{n1}}(z) = \frac{1}{D(z)} [z^{-2} - z^{-1} (2 + \frac{a}{3} + \frac{a}{4}) + (1 + \frac{a}{3})(1 + \frac{a}{4})] \quad (3-14a)$$

$$H_{n2}(z) \Big|_{\text{conv. BP}} = \frac{V_1}{V_{n2}}(z) = \frac{1}{D(z)} [z^{-1} \frac{a}{4} (1 + \frac{a}{c5}) - \frac{a}{4} (1 + \frac{a}{22} + \frac{a}{3} + \frac{a}{c5})] \quad (3-14b)$$

At DC, Eqs. (3-14a) and (3-14b) become:

$$H_{n1}(z=1) \Big|_{\text{conv. BP}} = \frac{\frac{a}{3}}{\frac{a}{22}} \quad (3-14c)$$

$$H_{n2}(z=1) \Big|_{\text{conv. BP}} = - (1 + \frac{\frac{a}{3}}{\frac{a}{22}}) \quad (3-14d)$$

These results again agree with those obtained from the continuous

active-RC equivalent. Next, for the CDS bandpass biquad shown in Fig. 3.13(a), the values of all the parameters (i.e., J, K, L and M) are one. Substituting these value into Eqs. (3-13a) and (3-13b) gives:

$$\begin{aligned}
 H_{n1}(z) \Big|_{\text{CDS BP}} &= \frac{V}{V_{n1}}(z) \\
 &= \frac{1}{D(z)} \left[(1 - z^{-1/2})(1 + a_3 - z^{-1})(1 + a_4 - z^{-1}) + z^{-1/2} a_{22} a_{44} \right]
 \end{aligned}
 \quad (3-15a)$$

$$\begin{aligned}
 H_{n2}(z) \Big|_{\text{CDS BP}} &= \frac{V}{V_{n2}}(z) \\
 &= \frac{1}{D(z)} \left[z^{-1/2} a_4 (1 - z^{-1}) - a_4 (1 - z^{-1/2}) \times \right. \\
 &\quad \left. (1 + a_{22} + a_3 + a_{c5} - z^{-1} (1 + a_{c5})) \right]
 \end{aligned}
 \quad (3-15b)$$

At DC, these equations are simplified to:

$$H_{n1}(z=1) \Big|_{\text{CDS BP}} = 1 \quad (3-15c)$$

$$H_{n2}(z=1) \Big|_{\text{CDS BP}} = 0 \quad (3-15d)$$

The result shown in Eq. (3-15c) is as expected and has been discussed in the design of the CDS BP biquad (from the conventional version). The name of this biquad is chosen for the same

reason as that of the CDS LP filter. For the offset-free BP biquad of Fig. 3.13(b), J and L are equal to one while K and M equals zero. After substitution, Eqs. (3-13a) and (3-13b) yield:

$$\begin{aligned} H_{n1}(z) \Big|_{\text{offset-free BP}} &= \frac{V_1}{V_{n1}}(z) \\ &= \frac{1}{D(z)} [(1 - z^{-1/2})(1 + a_3 - z^{-1})(1 + a_4 - z^{-1})] \quad (3-16a) \end{aligned}$$

$$\begin{aligned} H_{n2}(z) \Big|_{\text{offset-free BP}} &= \frac{V_1}{V_{n2}}(z) \\ &= \frac{1}{D(z)} [-a_4(1 - z^{-1/2})(1 + a_{22} + a_3 + a_5 - z^{-1}(1 + a_{c5}))] \quad (3-16b) \end{aligned}$$

At DC:

$$H_{n1}(z=1) \Big|_{\text{offset-free BP}} = 0 \quad (3-16c)$$

$$H_{n2}(z=1) \Big|_{\text{offset-free BP}} = 0 \quad (3-16d)$$

Therefore, this offset-free biquad is indeed amplifier input offset-free. The above results at DC are as expected. Analysis of the noise behaviour at other frequencies requires the use of the exact analysis method.

Finally, the noise voltage associated with the additional noninverting amplifier in the CDS integrator-based biquads has not

22
OF / DE

been considered for two reasons. First, the amplifier stage has the low-frequency reduction property as pointed out in section 3.3. Second, any high frequency noise is lowpass filtered by the subsequent stage - a lossy integrator (Fig. 3.13).

3.3.2 EXACT ANALYSIS OF SECOND-ORDER BANDPASS FILTERS

The exact analysis method is further used to analyze the three bandpass biquads. The analyses include the S/H input stage shown in Fig. 3.12(b) and Fig. 3.13 and the corresponding output stage as for the first-order filters. The S/H input stage, shown in Fig. 3.15, is used to avoid direct signal feedthrough via C on $\emptyset$ if the input is continuous. The analysis procedure

has already been discussed in Appendix B for the CDS LP filter. The exact filter responses to signal and noise inputs of same magnitude are shown in Fig. 3.16 and Fig. 3.17 respectively. The non-zero DC noise response of the conventional BP biquad and the zero DC noise response of the other two CDS-type biquads are verified. Note that the overall noise performance of the CDS BP biquad is the best. Furthermore, the theoretical S/N ratios of the BP biquads with respect to V_{n1} and V_{n2} are plotted in Figs.

3.18(a) and (b) respectively. The advantage of the CDS-type biquads over the conventional biquad is seen, although it is not as obvious as that illustrated for the first-order lowpass filters (Fig. 3.9). This is because of the low-frequency signal characteristic of the BP biquads (Fig. 3.16) and the effective

$C_1 = 5 \text{ pf}$
 $C_2 = 5 \text{ pf}$
 $a_{22}C_2 = 5 \text{ pf}$
 $a_{32}C_2 = 0.16667 \text{ pf}$
 $a_4C_1 = 5 \text{ pf}$
 $a_{05}C_2 = 1.6667 \text{ pf}$
 $f_0 = 32 \text{ KHz}$

Fig. 3.16 Frequency response of the biquads shown in Figs. 3.12(b) and 3.13 to signal input.

Fig. 3.18(a) Theoretical S/N ratio: V_{n1} Fig. 3.18(b) Theoretical S/N ratio: V_{n2}

frequency range of the CDS-type filters in noise reduction. As a result, the S/N ratio, at the low frequency range in particular, is not as outstanding as that observed in the first-order lowpass filters. The advantage of the CDS-type filters will be further verified in section 5.1 for lowpass biquads.

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CHAPTER 4

EXPERIMENTAL RESULTS

4.0 INTRODUCTION

In order to verify the theoretical results obtained from the z-transform and the exact analysis method, an integrated circuit test vehicle was laid out by Prof. M.A. Copeland, the thesis supervisor of the author. This chip was fabricated at General Electric Corporate Research and Development, Schenectady, New York. The test chip is capable of realizing the conventional filters and the CDS-type filters discussed in the last chapter. The frequency response of these filters to signal and noise inputs was investigated experimentally. A wide range of clock frequency (from 8 kHz to 128 kHz) has been used without difficulties. This chapter presents the experimental results and explains the discrepancies.

4.1 DESCRIPTION OF THE TEST CHIP

The test chip consists of capacitors, switches and pairs of source followers. For the purpose of this thesis, on-chip op amps have not been considered in order to minimize the design time and chip size. Instead, source-follower pairs acting as impedance transformers are used to interface off-chip op amps. The photomicrograph of the test chip is shown in Fig. 4.1. The top part of the chip implements a conventional high-Q bandpass biquad while the bottom part provides the capability to construct a first-order

Fig. 4.1 Photomicrograph of the test chip.

CDS-type filter. Different filter responses can be realized with the bottom part by choosing different values of capacitors. In addition, suitable connections are incorporated in the layout design so that the noninverting amplifier required in the CDS biquad realizations can be formed. The layouts of the two parts are separately shown in Fig. 4.2(a) and (b).

It should be remarked that for the first-order CDS lowpass filter, the two off-chip input switches required were obtained by using a quad analog switch chip (a MCl4066). Two more switches are needed for the offset-free LP filter to realize the feedback SC resistor.

4.2 PERFORMANCE OF THE LOWPASS FILTERS

The experimental results presented in this section are for the lowpass filters; each is constructed with a single test chip and additional ICs such as op amps (LF356) and switches (MCl4066). The resulting circuit diagrams are shown in Fig. 4.3. The DC gain of these filters is determined by the capacitor ratio C_2/C_3 . The

test chips and chips containing switches are powered by plus and minus five volt power supplies whereas the op amp chips are biased with plus and minus twelve volt supplies in order to avoid distortions due to early amplifier saturation caused by high signal input.

Fig. 4.3 First-order lowpass (LP) filters.
 (a) A conventional noninverting LP filter.
 (b) An inverting offset-free LP filter.
 (c) An inverting CDS LP filter.

4.2.1 SIGNAL RESPONSE OF LOWPASS FILTERS

The aim of the following demonstration is to prove the ability of the exact analysis method, which has been extensively used in this thesis. Fig. 4.4 illustrates the effect of signal feedthrough on the signal responses of inverting and noninverting CDS LP filters of Fig. 4.3(c). If the input $V_i(t)$ is continuous, a noninverting filter will sample and hold the input for half a period before the signal, which hence has been converted into a sampled-data signal, is coupled into the filter. The z-transform is thus adequate to predict the frequency response. On the other hand, the continuous input is directly coupled into the inverting filter during ϕ . One can easily visualize that a continuous

input can be represented by a pure sampled-data input $V_i^{SD}(t)$ and a continuous deviation function $d(t)$. The deviation function can simply be calculated as:

$$d(t) = V_i(t) - V_i^{SD}(t) \quad (4-1)$$

This deviation function is zero only at the sampling instants (i.e., the end of ϕ). During ϕ , it enhances the energy of the

output spectrum and causes a deviation from the z-transform frequency analysis. As shown in Fig. 4.4, the 3-dB point of the inverting filter (the top trace) is slightly higher than that of the noninverting filter. The exact analysis method, for arbitrary input, takes account of the signal feedthrough by using the

Fig. 4.4 Demonstration of the effect of feedthrough. The top trace is the signal response of an inverting CDS LP filter. The bottom trace is that of the noninverting counterpart. The 3-dB point of the latter is marked.

Fig. 4.5 Theoretical curves obtained from the exact analysis method show the effect of feedthrough in CDS LP filters.

transfer function matrices $H_{0,0}$, $H_{0,1}$, $H_{1,0}$, and $H_{1,1}$. Although

the effect observed is relatively small, it is carefully analyzed here to show that the exact analysis method does account for such detailed effects. The theoretical curves obtained via the exact analysis method are shown in Fig. 4.5 for comparison.

Fig. 4.6 shows the frequency response of the conventional noninverting LP filter (in Fig. 4.3(a)) to signal input. This filter is the noninverting lossy integrator from the conventional high-Q bandpass biquad ($Q = 30$) of the test chip, the values of capacitors used are fixed by the filter design of the biquad. The DC gain of this filter is 30. The measured frequency response was found to be in agreement with the theoretical one.

The measured frequency responses for the filters shown in Figs. 4.3(b) and 4.3(c) are given in Figs. 4.7(a) and 4.7(b) respectively. Both filters have a relatively low DC gain ($= 3$) in order to avoid amplifier saturation due to clock feedthrough. As expected, both curves are exactly the same. The measured signal response deviates from that predicted by the exact analysis method. The deviation of the theoretical curve from the experimental curve is illustrated in Fig. 4.8. It is found that the experimental filter's DC gain is lower while its corner frequency is higher. The discrepancy is explained by a capacitive coupling, C_{sf} , between the output and the inverting input terminal of the op amp due to a layout error. The basic building block of these filters, the CDS integrator, is sensitive to such coupling

$C_1 = 5 \text{ pf}$
 $C_2 = 5 \text{ pf}$
 $C_3 = 0.16667 \text{ pf}$
 $f_s = 32 \text{ KHz}$

Fig. 4.6 Frequency response of the conventional noninverting LP filter (in Fig. 4.3(a)) to signal input. The marker is at the 3-dB point.

(a)

$C_1 = 5 \text{ pf}$
 $C_2 = 5 \text{ pf}$
 $C_3 = 1.6667 \text{ pf}$
 $C_I = 5 \text{ pf}$
 $f_s = 32 \text{ kHz}$

(b)

Fig. 4.7(a) Frequency response of the offset-free LP filter (Fig. 4.3(b)).
 (b) Frequency response of the CDS LP filter (Fig. 4.3(c)).
 The markers point to the DC gain and the 3-dB point respectively.

Fig. 4.8 Theoretical and measured responses of the filters shown in Figs. 4.3(b) and (c).

because, in conjunction with the initializing capacitor C_I , it reduces the effective gain (discussed in section 3.2.2) of the composite amplifier (defined in section 1.4.2) during the active phase ϕ . Fig. 4.9(a), which is a partial layout of the test chip, focuses on the layout error attributing to the stray capacitance, C_{sf} . The stray capacitance, as shaded in Fig. 4.9(a), is due to the crossing of two interconnecting lines - a metal line over a polysilicon underpass. The absolute location of the error is circled on the photomicrograph of the chip shown in Fig. 4.1.

The fact that the deviation is due to the effective gain being finite can be more specifically established by writing the charge-conservation equation at the "virtual ground" (or the integrating node) of the filters, shown in Figs. 4.3(b) and (c). The final form of the signal transfer function is:

$$\frac{V_o}{V_i}(z) = \frac{-\frac{a}{2}}{1 + \frac{a}{3} \left[1 + \frac{1}{A} \left(1 + \frac{1}{\frac{a}{3}} + \frac{1}{\frac{a}{3}} \right) \right] - z \left(1 + \frac{1}{A} \right)} \quad (4-2)$$

where A is the effective gain.

If A is infinite, Eq. 4.2 gives the ideal transfer function.

$$\frac{V_o}{V_i}(z) = \frac{-\frac{a}{2}}{1 + \frac{a}{3} - z} \quad (4-3)$$

Fig. 4.9(a) The stray capacitance C_{sf} .

- (b) The CDS LP filter.
 (c) Equivalent active-RC filter of (b).

From Eq. 4.2, the actual DC gain and the actual location of the real pole can be calculated.

The actual DC gain

$$G_{\text{act.}} = \frac{-\frac{a_2}{2}}{a_3 \left[1 + \frac{1}{A} \left(1 + \frac{a_2}{a_3} \right) \right]} \quad (4-4)$$

is indeed smaller than the ideal DC gain $(-a_2/a_3)$.

The actual pole location is

$$z_{\text{act.}} = \frac{1}{1 + \frac{1}{A}} \quad (4-5)$$

$$1 + a_3 \left[1 + \frac{1}{A} \left(1 + \frac{a_2}{a_3} \right) \right]$$

whereas the ideal pole location is

$$z_{\text{id.}} = \frac{1}{1 + \frac{a_2}{a_3}} \quad (4-6)$$

It is easy to prove algebraically that the value of $z_{\text{id.}}$ is greater

than that of $z_{\text{act.}}$. Recall that the relation between the s-plane

poles and the corresponding z-plane poles is given by $z_p = \exp(s_p T)$

where s_p is the location of a s-plane pole. According to this

relation, the corresponding s-plane pole of z_{act} is located

further away from the origin than that of z_{id} . Therefore the

corner frequency of the experimental filter is expected to be higher as demonstrated in the measured frequency response.

The circuit diagram of the CDS LP filter including the parasitic coupling capacitor C_{sf} is shown in Fig. 4.9(b).

Clearly, the effective gain during ϕ_2 is C_I / C_{sf} . Detailed

investigation reveals that since C_I and C_{sf} absorb charge on ϕ_2

and discharge on ϕ_1 , they are acting as SC resistors. The active-

RC equivalent of Fig. 4.9(b) is shown in Fig. 4.9(c). The size of C_{sf} was estimated experimentally and theoretically using the

technique given by Yuan and Trick [37]. Its value falls in the range from 0.02 to 0.03 pf. Since C_I is a 5 pf capacitor, the

effective gain during ϕ_2 is from 167 to 250. The experimental

curve and the theoretical curve corresponding to the effective gain equal to 180 is shown in Fig. 4.10. Note that the theoretical curve is obtained from the exact analysis.

4.2.2 NOISE PERFORMANCE OF LOWPASS FILTERS

The noise spectra at the output of the conventional and CDS LP filters of Fig. 4.3(a) and (c) with input grounded are shown in

Fig. 4.10 Theoretical response with effective gain equal 180 and measured response of the filters in Figs. 4.3(b) and (c).

Figs. 4.11(a) and (b), respectively. The $1/f$ noise spectrum and the wideband noise spectrum of the op amp are clearly displayed in Fig. 4.11(a). The success of the initializing technique adopted in CDS-type filters is evident from Fig. 4.11(b): the $1/f$ noise spectrum has disappeared.

To better substantiate the advantages of the CDS technique, the frequency responses of the testing filters (in Fig. 4.3) to noise were studied experimentally by applying a bandlimited white noise source to the noninverting input terminal of the op amp, through the source follower. Such a bandlimited noise source allows simple noise analysis and validates the application of Eq. (3-8) in this thesis work. Aliasing due to under-sampling can be neglected completely. A qualitative discussion concerning particularly the negligence of $1/f$ foldback effects will be given in section 5.1. The experimental and theoretical results for both the noise and signal responses of the high gain/conventional filter are shown in Figs. 4.12(a) and (b) respectively. The upper traces in the two figures show the noise responses while the bottom traces show the signal responses. The corresponding curves match closely. For the same magnitude of signal and noise inputs, the filter is seen to be more sensitive to the noise than to the signal.

Theoretical curves showing the responses of the CDS-type filters to signal and noise inputs are given in Fig. 4.13. The curves labelled I and II show the theoretical signal and noise responses respectively. The corresponding experimental results are given in Fig. 4.14 for the offset-free (in Fig. 4.14(a)) and

(a)

$C_1 = 5 \text{ pf}$
 $C_2 = 5 \text{ pf}$
 $C_3 = 0.16667 \text{ pf}$
 $f_c = 32 \text{ kHz}$

(b)

Fig. 4.11 Noise output spectra of (a) the conventional LP filter (in Fig. 4.3(a)) and (b) the GDS LP filter (in Fig. 4.3(c)), with input node grounded.

(a)

(b)

Fig. 4.12(a) Signal and noise responses of the conventional filter.

(b) The corresponding theoretical curves.

Fig. 4.13 Theoretical signal and noise responses of the offset-free and CDS LP filters.

(a)

(b)

Fig. 4.14(a) Signal and noise responses of the offset-free LP filter (Fig. 4.3(b)).

(b) Signal and noise responses of the CDS LP filter (Fig. 4.3(c)).

The markers are at the 3-dB points.

the CDS (in Fig. 4.14(b)) LP filters. Significant noise reduction from the CDS-type filters is obvious by comparing Fig. 4.12 and Fig. 4.14, even though the corresponding filter characteristics are different because of different values of C_3 . In Fig. 4.12(a),

it is seen that the noise response of the conventional LP filter is 1 or 2 dB above its signal response whereas the noise response of the CDS-type LP filters, shown in Fig. 4.14, is at least 10 dB below its signal response, up to the 3-dB point. Theoretically, the noise response of the offset-free filter at DC is minus infinity and the S/N ratio at the 3-dB point (i.e., $f_c = 1580$ Hz) is about 20 dB (Fig. 3.7), but the experimental results show that noise reduction at DC is about -30 dB and the S/N ratio at the 3-dB point is only 10 dB. The deviations are believed due to the combination of the effects of finite effective gain and parasitic capacitive coupling. According to [4], if the noninverting input of an op amp is not connected to a constant voltage, the filter becomes sensitive to all the parasitic capacitances due to switches and substrate that are connected to the inverting input. The theoretical curve accounting for the effective gain is shown in Fig. 4.15. The deviation after 200 Hz may be due to the parasitic coupling. The experimental noise response of the CDS LP filter is quite different from its theoretical response. Over the first 1.5 KHz, a notch filter response is apparent (see Fig. 4.14(b)). However, the overall noise performance of the filter is better than the theory predicted. The deviation is explained by the existence of parasitic feedthrough paths to the amplifier output. For example, one of these parasitic feedthrough paths is

Fig. 4.15 Theoretical noise response corresponds to the effective gain equal 180 and measured response for the offset-free LP filter of Fig. 4.3(b).

$C_1 = 5 \text{ pf}$
 $C_2 = 5 \text{ pf}$
 $C_3 = 1.6667 \text{ pf}$
 $C_4 = 5 \text{ pf}$
 $f_{\text{clock}} = 8 \text{ kHz}$

—voltage output due to clock feedthrough

0.2^V/div.

50^{uSec.}/div.

50^{mV}/div.

50^{uSec.}/div.

$\phi_2 \mid \phi_1 \mid \phi_2$

Fig. 4.16 Demonstration of the effect of the clock feedthrough cancellation circuit. The upper square wave is the output waveform due to clock feedthrough and the initializing operation. The lower trace is the output waveform with the clock feedthrough cancellation circuit.

believed to be through C_{sf}. These extra noise output components

have their own frequency responses and phase characteristics, which are different from those of the expected output. According to the picture, at frequencies around 600 Hz, the phase of the ideal-case (i.e., no parasitic feedthrough path) noise output and the resultant phase of the additional noise outputs is opposite in phase while their magnitudes are equal, thus causing the notch. Note that the experimental S/N ratios are not plotted since the performance of the CDS-type filters has been degraded by the layout error.

The clock feedthrough cancellation circuit was found to be very effective as shown in Fig. 4.16 for the single-ended output differential input CDS LP filter (Fig. 3.10). It can provide about 20 to 40 dB offset reduction depending on the match of the two halves connected to the input terminals of the op amp.

4.3 PERFORMANCE OF THE BANDPASS BIQUADS

The circuit diagrams of the three bandpass biquads discussed in chapter 3 are given in Fig. 4.17. Fig. 4.17(a) shows a conventional biquad which is present on the test chip. The CDS biquad of Fig. 4.17(b) requires three test chips to realize while the offset-free biquad of Fig. 4.17(c) developed from the CDS biquad needs four additional switches. Of course, off-chip op amps are also required.

Since the switch arrangements of these SC biquads, except the

(a)

(b)

Fig. 4.17 (a) The conventional bandpass biquad.
 (b) The CDS bandpass biquad.

(c)

$$C_1 = 5 \text{ pf}$$

$$C_2 = 5 \text{ pf}$$

$$C_5 = a_{c5} C_2 = 1.6667 \text{ pf}$$

$$C_{R2} = a_{22} C_2 = 5 \text{ pf}$$

$$C_{R3} = a_3 C_2 = 0.16667 \text{ pf}$$

$$C_{R4} = a_4 C_1 = 5 \text{ pf}$$

(d)

Fig. 4.17(c) The offset-free bandpass biquad.
(d) The capacitor values.

SC resistor C_{R3} , employ LDI timing, they approximate closely to their active-RC equivalent. Therefore knowledge of the RC biquad can be applied to the SC biquads. To obtain a finite Q-factor, the two integrator loop of these biquads must be damped. This is achieved by the lossy integrator. Often the RC time constants of the two integrators are made to be the same in order to simplify the design procedure. The resonant frequency is then the reciprocal of this unique time constant. Owing to this simplification, the resonant frequency of SC biquads is determined by the capacitor ratio C_{R2}/C_{R3} , the Q-factor is equal to the capacitor ratio C_{R2}/C_{R3} , and the gain peak is a product of capacitor ratios (i.e., $C_{R5}C_{R4}/(C_{R1}C_{R3})$). Approximate characteristics of these SC filters can be obtained simply from the knowledge of the RC biquad. However, either the z-transform analysis or the exact analysis method must be used to get the exact filter characteristics.

4.3.1 SIGNAL RESPONSE OF BANDPASS BIQUADS

Fig. 4.18 illustrates the measured and theoretical responses of the filter shown in Fig. 4.17(a) to signal input. The two curves match quite closely. Also included in the figure is the output noise spectrum with input node grounded. Theoretical and experimental curves showing the signal responses of the other two novel biquads (in Figs. 4.17(b) and (c)) are given in Figs.

Fig. 4.18 Signal response of the conventional bandpass biquad (in Fig. 4.17(a)).

Fig. 4.19(b) Signal response of the offset-free bandpass biquad (in Fig. 4.17(c)).

Fig. 4.19(a) Signal response of the CDS bandpass biquad (in Fig. 4.17(b)).

4.19(a) and (b) respectively. The bottom trace in each figure is the corresponding output noise spectrum. As expected, the measured signal responses of the CDS biquad and the offset-free biquad are exactly the same. The curves indicated that the actual resonant frequency is increased, the actual Q-factor is decreased, and the peak gain is lowered. The deviations are believed due to finite effective gain of the composite amplifier. This can be verified from the transfer function taking into account finite gain. However, this calculation is quite tedious for a second-order filter. Since the effect of finite effective gain on the signal response has been modelled successfully for a first-order lowpass filter, the conjecture should be accurate.

4.3.2 NOISE PERFORMANCE OF BANDPASS BIQUADS

The noise response was again measured by applying a band-limited white noise source to the noninverting input terminal of an op amp through the source follower. The noise source was connected indirectly to each op amp of the two-integrator biquads. The noise response at the bandpass output node corresponding to each location of the noise source was measured respectively. Fig. 4.20 shows the noise responses of the filter in Fig. 4.17(a). It is observed that the conventional bandpass biquad is more sensitive to the noise of the noninverting lossy integrator (i.e., V_{n2}). Furthermore, the noise is amplified, especially at the resonant frequency. The theoretical and experimental results are consistent.

Fig. 4.20 Noise responses of the conventional bandpass biquad in Fig. 4.17(a).

The noise responses of the CDS and offset-free biquads are shown in Figs. 4.21(a) and (b) respectively. A highpass noise response is evident. The noise reduction due to the initializing technique at low frequencies is clearly shown for the two filters, as compared to the noise responses of the conventional bandpass biquad. Both filters reduce the noise associated with the inverting and noninverting integrator by more than 15 dB and 30 dB at DC, respectively. The noise performance at DC should be estimated by extrapolating the experimental curves. In addition, the peak gain of the noise responses are lower by about 15 dB compared with that for the conventional biquad. Again, the noise response shows that the filter performance suffer from the effect of finite gain, particularly at DC. Of course, other contribution due to parasitic coupling discussed in section 4.2.2 should be considered as well. Again, the experimental S/N ratios have not been plotted for the same reason given above.

4.4 SUMMARY

The discussion to the present assumes that the op amps have sufficiently wide bandwidth. This is a reasonable assumption as the frequencies of signal and noise inputs and clock frequency are much lower than the unity-gain bandwidth of the op amps (5 MHz). The clock feedthrough cancellation circuit is found to be effective. Furthermore, the exact analysis is shown to be an important tool in SC network analysis.

Although the filters constructed with the CDS integrator(s)

Fig. 4.21(a) Noise responses of the CDS bandpass biquad in Fig. 4.17(b).

Fig. 4.21(b) Noise responses of the offset-free bandpass biquad in Fig. 4.17(c).

suffered from a layout error, the noise reduction capability in the low-frequency range is established. A significant reduction is expected from these filters as verified by the exact analysis. Regarding the overall noise performance, the CDS lowpass filter and the CDS bandpass biquad with novel feedback SC resistor(s) are better than their offset-free counterparts. Since the SC filters are sampled-data filters, the response to noise can be varied by changing the sampling rate. One can increase the clock rate to extend the noise-reduced frequency range, and make use of the extended region for signal processing applications.

CHAPTER 5

DISCUSSION AND CONCLUSION

5.1 DISCUSSION

The theoretical and experimental results for the first-order lowpass filters and the second-order bandpass filters have been presented in chapters 3 and 4. The use of the new topology in filtering applications has been established. Although the performance in noise reduction is degraded by a layout error on the test chip, the utility of the new topology is verified.

It should be remarked that the investigation of noise performance has been done in such a way that aliasing can be neglected. That is, the experimental white noise generator was bandlimited to less than or equal to half of the sampling clock frequency. In reality, the $1/f$ foldback effects must be considered: for example, in a biquad. The noise-reduced components of the $1/f$ noise over the Nyquist frequency, from the previous op amp stage, can be aliased back into the passband by the sampling of the following stage. In order to avoid the $1/f$ foldback noise, the sampling rate must be sufficiently high. Since the typical corner frequency of the $1/f$ noise is about 10 kHz, the minimum sampling rate for the new topology should be above 20 kHz to diminish the $1/f$ aliasing effect.

The notable feature in the CDS and offset-free biquads is the extra op-amp stage. This stage is required because of the need to hold the output of the previous integrator for half a period in

order to meet the requirement for LDI timing. An op amp usually occupies a large chip area, consumes power, and is a source of noise. The schematic diagram of a modified offset-free bandpass biquad is shown in Fig. 5.1. The extra op-amp stage is replaced by a parasitic-compensated SC resistor [38] which is the structure shown inside the dashed box. The discussion of the structure has been presented in [38]. This structure requires the capacitor ratio a to be doubled and the parasitic capacitances, as shown

22
in the diagram, associated with nodes (1) and (2) to be equal. To guarantee that the parasitic capacitances are equal, one must ensure that the routings associated with the two nodes match and that equal sized switches are used in the layout. The modified CDS bandpass biquad can also be obtained by removing the circled switch pairs shown in Fig. 5.1. Noted that the parasitic-compensated SC resistor has been successfully used by Nair [39] in his novel biquad realization.

It should be remarked that the amplifier initializing technique proposed in this thesis has recently been incorporated in a novel dynamic amplifier design for SC filters [39]. The initializing capacitor C_I and the shorting switch are used in a different context - to remove the high threshold voltage requirement of the active transistor [39].

The new technique for suppressing DC offsets caused by clock feedthrough has been tried and found to be useful. In addition, the balanced nature of the circuit should improve the power supply

Fig. 5.1 A modified schematic of the offset-free bandpass biquad (in Fig. 4.17(c)).

rejection as the power supply noise from the substrate (i.e., V_{SS}) appears at both inputs of the op amp. The major disadvantage of this circuit is that the area occupied by the capacitors and switches is doubled. However, even with this drawback, the technique is considered to be useful in some critical applications in which output offset error is stringent.

To conclude this section, the specific aspects accomplished by the author in this thesis are as follows. First, the CDS-type offset-free filters have been derived from the corresponding CDS filters which were contributed by Prof. M.A. Copeland. In addition, a letter consisting of the analytical and experimental results of the first-order offset-free lowpass filter had been submitted by the author and was published recently [40]. Second, the exact analysis method developed by Brglez has been extensively used in noise-performance study. To the knowledge of the author, such a use of the method has not been reported elsewhere. Last, a new offset-free biquad providing continuous output has been developed, as will be discussed in the following section.

5.2 PROPOSAL FOR AN IMPROVED BIQUAD

According to the s-domain results summarized in Table (C-1) of Appendix C, the output of the lossy integrator in the general active-RC biquad is shown to realize either lowpass (LP), highpass (HP), bandpass (BP), or notch-filter characteristics while the output of the nonlossy integrator does not have this flexibility. Based on the results in Table (C-1) and the following analysis, a

new input offset-free biquad which does not require the parasitic-compensated SC resistor is developed. Later, a new lowpass-type input offset-free biquad is shown in Fig. 5.3 as an example.

At DC, all capacitors are neglected from the general active-RC biquad shown in Fig. C.1 of Appendix C. The noise transfer functions for the lossy integrator can be determined by the following classical block diagram approach. The block diagrams are shown in Fig. 5.2, and the corresponding noise transfer functions are:

$$\frac{V_2}{V_{n1}}(W=0) = \frac{(A_1)(A_2)\left(-\frac{R_3}{R_2}\right)}{1 - (A_1)(A_2)\left(-\frac{R_3}{R_2}\right)(B)\left(-\frac{R_1}{R_4}\right)} \quad (5-1)$$

$$\frac{V_2}{V_{n2}}(W=0) = \left(1 + \frac{R_3}{R_2}\right) \frac{1}{1 - (A_1)(A_2)\left(-\frac{R_3}{R_2}\right)(B)\left(-\frac{R_1}{R_4}\right)} \quad (5-2)$$

where

A and B are used to indicate the location of the loop inversion. A is the open-loop gain of the first op amp, OAl.

Fig. 5.2 Block diagrams derived from Fig. C-1 for V_2 .

The inputs are the input-referred noise voltages of the op amps (i.e., V_{n1} or V_{n2}).

Assuming the open-loop gain of the op amp is infinite, then

$$\frac{V_2}{V_{n1}}(W=0) = -\frac{1}{B} \left(1 + \frac{R_4}{R_1}\right) \quad (5-3)$$

$$\frac{V_2}{V_{n2}}(W=0) = 0 \quad (5-4)$$

According to Eqs. (5-3) and (5-4), the output of the lossy integrator is free from its own amplifier offset, V_{n2} . Furthermore, if the non-lossy integrator has no input-referred offset (i.e., $V_{n1} = 0$), the output of the lossy integrator is completely free of amplifier input offsets. Therefore, a CDS integrator should be employed to replace the continuous non-lossy integrator for the SC realization. As a demonstration, such a new lowpass biquad is shown in Fig. 5.3. Note that the lossy integrator is a conventional type. The advantage of this biquad is that its output (i.e., V_2) is "continuous", unlike the comb-shaped output of CDS filters.

The theoretical signal and noise transfer functions, V_{LP}/V_i , LP

V_{LP}/V_{n1} and V_{LP}/V_{n2} , of the various lowpass biquads are shown in

Fig. 5.4 and Figs. 5.5(a) and (b), respectively. Again, the expected highpass noise response of the CDS-type filters is seen from the figures. The theoretical S/N ratios for the four types

Fig. 5.3 A two-amplifier offset-free continuous output lowpass biquad which is composed of a CDS integrator and a conventional integrator.

Fig. 5.4 Signal response: V_{LP}/V_1

Fig. 5.5(a) Noise response: V_{LP}/V_{n1}
 where V_{n1} is the input-referred noise of op amp #1 (OA1).

Fig. 5.5(b) Noise response: V_{LP}/V_{n2}
 where V_{n2} is the input-referred noise of op amp #2 (OA2).

(a)

(b)

Fig. 5.6(a) Theoretical S/N ratio: V_{n1}

(b) Theoretical S/N ratio: V_{n2}

of lowpass (LP) biquads are shown in Fig. 5.6. Although the noise performance of the new offset-free LP biquad discussed above is not as good as that of the CDS LP biquad, it is comparable to that of the CDS-type offset-free LP biquad. Furthermore, its performance is better than that of the conventional LP biquad. It should be emphasized again that the output of the new biquad is continuous.

5.3 CONCLUSIONS

A novel switched-capacitor topology, which uses the act of initialization (i.e., shorting the output of the amplifier back to the input) as a means of reducing offset and low frequency noise in the amplifier, has been studied analytically and experimentally in filtering applications. Despite the fact that the noise performance of the filters is degraded due to a layout error, the goal of noise reduction is demonstrated. Since the $1/f$ noise, which is a dominant noise source in SC filters, concentrates in the low frequency range, it will be much reduced by the initializing technique. A significant improvement of S/N ratio is thus achieved. The basic building block, being parasitic-free and amplifier input offset-free, can be used to realize higher order filters. Furthermore, SC circuits which are free from amplifier input offset can be constructed. The same technique can be used also for D/A converters, where offset can be very important.

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APPENDIX A

DERIVATIONS OF INTEGRATOR TRANSFER FUNCTION WITH OP AMP GAIN

If the op amp gain (A_o) of the "parasitic-free" inverting integrator of Fig. 2.1(a) is finite, the charge-conservation equation at the end of Δt is:

$$C[V_o(n) - (V_o(n-1) + V_o(n-1)/A_o) + V_o(n)/A_o] + aC[V_i(n) + V_o(n)/A_o] + aC V_o(n)/A_o = 0 \quad (A1)$$

Rearranging Eq. (A1),

$$V_o(n) - V_o(n-1) - V_o(n-1)/A_o + V_o(n)/A_o + aV_o(n)/A_o + aV_o(n)/A_o = -aV_i(n) \quad (A2)$$

Taking the z-transform of both sides:

$$V_o(z)[(1 - z^{-1})(1 + 1/A_o) + (a + a_p)/A_o] = -aV_i(z) \quad (A3)$$

Thus the actual transfer function of the inverting integrator is:

$$H_{act.}(z) = \frac{V_o}{V_i}(z) = \frac{-a}{(1 - z^{-1})(1 + 1/A_o) + (a + a_p)/A_o} \quad (A4)$$

Obtaining the ideal transfer function by letting $A_o \rightarrow \infty$ gives:

$$H_{id.}(z) = \frac{V_o}{V_i}(z) = \frac{-a}{(1 - z^{-1})} \quad (A5)$$

Eq. (A4) is expressed in the form as Eq. (A5) to find the actual gain and pole location due to finite op amp gain. Eq. (A4) becomes:

$$H_{act.}(z) = \frac{-a}{[1 + (1 + a + a_p)/A_o] - (1 + 1/A_o)z^{-1}}$$

$$= \frac{-G'}{1 - P'z^{-1}} \quad (A6)$$

where the actual gain

$$G' = \frac{a}{1 + (1 + a + a_p)/A_o} \quad (A6a)$$

and the actual pole

$$P' = \frac{1 + 1/A_o}{1 + (1 + a + a_p)/A_o} \quad (A6b)$$

The gain error is

$$G^* = 1 - G'/a = \frac{1 + a + a_p}{A_o + (1 + a + a_p)} \quad (A6c)$$

and the pole error is

$$\begin{aligned}
 p^* &= 1 - p' = 1 - \frac{1}{1 + [(a + a_p)/A_o]/(1 + 1/A_o)} \\
 &= \frac{a + a_p}{A_o} \quad (A6d)
 \end{aligned}$$

Using the same analytic procedure on the noninverting integrator of Fig. 2.1(b), the actual transfer function is calculated as:

$$H_{act.}(z) = \frac{z^{-1}}{(1 - z^{-1})(1 + 1/A_o) + (a + a_p)/A_o} \quad (A7)$$

$$H_{id.}(z) = \frac{z^{-1}}{1 - z^{-1}} \quad (A8)$$

The error equations are easily verified to be the same as those previously derived.

APPENDIX B

AN EXAMPLE OF EXACT ANALYSIS METHOD

Procedures required to determine matrices F , F_k , G , and G_k

for the exact analysis method are as follows:

- (1) Assign a polarity to the voltage across each capacitor in the SC network and determine the entries of each matrix according to the sign convention.
- (2) Fill in F_k columnwise by evaluating the voltages across the capacitors due to a single unit-valued initial condition (i.e., no voltage across all the capacitors except the one being considered) with the input(s) shorted to ground, for every switched state, k .
- (3) Fill in G_k columnwise by evaluating the voltages across the capacitors due to a single unit-valued input for zero-valued initial condition (i.e., no voltage across all capacitors), for every switched state, k .

Obviously, F_k is a $N \times N$ matrix while G_k is a $N \times R$ matrix, where

N is the number of capacitors in the SC network and R is the number of independent voltage sources.

These procedures are applied to the CDS LP filter of Fig. 3.4 as an example. Fig. 3.5(a) is reproduced in Fig. B.1 for convenience. The definitions of variables are given in Fig. 3.5(b). State 0 is defined as the switched state during which

$$\begin{bmatrix}
 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0
 \end{bmatrix}$$

F_0

$$\begin{bmatrix}
 0 & 1 \\
 0 & 0 \\
 0 & 1 \\
 0 & 0 \\
 0 & 1 \\
 0 & 1 \\
 0 & 0 \\
 0 & 0
 \end{bmatrix}$$

G_0

$$\begin{bmatrix}
 1 - \frac{c}{s} & 1 - \frac{c}{s} \\
 1 - \frac{c}{s} & -\frac{c}{s} \\
 -\frac{(a+1)c}{s} & x - \frac{c}{s} \\
 -\frac{(a+1)c}{s} & x - \frac{c}{s} \\
 -\frac{ac}{s} & x \\
 -\frac{ac}{s} & 0 \\
 -\frac{ac}{s} & x \\
 -\frac{c}{s} & -\frac{c}{s}
 \end{bmatrix}$$

G_1

$$\begin{bmatrix}
 1 & \frac{c}{s} & \frac{d}{s} & \frac{e}{s} & 0 & 0 & 0 & \frac{f}{s} \\
 1 & \frac{c}{s} & \frac{d}{s} & \frac{e}{s} & 0 & 0 & 0 & \frac{f}{s} \\
 -b & \frac{(a+1)c}{s} & \frac{(a+1)d}{s} & \frac{(a+1)e}{s} & 0 & 0 & 0 & \frac{(a+1)f}{s} \\
 -b & \frac{(a+1)c}{s} & \frac{(a+1)d}{s} & \frac{(a+1)e}{s} & 0 & 0 & 0 & \frac{(a+1)f}{s} \\
 -b-1 & \frac{ac}{s} & \frac{ad}{s} & \frac{ae}{s} & 0 & 0 & 0 & \frac{af}{s} \\
 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\
 -b-1 & \frac{ac}{s} & \frac{ad}{s} & \frac{ae}{s} & 0 & -1 & 0 & \frac{af}{s} \\
 1 & \frac{c}{s} & \frac{d}{s} & \frac{e}{s} & 0 & 0 & 0 & \frac{f}{s}
 \end{bmatrix}$$

F_1

Fig. B.1 Switching and feedthrough matrices of the inverting CDS LP filter shown in Fig. 3.4.

ϕ_1 is high and ϕ_2 is low. The first column of F_0 is evaluated by

applying step 2: shorting V_1 and V_n to ground and assuming no voltage in other capacitors except the capacitor, C_1 (see Fig.

3.4). During state 0, since the positive input is grounded and since both plates of C_1 are at ground potential, C_1 is discharged.

This results in zero entries in the first column (or nodal voltage vector). The entries of the fourth column are the result of capacitor C_4 being disconnected from the filter during ϕ_1 , thus

not affecting the other capacitors. The second column of G_0 is

evaluated by applying step 3 instead: shorting V_1 to ground and considering no charge on all capacitors. The entries of the column are due to the unit-valued noise voltage (V_n) which are easily obtained by inspection. Similar procedures are applied to evaluate the F_1 and G_1 matrices of State 1 (ϕ_1 is low and ϕ_2 is

high). The derivations of the third column of F_1 and G_1 , which are rather complex, are given in the following calculations. Note that the effective gain of the compositive amplifier is considered to be finite in the derivation.

The third column of the F_1 matrix is evaluated by considering

the charge (Q) stored on C_3 only.

$$Q = V \times C_3 \quad \text{where } V \text{ is equal to 1 (step 2)}$$

With reference to Fig. 3.4, this charge is shared by C_2 , C_4 and C_8

according the following equation.

$$Q = -V'(C_2 + C_8) + (V_{c5} - V')(C_3 + C_4) \quad (B1)$$

where

$$V' = -V_{c5} / A$$

and

$$A = C_1 / C_{sf}$$

Substituting Q and V' into Eq. (B1) gives:

$$C_3 = V_{c5} [(C_2 + C_8)/A + (1 + 1/A)(C_3 + C_4)] \quad (B2)$$

and thus

$$V_{c5} = AC_3 / [C_2 + C_8 + (A+1)(C_3 + C_4)] \quad (B3)$$

From Fig. 3.4, it is seen that

$$V_{c3} = V_{c4} = V_{c5} - V' = V_{c5} (1 + 1/A)$$

Therefore

$$V_{c3} = V_{c4} = (A+1)C_3 / [C_2 + C_8 + (A+1)(C_3 + C_4)] \quad (B4)$$

Also by the sign convention shown,

$$\begin{aligned}
 V_{c2} &= -V' = V_{c5} / A \\
 &= C_3 / [C_2 + C_8 + (A + 1)(C_3 + C_4)] \quad (B5)
 \end{aligned}$$

The rest of the entries are found with respect to the circuit configuration of state 1. The above calculated nodal voltages can be applied to column 2, 4, and 8.

Next, the first column of G_1 (due to a signal input (V_1)) is

determined by writing a charge-conservation equation at the virtual ground of the composite amplifier:

$$(V_1 - V')C_2 - V'C_8 + (V' - V')(C_3 + C_4) = 0 \quad (B6)$$

Substituting $V' = -V_{c5} / A$ and $V_1 = 1$ volt, V_{c5} is calculated as:

$$V_{c5} = -AC_2 / [C_2 + C_8 + (1 + A)(C_3 + C_4)] \quad (B7)$$

Again $V_{c3} = V_{c4} = (1 + 1/A)V_{c5}$

$$= -[(1 + A)C_2] / [C_2 + C_8 + (1 + A)(C_3 + C_4)] \quad (B8)$$

Also according to the circuit diagram and the sign convention:

$$\begin{aligned}
 V_{c2} &= V_1 - V' = 1 + V_{c5} / A \\
 &= 1 - C_2 / [C_2 + C_8 + (1 + A)(C_3 + C_4)] \quad (B9)
 \end{aligned}$$

Note that $V_{c1} = V_{c8} = -V'$

$$= -C_2 / [C_2 + C_8 + (1 + A)(C_3 + C_4)] \quad (B10)$$

Similarly, the second column of G_1 (due to the unit-valued noise voltage (V_n)) is determined by writing the charge-conservation equation at the virtual ground of the composite amplifier:

$$\begin{aligned} -V'(C_2 + C_8) + (V_{c5} - V')(C_3 + C_4) + (V_n - V')C_1 &= 0 \\ \Rightarrow V'(C_1 + C_2 + C_3 + C_4 + C_8) &= V_n C_1 + V_{c5} (C_3 + C_4) \end{aligned}$$

Letting $C_T = C_1 + C_2 + C_3 + C_4 + C_8$, then

$$V' = [V_n C_1 + V_{c5} (C_3 + C_4)] / C_T \quad (B11)$$

The charge-conservation equation at the virtual ground of the op amp is:

$$(V_{c5} - V_n)C_{sf} + (V' - V_n)C_1 = 0 \quad (B12)$$

Substituting Eq. (B11) into Eq. (B12) to eliminate V' and letting V_n equal one.

$$\begin{aligned} V_{c5} &= \frac{[C_T (C_3 + C_4) - C_1^2]}{C_T C_{sf} + C_1 (C_3 + C_4)} \\ &= x \end{aligned} \quad (B13)$$

V_{c2} and V_{c8} are the same as shown in the circuit diagram and are

calculated by substituting Eq. (B13) into Eq. (B11) and by letting V_n equal one.

$$\begin{aligned}
 V_{c2} &= V_{c8} = -V' \\
 &= - \left[\frac{C_1}{C_T} + \left(\frac{C_3 + C_4}{C_T} \right) x \right] \quad (B14) \\
 &= -y
 \end{aligned}$$

Note that according to Fig. 3.4, $V_{c1} = 1 - V'$ and

$V_{c3} = V_{c4} = V_{c5} - V'$, which are calculated by using Eq. (B13)

and Eq. (B14) as:

$$V_{c1} = 1 - y \quad (B15)$$

$$V_{c3} = V_{c4} = x - y \quad (B16)$$

Repeating the above steps, the switching and feedthrough matrices can be derived successfully, as shown in Fig. B.1. These matrices are then used to calculate the closed-form transfer function matrix, $T(W)$:

According to Eqs. (3-8) and (3-8a-d) in section 3.2.2, the evaluation of $T(W)$ for a particular frequency requires the transfer function matrices ($H_{0,0}$, $H_{0,1}$, $H_{1,0}$, and $H_{1,1}$) to be calculated for that particular frequency. The calculation in turn

requires the inversion matrix $[I - z^{-1} \begin{smallmatrix} -1 & -1 \\ 0 & 0 \end{smallmatrix}]$ which is also a

function of frequency. In particular, the inversion matrix must be obtained for every frequency of interest. The evaluation of the inversion matrix for each frequency becomes tedious and time-consuming, even with the aid of a computer, when the order of the SC filter increases. As a result, a software tool called MACSYMA was used to calculate the general inversion matrix, and the general transfer function matrices subsequently (Eqs. (3.8a - 3.8d)). These calculations are needed to be done once only. Finally, a program written in Fortran by the author was used to calculate the closed-form transfer function matrix (see Eq. 3-8).

MACSYMA is a large computer programming system written in LISP used for performing symbolic as well as numerical mathematical manipulations. It is developed by the Mathlab Group of the MIT Laboratory for Computer Science [41]. In this thesis work, it was explicitly used to do matrix calculations symbolically - multiplication, addition, subtraction, and inversion. The detail of these matrix manipulations should be referred to sections 2.8 and 6.4 of the MACSYMA Reference Manual.

APPENDIX C ANALYSIS OF A GENERAL STATE-VARIABLE BIQUAD

A general active-RC biquad is shown in Fig. C.1. It has the capability of realizing all two-pole filters by removing one or two of the feed forward path(s). The symbols A, B, E and F are used in the s-domain analysis to yield informations concerning the SC equivalents.

An inversion must be incorporated in the two-integrator loop for the biquad to be stable. The possible locations are shown with the symbols A and B. The values of A and B can be 1 or -1. Since only one inversion is required, either A or B is equal to -1 depending on where the inversion occurs. Furthermore, E and F can take on either 1 or -1 to indicate whether or not the input signal is inverted. The input signal is inverted in the biquad to avoid feedthrough. Applying the KCL at the summing nodes of amplifiers OA1 and OA2 gives the following signal and noise transfer functions for the corresponding amplifier outputs (i.e., V_1 and V_2).

$$\frac{V_1(s)}{V_1} = \frac{s \left(\frac{BC}{C C R} - \frac{E}{C R} \right) + \frac{BF}{C C R R} - \frac{E}{C C R R}}{D(s)} \quad (C1a)$$

$\begin{matrix} BC & & E & & BF & & E \\ 5 & & & & & & \\ s \left(\frac{C C R}{1 2 4} - \frac{C R}{1 1} \right) + \frac{C C R R}{1 2 4 5} - \frac{C C R R}{1 2 1 3} \end{matrix}$

Fig. C-1 The schematic of a general active-RC biquad.

$$\frac{V_1}{V_{n1}}(s) = \frac{s^2 + s \left(\frac{1}{CR_{11}} + \frac{1}{CR_{14}} + \frac{1}{CR_{23}} \right) + \frac{1}{CCRR_{12314}}}{D(s)} \quad (C1b)$$

$$\frac{V_1}{V_{n2}}(s) = -B \frac{s \frac{1}{CR_{14}} + \frac{1}{C} \left(1 + \frac{1}{CR_{25}} \right) + \frac{1}{CCRR_{124235}}}{D(s)} \quad (C1c)$$

$$\frac{V_2}{V_1}(s) = - \frac{\left(\frac{1}{s} + \frac{F}{s} - \frac{AE}{s} \right)}{D(s)} \quad (C2a)$$

$$\frac{V_2}{V_{n1}}(s) = -A \frac{s \frac{1}{CR_{22}} + \frac{1}{CCRR_{1224}} + \frac{1}{CCRR_{1212}}}{D(s)} \quad (C2b)$$

$$\frac{V_2}{V_{n2}}(s) = \frac{s \left(1 + \frac{1}{CR_{22}} \right) + \frac{1}{C} \left(\frac{1}{CR_{22}} + \frac{1}{R_3} + \frac{1}{R_5} \right)}{D(s)} \quad (C2c)$$

where

$$D(s) = s^2 + s \frac{1}{CR_{23}} + \frac{AB}{CCRR_{1224}}$$

V_{n1} and V_{n2} are the input-referred noise sources associated with

the two amplifiers. As expected, all transfer functions have the same denominator. Filter types realized through a particular input resistor and/or a capacitor are shown in Table (C-1). Three results applicable to SC equivalents are obtained. The first result is that the implementation of a notch filter depends on whether or not the signal is inverted and on the location of the loop inversion. The second result is that the location of the inversion is only important for the notch filter realization. Third, filters are typically classified according to their filter characteristics. Table (C-1) shows that the output of the lossy integrator can give lowpass (LP), highpass (HP), bandpass (BP) and notch-filter characteristics while the non-lossy integrator does not have this flexibility. This property is important in the derivation of a new biquad as will be discussed in chapter 5.

The SC versions of the general active-RC biquad realized by the conventional integrators of Fig. 1.6(a) and (b), and the CDS integrators are shown in Figs. C.2 and C.3, respectively. The double subscript of a_s (capacitor ratios) means that the SC resistors are inverting type. Applying the charge-conservation equation at the summing nodes of the amplifiers and simplifying the z-domain expressions gives:

Table 1. A summary of filters realized from the general active filter of Fig. 1. Note that the feedforward gain is indicated by the symbol A.

I	A	C	I	J	II		III	
					N(s)	FILTER TYPE	N(s)	FILTER TYPE
X	-	-	1	d			$\frac{1}{A \frac{CCKR}{1212}}$	LP
X	-	-	-1	d			$-\frac{1}{A \frac{CCKR}{1212}}$	LP
	X	-	d	1	$\frac{1}{B \frac{CCKR}{1225}}$	LP	$-\frac{s}{CR \frac{25}{25}}$	BP
	X	-	d	-1	$-\frac{1}{B \frac{CCKR}{1225}}$	LP	$\frac{s}{CR \frac{25}{25}}$	BP
		X	d	d	$\frac{SC}{B \frac{5}{CCKR \frac{124}{124}}}$	BP	$\frac{C}{S \frac{2}{C} \frac{2}{2}}$	HP
X	-	X	1	d			$\frac{C}{S \frac{2}{C} \frac{1}{A \frac{CCKR}{1212}}}$	?
X	-	X	-1	d			$\frac{C}{S \frac{2}{C} \frac{1}{A \frac{CCKR}{1212}}}$	??

d = don't care or not applicable

$$\text{eq 1: } \frac{V}{U} = \frac{N(s)}{D(s)} \quad ; N(s) \text{ is the numerator of the transfer function } \frac{V}{U}(s).$$

$$\text{eq 2: } \frac{V}{U} = \frac{N(s)}{D(s)} \quad ; N(s) \text{ is the numerator of the transfer function } \frac{V}{U}(s).$$

$$\text{where } D(s) = s^2 + \frac{C}{CK} + \frac{1}{CCKR \frac{1224}{1224}}$$

? : a notch filter if and only if the symbol A is -1.

?? : a notch filter if and only if the symbol A is +1.

Fig. C-2 A general SC biquad.

Fig. C-3 A general CDS biquad.

$$\begin{aligned}
 V_1(z) = & [V_{n1}(z)(1 - Jz^{-1/2})(1 + a_{11} + a_{14} + a_{44} - z^{-1}) \\
 & + Mz^{-1/2}(a_{44} - a_{n2})V_{n2}(z) + V_2(z)(a_{44}z^{-1} - a_{44}) \\
 & + V_1(z)(a_{11}z^{-1} - a_{11})]/(1 - z^{-1})
 \end{aligned}
 \tag{C3}$$

$$\begin{aligned}
 V_2(z) = & [V_{n2}(z)(1 - Lz^{-1/2})(1 + a_{22} + a_{23} + a_{35} + a_{55} \\
 & + a_{c5} - z^{-1}(1 + a_{c5})) + Ma_3z^{-1/2}V_{n2}(z) + \\
 & V_{n1}(z)Kz^{-1/2}(a_{22} - a_{22}) + V_1(z)(a_{22}z^{-1} - a_{22}) + \\
 & V_1(z)[(a_{55}z^{-1} - a_{55}) - a_{c5}(1 - z^{-1})]/(1 + a_{33} - z^{-1})
 \end{aligned}
 \tag{C4}$$

Substituting Eq. (C4) into Eq. (C3) and simplifying gives the signal and noise transfer functions for the output of the first integrator:

$$\begin{aligned}
 \frac{V_1}{V_i}(z) = & \frac{1}{D(z)} [z^{-2}(a_{44}a_{55} + a_{44}a_{c5} - a_{11}) + z^{-1}(a_{11} + a_{11} \\
 & + a_{11}a_{33} - a_{44}a_{55} - a_{44}a_{c5} - a_{44}a_{c5} - a_{44}a_{55}) + a_{44}a_{55} \\
 & + a_{44}a_{c5} - a_{11}(1 + a_{55})]
 \end{aligned}
 \tag{C5a}$$

$$\frac{V}{V_{nl}}(z) = \frac{1}{D(z)} [(1 - Jz^{-1/2})(1 + a_3^{-1}z^{-1})(1 + a_1 + a_{11} + a_4 + a_{44}^{-1}z^{-1}) + Kz^{-1/2}(a_2^{-1}z^{-1/2})(a_{22}^{-1}z^{-1/2})(a_{44}^{-1}z^{-1/2})(a_4^{-1}z^{-1/2})]$$

(C5b)

$$\frac{V}{V_{n2}}(z) = \frac{1}{D(z)} [Mz^{-1/2}(a_4^{-1}z^{-1/2})(a_{44}^{-1}z^{-1/2})(1 + a_3^{-1}z^{-1}) + (1 - Lz^{-1/2}) \times (a_{44}^{-1}z^{-1/2})(a_4^{-1}z^{-1/2})[1 + a_2 + a_{22} + a_3 + a_5 + a_{55} + a_{c5}^{-1}z^{-1}(1 + a_{c5}^{-1})] + Ma_3^{-1/2}z^{-1/2}(a_{44}^{-1}z^{-1/2})(a_4^{-1}z^{-1/2})]$$

(C5c)

Similarly, substituting Eq. (C3) into Eq. (C4) gives:

$$\frac{V}{V_1}(z) = \frac{1}{D(z)} [z^{-2}(a_{11}^{-1}a_{22}^{-1} - a_{55}^{-1} - a_{c5}^{-1}) + z^{-1}(a_{55}^{-1} + a_5 + 2a_{c5} - a_{12}a_{22} - a_{11}a_2) + a_{12}a_2 - a_5 - a_{c5}]$$

(C6a)

$$\frac{V}{V_{nl}}(z) = \frac{1}{D(z)} [Kz^{-1/2}(1 - z^{-1/2})(a_2^{-1}z^{-1/2})(a_{22}^{-1}z^{-1/2}) + (a_{22}^{-1}z^{-1/2})(a_2^{-1}z^{-1/2}) \times (1 - Jz^{-1/2})(1 + a_1 + a_{11} + a_4 + a_{44}^{-1}z^{-1/2})]$$

(C6b)

$$\begin{aligned}
 \frac{V}{V} \frac{z^2}{n^2} &= \frac{1}{D(z)} [(1 - z^{-1})(1 - Lz^{-1/2})(1 + a_2 + a_{22} + a_3 + \\
 &\quad a_5 + a_{55} + a_{c5} - z^{-1}(1 + a_{c5})) + Mz^{-1/2}[a_3(1 - z^{-1}) \\
 &\quad + (a_{22}z^{-1} - a_2)(a_4 - a_{44})]] \quad (C6c)
 \end{aligned}$$

where

$$\begin{aligned}
 D(z) &= z^{-2}(1 - a_{22}a_{44}) - z^{-1}(2 + a_3 - a_{22}a_4 - a_2a_{44}) + 1 \\
 &\quad + a_3 - a_2a_4
 \end{aligned}$$

J, K, L and M are equal to 1 or 0. J, K, and L, M are associated with the non-lossy and lossy integrators, respectively. Their use is the same as in the analyses of lowpass filters.

END

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