Coplanar technology for the design of a 39.25GHz active mixer

by

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Abstract

This thesis explores coplanar technology as a means of facilitating the design of active microwave mixers. The advantages of coplanar technology in designing reduced- area components are investigated.

After a review of current technology, advances in coplanar technology for producing reduced-area structures are discussed. A microwave mixer design is presented, showing the potential coplanar technology has to provide relatively high-gain mixers. The design is then optimized, using particle swarm optimization, to further increase the potential gain of the mixer. A new design is then presented, based on the optimized microwave mixer.

Coplanar technology offers some advantages over the better known microstrip technology for fabricating monolithic microwave integrated circuits (MMIC). One advantage is the ability to insert series and shunt structures directly into the centre conductor. This technique can significantly reduce the area occupied by the structure, providing lower cost. Novel folded structures will be presented that are used to match input impedances to 50Ω while offering the same performance as non-folded structures.

Coplanar microwave mixers are most often designed as diode mixers having loss. Active microwave mixers have been in use for many years, but mainly in microstrip technology. The Gilbert cell is probably the most used active design for RF mixers. Very few active mixers have been designed in coplanar technology. A microwave mixer

design based on the Gilbert cell will be presented. Its performance is evaluated and shown to be better than standard diode mixers, with 5dB of conversion gain.

A further refinement of the design is done to improve conversion gain. Particle swarm optimization, a relatively new optimization technique, is used to optimize the design of the Gilbert cell. This optimization simplifies the design of the Gilbert cell.

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Chapter 1

Introduction

1.1 Overview

The emergence of personal communication devices (such as cellular phones, personal digital assistants) has greatly accelerated the development of low-cost integrated systems at higher frequencies. Also, development of features such as Internet on cellular phones has pushed the demand for bandwidth even higher. Typical multi-user systems require bandwidths that are close to 1 GHz. At 1 GHz, the transmission frequencies of these devices must be of higher order than this 1 GHz bandwidth. For example, a communications band exists in the 38.7 to 39.8GHz range in Canada [1]. This band is used for Space-to-Earth and point-to-point communications.

And so the push in the telecommunications industry has been to develop integrated systems that can operate either as short-distance communications devices, for local-area networks (LAN) or through inter-satellite communications, or simply as part of local personal communications cells (cell phones, for example).

The mixer is an important part of any integrated radio system. At any time when a frequency higher than baseband is used to send or receive information, a frequency translation must be done. A device or technique must be used to shift one frequency up or down to another. A frequency is shifted up to allow transmission, and shifted

down at the receiving end. The mixer is the component or device that achieves this frequency shift.

Many different devices or techniques can be used to achieve mixing. At lower frequencies, most of these techniques are well documented and perform extremely well. Even at frequencies of a few GHz, mixing circuits are well characterized.

However, at higher microwave frequencies, these techniques present different problems. Matching at higher frequencies, device performance and constructing these circuits are much harder. It is therefore important to understand the difference between the mixing techniques at 1GHz and 40GHz in order to apply them properly. At 1GHz, certain characteristics of the devices and circuits are ignored because the wavelength of the signal is large compared to the device size. At 40GHz, line lengths and parasitics have a much greater impact. A proper design must take into account all the various line lengths and parasitics present in devices, matching circuits, and input and output pads.

There are currently two major millimetre wave circuit design techniques: microstrip and coplanar. Microstrip technology has been in use for many years and is the dominant structure for millimetre wave circuits. Coplanar technology, although close to 40 years old, has seen limited use because of cost considerations, difficulty in simulating the higher-frequency components, and the preponderance of microstrip.

It has been decided in this work to use coplanar waveguide technology to design a mixer using active components. Coplanar waveguide offers many challenges, but has seen improved growth in the last few years, including some interesting designs for stubs and couplers. These new designs are not possible in microstrip.

The following section will explain the difference between microstrip and coplanar, and give the reader the information necessary to understand why coplanar was chosen for this design.

1.1.1.1 The Coplanar Waveguide

The usual method of propagating a signal on a dielectric substrate is through the use of a waveguide. In microstrip, the most common waveguide technology, the waveguide is a thin layer of metal a few microns thick ($3\text{-}6\mu\text{m}$). The ground reference for the microstrip line is a layer of metal underneath the substrate [2], as shown in Figure 1.1. The signal propagates between the metal layers.

Figure 1.1: Microstrip waveguide

The coplanar waveguide differs from the traditional microstrip line because the ground plane is parallel to the waveguide [3], rather than being underneath it (refer to Figure 1.2). In this configuration, fields will couple in a horizontal fashion, rather than in a vertical manner to the ground.

Figure 1.2: Coplanar waveguide

When designing lines of specific impedance for a circuit, a coplanar waveguide gives much greater latitude of possible line impedances. The impedance of a line is a function of the line width and the spacing between the ground planes and the centre

conductor [4], parameters that any designer may modify. On a microstrip circuit, the line impedance is a function of the centre conductor width and the substrate thickness [2]. The substrate has a fixed thickness, and so a designer is left with only one parameter to modify when designing a line of different impedance. On a coplanar line, the two parameters of line width and gap give many more options to a designer.

These two parameters (line width and gap) also give more flexibility when designing stubs. Stubs are used at higher frequencies to simulate either capacitive or inductive effects, in series or shunt configuration. At lower frequencies, the use of stubs is often prohibitive, requiring much space and making circuits too big to be of practical (and economic) use. Since $\lambda = c/f$ (in free space), for stubs that approach a quarter-wavelength, even at frequencies of 1 GHz these dimensions are usually too big (on a $\epsilon_r = 12.9$ substrate, a 1 GHz quarter wavelength line is approximately 2.8cm long). At 40GHz, a quarter wavelength line is approximately 0.7mm long, well within the dimensions of common circuits.

New techniques for coplanar stubs have been developed in recent years (refs. [5–9]). These new techniques produce a significant reduction in the size of stubs by folding them into the centre conductor, or folding them into the ground planes. These methods are not available in microstrip [10], because folding a stub into the centre conductor will significantly change the impedance of the line. In coplanar, since the gap to the ground plane can be controlled by the designer, the impedance can be controlled.

1.1.2 Coplanar vs Microstrip

Coplanar technology has been around for many years [3], however it has received limited use in practical applications, mostly because of cost-related issues [11]. However, recent developments have rendered coplanar technology increasingly attractive for millimetre-wave applications [11]. Some advantages of coplanar technology over

microstrip technology are [4]:

- Lower dispersion of the modes
- Less coupling between adjacent lines
- Reduced parasitic effects
- Compatibility with flip-chip technology
- Potentially lower cost

Microstrip circuits still have some advantages over coplanar in some respects: layout of circuits in coplanar technology is often more difficult than in microstrip, since accessing the grounds in microstrip is done by etching a hole through the substrate to the ground plane beneath, rather than having the ground follow the centre conductor (in coplanar). To ensure proper impedance in the lines when designing a microstrip line, the substrate thickness is kept small [2]. Also, coplanar waveguides require air bridges to prevent the generation of parasitic modes [12], which can add to the complexity and cost of fabrication.

Coplanar technology also offers more options when designing passive elements such as stubs. Stubs can be folded into the centre conductor when using a coplanar line, which cannot be done in microstrip [4].

The objective of this thesis is therefore to explore coplanar technology as a means to design an active microwave mixer. Coplanar waveguide technology will also be explored as a means of reducing the size of the matching circuits necessary in any microwave design. The design of the mixer will also be optimized by using particle swarm optimization, to reduce the time needed to optimize the centre core of the mixer.

1.2 Summary of Thesis Contribution

The main contribution of this thesis is the design of an active mixer at 39.25GHz using coplanar technology. Coplanar waveguide technology offers interesting possibilities in the design of microwave active mixers. Specific contributions include:

1. Active microwave mixer in coplanar technology with conversion gain.
2. Use of folded structures for impedance matching in coplanar technology to reduce the size of the matching circuit.
3. Use of particle swarm optimization as a means of optimizing the design of the Gilbert cell.

1.3 Thesis Overview

This thesis is organized as follows.

Chapter 2 presents background information on active mixers and coplanar technology. The chapter begins with a brief overview of diode mixers, then of active microwave mixers. A review of coplanar technology and folded structures is then presented.

Folded structures used for impedance matching are presented in Chapter 3. The design of new folded structures is presented and sample design and experimental results are presented.

The design of an active microwave mixer is presented in Chapter 4. A half Gilbert cell design is presented, in coplanar technology, that has conversion gain. This mixer uses an active balun. Experimental results for this mixer are given in this chapter.

A further refinement of the design is done in Chapter 5. Particle swarm optimization is used to increase the performance of the half Gilbert cell, and the new design

does not use an active balun to better study the performance. Experimental results are also presented.

Finally, Chapter 6 summarizes the work done and lists the contributions of the thesis, as well as discussing future work.

Chapter 2

Millimetre-wave Mixers and Coplanar Waveguide

Mixing circuits at millimetre-wave frequencies are usually made using diode circuits [13]. The mixing is done by using the non-linear characteristics of the diode. However, the diode cannot provide gain. Typical diode mixers at 30 GHz usually have 10 dB conversion loss [14].

In the last few years, active mixers have become more popular as mixers at low microwave frequencies. Resistive mixers, single-FET mixers and Gilbert cells have become increasingly visible in the literature.

This chapter will begin with a small overview of diode mixers at microwave frequencies, to give the reader a better understanding of the advantages and limitations of these diode mixers. Then an overview of the Gilbert cell circuits published in the literature will be presented.

A review of mixers, and more specifically diode mixers, was done in the IEEE Transactions on Microwave Theory and Techniques, in March 2002 [13]. The diode mixer is mentioned abundantly in the review article, with little mention of active mixers. Some mention is made of single FET mixers, but no mention is made of Gilbert cells used as microwave mixers.

Afterwards, an overview of coplanar technology is presented. A brief history is presented, and an analysis of coplanar discontinuities. These discontinuities (open circuit and short circuit) are used in stubs, which are used to design matching circuits. Some theoretical background on the calculation of line impedance for coplanar circuits is given, which also affects the design of matching circuits.

A brief overview of Finite Ground CPW (FGCPW) is then presented. FGCPW is a more realistic representation of coplanar circuits, since the ground plane in actual circuits is finite. The standard coplanar waveguide is defined by an infinite ground plane.

2.1 Diode Mixers

A lot of research has been done on diode mixers, and numerous articles may be found on the subject, from diode mixers at lower frequencies to diode mixers above 200GHz [15–18]. Some of these articles will be mentioned here, since an understanding of diode mixers will give a better overview of their strengths and weaknesses. Understanding their characteristics will help to see how active mixers can be useful.

Although a complete review of the diode mixer is given in [13], an overview of the developments in the last years will be presented here.

Mixer circuits started appearing on MICs in the late 1960s. Planar transmission media, such as fin-line, microstrip and stripline were mostly used with Schottky barrier diodes, with frequencies up to 12 GHz. These new configurations permitted the development of image reject mixers (IMR), double balanced mixers (DBM) and anti-parallel subharmonic mixers (SHM). Some problems associated with accessing the quad structure were overcome by using multi-layer techniques with innovative balun designs. New configurations were introduced to eliminate via holes and back-metallization; the coplanar waveguide is still being used in this regard.

The anti-parallel diode pair was first demonstrated for millimetre-wave frequencies in the early 1970s. The advantages of pumping at one-half the signal frequency were demonstrated and used in many applications where limited LO power was available. The wide frequency separation between the RF and LO meant good isolation could be achieved between these ports.

In the 1970s, GaAs MESFETs were explored as a possible replacement or competitor to the diode mixer. However, research at that time indicated these active mixers, with medium noise figures and poor $1/f$ noise, were not competitive with diode mixers.

The advances in MMIC technology in the late 1970s and early 1980s permitted a vast increase in the potential for mixers. Miniaturization of components reduced costs and increased the potential appeal of MMIC mixer circuits.

With advances in LNA techniques and integrated structures, the mixer as a variable-resistance element was explored. Transistors such as MESFETs, MISFETs, HEMTs and HBTs were explored for use as mixers with increased IP3 characteristics. The variable resistor device was demonstrated to possess improved $1/f$ noise, lower DC power consumption, and better intermodulation products. Other improvements to MMIC design, such as the implementation of baluns on MMICs, lead to increasing progress. With the increase of on-chip applications, mixers were being realized that incorporated many different attributes, such as amplification.

MMIC Diode Mixer Example

One diode mixer was designed by Verver, Laneve and Stubbs (ref [17]). It is a subharmonic mixer, meaning it uses a harmonic of the LO frequency for mixing rather than the LO itself. Their mixer uses an anti-parallel diode pair (two diodes connected together in opposite directions) to mix the RF with the second harmonic of the LO signal. The circuit is built on a GaAs substrate, with a surface area of

1.2mm $\times$ 1.3mm. The measured conversion loss is 13dB for a 61GHz input signal, with a return loss of 10dB. The schematic is given in Figure 2.1.

Figure 2.1: Schematic diagram for diode mixer

An upconverter must have good carrier suppression properties, and the subharmonic mixer accomplishes just that. One advantage of the even-harmonic mixer is that it has a high $2 \times \text{LO}$ -to-RF suppression by virtue of the cancelation of the even-harmonic currents in the anti-parallel diode pair. LO to RF suppression is also high because the mixing is done with a harmonic of the LO signal, and so a large frequency separation exists between the LO and RF signals. As well, LO noise suppression is improved because of this large frequency separation.

For their design, the authors used open and short-circuit stubs to act as filters to separate the RF input signal, the IF output signal and the LO. A single parallel-coupled line section is used at the RF port to reject the IF and perform some matching. An RF bandstop filter is used at the output to extract the IF.

The LO signal is applied directly to the anti-parallel diode pair. A short-circuit stub connected to the same point has a length of $\lambda_{\text{LO}}/4$, which acts as an open circuit to the LO frequency but shorts out $2f_{\text{LO}}$ and f_{RF} , since $f_{\text{RF}} \cong 2f_{\text{LO}}$. This stub is

used to suppress the RF at the LO port and acts as a DC return path.

To the other side of the anti-parallel diode pair, another stub is connected, this time a $\lambda_{LO}/4$ open-circuit stub. This provides a ground at the LO frequency so the diodes can be pumped, and also prevents leakage into the IF and RF ports. At $2f_{LO}$ and f_{RF} it appears as an open circuit and does not affect the RF signal.

An RF parallel-coupled line bandpass filter is used to inject the RF signal. The passband of the filter is 59 - 61GHz, the desired RF frequency of the circuit. This filter is also used to provide some matching at the RF port. Better matching could have been done with a matching circuit, but limited space forced the authors to compromise. This bandpass filter also works to attenuate the LO at the RF port.

An RF bandstop filter is used at the output to extract the IF signal. It consists of an open-circuit stub followed by a microstrip line, both of $\lambda_{RF}/4$ in length. This creates a high impedance at RF so the RF signal does not appear at the output.

2.2 Active Mixers

For active mixers, a few standard active mixing circuits have emerged. The simplest topology uses a single FET. The RF and LO signals are applied to the FET's gate, and the IF signal is recovered at the drain. A balanced topology can be utilized where two FETs are used, one which takes the RF as input, and one which takes the LO as input.

The FET resistive mixer [19–26] is another possible topology [27]. It is a simple, one-FET mixer. It uses no DC bias at the drain. The RF signal is applied at the drain, and then the IF is filtered at the drain. The resistive mixer operates almost the same as a diode mixer, except that it has less noise than a diode mixer [14], while having comparable loss. The resistive mixer is based on the principle that at very low drain voltages, the channel induced in the device is linear. When an LO signal

is applied to the gate, the channel depth is changed, and hence also the resistance of the channel. The gate voltage of the device must be slightly above V_t , while the DC drain voltage must remain at 0V.

The Gilbert cell [28] is the most common active mixer configuration. It consists of two differential amplifier topologies connected together (Figure 2.2). The two lower transistors function as controlled current sources, operated by the RF signal, while the four upper transistors are switched by the LO. The IF is obtained at the outputs of the upper quad, either in balanced or unbalanced fashion (using a balun). Three baluns are necessary for this configuration; one to split the RF to drive the two current sources, one to split the LO to drive the upper switching quad and one to obtain the IF. Active circuits can also be used instead of the baluns.

Figure 2.2: The Gilbert cell

The Gilbert cell has mostly been used at RF frequencies (less than 6GHz). However, more and more research is being done that uses the Gilbert cell topology (or a variation) to provide mixing on MMIC circuits.

2.2.1 Circuits Using the Gilbert Cell

Silicon has been used extensively to implement the Gilbert cell configuration. These implementations give good performance, with regards to conversion gain, linearity, noise figure, voltage supply and current consumption. One such implementation is given in [29]. The authors have developed a downconverter / upconverter circuit that works at radio frequencies, i.e., 1 to 5 GHz. They have optimized their mixer for conversion gain and noise figure, rather than linearity or IIP3. They used resistive loading of the mixer to maximize the frequency of operation. This also produces a broad-band match for upconverting at the RF port.

Measurements were done at various voltages. As can be expected, with higher supply voltage came higher gain, more current, increased IIP3, and lower noise figure. However, power consumption increases. Since battery life is an important part of a wireless system (especially for a cellular phone user), minimizing power consumption is often the most important design factor.

As an upconverter, gain varied from 17dB at 900MHz to 1 dB at 5 GHz.

Among the first examples of the Gilbert cell being used at MM-wave frequencies is given in ref [30]. The authors, employees of Siemens AG, used a Gilbert cell on a silicon bipolar process to create a mixer. The transistors used had a cutoff frequency of 20 GHz, so getting conversion gain out of the circuit up to 17GHz is impressive. Noise figure at 17GHz was approximately 18dB, however. The authors also tested the circuit as a frequency doubler, which worked quite well.

A Gilbert cell was implemented on a Si/SiGe bipolar technology in [31]. The authors use a standard implementation of the Gilbert cell, using the standard circuit

design. The transistors used in this design had a f_T of 80GHz. No matching was done on-chip. Conversion gain varied from 15dB at 1GHz to 0dB at 32GHz. The IF frequency was chosen to be 100MHz. The chip has a total area of $0.45 \times 0.45 \text{ mm}^2$. The input 1dB compression point is -17dBm.

A design of a Gilbert cell circuit using the same process as that used in this work is presented in ref [32]. An alternate method of biasing the transistors in the Gilbert cell is presented, while impedance matching was not done in order to emphasize a wideband operation limited only by the devices. A theoretical approach is presented in the paper to calculate the various bias points of the transistors to minimize inter-modulation distortion.

The model used for the FETs was a modified version of Chalmers' model, given in [33]. A Volterra series analysis was used to obtain the optimum currents, voltages and device sizes for the Gilbert cell transistors.

The chip had an area of $1.5 \times 2 \text{ mm}^2$, and was fabricated with ED02AH HEMTs with gate length of $0.2\mu\text{m}$. Measurements were done up to 10GHz and various output parameters were measured. Maximum output power was obtained with a LO level of 1.6dBm at 5GHz, which is lower than most designs (which typically operate with a LO level of +10dBm). An active balun was used at the output. No plot of the conversion gain or noise figure was given, however.

One circuit using a variation of the Gilbert cell is given in [34]. The authors used a half Gilbert-cell topology, shown in Figure 2.3. In this configuration, the gate of the second switching FET is grounded. This eliminates the need for a balun for the LO, hence reducing the area needed for that part of the circuit. The lower transistor functions as a constant current source, and the upper switching transistors act as a differential amplifier.

The design goals for the authors were a circuit of minimum area, a conversion loss of 6dB or less for an LO power of +10 dBm. The circuit was designed for an RF

Figure 2.3: Half Gilbert cell

input of 41 - 44 GHz, and a fixed intermediary frequency (IF) of 5.2 GHz.

In designing their circuit, a +5V power supply was used. The lower transistor is biased at 25% I_{dss} , and hence the other two transistors function at 12.5% of I_{dss} , which is sufficiently near pinch-off for non-linear operation. An IF balun was used as well.

The completed circuit had a chip area of 1.65mm². At 44GHz, the conversion loss was 6dB (loss was 5.3dB in simulation). Over the 41 to 44 GHz bandwidth, the conversion loss varied from 2dB to 6dB. The best performance was achieved with a LO power of +10dBm (with a measured performance varying from 16dB loss to 6dB loss at 44GHz for an LO power varying from 0 to 10 dBm).

An idea to increase the conversion gain of a Gilbert cell downconverting mixer was proposed in ref [35]. The authors propose a solution to minimize the number of different bias voltages needed to bias the transistors in the Gilbert cell. Since cost is the biggest motivator in personal communication systems, a low-power device means longer battery life and hence lower cost. The circuit is shown in Figure 2.4.

Figure 2.4: Circuit schematic for bias-enhanced Gilbert cell

The authors propose to split the signal current and DC currents in the Gilbert cell. Current injection resistors were added between the positive supply voltage and the sources of the upper transistors of the Gilbert cell.

High value resistors (12-15k Ω , resistors R_{11} and R_{12} in Figure 2.4) are connected from the power supply to the amplifying transistors (the lower transistors of the Gilbert cell). The signal current flows through the upper switching transistors. Since these transistors have low DC current consumption, bigger load resistors can be used (50k Ω , resistors R_1 and R_2). These large resistors can also provide larger gain.

A diode stabilizing circuit is used to correct small fluctuations in the biasing conditions of the upper switching transistors. The DC bias voltage of these transistors

must not change too much, or else the injection current would change as well.

Since the load resistors are very large, a small deviation in current will create a big change in voltage. To avoid any potential instabilities, the authors used feedback circuits to stabilize the DC bias points. A 1pF capacitor (C_2) is also used to prevent oscillations.

This circuit used a 2.7V supply voltage, which consumed $278\mu\text{A}$ of current, for a total power consumption of less than $800\mu\text{W}$. The chip has a surface area of $0.6\text{mm} \times 0.6\text{mm}$. The circuit was characterized for an operating RF frequency of up to 2GHz.

One variation to the Gilbert cell, called the micromixer, was proposed by the original designer of the Gilbert cell, Barrie Gilbert. In his paper [36], the author proposed a modification to the Gilbert cell by using a class-AB input stage for the RF input. This modification is proposed in order to increase the linearity of the mixer.

The class-AB input stage provides a well-defined matching impedance and much lower input-related non-linearity. There is no gain compression in this configuration; gain increases at higher output levels.

The main limitations of the classical form of the Gilbert cell, with regards to linearity, is the RF input stage. The dynamic range of a mixer is conventionally defined by its 1dB compression point (P_{1dB}). This measure of linearity is based on the assumption that the non-linearity of the device is cubic in nature, which most often is not the case in modern devices. Thus, this 1dB compression point may be a misleading measurement of linearity.

The input impedance of the RF stage is frequency dependant, since the impedance is a function of the high-frequency β (gain). The singly-balanced form of the mixer (the half-Gilbert cell), can be used for matching, but this match rapidly deteriorates at higher input levels.

Noise is a cause for the lower bounds of the linearity of a mixer. Even if measurements cannot isolate one noise source from another, it is important to take note and understand the effect of noise on the linearity of the device.

Mixer gain is also an important parameter of the mixer. There is usually a trade-off between the conversion gain and linearity: higher gain means less linearity, or conversely less gain means a higher linearity can be achieved. The non-mixing gain of the mixer, when the mixer is used as an amplifier (when a large DC bias is applied at the LO input), is defined by the ratio of the IF load impedance (Z_{IF}) to the input matching impedance (Z_{IN}). The conversion gain will usually be 4dB ($\pi/2$) less than the nonmixing gain.

Emitter degeneration is often used to extend the dynamic range of the mixer, by adding resistors at the emitters of the transistors in the input RF stage. These resistors add noise to the mixer however, so there is a limit to how much improvement can be achieved. One study by Gilbert (ref. [37]) shows the theoretical improvement in linearity is possible by an amount:

$$20 \log \left[\frac{1 + 1.7\sigma}{\sqrt{1 + 2\sigma}} \right] \text{ dB} \quad (2.1)$$

where

$$\sigma = \frac{I_Z R_E}{2V_T} \quad (2.2)$$

and R_E is the resistor added into each emitter.

The basic micromixer differs from the classical Gilbert cell at the RF input stage. Instead of having the RF signal input into two transistors and having the RF input stage being basically a differential amplifier, a class-AB amplifier is substituted at the input. Two stages are included in this design, one that handles the positive swing of the RF, and one that handles the negative swing of the RF. The new input stage uses two more transistors than the classical configuration.

The author presents equations used to determine the appropriate bias points and voltages for the input stage; these equations will not be reproduced here.

Tests done at 300MHz show that at very high RF drive levels the gain *increases*. So the RF stage will not have gain compression, but rather expansion at high drive levels. This is unusual, as all other designs, even the classical Gilbert cell, show compression as RF drive level increases.

The micromixer was shown to be a very useful alternative to the classical Gilbert cell, at lower frequencies. The analysis done on the transistors was performed at sub-GHz frequencies; many of the assumptions and calculated values will not apply at higher microwave frequencies. However, as a low-frequency alternative, the micromixer demonstrated accurate input impedance, high intermodulation intercepts, and very high input signals, with acceptable noise performance.

Other references to Gilbert cell mixers can be found in [38–45].

Coplanar Gilbert-cell Circuits

There have been very few coplanar Gilbert cell mixers reported in the literature. Only one very recent example was found in the IEEE online archives [46]. Very few coplanar FET mixers have been reported (refs [47, 48]).

2.3 Coplanar Waveguide

Among the earliest references to coplanar waveguides is a Master's thesis by R.F. Frazita [49], in 1965. One of the first published references is the paper by Cheng P. Wen [3], in 1969, presented at the annual IEEE International Microwave Symposium (the precursor to MTT-S).

Wen first proposed the coplanar waveguide for gyromagnetic applications. Coplanar waveguide has certain advantages over microstrip, the most important which

was having all circuit elements on the same plane. In his paper, the author presented calculations of characteristic impedance, phase velocity and attenuation for the coplanar waveguide. The characteristic impedance was calculated using conformal mapping [50].

Few developments were made in the 1970s with regards to the modeling of coplanar discontinuities. Most research focused on the application of coplanar waveguides [51–53].

In the 1980s, more and more applications of coplanar waveguides became common, such as filters [54–56], oscillators [57–59], or antennas [60–64]. One paper by Jackson [65] compared coplanar waveguide to microstrip in terms of conductor loss. A review of the work done in Europe on coplanar waveguide was done in 1993 in [66].

2.3.1 Discontinuities

Among the first attempts to define coplanar waveguide discontinuities was by Simons and Ponchak [67]. They investigated three discontinuities: open circuit, a series gap in the centre conductor, and a step change in centre conductor width.

Further research into coplanar waveguide discontinuities was done by Beilenhoff et al. [68]. The authors looked at three discontinuities: an open circuit, a short circuit, and a MIM short circuit. All three discontinuities were described in terms of length extension.

Open Circuit

A finite-difference method was used by the authors [68] to analyse all three discontinuities. For the open circuit, the fringing fields at the end of the line increase the capacitance. This added capacitance can be described as a length extension of the line. For a ground to ground separation of d , the length extension can be roughly

described by the following equation, if $g > d$

$$l_{ext} \approx \frac{1}{4} d \quad (2.3)$$

where g is the gap from the end of the line to the ground plane, as shown in Figure 2.5. This equation is valid for a 50Ω line; for other impedances, a difference of up to 20% was observed.

Figure 2.5: Open circuit coplanar waveguide

When the gap to ground g is greater than the ground to ground separation d , the length extension is constant. Therefore, a good design rule is to keep $g > d$. The author's research was done using a GaAs substrate ($\epsilon_r = 12.9$). These results were also obtained in [69].

Metallization thickness did not have a significant impact on length extension. Varying the thickness from 0 to $5\mu\text{m}$ leads to about a 1% variation in the length extension.

Short-circuit

The short-circuit stub also presents length extension because of current distribution in the discontinuity. In this case, the length extension is given by [68]:

$$l_{ext} = \frac{1}{8} d \quad (2.4)$$

where d is the ground to ground separation, as in Figure 2.5.

Equation 2.4 is only valid for a frequency range where no dispersion is observed, and if the metallization thickness does not become too large.

Other modeling of coplanar discontinuities was done in [12, 70–75].

2.3.2 Other Design Considerations

Other research has been done on coplanar waveguides with regards to design rules applicable to MMIC design. A paper by Riaziat et al. [76] investigated radiation loss and guided modes for different structures (substrate thickness, backside metallization and ground plane width). Their research showed that for coplanar waveguides, dispersion “strongly depends on the ground-to-ground spacing. If the spacing is small compared to dielectric wavelength and substrate thickness, both dispersion and radiation losses are minimized.” Reducing the ground-to-ground spacing will also impact impedance of the coplanar line; to maintain the same impedance, the centre conductor must be made smaller, and hence conductor loss will increase.

Another design consideration is the spacing between adjacent coplanar lines. A paper by Schnieder et al. [77] showed that coupling between adjacent lines can be ignored (is less than -30dB) if the distance between the lines is more than twice the ground to ground separation of the lines. However, in conductor-backed coplanar applications, this design rule does not hold.

One important design restriction is the use of air bridges at discontinuities to prevent the coupled slotline mode from being excited [12]. A coplanar waveguide

circuit should also maintain transverse symmetry with regards to the direction of propagation to prevent the coupled slotline mode from being excited [12], [78].

2.3.3 Stub Matching Networks

At higher frequencies, the matching networks of high frequency inputs and outputs are usually done with stubs, since lumped elements must be well modeled to account for parasitics. Capacitors function well at higher frequencies, but inductors must be well modeled and simulated to ensure inductive behaviour at higher frequencies. There are also physical limits to the lumped element models; for example, in the process being used here, MIM capacitors must be bigger than $10\mu\text{m} \times 10\mu\text{m}$. If element values needed are really small, lumped elements are too big; distributed elements are therefore needed.

Distributed elements take the form of transmission lines terminated by short or open circuits. A review of these stubs in a coplanar environment is presented here.

2.4 Capacitive and Inductive Stubs

A transmission line connected to an arbitrary load is presented in Figure 2.6.

Figure 2.6: Loaded transmission line

If loss is neglected in the transmission line, the impedance seen looking into the line (Z_{in}) is given by the well-known transmission line impedance equation [79]:

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 \tan(\beta l)}{Z_0 + jZ_L \tan(\beta l)} \quad (2.5)$$

Using a short or open circuit as the load in Figure 2.6 creates impedances that are completely imaginary; no real part exists to the impedance. Such a transmission line (with a short or open circuit as the load) is called a *stub*.

If the load impedance is zero ($Z_L = 0$) and the line is less than a quarter wavelength at the frequency of interest, the impedance seen looking into the line will be inductive. Setting the load to zero, Equation 2.5 becomes

$$Z_{in} = Z_0 \frac{jZ_0 \tan(\beta l)}{Z_0} = jZ_0 \tan(\beta l) \quad (2.6)$$

For an inductive load, $Z_{in} = jL\omega$, where L is the inductance value being calculated and ω is the frequency of interest. The objective is calculating the length of the transmission line giving the same inductance as L . Making the appropriate substitutions, Equation 2.6 becomes

$$Z_{in} = jL\omega = jZ_0 \tan(\beta l) \quad (2.7)$$

$$L\omega = Z_0 \tan(\beta l) \quad (2.8)$$

where, solving for l (the length of the stub), the following equation is obtained

$$l = \frac{1}{\beta} \tan^{-1} \left(\frac{L \cdot 2\pi f}{Z_0} \right) \quad (2.9)$$

This can be further expanded by noting that [79]

$$\beta = \frac{2\pi}{\lambda_g} \quad (2.10)$$

and

$$\lambda_g = \frac{c}{f\sqrt{\epsilon_{eff}}} \quad (2.11)$$

where λ_g is the wavelength in the medium, ϵ_{eff} is the effective dielectric constant, and c is the speed of light in vacuum. ϵ_{eff} is usually obtained by simulation. Putting all these equations together, the following equation for the length of the transmission line is obtained:

$$l_{stub} = \frac{c}{2\pi f\sqrt{\epsilon_{eff}}} \tan^{-1} \left(\frac{L \cdot 2\pi f}{Z_0} \right) \quad (2.12)$$

or,

$$l_{stub} = \frac{0.3}{2\pi f \sqrt{\epsilon_{eff}}} \tan^{-1} \left(\frac{L \cdot 2\pi f}{Z_0} \right) \quad (2.13)$$

where L is in nH and f in GHz.

From the above equation, to make the length of the stub as small as possible, the impedance Z_0 of the line should be high. However, in a coplanar environment, raising the impedance means increasing the gap between the centre conductor and the ground planes, or reducing the width of the centre conductor. Increasing the gap is usually the better solution, but doing so makes the circuit larger. Reducing the line width increases the resistance of the conductor, and poses current limitations if the line also carries DC bias current.

The same development can be made for a capacitive stub, where the load impedance, instead of being a short, is an open circuit ($Z_L = \infty$). Solving for l in Equation 2.5 and making the appropriate substitutions gives

$$l_{stub} = \frac{c}{2\pi f \sqrt{\epsilon_{eff}}} \tan^{-1} (2\pi f Z_0 C) \quad (2.14)$$

or,

$$l_{stub} = \frac{0.3}{2\pi f \sqrt{\epsilon_{eff}}} \tan^{-1} \left(\frac{2\pi f Z_0 C}{1000} \right) \quad (2.15)$$

where C is in pF and f in GHz.

For the capacitive stub, the stub impedance should be as low as possible to reduce the length of the stub, the opposite of what was needed for the inductive stub. Widening a line leads to lower impedance, and lower resistance, but it also makes the circuit wider.

Equations 2.13 and 2.15 can now be used in the design of stubs having a particular reactance.

2.5 Finite Ground Plane Coplanar Circuits

The classical definition of a coplanar waveguide is one with an infinite width ground plane. In practice, the ground plane of microwave circuits is always finite. However, if the total width of the ground plane is larger than twice the ground-to-ground separation of the centre conductor, an infinite ground plane can be assumed [80].

The transmission line used in the current process can be modeled by the multi-layered structure of Figure 2.7. Heights and relative permittivity are found in the manufacturer's user guide.

Figure 2.7: Finite ground coplanar transmission line

Some notes on Figure 2.7: the height of the conductors (the black rectangles) is ignored. The width of the centre conductor is $2a$, while the gap between the centre conductor and the ground planes is $(2b - 2a)/2$. The width of the ground planes is $(2c - 2b)/2$. From conformal mapping [4], the effective dielectric constant of the structure is

$$\begin{aligned} \epsilon_{eff} = 1 &+ \frac{1}{2}(\epsilon_1 - 1) \frac{K(k)}{K(k')} \cdot \frac{K(k'_1)}{K(k_1)} + \frac{1}{2}(\epsilon_2 - \epsilon_1) \frac{K(k)}{K(k')} \cdot \frac{K(k'_2)}{K(k_2)} \\ &+ \frac{1}{2}(\epsilon_3 - \epsilon_4) \frac{K(k)}{K(k')} \cdot \frac{K(k'_3)}{K(k_3)} + \frac{1}{2}(\epsilon_4 - \epsilon_5) \frac{K(k)}{K(k')} \cdot \frac{K(k'_4)}{K(k_4)} \\ &+ \frac{1}{2}(\epsilon_5 - 1) \frac{K(k)}{K(k')} \cdot \frac{K(k'_5)}{K(k_5)} \end{aligned} \quad (2.16)$$

where $K(x)$ is the complete elliptical integral of the first kind.

$$K(k) = F\left(\frac{\pi}{2}, k\right) \quad (2.17)$$

The function F is the incomplete elliptic integral of the first kind, and is given by [4]:

$$F(\phi, k) = \int_0^\phi \frac{1}{\sqrt{1 - k^2 \sin^2 \theta}} d\theta \quad (2.18)$$

The first coefficients in Equation 2.16 depend on the geometry of the line and are given by [4]:

$$k = \frac{c}{b} \sqrt{\frac{b^2 - a^2}{c^2 - a^2}} \quad (2.19)$$

$$k' = \sqrt{1 - k^2} = \frac{a}{b} \sqrt{\frac{c^2 - b^2}{c^2 - a^2}} \quad (2.20)$$

The other coefficients are [4]:

$$k_i = \frac{\sinh\left(\frac{\pi c}{2h_i}\right)}{\sinh\left(\frac{\pi b}{2h_i}\right)} \sqrt{\frac{\sinh^2\left(\frac{\pi b}{2h_i}\right) - \sinh^2\left(\frac{\pi a}{2h_i}\right)}{\sinh^2\left(\frac{\pi c}{2h_i}\right) - \sinh^2\left(\frac{\pi a}{2h_i}\right)}} \quad (2.21)$$

$$k'_i = \sqrt{1 - k_i^2} = \frac{\sinh\left(\frac{\pi a}{2h_i}\right)}{\sinh\left(\frac{\pi b}{2h_i}\right)} \sqrt{\frac{\sinh^2\left(\frac{\pi c}{2h_i}\right) - \sinh^2\left(\frac{\pi b}{2h_i}\right)}{\sinh^2\left(\frac{\pi c}{2h_i}\right) - \sinh^2\left(\frac{\pi a}{2h_i}\right)}} \quad (2.22)$$

The impedance of the line is [4]

$$Z_0 = \frac{30\pi}{\sqrt{\epsilon_{eff}}} \cdot \frac{K(k)}{K(k')} \quad (2.23)$$

The impedance of the line as a function of the ground plane width can be calculated easily and is displayed in Figure 2.8. In this case, the centre conductor is $10\mu\text{m}$ wide ($a = 5\mu\text{m}$), with a gap of $5\mu\text{m}$ ($b = 10\mu\text{m}$). For a $5\mu\text{m}$ -wide ground plane ($c = 15\mu\text{m}$), the impedance of the line is approximately 58Ω .

For $c = 50\mu\text{m}$ (which means a ground plane width of $40\mu\text{m}$), the impedance of line varies little if the ground planes are wider.

Figure 2.8: Impedance as a function of the ground plane width

If the ground plane were infinite ($c = \infty$), Equations 2.19 and 2.20 become

$$\lim_{c \rightarrow \infty} k = \sqrt{1 - \frac{a^2}{b^2}} \quad (2.24)$$

$$\lim_{c \rightarrow \infty} k' = \frac{a}{b} \quad (2.25)$$

The other coefficients become

$$\lim_{c \rightarrow \infty} k_i = \sqrt{1 - \frac{\sinh^2\left(\frac{\pi a}{2h}\right)}{\sinh^2\left(\frac{\pi b}{2h}\right)}} \quad (2.26)$$

$$\lim_{c \rightarrow \infty} k'_i = \frac{\sinh\left(\frac{\pi a}{2h}\right)}{\sinh\left(\frac{\pi b}{2h}\right)} \quad (2.27)$$

Given these equations, the impedance for the line when the ground plane is infinite is 49.91Ω . The impedance obtained by simulation with HPADS for an infinite ground plane is 51.23Ω .

For a ground plane width of $40\mu\text{m}$, the calculated impedance of the line is 50.51Ω , which represents a 1.2% difference compared to the infinite ground plane. Therefore,

a ground plane width of $40\mu\text{m}$ for a line with a ground-to-ground separation of $20\mu\text{m}$ has the same impedance as a line with an infinite ground plane. A ground plane width of twice the ground-to-ground separation is sufficient to assume the ground plane is infinite.

2.6 Summary

This chapter presented an overview of diode mixers and active mixers used at millimetre-wave frequencies. At these frequencies, diode mixers have been used extensively, however the Gilbert cell, the most common mixer topology at RF frequencies, has seen limited use. Most of the designs also use microstrip technology, with few coplanar designs.

The Gilbert cell has been extensively studied, with many variations and improvements suggested over the years. One improvement which will be used later on in the design of an active mixer is a new biasing scheme [35]. The proposed circuit uses a different biasing method to increase the conversion gain of the mixer.

Some background on coplanar waveguide was also presented. In particular, equations used in the design of stubs were presented. Other design considerations were also presented, such as the line-to-line separation, the use of air bridges and length extension. Finite ground coplanar waveguide was also discussed, as it affects the impedance of the line.

Chapter 3

Folded Stubs

Folded stubs can be used to design reduced-size matching networks in coplanar circuits. Based on the background presented in the previous chapter, new folded stub structures are investigated. Some of these structures have been fabricated and their performance measured and compared with simulation.

Standard stub configurations are presented first, using the design rules of the OMMIC fabrication process. The folded versions of these stubs are then presented, as are measurement results.

3.1 Standard Stub Configurations

This first section presents standard stub configurations in a coplanar waveguide environment. Series inductive stubs and shunt capacitive stubs are presented in their standard configuration, as well as some ways to include the shunt stub in the centre conductor.

Circuits combining the series and shunt stubs are then presented, which are the most common matching L-networks in use.

3.1.1 Series Inductive Stub

To make the inductive stub, values of the effective dielectric constant (ϵ_{eff}) must be simulated, as well as the corresponding impedance. This data will help determine the width of the stub. For a $10\mu\text{m}$ -wide line, the effective dielectric constant and impedance are given in Table 3.1 for different gap values, based on the fabrication process.

Table 3.1: Simulated values of effective dielectric constant and impedance

Gap	ϵ_{eff}	Z_0 (Ω)
$20\mu\text{m}$	5.941	71.776
$25\mu\text{m}$	6.014	75.480
$30\mu\text{m}$	6.072	78.554

The gap between the centre conductor and the ground plane has an important effect on the total line width. The stub will be placed inside a centre conductor [8], [81]. The higher the impedance, the wider the gap will be, so to maintain a 50Ω centre conductor, the corresponding gap to the ground plane will increase as well.

A series inductive stub is presented in Figure 3.1. The stub is formed by introducing two symmetrical gaps in the centre conductor. It should be noted that the ground planes in the actual circuit would be much wider; they are drawn here in smaller dimensions to reduce space.

In Figure 3.1, the series inductive stub is defined by width w_2 and gap g_2 (and its virtual ground plane w_3), while the main conductor is defined by width w_1 and gap g_1 [71]. From the previous analysis, if the gap of the stub is larger, the impedance will be higher and the stub can be made shorter. Hence gap g_2 should be made as large as possible.

Increasing g_2 means that g_1 will have to be made larger as well if the same

Figure 3.1: Centre conductor loaded with series stub

impedance is maintained for the centre conductor, since

$$w_1 = w_2 + 2g_2 + 2w_3 \quad (3.1)$$

For example, if a $10\mu\text{m}$ -wide stub is chosen, with a $20\mu\text{m}$ gap (for an impedance of roughly 72Ω), and $5\mu\text{m}$ virtual ground planes, the total width is $60\mu\text{m}$. To maintain a 50Ω main conductor, the gap g_1 should be $39\mu\text{m}$ (obtained by simulation).

If the chosen gap for the inductive stub were $25\mu\text{m}$ (instead of $20\mu\text{m}$), the impedance of the stub would be 76Ω , the centre conductor would be $70\mu\text{m}$ wide, and to maintain 50Ω for the centre conductor, g_1 would have to be $50\mu\text{m}$. In this case, increasing the impedance of the stub by 5% means increasing the width of the whole structure by 23%. In the design of such structures, a compromise must be made between the stub length and the total width.

3.1.2 Shunt Capacitive Stub

For a shunt capacitive stub, referring to Equation 2.15, the impedance of the stub must be low to shorten the length of the stub. Also, to maintain transverse symmetry, two shunt stubs will be used. Figure 3.2 shows dual capacitive shunt stubs formed in

the ground plane.

Figure 3.2: Coplanar shunt capacitive stub

The shunt stub is simply a length of metal extending from the centre conductor into the ground plane. A gap to ground forms the required open circuit for a capacitive stub. If this gap were omitted, a short-circuit shunt stub would be created, and the stub would present an inductive reactance if its length were less than a quarter wavelength at the frequency of interest.

Coplanar shunt stubs are easier to design, since the width and impedance of the stub do not affect the centre conductor. Two stubs are used for two primary reasons: 1) the stubs can be made shorter, since parallel capacitances add; 2) the circuit is symmetrical with respect to the direction of propagation, reducing the generation

of unwanted modes. Notice in Figure 3.2 that air bridges (actually underpasses in the process being used) are used to prevent the generation of unwanted modes and maintain proper grounding of the ground plane.

The shunt stub can be folded into the centre conductor [8], as shown in Figure 3.3. In this configuration, a single stub is used, though it is possible to use double stubs [8] in the centre conductor (one facing left and one facing right). To accomplish this circuit (shunt stub in the centre conductor), a thin strip of ground plane is extended across the centre conductor. Air bridges are used in the centre conductor to jump across the thin ground strip. The stub to ground is then formed within the centre conductor using the new local ground point.

Figure 3.3: Centre conductor loaded with shunt stub

The shunt capacitive folded stub is wider than its inductive counterpart; as was mentioned previously, to make the stub shorter, the impedance must be as low as possible. For a coplanar transmission line, a small gap (g_c) and wide conductor (w_c)

create the small impedance needed to keep the stub as short as possible.

Another method of creating these stubs is to use an air bridge from ground to the shunt stub while keeping the centre conductor intact, as shown in Figure 3.4. In this manner, the centre conductor remains continuous, while the ground connection for the stub is accomplished through the air bridge (or underpass).

Figure 3.4: Centre conductor loaded with a shunt stub, using an air bridge as ground connection

Both methods of creating the stub are equally valid; the resulting behaviour is the same. The stub carries no DC current; therefore current limitations of the material used in the air bridge have no effect. There is one disadvantage to using the method of Figure 3.4: the shunt stub is completely enclosed within a box. For fabrication, the centre conductor will have to be opened up at some point and an air bridge used to bridge the created gap. Again, to maintain symmetry, the centre conductor will be discontinued at two places. This means there are more air bridges in the second

configuration than in the first.

The simulated S parameters of the centre shunt stub (for the metal connection to ground and the air bridge to ground) are shown in Figure 3.5. There is very little difference between the S_{11} and S_{21} amplitude and phase of both circuits. The S_{12} and S_{22} amplitude and phase are not shown on Figure 3.5 because they are the same as S_{21} and S_{11} , respectively. This demonstrates that both stub configurations are equally valid and may be used in circuit design.

Figure 3.5: Simulated S parameters (S_{11} and S_{21}) centre shunt stub

3.1.3 Combined Stub for Matching

When doing a matching circuit, a typical configuration is given in Figure 3.6.

To achieve such a circuit using stubs, the circuits of Figures 3.1 and 3.2 can be

Figure 3.6: Load matching network

combined. The two stubs (inductive and capacitive) are usually combined in one circuit as shown in Figure 3.7. In this circuit, the shunt stubs are attached to the end of the inductive stub.

Figure 3.7: Centre conductor loaded with series and shunt stubs

Some comments on Figure 3.7:

1. The length of the capacitive stub will have to be increased from the calculated value, since the added length g_1 of the stub adds inductive impedance to the

line. A longer stub will have increased capacitive impedance, balancing out the added inductance.

2. The point where the capacitive stub attaches to the main conductor (point a in Figure 3.7) defines the point where the capacitance and inductance are connected. The length of line from that point to the end of the line (towards the left) represents a phase shift that must be accounted for. However, if the centre conductor is 50Ω and the matching is done to 50Ω , this length of line has little impact on the circuit (the phase shift is not important in this case).

3.2 Novel Shunt C, Series L Folded Stub

The overall size of the matching circuit can be further reduced by folding the capacitive stub into the virtual ground plane of the inductive stub. The circuits of Figures 3.1 and 3.4 are combined. The virtual ground (width w_3) in Figure 3.7 is used, into which the shunt stub is folded. In order to fold the stub, the virtual ground planes (w_3) must be made wider to accommodate the capacitive stub. This will make w_1 wider as well, and the gap g_1 will need to be increased to maintain the same impedance (50Ω).

For the shunt stub, the second configuration (that of Figure 3.4) is used, with the air bridge providing the connection to ground. As in the case of Figure 3.4, the stub is completely enclosed within a box of metal, and the conductor will have to be opened to permit fabrication (these gaps are not shown in Figure 3.8). Therefore, four other air bridges will be needed to create the circuit.

Figure 3.8: Centre conductor loaded with series stub and folded capacitive stub

3.2.1 Shunt C, Series L Test Circuit

To test the folded shunt C, series L circuit, a circuit was built as part of a coplanar mixer. The folded shunt C, series L circuit was used as the RF matching circuit. The input impedance to be matched to 50Ω was $Z_{in} = 38.43 - j10.97 \Omega$.

The simulated RF matching circuit is a 0.13nH inductor in series with the load, followed by a shunt 44.5fF capacitor. Using a characteristic impedance of 71.776Ω (for a $20\mu\text{m}$ gap), and ϵ_{eff} of 5.941 , the length of the series stub is $209.65\mu\text{m}$ (from Eq. 2.13). A $10\mu\text{m}$ -wide capacitive stub is used with a gap of $5\mu\text{m}$, giving 51.2Ω , for a stub length of $205\mu\text{m}$ (from Eq. 2.15), which is divided in two since two stubs are used, for a length of $103\mu\text{m}$ per shunt stub.

The total width of the centre conductor now becomes

$$w_1 = w_2 + 2w_c + 2g_2 + 4w_3 + 4g_c \quad (3.2)$$

From the dimensions given above, this results in $w_1 = 110\mu\text{m}$; to maintain a 50Ω

centre conductor, the gap must be $80\mu\text{m}$. The lengths of the stubs (l_2 and l_c) will be different in the folded stub configuration from the combined configuration (Figure 3.7). The calculated and simulated values are shown in Table 3.2.

Table 3.2: Calculated and simulated values for combined and folded stub structures

		Simulated	
Dimension	Calculated	Combined	Folded
l_2 (μm)	209.65	210	229
l_c (μm)	103.0 ($\times 2$)	108($\times 2$)	163($\times 2$)

The simulated values for the combined stub are very close to the calculated values. The capacitive stub is slightly longer to offset the inductive portion of the line that lies in the gap between the centre conductor and the ground plane (length g_1).

For the folded stub, both lengths are longer than their simulated values, especially the capacitive stub. Some reasons follow:

1. The impedance of the capacitive stub is actually higher than the value used in the calculations, since it is effectively in a finite ground plane environment. As will be shown later, this finite ground plane environment shows strong correlation between the increase in impedance and the increase in length.
2. Coupling effects are not taken into account when calculating the lengths. Only a very thin strip of virtual ground plane separates the shunt stub from the centre series stub. A good rule of thumb is that twice the ground to ground separation is needed between lines for there to be no coupling (-30dB) [77]. This rule of thumb is not respected in this case.
3. The ground connection for the capacitive stub adds an inductive component to the stub.

For all these reasons, the lengths of the stubs are longer than their calculated

values. A designer must be aware of these differences and be prepared to adjust his design accordingly.

The S parameters of the folded stub are compared to the S parameters of the standard, non-folded stub in Figure 3.9, where the amplitude of the S parameters is shown. There is very little difference between the amplitudes of the folded and non-folded stubs, demonstrating that both have the same behaviour.

Figure 3.9: Simulated S parameters (amplitude) of the folded and standard stub in a shunt C, series L configuration

There is a discrepancy in the S_{22} amplitudes at approximately 10GHz. The folded stub shows a dip in the amplitude, similar to a resonance dip. However, as will be seen later, this resonance dip does not appear in the measured circuit.

The phase of the S parameters of the standard and folded stubs are compared in Figure 3.10. From this figure, there is a discrepancy in the phase of the S parameters

as the frequency increases. This makes sense, since the folded stub is longer because it behaves less as an idealized transmission line.

Figure 3.10: Simulated S parameters (phase) of the folded and standard stub in a shunt C, series L configuration

The standard stub occupied a circuit area equal to $250 \times 476 = 119000 \mu\text{m}^2$. The total length of the circuit is $210 \mu\text{m}$ for the series stub, $20 \mu\text{m}$ for the gap to the centre conductor, and $10 \mu\text{m}$ on each side for the centre conductor. The total width of the standard stub is $60 \mu\text{m}$ for the centre conductor, $39 \mu\text{m}$ for each gap, $79 \mu\text{m}$ for the length of each shunt stub extending into the ground plane, $40 \mu\text{m}$ for the gap at the end of the shunt stub to ground, and $50 \mu\text{m}$ of ground plane.

The folded stub occupies a circuit area of $269 \times 370 = 99530 \mu\text{m}^2$, a reduction of 16%. The total length of the circuit is $229 \mu\text{m}$ for the series stub, plus the additional lengths (same as the standard stub). The total width is $110 \mu\text{m}$ for the centre conductor, and

two gaps of $80\mu\text{m}$, and an additional $50\mu\text{m}$ for the ground planes.

To better understand the effect of finite ground planes, conformal mapping was used [4].

When the capacitive stub was in the combined configuration, the ground planes were considered infinite. But when the stub is folded into the centre conductor, the impedance of the line increased, since the ground plane is now much smaller. By calculation with conformal mapping, the impedance of the line has increased by roughly 16%. Comparing the calculated value of the line ($268\mu\text{m}$) with the simulated length of line ($308\mu\text{m}$), an increase of 15%, there is strong correlation between the increase in impedance and the increase of the length of the stub.

The matching circuit was fabricated by OMMIC, using their ED02AH process. A photograph of the test structure is shown in Figure 3.11.

Figure 3.11: Microphotograph of the shunt C, series L test structure

The measured and simulated S parameters of the circuit are shown in Figure 3.12. There is very little difference between the measured and simulated S parameters.

Figure 3.12: Simulated and measured S parameters (amplitude) of the folded shunt C, series L test structure

The matching circuit gave a measured return loss of -18dB when used in a coplanar mixer. These results were published in 2005 [82].

3.3 Series L, Shunt C Configuration

Another important matching configuration is one with a shunt capacitor to ground in parallel with the load followed by a series inductor, as in Figure 3.13. This type of L-network can be used when the admittance of the load is less than 1 (normalized) [79]. This combination is similar to the one previously presented, except that the shunt capacitor is not connected to the same part of the circuit. As will be seen, this poses some challenges when folding the stub to reduce its size.

The standard planar stub configuration for the circuit of Figure 3.13 is given in Figure 3.14. The circuits of Figures 3.1 and 3.2 are combined in a manner similar

Figure 3.13: Load matching network; series L, shunt C

to the one used in Figure 3.7, except that the shunt stub is connected to a different point in the circuit. In this case, the shunt stub is connected to the centre conductor after the gap for the inductive stub.

Figure 3.14: Centre conductor loaded with series and shunt stubs

The planar circuit is slightly longer than the shunt C, series L configuration, since the shunt stub is after the series inductive stub; the ground plane has to extend a

bit more to provide proper grounding for the shunt stub. Also, the circuit is symmetrical with regards to the centre conductor; two shunt stubs are used, making each smaller than a single capacitive stub would be, and the circuit remains symmetrical, preventing the generation of unwanted modes.

An air bridge is used in the circuit of Figure 3.14 to properly connect both sides of the ground plane, ensuring proper grounding (as was the case for the series L, shunt C configuration in Figure 3.7). For the manufacturing process used, this air bridge is in fact an underpass.

Similar comments to those of Figure 3.7 can be made about the layout of the circuit in Figure 3.14:

1. The shunt stub will be made slightly longer because of the small length of line that extends between the centre conductor and the ground plane (length g_1). However, this has a very limited impact on the length of the stub.
2. The length of line extending from point a to the left represents a phase shift that cannot be ignored. However, if the stub is being used to match to 50Ω , and the centre conductor is 50Ω , this length of line has little impact on the circuit performance.

To further reduce the size of this matching circuit, the shunt stubs can be folded into the centre conductor, in a manner similar to that of Figure 3.8.

3.3.1 Novel Folded Series L, Shunt C Configuration

The series L, shunt C configuration can be reduced in size by folding the shunt stubs into the centre conductor. The centre conductor will have to be made wider to accommodate the shunt stub. Figure 3.15 presents this folded stub configuration.

The shunt stub has the same width in its folded configuration, $10\mu\text{m}$ in this case. With a $5\mu\text{m}$ gap and a $5\mu\text{m}$ virtual ground, the centre conductor has a total width

Figure 3.15: Centre conductor loaded with series and folded shunt stub

of $30\mu\text{m}$. With the increased centre conductor width, the gap g_2 to form the series inductive stub must be made wider to maintain the same stub impedance. Should the same impedance be difficult to maintain, the stub can be made longer to obtain the same inductive effect.

There is a single shunt stub used in this case, while there were two in the planar, non-folded configuration. This means the shunt stub will probably be longer in the folded configuration than in the non-folded configuration; however, as will be seen, this is not the case for this particular application.

To properly compare the folded and non-folded configuration, an arbitrary point on the Smith chart was chosen, to be matched to 50Ω . This point was chosen so the matching network of Figure 3.13 could be used to provide matching. In this case, the point chosen was $80 - j7.2\Omega$. The ideal series L, shunt C values that provide matching to 50Ω are 0.16nH , and 34.7fF , respectively.

The ideal lumped element values correspond to stub dimensions of $108\mu\text{m}$ ($\times 2$) for the capacitive stubs, and $251\mu\text{m}$ for the inductive stub, using Equations 2.15 and

2.13, with stub impedances of 51.2Ω and 71.8Ω , respectively. The simulated values for the stub are $98\mu\text{m}$ ($\times 2$) and $275\mu\text{m}$. The dimensions of the stub, corresponding to Figure 3.14, are given in Table 3.3.

Table 3.3: Dimensions for the shunt C, series L stub configuration.

	w_1	g_1	w_2	g_2	w_3
Dimensions (μm)	60	39	10	20	5

When the shunt stubs are folded into the centre conductor, the centre conductor will have to be made wider, as stated earlier. If the shunt stub's width and impedance are unchanged, the centre conductor must be $30\mu\text{m}$ wide to accommodate the stub. To maintain the same impedance for the series inductive stub, the gap g_2 will have to be increased as well. Increasing g_2 and w_2 means w_1 will also increase; therefore, to maintain a 50Ω environment, gap g_1 will have to be increased.

A compromise was made to keep the overall dimensions as small as possible. The impedance of the series inductive stub was reduced. The gap chosen (g_2) is $35\mu\text{m}$, for an impedance of $59.7\mu\text{m}$. This would give an overall centre conductor width (w_1) of $110\mu\text{m}$, with a gap of $79\mu\text{m}$, to maintain the 50Ω environment. The stub dimensions are summarized in Table 3.4.

Table 3.4: Dimensions for the shunt C, series L folded stub configuration

	w_1	g_1	w_2	g_2	w_3
Dimensions (μm)	110	79	30	35	5

With the new dimensions given for the series inductive stub (and its new impedance), the calculated stub length is $281\mu\text{m}$ (using Equation 2.13).

The simulated lengths for the shunt and series stubs to obtain a 50Ω match are $106\mu\text{m}$ and $360\mu\text{m}$. The single shunt stub is much shorter than the calculated value and the simulated value in the standard configuration. The length of the stub can

be explained by considering the fringe capacitance of the metal strip used to connect the shunt stub to the ground plane and the centre conductor.

To estimate this fringe capacitance, a simulation was made of the connecting metal strip and these results were fitted to a simple shunt capacitor model. The simulated circuit is given in Figure 3.16. This circuit has the same general layout as the one in Figure 3.15, except that there is no shunt stub in the centre conductor, and also no series stub.

Figure 3.16: Circuit for estimation of fringe capacitance

The cross-hatched section in Figure 3.16 represents the overlap area of the metal strip connecting the ground planes and the centre conductor. This area forms a SiN + SiO₂ capacitor, whose capacitance can be estimated using supplied foundry data and models. The hatched area represents the fringe capacitance to be estimated.

The equivalent circuit for the planar circuit of Figure 3.16 is given by Figure 3.17. The simple circuit consists of two lengths of transmission line of different impedance and length and a shunt capacitance to ground.

The shunt capacitance to ground of Figure 3.17 has two major components:

Figure 3.17: Equivalent circuit for fringe capacitance estimation

1. The capacitance C_o of the overlap of the metal strip connecting the grounds and the centre conductor (the cross-hatched area in Figure 3.16), and
2. The fringe capacitance C_f of these two metals when there is no overlap (the hatched area in Figure 3.16).

If the overlap capacitance can be estimated, and the total capacitance is known, then the non-overlapping fringe capacitance can be estimated as well. Therefore:

$$C_{ft} = C_f + C_o \quad (3.3)$$

where C_f is the fringe capacitance and C_o is the overlap capacitance.

In Figure 3.17, the values used for the transmission lines are: $Z_{01} = 79.51\Omega$, $\epsilon_{eff} = 6.712$ and $\theta_1 = 7.32^\circ$; $Z_{02} = 50.186\Omega$, $\epsilon_{eff} = 6.840$ and $\theta_2 = 2.22^\circ$. The impedances and effective dielectric constants for the transmission lines were obtained by simulation.

The total shunt capacitance C_{ft} was estimated to be 0.029pF, by comparing the S parameters of the planar circuit and its model. Using foundry data and models, the overlap capacitance is estimated to be about 0.01pF. The fringe capacitance is then estimated to be $C_f = C_{ft} - C_o = 0.019\text{pF}$.

In the model of Figure 3.17, the inductance of the small length of line extending to the ground plane (the part that isn't hatched or cross-hatched) is neglected. This inductance is usually very small. It can be estimated by the following equation [83]:

$$L = \frac{Z_0 \sqrt{\epsilon_{eff}}}{c} \text{ [H/m]} \quad (3.4)$$

where ϵ_{eff} is the effective dielectric constant, Z_0 is the impedance of the line, and c is the speed of light in vacuum. With the line values given above, this would result in an inductance of approximately 16pH for a $39\mu\text{m}$ gap. This is extremely small, and has little impact on the circuit model. It should also be mentioned the net effect of the fringe capacitance is of interest here. The small line length extending to the ground plane may reduce the capacitance C_{ft} of the model, but since this length is present in all circuits considered, its impact has already been taken into consideration.

The shunt stub was simulated to a length of $106\mu\text{m}$ to obtain a 50Ω match. In a finite-ground coplanar environment, with the dimensions given, this would correspond approximately to a 58Ω stub (using conformal mapping). Using Equation 2.15, this would be equivalent to a capacitance of 0.015pF. The total shunt capacitance, in the circuit of Figure 3.15, would be from the shunt stub and the fringe capacitance, which would give a total of $0.015 + 0.019 = 0.034\text{pF}$. This is the same as the required value of 0.034pF necessary for a 50Ω match. The fringe capacitance is a gross estimate, but the total value of capacitance found supports the idea that the fringe capacitance contributes a significant part of the required shunt capacitance for the matching circuit. Another contribution to the capacitance comes from length extension [67], [68]. For the circuits used here, the length extension is approximately $5\mu\text{m}$ for all stubs.

The S parameters of the standard and folded configurations are given in Figures 3.18 and 3.19. The first plot (Figure 3.18) shows the amplitude of the S parameters. As was the case for the series L, shunt C configuration, there is very little difference between the amplitudes of the folded and standard configurations.

The phases of the S parameters are compared in Figure 3.19. There is an obvious discrepancy in the S_{11} and S_{22} phases, similar to the difference observed in the series L, shunt C configuration. The difference in phase is small for S_{12} and S_{21} .

Figure 3.18: Simulated S parameters (amplitude) of the folded and standard stub

Explanation for the varying lengths

To further explore the relationship between the lengths of the stubs in the standard and folded configurations, simulations were done on six other similar circuits. In each case, the starting point to be matched to 50Ω was slightly different. Table 3.5 summarizes the different lengths in the standard and folded case.

While this data may seem confusing at first, a number of observations can be made and some general design rules developed. First, the length of the shunt stub in the standard configuration is compared to the required value of capacitance to achieve a 50Ω match. The length given in Table 3.5 refers to the total length of line extending from the centre conductor to the end of the stub (see Figure 3.14). The actual length

Figure 3.19: Simulated S parameters (phase) of the folded and standard stub in the shunt C, series L configuration

Table 3.5: Lengths of shunt and series stubs in standard and folded configurations.

$Z_L (\Omega)$	Matching Circuit		Standard Stubs (μm)		Folded Stubs (μm)	
	C_m (pF)	L_m (nH)	l_{shunt}	l_{series}	l_{shunt}	l_{series}
$80 - j15$	0.0305	0.164	80	280	67	365
$80 - j5$	0.0362	0.158	100	272	131	357
80	0.0393	0.157	113	272	163	355
$80 + j5$	0.0425	0.158	122	273	185	365
$80 + j8$	0.0444	0.159	128	286	200	370
$80 + j15$	0.0488	0.164	143	300	236	385

of the stub is therefore given by

$$\Delta l = l_{shunt} - g_1 + l_{oc} \quad (3.5)$$

where l_{oc} is the length extension. For the circuits in Table 3.5, gap g_1 is $39\mu\text{m}$, and the length extension is $5\mu\text{m}$. Using Equation 2.15, the actual capacitance of the stub can be determined. Results for all stubs are given in Table 3.6.

Table 3.6: Capacitance of standard shunt stub

Stub Length (μm)	Equivalent Capacitance (fF)	Total capacitance needed (fF)	ΔC (fF)
80	6.98	15.24	8.26
100	10.04	18.08	8.04
113	12.05	19.63	7.58
122	13.45	21.23	7.79
128	14.38	22.20	7.82
143	16.74	24.42	7.68

The “missing” capacitance (ΔC) in Table 3.6 is roughly constant for each stub. It should therefore be related to the geometry of the circuit. Two things are constant for each shunt stub: the length extension and the underpass overlap. The length extension [68] can be estimated to about $5\mu\text{m}$. The underpass overlap creates a MIM capacitor to ground. Using foundry data and models, this capacitance is estimated to be about 3.4fF. Therefore, about 4.5fF of the 7.9fF (average) are unaccounted for. This capacitance is probably due to the fringing fields where the shunt stub enters the ground plane. The capacitance of the stub is therefore given by the following equation:

$$C_t = C_s + C_{underpass} + C_{fringe} \quad (3.6)$$

where C_t is the total capacitance needed, C_s is the actual capacitance of the stub, $C_{underpass}$ is the capacitance due to the overlap between the stub and the underpass,

and C_{fringe} is the capacitance due to the fringing fields at the point where the stub enters the ground plane.

Three of these capacitances are constant for all stubs regardless of the length of the stub (unless the stub is only slightly longer than the gap g_1).

The data from Table 3.5 can be plotted on a graph by comparing the percentage difference between the calculated value of the series and shunt stubs as a function of the length of the folded shunt stub. Figure 3.20 shows this data.

Figure 3.20: Percentage difference between calculated and simulated values of stubs as a function of folded shunt stub length

The first curve, labelled “Shunt Stub (folded)”, represents the difference between the calculated length of the folded shunt stub and its simulated value. The stub is much shorter than expected, due in part to the fringe capacitance contributing a significant amount to the capacitance. Since this fringe capacitance is constant, its effect is lessened as the required capacitance increases (and the calculated stub length increases).

The second curve, labelled “Series Stub”, shows that the series stub is consistently 30% longer than its calculated value. This could be attributed to coupling between the series stub and the ground connection for the folded shunt stub.

For the third curve, “Shunt Stub (folded) with fringe”, the effect of the fringe capacitance is taken into account. In this case, the capacitance compared is C_m (the capacitance needed for matching by an ideal lumped capacitor) to the sum of the capacitance of the stub and the fringe capacitance ($C_s + C_f$). There is little deviation from the expected value.

The final curve, “Shunt Stub with overlap”, is a plot of the data from Table 3.6. The percentage difference is the difference between the matching capacitance C_m and the sum of C_s , $C_{underpass}$, and $C_{l_{ext}}$ from Equation 3.6. In this case, the deviation remains mostly constant, and the difference can be attributed to the fringing fields at the point where the stub enters the ground plane, as explained above.

In general, the design procedure for this type of folded stub can be summarized as follows:

1. Determine the lumped element values for the shunt capacitor and the series inductor, either by simulation or calculation.
2. Using Equations 2.15 and 2.13, calculate the length of the stubs.
3. For symmetry reasons, it is better to use two shunt stubs rather than one; each will have half the length calculated above.
4. Simulate and extract the S parameters of the combined planar circuit.
5. Fold the shunt stubs as a single stub into the centre conductor; adjust the length as required by taking into account the fringe capacitance of the ground connection.
6. Adjust the length of the series stub to attain the required matching.

3.3.2 Series L, Shunt C Test Circuit

To validate the analysis presented in the previous section for the series L, shunt C folded stub circuit, a new structure was designed. A 100Ω impedance was chosen as the load impedance, to be matched to 50Ω , at 39.25GHz .

The ideal series L, shunt C matching network is a 0.2028 nH inductor and a 40.55fF capacitor. Using Eqs. 2.13 and 2.15, the calculated lengths of the stubs are $304\mu\text{m}$ for the series inductive stub (using an impedance of 71.8Ω), and $248\mu\text{m}$ for the single capacitive shunt stub (using an impedance of 51.2Ω), or $131\mu\text{m}$ for each of the dual shunt stubs.

If the analysis of the previous section is applied, for the standard stub configuration, for each of the dual shunt stubs, using Equation 3.6,

$$20.28 = C_s + 3.4 + 4.5 \quad (3.7)$$

where 3.4fF is the underpass capacitance, and 4.5fF is the fringe capacitance. Therefore, $C_s = 12.38\text{fF}$, which gives a stub length of $\Delta l = 81\mu\text{m}$ (using Eq. 2.15). The total stub length will be (using Eq. 3.5),

$$l_s = \Delta l + g_1 - l_{oc} = 81 + 39 - 5 = 115\mu\text{m} \quad (3.8)$$

The simulated length of the dual shunt stubs that matches the load to 50Ω is $113\mu\text{m}$.

For the series stub, if the finite ground planes are considered as the dominant effect, the stub impedance would not be 71.8Ω , but rather 58Ω . For a 58Ω stub, the stub length required to obtain a 0.2028nH inductance is $335\mu\text{m}$. The simulated length of the series inductive stub that matches the load to 50Ω is $345\mu\text{m}$.

For the folded series L, shunt C stub, the analysis of the previous section is applied as well. The total capacitance of the shunt capacitive stub is given by:

$$C = C_s + C_{fr} \quad (3.9)$$

where C_s is the stub's capacitance, and C_{fr} is the fringe capacitance (19fF). Using this equation, the capacitance needed for the stub is 21.55fF, which gives a length of $150\mu\text{m}$. With the length extension of the stub, the required length is $145\mu\text{m}$.

For the series L stub, the previous analysis showed the length in the folded configuration is about 30% to 35% longer than in the non-folded case. The calculated, non-folded length was $335\mu\text{m}$; adding an extra 32.5% gives a stub length of $444\mu\text{m}$.

The simulated length of the stubs (in the folded configuration) that matched the load to 50Ω is $450\mu\text{m}$ for the series L stub, and $150\mu\text{m}$ for the shunt capacitive stub. The results are summarized in Table 3.7.

Table 3.7: Calculated and simulated lengths of the folded series L, shunt C stub

	Standard		Folded	
	Calculated	Simulated	Calculated	Simulated
$l_{series} (\mu\text{m})$	335	345	444	450
$l_{shunt} (\mu\text{m})$	115	113	145	150

The circuit was fabricated by OMMIC in France, using their ED02AH process. The simulated and measured S parameters are given in Figure 3.21. There is very little difference between the simulated and measured S parameters.

Using the measured S parameters, the matching was verified with an ideal 100Ω load, giving a return loss of -19.2dB at 39.25GHz. A microphotograph of the fabricated circuit is shown in Figure 3.22.

The standard stub had dimensions of $366 \times 405 = 148230\mu\text{m}^2$, while the folded stub had dimensions of $268 \times 505 = 135340\mu\text{m}^2$, a reduction of 9% of the total surface area. The overall width of the circuit has been reduced by 27%, while the total length has increased by 20%.

Figure 3.21: Simulated and measured S parameters for the series L, shunt C folded stub

3.4 Summary

Coplanar waveguides offer interesting possibilities when designing matching circuits. The ability to fold shunt stubs into the centre conductor can reduce the overall width of a matching circuit; this was the main focus of this chapter.

Some test structures for common L-network matching circuits created using folded configurations have been presented. These test structures were fabricated and tested, and their performance compared to their classic configuration [82].

The folded structures do not behave exactly the same as their standard configuration, and these differences were investigated. The reduced ground plane of the folded stub is an important contributor to the difference between the standard and folded

Figure 3.22: Microphotograph of the series L, shunt C folded stub test circuit

structure. Also, the fringe capacitance of the line necessary to bring the ground plane to the centre conductor can also have an important impact on the folded configuration.

Overall, the main contribution was to show that folded stub structures can be used to reduce the size of matching circuits. This is one advantage of coplanar waveguide over microstrip in the design of MMICs.

Chapter 4

Design of a Coplanar Gilbert Cell Mixer

The design chosen in this work is similar to the one given in ref [34]. A half-Gilbert cell configuration was chosen, with one switching transistor grounded. The operation of the half-Gilbert cell with one switching transistor grounded is roughly the same as one with LO+ and LO- inputs, while giving a simpler layout (since only one LO input is needed) [84], [85]. The circuit will be designed to achieve maximum gain.

A schematic of the circuit is given in Figure 4.1.

Figure 4.1: Half Gilbert cell

The three transistors form the central core of the mixer. Transistor H_1 serves to amplify the RF input. Transistors H_2 and H_3 are switched by the LO.

4.1 Fabrication Process

The fab used to create the MMIC circuits is OMMIC¹, located near Paris, France. The process is proprietary and cannot be described completely here. However, many references are made later on in the text to certain layers or process procedures; a quick overview of the OMMIC process is explained here.

The OMMIC ED02AH process is a standard three metal process. The substrate is GaAs. The three metal layers will be referred to as **Metal1**, **Metal2** and **Metal3**. The standard naming scheme for integrated circuits has not been used here, where **Metal1** would typically be the lowest-level metal layer. The **Metal1** layer is the layer used for most of the design; it is the main transmission line layer, and the topmost metal layer of this process. The **Metal2** layer is the lowest metal layer. It is most often used as the bottom layer for capacitors. The **Metal3** layer is used as the top electrode in certain capacitors. Its depth lies between the top **Metal1** layer and the bottom **Metal2** layer. A simplified cross-section of the standard process is shown in Figure 4.2. The **Metal2** layer can be used as a transmission line layer, but its characteristics are less desirable than the **Metal1** layer, and so is rarely used for transmission lines. The **Metal3** layer is only recommended for use as a MIM capacitor metal.

Figure 4.2: Cross-section of OMMIC process; shown is a series MIM capacitor

There are two types of MIM (Metal-Insulator-Metal) capacitors available in this process.

¹Website: <http://www.ommic.com>

1. **Type 1:** These capacitors are the ones most used. They are constructed with the **Metal3** and **Metal2** layers, with a thin dielectric in-between. These capacitors have a thinner dielectric layer, and hence more capacitance per area. A hole is etched through the dielectric connecting the **Metal1** and **Metal3** layers.
2. **Type 2:** These capacitors use a thicker dielectric, and are made between the **Metal1** and **Metal2** layers. With a thicker dielectric, they represent smaller capacitances.

In all cases, the smallest capacitor recommended is $10\mu\text{m}$ by $10\mu\text{m}$, where the fringe capacitance is of the same order as the overlap capacitance.

Air bridges are in fact underpasses in this process. The **Metal2** layer is used to connect both ground planes and cross under the **Metal1** layer. The connection to **Metal1** is made with the CO layer. This connection can be seen in Figure 4.2. The connection is on the right of the figure, where the **Metal1** and **Metal2** are connected through the CO layer.

Inductors are formed with the **Metal1** layer as the main layout layer. The connection from the centre of the inductor to the rest of the circuit is made using the **Metal2** layer. The inductors are square, defined by their line width and separation (the gap between each line). A wider gap between the lines means a lower parasitic capacitance, however the inductor occupies more area.

Resistors are of two types: GaAs resistors and Nichrome (NiCr) resistors. For high resistances, the GaAs resistor is much better, as GaAs has a higher resistivity than NiCr, while the NiCr resistor is used for small resistances.

4.2 Characterizing the OMMIC pHEMT

The first step in the design was the characterization of the transistors used. The current-voltage (I-V) curves were analysed, as were bias points, gate and drain impedances and model limitations. The OMMIC pHEMT (pseudomorphic High Electron Mobility Transistor) was used in a test bench to obtain several I-V curves. These are shown in Figure 4.3. The large-scale (nonlinear) model of the transistor is used to obtain these values. The model is supplied by the foundry and is proprietary, and hence will not be shown here.

Figure 4.3: Device bias I-V curves

Tests were done at different values of V_{DS} to compare with the foundry-supplied curves. The results were the same as those provided by the foundry. The model is valid from $-1.2V \leq V_{GS} \leq 0.8V$ and $-5 \leq V_{DS} \leq 5V$.

A linear test bench was run to obtain the S parameters of the transistor (S_{11} , S_{12} , S_{21} and S_{22}). The terminating output of the drain was a 50Ω load. For the biasing

values given in ref. [34], a plot was constructed of input and output impedances for various device sizes (Figure 4.4). Port 1 is the gate of the FET while port 2 is the drain. The source of the FET was grounded. The results shown are for a 6-finger FET with widths varying from $10\mu\text{m}$ to $50\mu\text{m}$.

Figure 4.4: Smith chart of input and output impedances at 38.9GHz

4.2.1 Stability Analysis of the Transistor

The transistor's stability was analyzed to determine whether the transistor will self-oscillate. A linear analysis of the transistor's small-signal model gives the K and B_1 parameters. It is well known that the condition for unconditional stability is that $K > 1$ and $B_1 > 0$ [50]. Results show the transistor is unstable from approximately 30MHz to 70GHz.

To reduce the instability at higher frequencies, one can increase the transistor size; this will reduce the transistor's impedance. However, changing the transistor

size affects the current and biasing point, and for a device functioning in its nonlinear region, this change can have a drastic effect on performance. Another option is to add an inductive load at the source of the transistor [84]. A shorted transmission line was used to provide the inductive effect. Adding this transmission line reduced the point of higher instability from 70 GHz to approximately 25 GHz. A line of 70Ω with an electrical length of 15° produces the required effect for this particular transistor.

A RC network added at the drain will push the high frequency instability to even lower frequencies, while at the same time not permitting the circuit to become unstable again at even higher frequencies. However, this RC network has a big impact on gain.

As a final step in stabilizing the transistor, a shunt resistor to ground is added to the gate. This resistor will provide stabilization at lower frequencies [79]. Again, this stability is obtained at the expense of gain. The higher the resistor value used, the less the impact on the transistor's gain will be.

4.2.2 Current and Voltage Analysis of Mixer Core

To measure currents flowing through the transistors, a DC analysis of the central cell (consisting of the three transistors) was done. Testing the currents must be done with the Large-scale signal models. The DC voltage where the transistors turn on is approximately -0.9V, as is given in the OMMIC design manual. The plot of the current as a function of bias voltage is given in Figure 4.5.

As V_{GS} of H_1 increases beyond threshold ($V_t = -0.9V$), the transistor begins conducting current. From the current Gilbert cell configuration (Figure 4.1), the current in H_1 equals the sum of the currents in H_2 and H_3 .

$$I_{H1} = I_{H2} + I_{H3} \quad (4.1)$$

Figure 4.5: Current in the transistors of the half Gilbert cell

where $I_{H_2} = I_{H_3}$ since the devices are of the same size. One would expect the drain-to-source voltage in the transistors to be half the supply voltage, equally distributing the supply voltage between the two stages. However, since $I_{H_1} = 2 \times I_{H_2}$, the current imposes the condition that the voltages must stabilize to this point.

Comparing the results with [34], it is not mentioned that the point joining H_1 and H_2 (and H_3) is supplied by a second voltage source. At those levels, to get ~ 10 mA in the bottom transistor and ~ 0 mA in the top transistors, and maintain the mentioned bias point, there has to be a source at the centre point. If there is not, it is impossible to get a current in H_1 that is more than twice the current in the top branch (H_2 or H_3). So the 3.2V supply added in provides the current for the lower *amplifying* transistor.

A higher current in the lower branch provides more amplification of the RF signal, and hence possibly enhances the conversion gain of the mixer. However, there are

many parameters that can affect the overall conversion gain. Transistor size and bias points affect the S parameters of the centre core of the mixer. Each transistor's S parameters will change depending on these parameters, which can affect the matching between the bottom transistor (H_1) and the top transistors (H_2 and H_3). To optimize the conversion gain of the mixer, the following steps were performed.

1. Keep RF and LO power fixed. Vary bias points and measure gain.
2. Vary LO power, measure effect on conversion gain.
3. Measure gain for different transistor sizes.
4. Verify operation in triode region for the top transistors. This is usually not used, since this means higher current and hence more power dissipation.

RF and LO Power Level Fixed

After stabilizing the circuit, results show limited gain. With the circuit stabilized, results of varying the bias while keeping the RF and LO levels fixed are shown in the following tables.

Table 4.1 shows the output IF power as a function of the drain bias of transistor H_1 .

Table 4.1: Variation of V_{D2}

$V_{GS1}(V)$	$V_{DD} (V)$	$V_{D1} (V)$	$I_1, I_2 (mA)$	$P_{IF} (dBm)$
-0.35	4.80	3.00	7.0, 0.03	-61.44
-0.35	4.80	3.15	7.0, 0.03	-59.30
-0.35	4.80	3.20	7.0, 0.03	-59.20
-0.35	4.80	3.25	7.0, 0.03	-59.36
-0.35	4.80	3.30	7.0, 0.03	-59.67
-0.35	4.80	3.40	7.0, 0.03	-60.65

Table 4.2 shows the IF output power as a function of the gate bias voltage of transistor H_1 . In this case, the higher the gate bias, the higher the IF output of the mixer.

Table 4.2: Variation of V_{GS1}

$V_{GS1}(V)$	$V_{DD} (V)$	$V_{D1} (V)$	$P_{IF} (dBm)$
-0.70	4.80	3.20	-59.30
-0.50	4.80	3.20	-59.26
-0.45	4.80	3.20	-59.25
-0.40	4.80	3.20	-59.24
-0.30	4.80	3.20	-59.20
-0.25	4.80	3.20	-59.20
-0.20	4.80	3.20	-59.20
+0.20	4.80	3.20	-59.10
+0.60	4.80	3.20	-59.00

In Table 4.3, the IF output power as a function of the gate bias of transistors H_2 and H_3 is shown.

From these tables, the optimum values are $V_{D1} = 3.2V$, $V_{GS1} = 0.6V$, and $V_{G2,3} = 2.45V$. However, if $V_{GS1} = +0.6V$, the transistor is close to the model limitations, and the current is very high. For a small drop in gain, the transistor can operate at a much lower current.

Varying Transistor Size

The transistor sizes were varied to obtain the maximum gain. However, this affects the biasing point, and could mean that the simulations and results of Tables 4.1, 4.2 and 4.3 will need to be redone.

From Table 4.4, optimum gain is achieved when the lower transistor (H_1) is of a biggest size ($6 \times 50 \mu m$) and the switching transistors (H_2 , H_3) are smaller ($4 \times 10 \mu m$).

Table 4.3: Variation of V_{G2}

$V_{G2}(V)$	$V_{DD} (V)$	$V_{D1} (V)$	$P_{IF} (dBm)$
2.00	4.80	3.20	-60.92
2.10	4.80	3.20	-60.67
2.25	4.80	3.20	-59.93
2.30	4.80	3.20	-59.66
2.35	4.80	3.20	-59.40
2.40	4.80	3.20	-59.23
2.45	4.80	3.20	-59.20
2.50	4.80	3.20	-59.30
2.60	4.80	3.20	-60.20
2.80	4.80	3.20	-66.40

The results are slightly unexpected. A bigger transistor has less resistance, and hence can provide more gain. This works well for transistor H_1 , whose purpose is to amplify the input RF signal. However, for the switching transistors, smaller transistors can handle less current and provide less gain. It is possible the smaller size matches better to the amplifying transistor.

4.3 Matching

Matching is an important part of the design process, especially at higher frequencies. Matching can have a huge impact on gain, since the input power should flow to the transistor, and not be reflected.

4.3.1 Transistor Matching

A first step in matching is matching the output of the bottom amplifying transistor and the source of the top switching transistors. It would be unreasonable to match

Table 4.4: Variation of transistor sizes; effect on gain

Bottom transistor (H_1)		Upper transistors (H_2, H_3)	
Size (μm)	P_{IF} (dBm)	Size (μm)	P_{IF} (dBm)
2x40	-59.23	4x10	-38.11
2x30	-61.38	4x20	-44.72
2x20	-64.85	4x30	-49.06
2x10	-71.96	4x40	-52.34
6x50	-52.97	4x50	-54.82
6x40	-53.56	4x60	-56.84
6x30	-54.62	6x50	-59.23
6x20	-56.65	6x40	-56.79
6x10	-61.37	6x30	-53.75
4x30	-56.68	6x20	-49.52
		6x10	-45.63

both terminals to 50Ω , which would mean having two matching circuits. A conjugate match will therefore be performed. This means S_{22} of H_1 will see its conjugate in S_{11} of the two parallel switching transistors.

A linear test bench simulation of the input and output S parameters of the transistors shows how matching needs to be done. From the plot of the S parameters, a transmission line was added between H_1 and H_2 (H_3) to provide matching. This transmission line was then optimized to provide maximum output at the drain of the switching transistors. After optimization, a 60Ω , 30° transmission line at 38.9GHz was chosen.

4.3.2 Input and Output Matching

Matching the input and output ports of the devices follows the same standard procedure used in any other impedance-matching problem. A plot of the S_{11} and the S_{22}

parameters was generated, and then passive reactive components were used to match to 50Ω . Matching at the RF port consists of a series inductor of 0.27nH and a shunt capacitor of 0.05pF . The 0.05pF capacitor is too small to be physically realizable with a MIM capacitor (based on the process being used), but this value will be retained until the layout process is begun and other options are considered. At that time, the matching values will probably need to be changed, so this small capacitance value will most likely be different.

For matching the LO port, a 0.33nH inductor and a 0.21pF capacitor were used. These values are easily realizable with the current technology, and pose no layout problems.

The matching at the IF port consists of a 23.5nH inductor and a 0.9pF capacitor. Here again, one of the values is not physically realizable: the inductor. The same solution to the RF matching will be used: the value will stay, until the layout of the circuit becomes more defined, and then this value will most likely change.

4.3.3 IF Output

The IF output, at this stage in the design, is not configured properly. The outputs are simply connected together, and since the output of H_3 is theoretically 180° out of phase of the IF signal at H_2 , the signals cancel each other out. So a balun of some sort needs to be added, or a 180° phase shifter used so the signals add up.

At the IF output, the RF and LO signals leaking out through the output should be filtered. A low-pass filter (LPF) must be added at the drain of H_2 and H_3 to block out the higher frequencies ($37+\text{GHz}$), while letting the IF get through. Alternatively, a short circuit at the higher frequencies will reflect the signals back into the devices, while letting the IF through. A 1pF capacitor is used at the drain of H_2 and H_3 . This means the impedance of this capacitor is $4.3\text{m}\Omega$ at 37GHz , while at 1GHz , it is $159\text{m}\Omega$.

With all these changes, the output of the circuit, using an ideal 180° phase shifter, is -17dBm for an input RF signal of -20dBm, a gain of 3dB. If the combined output of the IF port is matched to 50Ω , then the circuit has 6dB of gain.

4.3.4 Transistor Sizes

With the circuit matched, and all components in place, the design was optimized. Varying the transistor sizes and biasing again will optimize the output.

Plots of output power versus transistor sizes show the output is maximum when the switching devices H_2 and H_3 are $4 \times 20\mu\text{m}$. Maximum output is achieved when these devices are biased at $V_{GS} = -0.9\text{V}$. For the lower device, optimum output is obtained when $V_{GS} = -0.1\text{V}$. However, when H_1 is biased at -0.1V, for a transistor of $6 \times 50\mu\text{m}$, the current is approximately 60mA, which is too much. From the plot of the output power versus bias for H_1 , by going to -0.5V, only 0.4dBm of output power is lost, while the current drops to 11.7mA. The 0.4dBm loss in output power is acceptable for a 6X drop in current.

4.4 Phase Shifter

The phase shifter currently used in the simulations is an ideal 180° phase shifter. To design a component to do this shifting, a few options are considered. The first one is a passive shifter [86]. From [86], two configurations are possible. They both will require three inductors and three capacitors. If this circuit was being used to provide a phase shift of less than 180° , it is possible that one configuration would be of smaller dimensions than the other, since the components in each branch would be different.

For a 180° shifter, the components are the same. The equations given in [86] are:

$$X_n = \tan\left(\frac{\Delta\phi}{4}\right) \quad (4.2)$$

$$B_n = \sin\left(\frac{\Delta\phi}{2}\right) \quad (4.3)$$

where

$$X_n = \frac{\omega L}{Z_0} \text{ and } B_n = \omega C Z_0 \text{ for a low-pass filter} \quad (4.4)$$

and

$$X_n = \frac{1}{\omega C Z_0} \text{ and } B_n = \frac{Z_0}{\omega L} \text{ for a high-pass filter} \quad (4.5)$$

A table published in the document gives the values for X_n and B_n for a 180° shift, which is 1 for both. So, for a 1GHz IF:

$$X_n = 1 = \frac{\omega L}{Z_0} \Rightarrow L = \frac{50}{\omega} = 7.98nH \quad (4.6)$$

and

$$B_n = 1 = \omega C Z_0 \Rightarrow C = \frac{1}{50\omega} = 3.18pF \quad (4.7)$$

An 8nH inductor is too big to be of practical value in this design. Another option must therefore be considered.

4.4.1 An Active 180° Phase Shifter

An active circuit can also be used to provide phase shift. The well-known common-emitter configuration provides 180° of phase shift. The circuit is shown in Figure 4.6. However, a simple use of the common-emitter circuit will not be of use, since stability tests show this circuit to be unstable at 1 GHz. It must therefore be stabilized before being used in the Gilbert cell circuit. A 35Ω feedback resistor between the gate and source will stabilize the transistor. With a 50Ω drain resistor and a 12Ω source resistor, this circuit provides 180° of phase shift and 0dB of gain.

Figure 4.6: Active phase shifter

Inserting this phase shifter into the half Gilbert cell circuit results in -6dB of conversion gain. This means matching must be done at the input and output of the phase shifter. A stability analysis shows the complete circuit is stable.

4.5 Active Balun

Rather than using an active 180° phase shifter and a Wilkinson coupler to combine the two IF signals, an active balun was pursued. The Wilkinson combiner would have been too large, since at 1GHz, 11nH inductors would have been required. An active balun circuit is proposed in ref [87]. The circuit is given in Figure 4.7.

All the parameters of the components of the active balun were optimized: transistor size, R_G , R_S and R_D were optimized to get maximum signal power at the output. Table 4.5 shows the optimized parameters for the different components.

The matching circuit was obtained by varying the output S parameters of the half-Gilbert cell and then matching to the conjugate. A 3.8pF capacitor was added at the drain of the switching transistors, while a 5.17nH inductor was put at the input of the active balun. So S_{11} of the active balun is now the conjugate of S_{22} of the half-Gilbert cell.

Figure 4.7: Active balun

4.6 Stability and Gain

From the plots of the conversion gain, the gain is reduced by a significant amount at the output. The problem is caused by the stabilizing network connected to the drain of the switching transistors. The stabilizing RC network reduces the gain significantly. While it helps to match the output of the transistor, it has a detrimental effect on the gain.

To reduce this effect, the stability of the circuit was examined again. Since many lossy components have been added, these will increase the stability of the circuit.

With all the added components, and a slight modification to the transmission line between the drain of H_1 and the source of H_2 and H_3 , the circuit is stable.

The final schematic for the half-Gilbert cell is shown in Figure 4.8.

4.6.1 Bandwidth Issues

A suitable bandwidth must be chosen in which the circuit must operate; it is good to design for high frequencies, but the circuit must have a practical application.

Table 4.5: Optimized parameters of the active balun

Component	Optimized value
H_4	$4 \times 25 \mu\text{m}$
H_5	$4 \times 25 \mu\text{m}$
H_6 (current source)	$6 \times 50 \mu\text{m}$
H_7 (output transistor)	$6 \times 25 \mu\text{m}$
R_G	400Ω
R_S	100Ω
R_D	900Ω
R_{S_O}	50Ω
V_{GG}	-0.35V

The Canadian Radio-television and Telecommunications Commission (CRTC) is the governing body in Canada with regards to bandwidth issues. The CRTC allocates and monitors all radio spectrums. A recently allocated satellite band exists from 38.7 GHz to 39.8GHz for upload and download (see <http://strategis.ic.gc.ca/>). The half-Gilbert cell circuit should produce as flat a gain as possible in this range, centred at 39.25GHz.

4.7 Layout of the Circuit

All coplanar circuit elements, running at 37GHz and above, must be simulated using an electromagnetic simulator. Momentum© is a 2.5D electromagnetic simulator used in HP's ADS© software package. Electromagnetic (EM) simulation is needed to ensure the layout of the circuit and the schematic simulation are the same. EM simulations take into account the coupling between different elements, as well as being more precise than the schematic simulations. However, the downside is these simulations take longer, sometimes in excess of 24 hours to simulate a complex circuit.

Figure 4.8: Schematic of the half Gilbert cell

4.7.1 Stabilizing Transmission Line

The first component simulated with Momentum© is the transmission line that stabilizes the amplifying transistor (H_1). This line is a 100Ω , 30° line at 39.25 GHz (see Figure 4.9).

However, coplanar circuits operate much better if their design is symmetrical with regards to the direction of propagation; this prevents the excitation of the parasitic slotline mode [12]. To maintain the symmetry of the layout, the amplifying transistor

Figure 4.9: Schematic of transmission line at H_1 's source

will have two sources. With a two source device, the transmission line at the source must be modified as well, and the impedance of the device will change. One possible configuration is to use two 200Ω lines in parallel, as shown in Figure 4.10.

Figure 4.10: Transmission line at H_1 's source with two lines

However, a 200Ω line cannot be realized on a circuit; a $10\mu\text{m}$ wide line would require a gap of $2500\mu\text{m}$, and even then, this calculation is an extrapolation of current equations and most certainly erroneous. This is not realizable with this technology. The technology limits waveguides to approximately 110Ω .

A grounded transmission line has an input impedance of [79]

$$Z_{in} = jZ_0 \tan(\beta l) \quad (4.8)$$

If the same line impedance is chosen (100Ω), then the length of line needed to produce twice the input impedance is given by:

$$j100 \tan\left(\beta \frac{\theta}{360}\right) = 2j100 \tan\left(\beta \frac{30}{360}\right) \quad (4.9)$$

Solving this equation gives a line length of $\theta = 49^\circ$. This circuit is shown in Figure 4.11.

Figure 4.11: Dual transmission lines at H_1 's source, optimized

The 200Ω , 30° line can be replaced with two 100Ω , 50° lines. Simulation of these two lines gives the same results as the one 30° line. In order to reduce the gap needed to produce a 100Ω impedance, a $10\mu\text{m}$ wide line is chosen. The line could have been made smaller, but these lines will carry all the current of the amplifying transistor to ground. Foundry documentation shows the **Metal1** lines can support $6\text{mA}/\mu\text{m}$, whereas the **Metal2** layer can only support half as much ($3\text{mA}/\mu\text{m}$). If a transition to **Metal2** is ever needed, this drop in current density must be taken into consideration. Table 4.6 shows different gaps, widths and lengths to produce a 100Ω , 50° line.

Table 4.6: Physical dimensions for a 100Ω , 50° transmission line.

Width (μm)	Gap (μm)	Length (μm)
10	97.8	416.5
20	191.4	417.6
30	280.1	419.5

From Table 4.6, the gap increases significantly as the line width is increased (roughly doubling the gap for a doubling of the width). And since there exists a gap on each side of the line, the total area of this component can increase rapidly.

By comparison, a 50Ω , 50° line $10\mu\text{m}$ wide requires a gap of $8.9\mu\text{m}$ and a length of $433\mu\text{m}$. All measurements were done with LineCalc©, a tool available with ADS for calculating line gaps and impedances.

Once the layout of the line was simulated, the S parameters were generated by Momentum©. These S parameters were then saved to a file to be used by the circuit simulator. The S parameters are used in the circuit simulator to ensure the behaviour and performance are the same as in the ideal element case that existed previously. Some tweaking of the simulated layout was done so the layout and schematic element agree. This means re-simulating to obtain the desired response.

The optimized transmission line is given in Figure 4.12. The corresponding S parameters of the line from 1GHz to 45GHz are shown in Figure 4.13.

Figure 4.12: Layout of transmission line at H_1 's source

4.7.2 Layout of the RF Input Circuit

The next component to be modeled in layout is the input RF circuit. This consists of the stabilizing resistor and the transmission line that connects the resistor to transistor H_1 . A $50\mu\text{m}$ wide line was chosen at this point, because it connects better to the gate of the $6\times 50\mu\text{m}$ transistor. For a $50\mu\text{m}$ line, the gap must be $36\mu\text{m}$ for a 50Ω

Figure 4.13: S parameter of H_1 stabilizing line

impedance. The layout is given in Figure 4.14. A $20\mu\text{m}$ wide resistor was chosen, with a length of $100\mu\text{m}$ to give 1000Ω . The GaAs resistor is limited to $0.075\text{V}/\mu\text{m}$ of length (from the design manual of the fab process). In this case, the resistor is limited to a maximum of 7.5V difference between its two terminals. Since the biasing at the gate is -0.35V , and the gate draws very little current, the voltage limitation will not be exceeded.

Figure 4.14: Layout of RF input circuit

A 5pF capacitor has been added between the resistor and ground to block any DC current from flowing through the resistor to ground. Since this resistor is used to stabilize the higher frequencies, the stability will not be affected by adding this capacitor. At 39.25GHz , the 5pF capacitor represents an impedance of only 0.8Ω ; the effect is negligible on the RF.

EM simulation results are very similar to those of the circuit simulation. Few modifications were needed to the circuit. The S parameter plot of the RF input circuit is given in Figure 4.15.

Figure 4.15: S parameters of the RF input circuit

As can be seen in Figure 4.15, the circuit functions correctly. S_{11} is high at DC, indicating the DC blocking capacitance is working properly. S_{21} is very low at DC, meaning no DC voltage can get to port 2, while at 39GHz it is close to 0dB, indicating the RF input is getting through.

RF Matching

By looking at the input S parameter plot of the RF input circuit, it was determined the matching could be done using a transmission line and shunt capacitors. The transmission line rotates the impedance around the centre of the Smith chart, and the shunt capacitance will then move the impedance to 50Ω .

At 39GHz, it is better to use stubs rather than capacitors to provide capacitance, if the capacitance value required is small. A stub will be less affected by process variation than a capacitor. If a hole appears in the dielectric between the top and

bottom electrodes, the capacitor is of no use. If the same thing happens to the stub, it is still useful.

Two stubs will be used, in order to maintain the symmetry of the circuit. The stub length required is calculated using Equation 2.15.

4.7.3 LO Circuit

The LO input circuit consists of two sections: the stabilizing RC network, and the matching network. Both of these circuits need to be designed separately, and then integrated together.

Stabilizing Circuit

The RC network is the first circuit of the LO input that will be put to layout. The resistor provides stability at lower frequencies, while the capacitor provides a low impedance path for the LO frequency. A straight layout of the circuit as presented in a schematic diagram would give a layout with the central conductor splitting in two, and then each component would be placed, with a ground in between. Figure 4.16 shows this design. However, the RC network can be simplified if the resistor and the capacitor can be put on the same line.

Some problems are visible by looking at Figure 4.16. The central line will be a 50Ω line, and to maintain this impedance, the resistor and capacitor will have to be made small. So the standard $50\mu\text{m}$ wide line must be made wider to accommodate both the resistor and the capacitor. If the conductor is too wide, however, the gap increases correspondingly, and so does the surface area taken up by this circuit. Table 4.7 shows some possible combinations for the centre conductor width and the corresponding gap needed to maintain a 50Ω impedance.

The resistor in the RC network is 2000Ω , and the capacitor is 1pF . The widths of the components will need to be determined, as well as the minimum spacing between

Figure 4.16: Preliminary layout of the RC network

Table 4.7: Widths and gaps for a 50Ω line

Width (μm)	Gap (μm)
50	36
60	44
70	50
80	57
90	64

each, in order to determine the centre conductor width.

Coplanar circuits should be designed as symmetrical as possible, to ensure that no unwanted modes are excited [12]. So the proper layout of the RC network is to use two resistors in parallel with the capacitor. The resistors will have a value of $2R$.

Table 4.8 shows the possible lengths and widths necessary to obtain a 1pF MIM capacitor. The minimum size of the capacitor is $10 \times 10 \mu\text{m}$. The maximum voltage that can be applied to the capacitor without breakdown is 15V .

To design the resistor, maximum currents and voltages must also be taken into

Table 4.8: Widths and lengths for a 1pF capacitor

Width (μm)	Length (μm)
10	201
15	143
20	111
25	90
30	76
35	65

account. Table 4.9 shows different values of resistor, with their length, maximum current and maximum voltage.

The original design was a 2000Ω resistor providing stability to the circuit. If the resistors are too wide, they require more length to get an equivalent resistance. A compromise was made between width and length. Also, the capacitor models are only valid if the width to length ratio is 3:1 (from foundry data). For a 1 pF capacitor, from Table 4.8, the minimum width for a 3:1 ratio is $30\mu\text{m}$ (for a length of $71\mu\text{m}$). The capacitance value is determined by the overlap of the `Metal3` and `Metal2` layers. The design rules for the construction of the capacitor will add another $7\mu\text{m}$. If a minimum length of transmission line is wanted, the resistors must be as close as possible to $78\mu\text{m}$. From Table 4.9, a good choice of resistor that gives good current and voltage characteristics is a 1500Ω , $15\mu\text{m}$ wide resistor.

Two 1500Ω resistors in parallel will only represent a 750Ω resistance. The input will need to be redesigned and verified to see if a 750Ω resistor is enough to ensure stability.

A stability analysis shows that a 750Ω resistor is enough to ensure the circuit is stable up to 80GHz. Figure 4.17 shows the K and B_1 parameters, respectively. Alternatively, the μ parameter [88] may be used; simulations show $\mu > 1$ for all frequencies.

With the proper resistance values calculated, the two 1500Ω resistors can be added

Table 4.9: Physical dimensions and maximum ratings for different resistors.

Resistance (Ω)	Width (μm)	Length (μm)	Maximum Current (mA)	Maximum Voltage (V)
1500	10	67.7	3.4	5.1
	15	106.2	5.3	8.0
	20	144.6	7.3	10.8
2000	10	90.8	3.4	6.8
	15	142.1	5.3	10.7
	20	193.3	7.3	14.5
3000	10	136.9	3.4	10.3
	15	213.8	5.3	16.0
	20	290.8	7.3	21.8
4000	10	183.1	3.4	13.7
	15	285.6	5.4	21.4
	20	388.2	7.3	29.1

to the layout. Figure 4.18 shows the completed layout (not to scale) of the RC network.

LO Matching

A bypass capacitor must be added to the LO input circuit to block all DC currents from leaking out through the input. This bypass capacitor should be large enough so it has little impact on the input. For a $70\mu\text{m}$ wide transmission line, to maintain the 50Ω impedance of the line, a $66\mu\text{m}$ wide capacitor must be used. If the length of the capacitor is $100\mu\text{m}$, the capacitance is 2.7pF , which represents a 1.6Ω impedance.

Looking at the input S parameters of the circuit at the LO input, matching can be achieved with a transmission line and a shunt stub (or parallel capacitors). A $63\mu\text{m}$ long line with two $43\times 45\mu\text{m}$ (0.85pF) capacitors provides 50Ω matching.

Figure 4.17: Plot of K and B_1 vs frequency for the centre cell

Figure 4.18: Layout of the RC network

Transistor Matching Line

The transmission line that matches the amplifying transistor to the switching transistors needs to be added to the layout. A 60Ω , 30° line was found to be the optimum. Figure 4.19 shows the conversion gain for different impedances and line lengths. The spacing between the ground planes was modified to obtain the 60Ω impedance. Currently, there is a $50\mu\text{m}$ wide line connected to the gate of the amplifying transistor. The gap for a 50Ω line is $37\mu\text{m}$. To maintain the same dimensions, that is a total separation of $37 + 50 + 37 = 124\mu\text{m}$ between ground planes, the centre conductor will be $32\mu\text{m}$ wide for the matching line, and the gap will be $46\mu\text{m}$ (for 60Ω).

Figure 4.19: Conversion gain vs electrical length of interstage matching line

The matching line will connect the amplifying transistor's drain with the two switching transistor's sources. The width of the $4 \times 20\mu\text{m}$ transistors is $39\mu\text{m}$, and

distance from the device to the transistor should be $15\mu\text{m}$ to minimize coupling. This means that the total distance between grounds at the point where the two switching transistors are located must be at least $108\mu\text{m}$ plus the width of the line. If the line width increases to $40\mu\text{m}$, then the gap must be $54\mu\text{m}$.

4.7.4 Layout of the Active Balun

The layout of the active balun should be fairly simple, since its operating frequency is 1GHz. At 1GHz, the lengths of the lines are not that important since they represent a very small phase shift.

A problem arose when replacing the ideal components in the circuit schematic with their equivalent OMMIC-supplied elements. When the matching shunt inductors were replaced with their OMMIC equivalent, a big drop in gain (10 dB) was noticed. Further investigation helped to determine the problem.

By replacing the OMMIC inductors with a circuit consisting of its equivalent model, and calculating the component values for the elements, and then eliminating them one by one, the small resistor is found to be the problem. The resistance in the inductor comes from the length of the component.

Table 4.10: Physical parameters of a 5.17nH inductor

C_p	6.8 fF
C_{metal1}	75 fF
C_{metal2}	49 fF
Line inductance	0.23nH
Series inductance	4.7nH
Resistance	10.87Ω
Resonance frequency	9.82 GHz
Total length	3.8mm

The parameters of the OMMIC inductor are given in Table 4.10. If the output

impedance of the half-Gilbert cell were high, then the 10.87Ω resistor would have little impact on the matching. But since the matching is being done on the low-impedance side of the Smith chart, the impact is much greater. The impact of the 10.87Ω resistor can be seen in Figure 4.20. Point A on the figure is the S_{22} value or output impedance of the half-Gilbert cell. Point B represents the S_{11} parameter or input impedance of the active balun with an ideal inductor. Point C is the input impedance of the active balun with the 10.87Ω resistor. The input impedance of the active balun has moved from point B to point C with the addition of a small resistor. The mismatch caused by such a small resistor is quite high.

Figure 4.20: Smith chart plot of the input impedance of the active balun and the output impedance of the half Gilbert cell

Since the mismatch is so high, the shunt inductor has been removed, resulting in

higher gain for the total circuit.

The same problem arose at the output of the active balun. The matching at the output used a shunt inductor as well. Replacing the ideal inductor used in the simulations by the OMMIC-modeled inductor produced a large drop in gain. Again, it was determined that the output was better if no shunt inductor were used. The output was matched as close to 50Ω as possible, without using shunt inductors, but a relatively large mismatch still occurs.

4.7.5 Bias

With the circuit properly laid-out, the next step was to add the bias lines. The bias lines will probably affect the layout; up to this point, they have not been taken into consideration for the layout. Figures 4.7 and 4.8 show the bias lines needed. The parts of the circuit that need bias are:

- Gate of transistor H_1
- Drain of transistor H_1
- Gate of transistor H_2
- Gate of transistor H_3
- Drain of H_2 and H_3
- Gate of transistors H_4 and H_5
- Drain of transistors H_4 , H_5 and H_7

For all these bias lines, S parameter plots are shown. On these plots are also included the S_{21} and S_{31} curves, for completeness of information.

The bias line for the gate of transistor H_1 will be fairly simple to add. The line will be added to the capacitor between the 1000Ω stabilizing resistor at the RF input and the ground. The capacitor needed to be redesigned, however. Since the capacitor provides an RF ground, it can be used to ensure that no RF leaks out through the DC bias line, and that everything works as if there were no bias line at that point. The DC bias line will be made on the **Metal1** layer, and will connect to the top plate of the capacitor. The bottom layer of the capacitor, the **Metal2** layer, will connect to ground. The capacitance (from an RF point of view) will remain the same (actually it is better, since both sides of the capacitor are connected to ground). The DC bias ignores the capacitor, and a straight, DC connection exists to the gate of the transistor. Figure 4.21 shows the layout of the circuit. Transistor H_1 is connected to port 2 (in Figure 4.21).

Figure 4.21: Layout of gate bias circuit for transistor H_1

The simulated S parameters of the H_1 gate bias circuit are shown in Figure 4.22. The circuit's behaviour is as expected:

Figure 4.22: S parameter plot of H_1 biasing circuit

- S_{11} is 0dB at DC, indicating no DC current is getting through port 1.
- S_{21} is close to 0dB at 39GHz, indicating the RF input is getting to the gate of H_1 with little attenuation.
- S_{31} at DC is very low, indicating no DC current is getting through port 1. At 39GHz, S_{31} is very low, indicating no signal is leaking through the DC bias circuit.
- S_{32} at DC is around -20dB, indicating the 1000Ω resistor is affecting the circuit while letting current through. At 39GHz, S_{32} is very low, indicating no signal is leaking through the DC bias circuit.

Biasing the Drain of H_1

Biasing the drain of transistor H_1 is a bit trickier. In the schematic simulation of the circuit, the bias line connects directly to the drain of the transistor. From Figure 4.23, this will be impossible because of the stabilizing transmission lines at the sources of H_1 . The line was connected as close as possible to the drain of H_1 , in order for the layout to be as close as possible to the schematic circuit diagrams. However, sufficient ground plane must be maintained between the edge of the gap for the stabilizing ground and the bias line, further pushing the bias line connection point away from the drain of the transistor. This will affect the matching transmission line between the drain of H_1 and the source of H_2 and H_3 .

Figure 4.23: Layout of the H_1 drain biasing circuit

It was determined through simulation that an $80\mu\text{m}$ distance should be enough to ensure proper ground. The matching transmission line is now of different geometry;

it has a T in the centre. The line was simulated again, as a 3-port device, to ensure the effect the T has on its matching is minimal. If the effect is significant, the line will need to be redesigned to obtain the best matching possible.

After simulating the new 3-port device, the effect on the matching of the transistors was significant enough to warrant redesign of the line. Multiple variations of the line length were tried in order to maximize gain at the output of the complete circuit. A total line length of $400\mu\text{m}$ gave best results, with a distance of $250\mu\text{m}$ between the drain of transistor H_1 and the connecting point of the bias line.

The bias line is a $\lambda/4$ transmission line at 39.25GHz. For the current process, this means a quarter-wavelength line is roughly $760\mu\text{m}$ at that frequency. The length was optimized to give maximum gain at the output; final length is $730\mu\text{m}$. To reduce circuit size, the line was not made simply straight; it was bent at a few places in order to take advantage of the relatively wide ground plane. The optimized layout of the circuit is given in Figure 4.23, while the S parameter plot is shown in Figure 4.24.

Again, the S parameter plot of Figure 4.24 can be examined to ensure the circuit is functioning properly.

- S_{11} is low at DC, indicating DC current is getting through to port 1 (the drain of H_1).
- S_{21} is close to 0dB at 39GHz, indicating the RF input is getting to the source of H_2 and H_3 with little attenuation.
- S_{31} and S_{32} at DC are relatively high, indicating DC voltage is getting to ports 1 and 2. At 39GHz, S_{31} and S_{32} are very low, indicating no signal is leaking through the DC bias circuit.

Figure 4.24: S parameter plot of H_1 drain bias circuit

Biasing the Gate of H_2

The gate of H_2 must also be biased with the 2.3V DC source. For testing purposes, the probes used to deliver the bias must be at the bottom of the circuit. Since there are only 4 sides to the circuit, and that three of those sides are taken up by the RF, LO and IF probes, the only free space remaining is at the bottom.

One possibility to deliver the bias to the gate of H_2 is to go under the matching transmission line by making use of the `Metal2` layer, and then connecting directly to the gate. This represents a serious problem, however. By crossing under the matching transmission line, a capacitance would be created between the `Metal2` layer and the `Metal1` layer. The line would cross under the portion of the line that is $40\mu\text{m}$ wide. The capacitance of a $10 \times 40\mu\text{m}$ capacitor between the `Metal2` and `Metal1` layers is 25fF. This represents an impedance of 162Ω at 39.25GHz. This is enough to possibly affect the circuit performance.

Another possibility is to run the bias line all around the right side of the circuit and come back down on the 1GHz side of the circuit. If a Metal2-Metal1 crossing is needed, at 1GHz the impedance of a $10 \times 10 \mu\text{m}$ Metal2-Metal1 capacitor is $22.8\text{k}\Omega$. This is high enough so little impact should be felt on the circuit performance.

The closest point of connection for the DC bias line at the LO input is between the RC network and the stabilizing network. A DC blocking capacitor is added between these two parts of the circuit to ensure that no DC feeds through the LO input. The DC bias line for this part of the circuit will consist of a $\lambda/4$ transmission line terminated by a 5pF capacitor. This will ensure a proper ground for any 38GHz signal trying to leak out through the DC bias. The bias line will run on top of the capacitor, just as the RF input bias line was designed. The bottom plate of the capacitor (the Metal2 layer), will connect on both sides to ground. Figure 4.25 shows the layout of the LO input circuit.

Figure 4.25: Layout of LO circuit

The S parameters of the LO input circuit are shown in Figure 4.26. This figure

shows the circuit behaves as required.

Figure 4.26: S parameter plot of H_2 gate bias circuit

- S_{11} is 0dB at DC, indicating no DC current is getting through to port 1 (the LO input).
- S_{21} is close to 0dB at 39GHz, indicating the LO input is getting to the gate of H_2 with little attenuation.
- S_{31} at DC is very low, indicating no DC voltage is getting to port 1. At 39GHz, S_{31} is very low, indicating no signal is leaking through the DC bias circuit.
- S_{32} at DC is relatively high, though the value is somewhat low because of the stabilizing resistors, while at 39GHz S_{32} is very low, indicating no signal is leaking through the DC bias circuit.

The bias T introduces a connection in the circuit where there was none before. The LO input circuit was simulated again, as a 3-port device, to see if the T connection

has an effect on the matching. Simulation results showed the bias T had a big impact on the LO matching. The matching was redone to 50Ω .

Biasing the Gate of H_3

At the gate of H_3 is a capacitor to ground that serves as a RF short for high frequencies. This capacitor can be used much in the same way as the capacitors to ground are used for the other DC bias lines. A quarter-wavelength line will be connected to the top plate of the capacitor, terminated by another 5pF capacitor to ground. This 5pF capacitor represents only a 0.8Ω impedance to ground for a 39.25GHz signal.

The capacitor was redesigned so the bottom plate is connected to ground, and that a clear, `Metal1` path exists from the pad to the gate of the transistor. The line length was optimized to provide maximum gain at the output. The S parameter file of the layout simulation was added to the schematic simulation, and the whole circuit simulated again to ensure proper operation.

Biasing the Drain of H_2 and H_3

To bias the drain of H_2 and H_3 , a slightly different approach was used. At the drain of the switching transistors and after the capacitors to ground, only the 1GHz signal should appear. A quarter-wavelength transmission line at 1GHz is too long (almost 30mm). So inductors were used to isolate the DC inputs from the circuit.

To provide sufficient isolation from the circuit, the inductors must be at least 10nH. This is a very large inductor to be used on this process. The total length of a $10\mu\text{m}$ line, $5\mu\text{m}$ gap inductor is 5.52mm.

Now that the required inductance is known, a simulation of the inductor was completed. The calculation given by OMMIC says this inductor should resonate at approximately 6.5GHz; this is the point where the inductor is more capacitive than inductive. A S parameter plot of the inductor vs frequency is important in the design;

care must be taken that the resonance points (where the plot crosses the centre line of the Smith chart) do not occur at frequencies present in the circuit.

The inductor for biasing the drain of H_3 was connected to the top plate of the RF grounding capacitor. A small line length connects the top plate to the inductor, and in turn the inductor is connected to the pad.

For biasing the drain of H_2 , it is necessary to cross the output line of the drain of H_3 . A Metal1-to-Metal2 connection was used; the Metal2 layer being used to cross under the output line. This Metal2 connection then connects to the drain of H_2 . The output line and the Metal2 cross line are both $10\mu\text{m}$ wide. The capacitance between the crossing is therefore $22.8\text{k}\Omega$.

Biasing the Gate of H_4 and H_5 and the Drain of H_4 , H_5 and H_7

The biasing of transistors H_4 and H_5 is fairly simple. A 10nH inductor is used, connected to two 500Ω resistors to provide bias. Two Metal1-Metal2 crossings are necessary for connecting the bias to the two gates; at 1GHz , these represent a high impedance and should not impact the design.

To bias the drain of H_4 , H_5 and H_7 , a 10nH inductor is used again. The drain of these three transistors is connected to a 4.8V power supply.

A microphotograph of the complete circuit is shown in Figure 4.27 (the schematic was given in Figure 4.8). The circuit's dimensions are $2.4\text{mm} \times 1.8\text{mm}$.

Figure 4.27: Coplanar half Gilbert cell mixer

4.8 Experimental Results

The following pages show results characterizing the completed mixer. These plots include conversion gain as a function of various parameters (input RF power, LO power and frequency) and the return loss as a function of various parameters. Also characterized are the IF output parameters, including matching, return loss, impedance.

4.8.1 Experimental Setup

A schematic of the experimental setup used for the measurements is shown in Figure 4.28. The RF and LO power levels were measured at the probe, using an HP 437B

Figure 4.28: Experimental setup

Power Meter. The probing station is a Karl Suss PA200 Semi Automatic Probing Station.

The rest of the equipment used is as follows:

- RF and LO probes: RF is a Picoprobe² model 40A-GSG-150-P, with 0.65dB loss at 39.25GHz. LO probe is also a Picoprobe model 40A-GSG-150-P, with 0.7dB loss at 38.25GHz.

²<http://www.ggbindustries.com/>

- The IF probe is a Picoprobe model 40A-GSG-150-P, with 0.13dB loss at 1GHz.
- Cables are type K, with approximately 0.3dB loss at 1GHz, and 4.5dB loss at 39GHz.

4.8.2 Results

Figure 4.29 shows the variation of the gain as a function of the RF input level. The input LO level is +10dBm, at 38.25GHz. The RF frequency is 39.25GHz, for an IF output at 1GHz. The measured results agree quite well with the simulated results, validating the simulations.

Figure 4.29: Conversion gain vs RF input power

Figure 4.30 shows the gain as a function of the input LO power. This can be useful to determine the minimum power required to get good gain. As in all mixers, gain

increases as LO power increases, until at a certain point the gain no longer increases. From Figure 4.30, it can be seen that the gain is stable at around 10 dBm, and that there is very little increase in gain starting around 8 dBm. At 3dBm of input LO power, there is no gain in the mixer. This information can be useful if power consumption is more important than the gain of the mixer. A trade-off can occur, where gain is sacrificed for input power. The RF input power for these measurements is -20dBm at a frequency of 39.25GHz, with an LO frequency of 38.25GHz.

Figure 4.30: Conversion gain vs LO power

The linearity of this mixer is presented in Figure 4.31. The measured values are shown with the circled data, while the linear extrapolation of those points is also shown. The input intercept point is given as $IIP3 = 3.33\text{dBm}$. This is a bit lower than the simulated value of 7.3dBm. The RF input frequencies were 39.25GHz and

39.26GHz, giving output frequencies of 0.99GHz, 1.0GHz, 1.01GHz, and 1.02GHz. The LO input power was +10dBm.

Figure 4.31: 3rd order intermodulation point

Return loss is another important parameter of the circuit. It is undesirable for all the power that is applied into the circuit to come back out the same port. Figure 4.32 shows the return loss for the RF input. The RF return loss is better than -12dB for the bandwidth. The measured S parameters show some fluctuations; however the equipment used had been recently calibrated. A best fit is shown that eliminates the fluctuations on the measurements. The best fit is a 3rd-order polynomial.

To summarize the mixer's parameters, Table 4.11 is presented. These simulated results compare well with other research, as shown in Table 4.12. The mixer designed in this work compares well with other mixers using the same technology, demonstrating that coplanar waveguide is a good alternative to microstrip.

Figure 4.32: Measured return loss for the RF input

Table 4.11: Mixer parameters

RF	39.25GHz
IF	1GHz (fixed)
IIP3	3.33dBm
Conversion Gain	5dB
LO	10dBm
Return Loss (RF)	<-14dB
Return Loss (LO)	<-6dB

Table 4.12: Mixer results

Frequency	Gain	IIP3	Technology	Reference
2 GHz	10dB	+5dBm	GaAs	ref [35]
30 GHz	1 dB	+3dBm	GaInP/GaAs HBT	ref [89]
30 GHz	5.9dB	$P_{1dB} = -17\text{dBm}$	SiGe	ref [31]
10 GHz	-	+3dBm	GaAs	ref [87]
1 GHz	14.5dB	+2.4dBm	CMOS	ref [90]
8 GHz	4 - 15dB	-	GaAs	ref [38]
44 GHz	-6dB	-	GaAs	ref [34]
39 GHz	-5dB	-	GaAs	ref [91]
4-40GHz	2.5dB (at 40GHz)	-	GaAs	ref [92]
39.25 GHz	5dB	3.33 dBm	GaAs	this work

4.9 Summary

The focus of this chapter was to design a coplanar half Gilbert cell mixer [93]. The designed mixer has good gain and linearity, and compares well with other published mixers.

The designed mixer was based on a half-Gilbert cell configuration, a three-transistor circuit. The circuit had two inputs, an RF and an LO input, with one of the transistor's gate grounded. A transmission line was used to provide matching between the two stages of the mixer, resulting in a 2dB improvement in conversion gain.

The centre core of the circuit, with three transistors, has many parameters that can affect conversion gain. The matching transmission line used in the circuit also affects gain, and is yet another parameter to be optimized in the design. To improve on the performance of the centre cell, another circuit was designed and the centre cell optimized. That is the focus of the following chapter.

Chapter 5

Optimizing the Centre Cell

When designing a differential mixer, many parameters are present. These parameters must be optimized according to specific goals: conversion gain, linearity, or noise. In chapter 4, during the design of the mixer core, many simulations were done to find the optimum values of transistor size (number of fingers and length), matching transmission line, source stabilizing line, and input stabilizing resistor. Many simulations were done in order to find the optimum values. The objective of this chapter is to optimize and automate the calculation of these parameters using particle swarm optimization (Appendix A).

Using the FET model, particle swarm optimization will be used to match the input impedance of the top two switching transistors of the half Gilbert cell to the output impedance (the drain) of the bottom amplifying transistor (as in Figure 4.1).

5.1 PHEMT Model

A first step in optimizing the centre cell is to correctly model the FETs used in the cell (pHEMTs in the current process). Although this modeling will result in a small-signal model, this is sufficiently precise to serve as a starting point in the design.

The objective of this section is to compare the OMMIC pHEMT model and its

extracted S parameters to the simulation results. The pHEMT will be modeled using a standard high-frequency FET model, and foundry data will be used to complete the model.

5.1.1 Impedance Seen Looking into the Drain

To get an equation of the output impedance of the pHEMT, the first step is to determine which parameters from the model are present. The model given by the foundry for the small-signal equivalent circuit is given in Figure 5.1. This model is similar to standard FET models [94], [14], [95]. Although many models ignore some of the parasitics presented in Figure 5.1, they are included here for completeness.

Figure 5.1: Small-signal model of the OMMIC pHEMT

In order to use this model to optimize the impedance between the bottom FET of the centre cell and the top two FETs, an equation is needed giving the impedance seen looking into the drain (for the bottom FET) and the source (for the top two FETs). From the circuit given in Figure 5.1, certain parasitics can be grouped together to

simplify the analysis. The following impedances are defined:

$$Z_s = R_s + L_s || C_s \quad (5.1)$$

$$Z_g = (Z_{in} + L_g) || C_g + R_g \quad (5.2)$$

$$Z_{gs} = C_{gs} + R_{gs} \quad (5.3)$$

$$Z_{gd} = (C_{gd} + R_{gd}) || (1/G_{gd}) \quad (5.4)$$

$$Z_{ds} = R_{ds} || C_{ds} \quad (5.5)$$

where it is of course understood that the capacitances and inductances in the above equations represent their actual impedance. All the parasitics given in Figure 5.1 depend on the size of the pHEMT (number of fingers and finger width). With these simplifications done, standard circuit analysis (using a mesh current technique) is used to get a matrix for the impedances (matrix **A**):

$$\mathbf{A} = \begin{bmatrix} Z_{cd} + Z_{ld} & -Z_{cd} & 0 & 0 \\ -Z_{cd} & Z_s + Z_{ds} + R_d + Z_{cd} & -Z_{ds} - g_m Z_{gs} Z_{ds} & -Z_s + g_m Z_{gs} Z_{ds} \\ 0 & -Z_{ds} & Z_{gs} + Z_{gd} + Z_{ds} + g_m Z_{gs} Z_{ds} & -g_m Z_{gs} Z_{ds} - Z_{gs} \\ 0 & -Z_s & -Z_{gs} & Z_g + Z_{gs} + Z_s \end{bmatrix} \quad (5.6)$$

where Z_{cd} represents the impedance of C_d and Z_{ld} is the impedance of L_d .

The voltage matrix $\mathbf{B}$ is given by:

$$\mathbf{B} = \begin{bmatrix} V_x \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (5.7)$$

where V_x is a test voltage applied to the drain (terminal under study).

The impedance seen looking into the drain is then given by:

$$Z_x = \frac{V_x}{I_x} \quad (5.8)$$

where I_x is the first current obtained from solving the system:

$$\mathbf{C} = \mathbf{A}^{-1} \cdot \mathbf{B} \quad (5.9)$$

The output impedance calculated by the above model was compared to the values given by a HPADS simulation (small-signal S parameter linear test bench). A 6-finger FET is simulated, with the finger length varied from $10\mu\text{m}$ to $60\mu\text{m}$. The results are given in Figure 5.2.

There is a small difference between the calculated output impedance and the simulated S parameters. The calculated values show good agreement with the pHEMT simulation.

The impedance can be obtained from the S parameters by using the following equation¹:

$$\Gamma_o = S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_s} \quad (5.10)$$

In HPADS, for the S parameter measurements, the input impedance $Z_{in} = 50\Omega$, and so $\Gamma_s = 0$. Hence $\Gamma_o = S_{22}$, and the reflection coefficient can be transformed into an

¹K.Chang, Microwave Solid-State Circuits, p.335

Figure 5.2: Smith chart showing the calculated output impedance and simulated S parameters

impedance, using the well known relation [79]:

$$Z_x = Z_0 \frac{1 + \Gamma_o}{1 - \Gamma_o} \quad (5.11)$$

where Z_0 is the reference impedance, 50Ω .

5.1.2 Impedance Seen Looking into the Source

For the top two pHEMTs of the differential mixer, the impedance used for matching is the source impedance. Although these pHEMTs operate in large-signal, the small-signal equivalent circuit (Figure 5.1) is used for simplification.

In this case, the simplified impedances Z_g , Z_{gs} , Z_{gd} and Z_{ds} given by equations

5.2, 5.3, 5.4 and 5.5 will remain the same. A new impedance Z_d will be added:

$$Z_d = (Z_{dd} + L_d) || C_d + R_d \quad (5.12)$$

where Z_{dd} is the impedance connected to terminal D . The impedance Z_s (Eq. 5.1) will not be used here, and using the same analysis technique,

$$\mathbf{A} = \begin{bmatrix} Z_{cs} + Z_{ls} & -Z_{cs} & 0 & 0 \\ -Z_{cs} & Z_g + Z_{gs} + R_s + Z_{cs} & -Z_{gs} & -Z_g \\ 0 & -Z_{gs} - g_m Z_{gd} Z_{gs} & Z_{gd} + Z_{gs} + Z_{ds} + g_m Z_{gd} Z_{gs} & -Z_{gd} \\ 0 & -Z_g & -Z_{gd} & Z_d + Z_{gd} + Z_g \end{bmatrix} \quad (5.13)$$

The voltage matrix $\mathbf{B}$ is the same as for the calculation of the drain impedance (Eq. 5.7). The impedance is given in the same manner by Eq 5.8.

Again, for clarification purposes, the inductances and capacitances used in equations 5.2 - 5.5 and Equation 5.12 represent the actual impedances. The impedance Z_{cs} represents the impedance of C_s and Z_{ls} is the impedance of L_s .

As was the case for the drain impedance, a 6-finger FET is simulated, with the finger lengths varied from $10\mu\text{m}$ to $60\mu\text{m}$. Figure 5.3 shows the calculated and simulated values of the source impedance. There is very little difference between both results.

5.2 Problem Definition

Now that the output impedance of the lower pHEMT and the input impedance of the top pHEMTs are known, the problem becomes one of optimization. Figure 5.4

Figure 5.3: Smith chart showing the calculated output impedance at the source of pHEMT2

illustrates the problem.

The output impedance of the pHEMTs is a function of their width and number of fingers (as well as the bias values, but these are not considered here). So $Z_1 = f(W_1, N_1)$, and $Z_{2,3} = f(W_2, N_2)$, because the top two pHEMTs will be of the same dimensions. The reflection coefficient of the matching line is a function of its characteristic impedance and its length.

The optimization will be done at point 1 (though point 2 could be chosen to achieve the same results). From standard transmission line theory [79],

$$Z_{11} = Z_0 \frac{Z_2 + j Z_0 \tan(\beta l)}{Z_0 + j Z_2 \tan(\beta l)} \quad (5.14)$$

Figure 5.4: Diagram of optimization problem

where

$$\beta = \frac{2\pi}{\lambda_g} \quad (5.15)$$

$$l = \frac{\theta}{2\pi} \cdot \lambda_g \quad (5.16)$$

Maximum power transfer is achieved if $\Gamma_{l1} = \Gamma_1^*$ [79], or

$$Z_{l1} = Z_1^* \quad (5.17)$$

This is a first approximation of the problem. The pHEMTs must be biased, and so far the biasing circuitry has been neglected. For H_1 , a drain bias must be applied. A bias T will therefore be placed between H_1 and the matching line. The circuit will resemble that of Figure 5.5.

The bias T was simulated as a 2-port circuit, assuming the impedance of the third branch, connected to the biasing circuit, would present a very high impedance at the frequency of interest. This is a reasonable assumption in this case, since a first-order approximation is all that is needed. The bias T is represented in Figure 5.6.

Once this 2-port circuit was simulated, the S parameters were extracted, and then converted to an ABCD matrix. The FET impedance was calculated and then converted to an ABCD matrix as well. Since these two components are in cascade, it

Figure 5.5: Diagram of revised optimization problem

Figure 5.6: Bias "T" circuit

is easy to multiply the two ABCD matrices to obtain a single matrix.

$$[\mathbf{ABCD}]_1 = [\mathbf{ABCD}]_{H_1} \cdot [\mathbf{ABCD}]_T \quad (5.18)$$

This ABCD matrix is then converted to a Z impedance [79], which is used to calculate the optimum matching.

Other additions to the FET model are a transmission line and a shunt resistor used to stabilise H_1 . A stability analysis for H_1 gives a range of values for the transmission lines and the shunt resistor. The shunt resistor is placed at the input (gate) of H_1 , while the transmission line is placed at the source. The input resistance Z_{in} of Figure 5.1 will be modified as follows:

$$Z_{in} = Z_{ref} || R_{stab} \quad (5.19)$$

where Z_{ref} is the reference impedance (50Ω) and R_{stab} is the stabilizing resistor.

At the source, instead of inductance L_s being grounded, it is now in series with a grounded transmission line, whose impedance is given by [79]:

$$Z_{stab} = jZ_{0stab} \tan(\theta_{stab}) \quad (5.20)$$

where Z_{0stab} is the impedance of the stabilizing transmission line, and θ_{stab} is the electrical length of the line.

Optimization was done using a particle swarm algorithm (see Appendix A). In this case, there are nine variables to optimize: W_1 , N_1 , Z_0 , θ , W_2 , N_2 , R_{stab} , Z_{0stab} and θ_{stab} . The algorithm is designed to minimize a certain function, usually the difference between two sets of data. In this case, the error function or *objective function* for this problem is such that $Z_{l1} - Z_1^* = 0$, or

$$f_{obj} = \Re\{Z_{l1} - Z_1^*\}^2 + \Im\{Z_{l1} - Z_1^*\}^2 \quad (5.21)$$

5.3 Particle Swarm Results

Although the model does not correspond exactly to the calculated values, the results calculated by the particle swarm will be a good starting point for the design of the mixer. Electromagnetic simulations must still be done, especially on the length of line since the effective permittivity (ϵ_{eff}) used is just an approximation. Also, no loss was considered in the line, and the pHEMT models will not correspond exactly to measured data. Nonetheless, the steps presented here can give a designer a good reference point from which to start his design.

The upper and lower limits used to perform the calculations are given in Table 5.1.

The parameters are chosen according to the limitations of the design process. The individual finger widths are limited to $60\mu\text{m}$, and the maximum number of fingers

Table 5.1: Upper and lower limits for the optimization parameters

Parameter	Lower Limit	Upper Limit
W_1	$10\mu\text{m}$	$60\mu\text{m}$
N_1	2	8
Z_0	30Ω	90Ω
θ	10°	70°
W_2	$10\mu\text{m}$	$60\mu\text{m}$
N_2	2	8
R_s	500Ω	1500Ω
Z_{0stab}	30Ω	110Ω
θ_{stab}	10°	70°

is 8. A design could be made to have more fingers, but the scaling model is only accurate up to 8 fingers. The impedances chosen for the matching line are values that can be readily created on-chip without taking up too much space.

5.3.1 Calculated Results

Using the particle swarm algorithm, the following parameters were calculated as the optimum (see Table 5.2). These values are compared here to the values obtained by simulation with ADS. The values calculated by the particle swarm algorithm are very close to the optimum values obtained by ADS simulation.

The particle swarm algorithm arrived at these values consistently, with an error function of 0 (or $f_{obj} = 0$). The error was of the order of magnitude of the precision of the **double** variable type in Matlab ®.

5.3.2 Design of the Centre Cell

Once the parameters for the centre cell have been chosen, the next step is designing the matching circuits and doing the layout of the circuit. First, however, the bias

Table 5.2: Optimized parameters for the differential mixer

Parameter	Particle Swarm	ADS Simulated Value
W_1	$42\mu\text{m}$	$38\mu\text{m}$
N_1	2	2
Z_0	80Ω	75Ω
θ	40°	41°
W_2	$50\mu\text{m}$	$50\mu\text{m}$
N_2	6	6
R_s	1200Ω	1200Ω
Z_{0stab}	40Ω	40Ω
θ_{stab}	10°	10°

circuits for the mixer core must be designed, before any matching is done. Designing the layout and matching circuits follows an 'inside-out' approach: the layout of the circuit between the top and bottom transistors is done first, and then steadily moving 'outwards', finishing with the matching circuits.

5.4 Centre Cell Bias Circuit

The centre cell must be biased using the bias T presented in Figure 5.6. The bias circuit must present a high impedance at the RF frequency, in order to minimize the signal loss in the bias path. A quarter-wave transmission line at 39.25GHz was used, followed by a 5pF capacitor, to provide a low impedance point.

The layout (not to scale) of the centre cell bias circuit is shown in Figure 5.7. Port 1 will be connected to transistor H_1 of the centre cell, while port 2 will be connected to the sources of transistors H_2 and H_3 . Port 3 is the DC input, connected to the top plate of the 5pF capacitor. The capacitor is connected to ground by its bottom plate.

Figure 5.7 is a general representation of the bias circuit. Some air bridges are missing, used to provide proper grounding all along the quarter-wavelength transmission line.

Figure 5.7: Layout of centre cell bias circuit

The simulated S_{11} , S_{21} and S_{31} parameters are shown in Figure 5.8.

As can be seen in Figure 5.8, the circuit has the required behaviour. At 39.25GHz, the S_{31} parameter has a very low amplitude (-37.6dB). S_{21} has a value close to 0dB (-0.6dB), indicating that almost all of the signal is getting through.

5.5 RF Input Stabilizing Transmission Line

The RF input transistor, H_1 , is stabilized by using a 40Ω , 10° transmission line (see Table 5.2). To achieve such a transmission line, a $50\mu\text{m}$ wide line was used with a $14\mu\text{m}$ gap. These dimensions correspond to a 40.42Ω transmission line. The layout

Figure 5.8: Simulated S parameters of centre cell bias circuit

of this transmission line is given in Figure 5.9.

Figure 5.9: Layout of the RF input stabilizing transmission line

The end of the transmission line extends a bit further than its ground plane; this is so a proper connection can be made to the FET.

5.6 RF Input

The next section to design is the RF input circuit. This consists of the RF stabilizing resistor and a DC blocking capacitor. The value of the RF stabilizing resistor was calculated in Table 5.2. The gate bias will be supplied to the RF input transistor through the resistor. A shunt capacitor to ground will be used to provide a ground for all high frequencies, ensuring that the RF input sees only a resistor connected to ground.

A schematic of the RF input is shown in Figure 5.10.

Figure 5.10: Schematic of RF input circuit

The stabilizing resistor R_{stab} will be designed as a GaAs resistor, since the required value is high. A $20\mu\text{m}$ width was chosen for the resistor, for a length of $120\mu\text{m}$, using foundry data. For this configuration, the maximum voltage drop across the resistor is 9V, or 7mA, to maintain a linear resistance. Since the RF input is connected to the gate of transistor H_1 , the current through the resistor will be negligible. The gate of transistor H_1 is biased at -0.3V, so no tolerance will be exceeded.

The input transmission line to the FET gate is $50\mu\text{m}$, so a width of $70\mu\text{m}$ was chosen to minimize the transversal width of the input. A 3pF DC blocking capacitor was used, for a $100\mu\text{m}$ -long capacitor, using foundry data.

The layout of the RF input circuit is shown in Figure 5.11, while the simulated S parameters for the circuit are shown in Figure 5.12.

The circuit performs correctly:

- S_{11} at DC is 0, meaning everything is reflected at low frequencies.

Figure 5.11: RF input circuit layout

Figure 5.12: Simulated S parameters of RF input circuit

- S_{21} at DC is very low, meaning no signal gets through, while at high frequencies it is close to 0dB, indicating all signal is getting to FET H_1 .
- S_{32} at low frequencies is relatively high, since the 1200Ω resistor will translate into some loss, while at high frequencies, it is very low, indicating no signal is bleeding through the DC input.

5.7 RF Matching Circuit

Once the RF input circuit has been designed, a matching circuit must be used. At 39.25 GHz, the RF input has an impedance of $Z_{RF} = 12.5 + j7.0\Omega$. For this impedance, a series L, shunt C matching circuit is used. The ideal values that provide matching to 50Ω are 0.059nH and 140.5fF, respectively. From Equations 2.13 and 2.15, using the standard parameters for the inductive and capacitive stubs (given in Table 5.3) this gives stub lengths of $100\mu\text{m}$ for the series stub and $379\mu\text{m}$ for each of the shunt stubs.

Table 5.3: Parameters for the series and shunt stubs

	Width (μm)	Gap (μm)	Impedance (Ω)	ϵ_{eff}	λ (μm)
Series Stub	10	20	71.776	5.941	3136
Shunt Stub	10	5	51.235	5.412	3285

The series stub is short, however the dual shunt stubs are fairly long. To reduce the length of the shunt stubs (and therefore reduce the area occupied by the matching circuit), four shunt stubs were used instead of two. The circuit used is given in Figure 5.13.

The transmission line between the two shunt capacitors represents the physical separation needed between shunt stubs on each side of the centre conductor. A good rule of thumb is twice the ground to ground separation [77]. In this case, the shunt

Figure 5.13: Matching circuit for RF input

stubs have a ground to ground separation of $20\mu\text{m}$. The separation between the shunt stubs was chosen to be $45\mu\text{m}$.

With $45\mu\text{m}$ of separation, the transmission line has an electrical length of 5.44° at 39.25 GHz , given the 50Ω line of the centre conductor. With the model of Figure 5.13, the inductance and capacitance required to achieve a 50Ω match are 0.0495nH and 35.8fF for each of the quad shunt stubs. These values represent an $84\mu\text{m}$ series stub and four $222\mu\text{m}$ shunt stubs. The circuit layout is shown in Figure 5.14.

The series stub has a minimum length, since there are four shunt stubs attached to it. The minimum length needed for the series stub is $45\mu\text{m}$ (the shunt stub separation) plus twice the ground separation of $10\mu\text{m}$, so $65\mu\text{m}$.

The final values for the stub are four $220\mu\text{m}$ shunt stubs, with a $58\Omega\text{m}$, $71\mu\text{m}$ series stub. The values are slightly different from those calculated.

The simulated S_{11} and S_{21} parameters are shown in Figure 5.15.

5.8 LO Input Circuit

The LO input circuit is where the drive signal for the top two FETs in the differential mixer arrives. The circuit must have a DC feed line where the gate voltage can be applied to the FET. Also, a DC blocking capacitor is needed to prevent the DC voltage from leaking out through the input. The layout of the LO input circuit is shown in Figure 5.16.

Figure 5.14: Layout of RF input matching circuit

Figure 5.15: Simulated S parameters for the RF matching circuit

Figure 5.16: Layout of LO input circuit

The DC feed line is a quarter-wave transmission line connected to a 5pF capacitor, to provide a low impedance. At 38.25GHz (the LO input frequency), the 5pF capacitor represents a 0.8Ω impedance. With the quarter-wave transmission line, the impedance seen at the connection to the central conductor is very high, preventing the LO signal from leaking through the DC line.

The simulated S parameters of the LO input circuit are shown in Figure 5.17.

Figure 5.17: Simulated S parameters of LO bias circuit

The circuit performs as needed:

- S_{11} at DC is 0dB, meaning every thing is reflected at low frequencies.
- S_{21} at DC is very low, meaning no signal gets through, while at high frequencies it is close to 0dB, indicating all signal is getting to FET H_2 . At 38.25GHz, $S_{21} = -0.7\text{dB}$.

- S_{32} at low frequencies is close to 0dB, indicating the DC is getting from port 3 to port 2, while at high frequencies, it is very low, indicating no signal is bleeding through the DC input. At 38.25GHz, $S_{32} = -36.9\text{dB}$.

5.9 LO Matching Circuit

With the LO bias circuit completed, the LO input must be matched to 50Ω . The impedance seen looking into the LO bias circuit is $6.1 + j8.0$. For this impedance, a series L, shunt C matching circuit is used. The ideal values that provide matching to 50Ω are 0.019nH and 217.6fF , respectively. From Equations 2.13 and 2.15, using the standard parameters for the inductive and capacitive stubs (given in Table 5.3) this gives stub lengths of $39\mu\text{m}$ for the series stub and $476\mu\text{m}$ for each of the shunt stubs.

The series stub is very short and the dual shunt stubs are very long. Rather than using stubs, MIM capacitors will be used instead of shunt stubs. Using foundry-supplied data, the size of the shunt capacitors is estimated to be $40 \times 50\mu\text{m}^2$. The final values obtained after simulation are a $18\mu\text{m}$ long series stub, with two $39 \times 31\mu\text{m}^2$ shunt capacitors.

The simulated S parameters of the LO matching circuit are shown in Figure 5.18.

5.10 Completed Circuit

A schematic of the completed circuit is shown in figure 5.19. The two IF outputs will be matched off chip using a jig circuit.

A microphotograph of the mixer is shown in Figure 5.20. The mixer has a height of 1.614mm , and a width of 1.875mm .

Figure 5.18: Simulated S parameters of the LO matching circuit

Figure 5.19: Circuit schematic of centre cell

Figure 5.20: Coplanar half Gilbert cell mixer: design 2

5.11 Jig Circuit

The jig circuit will be used to apply the DC bias to the MMIC via $\lambda/4$ transmission lines at 1GHz. It will also be used to provide matching for the IF outputs.

The DC bias for the drain of transistors H_2 and H_3 must be designed using $\lambda/4$ lines at 1GHz terminated by a large capacitor to provide adequate grounding at 1GHz. The $\lambda/4$ line at 1GHz would be too long to include on the MMIC: it would be approximately 3mm in total length. A jig circuit is therefore needed to design such a line.

The matching circuits for the IF outputs were also designed on the jig. The line lengths necessary for matching would be too long to include on the MMIC. The IF output impedances are shown in Figure 5.21. The top output has an impedance of $195.5 - j127.2$, while the bottom output has an impedance of $11.0 - j438.0$. The bottom output is at the far edge of the Smith chart and will be very difficult to match.

The matching circuits for the IF outputs were done using single-stub matching. The jig circuit is a 10mil Alumina substrate with gold conductors. The matching circuit for each output is shown in Figure 5.22. Figure 5.22a shows the matching circuit for the top output, while Figure 5.22b shows the matching circuit for the bottom output.

Because the line lengths are long, the matching circuits of Figure 5.22 will not provide good bandwidth, especially the bottom output, whose length is 80.45° .

The completed jig layout is shown in Figure 5.23. The MMIC will be placed in the centre left, with the DC bias lines going down. The two IF outputs are at the right of the image.

Figure 5.21: IF output impedance

Figure 5.22: IF output matching circuits

Figure 5.23: Jig layout

5.12 Results

Some modification were made to the simulations of the circuit because the jig circuit is slightly different than the design. The MMIC chip has a higher substrate than the jig circuit. The MMIC chip has a $625\mu\text{m}$ high GaAs substrate, while the jig circuit is a 10 mil ($254\mu\text{m}$) substrate. The MMIC is bonded on top of the Alumina substrate.

The bond wire inductance is estimated from its length: the IF output pads are approximately $500\mu\text{m}$ distant from the output pads of the MMIC. There is a height difference of approximately $650\mu\text{m}$ between the MMIC and the jig circuit. Accounting for the loop, the total length of the bond wire is estimated to be 0.8mm . Using an estimate of 1nH/mm [96], the inductance of the bond wire is 0.8nH .

For a standard 1mil width bond wire, the resistance is approximately $125\text{m}\Omega/\text{mm}$ [96] of length. This means each bond wire has approximately $100\text{m}\Omega$ of resistance.

The jig circuit connections were simulated to include the loss and line length. These S parameter simulations were included into the overall circuit simulation.

The jig circuit was improperly fabricated. The conductor layer (Au) was fabricated with the wrong thickness, $0.5\mu\text{m}$ instead of the typical $4\mu\text{m}$ for a gold conductor. This has a significant impact on the circuit's performance, as the loss of the jig circuit, for lines close to 30mm long, is significant. Also, open circuit stubs were fabricated instead of short circuit stubs. The jig circuits were simulated again using the fabricated thickness and stubs. The results shown in the following section take into account this error in fabrication. Also shown in a few graphs are the simulation results with correctly fabricated jig circuit.

5.12.1 Experimental Setup

The experimental setup used in the measurement of the mixer's performance is shown in Figure 5.24. The RF and LO power levels were measured at the probe, using an

Figure 5.24: Experimental setup

HP 437B Power Meter. The probing station is a Karl Suss PA200 Semi Automatic Probing Station. The rest of the equipment used is as follows:

- RF and LO probes: RF is a Picoprobe² model 40A-GSG-150-P, with 0.65dB loss at 39.25GHz. LO probe is also a Picoprobe model 40A-GSG-150-P, with 0.7dB loss at 38.25GHz.
- The IF dual probe is a Picoprobe model 40A-GSG-150/40A-GSG-150-D-800, with 0.13dB loss at 1GHz.
- Cables are type K, with approximately 0.3dB loss at 1GHz, and 4.5dB loss at 39GHz.

5.12.2 Measured Results

The conversion gain as a function of the RF input power is given in Figure 5.25. The measured gain of the mixer is close to the simulated gain. The gain is relatively stable until around -10dBm of input power. The input LO power was +10dBm at the

²<http://www.ggbindustries.com/>

probe, at a frequency of 38.25GHz. The RF input is at 39.25GHz. With the properly fabricated jig, the conversion gain would have been approximately 2.5dB better.

Figure 5.25: Conversion gain vs RF input power

The conversion gain as a function of the RF input frequency is given in Figure 5.26. There is a large difference between the measured and simulated gain at 39.05GHz. The simulated gain at that frequency appears to have a sort of resonance effect that is not present in the measured conversion gain. Overall, the trend of the measured gain is close to the gain obtained by simulation. As was the case for the previous graph, the results at 39.25GHz with the correct jig circuit would have been 2.5dB better.

The IP3 of the top output is given in Figure 5.27. The measured data are marked with circles, while the linear extrapolation of that data is shown in dashed lines. The third order intercept point is 10.6dBm.

The measured return loss for the RF and LO inputs are given in Figure 5.28. The

Figure 5.26: Conversion gain vs RF input frequency

Figure 5.27: 3rd order intercept point

measured RF return loss at 39.25GHz is slightly less than -20dB, which is close to the simulated value of -24dB. The measured LO return loss is approximately -11dB, close to the simulated value of -12dB.

Figure 5.28: RF and LO return loss, measured

The measured return loss for the top output is shown in Figure 5.29. This is better than the simulated return loss. For the top output, the return loss at 1GHz is -14dB.

5.13 Summary

To improve the performance of the half-Gilbert cell mixer core, a particle swarm algorithm was used to optimize the parameters of the centre cell. Particle swarm optimization is a relatively new technique belonging to the class of nature-based optimization algorithms. Nine variables were optimized to achieve the best matching between the bottom transistor and the top two switching transistors of the mixer

Figure 5.29: IF return loss, measured

core. The mixer was built on a GaAs substrate, by OMMIC, in France.

The matching circuit for the IF outputs was designed on an 10mil Alumina substrate. The MMIC was then epoxied on this substrate, and bond wires were used to connect the MMIC to the matching circuit.

This circuit did not perform as well as the previous design, since the fabrication error degraded the overall performance. However, the use of the particle swarm algorithm significantly simplified the initial design of the mixer core. The conversion gain of the mixer would have been approximately 2.5dB better with a properly fabricated jig.

Chapter 6

Conclusion

6.1 Summary

Coplanar technology is an interesting alternative to microstrip when designing high frequency circuits. Coplanar technology gives a designer more options when designing transmission lines, because coplanar technology allows for a variable gap to the ground plane, something that microstrip cannot do, since the ground plane's height is fixed. Coplanar technology was investigated as a means to reduce the size of matching circuits. A 39.25GHz mixer was designed using coplanar technology.

A summary of research in the area of microwave mixers was presented first. Most microwave mixers are diode-based, that all show conversion loss. A review of FET-based mixers was then presented, whereas most FET mixers are in microstrip technology. Very few FET-based mixers have been done in coplanar technology. Therefore, a microwave mixer based on the well known Gilbert cell presents an interesting challenge. A review of coplanar technology, with equations to be used in the design of stubs was then presented.

Coplanar technology as a means of reducing the size of matching circuits was first investigated. Coplanar technology allows a design to include shunt elements directly in the centre conductor of the main transmission line. By using these folded elements

in matching circuits, the overall size of the circuit can be reduced. Novel structures were designed and fabricated, and their performance evaluated. These structures performed very well as matching circuits. The difference between the standard configuration and the folded configuration was also investigated. The reduced ground plane of the folded structure increased the impedance of the shunt element, while the fringe capacitance of the ground plane connections also had an impact on circuit performance [82]. The two novel folded structures achieved area reductions of 16% and 9%, while providing close to 20dB return loss.

A coplanar microwave mixer was designed, based on the Gilbert cell. The mixer used some of the advantages of coplanar waveguide, such as the ability to easily design lines of different impedance. An active balun was used at the output. A transmission line was used between the RF input transistor and the LO input transistors, in order to improve the gain of the circuit. Simulations with various widths and impedance were done. This transmission line can have a significant impact on the gain; and coplanar technology gives a designer the opportunity to design lines of various impedances and lengths. An improvement of close to 2dB in conversion gain was achieved. The mixer achieved good results, with a conversion gain of 5dB [93].

To improve on the performance of the centre cell, particle swarm optimization was applied to the centre cell to achieve a minimum reflection coefficient between the RF input transistor and the LO input transistors. The optimization used 9 parameters (number of fingers and width of transistors, line impedance and electrical length) to achieve optimum conditions. The results of the particle swarm algorithm gave results very close to the optimum provided by large-signal S parameter simulations of the centre cell. This technique can therefore be used as a very good starting point in the design of a coplanar mixer.

A second mixer was fabricated using the results of the particle swarm algorithm. In this case, the IF outputs were not combined on chip, and a jig circuit was used to

provide matching. This circuit did not perform as well overall as the previous one, because fabrication error and parasitic elements in the jig resulted in conversion loss rather than conversion gain.

Overall, coplanar technology is a good alternative in the design of active microwave mixers. The ease of design of transmission lines with various widths and lengths gives a design more options. Also, the ability to fold shunt stubs directly into the centre conductor leads to matching circuits with reduced cross-section while keeping the same matching.

6.2 Contributions

The main contribution of this work was the design of an active microwave mixer in coplanar technology based on the Gilbert cell [93]. The advantages of coplanar technology in designing microwave circuits were also explored, in particular the ability to fold shunt elements directly into the centre conductor, to reduce the cross-section of matching circuits [82].

Other design techniques were also applied in the design of a coplanar microwave mixer. In particular, the use of a matching transmission line between the two stages of the mixer can significantly increase the gain of the mixer. Particle swarm optimization was used to optimize the parameters of the centre cell to improve the conversion gain.

6.3 Future Work

There are many possible avenues to explore in using coplanar technology to design active microwave mixers. In particular, the ability to fold stubs directly into the centre conductor means that instead of using a simple transmission line between the two stages of an active Gilbert cell-based mixer, a compact, complete matching circuit

can be used.

The folded stubs used in this work can also be further explored. In this work, a first-order approximation of the difference between the standard and folded configurations has been done. A better understanding of these differences and the development of design guidelines would increase their use in coplanar circuits.

Also, the use of particle swarm optimization as a design tool could be further explored. Neural network based design has been done before, as well as the use of genetic algorithms, but particle swarm optimization has yet to be used as a design tool for designing a mixer, to the author's knowledge. Particle swarm optimization is a simpler algorithm than genetic algorithms, and may yield faster results.

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Appendix A

Particle Swarm Optimization

Particle swarm optimization is a relatively new technique for solving optimization problems. The first particle swarm optimization algorithm was proposed by Kennedy and Eberhart [97]. It is another evolution-based algorithm, based on the behaviour of animal swarms (bees, birds, fish, etc.). The algorithm is very simple, more so than the typical genetic algorithm (to which it is often compared).

For a problem in which the solution is unknown, a set of possible solutions is created randomly (within specified bounds). This set of possible solutions is called the population. Each possible solution is called a particle, in terms of the algorithm, and has a behaviour similar to that of a swarm animal. The performance of each particle is evaluated, with the optimum solution being retained. Each particle will then gravitate towards the optimum particle in the n -dimensional space. At each time increment, the performance of all particles is evaluated. If a new optimum is found, the swarm will gravitate towards the new optimum. In this manner, after a fixed number of iterations, the optimum solution will be found.

The basic particle swarm optimization algorithm has the following structure:

Create an initial population

Repeat

Evaluate performance

Find best global performance

Update position of particles

Verify if end condition is met

A.1 The Particle Swarm Algorithm

The basic algorithm can be explained by the following analogy.

When bees venture out of the bees' nest to find honey, they scatter all around their territory, looking for pollen. They will fly all around, until they find a good source of pollen. If a bee finds a good source, it will communicate this to the other bees who will then fly towards the source. If a bee finds a better source of pollen, the swarm will then change direction to go to this new, better source.

From this analogy, there are two factors affecting the behaviour of a particle:

1. Individual factor (the particle).
2. Social factor (other particles).

Each particle has a position and a velocity: the particle is moving in an n -dimensional space (for a problem with n variables). The future position of the particle is a function of four parameters:

1. The current position
2. The current velocity
3. The best position obtained by the particle

4. The best position obtained by all particles

With these principles, the algorithm can now be properly explained. Certain constraints must be kept in mind, however. As in all optimization problems, the problem must be properly defined. The objective function, that is, the function that evaluates the performance of a particle, must be clearly defined. The search space must be well delimited: it is very important to know the boundaries of all variables.

A.1.1 Initial Population

The initial population is created randomly within the search space. The values are randomly selected with a uniform distribution over all the search space.

Let M be the total size of the population (the total number of particles), and n the number of variables. Each variable is denoted $a_1, a_2, \dots, a_n$. The initial population would be:

$$Pop = \begin{cases} x_1 = (a_{1,1}, a_{2,1}, \dots, a_{n,1}) \\ x_2 = (a_{1,2}, a_{2,2}, \dots, a_{n,2}) \\ \vdots \\ x_M = (a_{1,M}, a_{2,M}, \dots, a_{n,M}) \end{cases} \quad (A.1)$$

where x_i is the position of particle i in the n -dimensional space. Each particle is composed of a value for each variable. Note that each parameter of a particle has its own value, ie,

$$a_{i,1} \neq a_{i,2} \neq \dots \neq a_{i,M} \text{ where } i = 1, 2, \dots, n \quad (A.2)$$

Each particle has an additional parameter: velocity. Let v_i denote the velocity of particle i . In a manner similar to the creation of the initial population, each particle is assigned a velocity v_i randomly within boundaries of v_{max} and v_{min} .

Once the initial population is created, the next step will be to evaluate (update) the particle's performance.

A.1.2 Performance

The performance of each individual is evaluated with a single function, called the objective function. The performance is a measure of the exactness of the solution obtained by the particle. This objective function varies from one problem to another. It is calculated from the parameters (variables) of each particle. One value of the objective function is obtained for each particle, so there are M total values.

If the problem defines a function to minimize (as is often the case), the objective function takes the form of an error function, such as:

$$f_{obj} = (\Delta_m - \Delta_c)^2 \quad (\text{A.3})$$

where Δ_m is the measured value and Δ_c is the calculated value, obtained from the parameters of the particle. This value of the objective function becomes the performance (sometimes called fitness in genetic algorithms) of the particle.

A.1.3 Evaluating the Particles

There are two steps in the evaluation of the particles:

1. Compare the current performance of particle i with its best performance
2. Find the best performance of the swarm

The performance of each particle is compared to its best performance obtained. Let p_i be the particle's position giving the best-ever obtained performance, and x_i the current position.

$$\text{IF } f(x_i) > f(p_i) \rightarrow p_i = x_i \quad i = 1, 2, \dots, M \quad (\text{A.4})$$

which simply states: if the current position gives a better performance than the best-obtained position, then new best-obtained position equals the current position.

The second parameter is the global best position of the swarm. Let p_g be the best position of all particles.

$$\text{IF } f(x_i) > f(p_g) \rightarrow p_g = x_i \quad i = 1, 2, \dots, M \quad (\text{A.5})$$

which is also simple: if the current position gives a better performance than the current best position of the swarm, then the new best position of the swarm equals the current position.

A.1.4 Updating the Position

The last step of the algorithm is updating the position of each particle. From Kennedy and Eberhart [98], the following equation is used to update the velocity.

$$\vec{v}_i(t) = \vec{v}_i(t-1) + \varphi_1 r_1 [\vec{p}_i - \vec{x}_i(t-1)] + \varphi_2 r_2 [\vec{p}_g - \vec{x}_i(t-1)] \quad (\text{A.6})$$

where φ_1 and φ_2 are constants (equal to 2, based on empirical testing), and r_1 and r_2 are uniformly distributed random numbers between 0 and 1. Clearly, from Eq. A.6, the velocity depends on three parameters: the previous velocity, the distance between the particle's current position and its best position, and the distance between the particle's current position and the global best position.

The velocity is applied in all dimensions; there are n velocities in total for each particle. An additional check is needed in this case; the velocity must be within the bounds of v_{max} and v_{min} .

To update the position, the following simple equation is used:

$$\vec{x}_i(t) = \vec{x}_i(t-1) + \vec{v}_i(t) \quad (\text{A.7})$$

where a unit time step is considered. Normally, Eq. A.7 is of the form $x_i(t) = x_i(t-1) + \Delta x$, where $\Delta x = v_i \Delta t$. If the time increment Δt is assumed to be 1, then Eq. A.7 is obtained.

This whole process is repeated until the maximum number of iterations is reached, or a pre-determined minimum error is obtained.

A.2 Practical Implementation

The practical implementation of the particle swarm algorithm differs slightly from the previously discussed algorithm. The major difference is velocity adjustment [99]: as the number of iterations increases, the maximum velocity decreases. This modification is also called *inertial weight*.

A.2.1 Maximum and Minimum Velocity

The maximum and minimum velocities are defined according to the boundaries of each variable. Let $b_{i,max}$ be the upper boundary for variable a_i , and $b_{i,min}$ the lower boundary for the same variable. Then the maximum and minimum velocities are defined as:

$$v_{i,max} = 2(b_{i,max} - b_{i,min}) \quad (\text{A.8})$$

$$v_{i,min} = -2(b_{i,max} - b_{i,min}) \quad (\text{A.9})$$

where $i = 1, 2, \dots, M$. The constant 2 used in the equations is a general starting point. It may be necessary to modify this value to obtain better performance of the algorithm.

A.2.2 Inertial Weight

The equation for the velocity is modified to reduce the velocity as the number of iterations increases. This prevents the particle from oscillating around the optimum point. The previous velocity is multiplied by the inertial weight w , where w is defined

as:

$$w = (w_1 - w_2) \times \frac{t_{max} - t}{t_{max}} + w_2 \quad (\text{A.10})$$

where t is the current iteration and t_{max} is the maximum number of iterations. From empirical data, the best results are achieved when $w_1 = 0.9$ and $w_2 = 0.4$ [99].